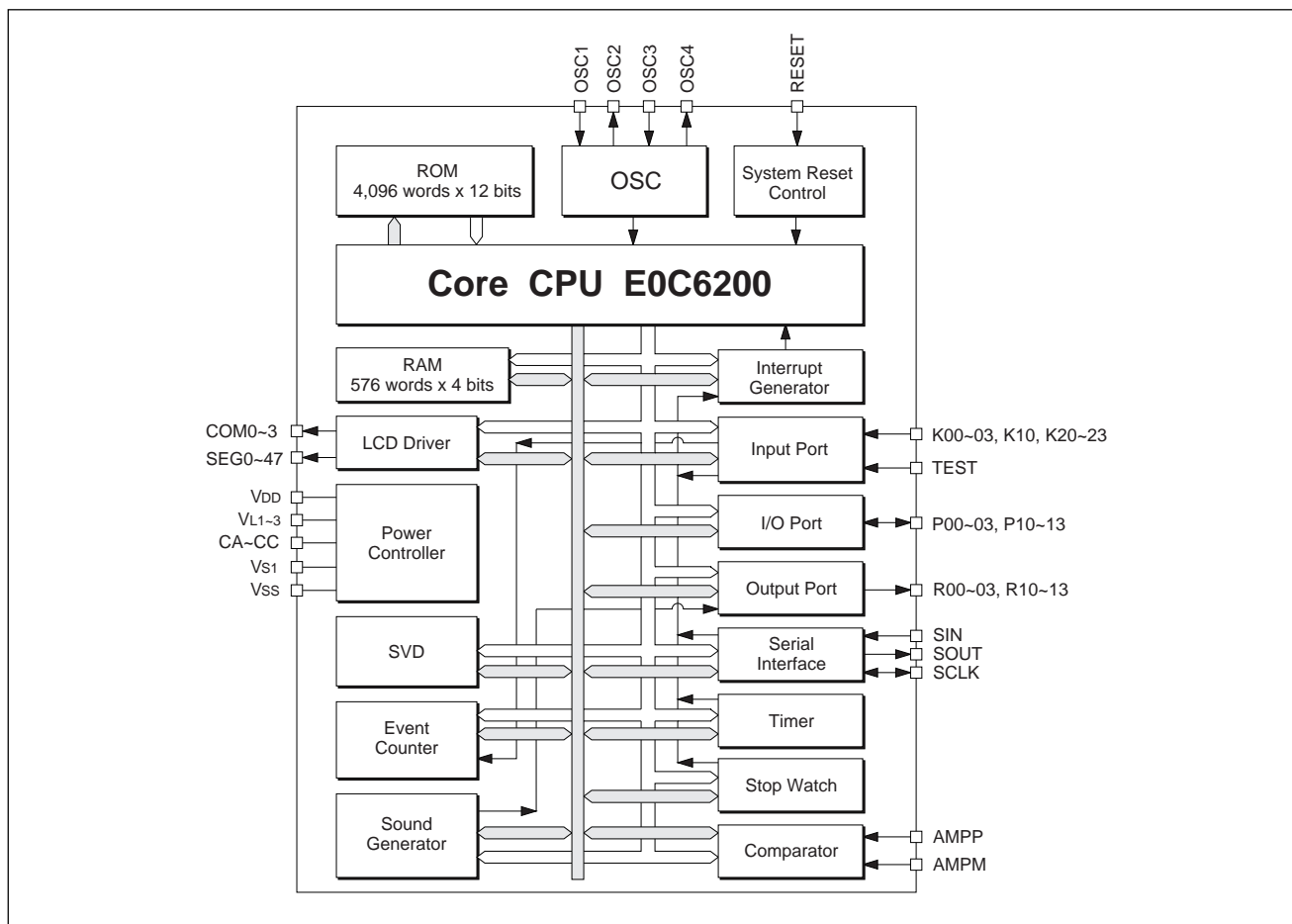
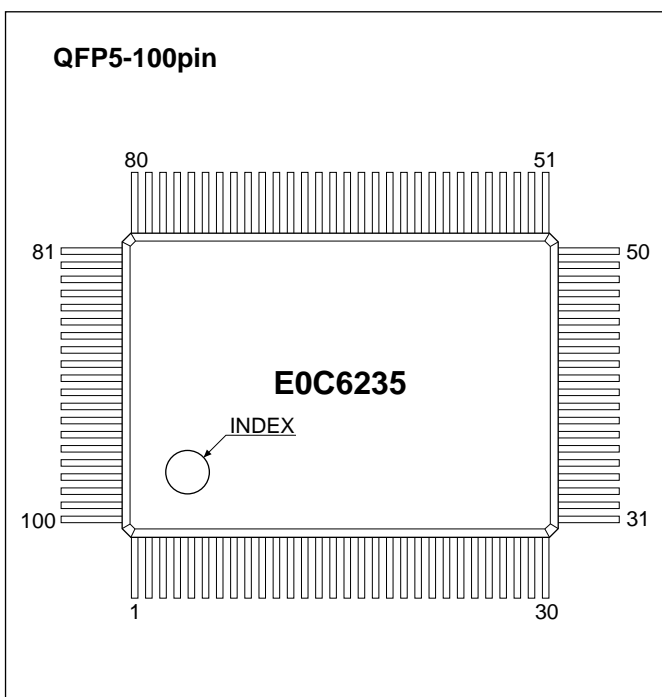


■ BLOCK DIAGRAM

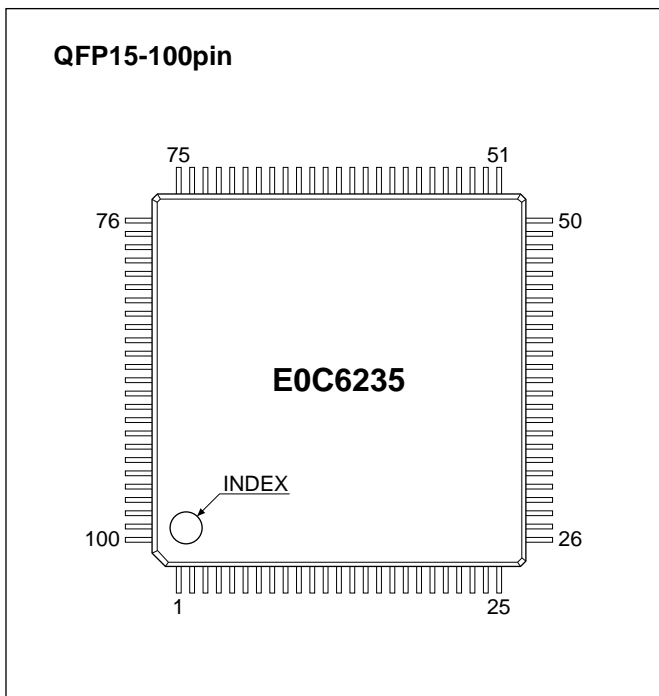


■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	26	SEG24	51	SEG0	76	P10
2	COM0	27	TEST	52	AMPP	77	R03
3	SEG47	28	SEG23	53	AMPM	78	R02
4	SEG46	29	SEG22	54	K23	79	R01
5	SEG45	30	SEG21	55	K22	80	R00
6	SEG44	31	SEG20	56	K21	81	R12
7	SEG43	32	SEG19	57	K20	82	R11
8	SEG42	33	SEG18	58	K10	83	R10
9	SEG41	34	SEG17	59	K03	84	R13
10	SEG40	35	SEG16	60	K02	85	Vss
11	SEG39	36	SEG15	61	K01	86	RESET
12	SEG38	37	SEG14	62	K00	87	OSC4
13	SEG37	38	SEG13	63	SIN	88	OSC3
14	SEG36	39	SEG12	64	SOUT	89	Vs1
15	SEG35	40	SEG11	65	N.C.	90	OSC2
16	SEG34	41	SEG10	66	SCLK	91	OSC1
17	SEG33	42	SEG9	67	P03	92	VDD
18	SEG32	43	SEG8	68	P02	93	VL3
19	SEG31	44	SEG7	69	P01	94	VL2
20	SEG30	45	SEG6	70	P00	95	VL1
21	SEG29	46	SEG5	71	N.C.	96	CA
22	SEG28	47	SEG4	72	N.C.	97	CB
23	SEG27	48	SEG3	73	P13	98	CC
24	SEG26	49	SEG2	74	P12	99	COM3
25	SEG25	50	SEG1	75	P11	100	COM2

N.C. = No Connection



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG47	26	SEG23	51	AMPP	76	R02
2	SEG46	27	SEG22	52	AMPM	77	R01
3	SEG45	28	SEG21	53	K23	78	R00
4	SEG44	29	SEG20	54	K22	79	R12
5	SEG43	30	SEG19	55	K21	80	R11
6	SEG42	31	SEG18	56	K20	81	R10
7	SEG41	32	SEG17	57	K10	82	R13
8	SEG40	33	SEG16	58	K03	83	Vss
9	SEG39	34	SEG15	59	K02	84	RESET
10	SEG38	35	SEG14	60	K01	85	OSC4
11	SEG37	36	SEG13	61	K00	86	OSC3
12	SEG36	37	SEG12	62	SIN	87	Vs1
13	SEG35	38	N.C.	63	SOUT	88	OSC2
14	SEG34	39	SEG11	64	N.C.	89	OSC1
15	SEG33	40	SEG10	65	SCLK	90	VDD
16	SEG32	41	SEG9	66	N.C.	91	VL3
17	SEG31	42	SEG8	67	P03	92	VL2
18	SEG30	43	SEG7	68	P02	93	VL1
19	SEG29	44	SEG6	69	P01	94	CA
20	SEG28	45	SEG5	70	P00	95	CB
21	SEG27	46	SEG4	71	P13	96	CC
22	SEG26	47	SEG3	72	P12	97	COM3
23	SEG25	48	SEG2	73	P11	98	COM2
24	SEG24	49	SEG1	74	P10	99	COM1
25	TEST	50	SEG0	75	R03	100	COM0

N.C. = No Connection

PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-100	QFP15-100		
VDD	92	90	I	Power source (+) terminal
VSS	85	83	I	Power source (-) terminal
Vs1	89	87	O	Oscillation and internal logic system regulated voltage output terminal
VL1	95	93	O	LCD system regulated voltage output terminal (approx. -1.05 V)
VL2	94	92	O	LCD system booster output terminal (VL1 x 2)
VL3	93	91	O	LCD system booster output terminal (VL1 x 3)
CA-CC	96-98	94-96	-	Booster capacitor connecting terminal
OSC1	91	89	I	Crystal oscillation input terminal
OSC2	90	88	O	Crystal oscillation output terminal
OSC3	88	86	I	Ceramic or CR oscillation input terminal (Switchable by mask option, 62A35 only)
OSC4	87	85	O	Ceramic or CR oscillation output terminal (Switchable by mask option, 62A35 only)
K00-K03, K10 K20-K23	54-62	53-61	I	Input terminal
P00-P03 P10-P13	67-70 73-76	67-74	I/O	I/O terminal
R00-R03	77-80	75-78	O	Output terminal
R10	83	81	O	Output terminal (DC or BZ output may be selected by mask option)
R13	84	82	O	Output terminal (DC or BZ output may be selected by mask option)
R11	82	80	O	Output terminal (DC or SIOF output may be selected by mask option)
R12	81	79	O	Output terminal (DC or FOUT output may be selected by mask option)
SIN	63	62	I	Serial interface input terminal
SOUT	64	63	O	Serial interface output terminal
SCLK	66	65	I/O	Serial interface clock input/output terminal
AMPP	52	51	I	Analog comparator non-inverted input terminal
AMPM	53	52	I	Analog comparator inverted input terminal
SEG0-47	3-26, 28-51	1-24, 26-50	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0-3	1, 2, 99, 100	97-100	O	LCD common output terminal
RESET	86	84	I	Initial reset input terminal
TEST	27	25	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

E0C6235/62A35

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-5.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _{Iosc}	V _{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI _{VSS}	10	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *2	P _D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*2: In case of plastic package (QFP5-100pin, QFP15-100pin).

E0C62L35

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-2.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _{Iosc}	V _{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI _{VSS}	10	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *2	P _D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*2: In case of plastic package (QFP5-100pin, QFP15-100pin).

● Recommended Operating Conditions

E0C6235

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-3.0	-1.8	V
Oscillation frequency	fosc1	Either one is selected	—	32.768	—	kHz
			—	38.400	—	

E0C62L35

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-1.7	-1.5	-1.1	V
		V _{DD} =0V, With software control *1	-1.7	-1.5	-0.9 *2	V
		V _{DD} =0V, When the analog comparator is used	-1.7	-1.5	-1.2	V
Oscillation frequency	fosc1	Either one is selected	—	32.768	—	kHz
			—	38.400	—	

*1: When switching to heavy load protection mode.

*2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C62A35

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-3.0	-2.2	V
Oscillation frequency (1)	fosc1	Either one is selected	—	32.768	—	kHz
			—	38.400	—	
Oscillation frequency (2)	fosc3	duty 50±5%	50	500	600	kHz

● DC Characteristics

E0C6235/62A35

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{osc1}=32.768kHz, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00-03, K10, K20-23 P00-03, P10-13, SIN	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	SCLK, RESET, TEST	0.1•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00-03, K10, K20-23 P00-03, P10-13, SIN	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	SCLK, RESET, TEST	V _{SS}		0.9•V _{SS}	V
High level input current (1)	I _{IH1}	V _{IH1} =0V No pull down resistor K00-03, K10, K20-23 P00-03, P10-13, SIN, SCLK AMPP, AMPM, RESET	0		0.5	μA
High level input current (2)	I _{IH2}	V _{IH2} =0V With pull down resistor K00-03, K10, K20-23 SIN, SCLK	4		16	μA
High level input current (3)	I _{IH3}	V _{IH3} =0V With pull down resistor P00-03, P10-13 RESET, TEST	25		100	μA
Low level input current	I _{IL}	V _{IL} =V _{SS} K00-03, K10, K20-23 P00-03, P10-13, SIN, SCLK AMPP, AMPM, RESET, TEST	-0.5		0	μA
High level output current (1)	I _{OH1}	V _{OH1} =0.1•V _{SS} R10, R11, R13			-1.8	mA
High level output current (2)	I _{OH2}	V _{OH2} =0.1•V _{SS} R00-03, R12, P00-03, P10-13 SOUT, SCLK			-0.9	mA
Low level output current (1)	I _{OL1}	V _{OL1} =0.9•V _{SS} R10, R11, R13	6.0			mA
Low level output current (2)	I _{OL2}	V _{OL2} =0.9•V _{SS} R00-03, R12, P00-03, P10-13 SOUT, SCLK	3.0			mA
Common output current	I _{OH3}	V _{OH3} =-0.05V COM0-COM3			-3	μA
	I _{OL3}	V _{OL3} =V _{L3} +0.05V	3			μA
Segment output current (during LCD output)	I _{OH4}	V _{OH4} =-0.05V SEG0-SEG47			-3	μA
	I _{OL4}	V _{OL4} =V _{L3} +0.05V	3			μA
Segment output current (during DC output)	I _{OH5}	V _{OH5} =0.1•V _{SS} SEG0-SEG47			-200	μA
	I _{OL5}	V _{OL5} =0.9•V _{SS}	200			μA

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(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{osc1}=32.768kHz, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00-03, K10, K20-23 P00-03, P10-13, SIN	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	SCLK, RESET, TEST	0.1•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00-03, K10, K20-23 P00-03, P10-13, SIN	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	SCLK, RESET, TEST	V _{SS}		0.9•V _{SS}	V
High level input current (1)	I _{IH1}	V _{IH1} =0V No pull down resistor K00-03, K10, K20-23 P00-03, P10-13, SIN, SCLK AMPP, AMPM, RESET	0		0.5	μA
High level input current (2)	I _{IH2}	V _{IH2} =0V With pull down resistor K00-03, K10, K20-23 SIN, SCLK	2		10	μA
High level input current (3)	I _{IH3}	V _{IH3} =0V With pull down resistor P00-03, P10-13 RESET, TEST	12		60	μA
Low level input current	I _{IL}	V _{IL} =V _{SS} K00-03, K10, K20-23 P00-03, P10-13, SIN, SCLK AMPP, AMPM, RESET, TEST	-0.5		0	μA
High level output current (1)	I _{OH1}	V _{OH1} =0.1•V _{SS} R10, R11, R13			-300	μA
High level output current (2)	I _{OH2}	V _{OH2} =0.1•V _{SS} R00-03, R12, P00-03, P10-13 SOUT, SCLK			-150	μA
Low level output current (1)	I _{OL1}	V _{OL1} =0.9•V _{SS} R10, R11, R13	1,400			μA
Low level output current (2)	I _{OL2}	V _{OL2} =0.9•V _{SS} R00-03, R12, P00-03, P10-13 SOUT, SCLK	700			μA
Common output current	I _{OH3}	V _{OH3} =-0.05V COM0-COM3			-3	μA
	I _{OL3}	V _{OL3} =V _{L3} +0.05V	3			μA
Segment output current (during LCD output)	I _{OH4}	V _{OH4} =-0.05V SEG0-SEG47			-3	μA
	I _{OL4}	V _{OL4} =V _{L3} +0.05V	3			μA
Segment output current (during DC output)	I _{OH5}	V _{OH5} =0.1•V _{SS} SEG0-SEG47			-100	μA
	I _{OL5}	V _{OL5} =0.9•V _{SS}	100			μA

● Analog Circuit Characteristics and Current Consumption

E0C6235 (Normal Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, Vs1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.9	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
BLD voltage *1	VB0	BLC="0"	-2.35	-2.20	-2.05	V
	VB1	BLC="1"	-2.40	-2.25	-2.10	V
	VB2	BLC="2"	-2.45	-2.30	-2.15	V
	VB3	BLC="3"	-2.50	-2.35	-2.20	V
	VB4	BLC="4"	-2.55	-2.40	-2.25	V
	VB5	BLC="5"	-2.60	-2.45	-2.30	V
	VB6	BLC="6"	-2.65	-2.50	-2.35	V
VB7	BLC="7"	-2.70	-2.55	-2.40	V	
BLD circuit response time	tB				100	μS
Sub-BLD voltage	VBS		-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	tBS				100	μS
Analog comparator input voltage	VIP	Noninverted input (AMPP)	Vss+0.3		VDD-0.9	V
	VIM	Inverted input (AMPM)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tAMP	VIP=-1.5V, VIM=VIP±15mV			3	mS
Current consumption	IOP	During HALT	Without panel load		1.8	4.0
		During operation *2				

*1: The relationships among VB0-VB7 are VB0>VB1>VB2>...>VB5>VB6>VB7.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C6235 (Heavy Load Protection Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, Vs1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.9	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
BLD voltage *1	VB0	BLC="0"	-2.35	-2.20	-2.05	V
	VB1	BLC="1"	-2.40	-2.25	-2.10	V
	VB2	BLC="2"	-2.45	-2.30	-2.15	V
	VB3	BLC="3"	-2.50	-2.35	-2.20	V
	VB4	BLC="4"	-2.55	-2.40	-2.25	V
	VB5	BLC="5"	-2.60	-2.45	-2.30	V
	VB6	BLC="6"	-2.65	-2.50	-2.35	V
VB7	BLC="7"	-2.70	-2.55	-2.40	V	
BLD circuit response time	tB				100	μS
Sub-BLD voltage	VBS		-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	tBS				100	μS
Analog comparator input voltage	VIP	Noninverted input (AMPP)	Vss+0.3		VDD-0.9	V
	VIM	Inverted input (AMPM)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tAMP	VIP=-1.5V, VIM=VIP±15mV			3	mS
Current consumption	IOP	During HALT	Without panel load		35	90
		During operation *2				

*1: The relationships among VB0-VB7 are VB0>VB1>VB2>...>VB5>VB6>VB7.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

E0C62L35 (Normal Mode)

(Unless otherwise specified: VDD=0V, VSS=-1.5V, fosc1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.9	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
BLD voltage *1	VB0	BLC="0"	-1.15	-1.05	-0.95	V
	VB1	BLC="1"	-1.20	-1.10	-1.00	V
	VB2	BLC="2"	-1.25	-1.15	-1.05	V
	VB3	BLC="3"	-1.30	-1.20	-1.10	V
	VB4	BLC="4"	-1.35	-1.25	-1.15	V
	VB5	BLC="5"	-1.40	-1.30	-1.20	V
	VB6	BLC="6"	-1.45	-1.35	-1.25	V
	VB7	BLC="7"	-1.50	-1.40	-1.30	V
BLD circuit response time	tB				100	μS
Sub-BLD voltage	VBS		-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	tBS				100	μS
Analog comparator input voltage	VIP	Noninverted input (AMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (AMPM)				
Analog comparator offset voltage	VOF				20	mV
Analog comparator response time	tAMP	VIP=-1.1V, VIM=VIP±30mV			3	mS
Current consumption	IOP	During HALT		1.5	3.0	μA
		During operation *2	Without panel load	5.0	8.0	μA

*1: The relationships among VB0-VB7 are VB0>VB1>VB2>...VB5>VB6>VB7.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C62L35 (Heavy Load Protection Mode)

(Unless otherwise specified: VDD=0V, VSS=-1.5V, fosc1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL3 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.85	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.85	V
BLD voltage *1	VB0	BLC="0"	-1.15	-1.05	-0.95	V
	VB1	BLC="1"	-1.20	-1.10	-1.00	V
	VB2	BLC="2"	-1.25	-1.15	-1.05	V
	VB3	BLC="3"	-1.30	-1.20	-1.10	V
	VB4	BLC="4"	-1.35	-1.25	-1.15	V
	VB5	BLC="5"	-1.40	-1.30	-1.20	V
	VB6	BLC="6"	-1.45	-1.35	-1.25	V
	VB7	BLC="7"	-1.50	-1.40	-1.30	V
BLD circuit response time	tB				100	μS
Sub-BLD voltage	VBS		-1.30	-1.20	-1.10	V
Sub-BLD circuit response time	tBS				100	μS
Analog comparator input voltage	VIP	Noninverted input (AMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (AMPM)				
Analog comparator offset voltage	VOF				20	mV
Analog comparator response time	tAMP	VIP=-1.1V, VIM=VIP±30mV			3	mS
Current consumption	IOP	During HALT		3.0	7.0	μA
		During operation *2	Without panel load	10.0	18.0	μA

*1: The relationships among VB0-VB7 are VB0>VB1>VB2>...VB5>VB6>VB7.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

E0C62A35 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, T_a=25°C, C_G=25pF, V_{S1}/V_{L1}-V_{L3} are internal voltage, C₁-C₆=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load)	2•V _{L1} -0.1		2•V _{L1} ×0.9	V
	V _{L3}	Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load)	3•V _{L1} -0.1		3•V _{L1} ×0.9	V
BLD voltage *1	V _{B0}	BLC="0"	-2.35	-2.20	-2.05	V
	V _{B1}	BLC="1"	-2.40	-2.25	-2.10	V
	V _{B2}	BLC="2"	-2.45	-2.30	-2.15	V
	V _{B3}	BLC="3"	-2.50	-2.35	-2.20	V
	V _{B4}	BLC="4"	-2.55	-2.40	-2.25	V
	V _{B5}	BLC="5"	-2.60	-2.45	-2.30	V
	V _{B6}	BLC="6"	-2.65	-2.50	-2.35	V
	V _{B7}	BLC="7"	-2.70	-2.55	-2.40	V
BLD circuit response time	t _B				100	μS
Sub-BLD voltage	V _{BS}		-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t _{BS}				100	μS
Analog comparator input voltage	V _{IP}	Noninverted input (AMPP)	V _{SS} +0.3		V _{DD} -0.9	V
	V _{IM}	Inverted input (AMPM)				
Analog comparator offset voltage	V _{OF}				10	mV
Analog comparator response time	t _{AMP}	V _{IP} =-1.5V, V _{IM} =V _{IP} ±15mV			3	mS
Current consumption	I _{OP}	During HALT		2.0	5.0	μA
		During operation at 32kHz *2	Without panel load	8.0	15	μA
		During operation at 500kHz *2		130	300	μA

*1: The relationships among V_{B0}-V_{B7} are V_{B0}>V_{B1}>V_{B2}>...>V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit, sub-BLD circuit and analog comparator are in the OFF status.

E0C62A35 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, T_a=25°C, C_G=25pF, V_{S1}/V_{L1}-V_{L3} are internal voltage, C₁-C₆=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (without panel load)	2•V _{L1} -0.1		2•V _{L1} ×0.9	V
	V _{L3}	Connect 1MΩ load resistor between V _{DD} and V _{L3} (without panel load)	3•V _{L1} -0.1		3•V _{L1} ×0.9	V
BLD voltage *1	V _{B0}	BLC="0"	-2.35	-2.20	-2.05	V
	V _{B1}	BLC="1"	-2.40	-2.25	-2.10	V
	V _{B2}	BLC="2"	-2.45	-2.30	-2.15	V
	V _{B3}	BLC="3"	-2.50	-2.35	-2.20	V
	V _{B4}	BLC="4"	-2.55	-2.40	-2.25	V
	V _{B5}	BLC="5"	-2.60	-2.45	-2.30	V
	V _{B6}	BLC="6"	-2.65	-2.50	-2.35	V
	V _{B7}	BLC="7"	-2.70	-2.55	-2.40	V
BLD circuit response time	t _B				100	μS
Sub-BLD voltage	V _{BS}		-2.55	-2.40	-2.25	V
Sub-BLD circuit response time	t _{BS}				100	μS
Analog comparator input voltage	V _{IP}	Noninverted input (AMPP)	V _{SS} +0.3		V _{DD} -0.9	V
	V _{IM}	Inverted input (AMPM)				
Analog comparator offset voltage	V _{OF}				10	mV
Analog comparator response time	t _{AMP}	V _{IP} =-1.5V, V _{IM} =V _{IP} ±15mV			3	mS
Current consumption	I _{OP}	During HALT		22	40	μA
		During operation at 32kHz *2	Without panel load	28	50	μA
		During operation at 500kHz *2		150	350	μA

*1: The relationships among V_{B0}-V_{B7} are V_{B0}>V_{B1}>V_{B2}>...>V_{B5}>V_{B6}>V_{B7}.

*2: The BLD circuit and sub-BLD circuit are in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6235 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤5sec (V _{SS})	-1.8			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-1.8			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-3.5	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

E0C62L35 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤5sec (V _{SS})	-1.1			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-1.1 to -1.7V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-1.7	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

*1: Items enclosed in parentheses () are those used when operating at heavy load protection mode.

E0C62A35 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤5sec (V _{SS})	-1.8			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-1.8			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-1.8 to -3.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-3.5	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

E0C62A35 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=82kΩ, T_a=25°C)

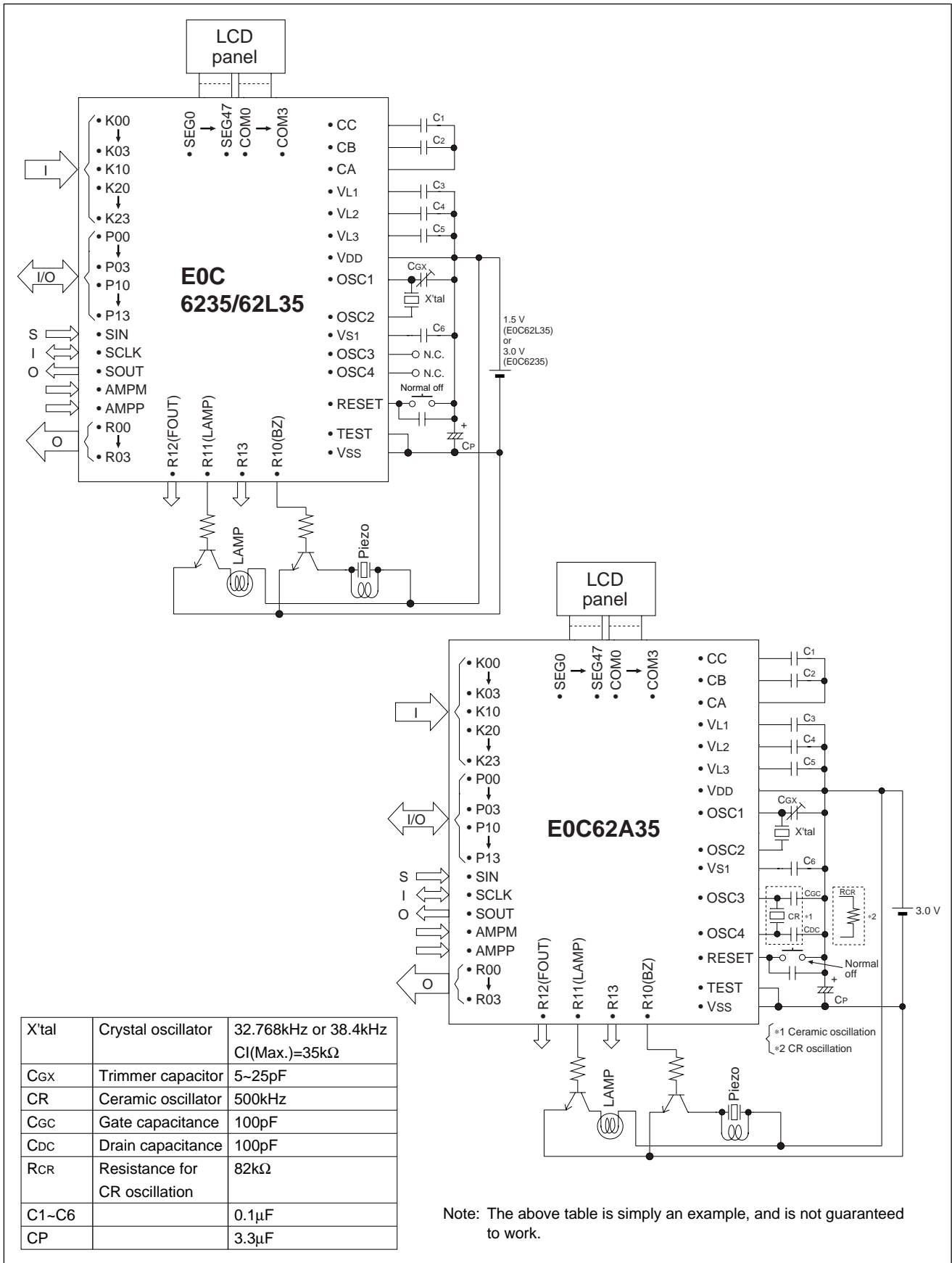
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc3		-30	480kHz	30	%
Oscillation start voltage	V _{sta}	(V _{SS})	-2.2			V
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -3.5V			3	mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-2.2			V

E0C62A35 (Ceramic oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 500kHz, C_{Gc}=C_{Dc}=100pF, T_a=25°C)

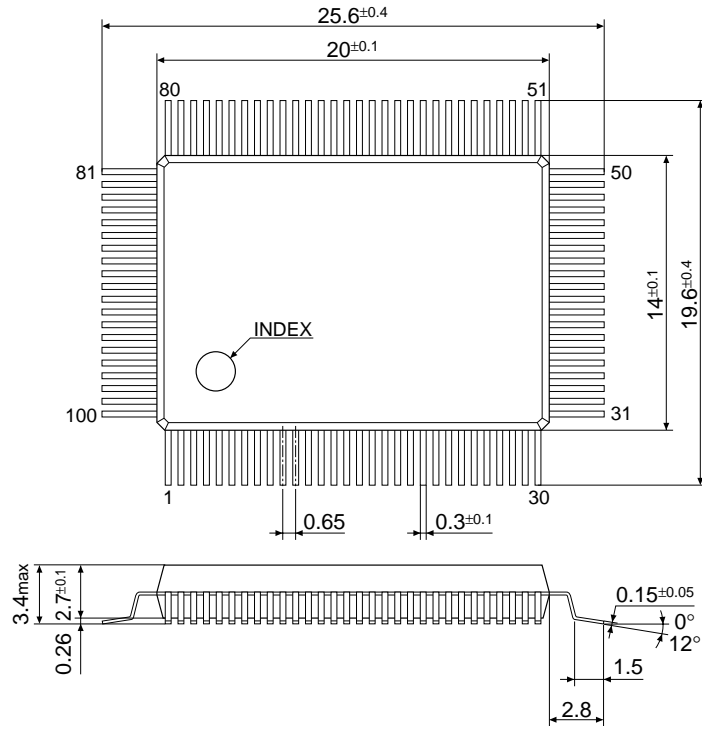
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	(V _{SS})	-2.2			V
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -3.5V			5	mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

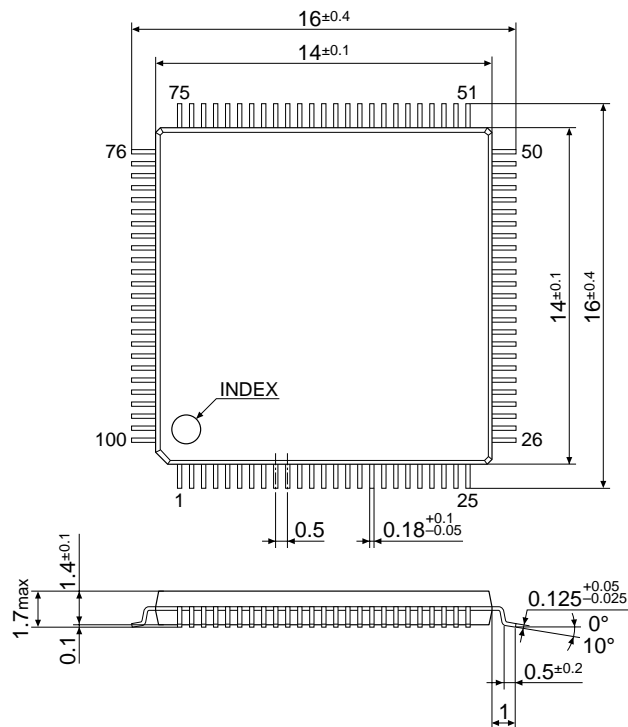


■ PACKAGE DIMENSIONS

Plastic QFP5-100pin



Plastic QFP15-100pin



Unit: mm

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