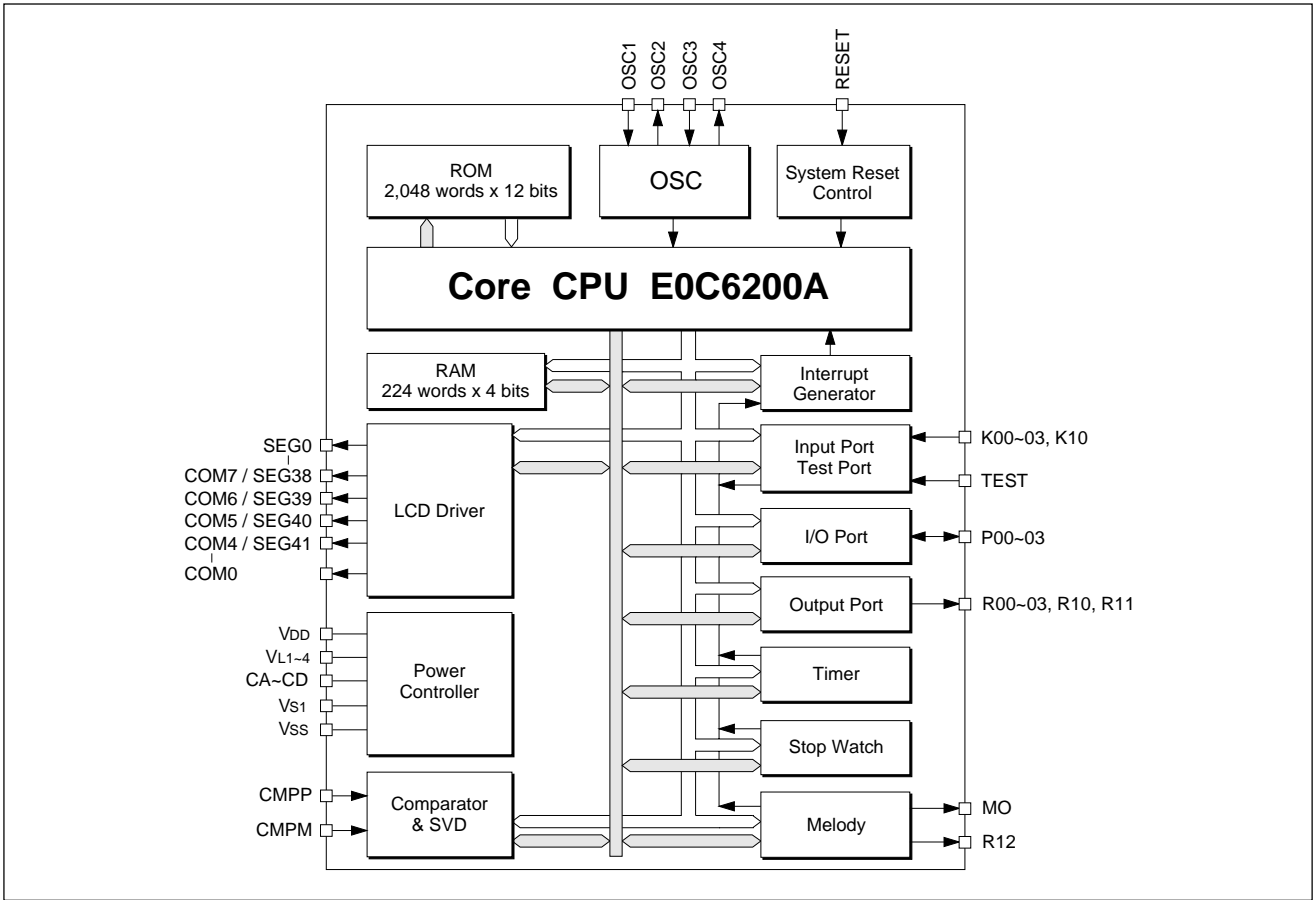
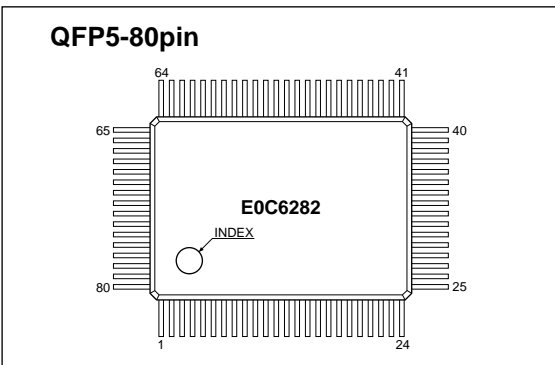


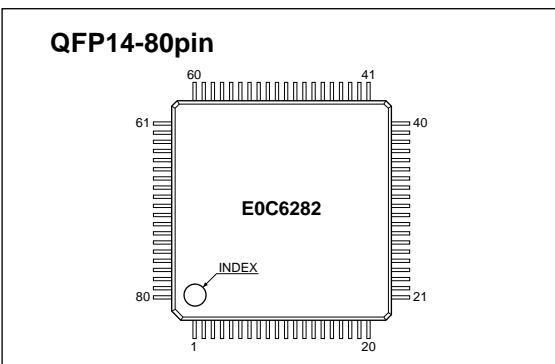
■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	VDD	17	SEG14	33	K02	49	SEG28	65	P01
2	TEST	18	SEG15	34	K01	50	SEG29	66	P00
3	SEG0	19	SEG16	35	K00	51	SEG30	67	CD
4	SEG1	20	SEG17	36	RESET	52	SEG31	68	CC
5	SEG2	21	SEG18	37	CMPP	53	SEG32	69	CB
6	SEG3	22	SEG19	38	CMPP	54	SEG33	70	CA
7	SEG4	23	R03	39	COM3	55	SEG34	71	VL4
8	SEG5	24	R02	40	COM2	56	SEG35	72	VL3
9	SEG6	25	R01	41	COM1	57	SEG36	73	VL2
10	SEG7	26	R00	42	COM0	58	SEG37	74	VL1
11	SEG8	27	MO	43	SEG22	59	SEG38/COM7	75	Vss
12	SEG9	28	R12	44	SEG23	60	SEG39/COM6	76	OSC4
13	SEG10	29	R11	45	SEG24	61	SEG40/COM5	77	OSC3
14	SEG11	30	R10	46	SEG25	62	SEG41/COM4	78	Vs1
15	SEG12	31	K10	47	SEG26	63	P03	79	OSC2
16	SEG13	32	K03	48	SEG27	64	P02	80	OSC1



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG0	17	SEG16	33	K00	49	SEG30	65	CD
2	SEG1	18	SEG17	34	RESET	50	SEG31	66	CC
3	SEG2	19	SEG18	35	CMPP	51	SEG32	67	CB
4	SEG3	20	SEG19	36	CMPP	52	SEG33	68	CA
5	SEG4	21	R03	37	COM3	53	SEG34	69	VL4
6	SEG5	22	R02	38	COM2	54	SEG35	70	VL3
7	SEG6	23	R01	39	COM1	55	SEG36	71	VL2
8	SEG7	24	R00	40	COM0	56	SEG37	72	VL1
9	SEG8	25	MO	41	SEG22	57	SEG38/COM7	73	Vss
10	SEG9	26	R12	42	SEG23	58	SEG39/COM6	74	OSC4
11	SEG10	27	R11	43	SEG24	59	SEG40/COM5	75	OSC3
12	SEG11	28	R10	44	SEG25	60	SEG41/COM4	76	Vs1
13	SEG12	29	K10	45	SEG26	61	P03	77	OSC2
14	SEG13	30	K03	46	SEG27	62	P02	78	OSC1
15	SEG14	31	K02	47	SEG28	63	P01	79	VDD
16	SEG15	32	K01	48	SEG29	64	P00	80	TEST

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-80pin	QFP14-80pin		
VDD	1	79	I	Power source (+) terminal
VSS	75	73	I	Power source (-) terminal
Vs1	78	76	-	Oscillation and internal logic system regulated voltage output terminal
VL1-VL4	71-74	69-72	-	LCD system power source terminal
CA-CD	67-70	65-68	-	LCD system booster capacitor connecting terminal
OSC1	80	78	I	Crystal or CR oscillation input terminal
OSC2	79	77	O	Crystal or CR oscillation output terminal
OSC3	77	75	I	Ceramic or CR oscillation input terminal (62A82 only)
OSC4	76	74	O	Ceramic or CR oscillation output terminal (62A82 only)
K00-K00, K10	32-35, 31	30-33, 29	I	Input terminal
P00-P03	63-66	61-64	I/O	I/O terminal
R00-R03	23-26	21-24	O	Output terminal
R10	30	28	O	Output terminal (FOUT output available by mask option)
R11	29	27	O	Output terminal
R12	28	26	O	Output terminal (Melody inverted output and envelope function available by mask option)
MO	27	25	O	Melody signal output terminal
CMPP	37	35	I	Analog comparator non-inverted input terminal
CMPM	38	36	I	Analog comparator inverted input terminal
SEG0-37	3-22, 43-58	1-20, 41-56	O	LCD segment output terminal (Convertible to DC output by mask option) SEG20 and 21 may be used only when the chip has been supplied
COM0-3	39-42	37-40	O	LCD common output terminal
SEG38-41 COM4-7	59-62	57-60	O	LCD segment output terminal when 1/4 duty is selected LCD common output terminal when 1/8 duty is selected
RESET	36	34	I	Initial reset input terminal
TEST	2	80	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(VDD=0V)

Rating	Symbol	Value	Unit
Supply voltage	VSS	-6.0 to 0.5	V
Input voltage (1)	Vi	VSS - 0.3 to 0.5	V
Input voltage (2)	Viosc	Vs1 - 0.3 to 0.5	V
Permissible total output current *1	ΣIvss	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	-
Permissible dissipation *2	Pd	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).

*2: In case of plastic package (QFP5-80pin, QFP14-80pin).

● Recommended Operating Conditions

E0C6282

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	VSS	VDD=0V	-5.5	-3.0	-2.2	V
Oscillation frequency	fosc1		-	32.768	-	kHz

E0C62L82

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	VSS	VDD=0V	-3.5	-1.5	-1.1	V
		VDD=0V, With software control *1	-3.5	-1.5	-0.9 *2	V
		VDD=0V, When the analog comparator is used	-3.5	-1.5	-1.3	V
Oscillation frequency	fosc1		-	32.768	-	kHz

*1: When switching to heavy load protection mode. The SVD circuit and analog voltage comparator are turned OFF.

*2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C62A82

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	VSS	VDD=0V	-5.5	-3.0	-2.2	V
Oscillation frequency (1)	fosc1		-	32.768	-	kHz
Oscillation frequency (2)	fosc3	duty 50±5%	-	1,000	-	kHz

● DC Characteristics

E0C6282/62A82

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fosc1=32.768kHz, Ta=25°C, Vs1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	VIH1	K00-K03, K10, P00-P03	0.2•Vss		0	V
High level input voltage (2)	VIH2	RESET, TEST	0.10•Vss		0	V
Low level input voltage (1)	VIL1	K00-K03, K10, P00-P03	Vss		0.8•Vss	V
Low level input voltage (2)	VIL2	RESET, TEST	Vss		0.90•Vss	V
High level input current (1)	IiH1	VIH1=0V No pull down resistor	0		0.5	μA
High level input current (2)	IiH2	VIH2=0V With pull down resistor	5		16	μA
High level input current (3)	IiH3	VIH3=0V With pull down resistor	30		100	μA
Low level input current	IiL	VIL=Vss	-0.5		0	μA
High level output current (1)	IoH1	VOH1=0.1•Vss			-1.0	mA
High level output current (2)	IoH2	VOH2=0.1•Vss			-1.0	mA
High level output current (3)	IoH3	VOH3=0.1•Vss			-2.0	mA
Low level output current (1)	IoL1	VOL1=0.9•Vss	3.0			mA
Low level output current (2)	IoL2	VOL2=0.9•Vss	3.0			mA
Low level output current (3)	IoL3	VOL3=0.9•Vss	4.5			mA
Common output current	IoH4	VOH4=-0.05V			-3	μA
1/4 duty	IoL4	VOL4=VL3+0.05V	3			μA
Segment output current	IoH5	VOH5=-0.05V			-3	μA
(during LCD output)1/4 duty	IoL5	VOL5=VL3+0.05V	3			μA
Segment output current	IoH6	VOH6=0.1•Vss			-300	μA
(during DC output) 1/4 duty	IoL6	VOL6=0.9•Vss	300			μA
Common output current	IoH7	VOH7=-0.05V			-3	μA
1/8 duty	IoL7	VOL7=VL4+0.05V	3			μA
Segment output current	IoH8	VOH8=-0.05V			-3	μA
(during LCD output)1/8 duty	IoL8	VOL8=VL4+0.05V	3			μA
Segment output current	IoH9	VOH9=0.1•Vss			-300	μA
(during DC output) 1/8 duty	IoL9	VOL9=0.9•Vss	300			μA

E0C62L82

(Unless otherwise specified: VDD=0V, VSS=-1.5V, fosc1=32.768kHz, Ta=25°C, Vs1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	VIH1	K00-K03, K10, P00-P03	0.2•Vss		0	V
High level input voltage (2)	VIH2	RESET, TEST	0.10•Vss		0	V
Low level input voltage (1)	VIL1	K00-K03, K10, P00-P03	Vss		0.8•Vss	V
Low level input voltage (2)	VIL2	RESET, TEST	Vss		0.90•Vss	V
High level input current (1)	IiH1	VIH1=0V No pull down resistor	0		0.5	μA
High level input current (2)	IiH2	VIH2=0V With pull down resistor	2.0		10	μA
High level input current (3)	IiH3	VIH3=0V With pull down resistor	9.0		60	μA
Low level input current	IiL	VIL=Vss	-0.5		0	μA
High level output current (1)	IoH1	VOH1=0.1•Vss			-450	μA
High level output current (2)	IoH2	VOH2=0.1•Vss			-200	μA
High level output current (3)	IoH3	VOH3=0.1•Vss			-0.8	mA
High level output current (4)	IoH4	VOH4=0.1•Vss When envelope is used			-0.4	mA
Low level output current (1)	IoL1	VOL1=0.9•Vss	1,300			μA
Low level output current (2)	IoL2	VOL2=0.9•Vss	700			μA
Low level output current (3)	IoL3	VOL3=0.9•Vss	1.5			mA
Low level output current (4)	IoL4	VOL4=0.9•Vss When envelope is used	750			μA
Common output current	IoH5	VOH5=-0.05V			-3	μA
1/4 duty	IoL5	VOL5=VL3+0.05V	3			μA
Segment output current	IoH6	VOH6=-0.05V			-3	μA
(during LCD output)1/4 duty	IoL6	VOL6=VL3+0.05V	3			μA
Segment output current	IoH7	VOH7=0.1•Vss			-100	μA
(during DC output) 1/4 duty	IoL7	VOL7=0.9•Vss	130			μA
Common output current	IoH8	VOH8=-0.05V			-3	μA
1/8 duty	IoL8	VOL8=VL4+0.05V	3			μA
Segment output current	IoH9	VOH9=-0.05V			-3	μA
(during LCD output)1/8 duty	IoL9	VOL9=VL4+0.05V	3			μA
Segment output current	IoH10	VOH10=0.1•Vss			-100	μA
(during DC output) 1/8 duty	IoL10	VOL10=0.9•Vss	130			μA

● Analog Circuit Characteristics and Current Consumption

E0C6282 (Normal Operating Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fosc1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	0.5•VL2 -0.1		0.5•VL2 +0.1	V	
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	-2.25	-2.10	-1.95	V	
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V	
	VL4	Connect 1MΩ load resistor between VDD and VL4 (without panel load)	4•VL1 -0.1		4•VL1 ×0.9	V	
SVD voltage	VSVD		-2.55	-2.40	-2.25	V	
SVD circuit response time	tsVD				100	μS	
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V	
	VIM	Inverted input (CMPM)					
Analog comparator offset voltage	VOF				10	mV	
Analog comparator response time	tcMP	VIP=-1.5V, VIM=VIP±15mV			1	mS	
Current consumption	IOP1	During HALT *1	Without panel load		1.5	3.0	μA
		During operation *1	OSC1 is crystal oscillation		4.0	7.0	μA
	IOP2	During HALT *1	Without panel load		6.0	10.5	μA
		During operation *1	OSC1 is CR oscillation		8.7	14.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C6282 (Heavy Load Protection Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fosc1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	0.5•VL2 -0.1		0.5•VL2 +0.1	V	
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	-2.25	-2.10	-1.95	V	
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V	
	VL4	Connect 1MΩ load resistor between VDD and VL4 (without panel load)	4•VL1 -0.1		4•VL1 ×0.9	V	
SVD voltage	VSVD		-2.55	-2.40	-2.25	V	
SVD circuit response time	tsVD				100	μS	
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V	
	VIM	Inverted input (CMPM)					
Analog comparator offset voltage	VOF				10	mV	
Analog comparator response time	tcMP	VIP=-1.5V, VIM=VIP±15mV			1	mS	
Current consumption	IOP1	During HALT *1	Without panel load		11.5	33.0	μA
		During operation *1	OSC1 is crystal oscillation		14.0	37.0	μA
	IOP2	During HALT *1	Without panel load		16.0	40.5	μA
		During operation *1	OSC1 is CR oscillation		18.7	44.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62L82 (Normal Operating Mode)

(Unless otherwise specified: VDD=0V, VSS=-1.5V, fosc1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V	
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.9	V	
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V	
	VL4	Connect 1MΩ load resistor between VDD and VL4 (without panel load)	4•VL1 -0.1		4•VL1 ×0.9	V	
SVD voltage	VSVD		-1.30	-1.20	-1.10	V	
SVD circuit response time	tsVD				100	μS	
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V	
	VIM	Inverted input (CMPM)					
Analog comparator offset voltage	VOF				20	mV	
Analog comparator response time	tcMP	VIP=-1.1V, VIM=VIP±30mV			1	mS	
Current consumption	IOP1	During HALT *1	Without panel load		1.5	3.0	μA
		During operation *1	OSC1 is crystal oscillation		4.0	7.0	μA
	IOP2	During HALT *1	Without panel load		6.0	10.5	μA
		During operation *1	OSC1 is CR oscillation		8.7	14.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62L82 (Heavy Load Protection Mode)

(Unless otherwise specified: VDD=0V, VSS=-1.5V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V	
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.85	V	
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.85	V	
	VL4	Connect 1MΩ load resistor between VDD and VL4 (without panel load)	4•VL1 -0.1		4•VL1 ×0.85	V	
SVD voltage	VSVD		-1.30	-1.20	-1.10	V	
SVD circuit response time	tsVD				100	μS	
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V	
	VIM	Inverted input (CMPP)					
Analog comparator offset voltage	VOF				20	mV	
Analog comparator response time	tCMP	VIP=-1.1V, VIM=VIP±30mV			1	mS	
Current consumption	IOP1	During HALT *1	Without panel load		2.5	6.0	μA
		During operation *1	OSC1 is crystal oscillation		7.0	12.0	μA
	IOP2	During HALT *1	Without panel load		11.5	20.5	μA
		During operation *1	OSC1 is CR oscillation		16.5	27.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A82 (Normal Operating Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	0.5•VL2 -0.1		0.5•VL2 +0.1	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	-2.25	-2.10	-1.95	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
	VL4	Connect 1MΩ load resistor between VDD and VL4 (without panel load)	4•VL1 -0.1		4•VL1 ×0.9	V
SVD voltage	VSVD		-2.55	-2.40	-2.25	V
SVD circuit response time	tsVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (CMPP)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tCMP	VIP=-1.5V, VIM=VIP±15mV			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	1.70	3.0	μA
		During operation at 32kHz *1	OSC1 is crystal oscillation	4.0	7.0	μA
		During operation at 1MHz *2		150.0	300.0	μA
	IOP2	During HALT *1	Without panel load	30	60	μA
		During operation at 32kHz *1	OSC1 is CR oscillation	30	60	μA
		During operation at 1MHz *2		160	300	μA

*1: The OSC3 circuit, SVD circuit and analog voltage comparator are turned OFF.

*2: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A82 (Heavy Load Protection Mode)

(Unless otherwise specified: VDD=0V, VSS=-3.0V, fOSC1=32.768kHz, Ta=25°C, CG=25pF, VS1/VL1-VL4 are internal voltage, C1-C6=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1MΩ load resistor between VDD and VL1 (without panel load)	0.5•VL2 -0.1		0.5•VL2 +0.1	V
	VL2	Connect 1MΩ load resistor between VDD and VL2 (without panel load)	-2.25	-2.10	-1.95	V
	VL3	Connect 1MΩ load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
	VL4	Connect 1MΩ load resistor between VDD and VL4 (without panel load)	4•VL1 -0.1		4•VL1 ×0.9	V
SVD voltage	VSVD		-2.55	-2.40	-2.25	V
SVD circuit response time	tsVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (CMPP)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tCMP	VIP=-1.5V, VIM=VIP±15mV			1	mS
Current consumption	IOP1	During HALT *1	Without panel load	11.7	33.0	μA
		During operation at 32kHz *1	OSC1 is crystal oscillation	14.0	37.0	μA
		During operation at 1MHz *2		160.0	330.0	μA
	IOP2	During HALT *1	Without panel load	40	90	μA
		During operation at 32kHz *1	OSC1 is CR oscillation	40	90	μA
		During operation at 1MHz *2		200	420	μA

*1: The OSC3 circuit, SVD circuit and analog voltage comparator are turned OFF.

*2: The SVD circuit and analog voltage comparator are turned OFF.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6282/62A82 (OSC1 Crystal oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_i=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤3sec (V _{SS})	-2.2			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-2.2			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	40			ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-5.5	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

E0C62L82 (OSC1 Crystal oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_i=35kΩ), C_G=25pF, C_D=built-in, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	t _{sta} ≤3sec (V _{SS})	-1.1			V
Oscillation stop voltage	V _{stp}	t _{stp} ≤10sec (V _{SS})	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C _D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V _{SS} =-1.1 to -3.5V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C _G	C _G =5 to 25pF	40			ppm
Harmonic oscillation start voltage	V _{hho}	(V _{SS})			-3.5	V
Permitted leak resistance	R _{leak}	Between OSC1 and V _{DD} , V _{SS}	200			MΩ

*1: Items enclosed in parentheses () are those used when operating at heavy load protection mode.

E0C6282/62A82 (OSC1 CR oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=850kΩ, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc1		-20	32.768kHz	20	%
Oscillation start voltage	V _{sta}	(V _{SS})	-2.2			V
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -5.5V		3		mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-2.2			V

E0C62L82 (OSC1 CR oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, R_{CR}=850kΩ, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc1		-20	32.768kHz	20	%
Oscillation start voltage	V _{sta}	(V _{SS})	-0.9			V
Oscillation start time	t _{sta}	V _{SS} =0.9 to -3.5V		3		mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-0.9			V

E0C62A82 (OSC3 CR oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=35kΩ, T_a=25°C)

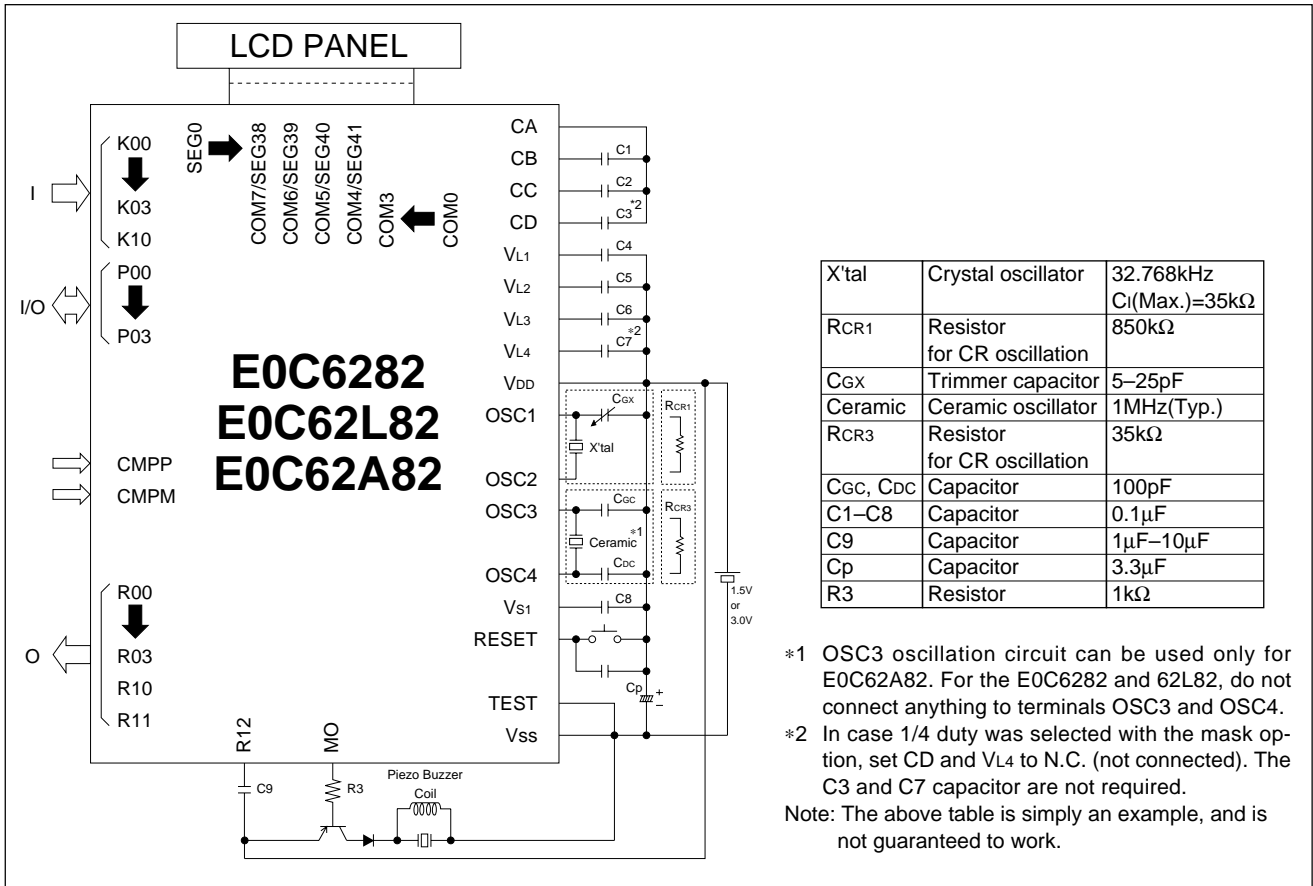
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc3		-30	1MHz	30	%
Oscillation start voltage	V _{sta}	(V _{SS})	-2.2			V
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -5.5V			3	mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-2.2			V

E0C62A82 (OSC1 Ceramic oscillation)

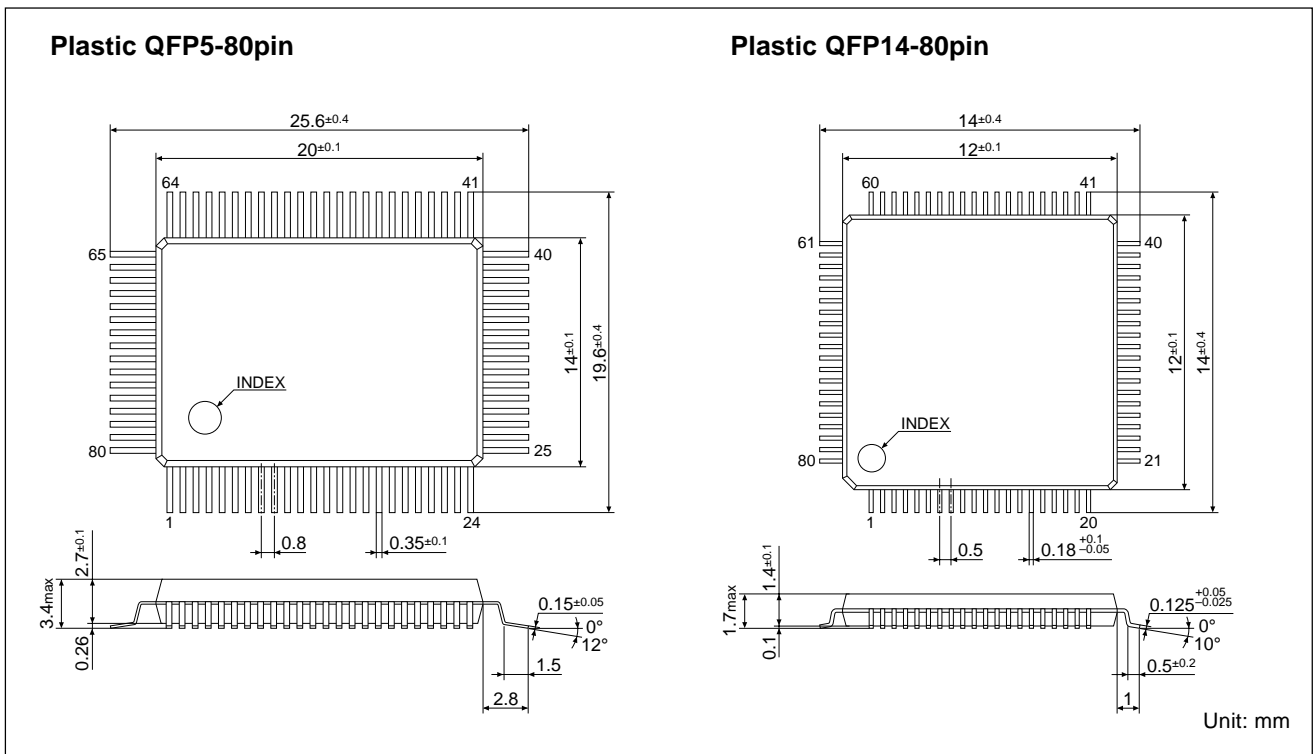
(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 1MHz, C_{cc}=C_{dc}=100pF, T_a=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V _{sta}	(V _{SS})	-2.2			V
Oscillation start time	t _{sta}	V _{SS} =-2.2 to -5.5V			5	mS
Oscillation stop voltage	V _{stp}	(V _{SS})	-2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM



■ PACKAGE DIMENSIONS



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