EPSON

E0C63358

4-bit Single Chip Microcomputer

Low Voltage Operation Products

■ DESCRIPTION

The E0C63358 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, ROM (8,192 words × 13 bits), RAM (512 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counter (1 system), SVD circuit, a segment type LCD driver that can drive a maximum 32 segments × 4 commons, a 4-channel A/D converter and a special input port that can implement key position discrimination function using with the A/D converter. The E0C63358 features low voltage/high speed (4 MHz Max.) operation and low current consumption while the LCD is ON (current consumption in HALT: 2.5 µA), this makes it suitable for battery driven portable equipment such as a head phone stereo.

■ FEATURES

- ● CMOS LSI 4-bit parallel processing
- ● OSC1 oscillation circuit .... 32.768 kHz (Typ.) Crystal oscillation circuit or CR oscillation circuit (∗1)
- ● OSC3 oscillation circuit .... 1.8 MHz (Typ.) CR or 4 MHz (Max.) Ceramic oscillation circuit (∗1)
  Operatable in 2.3 V
- ● Instruction set .... Basic instruction: 46 types (411 instructions with all)
  Addressing mode: 8 types
- ● Instruction execution time .... During operation at 32.768 kHz: Min. 61 µsec
  During operation at 4 MHz: Min. 0.5 µsec
- ● ROM capacity .... Code ROM: 8,192 words × 13 bits
- ● RAM capacity .... Data memory: 512 words × 4 bits
  Display memory: 32 words × 4 bits
- ● Input port .... 9 bits   8 bits (Pull-up resistors may be supplemented ∗1)
                                                                  1 bit (Input interrupt for key position sensing by A/D)
- ● Output port .... 12 bits (It is possible to switch the 2 bits to special output ∗2)
- ● I/O port .... 20 bits (It is possible to switch the 4 bits to serial input/output ∗2)
                                                                  (It is possible to switch the 4 bits to A/D input ∗2)
- ● Serial interface .... 1 port   (8-bit clock synchronous system)
- ● LCD driver .... 32 segments × 4, 3 or 2 commons (∗2) 1/3 or 1/2 bias drive (∗1)
- ● Time base counter .... 1 system (Clock timer)
- ● Programmable timer .... Built-in, 2 channels × 8 bits, with event counter function
                                                                  or 1 channel × 16 bits (∗2)
- ● Watchdog timer .... Built-in
- ● A/D converter .... 8-bit resolution
  Maximum error:
           ±3 LSB, A/D clock: OSC1, OSC3, 2.7 V to 3.6 V
           ±3 LSB, A/D clock: OSC1, OSC3 ≤ 2.5 MHz, 2.3 V to 2.7 V
           ±5 LSB, A/D clock: OSC1, 1.6 V to 2.3 V
           ±5 LSB, A/D clock: OSC1, 0.9 V to 1.6 V
- ● Buzzer output .... Buzzer frequency: 2 kHz or 4 kHz (∗2), 2 Hz interval (∗2)

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● Supply voltage detection (SVD) circuit .. 16 values, programmable (1.05 V to 2.60 V)

● External interrupt .... Input port interrupt: 2 systems

                                         Key sensing interrupt: 1 system

● Internal interrupt .... Clock timer interrupt: 4 systems

                                       Programmable timer interrupt: 2 systems

                                       Serial interface interrupt: 1 system

                                       A/D converter: 1 system

● Power supply voltage .... 0.9 V to 3.6 V (One battery or two batteries)

● Operating temperature range .... -20°C to 70°C

● Current consumption (Typ.) .... Single clock: During HALT (32 kHz)

                                                 1.5 V (LCD power OFF)   2 μA

                                               1.5 V (LCD power ON)   2.5 μA

                                       During operation (32 kHz)

                                               1.5 V (LCD power ON)   6 μA

                                  Twin clock: During operation (4 MHz)

                                               3.0 V (LCD power ON)   900 μA

Package .... QFP15-100pin (plastic)

∗1: Can be selected with mask option   ∗2: Can be selected with software

■ BLOCK DIAGRAM

■ PIN CONFIGURATION

QFP15-100pin

E0C63358

INDEX

75   51
76   50
100   26
1   25
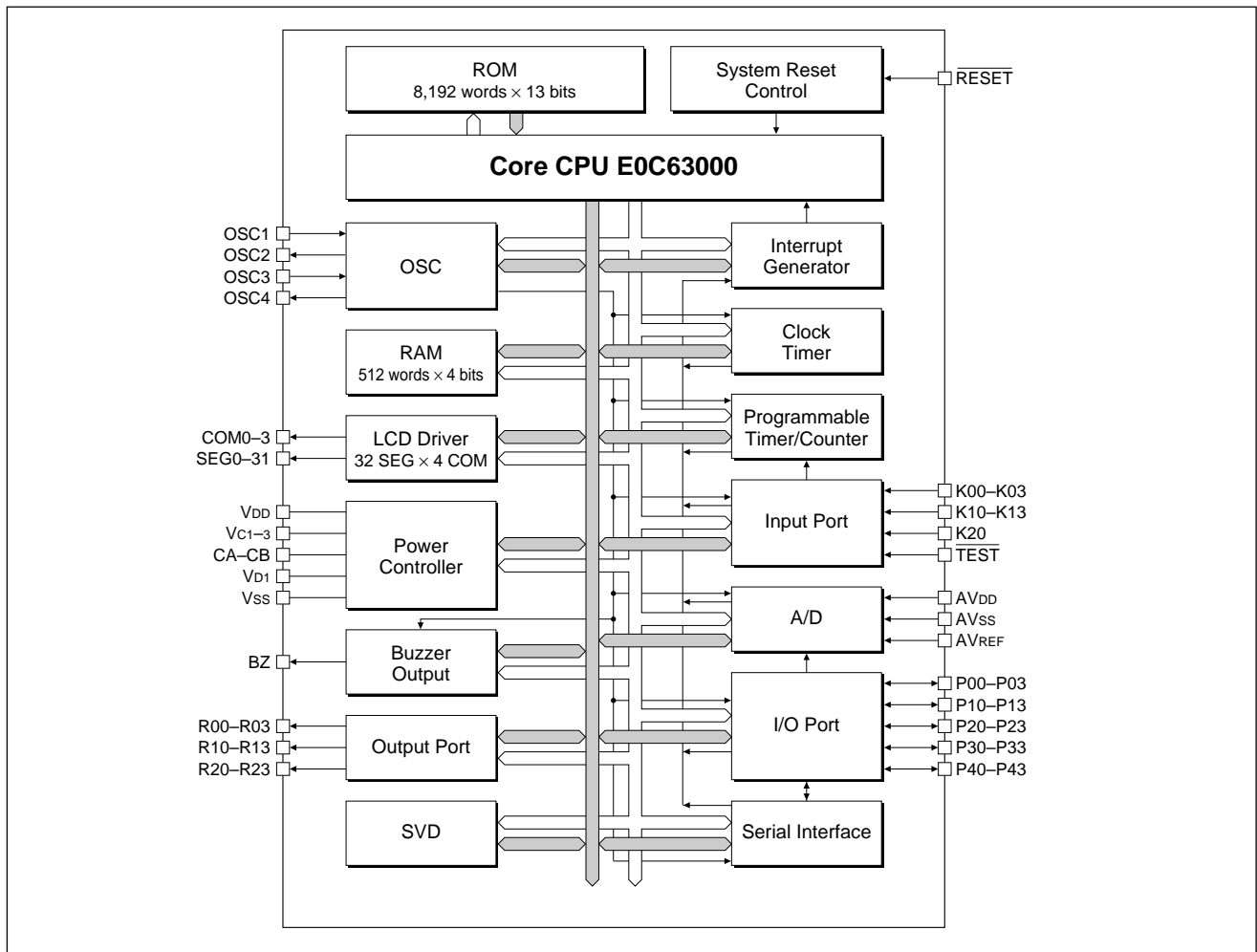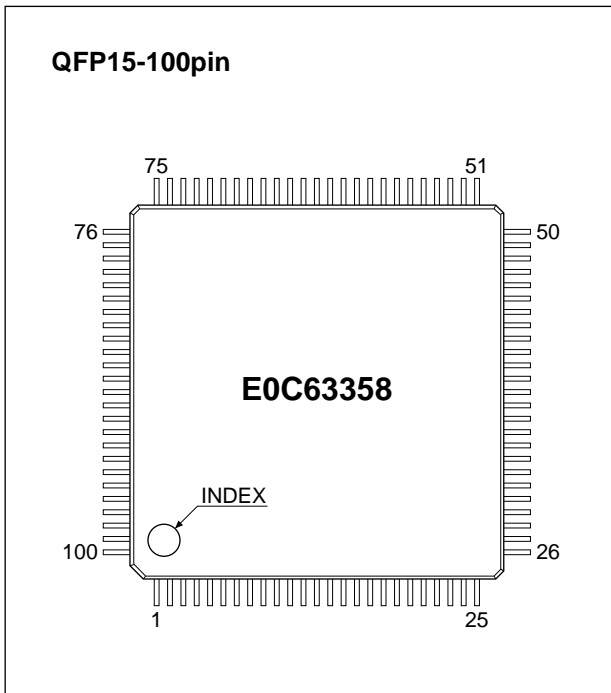
No.	Name	No.	Name	No.	Name	No.	Name
1	SEG7	26	N.C.	51	N.C.	76	R13
2	SEG8	27	N.C.	52	P43	77	R12
3	SEG9	28	COM0	53	P42	78	R11
4	SEG10	29	COM1	54	P41	79	R10
5	SEG11	30	COM2	55	P40	80	R03
6	SEG12	31	COM3	56	P33	81	R02
7	SEG13	32	CB	57	P32	82	R01
8	SEG14	33	CA	58	P31	83	R00
9	SEG15	34	V_{C3}	59	P30	84	BZ
10	SEG16	35	V_{C2}	60	P23	85	K00
11	SEG17	36	V_{C1}	61	P22	86	K01
12	SEG18	37	V_{SS}	62	P21	87	K02
13	SEG19	38	OSC1	63	P20	88	K03
14	SEG20	39	OSC2	64	P13	89	K10
15	SEG21	40	V_{D1}	65	P12	90	K11
16	SEG22	41	OSC3	66	P11	91	K12
17	SEG23	42	OSC4	67	P10	92	K13
18	SEG24	43	V_{DD}	68	P03	93	K20
19	SEG25	44	$\overline{RESET}$	69	P02	94	SEG0
20	SEG26	45	$\overline{TEST}$	70	P01	95	SEG1
21	SEG27	46	AV_{REF}	71	P00	96	SEG2
22	SEG28	47	AV_{DD}	72	R23	97	SEG3
23	SEG29	48	AV_{SS}	73	R22	98	SEG4
24	SEG30	49	N.C.	74	R21	99	SEG5
25	SEG31	50	N.C.	75	R20	100	SEG6

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	43	–	Power (+) supply pin
V_{SS}	37	–	Power (–) supply pin
V_{D1}	40	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C3}	36–34	–	LCD system power supply pin 1/3 or 1/2 bias (selected by mask option)
CA, CB	33, 32	–	LCD system boosting/reducing capacitor connecting pin
OSC1	38	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	39	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	41	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	42	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	85–88	I	Input port
K10–K13	89–92	I	Input port
K20	93	I	Input port with control
P00–P03	71–68	I/O	I/O port
P10–P13	67–64	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20–P23	63–60	I/O	I/O port
P30–P33	59–56	I/O	I/O port
P40–P43	55–52	I/O	I/O port (can be used as A/D input)
R00	83	O	Output port
R01	82	O	Output port
R02	81	O	Output port (switching to TOUT output is possible by software)
R03	80	O	Output port (switching to FOUT output is possible by software)
R10–R13	79–76	O	Output port
R20–R23	75–72	O	Output port
COM0–COM3	28–31	O	LCD common output pin (1/4, 1/3, 1/2 duty can be selected by software)
SEG0–SEG31	94–100, 1–25	O	LCD segment output pin
AV_{DD}	47	–	Power (+) supply pin for A/D converter
AV_{SS}	48	–	Power (–) supply pin for A/D converter
AV_{REF}	46	–	Reference voltage for A/D converter
BZ	84	O	Buzzer output pin
$\overline{RESET}$	44	I	Initial reset input pin
$\overline{TEST}$	45	I	Testing input pin

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