EPSON

E0C63P466

4-bit Single Chip Microcomputer

Preliminary

Wide Voltage Operation Products

- Evaluation chip with Flash built-in
- Compatible with E0C63454, 458 and 466
- On-board writing supported

■ DESCRIPTION

The E0C63P466 is a CMOS 4-bit microcomputer composed of a 4-bit CMOS core CPU, rewritable ROM (Flash), RAM, dot-matrix type LCD driver, serial interface and timers. The E0C63P466 has a built-in large-capacity Flash ROM (16K × 13 bits) and a RAM (5K × 4 bits), and is upper compatible with the E0C63454, E0C63458 and E0C63466. The E0C63P466 can be used as a MTP (Multi-Time Programming) when developing programs.

■ FEATURES

- CMOS LSI 4-bit parallel processing ..... E0C63000 core CPU
- OSC1 oscillation circuit ..... 32.768kHz (Typ.) crystal oscillation
- OSC3 oscillation circuit ..... 4MHz (Typ.) ceramic oscillation
- Instruction set ..... Basic instruction: 46 types (411 instructions with all)
  Addressing mode: 8 types
- Instruction execution time ..... During operation at 32.768kHz: 61µsec, 122µsec, 183µsec
  During operation at 4MHz: 0.5µsec, 1µsec, 1.5µsec
- ROM (Flash) capacity ..... Code ROM: 16,384 words × 13 bits
  Data ROM: 2,048 words × 4 bits (8K bits)
  Programming: Parallel and serial programming (exclusive ROM writer is used)
  Rewriting: 10 times
- RAM capacity ..... Data memory: 5,120 words × 4 bits
  Display memory: 1,020 bits (240 words × 4 bits + 60 × 1 bit)
- Input port ..... 8 bits (With pull-up resistors)
- Output port ..... 12 bits (It is possible to switch the 2 bits to special output ∗1)
- I/O port ..... 12 bits (It is possible to switch the 2 bits to special output and the 4 bits to serial I/F input/output ∗1)
- Serial interface ..... 1 port (8-bit clock synchronous system)
- LCD driver ..... 60 segments × 8 / 16 / 17 commons (∗1)
- Time base counter ..... Built-in (Clock timer, stopwatch timer)
- Programmable timer ..... Built-in (8 bits × 2 ch., with event counter function)
- Watchdog timer ..... Built-in
- Sound generator ..... With envelope and 1-shot output functions
- Interrupts ..... External: Input port interrupt 2 lines
  Internal: Clock timer interrupt 4 lines
  Stopwatch timer interrupt 2 lines
  Programmable timer interrupt 2 lines
  Serial interface interrupt 1 line
- Supply voltage ..... 2.7 to 5.5V
- Operating temperature ..... -20 to 70°C

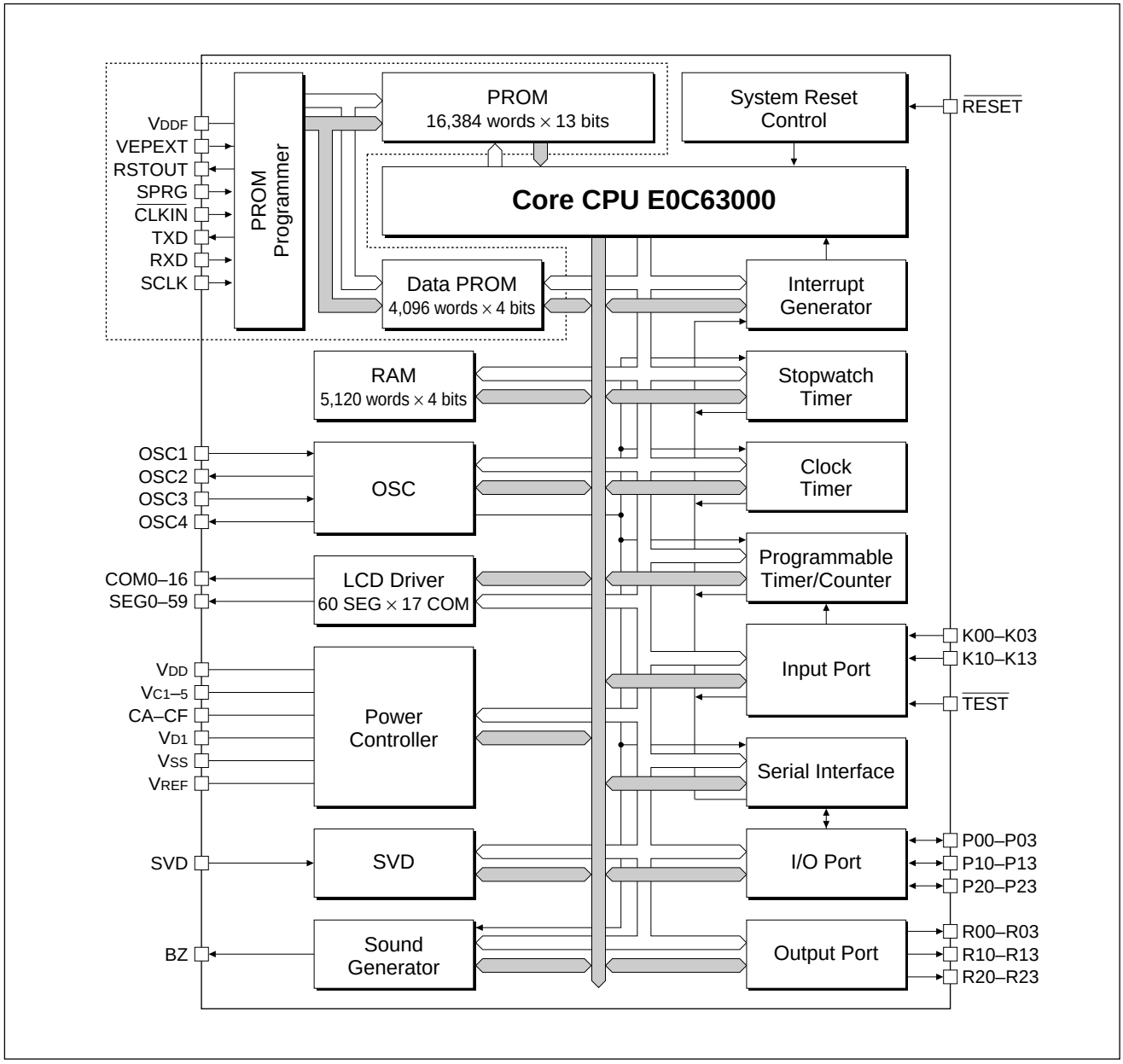
● Current consumption (Typ.) ..... Single clock (OSC1: crystal oscillation)

HALT mode (32kHz)	3V ±10%	2µA (∗2)
	5V ±10%	2µA (∗2)
OPERATING mode (32kHz)	3V ±10%	300µA
	5V ±10%	1mA
Twin clock		
OPERATING mode (4MHz)	3V ±10%	2mA
	5V ±10%	4mA

● Package ..... QFP8-144pin / QFP17-144pin (∗3, ∗4) or die form

∗1: Can be selected with software
∗2: Target current (This value has possibility to change.)
∗3: 128-pin package is not available
∗4: Parallel programming is supported only QFP17-144pin

■ BLOCK DIAGRAM

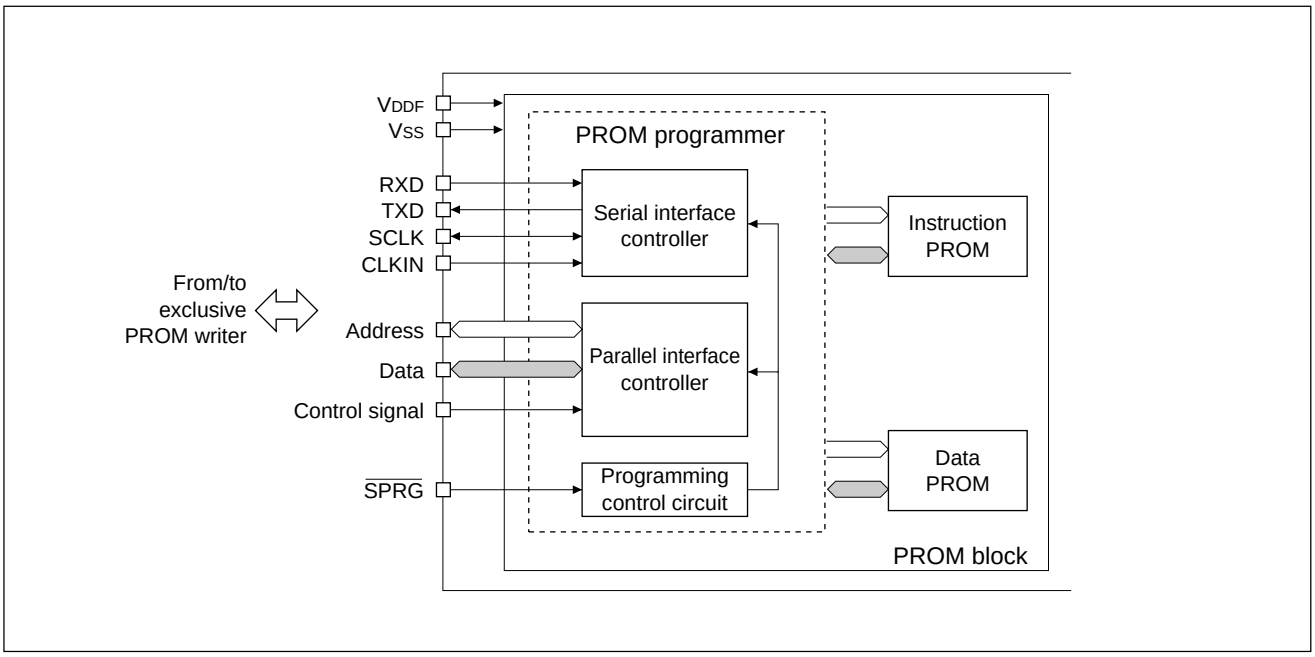


■ PROM PROGRAMMING AND OPERATING MODE

The E0C63P466 has built-in Flash EEPROMs as the instruction ROM and the data ROM that allow the developer to program the ROM data using the exclusive PROM writer (UNIVERSAL ROM WRITER II). This section explains the PROM programmer that controls data writing and the writing mode.

● Configuration of PROM Programmer

The configuration of the PROM programmer is shown below.



The PROM programmer supports the following two writing modes.

1) Serial Programming

2) Parallel Programming (Only QFP17-144pin)

Serial Programming mode uses the serial communication ports of the PROM writer and E0C63P466 to write data. This mode enables on-board programming by designing the target board with a serial writing function. In Parallel Programming mode, the on-chip Flash ROM can be directly programmed using the exclusive PROM writer with the adaptor socket installed. Refer to "Operating Mode" for each programming method.

Terminals

The E0C63P466 provides the following terminals for programming the Flash EEPROM.

V_{DDF}	Power supply (+) terminal for Flash EEPROM
$\overline{SPRG}$	Flash programming control terminal (pull-up resistor built-in)
	When set to High Normal operation mode (The CPU executes the program in the Flash EEPROM.)
	When set to Low Programming mode (for writing data to the Flash EEPROM)
SCLK	Serial transfer clock input/output terminal for Serial Programming (pull-up resistor built-in)
RXD	Serial data input terminal for Serial Programming (pull-up resistor built-in)
TXD	Serial data output terminal for Serial Programming
CLKIN	PROM programmer clock input terminal (1MHz; pull-up resistor built-in)
RSTOUT	Test signal monitor terminal (Not used when writing; keep it open)
VEPEXT	Test signal monitor terminal (Not used when writing; keep it open)

The eight terminals above are provided exclusively for the Flash EEPROM. The E0C63454, E0C63458 and E0C63466 do not have these terminals.

● Operating Mode

Three operating modes are available in the E0C63P466: one is for normal operation and the others are for programming.

The operating mode is decided by the terminal settings at power-on or initial reset.

When the $\overline{\text{SPRG}}$ terminal is set to Low, the E0C63P466 enters Serial Programming mode. To operate the E0C63P466 in Normal Operation mode (to execute the instruction written to the Flash EEPROM after programming), the $\overline{\text{SPRG}}$ terminal should be set to High or open.

The parallel programming including the mode switching and terminal settings is controlled by the exclusive PROM writer.

The following table lists the operating modes.

Operating mode	$\overline{\text{SPRG}}$ terminal
Normal Operation mode	High or open
Serial Programming mode	Low
Parallel Programming mode	Set by the PROM writer

Normal Operation Mode

In this mode, the E0C63000 core CPU and the peripheral circuits operate by the instructions programmed in the Flash EEPROM. The Flash EEPROM bit data is set to "1" at shipment.

In Normal Operation mode, set the terminals for programming the Flash EEPROM as below. The board must be designed so that the terminal settings cannot be changed while the IC is operating.

Terminal	Set-up
V_{DDF}	Supply the same voltage as V_{DD}
$\overline{\text{SPRG}}$	High or open
SCLK	High or open
RXD	High or open
TXD	Open
CLKIN	High or open
RSTOUT	Open
VEPEXT	Open

Serial Programming Mode

Serial Programming mode writes data to the Flash EEPROM using a serial communication between the exclusive PROM writer (UNIVERSAL ROM WRITER II) and the E0C63P466. By providing a serial communication port on the target board, the E0C63P466 on the board can be programmed (on-board writing).

Terminal	Set-up
V_{DDF}	Supply the same voltage as V_{DD}
$\overline{\text{SPRG}}$	Low
SCLK	Connected to the PROM writer
RXD	Connected to the PROM writer
TXD	Connected to the PROM writer
CLKIN	Connected to the PROM writer
RSTOUT	Open
VEPEXT	Open

When the $\overline{\text{SPRG}}$ terminal is set to Low, the E0C63P466 starts operating in Serial Programming mode after power-on or an initial reset.

Be sure not to change the $\overline{\text{SPRG}}$ terminal status during normal operation or serial programming, because the operating mode may change according to the terminal status.

The serial programming is performed using the 1MHz clock supplied from the PROM writer to the CLKIN terminal. Take noise measure into consideration so that noise does not affect the clock line input to the CLKIN terminal when designing the target board.

The PROM writer does not supply the source voltage to the E0C63P466 during serial programming. Therefore, supply a 5V source voltage between the V_{DD} and V_{SS} terminals and between the V_{DDF} and V_{SS} terminals of the E0C63P466. Furthermore, to start a serial programming, an initial reset to the E0C63P466 is required. Use the $\overline{\text{RESET}}$ terminal to reset the E0C63P466 securely.

Parallel Programming Mode

The parallel programming can be performed by installing the E0C63P466 to the exclusive PROM writer via the adaptor socket. In this mode, it is not necessary to set up the programming terminals since it is controlled by the exclusive PROM writer. For the E0C63P466, the adaptor socket for the QFP17-144pin package only is available. Note that the QFP8-144pin and QFP5-128pin packages are not supported.

Package type	Adapter socket support
QFP17-144pin	Available
QFP8-144pin	Not available
QFP5-128pin	Not available

When using a package other than QFP17-144pin or a die form, perform on-board programming in Serial Programming mode.

■ DIFFERENCES FROM THE MASK ROM MODELS

This section explains the differences in functions (except for the Flash EEPROM block) between the E0C63P466 and the mask ROM models (E0C63454, E0C63458 and E0C63466).

● Mask Option

The mask option items are fixed in the E0C63P466 as shown in the table below.

Mask option		Setting
OSC1 oscillation circuit		Crystal oscillation (32.768 kHz)
OSC3 oscillation circuit		Use <ceramic> or Not use
Multiple key entry reset combination		Not use
Multiple key entry reset time authorization		Not use
Input port pull-up resistor	K00	With pull-up resistor
	K01	With pull-up resistor
	K02	With pull-up resistor
	K03	With pull-up resistor
	K10	With pull-up resistor
	K11	With pull-up resistor
	K12	With pull-up resistor
	K13	With pull-up resistor
Output port specification	R00	Complementary
	R01	Complementary
	R02	Complementary
	R03	Complementary
	R1x	Complementary
	R2x	Complementary
I/O port specification	P0x	Complementary
	P1x	Complementary
	P20	Complementary
	P21	Complementary
	P22	Complementary
	P23	Complementary
I/O port pull-up resistor	P0x	With pull-up resistor
	P1x	With pull-up resistor
	P20	With pull-up resistor
	P21	With pull-up resistor
	P22	With pull-up resistor
	P23	With pull-up resistor
LCD drive power		Internal power supply
Serial interface polarity		Negative polarity
SVD circuit external voltage detection		Use
Sound generator buzzer output specification		Positive polarity

● Power Supply

Since the E0C63P466 is produced using the Flash EEPROM process, the characteristics are different from those of the mask ROM models.

1) Operating voltage range

E0C63P466: 2.7 to 5.5V
E0C63454: 2.2 to 5.5V (Min. 1.8V when the OSC3 is not used)
E0C63458: 2.2 to 5.5V (Min. 1.8V when the OSC3 is not used)
E0C63466: 2.2 to 5.5V (Min. 1.8V when the OSC3 is not used)

The circuit blocks of the E0C63P466 except for the OSC1 oscillation circuit and LCD driver (CPU, ROM, RAM and peripheral digital circuits) operate with the source voltage supplied between the V_{DD} and V_{SS} terminals. Therefore, the VDC register (I/O memory address: FF00H, data bit: D0) is invalidated and is used as a general-purpose register. Writing "1" or "0" to this register does not affect the V_{D1} output voltage level.

E0C63P466

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	1	0	General-purpose register

E0C63454, E0C63458, E0C63466

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0	–			Unused
					VDC	0	2.1 V	1.3 V	CPU operating voltage switch (1.3 V: OSC1, 2.1 V: OSC3)

2) Power supply terminal for the Flash EEPROM (V_{DDF})

The E0C63P466 has a power supply (+) terminal exclusively for use with the Flash EEPROM block (V_{DDF}). In Serial Programming mode or Normal Operation mode, the V_{DDF} terminal should be connected to the V_{DD} terminal so that the V_{DD} voltage level is supplied to the V_{DDF} terminal.

3) Power supply terminal for the OSC1 oscillation circuit (V_{D1})

The V_{D1} voltage that is generated by the internal voltage regulator is used only for the OSC1 oscillation circuit to stabilize the oscillation. As explained in Item 1 above, the VDC register (FF00H•D0) does not affect the V_{D1} output voltage. In the E0C63P466, the V_{D1} voltage is fixed as follows:

V_{D1} output voltage = 1.6 V ± 0.3 V

4) Power supply for driving the LCD (V_{C1} to V_{C5})

The LCD system voltage circuit in the E0C63P466 generates the four voltages (for 1/4 bias): V_{C1}, V_{C2}, V_{C4} and V_{C5}. As similar to the E0C63454, E0C63458 and E0C63466, V_{C1} or V_{C2} is generated by the internal voltage regulator and the other three voltages are generated by boosting and reducing it. The following table lists the voltage values.

LCD drive voltage	V_{C1} standard	V_{C2} standard
V_{C1} (0.975–1.2V)	V_{C1} (regulated voltage)	1/2 × V_{C2}
V_{C2} (1.950–2.4V)	2 × V_{C1}	V_{C2} (regulated voltage)
V_{C4} (2.925–3.6V)	3 × V_{C1}	3/2 × V_{C2}
V_{C5} (3.900–4.8V)	4 × V_{C1}	2 × V_{C2}

(V_{DD} = 2.7 to 5.5V)

Since the minimum operating voltage of the E0C63P466 is 2.7V, either V_{C1} standard or V_{C2} standard can be selected. V_{C2} standard can improve the display quality and reduce current consumption. However, in the mask ROM model, V_{C1} standard must be selected when using the IC with a 2.6V or less operating voltage V_{DD}. Take this into consideration when creating a program.

● **ROM, RAM**

The E0C63P466 employs a Flash EEPROM for the internal ROM. The Flash EEPROM can be rewritten up to 10 times. Rewriting data is done at the user's own risk.
The following table lists the internal memory size of each model.

Memory	E0C63P466	E0C63454	E0C63458	E0C63466
Code ROM	16K × 13 bits	4K × 13 bits	8K × 13 bits	16K × 13 bits
Data RAM	5,120 × 4 bits	1,024 × 4 bits	5,120 × 4 bits	1,792 × 4 bits
Data ROM	2K × 4 bits	2K × 4 bits	2K × 4 bits	2K × 4 bits
Display RAM	1,020 × 4 bits	680 × 4 bits	1,020 × 4 bits	1,020 × 4 bits

The code ROM and data ROM of the E0C63P466 is a Flash EEPROM and can be rewritten using the exclusive PROM writer. The size is set according to the largest model among the E0C63454, E0C63458 and E0C63466. When developing an application for the E0C634xx Series mask ROM model, pay attention to the memory size.

● **Input/Output Ports and LCD Driver**

The configuration of the input/output ports and LCD driver is the same as those of the E0C63466. The following table lists the configuration of each model.

Port	E0C63P466	E0C63454	E0C63458	E0C63466
Input (K) port	8 bits	4 bits	8 bits	8 bits
Output (R) port	12 bits	4 bits	12 bits	12 bits
I/O (P) port	12 bits	8 bits	12 bits	12 bits
LCD driver	60 SEG × 17 COM	40 SEG × 17 COM	60 SEG × 17 COM	60 SEG × 17 COM

Note that the E0C63454 supports only one system of the external input interrupt since the input port is configured with 4 bits (K00–K03). Refer to the "E0C63454 Technical Manual" for details.

● **Oscillation Circuit**

The E0C63P466 has two oscillation circuits built-in: OSC1 generates a low-speed clock and OSC3 generates a high-speed clock.
In the E0C63454, E0C63458 and E0C63466, the OSC1 and OSC3 oscillation circuits operate with the internal regulated voltage V_{D1}, note, however, the OSC3 oscillation circuit in the E0C63P466 operates with the supply voltage V_{DD}. Therefore, the oscillation characteristics of the E0C63P466 are different from those of the mask ROM model (E0C634xx). When using the E0C63P466 as a development tool for the mask ROM model, the constant of the OSC3 oscillation circuit must be decided according to the characteristics of the mask ROM model. Also the OSC1 oscillation circuit of the E0C63P466 has differences in its production process from the mask ROM models. The constant must be decided according to the characteristics of the mask ROM model.
The following table lists the configuration of the oscillation circuits for each model.

Oscillation circuit	E0C63P466	E0C63454	E0C63458	E0C63466
OSC1	32.768kHz crystal	32.768kHz crystal	32.768kHz crystal	32.768kHz crystal
	—	60kHz (Typ.) CR	60kHz (Typ.) CR	60kHz (Typ.) CR
OSC3	—	1.8MHz (Typ.) CR	1.8MHz (Typ.) CR	1.8MHz (Typ.) CR
	4.1MHz (Max.) ceramic	4.1MHz (Max.) ceramic	4.1MHz (Max.) ceramic	4.1MHz (Max.) ceramic

∗ In the mask ROM models, either crystal or CR can be selected for the OSC1 oscillation circuit by mask option and either CR or ceramic can be selected for the OSC3 oscillation circuit.

● **SVD Circuit**

The E0C63P466 has a built-in SVD (Supply Voltage Detection) circuit with the same configuration as that of the mask ROM model (E0C634xx). However, the mask option is fixed at "with external voltage detection".
The following table lists the criteria voltages.

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)	
				E0C63P466	E0C634xx
0	0	0	0	1.05 (external voltage)	1.85/1.05
0	0	0	1	—	1.90
0	0	1	0	—	2.00
0	0	1	1	—	2.10
0	1	0	0	—	2.20
0	1	0	1	—	2.30
0	1	1	0	—	2.40
0	1	1	1	—	2.50
1	0	0	0	—	2.60
1	0	0	1	—	2.70
1	0	1	0	2.80	2.80
1	0	1	1	2.90	2.90
1	1	0	0	3.00	3.00
1	1	0	1	3.10	3.10
1	1	1	0	3.20	3.20
1	1	1	1	3.30	3.30

A criteria voltage can be set using the SVDS0–SVDS3 register (I/O memory address: FF04H).
Since the minimum operating voltage of the E0C63P466 is 2.7V, 2.7V or less criteria voltages are not available. Be aware that the SVD circuit in the E0C63P466 may not operate when a 2.7V or less criteria voltage is selected.
For the software control sequence of the SVD circuit, refer to the "E0C634xx Technical Manual".

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
PROM power voltage	V_{DDF}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{DD} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package (QFP8-144pin, QFP17-144pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	2.7		5.5	V
PROM power voltage	V_{DDF}	Normal operation mode	2.7		5.5	V
		Programming mode	4.5	5.0	5.5	V
Oscillation frequency	f_{OSC1}	Crystal oscillation		32.768	–	kHz
	f_{OSC3}	Ceramic oscillation			4.1	MHz
SVD terminal input voltage	SVD	$V_{SVD} \leq V_{DD}$, criteria voltage=1.05V	0		5.5	V

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2•V_D	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-16		-6	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23			-2	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ			-2	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23	3			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	3			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–COM16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–SEG59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

(Unless otherwise specified: V_{DD}=5.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23	0		0.2•V_D	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=5.0V	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull-up	K00–03, K10–13 P00–03, P10–13, P20–23 $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23			-5	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	BZ			-5	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00–03, R10–13, R20–23 P00–03, P10–13, P20–23	7.5			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	BZ	7.5			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–COM16			-25	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		25			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–SEG59			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

● Analog Circuit Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (No panel load)	LC0–3="0"	Typ.×0.88	0.975	Typ.×1.12	V
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"		1.080		
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="A"		1.125		
			LC0–3="B"		1.140		
			LC0–3="C"		1.155		
			LC0–3="D"		1.170		
			LC0–3="E"		1.185		
			LC0–3="F"		1.200		
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (No panel load)		2•V_{C1}		2•V_{C1} ×0.9	V
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (No panel load)		3•V_{C1}		3•V_{C1} ×0.9	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (No panel load)		4•V_{C1}		4•V_{C1} ×0.9	V

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF)

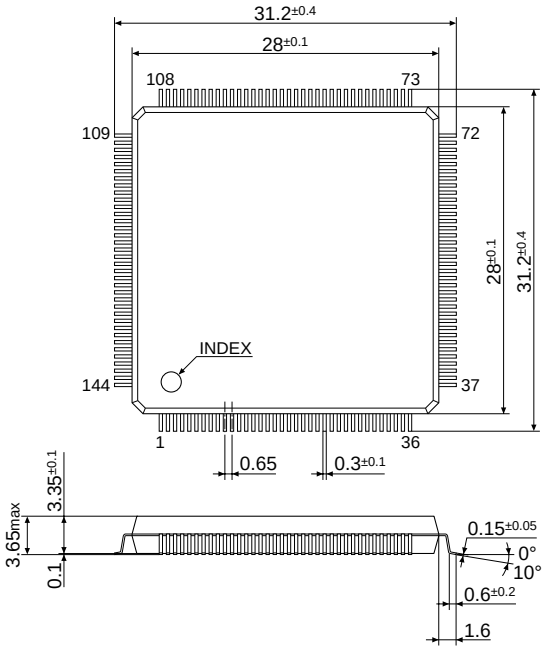
Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1MΩ load resistor between V_{SS} and V_{C1} (No panel load)		1/2•V_{C2} -0.1		1/2•V_{C2} ×0.95	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (No panel load)	LC0–3="0"	Typ.×0.88	1.95	Typ.×1.12	V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="A"		2.25		
			LC0–3="B"		2.28		
			LC0–3="C"		2.31		
			LC0–3="D"		2.34		
			LC0–3="E"		2.37		
			LC0–3="F"		2.40		
	V_{C4}	Connect 1MΩ load resistor between V_{SS} and V_{C4} (No panel load)		3/2•V_{C2} ×0.95		3/2•V_{C2}	V
	V_{C5}	Connect 1MΩ load resistor between V_{SS} and V_{C5} (No panel load)		2•V_{C2} ×0.95		2•V_{C2}	V
SVD voltage	V_{SVD1}	SVDS0–3="0" (external) *3		0.95	1.05	1.15	V
		SVDS0–3="1"		Typ.×0.93	–	Typ.×1.02	V
		SVDS0–3="2"			–		
		SVDS0–3="3"			–		
		SVDS0–3="4"			–		
		SVDS0–3="5"			–		
		SVDS0–3="6"			–		
		SVDS0–3="7"			–		
		SVDS0–3="8"			–		
		SVDS0–3="9"			–		
		SVDS0–3="10"			2.80		
		SVDS0–3="11"			2.90		
		SVDS0–3="12"			3.00		
		SVDS0–3="13"			3.10		
		SVDS0–3="14"			3.20		
		SVDS0–3="15"			3.30		
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT (32kHz, crystal)	LCD power OFF *1,*2,*4		2	5	µA
			LCD power ON (V_{C1} standard) *1,*2		11	19	µA
			LCD power ON (V_{C2} standard) *1,*2		9	15	µA
		During execution (32kHz, crystal)	V_{DD}=3.0V *1,*2		300		µA
			V_{DD}=5.0V *1,*2		1		mA
		During execution (4MHz, ceramic)	V_{DD}=3.0V *1		2		mA
			V_{DD}=5.0V *1		4		mA

∗1: No panel load. The SVD circuit is OFF.
∗2: OSCC="0"
∗3: Do not apply a voltage level that exceeds the V_{SS}–V_{DD} range to the SVD terminal.
∗4: Target current (This value has possibility to change.)

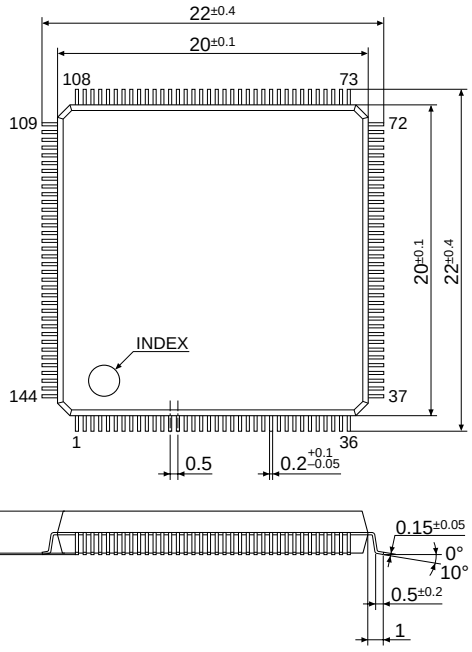
■ PACKAGE

● Package Dimensions

Plastic QFP8-144pin



Plastic QFP17-144pin



The dimensions are subject to change without notice.

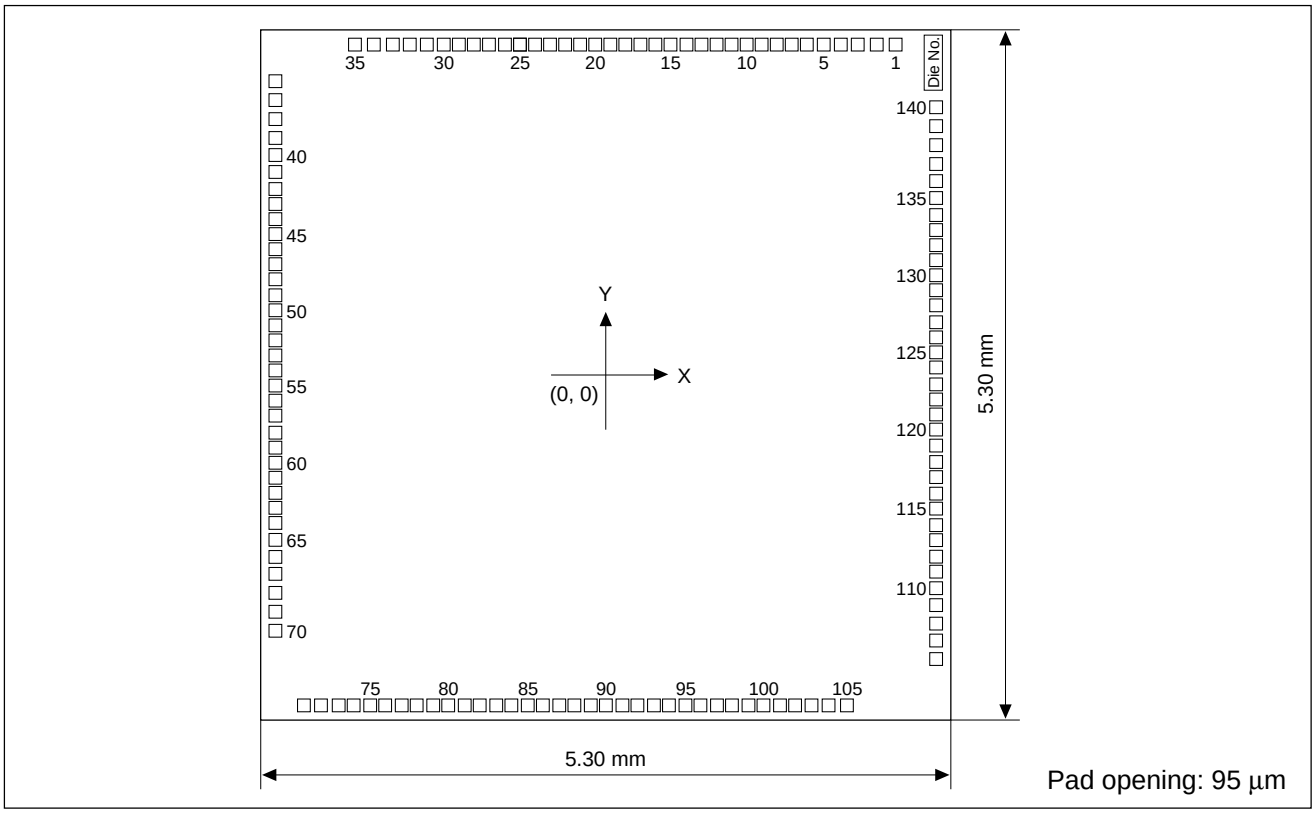
Unit: mm

● Pin Layout

No.	Pin name			No.	Pin name			No.	Pin name			No.	Pin name		
	E0C63458	E0C63466	E0C63P466		E0C63458	E0C63466	E0C63P466		E0C63458	E0C63466	E0C63P466		E0C63458	E0C63466	E0C63P466
1	SEG13	SEG13	SEG13	37	N.C.	N.C.	RXD	73	N.C.	N.C.	V_{DDF}	109	N.C.	N.C.	RSTOUT
2	SEG12	SEG12	SEG12	38	N.C.	N.C.	TXD	74	SVD	SVD	SVD	110	SEG47	SEG47	SEG47
3	SEG11	SEG11	SEG11	39	R23	R23	R23	75	V_{C1}	V_{C1}	V_{C1}	111	SEG46	SEG46	SEG46
4	SEG10	SEG10	SEG10	40	R22	R22	R22	76	V_{C2}	V_{C2}	V_{C2}	112	SEG45	SEG45	SEG45
5	SEG9	SEG9	SEG9	41	R21	R21	R21	77	V_{C3}	V_{C3}	V_{C3}	113	SEG44	SEG44	SEG44
6	SEG8	SEG8	SEG8	42	R20	R20	R20	78	V_{C4}	V_{C4}	V_{C4}	114	SEG43	SEG43	SEG43
7	SEG7	SEG7	SEG7	43	R13	R13	R13	79	V_{C5}	V_{C5}	V_{C5}	115	SEG42	SEG42	SEG42
8	SEG6	SEG6	SEG6	44	R12	R12	R12	80	CF	CF	CF	116	SEG41	SEG41	SEG41
9	SEG5	SEG5	SEG5	45	R11	R11	R11	81	CE	CE	CE	117	SEG40	SEG40	SEG40
10	SEG4	SEG4	SEG4	46	R10	R10	R10	82	CD	CD	CD	118	SEG39	SEG39	SEG39
11	SEG3	SEG3	SEG3	47	R03	R03	R03	83	CC	CC	CC	119	SEG38	SEG38	SEG38
12	SEG2	SEG2	SEG2	48	R02	R02	R02	84	CB	CB	CB	120	SEG37	SEG37	SEG37
13	SEG1	SEG1	SEG1	49	R01	R01	R01	85	CA	CA	CA	121	SEG36	SEG36	SEG36
14	SEG0	SEG0	SEG0	50	R00	R00	R00	86	COM8	COM8	COM8	122	SEG35	SEG35	SEG35
15	COM7	COM7	COM7	51	P23	P23	P23	87	COM9	COM9	COM9	123	SEG34	SEG34	SEG34
16	COM6	COM6	COM6	52	P22	P22	P22	88	COM10	COM10	COM10	124	SEG33	SEG33	SEG33
17	COM5	COM5	COM5	53	P21	P21	P21	89	COM11	COM11	COM11	125	SEG32	SEG32	SEG32
18	COM4	COM4	COM4	54	P20	P20	P20	90	COM12	COM12	COM12	126	SEG31	SEG31	SEG31
19	N.C.	N.C.	N.C.	55	P13	P13	P13	91	COM13	COM13	COM13	127	SEG30	SEG30	SEG30
20	COM3	COM3	COM3	56	P12	P12	P12	92	COM14	COM14	COM14	128	SEG29	SEG29	SEG29
21	COM2	COM2	COM2	57	P11	P11	P11	93	COM15	COM15	COM15	129	SEG28	SEG28	SEG28
22	COM1	COM1	COM1	58	P10	P10	P10	94	COM16	COM16	COM16	130	SEG27	SEG27	SEG27
23	COM0	COM0	COM0	59	P03	P03	P03	95	SEG59	SEG59	SEG59	131	SEG26	SEG26	SEG26
24	BZ	BZ	BZ	60	P02	P02	P02	96	SEG58	SEG58	SEG58	132	SEG25	SEG25	SEG25
25	V_{SS}	V_{SS}	V_{SS}	61	P01	P01	P01	97	SEG57	SEG57	SEG57	133	SEG24	SEG24	SEG24
26	OSC1	OSC1	OSC1	62	P00	P00	P00	98	SEG56	SEG56	SEG56	134	SEG23	SEG23	SEG23
27	OSC2	OSC2	OSC2	63	K13	K13	K13	99	SEG55	SEG55	SEG55	135	SEG22	SEG22	SEG22
28	V_{D1}	V_{D1}	V_{D1}	64	K12	K12	K12	100	SEG54	SEG54	SEG54	136	SEG21	SEG21	SEG21
29	OSC3	OSC3	OSC3	65	K11	K11	K11	101	SEG53	SEG53	SEG53	137	SEG20	SEG20	SEG20
30	OSC4	OSC4	OSC4	66	K10	K10	K10	102	SEG52	SEG52	SEG52	138	SEG19	SEG19	SEG19
31	V_{DD}	V_{DD}	V_{DD}	67	K03	K03	K03	103	SEG51	SEG51	SEG51	139	SEG18	SEG18	SEG18
32	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$	68	K02	K02	K02	104	SEG50	SEG50	SEG50	140	SEG17	SEG17	SEG17
33	$\overline{TEST}$	$\overline{TEST}$	$\overline{TEST}$	69	K01	K01	K01	105	SEG49	SEG49	SEG49	141	SEG16	SEG16	SEG16
34	V_{REF}	V_{REF}	V_{REF}	70	K00	K00	K00	106	SEG48	SEG48	SEG48	142	SEG15	SEG15	SEG15
35	N.C.	N.C.	CLKIN	71	N.C.	N.C.	$\overline{SPRG}$	107	N.C.	N.C.	VEPEXT	143	SEG14	SEG14	SEG14
36	N.C.	N.C.	SCLK	72	N.C.	N.C.	N.C.	108	N.C.	N.C.	N.C.	144	N.C.	N.C.	N.C.

■ PAD LAYOUT

● Diagram of Pad Layout



● Pad Coordinates

No.	Name	X (μm)	Y (μm)	No.	Name	X (μm)	Y (μm)	No.	Name	X (μm)	Y (μm)	No.	Name	X (μm)	Y (μm)
1	RXD	2,226	2,537	36	V_{DDF}	-2,537	2,256	71	RSTOUT	-2,318	-2,537	106	SEG13	2,537	-2,181
2	TXD	2,081	2,537	37	SVD	-2,537	2,111	72	SEG47	-2,187	-2,537	107	SEG12	2,537	-2,039
3	R23	1,935	2,537	38	V_{C1}	-2,537	1,965	73	SEG46	-2,051	-2,537	108	SEG11	2,537	-1,909
4	R22	1,805	2,537	39	V_{C2}	-2,537	1,820	74	SEG45	-1,936	-2,537	109	SEG10	2,537	-1,767
5	R21	1,674	2,537	40	V_{C3}	-2,537	1,689	75	SEG44	-1,809	-2,537	110	SEG9	2,537	-1,637
6	R20	1,544	2,537	41	V_{C4}	-2,537	1,559	76	SEG43	-1,694	-2,537	111	SEG8	2,537	-1,510
7	R13	1,428	2,537	42	V_{C5}	-2,537	1,428	77	SEG42	-1,567	-2,537	112	SEG7	2,537	-1,395
8	R12	1,313	2,537	43	CF	-2,537	1,313	78	SEG41	-1,452	-2,537	113	SEG6	2,537	-1,268
9	R11	1,197	2,537	44	CE	-2,537	1,197	79	SEG40	-1,325	-2,537	114	SEG5	2,537	-1,153
10	R10	1,082	2,537	45	CD	-2,537	1,082	80	SEG39	-1,210	-2,537	115	SEG4	2,537	-1,026
11	R03	966	2,537	46	CC	-2,537	966	81	SEG38	-1,083	-2,537	116	SEG3	2,537	-911
12	R02	851	2,537	47	CB	-2,537	851	82	SEG37	-968	-2,537	117	SEG2	2,537	-784
13	R01	735	2,537	48	CA	-2,537	735	83	SEG36	-841	-2,537	118	SEG1	2,537	-668
14	R00	620	2,537	49	COM8	-2,537	612	84	SEG35	-725	-2,537	119	SEG0	2,537	-542
15	P23	497	2,537	50	COM9	-2,537	497	85	SEG34	-599	-2,537	120	COM7	2,537	-419
16	P22	381	2,537	51	COM10	-2,537	381	86	SEG33	-483	-2,537	121	COM6	2,537	-303
17	P21	266	2,537	52	COM11	-2,537	266	87	SEG32	-357	-2,537	122	COM5	2,537	-188
18	P20	150	2,537	53	COM12	-2,537	150	88	SEG31	-241	-2,537	123	COM4	2,537	-72
19	P13	35	2,537	54	COM13	-2,537	35	89	SEG30	-115	-2,537	124	COM3	2,537	58
20	P12	-81	2,537	55	COM14	-2,537	-81	90	SEG29	1	-2,537	125	COM2	2,537	174
21	P11	-197	2,537	56	COM15	-2,537	-197	91	SEG28	128	-2,537	126	COM1	2,537	289
22	P10	-312	2,537	57	COM16	-2,537	-312	92	SEG27	243	-2,537	127	COM0	2,537	405
23	P03	-428	2,537	58	SEG59	-2,537	-443	93	SEG26	370	-2,537	128	BZ	2,537	535
24	P02	-543	2,537	59	SEG58	-2,537	-558	94	SEG25	485	-2,537	129	V_{SS}	2,537	651
25	P01	-659	2,537	60	SEG57	-2,537	-674	95	SEG24	612	-2,537	130	OSC1	2,537	766
26	P00	-774	2,537	61	SEG56	-2,537	-789	96	SEG23	727	-2,537	131	OSC2	2,537	882
27	K13	-897	2,537	62	SEG55	-2,537	-905	97	SEG22	854	-2,537	132	V_{D1}	2,537	997
28	K12	-1,013	2,537	63	SEG54	-2,537	-1,020	98	SEG21	969	-2,537	133	OSC3	2,537	1,113
29	K11	-1,128	2,537	64	SEG53	-2,537	-1,136	99	SEG20	1,096	-2,537	134	OSC4	2,537	1,228
30	K10	-1,244	2,537	65	SEG52	-2,537	-1,266	100	SEG19	1,211	-2,537	135	V_{DD}	2,537	1,359
31	K03	-1,374	2,537	66	SEG51	-2,537	-1,397	101	SEG18	1,338	-2,537	136	$\overline{RESET}$	2,537	1,489
32	K02	-1,505	2,537	67	SEG50	-2,537	-1,527	102	SEG17	1,454	-2,537	137	$\overline{TEST}$	2,537	1,620
33	K01	-1,635	2,537	68	SEG49	-2,537	-1,673	103	SEG16	1,580	-2,537	138	V_{REF}	2,537	1,765
34	K00	-1,781	2,537	69	SEG48	-2,537	-1,818	104	SEG15	1,711	-2,537	139	CLKIN	2,537	1,911
35	$\overline{SPRG}$	-1,926	2,537	70	VEPEXT	-2,537	-1,964	105	SEG14	1,852	-2,537	140	SCLK	2,537	2,056

■ Pin Description

Pin name	Pin No.	Pad No.	I/O	Function
V_{DD}	31	135	–	Power (+) supply pin
V_{SS}	25	129	–	Power (–) supply pin
V_{D1}	28	132	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C5}	75–79	38–42	–	LCD system power supply pin
V_{REF}	34	138	O	LCD system power supply testing pin
CA–CF	85–80	48–43	–	LCD system boosting capacitor connecting pin
OSC1	26	130	I	Crystal oscillation input pin
OSC2	27	131	O	Crystal oscillation output pin
OSC3	29	133	I	Ceramic oscillation input pin
OSC4	30	134	O	Ceramic oscillation output pin
K00–K03	70–67	34–31	I	Input pin
K10–K12	66–64	30–28	I	Input pin
K13	63	27	I	Input pin (can be used as external clock input pin for event counter)
P00–P03	62–59	26–23	I/O	I/O pin
P10–P13	58–55	22–19	I/O	I/O pin (switching to serial I/F input/output is possible by software)
P20	54	18	I/O	I/O pin
P21	53	17	I/O	I/O pin
P22	52	16	I/O	I/O pin (switching to CL signal output is possible by software)
P23	51	15	I/O	I/O pin (switching to FR signal output is possible by software)
R00	50	14	O	Output pin
R01	49	13	O	Output pin
R02	48	12	O	Output pin (switching to TOUT signal output is possible by software)
R03	47	11	O	Output pin (switching to FOUT signal output is possible by software)
R10–R13	46–43	10–7	O	Output pin
R20–R23	42–39	6–3	O	Output pin
COM0–COM16	23–20, 18–15 86–94	127–120 49–57	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
SEG0–SEG59	14–1 143–110 106–95	119–72 69–58	O	LCD segment output pin
BZ	24	128	O	Sound output pin
SVD	74	37	I	SVD external voltage input pin
$\overline{\text{RESET}}$	32	136	I	Initial reset input pin
$\overline{\text{TEST}}$	33	137	I	Testing input pin
TXD	38	2	O	Serial data output pin for Flash programming
RXD	37	1	I	Serial data input pin for Flash programming
SCLK	36	140	I/O	Serial clock I/O pin for Flash programming
CLKIN	35	139	I	Clock input pin for Flash programming
$\overline{\text{SPRG}}$	71	35	I	Testing input pin for Flash programming
RSTOUT	109	71	O	Flash testing pin (leave it open during normal operation)
V_{DDF}	73	36	–	Flash power (+) supply pin (normally connect to V_{DD} pin)
VEPEXT	107	70	I/O	Flash testing pin (leave it open during normal operation)

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