EPSON

E0C88308

8-bit Single Chip Microcomputer

- Original Architecture Core CPU
- Dot-matrix LCD Driver
- 512K-byte Addressable Space
- Wide-range Operating Voltage (1.8V to 5.5V)
- High Speed Operation in Low Voltage (0.48µsec/3.0V)

■ DESCRIPTION

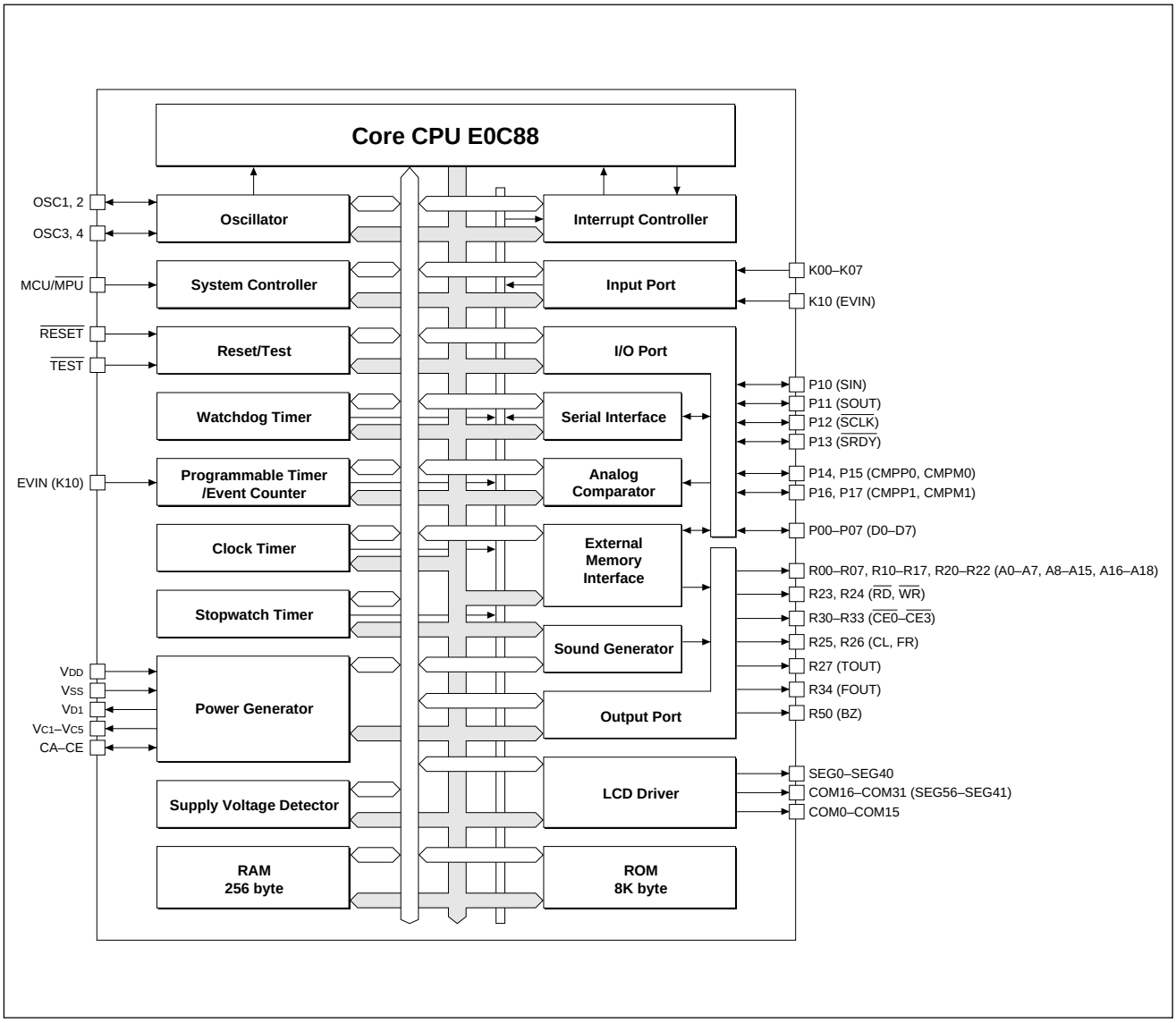
The E0C88308 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU, ROM, RAM, I/O, serial interface, dot-matrix LCD driver, timer and event counter. The E0C88308 is best suited for systems needing a large-sized memory and screen, such as a high performance data bank or an electronic dictionary.

■ FEATURES

- CMOS LSI 8-bit parallel processing
- Clock ..... Twin clock system — Low-speed clock: 32.768kHz; High-speed clock: 4.2MHz (3V) / 8MHz (5V)
- Instruction execution time ..... 0.48µsec (Min.)
- Multiplication and division instructions included
- ROM capacity ..... 8K × 8 bits
- RAM capacity ..... 256 × 8 bits (Working RAM)
  402 × 8 bits (Display RAM)
- Addressing ..... 512K-byte (19 bits)
  Address bus: 19-bit ROM addressing, 19-bit RAM addressing
  (Can be used as general output ports when the address bus is not used.)
  Data bus : 8 bits
  (Can be used as general I/O ports when the data bus is not used.)
  $\overline{CE}$ signal : 4 bits
  $\overline{WR}$ signal : 1 bit
  $\overline{RD}$ signal : 1 bit
  (Can be used as general output ports when the control signals are not used.)
- I/O port ..... Input only : 9 bits (EVIN is available by software)
  Output only : 5 bits (BZ, CL, FR, FOUT and TOUT are available by software)
  Bidirectional I/O : 8 bits ($\overline{SRDY}$, $\overline{SCLK}$, SIN, SOUT, CMPP0, CMPM0, CMPP1 and CMPM1 are available by software)
- Serial interface ..... 1 channel (Clock synchronous or Asynchronous can be selected by software)
- LCD driver ..... Dot-matrix type (5 × 8 or 5 × 5)
  57 segments × 16 commons (1/16 duty, 1/5 bias)
  41 segments × 32 commons (1/32 duty, 1/5 bias)
  Built-in power supply circuit for LCD driver (voltage booster)
  (LCD segments can be expanded with external LCD driver)
- Timer ..... 8-bit programmable timer/event counter : 2 channels
  (16-bit 1 channel timer is available)
  Time base counter (8 bits) : 1 channel
  Stopwatch timer (8 bits) : 1 channel
- Sound generator ..... 8 levels, with envelope, volume adjustment and 1 shot functions

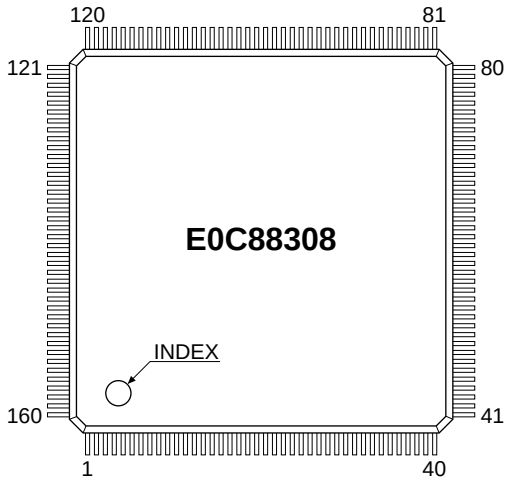
- Watchdog timer ..... Generates NMI
- Supply voltage detection (SVD) circuit .... 16 levels (0.2V steps from 1.8V to 5.5V) can be detected
- Analog comparator ..... 2 channels built-in (Bidirectional I/O port is used as the input port)
- Interrupt ..... External : 2 systems (SCI, K inputs)
  Internal : 4 systems (W/D, PTM/EV, TMB, SW)
- Supply voltage ..... 1.8V to 5.5V
- Current consumption ..... SLEEP mode 200nA (3V) (Low power mode)
  HALT mode 1.0µA (32.768kHz/3V) (Low power mode)
  RUN mode 8.0µA (32.768kHz/3V) (Low power mode)
  1.8mA (4.2MHz/3V) (Normal mode)
- Package ..... QFP8-160pin (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP8-160pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	41	N.C.	81	OSC1	121	N.C.
2	SEG13	42	COM22/SEG50	82	OSC2	122	R06/A6
3	SEG14	43	COM21/SEG51	83	$\overline{\text{TEST}}$	123	R07/A7
4	SEG15	44	COM20/SEG52	84	$\overline{\text{RESET}}$	124	R10/A8
5	SEG16	45	COM19/SEG53	85	MCU/$\overline{\text{MPU}}$	125	R11/A9
6	SEG17	46	COM18/SEG54	86	N.C.	126	R12/A10
7	SEG18	47	COM17/SEG55	87	K10/EVIN	127	R13/A11
8	SEG19	48	COM16/SEG56	88	K07	128	R14/A12
9	SEG20	49	COM15	89	K06	129	R15/A13
10	SEG21	50	COM14	90	K05	130	R16/A14
11	SEG22	51	COM13	91	K04	131	R17/A15
12	SEG23	52	COM12	92	K03	132	R20/A16
13	SEG24	53	COM11	93	K02	133	R21/A17
14	SEG25	54	COM10	94	K01	134	R22/A18
15	SEG26	55	COM9	95	K00	135	R23/$\overline{\text{RD}}$
16	SEG27	56	COM8	96	P17/CMPM1	136	R24/$\overline{\text{WR}}$
17	SEG28	57	COM7	97	P16/CMPP1	137	R25/CL
18	SEG29	58	COM6	98	P15/CMPM0	138	R26/FR
19	SEG30	59	COM5	99	P14/CMPP0	139	R27/TOUT
20	SEG31	60	COM4	100	P13/$\overline{\text{SRDY}}$	140	R30/$\overline{\text{CE0}}$
21	N.C.	61	N.C.	101	P12/$\overline{\text{SCLK}}$	141	N.C.
22	SEG32	62	COM3	102	P11/SOUT	142	R31/$\overline{\text{CE1}}$
23	SEG33	63	COM2	103	P10/SIN	143	R32/$\overline{\text{CE2}}$
24	SEG34	64	COM1	104	P07/D7	144	R33/$\overline{\text{CE3}}$
25	SEG35	65	COM0	105	P06/D6	145	R34/FOUT
26	SEG36	66	CE	106	P05/D5	146	R50/BZ
27	SEG37	67	CD	107	P04/D4	147	SEG0
28	SEG38	68	CC	108	P03/D3	148	SEG1
29	SEG39	69	CB	109	P02/D2	149	SEG2
30	SEG40	70	CA	110	P01/D1	150	SEG3
31	COM31/SEG41	71	V_{C5}	111	P00/D0	151	SEG4
32	COM30/SEG42	72	V_{C4}	112	N.C.	152	SEG5
33	COM29/SEG43	73	V_{C3}	113	N.C.	153	SEG6
34	COM28/SEG44	74	V_{C2}	114	R00/A0	154	SEG7
35	COM27/SEG45	75	V_{C1}	115	R01/A1	155	SEG8
36	COM26/SEG46	76	OSC3	116	R02/A2	156	SEG9
37	COM25/SEG47	77	OSC4	117	R03/A3	157	SEG10
38	COM24/SEG48	78	V_{D1}	118	R04/A4	158	SEG11
39	COM23/SEG49	79	V_{DD}	119	R05/A5	159	SEG12
40	N.C.	80	V_{SS}	120	N.C.	160	N.C.

N.C. : No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	79	–	Power supply (+) terminal
V_{SS}	80	–	Power supply (GND) terminal
V_{D1}	78	–	Regulated voltage output terminal for oscillators
V_{C1}–V_{C5}	75–71	O	LCD drive voltage output terminals
CA–CE	70–66	–	Booster capacitor connection terminals for LCD
OSC1	81	I	OSC1 oscillation input terminal (select crystal oscillation/CR oscillation/external clock input with mask option)
OSC2	82	O	OSC1 oscillation output terminal
OSC3	76	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation/external clock input with mask option)
OSC4	77	O	OSC3 oscillation output terminal
MCU/$\overline{MPU}$	85	I	Terminal for setting MCU or MPU modes
K00–K07	88–95	I	Input port (K00–K07) terminal
K10/EVIN	87	I	Input port (K10) terminal or event counter external clock (EVIN) input terminal
R00–R07 /A0–A7	114–119, 122, 123	O	Output port (R00–R07) terminals or address bus (A0–A7)
R10–R17 /A8–A15	124–131	O	Output port (R10–R17) terminals or address bus (A8–A15)
R20–R22 /A16–A18	132–134	O	Output port (R20–R22) terminals or address bus (A16–A18)
R23/$\overline{RD}$	135	O	Output port (R23) terminal or read signal ($\overline{RD}$) output terminal
R24/$\overline{WR}$	136	O	Output port (R24) terminal or write signal ($\overline{WR}$) output terminal
R25/CL	137	O	Output port (R25) terminal or LCD synchronous signal (CL) output terminal
R26/FR	138	O	Output port (R26) terminal or LCD frame signal (FR) output terminal
R27/TOUT	139	O	Output port (R27) terminal or programmable timer underflow signal (TOUT) output terminal
R30–R33 /$\overline{CE0}$–$\overline{CE3}$	140, 142–144	O	Output port (R30–R33) terminals or chip enable ($\overline{CE0}$–$\overline{CE3}$) output terminals
R34/FOUT	145	O	Output port (R34) terminal or clock (FOUT) output terminal
R50/BZ	146	O	Output port (R50) terminal or buzzer (BZ) output terminal
P00–P07/D0–D7	104–111	I/O	I/O port (P00–P07) terminals or data bus (D0–D7)
P10/SIN	103	I/O	I/O port (P10) terminal or serial I/F data input (SIN) terminal
P11/SOUT	102	I/O	I/O port (P11) terminal or serial I/F data output (SOUT) terminal
P12/$\overline{SCLK}$	101	I/O	I/O port (P12) terminal or serial I/F clock ($\overline{SCLK}$) I/O terminal
P13/$\overline{SRDY}$	100	I/O	I/O port (P13) terminal or serial I/F ready signal ($\overline{SRDY}$) output terminal
P14/CMPP0	99	I/O	I/O port (P14) terminal or comparator 0 non-inverted input terminal
P15/CMPM0	98	I/O	I/O port (P15) terminal or comparator 0 inverted input terminal
P16/CMPP1	97	I/O	I/O port (P16) terminal or comparator 1 non-inverted input terminal
P17/CMPM1	96	I/O	I/O port (P17) terminal or comparator 1 inverted input terminal
COM0–COM15	65–62, 60–49	O	LCD common output terminals
COM16–COM31 /SEG56–SEG41	48–42, 39–31	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 or 1/8 duty is selected)
SEG0–SEG40	147–159, 2–20, 22–30	O	LCD segment output terminals
$\overline{RESET}$	84	I	Initial reset input terminal
$\overline{TEST}$ *	83	I	Test input terminal

* $\overline{TEST}$ is the terminal used for outgoing inspection of the IC. For normal operation be sure it is connected to V_{DD}.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Rating	Symbol	Condition	Value	Unit	Note
Power voltage	V_{DD}		-0.3 to +7.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	2
Operating temperature	Topr		-40 to +85	°C	
Storage temperature	Tstg		-65 to +150	°C	

Note) 1 Case that to Nch open drain output by the mask option is included.
2 In case of plastic package.

● Recommended Operating Conditions

(V_{SS} = 0V, Ta = -40 to 85°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V_{DD}		1.8		3.5	V	
Operating power voltage (High speed mode)	V_{DD}		3.5		5.5	V	
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5V	30	32.768	50	kHz	3
	f_{OSC3}		0.03		4.2	MHz	3
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 3.5V	30	32.768	50	kHz	3
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5V	30	32.768	50	kHz	3
	f_{OSC3}		0.03		8.2	MHz	3
Liquid crystal power voltage	V_{C5}	$V_{C5} \geq V_{C4} \geq V_{C3} \geq V_{C2} \geq V_{C1} \geq V_{SS}$			6.0	V	4
Capacitor between V_{D1} and V_{SS}	C1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C2			0.1		µF	5
Capacitor between V_{C2} and V_{SS}	C3			0.1		µF	5
Capacitor between V_{C3} and V_{SS}	C4			0.1		µF	5
Capacitor between V_{C4} and V_{SS}	C5			0.1		µF	5
Capacitor between V_{C5} and V_{SS}	C6			0.1		µF	5
Capacitor between CA and CB	C7			0.1		µF	5
Capacitor between CA and CC	C8			0.1		µF	5
Capacitor between CD and CE	C9			0.1		µF	5
Resistor between V_{C1} and V_{SS}	R1			100		kΩ	6

Note) 3 When an external clock is input from the OSC1 terminal by the mask option, do not connect anything to the OSC2 terminal, and when an external clock is input from the OSC3 terminal, do not connect to the OSC4 terminal.
4 When external power supply is selected by the mask option.
5 When LCD drive power is not used, the capacitor is not necessary. In this case, do not connect anything to V_{C1} to V_{C5} and CA to CE terminals.
6 It is necessary when the panel load is large and for 1/32 duty driving. The resistance value should be decided by connecting it to the actual panel to be used.

● DC Characteristics

(Unless otherwise specified: V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx, MCU/$\overline{MPU}$	0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Kxx, Pxx, MCU/$\overline{MPU}$	0		0.2V_{DD}	V	
High level input voltage (2) (Normal mode)	V_{IH2}	OSC1, OSC3	1.6		V_{DD}	V	7
High level input voltage (2) (Low power mode)	V_{IH2}	OSC1	1.0		V_{DD}	V	7
High level input voltage (2) (High speed mode)	V_{IH2}	OSC1, OSC3	2.4		V_{DD}	V	7
Low level input voltage (2) (Normal mode)	V_{IL2}	OSC1, OSC3	0		0.6	V	7
Low level input voltage (2) (Low power mode)	V_{IL2}	OSC1	0		0.3	V	7
Low level input voltage (2) (High speed mode)	V_{IL2}	OSC1, OSC3	0		0.9	V	7
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	100		500	kΩ	8
Input terminal capacitance	C_{IN}	Kxx, Pxx, V_{IN} = 0V, f = 1MHz, Ta = 25°C			15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1V	5			µA	

Note) 7 When external clock is selected by mask option.
8 When addition of pull-up resistor is selected by mask option.

● SVD Circuit

(Unless otherwise specified: V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = 25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.82	Typ×1.08	V	
		Level 2 → Level 1		2.00		V	
		Level 3 → Level 2		2.18		V	
		Level 4 → Level 3		2.36		V	
		Level 5 → Level 4		2.54		V	
		Level 6 → Level 5		2.72		V	
		Level 7 → Level 6		2.90		V	
		Level 8 → Level 7		3.08		V	
		Level 9 → Level 8		3.26		V	
		Level 10 → Level 9	Typ×0.88	3.45	Typ×1.12	V	
		Level 11 → Level 10		3.65		V	
		Level 12 → Level 11		3.85		V	
		Level 13 → Level 12		4.05		V	
		Level 14 → Level 13		4.25		V	
		Level 15 → Level 14		4.50		V	

● Analog Comparator

(Unless otherwise specified: V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = 25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog comparator operating voltage input range	V_{CMIP}	Non-inverted input (CMPP)	0.7		V_{DD} - 0.7	V	9
	V_{CMIM}	Inverted input (CMPM)	0.7		V_{DD} - 0.7	V	9
Analog comparator offset voltage	V_{CMOF}	V_{CMIP} = 0.7V to V_{DD} - 0.7V V_{CMIM} = 0.7V to V_{DD} - 0.7V			20	mV	9
Analog comparator stability time	t_{CMP1}				1	mS	10
Analog comparator response time	t_{CMP2}	V_{CMIP} = 0.7V to V_{DD} - 0.7V V_{CMIM} = 0.7V to V_{DD} - 0.7V V_{CMIP} = V_{CMIM} ± 0.025V			2	mS	9 11

Note) 9 When "without pull-up resistor" (comparator input terminal) is selected by mask option.
10 Stability time is the time from turning the circuit ON until the circuit is stabilized.
11 Response time is the time that the output result responds to the input signal.

● Current Consumption

(Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0V, Ta = 25°C,
OSC1 = 32.768kHz crystal oscillation, C_G = 25pF, OSC3 = External clock input, Non heavy load protection mode, C1–C9 = 0.1µF, No panel load)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status *1		0.3	1	µA	
	I_{DD2}	In HALT status *2		2	5	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		14	18	µA	
	I_{DD4}	CPU is in operating (1MHz) *4		0.45	0.60	mA	
	I_{HVL}	In heavy load protection mode		25	50	µA	12
Power current (Low power mode)	I_{DD1}	In SLEEP status *1		0.2	1	µA	
	I_{DD2}	In HALT status *2		1	5	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		8	12	µA	
	I_{HVL}	In heavy load protection mode		15	30	µA	12
Power current (High speed mode)	I_{DD1}	In SLEEP status *1		1	3	µA	
	I_{DD2}	In HALT status *2		5	10	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		24	30	µA	
	I_{DD4}	CPU is in operating (1MHz) *4		0.70	1.00	mA	
	I_{HVL}	In heavy load protection mode		35	70	µA	12
LCD drive circuit current	I_{LCDN}			2.5	5	µA	
	I_{LCDH}	In heavy load protection mode		15	30	µA	12
SVD circuit current	I_{SVDN}	V_{DD} = 3.0V		30	60	µA	13
	I_{SVDH}	In heavy load protection mode		25	75	µA	12
Analog comparator circuit current	I_{CMP1}	CMPXDT = "1"		40	100	µA	
	I_{CMP2}	CMPXDT = "0"		4	10	µA	
OSC1 CR oscillation current	I_{CR1}			20	50	µA	14

*1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
*2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
*3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768kHz, Clock timer: Operating, Others: Stop status
*4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 1MHz, Clock timer: Operating, Others: Stop status

Note) 12 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).
13 The value in x V can be found by the following expression:
I_{SVDN} (V_{DD} = x V) = (x × 20) - 30 (Typ. value), I_{SVDN} (V_{DD} = x V) = (x × 30) - 30 (Max. value)
14 When OSC1 CR oscillation circuit is selected by the mask option.

● LCD Driver

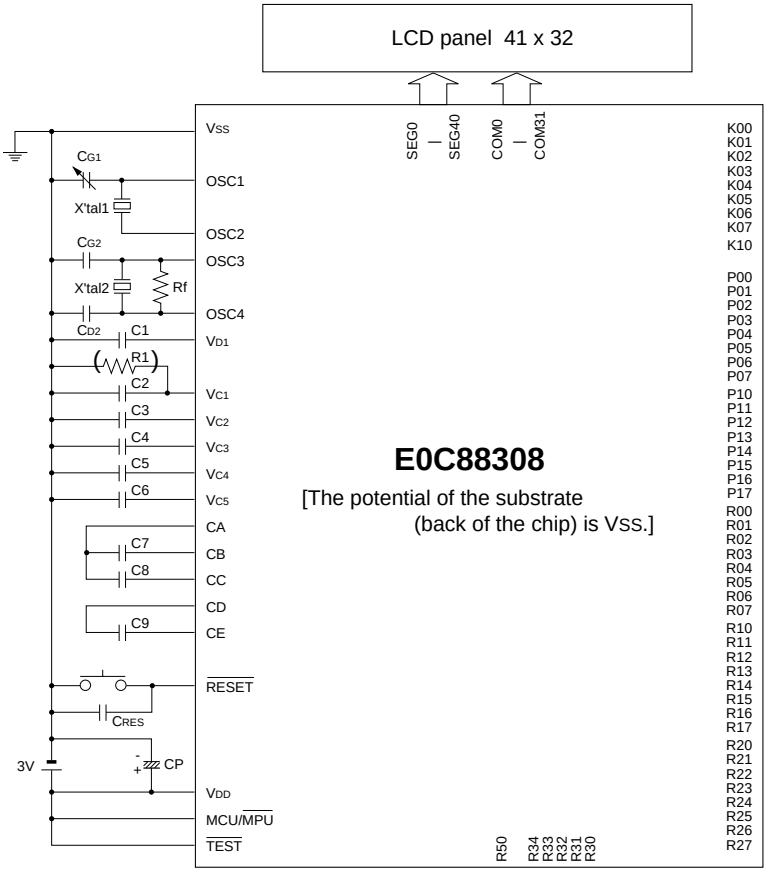
The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number). Therefore, these should be evaluated by connecting to the actual panel to be used. Moreover, if the display is uneven with a large panel load, connect a resistor (R1) between the V_{SS} and V_{C1} terminal. (it is necessary in 1/32 duty driving.)

(Unless otherwise specified: V_{DD} = V_{C2} (LCX = FH) +0.1 to 5.5V, V_{SS} = 0V, Ta = 25°C, C1–C9 = 0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	*1		0.18V_{C5}		0.22V_{C5}	V	
	V_{C2}	*2		0.39V_{C5}		0.43V_{C5}	V	
	V_{C3}	*3		0.59V_{C5}		0.63V_{C5}	V	
	V_{C4}	*4		0.80V_{C5}		0.84V_{C5}	V	
	V_{C5} TYPE A (4.5V)	*5	LCX = 0H		3.89		V	
			LCX = 1H		3.96		V	
			LCX = 2H		4.04		V	
			LCX = 3H		4.11		V	
			LCX = 4H		4.18		V	
			LCX = 5H		4.26		V	
			LCX = 6H		4.34		V	
			LCX = 7H	Typ×0.94	4.42	Typ×1.06	V	
			LCX = 8H		4.50		V	
			LCX = 9H		4.58		V	
			LCX = AH		4.66		V	
			LCX = BH		4.74		V	
			LCX = CH		4.82		V	
			LCX = DH		4.90		V	
			LCX = EH		4.99		V	
			LCX = FH		5.08		V	
	V_{C5} TYPE B (5.5V)	*5	LCX = 0H		4.73		V	
			LCX = 1H		4.83		V	
			LCX = 2H		4.92		V	
			LCX = 3H		5.02		V	
			LCX = 4H		5.11		V	
			LCX = 5H		5.21		V	
			LCX = 6H		5.30		V	
			LCX = 7H	Typ×0.94	5.40	Typ×1.06	V	
			LCX = 8H		5.50		V	
			LCX = 9H		5.60		V	
			LCX = AH		5.70		V	
			LCX = BH		5.81		V	
			LCX = CH		5.93		V	
			LCX = DH		6.05		V	
			LCX = EH		6.17		V	
			LCX = FH		6.29		V	

∗1 Connects 1MΩ load resistor between V_{SS} and V_{C1}.
∗2 Connects 1MΩ load resistor between V_{SS} and V_{C2}.
∗3 Connects 1MΩ load resistor between V_{SS} and V_{C3}.
∗4 Connects 1MΩ load resistor between V_{SS} and V_{C4}.
∗5 Connects 1MΩ load resistor between V_{SS} and V_{C5}.

■ BASIC EXTERNAL CONNECTION DIAGRAM

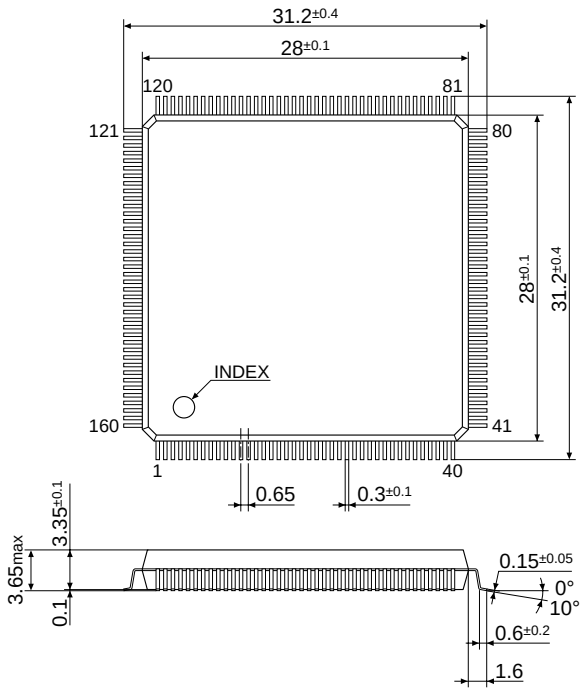


Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768kHz, CI (Max.) = 35kΩ
X'tal2	Crystal oscillator	4.9152MHz
Rf	Feedback resistor	1MΩ
C_{G1}	Trimmer capacitor	5–25pF
C_{G2}	Gate capacitor	15pF
C_{D2}	Drain capacitor	15pF
C1	Capacitor between V_{SS} and V_{D1}	0.1µF
C2	Capacitor between V_{SS} and V_{C1}	0.1µF
C3	Capacitor between V_{SS} and V_{C2}	0.1µF
C4	Capacitor between V_{SS} and V_{C3}	0.1µF
C5	Capacitor between V_{SS} and V_{C4}	0.1µF
C6	Capacitor between V_{SS} and V_{C5}	0.1µF
C7–C9	Booster capacitors	0.1µF
CP	Capacitor for power supply	3.3µF
C_{RES}	Capacitor for $\overline{RESET}$ terminal	0.47µF
R1	Load resistor between V_{SS} and V_{C1}	100 kΩ (It is needed when driving an LCD panel that constitutes a heavy load.)

■ PACKAGE DIMENSIONS

Plastic QFP8-160pin



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