EPSON

E0C88408

8-bit Single Chip Microcomputer

- Original Architecture Core CPU
- Low Voltage Operation (1.8V min.)
- High Speed Operation (0.244µsec/3.0V)
- Built-in LCD Controller
- Built-in Display RAM (Max. 3.5KB)

■ DESCRIPTION

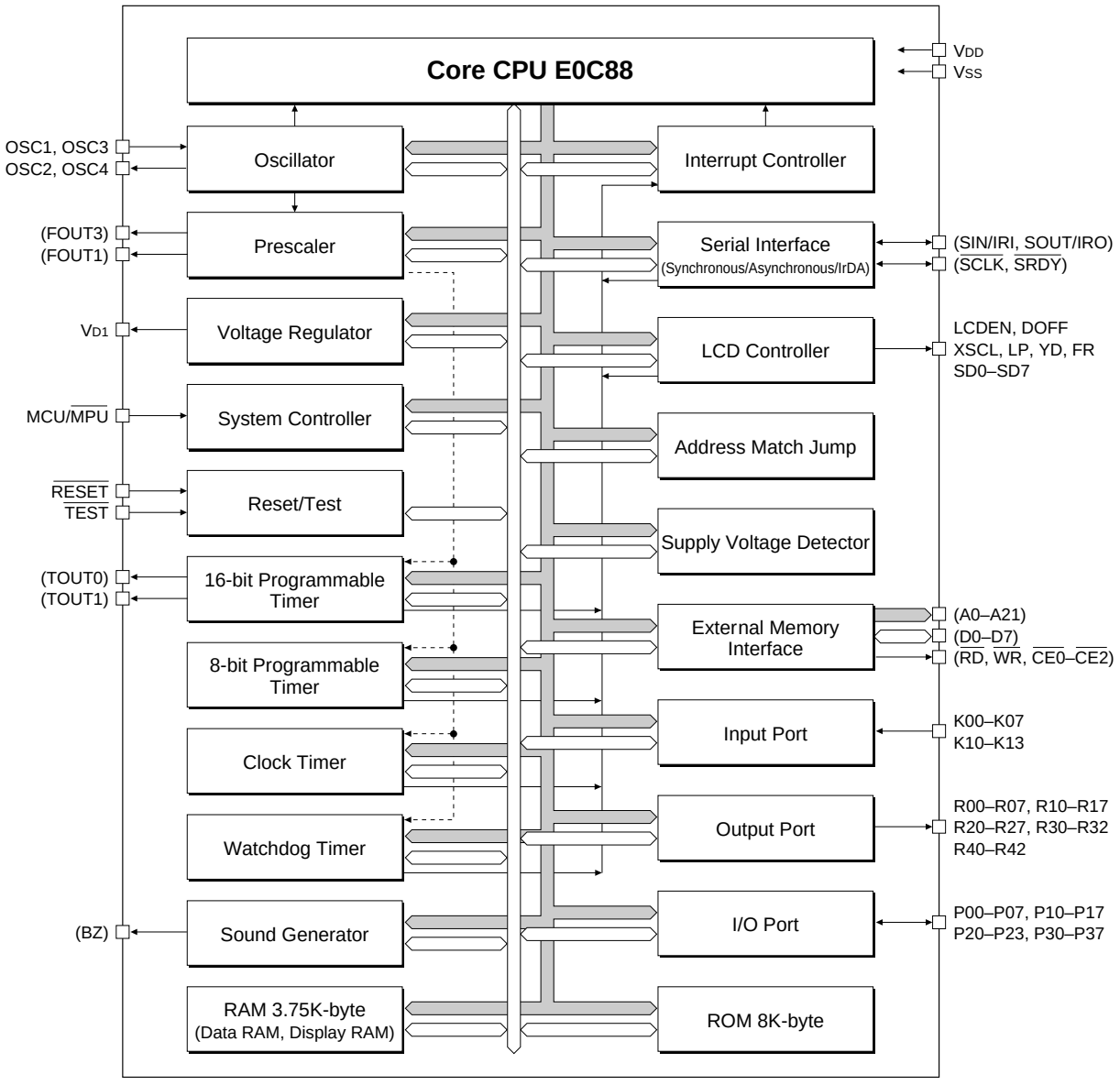
The E0C88408 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU, ROM, RAM, LCD controller and Display RAM. So that the E0C88408 can drive mid size LCD panel (for example, 160 × 100 dots). Therefor the E0C88408 is suitable for organizer and educational computer with mid size LCD display.

■ FEATURES

- CMOS LSI 8-bit parallel processing
- Clock ..... Twin clock system Low-speed clock: 32.768kHz
  High-speed clock: 4.2MHz / 8.2MHz
- Instruction execution time ..... 0.48µsec (Min.)
- Multiplication and division instructions included
- ROM capacity ..... 8K × 8 bits
- RAM capacity ..... 3.75K × 8 bits (Can be chosen as data RAM or display RAM by option swich)
- Addressing ..... 4M-byte (22 bits)
  Address bus: 22-bit ROM addressing, 22-bit RAM addressing
  (Can be used as general output ports when the address bus is not used.)
  Data bus : 8 bits
  (Can be used as general I/O ports when the data bus is not used.)
  $\overline{CE}$ signal : 3 bits
  $\overline{WR}$ signal : 1 bit
  $\overline{RD}$ signal : 1 bit
  (Can be used as general output ports when the control signals are not used.)
- I/O port ..... Input only : 12 bits (EXCL0 or EXCL1 is available by software)
  Output only : 30 bits (BZ, FOUT and TOUT are available by software)
  LCD interface : 14 bits (SD0–SD7, XSCL, LP, FR, DOFF, YD and LCDEN are available by software)
  Bidirectional I/O : 28 bits ($\overline{SRDY}$, $\overline{SCLK}$, SIN and SOUT are available by software)
- Serial interface ..... 1 channel (Clock synchronous or Asynchronous can be selected by software, available for IrDA protocol)
- LCD controller ..... Dot-matrix type (size programmable) controller built-in
  LCD function can be implemented with external segment driver (SED1606 or SED1570) common driver (SED1635)
- Supply voltage detection (SVD) circuit .... 3 levels (1.9, 2.8, 3.4V) can be detected
- Timer ..... 8-bit programmable timer/event counter : 2 channels
  (16-bit 1 channel timer is available)
  8-bit programmable for SIO baud rate generator
  Time base counter : 1 channel (Include 60 seconds)
- Watchdog timer ..... Generates NMI
- Address mach jump ..... Internal ROM op-code fech address mach jump circuit (4 vectors)

- Sound generator ..... 8 levels, with envelope, volume adjustment and 1 shot functions
- Interrupt ..... External : 2 systems
  Internal : 6 systems
- Supply voltage ..... 1.8V to 5.5V
- Current consumption ..... SLEEP mode 500nA (3V)
  HALT mode 3µA (32.768kHz/3V)
  RUN mode 14µA (32.768kHz/3V)
  2mA (8.2MHz/5V)
- Package ..... Die form or QFP15-100pin

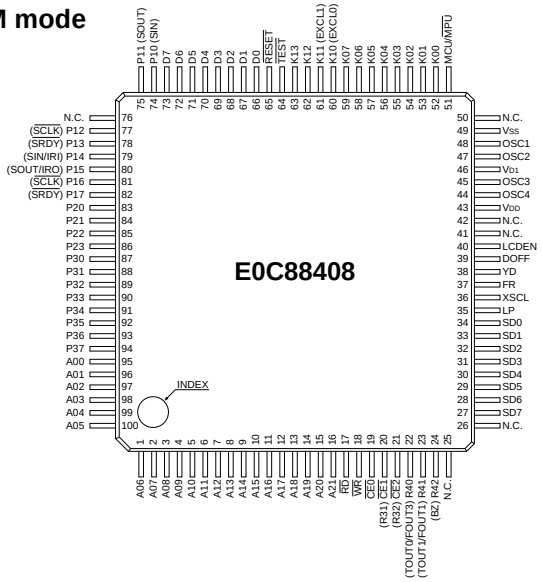
■ BLOCK DIAGRAM



∗ The terminals that are shown in ( ) are shared with Pxx or Rxx terminals.

■ PIN CONFIGURATION

• Pin layout for expanded 4M mode (for multi-chip system)



■ PIN DESCRIPTION

Pin name	Pin No.	I/O	Function
V_{DD}	43	–	Power supply (+) pin
V_{SS}	49	–	Power supply (GND) pin
V_{D1}	46	O	Voltage regulator output pin
OSC1	48	I	OSC1 oscillation input pin (32 kHz crystal, CR oscillation, external clock input)
OSC2	47	O	OSC1 oscillation output pin
OSC3	45	I	OSC3 oscillation input pin (crystal/ceramic, CR oscillation, external clock input)
OSC4	44	O	OSC3 oscillation output pin
MCU/$\overline{\text{MPU}}$	51	I	MCU/MPU mode stting pin
K00–K07	52–59	I	Input port pin
K10 (EXCL00)	60	I	Input port pin or external clock input pin for event counter (Timer 0)
K11 (EXCL01)	61	I	Input port pin or external clock input pin for event counter (Timer 1)
K12–K13	62–63	I	Input port pin
A00–A21	95–100, 1–16	O	Address bus
$\overline{\text{RD}}$	17	O	Read signal output pin
$\overline{\text{WR}}$	18	O	Write signal output pin
$\overline{\text{CE0}}$	19	O	Chip enable signal output pin
$\overline{\text{CE1}}$ (R31)	20	O	Chip enable signal output pin or output port pin
$\overline{\text{CE2}}$ (R32)	21	O	Chip enable signal output pin or output port pin
R40 (TOUT0/FOUT3)	22	O	Output port pin or TOUT0/FOUT3 clock output pin
R41 (TOUT1/FOUT1)	23	O	Output port pin or TOUT1/FOUT1 clock output pin
R42 (BZ)	24	O	Output port pin or buzzer signal output pin
D0–D7	66–73	I/O	Data bus
P10 (SIN)	74	I/O	I/O port pin or serial I/F data input pin
P11 (SOUT)	75	I/O	I/O port pin or serial I/F data output pin
P12 ($\overline{\text{SCLK}}$)	77	I/O	I/O port pin or serial I/F clock input/output pin
P13 ($\overline{\text{SRDY}}$)	78	I/O	I/O port pin or serial I/F ready signal output pin
P14 (SIN/IRI)	79	I/O	I/O port pin, serial I/F data input or IR receiver input pin
P15 (SOUT/IRO)	80	I/O	I/O port pin, serial I/F data output or IR transmitter output pin
P16 ($\overline{\text{SCLK}}$)	81	I/O	I/O port pin or serial I/F clock input/output pin
P17 ($\overline{\text{SRDY}}$)	82	I/O	I/O port pin or serial I/F ready signal output pin
P20–P23	83–86	I/O	I/O port pin
P30–P37	87–94	I/O	I/O port pin
LCDEN	40	O	LCD controller enable signal output pin
DOFF	39	O	LCD controller forced blank signal output pin
YD	38	O	LCD controller scan start pulse output pin
FR	37	O	LCD controller frame signal output pin
XSCL	36	O	LCD controller shift clock output pin
LP	35	O	LCD controller latch pulse output pin
SD0–SD7	34–27	O	LCD controller data output pin
$\overline{\text{RESET}}$	65	I	Initial reset input pin
$\overline{\text{TEST}}$	64	I	Test input pin∗1

∗1 $\overline{\text{TEST}}$ is the terminal used for factory inspection of the IC. For normal operation, be sure to connect the $\overline{\text{TEST}}$ terminal to V_{DD}.

(Note) The pin configuration is different from that of single-chip mode or expanded 64K mode. Please refer to the technical manual before designing the system.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0 V)

Item	Symbol	Condition	Value	Unit	Note
Supply voltage	V_{DD}		-0.3 to V_{DD}+0.3	V	
Input voltage	V_I		-0.3 to V_{DD}+0.3	V	
Output voltage	V_O		-0.3 to V_{DD}+0.3	V	
High-level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low-level output current	I_{OL}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Operating temperature	Topr		-20 to +70	°C	
Storage temperature	Tstg		-65 to +150	°C	
Permissible disspation	P_D	Ta=25°C	200	mW	1

Note) 1. In case of plastic package.

● Recommended Operating Conditions

(V_{SS}=0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{DD}		1.8		5.5	V	
Clock frequency	f_{OSC1}	V_{DD}=1.8 to 5.5 V	30.000	32.768	50.000	kHz	1
	f_{OSC3}	V_{DD}=1.8 to 5.5 V	0.03		1.1	MHz	1
		V_{DD}=2.6 to 5.5 V	0.03		4.4	MHz	1
		V_{DD}=3.5 to 5.5 V	0.03		8.2	MHz	1
Operating temperature	Topr		-20		+70	°C	
Capacitor between V_{SS} and V_{D1}	C_1			0.1		µF	

Note) 1. When an external clock is input from the OSC1 terminal by setting the mask option, do not connect anything to the OSC2 terminal. When an external clock is input from the OSC3 terminal, do not connect anything to the OSC4 terminal.

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=-20 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High-level input voltage	V_{IH1}	Pxx, MCU/$\overline{MPU}$, Kxx	0.8V_{DD}		V_{DD}	V	
Low-level input voltage	V_{IL1}	Pxx, MCU/$\overline{MPU}$, Kxx	0		0.2V_{DD}	V	
High-level input voltage	V_{IH2}	OSC1, OSC3, V_{D1}=1.6 V	1.3		V_{DD}	V	1,3
		OSC1, OSC3, V_{D1}=2.4 V	1.8		V_{DD}	V	1,4
		OSC1, OSC3, V_{D1}=3.2 V	2.4		V_{DD}	V	1,5
Low-level input voltage	V_{IL2}	OSC1, OSC3, V_{D1}=1.6 V	0		0.3	V	1,3
		OSC1, OSC3, V_{D1}=2.4 V	0		0.6	V	1,4
		OSC1, OSC3, V_{D1}=3.2 V	0		0.8	V	1,5
High-level schmitt trigger input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low-level schmitt trigger input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
Schmitt trigger hysteresis voltage	V_{HS}	$\overline{RESET}$, V_{HS}=V_{T+}–V_{T-}	0.2			V	
High-level output current	I_{OH}	Pxx, Rxx, V_{OH}=V_{DD}-0.2 V	-0.5			mA	6
Low-level output current	I_{OL}	Pxx, Rxx, V_{OL}=0.2 V			0.5	mA	6
Input leak current	I_{LI1}	Kxx, Pxx, MCU/$\overline{MPU}$, $\overline{RESET}$	-1		1	µA	
Input leak current	I_{LI2}	OSC1, OSC3	-1		1	µA	1
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, MCU/$\overline{MPU}$, $\overline{RESET}$	100		500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx, V_{IN}=0 V, ϕ=1 MHz, Ta=25°C			15	pF	

Note) 1. When external clock is selected by mask option.
2. When pull-up resistor is added by mask option.
3. Low-power mode (VD1C1 = "0", VD1C0 = "1")
4. Normal mode (VD1C1 = "0", VD1C0 = "0")
5. High-speed mode 1 (VD1C1 = "1", VD1C0 = X)
6. Characteristics when only one terminal is driven. If two or more terminals are driven simultaneously, the characteristics had happen to reduced because the V_{OH} and V_{OL} voltages drop due to the parasitic resistance on the power line in the IC.

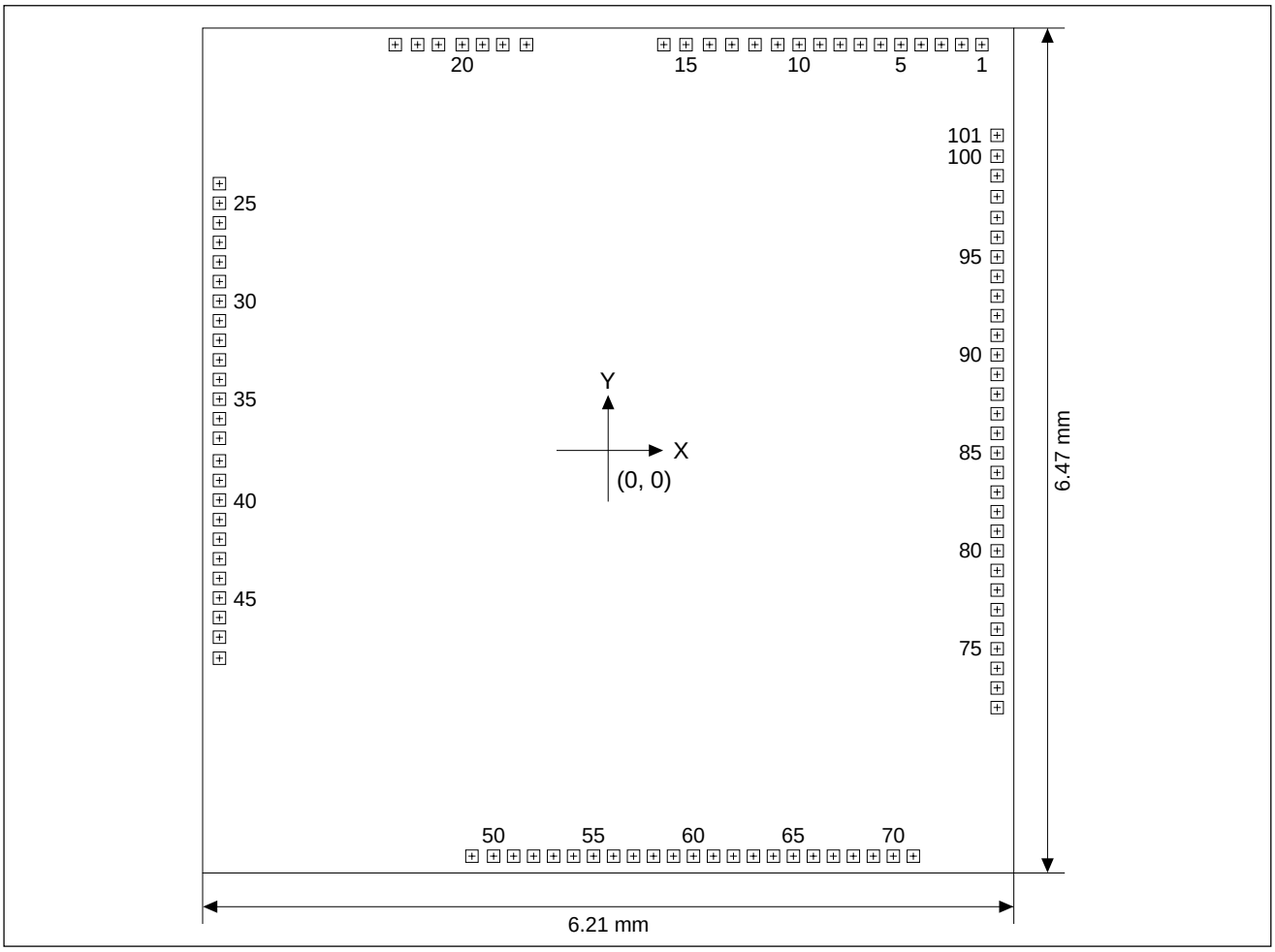
● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=25°C, OSC1=32.768 kHz crystal oscillation, OSC3=external clock input)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	SVD1="1", SVD0=X	3.05	3.4	3.75	V	
		SVD1="0", SVD0="1"	2.55	2.8	3.05	V	
		SVD1="0", SVD0="0"	1.7	1.9	2.1	V	
SVD circuit response time	t_{SVD}				100	µs	
Power current	I_{DD1}	In SLEEP status		0.45	1.0	µA	1
Low-power mode	I_{DD2}	In HALT status		1.8	5.0	µA	2
VD1C1="0", VD1C0="1"	I_{DD3}	CPU is in operating (32.768 kHz)		9.0	20.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.3	0.5	mA	4
Power current	I_{DD1}	In SLEEP status		0.55	1.5	µA	1
Normal mode	I_{DD2}	In HALT status		3.0	7.0	µA	2
VD1C1="0", VD1C0="0"	I_{DD3}	CPU is in operating (32.768 kHz)		14.0	25.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.45	0.7	mA	4
Power current	I_{DD1}	In SLEEP status		0.65	2.0	µA	1
High-speed mode	I_{DD2}	In HALT status		5.0	12.0	µA	2
VD1C1="1", VD1C0=X	I_{DD3}	CPU is in operating (32.768 kHz)		21.0	35.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.65	1.0	mA	4
SVD circuit current	I_{DD1}	V_{DD}=5.0 V		7	15	µA	5
OSC1 CR oscillation current	I_{SVDN}	R_{CR}=1.5 MΩ, normal mode		20	50	µA	6

Note) 1. OSC1: Stop OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Stop SVD: Off Others: Stop
2. OSC1: On OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Run SVD: Off Others: Stop
3. OSC1: On OSC3: Stop CPU, ROM, RAM: Run Clock Timer: Run SVD: Off Others: Stop
4. OSC1: On OSC3: On CPU, ROM, RAM: Run Clock Timer: Run SVD: Off Others: Stop
5. OSC1: On OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Run SVD: On Others: Stop
6. When the OSC1 CR oscillation circuit is selected by mask option.

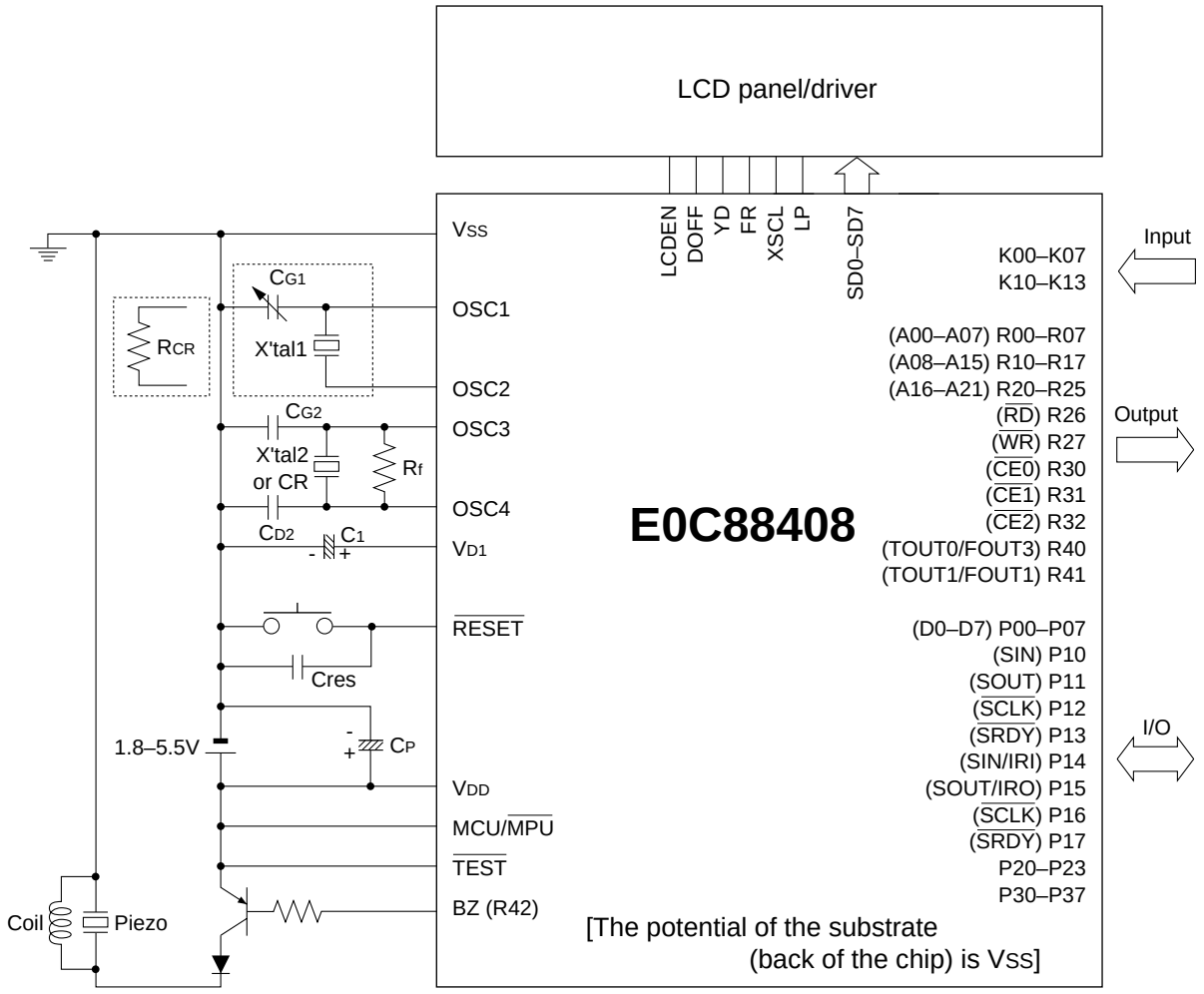
■ Diagram of Pad Layout



■ Pad Coordinates

No.	Pad name	X	Y	No.	Pad name	X	Y
1	N.C.	2,860	3,107	52	P15 (SOUT/IRO)	-572	-3,107
2	N.C.	2,705	3,107	53	P16 ($\overline{\text{SCLK}}$)	-419	-3,107
3	SD7	2,550	3,107	54	P17 ($\overline{\text{SRDY}}$)	-266	-3,107
4	SD6	2,395	3,107	55	P20	-113	-3,107
5	SD5	2,240	3,107	56	P21	40	-3,107
6	SD4	2,085	3,107	57	P22	193	-3,107
7	SD3	1,930	3,107	58	P23	346	-3,107
8	SD2	1,775	3,107	59	P30	499	-3,107
9	SD1	1,620	3,107	60	P31	652	-3,107
10	SD0	1,461	3,107	61	P32	805	-3,107
11	LP	1,297	3,107	62	P33	958	-3,107
12	XSCL	1,123	3,107	63	P34	1,111	-3,107
13	FR	946	3,107	64	P35	1,264	-3,107
14	YD	775	3,107	65	P36	1,417	-3,107
15	DOFF	595	3,107	66	P37	1,570	-3,107
16	LCDEN	425	3,107	67	R00 (A00)	1,723	-3,107
17	V_{DD}	-626	3,107	68	R01 (A01)	1,876	-3,107
18	OSC4	-808	3,107	69	R02 (A02)	2,029	-3,107
19	OSC3	-963	3,107	70	R03 (A03)	2,182	-3,107
20	V_{D1}	-1,118	3,107	71	R04 (A04)	2,335	-3,107
21	OSC2	-1,300	3,107	72	R05 (A05)	2,977	-1,969
22	OSC1	-1,460	3,107	73	R06 (A06)	2,977	-1,819
23	V_{SS}	-1,631	3,107	74	R07 (A07)	2,977	-1,669
24	MCU/$\overline{\text{MPU}}$	-2,977	2,043	75	R10 (A08)	2,977	-1,519
25	K00	-2,977	1,893	76	R11 (A09)	2,977	-1,369
26	K01	-2,977	1,743	77	R12 (A10)	2,977	-1,219
27	K02	-2,977	1,593	78	R13 (A11)	2,977	-1,069
28	K03	-2,977	1,443	79	R14 (A12)	2,977	-919
29	K04	-2,977	1,293	80	R15 (A13)	2,977	-769
30	K05	-2,977	1,143	81	R16 (A14)	2,977	-619
31	K06	-2,977	993	82	R17 (A15)	2,977	-469
32	K07	-2,977	843	83	R20 (A16)	2,977	-319
33	K10 (EXCL00)	-2,977	693	84	R21 (A17)	2,977	-169
34	K11 (EXCL01)	-2,977	543	85	R22 (A18)	2,977	-19
35	K12	-2,977	393	86	R23 (A19)	2,977	132
36	K13	-2,977	243	87	R24 (A20)	2,977	282
37	$\overline{\text{TEST}}$	-2,977	93	88	R25 (A21)	2,977	432
38	$\overline{\text{RESET}}$	-2,977	-80	89	R26 ($\overline{\text{RD}}$)	2,977	583
39	P00 (D0)	-2,977	-230	90	R27 ($\overline{\text{WR}}$)	2,977	733
40	P01 (D1)	-2,977	-380	91	R30 ($\overline{\text{CE0}}$)	2,977	883
41	P02 (D2)	-2,977	-530	92	R31 ($\overline{\text{CE1}}$)	2,977	1,033
42	P03 (D3)	-2,977	-680	93	R32 ($\overline{\text{CE2}}$)	2,977	1,183
43	P04 (D4)	-2,977	-830	94	R40 (TOUT0/FOUT3)	2,977	1,333
44	P05 (D5)	-2,977	-980	95	R41 (TOUT1/FOUT1)	2,977	1,483
45	P06 (D6)	-2,977	-1,130	96	R42 (BZ)	2,977	1,633
46	P07 (D7)	-2,977	-1,280	97	N.C.	2,977	1,783
47	P10 (SIN)	-2,977	-1,430	98	N.C.	2,977	1,943
48	P11 (SOUT)	-2,977	-1,590	99	N.C.	2,977	2,103
49	P12 ($\overline{\text{SCLK}}$)	-1,044	-3,107	100	N.C.	2,977	2,253
50	P13 ($\overline{\text{SRDY}}$)	-878	-3,107	101	N.C.	2,977	2,413
51	P14 (SIN/IRI)	-725	-3,107	–	–	–	–

■ BASIC EXTERNAL CONNECTION DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ
R_{CR}	Resistor for CR oscillation	1.8 Ω
X'tal2	Crystal oscillator	4, 6, 8 MHz
CR	Ceramic oscillator	4, 6, 8 MHz
R_f	Feedback resistor	1 MΩ
C_{G1}	Trimmer capacitor	5–25 pF
C_{G2}	Gate capacitor	15 pF
C_{D2}	Drain capacitor	15 pF
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF

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