MF1285-01

EPSON

CMOS 32-BIT SINGLE CHIP MICROCOMPUTER

E0C332L01 TECHNICAL MANUAL

E0C332L01 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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1 Outline

The E0C332L01 is a Seiko Epson original 32-bit microcomputer with a built-in LCD controller. It features high speed, low power and low-voltage operation and is most suitable for portable equipment that needs display function, such as information terminals, E-mail terminals, electronic dictionaries.
The E0C332L01 consists of the E0C33000 32-bit RISC type CPU as the core, a bus control unit, a DMA controller, an interrupt controller, timers, serial interface circuits, an A/D converter, ROM and RAM. The LCD controller unit is configured with the SEIKO EPSON SED1375 LCD controller and 40K bytes of SRAM display buffer (VRAM), and it allows driving of various LCD panels .
The E0C332L01 provides a DSP function, by using the internal MAC (multiplication and accumulation) operation function with the A/D converter, it makes it possible to design simply speech recognition and voice synthesis systems.

1.1 Features

Core CPU

Seiko Epson original 32-bit RISC CPU E0C33000 built-in

- Basic instruction set: 105 instructions (16-bit fixed size)
- Sixteen 32-bit general-purpose register
- 32-bit ALU and 8-bit shifter
- Multiplication/division instructions and MAC (multiplication and accumulation) instruction are available
- 20 ns of minimum instruction execution time at 50 MHz operation

Internal memory

ROM: 128K bytes
RAM: 8K bytes
VRAM: 40K bytes

Internal peripheral circuits

Oscillation circuit:	High-speed (OSC3) oscillation circuit 33 MHz max.	
	Crystal/ceramic oscillator or external clock input	
	Low-speed (OSC1) oscillation circuit 32.768 kHz typ.	
	Crystal oscillator or external clock input	
LCD controller:	SED1375 with 40KB VRAM	
	4 or 8-bit monochrome/color LCD interface	
	Active matrix TFT/D-TFD interface	
	2, 4 or 16-level (1, 2 or 4 bit-per-pixel) gray-scale display	
	2, 4, 16 or 256-level (1, 2, 4 or 8 bit-per-pixel) color display	
	Resolution examples:	640 × 480 dots with 1bpp color dipth
		640 × 240 dots with 2bpp color dipth
		320 × 240 dots with 4bpp color dipth
		320 × 160 dots with 8bpp color dipth
Timers:	8-bit timer	4 channels
	16-bit timer	6 channels
	Watchdog timer	(16-bit timer 0's function)
	Clock timer	1 channel (with alarm function)
Serial interface:	2 channels (clock-synchronous system, asynchronous system and IrDA interface are selectable)	
A/D converter:	10 bits × 8 channels	
DMA controller:	High-speed DMA	4 channels
	Intelligent DMA	128 channels

Interrupt controller:	Possible to invoke DMA	
	Input interrupt	10 types (programmable)
	DMA controller interrupt	5 types
	16-bit programmable timer interrupt	12 types
	8-bit programmable timer interrupt	4 types
	Serial interface interrupt	6 types
	A/D converter interrupt	1 type
	Clock timer interrupt	1 type
General-purpose input and output ports:	Shared with the I/O pins for internal peripheral circuits	
	Input port	13 bits
	I/O port	29 bits

External bus interface

BCU (bus control unit) built-in

- 24-bit address bus (internal 28-bit processing)
- 16-bit data bus
  Data size is selectable from 8 bits and 16 bits in each area.
- Little-endian memory access; big-endian may be set in each area.
- Memory mapped I/O
- Chip enable and wait control circuits built-in
- DRAM direct interface function built-in
  Supports fast page mode and EDO page mode.
  Supports self-refresh and CAS-before RAS refresh.
- Supports burst ROM.

Operating conditions and power consumption

Operating voltage:	Core (V_{DD})	1.8 V to 3.6 V
	I/O (V_{DDE1})	1.8 V to 5.5 V
	LCD I/F (V_{DDE2})	1.8 V to 5.5 V
Operating clock frequency:	CPU	50 MHz max. (when core voltage = 3.3 V ±0.3 V)
		40 MHz max. (when core voltage = 3.0 V ±0.3 V)
	LCD controller	25 MHz max. (when core voltage = 3.3 V ±0.3 V)
Operating temperature:	-40 to 85°C	
Power consumption:	During SLEEP	4 µW typ.
	During HALT	130 mW typ.
		(3.3 V, 50 MHz, LCD controller enabled)
		100 mW typ.
		(3.3 V, 50 MHz, LCD controller is in power-save mode)
	During execution	230 mW typ.
		(3.3 V, 50 MHz, LCD controller enabled)

Note:
- The values of power consumption during execution were measured when a test program that consisted of 55% load instructions, 23% arithmetic operation instructions, 1% mac instruction, 12% branch instructions and 9% ext instruction was being continuously executed.
- The LCD controller is configured with 640 × 480 display resolution, 1 bpp mode and a 25 MHz operating clock.

Supply form

QFP18-176pin plastic package

1.2 Block Diagram

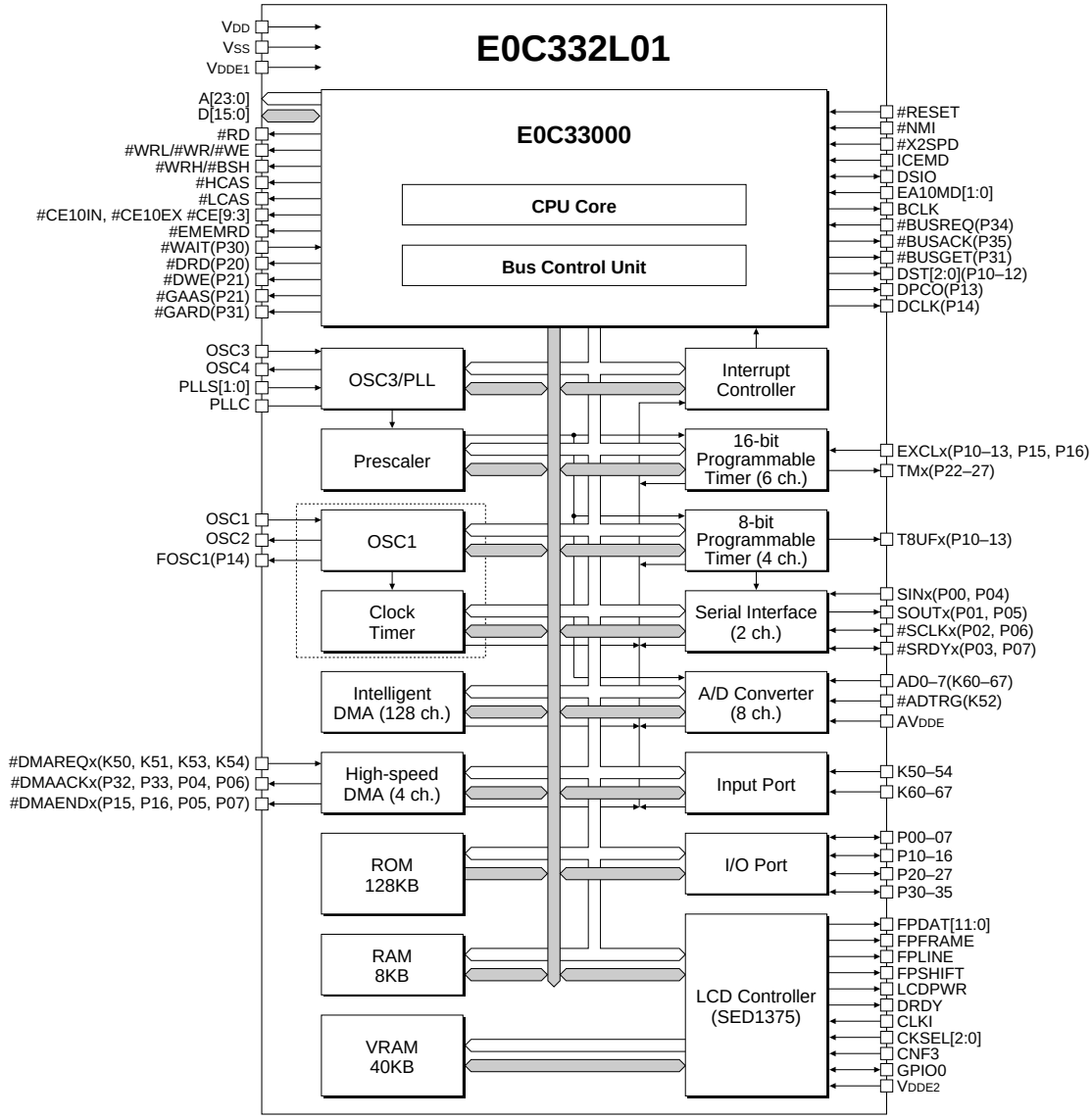
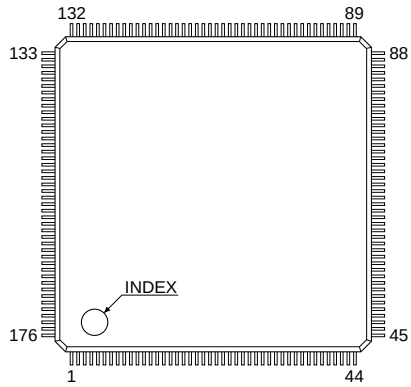


Figure 1.2.1 E0C332L01 Block Diagram

1.3 Pin Description

1.3.1 Pin Layout Diagram (plastic package)

QFP18-176pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	A23	45	D2	89	N.C.	133	P21/#DWE/#GAAS
2	A22	46	D1	90	VSS	134	P20/#DRD
3	A21	47	D0	91	GPIO0	135	P16/EXCL5/#DMAEND1
4	A20	48	VSS	92	FPDAT11/GPIO4/INVERSE	136	P15/EXCL4/#DMAEND0
5	VDDE1	49	BCLK	93	FPDAT10/GPIO3	137	VDDE1
6	A19	50	#EMEMRD	94	FPDAT9/GPIO2	138	P14/FOSC1/DCLK
7	A18	51	#RD	95	VDDE2	139	P13/EXCL3/T8UF3/DPCO
8	A17	52	#WRL/#WR/#WE	96	FPDAT8/GPIO1	140	P12/EXCL2/T8UF2/DST2
9	A16	53	#WRH/#BSH	97	FPSHIFT	141	P11/EXCL1/T8UF1/DST1
10	A15	54	VDDE1	98	FPDAT7	142	P10/EXCL0/T8UF0/DST0
11	VSS	55	#CE10EX/#CE9&10EX	99	FPDAT6	143	VSS
12	A14	56	#CE10IN	100	FPDAT5	144	P07/#SRDY1/#DMAEND3
13	A13	57	#CE3	101	VDD	145	P06/#SCLK1/DMAACK3
14	A12	58	VSS	102	FPDAT4	146	P05/SOUT1/#DMAEND2
15	A11	59	K67/AD7	103	FPDAT3	147	P04/SIN1/#DMAACK2
16	A10	60	K66/AD6	104	FPDAT2	148	VDD
17	VDD	61	K65/AD5	105	FPDAT1	149	OSC2
18	A9	62	AVDDE	106	VSS	150	OSC1
19	A8	63	K64/AD4	107	FPDAT0	151	VSS
20	A7	64	K63/AD3	108	FPLINE	152	P03/#SRDY0
21	A6	65	K62/AD2	109	FPFRAME	153	P02/#SCLK0
22	A5	66	VSS	110	DRDY/MOD/FPSHIFT2	154	P01/SOUT0
23	VSS	67	K61/AD1	111	VDDE2	155	P00/SIN0
24	A4	68	K60/AD0	112	LCDPWR	156	CNF3
25	A3	69	K54/#DMAREQ3	113	N.C.	157	CKSEL2
26	A2	70	K53/#DMAREQ2	114	N.C.	158	CKSEL1
27	A1	71	K52/#ADTRG	115	N.C.	159	CKSEL0
28	A0/#BSL	72	VDD	116	N.C.	160	VDDE1
29	VDDE1	73	K51/#DMAREQ1	117	N.C.	161	CLKI
30	D15	74	K50/#DMAREQ0	118	VSS	162	ICEMD
31	D14	75	#LCAS	119	P35/#BUSACK	163	VSS
32	D13	76	#HCAS	120	P34/#BUSREQ/#CE6	164	OSC4
33	D12	77	#CE9/#CE17/#CE17&18	121	P33/#DMAACK1	165	OSC3
34	D11	78	VSS	122	P32/#DMAACK0	166	EA10MD1
35	VSS	79	#CE8/#RAS1/#CE14/#RAS3	123	P31/#BUSGET/#GARD	167	EA10MD0
36	D10	80	#CE7/#RAS0/#CE13/#RAS2	124	P30/#WAIT/#CE4&5	168	#X2SPD
37	D9	81	#CE5/#CE15/#CE15&16	125	VDD	169	VDD
38	D8	82	#CE4/#CE11/#CE11&12	126	P27/TM5	170	PLLS1
39	D7	83	#CE6/#CE7&8	127	P26/TM4	171	PLLS0
40	D6	84	VDDE1	128	P25/TM3	172	#NMI
41	VDD	85	N.C.	129	P24/TM2	173	VSS
42	D5	86	N.C.	130	P23/TM1	174	PLLC
43	D4	87	N.C.	131	VSS	175	#RESET
44	D3	88	N.C.	132	P22/TM0	176	DSIO

Figure 1.3.1 Pin Layout Diagram (QFP18-176pin)

1.3.2 Pin Functions

Table 1.3.1 List of Pins for Power Supply System

Pin name	Pin No.	I/O	Pull-up	Function
V_{DD}	17,41,72, 101,125, 148,169	–	–	Power supply (+) for the internal logic
V_{SS}	11,23,35,48, 58,66,78,90, 106,118, 131,143 151,163, 173	–	–	Power supply (-); GND
V_{DDE1}	5,29,54,84, 137,160	–	–	Power supply (+) for the I/O block
V_{DDE2}	95,111	–	–	Power supply (+) for the LCD interface
AV_{DDE}	62	–	–	Analog system power supply (+); $AV_{DDE} = V_{DDE}$

Table 1.3.2 List of Pins for External Bus Interface Signals

Pin name	Pin No.	I/O	Pull-up	Function
A0 #BSL	28	O	–	A0: Address bus (A0) when SBUSST(D3/0x4812E) = "0" (default) #BSL: Bus strobe (low byte) signal when SBUSST(D3/0x4812E) = "1"
A[23:1]	1–4,6–10, 12–16, 18–22, 24–27	O	–	Address bus (A1 to A23)
D[15:0]	30–34, 36–40, 42–47	I/O	–	Data bus (D0 to D15)
#CE10EX	55	O	–	Area 10 chip enable for external memory ∗ When CEFUNC[1:0] = "1x", this pin outputs #CE9+#CE10EX signal.
#CE10IN	56	O	–	Area 10 chip enable for internal ROM emulation memory
#CE9 #CE17	77	O	–	#CE9: Area 9 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "00" (default) #CE17: Area 17 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "01" ∗ When CEFUNC[1:0] = "1x", this pin outputs #CE17+#CE18 signal.
#CE8 #RAS1 #CE14 #RAS3	79	O	–	#CE8: Area 8 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "00" and A8DRA(D8/0x48128) = "0" (default) #RAS1: Area 8 DRAM row strobe when CEFUNC[1:0](D[A:9])/0x48130) = "00" and A8DRA(D8/0x48128) = "1" #CE14: Area 14 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "01" or "1x" and A14DRA(D8/0x48122) = "0" #RAS3: Area 14 DRAM row strobe when CEFUNC[1:0](D[A:9])/0x48130) = "01" or "1x" and A14DRA(D8/0x48122) = "1"
#CE7 #RAS0 #CE13 #RAS2	80	O	–	#CE7: Area 7 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "00" and A7DRA(D7/0x48128) = "0" (default) #RAS0: Area 7 DRAM row strobe when CEFUNC[1:0](D[A:9])/0x48130) = "00" and A7DRA(D7/0x48128) = "1" #CE13: Area 13 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "01" or "1x" and A13DRA(D7/0x48122) = "0" #RAS2: Area 13 DRAM row strobe when CEFUNC[1:0](D[A:9])/0x48130) = "01" or "1x" and A13DRA(D7/0x48122) = "1"
#CE6	83	O	–	Area 6 chip enable ∗ When CEFUNC[1:0] = "1x", this pin outputs #CE7+#CE8 signal.
#CE5 #CE15	81	O	–	#CE5: Area 5 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "00" (default) #CE15: Area 15 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "01" ∗ When CEFUNC[1:0] = "1x", this pin outputs #CE15+#CE16 signal.
#CE4 #CE11	82	O	–	#CE4: Area 4 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "00" (default) #CE11: Area 11 chip enable when CEFUNC[1:0](D[A:9])/0x48130) = "01" ∗ When CEFUNC[1:0] = "1x", this pin outputs #CE11+#CE12 signal.

Pin name	Pin No.	I/O	Pull-up	Function
#CE3	57	O	–	Area 3 chip enable
#RD	51	O	–	Read signal
#EMEMRD	50	O	–	Read signal for internal ROM emulation memory
#WRL #WR #WE	52	O	–	#WRL: Write (low byte) signal when SBUSST(D3/0x4812E) = "0" (default) #WR: Write signal when SBUSST(D3/0x4812E) = "1" #WE: DRAM write signal (default)
#WRH #BSH	53	O	–	#WRH: Write (high byte) signal when SBUSST(D3/0x4812E) = "0" (default) #BSH: Bus strobe (high byte) signal when SBUSST(D3/0x4812E) = "1"
#HCAS	76	O	–	#HCAS: DRAM column address strobe (high byte) signal
#LCAS	75	O	–	#LCAS: DRAM column address strobe (low byte) signal
BCLK	49	O	–	Bus clock output
P34 #BUSREQ #CE6	120	I/O	–	P34: I/O port when CFP34(D4/0x402DC) = "0" (default) #BUSREQ: Bus release request input when CFP34(D4/0x402DC) = "1" #CE6: Area 6 chip enable when CFP34(D4/0x402DC) = "1" and IOC34(D4/0x402DE) = "1"
P35 #BUSACK	119	I/O	–	P35: I/O port when CFP35(D5/0x402DC) = "0" (default) #BUSACK: Bus acknowledge output when CFP35(D5/0x402DC) = "1"
P30 #WAIT #CE4&5	124	I/O	–	P30: I/O port when CFP30(D0/0x402DC) = "0" (default) #WAIT: Wait cycle request input when CFP30(D0/0x402DC) = "1" #CE4&5: Areas 4&5 chip enable when CFP30(D0/0x402DC) = "1" and IOC30(D0/0x402DE) = "1"
P20 #DRD	134	I/O	–	P20: I/O port when CFP20(D0/0x402D8) = "0" (default) #DRD: DRAM read signal output for successive RAS mode when CFP20(D0/0x402D8) = "1"
P21 #DWE #GAAS	133	I/O		P21: I/O port when CFP21(D1/0x402D8) = "0" and CFEX2(D2/0x402DF) = "0" (default) #DWE: DRAM write signal output for successive RAS mode when CFP21(D1/0x402D8) = "1" and CFEX2(D2/0x402DF) = "0" #GAAS: Area address strobe output for GA when CFEX2(D2/0x402DF) = "1"
P31 #BUSGET #GARD	123	I/O		P31: I/O port when CFP31(D1/0x402DC) = "0" and CFEX3(D3/0x402DF) = "0" (default) #BUSGET: Bus status monitor signal output for bus request when CFP31(D1/0x402DC) = "1" and CFEX3(D3/0x402DF) = "0" #GARD: Area read signal output for GA when CFEX3(D3/0x402DF) = "1"
EA10MD1	166	I	With pull-up	Area 10 boot mode selection EA10MD1 / EA10MD0 / Mode 1 / 1 / External ROM mode 1 / 0 / Internal ROM mode 0 / 1 / OTP mode 0 / 0 / Internal ROM emulation
EA10MD0	167	I	–	

Table 1.3.3 List of Pins for HSDMA Control Signals

Pin name	Pin No.	I/O	Pull-up	Function
K50 #DMAREQ0	74	I	With pull-up	K50: Input port when CFK50(D0/0x402C0) = "0" (default) #DMAREQ0: HSDMA Ch. 0 request input when CFK50(D0/0x402C0) = "1"
K51 #DMAREQ1	73	I	With pull-up	K51: Input port when CFK51(D1/0x402C0) = "0" (default) #DMAREQ1: HSDMA Ch. 1 request input when CFK51(D1/0x402C0) = "1"
K53 #DMAREQ2	70	I	With pull-up	K53: Input port when CFK53(D3/0x402C0) = "0" (default) #DMAREQ2: HSDMA Ch. 2 request input when CFK53(D3/0x402C0) = "1"
K54 #DMAREQ3	69	I	With pull-up	K54: Input port when CFK54(D4/0x402C0) = "0" (default) #DMAREQ3: HSDMA Ch. 3 request input when CFK54(D4/0x402C0) = "1"
P32 #DMAACK0	122	I/O	–	P32: I/O port when CFP32(D2/0x402DC) = "0" (default) #DMAACK0: HSDMA Ch. 0 acknowledge output when CFP32(D2/0x402DC) = "1"
P33 #DMAACK1	121	I/O	–	P33: I/O port when CFP33(D3/0x402DC) = "0" (default) #DMAACK1: HSDMA Ch. 1 acknowledge output when CFP33(D3/0x402DC) = "1"

Pin name	Pin No.	I/O	Pull-up	Function
P04 SIN1 #DMAACK2	147	I/O	–	P04: I/O port when CFP04(D4/0x402D0) = "0" and CFEX4(D4/0x402DF) = "0" (default) SIN1: Serial I/F Ch. 1 data input when CFP04(D4/0x402D0) = "1" and CFEX4(D4/0x402DF) = "0" #DMAACK2: HSDMA Ch. 2 acknowledge output when CFEX4(D4/0x402DF) = "1"
P06 #SCLK1 #DMAACK3	145	I/O	–	P06: I/O port when CFP06(D6/0x402D0) = "0" and CFEX6(D6/0x402DF) = "0" (default) #SCLK1: Serial I/F Ch. 1 clock input/output when CFP06(D6/0x402D0) = "1" and CFEX6(D6/0x402DF) = "0" #DMAACK3: HSDMA Ch. 3 acknowledge output when CFEX6(D6/0x402DF) = "1"
P15 EXCL4 #DMAEND0	136	I/O	–	P15: I/O port when CFP15(D5/0x402D4) = "0" (default) EXCL4: 16-bit timer 4 event counter input when CFP15(D5/0x402D4) = "1" and IOC15(D5/0x402D6) = "0" #DMAEND0: HSDMA Ch. 0 end-of-transfer signal output when CFP15(D5/0x402D4) = "1" and IOC15(D5/0x402D6) = "1"
P16 EXCL5 #DMAEND1	135	I/O	–	P16: I/O port when CFP16(D6/0x402D4) = "0" (default) EXCL5: 16-bit timer 5 event counter input when CFP16(D6/0x402D4) = "1" and IOC16(D6/0x402D6) = "0" #DMAEND1: HSDMA Ch. 1 end-of-transfer signal output when CFP16(D6/0x402D4) = "1" and IOC16(D6/0x402D6) = "1"
P05 SOUT1 #DMAEND2	146	I/O	–	P05: I/O port when CFP05(D5/0x402D0) = "0" and CFEX5(D5/0x402DF) = "0" (default) SOUT1: Serial I/F Ch. 1 data output when CFP05(D5/0x402D0) = "1" and CFEX5(D5/0x402DF) = "0" #DMAEND2: HSDMA Ch. 2 end-of-transfer signal output when CFEX5(D5/0x402DF) = "1"
P07 #SRDY1 #DMAEND3	144	I/O	–	P07: I/O port when CFP07(D7/0x402D0) = "0" and CFEX7(D7/0x402DF) = "0" (default) #SRDY1: Serial I/F Ch. 1 ready signal output when CFP07(D7/0x402D0) = "1" and CFEX5(D5/0x402DF) = "0" #DMAEND3: HSDMA Ch. 3 end-of-transfer signal output when CFEX7(D7/0x402DF) = "1"

Table 1.3.4 List of Pins for Internal Peripheral Circuits

Pin name	Pin No.	I/O	Pull-up	Function
K52 #ADTRG	71	I	With pull-up	K52: Input port when CFK52(D2/0x402C0) = "0" (default) #ADTRG: A/D converter trigger input when CFK52(D2/0x402C0) = "1"
K60 AD0	68	I	–	K60: Input port when CFK60(D0/0x402C3) = "0" (default) AD0: A/D converter Ch. 0 input when CFK60(D0/0x402C3) = "1"
K61 AD1	67	I	–	K61: Input port when CFK61(D1/0x402C3) = "0" (default) AD1: A/D converter Ch. 1 input when CFK61(D1/0x402C3) = "1"
K62 AD2	65	I	–	K62: Input port when CFK62(D2/0x402C3) = "0" (default) AD2: A/D converter Ch. 2 input when CFK62(D2/0x402C3) = "1"
K63 AD3	64	I	–	K63: Input port when CFK63(D3/0x402C3) = "0" (default) AD3: A/D converter Ch. 3 input when CFK63(D3/0x402C3) = "1"
K64 AD4	63	I	–	K64: Input port when CFK64(D4/0x402C3) = "0" (default) AD4: A/D converter Ch. 4 input when CFK64(D4/0x402C3) = "1"
K65 AD5	61	I	–	K65: Input port when CFK65(D5/0x402C3) = "0" (default) AD5: A/D converter Ch. 5 input when CFK65(D5/0x402C3) = "1"
K66 AD6	60	I	–	K66: Input port when CFK66(D6/0x402C3) = "0" (default) AD6: A/D converter Ch. 6 input when CFK60(D6/0x402C3) = "1"
K67 AD7	59	I	–	K67: Input port when CFK67(D7/0x402C3) = "0" (default) AD7: A/D converter Ch. 7 input when CFK67(D7/0x402C3) = "1"
P00 SIN0	155	I/O	–	P00: I/O port when CFP00(D0/0x402D0) = "0" (default) SIN0: Serial I/F Ch. 0 data input when CFP00(D0/0x402D0) = "1"
P01 SOUT0	154	I/O	–	P01: I/O port when CFP01(D1/0x402D0) = "0" (default) SOUT0: Serial I/F Ch. 0 data output when CFP01(D1/0x402D0) = "1"
P02 #SCLK0	153	I/O	–	P02: I/O port when CFP02(D2/0x402D0) = "0" (default) #SCLK0: Serial I/F Ch. 0 clock input/output when CFP02(D2/0x402D0) = "1"
P03 #SRDY0	152	I/O	–	P03: I/O port when CFP03(D3/0x402D0) = "0" (default) #SRDY0: Serial I/F Ch. 0 ready signal output when CFP03(D3/0x402D0) = "1"

Pin name	Pin No.	I/O	Pull-up	Function
P04 SIN1 #DMAACK2	147	I/O	–	P04: I/O port when CFP04(D4/0x402D0) = "0" and CFEX4(D4/0x402DF) = "0" (default) SIN1: Serial I/F Ch. 1 data input when CFP04(D4/0x402D0) = "1" and CFEX4(D4/0x402DF) = "0" #DMAACK2: HSDMA Ch. 2 acknowledge output when CFEX4(D4/0x402DF) = "1"
P05 SOUT1 #DMAEND2	146	I/O	–	P05: I/O port when CFP05(D5/0x402D0) = "0" and CFEX5(D5/0x402DF) = "0" (default) SOUT1: Serial I/F Ch. 1 data output when CFP05(D5/0x402D0) = "1" and CFEX5(D5/0x402DF) = "0" #DMAEND2: HSDMA Ch. 2 end-of-transfer signal output when CFEX5(D5/0x402DF) = "1"
P06 #SCLK1 #DMAACK3	145	I/O	–	P06: I/O port when CFP06(D6/0x402D0) = "0" and CFEX6(D6/0x402DF) = "0" (default) #SCLK1: Serial I/F Ch. 1 clock input/output when CFP06(D6/0x402D0) = "1" and CFEX6(D6/0x402DF) = "0" #DMAACK3: HSDMA Ch. 3 acknowledge output when CFEX6(D6/0x402DF) = "1"
P07 #SRDY1 #DMAEND3	144	I/O	–	P07: I/O port when CFP07(D7/0x402D0) = "0" and CFEX7(D7/0x402DF) = "0" (default) #SRDY1: Serial I/F Ch. 1 ready signal output when CFP07(D7/0x402D0) = "1" and CFEX5(D5/0x402DF) = "0" #DMAEND3: HSDMA Ch. 3 end-of-transfer signal output when CFEX7(D7/0x402DF) = "1"
P10 EXCL0 T8UF0 DST0	142	I/O	–	P10: I/O port when CFP10(D0/0x402D4) = "0" and CFEX1(D1/0x402DF) = "0" EXCL0: 16-bit timer 0 event counter input when CFP10(D0/0x402D4) = "1", IOC10(D0/0x402D6) = "0" and CFEX1(D1/0x402DF) = "0" T8UF0: 8-bit timer 0 output when CFP10(D0/0x402D4) = "1", IOC10(D0/0x402D6) = "1" and CFEX1(D1/0x402DF) = "0" DST0: DST0 signal output when CFEX1(D1/0x402DF) = "1" (default)
P11 EXCL1 T8UF1 DST1	141	I/O	–	P11: I/O port when CFP11(D1/0x402D4) = "0" and CFEX1(D1/0x402DF) = "0" EXCL1: 16-bit timer 1 event counter input when CFP11(D1/0x402D4) = "1", IOC11(D1/0x402D6) = "0" and CFEX1(D1/0x402DF) = "0" T8UF1: 8-bit timer 1 output when CFP11(D1/0x402D4) = "1", IOC11(D1/0x402D6) = "1" and CFEX1(D1/0x402DF) = "0" DST1: DST1 signal output when CFEX1(D1/0x402DF) = "1" (default)
P12 EXCL2 T8UF2 DST2	140	I/O	–	P12: I/O port when CFP12(D2/0x402D4) = "0" and CFEX0(D0/0x402DF) = "0" EXCL2: 16-bit timer 2 event counter input when CFP12(D2/0x402D4) = "1", IOC12(D2/0x402D6) = "0" and CFEX0(D0/0x402DF) = "0" T8UF2: 8-bit timer 2 output when CFP12(D2/0x402D4) = "1", IOC12(D2/0x402D6) = "1" and CFEX0(D0/0x402DF) = "0" DST2: DST2 signal output when CFEX0(D0/0x402DF) = "1" (default)
P13 EXCL3 T8UF3 DPCO	139	I/O	–	P13: I/O port when CFP13(D3/0x402D4) = "0" and CFEX1(D1/0x402DF) = "0" EXCL3: 16-bit timer 3 event counter input when CFP13(D3/0x402D4) = "1", IOC13(D3/0x402D6) = "0" and CFEX1(D1/0x402DF) = "0" T8UF3: 8-bit timer 3 output when CFP13(D3/0x402D4) = "1", IOC13(D3/0x402D6) = "1" and CFEX1(D1/0x402DF) = "0" DPCO: DPCO signal output when CFEX1(D1/0x402DF) = "1" (default)
P14 FOSC1 DCLK	138	I/O	–	P14: I/O port when CFP14(D4/0x402D4) = "0" and CFEX0(D0/0x402DF) = "0" FOSC1: OSC1 clock output when CFP14(D4/0x402D4) = "1" and CFEX0(D0/0x402DF) = "0" DCLK: DCLK signal output when CFEX0(D0/0x402DF) = "1" (default)
P15 EXCL4 #DMAEND0	136	I/O	–	P15: I/O port when CFP15(D5/0x402D4) = "0" (default) EXCL4: 16-bit timer 4 event counter input when CFP15(D5/0x402D4) = "1" and IOC15(D5/0x402D6) = "0" #DMAEND0: HSDMA Ch. 0 end-of-transfer signal output when CFP15(D5/0x402D4) = "1" and IOC15(D5/0x402D6) = "1"
P16 EXCL5 #DMAEND1	135	I/O	–	P16: I/O port when CFP16(D6/0x402D4) = "0" (default) EXCL5: 16-bit timer 5 event counter input when CFP16(D6/0x402D4) = "1" and IOC16(D6/0x402D6) = "0" #DMAEND1: HSDMA Ch. 1 end-of-transfer signal output when CFP16(D6/0x402D4) = "1" and IOC16(D6/0x402D6) = "1"
P22 TM0	132	I/O	–	P22: I/O port when CFP22(D2/0x402D8) = "0" (default) TM0: 16-bit timer 0 output when CFP22(D2/0x402D8) = "1"
P23 TM1	130	I/O	–	P23: I/O port when CFP23(D3/0x402D8) = "0" (default) TM1: 16-bit timer 1 output when CFP23(D3/0x402D8) = "1"

Pin name	Pin No.	I/O	Pull-up	Function
P24 TM2	129	I/O	–	P24: I/O port when CFP24(D4/0x402D8) = "0" (default) TM2: 16-bit timer 2 output when CFP24(D4/0x402D8) = "1"
P25 TM3	128	I/O	–	P25: I/O port when CFP25(D5/0x402D8) = "0" (default) TM3: 16-bit timer 3 output when CFP25(D5/0x402D8) = "1"
P26 TM4	127	I/O	–	P26: I/O port when CFP26(D6/0x402D8) = "0" (default) TM4: 16-bit timer 4 output when CFP26(D6/0x402D8) = "1"
P27 TM5	126	I/O	–	P27: I/O port when CFP27(D7/0x402D8) = "0" (default) TM5: 16-bit timer 5 output when CFP27(D7/0x402D8) = "1"

Table 1.3.5 List of Pins for LCD Controller (SED1375)

Pin name	Pin No.	I/O	Pull-up	Function
FPDAT11 GPIO4 INVERSE	92	I/O	–	FPDAT11: Panel data bit 11 for TFT/MD-TFD panels GPIO4: General-purpose I/O pin (default) INVERSE: Inverse video select pin
FPDAT10 GPIO3	93	I/O	–	FPDAT10: Panel data bit 10 for TFT/MD-TFD panels GPIO3: General-purpose I/O pin (default)
FPDAT9 GPIO2	94	I/O	–	FPDAT9: Panel data bit 9 for TFT/MD-TFD panels GPIO2: General-purpose I/O pin (default)
FPDAT8 GPIO1	96	I/O	–	FPDAT8: Panel data bit 8 for TFT/MD-TFD panels GPIO1: General-purpose I/O pin (default)
FPDAT[7:0]	98–100, 102–105, 107	O	–	Panel data bits [7:0]
FPFRAME	109	O	–	Frame pulse
FPLINE	108	O	–	Line pulse
FPSHIFT	97	O	–	Shift clock
LCDPWR	112	O	–	Active high LCD power control
DRDY MOD FPSHIFT2	110	O	–	DRDY: TFT/MD-TFD display enable MOD: LCD backplane bias (default) FPSHIFT2: Second shift clock for color passive panel (8-bit single format 1)
CLKI	161	I	–	External clock input
CKSEL[2:0]	157–159	I	–	Clock source selection CKSEL2 CKSEL1 CKSEL0 Clock source 1 1 1 reserved 1 1 0 1375 disable mode 1 0 1 External input clock from the CLKI pin 1 0 0 OSC3 oscillation clock x 1/4 0 1 1 OSC3 oscillation clock x 1/3 0 1 0 OSC3 oscillation clock x 1/2 0 0 1 OSC3 oscillation clock 0 0 0 PLL output clock
CNF3	156	I	–	Access method (endian) selection 1: Big endian, 0: Little endian
GPIO0	91	I/O	–	General-purpose I/O pin

∗1 The SED1375 CNF[2:0] pins are not available in the E0C332L01 and have been replaced with the CKSEL[2:0] pins. Refer to "SED1375 Hardware Functional Specification" for details of the LCD interface pins.

∗2 Note that some pins in Table 1.3.5 use different I/O interface level (power source) from other LCD controller pins.
CLKI, CKSEL[2:0], CNF3 pins (signals): V_{DDE1} (power voltage for I/O interface)
Other pins (signals): V_{DDE2} (power voltage for LCD interface)

Table 1.3.6 List of Pins for Clock Generator

Pin name	Pin No.	I/O	Pull-up	Function
OSC1	150	I	–	Low-speed (OSC1) oscillation input (32 kHz crystal oscillator or external clock input)
OSC2	149	O	–	Low-speed (OSC1) oscillation output
OSC3	165	I	–	High-speed (OSC3) oscillation input (crystal/ceramic oscillator or external clock input)
OSC4	164	O	–	High-speed (OSC3) oscillation output
PLLS[1:0]	170,171	I	–	PLL set-up pins PLLS1 / PLLS0 / fin (f_{OSC3}) / fout (f_{PSCIN}) 1 / 1 / 10–30MHz / 20–60MHz ∗1 10–25MHz / 20–50MHz ∗2 0 / 1 / 10–15MHz / 40–60MHz ∗1 10–12.5MHz / 40–50MHz ∗2 0 / 0 / PLL is not used / L ∗1: ROM-less model with 3.3 V ± 0.3 V operating voltage ∗2: ROM built-in model, or 3.0 V ± 0.3 V operating voltage
PLLC	174	I/O	–	Capasitor connecting pin for PLL

Table 1.3.7 List of Other Pins

Pin name	Pin No.	I/O	Pull-up/down	Function
ICEMD	162	I	With pull-down	High-impedance control input pin When this pin is set to High, all the output pins go into high-impedance state. This makes it possible to disable the E0C33 chip on the board.
DSIO	176	I/O	With pull-up	Serial I/O pin for debugging This pin is used to communicate with the debugging tool ICD33.
#X2SPD	168	I	–	Clock doubling mode set-up pin 1: CPU clock = bus clock x 1, 0: CPU clock = bus clock x 2
#NMI	172	I	With pull-up	NMI request input pin
#RESET	175	I	With pull-up	Initial reset input pin

Note: "#" in the pin names indicates that the signal is low active.

2 Power Supply

This chapter explains the operating voltage of the E0C332L01.

2.1 Power Supply Pins

The E0C332L01 has the power supply pins shown in Table 2.1.1.

Table 2.1.1 Power Supply Pins

Pin name	Pin No.	Function
V_{DD}	17,41,72,101,125,148,169	Power supply (+) for the internal logic
V_{SS}	11,23,35,48,58,66,78,90,106, 118,131,143,151,163,173	Power supply (-); GND
V_{DDE1}	5,29,54,84,137,160	Power supply (+) for the I/O block
V_{DDE2}	95,111	Power supply (+) for the LCD interface
AV_{DDE}	62	Analog system power supply (+); AV_{DDE} = V_{DDE}

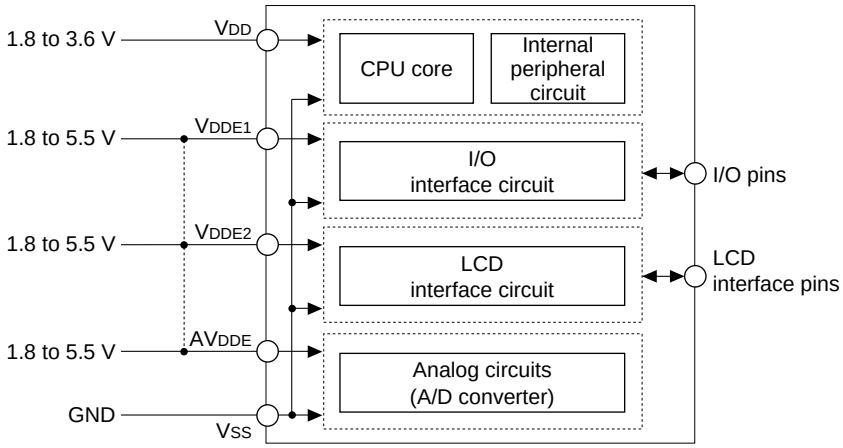


Figure 2.1.1 Power Supply System

2.2 Operating Voltage (V_{DD}, V_{SS})

The core CPU and internal peripheral circuits operate with a voltage supplied between the V_{DD} and V_{SS} pins. The following operating voltage can be used:

V_{DD} = 1.8 V to 3.6 V (V_{SS} = GND)

Note: The E0C332L01 has 7 V_{DD} pins and 15 V_{SS} pins. Be sure to supply the operating voltage to all the pins. Do not open any of them.

The operating clock frequency range (OSC3) is 5 MHz to 50 MHz with this voltage.

2.3 Power Supply for I/O Interface (V_{DDE1})

The V_{DDE1} voltage is used for interfacing with external I/O signals. For the I/O interface of the E0C332L01, the V_{DDE1} voltage is used as high level and the V_{SS} voltage as low level.
Normally, supply the same voltage level as V_{DD}. It can be supplied separately from V_{DD} for 5 V interface. The V_{SS} pin is used for the ground common with V_{DD} and V_{DDE2}.
The following voltage is enabled for V_{DDE1}:

V_{DDE1} = 1.8 V to 5.5 V (V_{SS} = GND)

Notes:
- The E0C332L01 has 6 V_{DDE1} pins. Be sure to supply a voltage to all the pins. Do not open any of them.
- When V_{DDE1} = 5 V, the data bus inputs CMOS-interface-level signals, not TTL level.
- When an external clock is input to the OSC1 or OSC3 pin, the clock signal level must be V_{DD}.
- The interface voltage level of the DSIO, P10, P11, P12, P13 and P14 pins is V_{DD}.

2.4 Power Supply for LCD Interface (V_{DDE2})

The V_{DDE2} voltage is used for interfacing with LCD control signals. It can be supplied separately from V_{DD} and V_{DDE1}. The V_{SS} pin is used for the ground common with V_{DD} and V_{DDE1}.
The LCD controller pins/signals (pin No. 91 to 112) shown in Table 1.3.5, "List of Pins for LCD Controller (SED1375)", except for the CLKI, CKSEL[2:0] and CNF3 pins use the V_{DDE2} voltage as their I/O interface level.
Note that the CLKI, CKSEL[2:0] and CNF3 pins use V_{DDE1} (power voltage for I/O interface).
The following voltage is enabled for V_{DDE2}:

V_{DDE2} = 1.8 V to 5.5 V (V_{SS} = GND)

Note: The E0C332L01 has 2 V_{DDE2} pins. Be sure to supply a voltage to all the pins. Do not open any of them.

2.5 Power Supply for Analog Circuits (AV_{DDE})

The analog power supply pin (AV_{DDE}) is provided separately from the V_{DD} and $V_{DDE1/2}$ pins in order that the digital circuits do not affect the analog circuit (A/D converter). The AV_{DDE} pin is used to supply an analog power voltage and the V_{SS} pin is used as the analog ground.
Supply the same voltage level as the V_{DDE1} to the AV_{DDE} pin.

AV_{DDE} = V_{DDE1}, V_{SS} = GND

Note: Be sure to supply V_{DDE1} to the AV_{DDE} pin even if the analog circuit is not used.

Noise on the analog power lines decrease the A/D converting precision, so use a stabilized power supply and make the board pattern with consideration given to that.

3 Internal Memory

This chapter explains the internal memory configuration.

Figure 3.1 shows the E0C332L01 memory map.

Area	Address	
Areas 18–11	0xFFFFFFF 0x1000000	External Memory
Area 10	0x0FFFFFF 0x0C20000	External Memory
	0x0C1FFFF **0x0C00000**	Internal ROM (128KB)
Areas 9–7	0x0BFFFFF 0x0400000	External Memory
Area 6	0x03FFFFF 0x03A0000	(Mirror of VRAM and LCD control registers)
	0x039FFFF **0x039FFE0**	LCD control registers
	0x039FFDF 0x038A000	(Reserved)
	0x0389FFF **0x0380000**	VRAM (40KB)
	0x037FFFF 0X0300000	(Reserved)
Areas 5–4	0x02FFFFF 0x0100000	External Memory
Area 3	0x00FFFFF 0x0080000	(Reserved) For middleware use
Area 2	0x007FFFF 0x0060000	(Reserved) For CPU, debug mode
Area 1	0x005FFFF 0x0050000	(Mirror of internal I/O)
	0x004FFFF **0x0040000**	Internal I/O
	0x003FFFF 0x0030000	(Mirror of internal I/O)
Area 0	0x0002FFF 0x0002000	(Mirror of internal RAM)
	0x0001FFF **0x0000000**	Internal RAM (8KB)

Figure 3.1 Memory Map

Area 2 is used in debug mode only and it cannot be accessed in user mode (normal program execution status).

Area 6 is configured as an external area at initial reset. To access the LCD control registers and VRAM in the SED1375 block, the "Area 6 internal/external access control" bit in the access control register (0x48132) must be set as "internal access" (A6IO/D9 = 1).

3.1 ROM and Boot Address

The E0C332L01 has a built-in 128KB ROM. The ROM is allocated to Area 10, address 0x0C00000 to address 0x0C1FFFF. The boot address is fixed at 0x0C00000 (beginning of the ROM) in the E0C332L01.
The built-in ROM can be used when the EA10MD[1:0] pins are set to "10" (internal ROM boot mode) and is read in 1 cycle.
For setting up Area 10, refer to the "BCU (Bus Controller Unit)" section in the "E0C33 Family ASIC Macro Manual".

3.2 RAM

The E0C332L01 has a built-in 8KB RAM. The RAM is allocated to Area 0, address 0x0000000 to address 0x0001FFF.
The internal RAM is a 32-bit sized device and data can be read/written in 1 cycle regardless of data size (byte, half-word or word).

3.3 VRAM

The E0C332L01 has a built-in 40KB VRAM. The VRAM is allocated to Area 6, address 0x0380000 to address 0x0389FFF and is accessed via the built-in LCD controller (SED1375).
When the LCD controller is disabled by setting the CKSEL[2:0] pins to "110", the VRAM is disconnected from the LCD controller but remains connected to the E0C332L01 bus. This allows use of the VRAM as a general-purpose RAM (device size: 16 bits).
When using the VRAM as a general-purpose RAM, set the number of wait cycles for accessing as follows:
(1) When the core voltage is 3.3 V ± 0.3 V and the bus clock frequency is lower than 20 MHz: No wait
(2) When the core voltage is 3.3 V ± 0.3 V and the bus clock frequency is 20 MHz or higher: 1 wait
(3) When the core voltage is 3.0 V ± 0.3 V: 1 wait (bus clock frequency: 33 MHz max.)
(4) When the core voltage is 2.0 V ± 0.2 V: 1 wait (bus clock frequency: 20 MHz max.)

The number of wait cycles can be set using the "Area 6 wait control" bit (A6WT[2:0]/D[A:8]) in Areas 6–4 setup register (0x4812A).

4 Peripheral Circuits

This chapter lists the built-in peripheral circuits and the I/O memory map. For details of the circuits, refer to the "E0C33 Family ASIC Macro Manual" and the "SED1375 Hardware Functional Specification".

4.1 List of Peripheral Circuits

The E0C332L01 consists of the C33 ASIC Macro Blocks: C33 Core Block, C33 Peripheral Block, C33 DMA Block and C33 Analog Block. It also contains the SED1375 LCD Controller Block.

C33 Core Block

CPU	E0C33000 32-bit RISC type CPU
BCU (Bus Control Unit)	24-bit external address bus and 16-bit data bus All the BCU functions can be used.
ITC (Interrupt Controller)	39 types of interrupts are available.
CLG (Clock Generator)	OSC3 oscillation circuit (33 MHz Max.), PLL and OSC1 oscillation circuit (32.768 kHz Typ.) built-in
DBG (Debug Unit)	Functional block for debugging with the ICD33 (In-Circuit Debugger for E0C33 Family)

C33 Peripheral Block

Prescaler	Programmable clock generator for peripheral circuits
8-bit programmable timer	4 channels with clock output function
16-bit programmable timer	6 channels with event counter, clock output and watchdog timer functions
Serial interface	2 channels (asynchronous mode, clock synchronous mode and IrDA are selectable.)
Input and I/O ports	13 bits of input ports and 29 bits of I/O ports (used for peripheral I/O)
Clock timer	1 channel with alarm function

C33 DMA Block

HSDMA (High-Speed DMA)	4 channels
IDMA (Intelligent DMA)	128 channels

C33 Analog Block

A/D converter	10-bit A/D converter with 8 input channels

SED1375 Block

LCD controller	40KB VRAM built-in 4 or 8-bit monochrome/color LCD interface Active matrix TFT/D-TFD interface 2, 4 or 16-level (1, 2 or 4 bit-per-pixel) gray-scale display 2, 4, 16 or 256-level (1, 2, 4 or 8 bit-per-pixel) color display Resolution examples: 640 × 480 dots with 1bpp color dipth 640 × 240 dots with 2bpp color dipth 320 × 240 dots with 4bpp color dipth 320 × 160 dots with 8bpp color dipth

4.2 I/O Memory Map

Table 4.2.1 I/O Memory Map

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
8-bit timer clock select register	0040146 (B)	D7–4	–	reserved	–	–	–	0 when being read.
		D3	P8TPCK3	8-bit timer 3 clock selection	1 θ/1 0 Divided clk.	0	R/W	θ: selected by Prescaler clock select register (0x40181)
		D2	P8TPCK2	8-bit timer 2 clock selection	1 θ/1 0 Divided clk.	0	R/W	
		D1	P8TPCK1	8-bit timer 1 clock selection	1 θ/1 0 Divided clk.	0	R/W	
		D0	P8TPCK0	8-bit timer 0 clock selection	1 θ/1 0 Divided clk.	0	R/W	
16-bit timer 0 clock control register	0040147 (B)	D7–4	–	reserved	–	–	–	0 when being read.
		D3	P16TON0	16-bit timer 0 clock control	1 On 0 Off	0	R/W	
		D2	P16TS02	16-bit timer 0 clock division ratio selection	P16TS0[2:0] Division ratio	0	R/W	θ: selected by Prescaler clock select register (0x40181) 16-bit timer 0 can be used as a watchdog timer.
		D1	P16TS01		1 1 1 θ/4096	0		
		D0	P16TS00		1 1 0 θ/1024	0		
					1 0 1 θ/256			
					1 0 0 θ/64			
					0 1 1 θ/16			
					0 1 0 θ/4			
					0 0 1 θ/2			
					0 0 0 θ/1			
16-bit timer 1 clock control register	0040148 (B)	D7–4	–	reserved	–	–	–	0 when being read.
		D3	P16TON1	16-bit timer 1 clock control	1 On 0 Off	0	R/W	
		D2	P16TS12	16-bit timer 1 clock division ratio selection	P16TS1[2:0] Division ratio	0	R/W	θ: selected by Prescaler clock select register (0x40181)
		D1	P16TS11		1 1 1 θ/4096	0		
		D0	P16TS10		1 1 0 θ/1024	0		
					1 0 1 θ/256			
					1 0 0 θ/64			
					0 1 1 θ/16			
					0 1 0 θ/4			
					0 0 1 θ/2			
					0 0 0 θ/1			
16-bit timer 2 clock control register	0040149 (B)	D7–4	–	reserved	–	–	–	0 when being read.
		D3	P16TON2	16-bit timer 2 clock control	1 On 0 Off	0	R/W	
		D2	P16TS22	16-bit timer 2 clock division ratio selection	P16TS2[2:0] Division ratio	0	R/W	θ: selected by Prescaler clock select register (0x40181)
		D1	P16TS21		1 1 1 θ/4096	0		
		D0	P16TS20		1 1 0 θ/1024	0		
					1 0 1 θ/256			
					1 0 0 θ/64			
					0 1 1 θ/16			
					0 1 0 θ/4			
					0 0 1 θ/2			
					0 0 0 θ/1			
16-bit timer 3 clock control register	004014A (B)	D7–4	–	reserved	–	–	–	0 when being read.
		D3	P16TON3	16-bit timer 3 clock control	1 On 0 Off	0	R/W	
		D2	P16TS32	16-bit timer 3 clock division ratio selection	P16TS3[2:0] Division ratio	0	R/W	θ: selected by Prescaler clock select register (0x40181)
		D1	P16TS31		1 1 1 θ/4096	0		
		D0	P16TS30		1 1 0 θ/1024	0		
					1 0 1 θ/256			
					1 0 0 θ/64			
					0 1 1 θ/16			
					0 1 0 θ/4			
					0 0 1 θ/2			
					0 0 0 θ/1			
16-bit timer 4 clock control register	004014B (B)	D7–4	–	reserved	–	–	–	0 when being read.
		D3	P16TON4	16-bit timer 4 clock control	1 On 0 Off	0	R/W	
		D2	P16TS42	16-bit timer 4 clock division ratio selection	P16TS4[2:0] Division ratio	0	R/W	θ: selected by Prescaler clock select register (0x40181)
		D1	P16TS41		1 1 1 θ/4096	0		
		D0	P16TS40		1 1 0 θ/1024	0		
					1 0 1 θ/256			
					1 0 0 θ/64			
					0 1 1 θ/16			
					0 1 0 θ/4			
					0 0 1 θ/2			
					0 0 0 θ/1			

(B) in [Address] indicates an 8-bit register and (HW) indicates a 16-bit register.

The meaning of the symbols described in [Init.] are listed below:

0, 1: Initial values that are set at initial reset.
(However, the registers for the bus and input/output ports are not initialized at hot start.)

X: Not initialized at initial reset.

–: Not set in the circuit.

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
16-bit timer 5 clock control register	**004014C (B)**	D7–4	**–**	reserved	–	–	–	0 when being read.
		D3	**P16TON5**	16-bit timer 5 clock control	1 On / 0 Off	0	R/W	
		D2	**P16TS52**	16-bit timer 5 clock division ratio selection	P16TS5[2:0] / Division ratio: 1 1 1 θ/4096 1 1 0 θ/1024 1 0 1 θ/256 1 0 0 θ/64 0 1 1 θ/16 0 1 0 θ/4 0 0 1 θ/2 0 0 0 θ/1	0	R/W	θ: selected by Prescaler clock select register (0x40181)
		D1	**P16TS51**			0		
		D0	**P16TS50**			0		
8-bit timer 0/1 clock control register	**004014D (B)**	D7	**P8TON1**	8-bit timer 1 clock control	1 On / 0 Off	0	R/W	
		D6	**P8TS12**	8-bit timer 1 clock division ratio selection	P8TS1[2:0] / Division ratio: 1 1 1 θ/4096 1 1 0 θ/2048 1 0 1 θ/1024 1 0 0 θ/512 0 1 1 θ/256 0 1 0 θ/128 0 0 1 θ/64 0 0 0 θ/32	0	R/W	θ: selected by Prescaler clock select register (0x40181) 8-bit timer 1 can generate the OSC3 oscillation-stabilize waiting period.
		D5	**P8TS11**			0		
		D4	**P8TS10**			0		
		D3	**P8TON0**	8-bit timer 0 clock control	1 On / 0 Off	0	R/W	
		D2	**P8TS02**	8-bit timer 0 clock division ratio selection	P8TS0[2:0] / Division ratio: 1 1 1 θ/256 1 1 0 θ/128 1 0 1 θ/64 1 0 0 θ/32 0 1 1 θ/16 0 1 0 θ/8 0 0 1 θ/4 0 0 0 θ/2	0	R/W	θ: selected by Prescaler clock select register (0x40181) 8-bit timer 0 can generate the DRAM refresh clock.
		D1	**P8TS01**			0		
		D0	**P8TS00**			0		
8-bit timer 2/3 clock control register	**004014E (B)**	D7	**P8TON3**	8-bit timer 3 clock control	1 On / 0 Off	0	R/W	
		D6	**P8TS32**	8-bit timer 3 clock division ratio selection	P8TS3[2:0] / Division ratio: 1 1 1 θ/256 1 1 0 θ/128 1 0 1 θ/64 1 0 0 θ/32 0 1 1 θ/16 0 1 0 θ/8 0 0 1 θ/4 0 0 0 θ/2	0	R/W	θ: selected by Prescaler clock select register (0x40181) 8-bit timer 3 can generate the clock for the serial I/F Ch.1.
		D5	**P8TS31**			0		
		D4	**P8TS30**			0		
		D3	**P8TON2**	8-bit timer 2 clock control	1 On / 0 Off	0	R/W	
		D2	**P8TS22**	8-bit timer 2 clock division ratio selection	P8TS2[2:0] / Division ratio: 1 1 1 θ/4096 1 1 0 θ/2048 1 0 1 θ/64 1 0 0 θ/32 0 1 1 θ/16 0 1 0 θ/8 0 0 1 θ/4 0 0 0 θ/2	0	R/W	θ: selected by Prescaler clock select register (0x40181) 8-bit timer 2 can generate the clock for the serial I/F Ch.0.
		D1	**P8TS21**			0		
		D0	**P8TS20**			0		
A/D clock control register	**004014F (B)**	D7–4	**–**	reserved	–	–	–	0 when being read.
		D3	**PSONAD**	A/D converter clock control	1 On / 0 Off	0	R/W	
		D2	**PSAD2**	A/D converter clock division ratio selection	P8TS0[2:0] / Division ratio: 1 1 1 θ/256 1 1 0 θ/128 1 0 1 θ/64 1 0 0 θ/32 0 1 1 θ/16 0 1 0 θ/8 0 0 1 θ/4 0 0 0 θ/2	0	R/W	θ: selected by Prescaler clock select register (0x40181)
		D1	**PSAD1**			0		
		D0	**PSAD0**			0		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Clock timer Run/Stop register	0040151 (B)	D7–2	–	reserved	–	–	–	0 when being read.
		D1	TCRST	Clock timer reset	1 Reset / 0 Invalid	X	W	0 when being read.
		D0	TCRUN	Clock timer Run/Stop control	1 Run / 0 Stop	X	R/W	
Clock timer interrupt control register	0040152 (B)	D7	TCISE2	Clock timer interrupt factor selection	TCISE[2:0] → Interrupt factor: 111 None; 110 Day; 101 Hour; 100 Minute; 011 1 Hz; 010 2 Hz; 001 8 Hz; 000 32 Hz	X	R/W	
		D6	TCISE1			X		
		D5	TCISE0			X		
		D4	TCASE2	Clock timer alarm factor selection	TCASE[2:0] → Alarm factor: 1XX Day; X1X Hour; XX1 Minute; 000 None	X	R/W	
		D3	TCASE1			X		
		D2	TCASE0			X		
		D1	TCIF	Interrupt factor generation flag	1 Generated / 0 Not generated	X	R/W	Reset by writing 1.
		D0	TCAF	Alarm factor generation flag	1 Generated / 0 Not generated	X	R/W	Reset by writing 1.
Clock timer divider register	0040153 (B)	D7	TCD7	Clock timer data 1 Hz	1 High / 0 Low	X	R	
		D6	TCD6	Clock timer data 2 Hz	1 High / 0 Low	X	R	
		D5	TCD5	Clock timer data 4 Hz	1 High / 0 Low	X	R	
		D4	TCD4	Clock timer data 8 Hz	1 High / 0 Low	X	R	
		D3	TCD3	Clock timer data 16 Hz	1 High / 0 Low	X	R	
		D2	TCD2	Clock timer data 32 Hz	1 High / 0 Low	X	R	
		D1	TCD1	Clock timer data 64 Hz	1 High / 0 Low	X	R	
		D0	TCD0	Clock timer data 128 Hz	1 High / 0 Low	X	R	
Clock timer second register	0040154 (B)	D7–6	–	reserved	–	–	–	0 when being read.
		D5	TCMD5	Clock timer second counter data	0 to 59 seconds	X	R	
		D4	TCMD4	TCMD5 = MSB		X		
		D3	TCMD3	TCMD0 = LSB		X		
		D2	TCMD2			X		
		D1	TCMD1			X		
		D0	TCMD0			X		
Clock timer minute register	0040155 (B)	D7–6	–	reserved	–	–	–	0 when being read.
		D5	TCHD5	Clock timer minute counter data	0 to 59 minutes	X	R/W	
		D4	TCHD4	TCHD5 = MSB		X		
		D3	TCHD3	TCHD0 = LSB		X		
		D2	TCHD2			X		
		D1	TCHD1			X		
		D0	TCHD0			X		
Clock timer hour register	0040156 (B)	D7–5	–	reserved	–	–	–	0 when being read.
		D4	TCDD4	Clock timer hour counter data	0 to 23 hours	X	R/W	
		D3	TCDD3	TCDD4 = MSB		X		
		D2	TCDD2	TCDD0 = LSB		X		
		D1	TCDD1			X		
		D0	TCDD0			X		
Clock timer day (low-order) register	0040157 (B)	D7	TCND7	Clock timer day counter data (low-order 8 bits)	0 to 65535 days (low-order 8 bits)	X	R/W	
		D6	TCND6			X		
		D5	TCND5	TCND0 = LSB		X		
		D4	TCND4			X		
		D3	TCND3			X		
		D2	TCND2			X		
		D1	TCND1			X		
		D0	TCND0			X		
Clock timer day (high-order) register	0040158 (B)	D7	TCND15	Clock timer day counter data (high-order 8 bits)	0 to 65535 days (high-order 8 bits)	X	R/W	
		D6	TCND14			X		
		D5	TCND13	TCND15 = MSB		X		
		D4	TCND12			X		
		D3	TCND11			X		
		D2	TCND10			X		
		D1	TCND9			X		
		D0	TCND8			X		
Clock timer minute comparison register	0040159 (B)	D7–6	–	reserved	–	–	–	0 when being read.
		D5	TCCH5	Clock timer minute comparison data	0 to 59 minutes (Note) Can be set within 0–63.	X	R/W	
		D4	TCCH4			X		
		D3	TCCH3	TCCH5 = MSB		X		
		D2	TCCH2	TCCH0 = LSB		X		
		D1	TCCH1			X		
		D0	TCCH0			X		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Clock timer	**004015A**	D7–5	**–**	reserved	–	–	–	0 when being read.
hour	**(B)**	D4	**TCCD4**	Clock timer hour comparison data	0 to 23 hours	X	R/W	
comparison		D3	**TCCD3**	TCCD4 = MSB	(Note) Can be set within 0–31.	X		
register		D2	**TCCD2**	TCCD0 = LSB		X		
		D1	**TCCD1**			X		
		D0	**TCCD0**			X		
Clock timer	**004015B**	D7–5	**–**	reserved	–	–	–	0 when being read.
day	**(B)**	D4	**TCCN4**	Clock timer day comparison data	0 to 31 days	X	R/W	Compared with
comparison		D3	**TCCN3**	TCCN4 = MSB		X		TCND[4:0].
register		D2	**TCCN2**	TCCN0 = LSB		X		
		D1	**TCCN1**			X		
		D0	**TCCN0**			X		

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
8-bit timer 0	**0040160**	D7–3	**–**	reserved	–				–	–	0 when being read.
control register	**(B)**	D2	**PTOUT0**	8-bit timer 0 clock output control	1	On	0	Off	0	R/W	
		D1	**PSET0**	8-bit timer 0 preset	1	Preset	0	Invalid	–	W	0 when being read.
		D0	**PTRUN0**	8-bit timer 0 Run/Stop control	1	Run	0	Stop	0	R/W	
8-bit timer 0	**0040161**	D7	**RLD07**	8-bit timer 0 reload data	0 to 255				X	R/W	
reload data	**(B)**	D6	**RLD06**	RLD07 = MSB					X		
register		D5	**RLD05**	RLD00 = LSB					X		
		D4	**RLD04**						X		
		D3	**RLD03**						X		
		D2	**RLD02**						X		
		D1	**RLD01**						X		
		D0	**RLD00**						X		
8-bit timer 0	**0040162**	D7	**PTD07**	8-bit timer 0 counter data	0 to 255				X	R	
counter data	**(B)**	D6	**PTD06**	PTD07 = MSB					X		
register		D5	**PTD05**	PTD00 = LSB					X		
		D4	**PTD04**						X		
		D3	**PTD03**						X		
		D2	**PTD02**						X		
		D1	**PTD01**						X		
		D0	**PTD00**						X		
8-bit timer 1	**0040164**	D7–3	**–**	reserved	–				–	–	0 when being read.
control register	**(B)**	D2	**PTOUT1**	8-bit timer 1 clock output control	1	On	0	Off	0	R/W	
		D1	**PSET1**	8-bit timer 1 preset	1	Preset	0	Invalid	–	W	0 when being read.
		D0	**PTRUN1**	8-bit timer 1 Run/Stop control	1	Run	0	Stop	0	R/W	
8-bit timer 1	**0040165**	D7	**RLD17**	8-bit timer 1 reload data	0 to 255				X	R/W	
reload data	**(B)**	D6	**RLD16**	RLD17 = MSB					X		
register		D5	**RLD15**	RLD10 = LSB					X		
		D4	**RLD14**						X		
		D3	**RLD13**						X		
		D2	**RLD12**						X		
		D1	**RLD11**						X		
		D0	**RLD10**						X		
8-bit timer 1	**0040166**	D7	**PTD17**	8-bit timer 1 counter data	0 to 255				X	R	
counter data	**(B)**	D6	**PTD16**	PTD17 = MSB					X		
register		D5	**PTD15**	PTD10 = LSB					X		
		D4	**PTD14**						X		
		D3	**PTD13**						X		
		D2	**PTD12**						X		
		D1	**PTD11**						X		
		D0	**PTD10**						X		
8-bit timer 2	**0040168**	D7–3	**–**	reserved	–				–	–	0 when being read.
control register	**(B)**	D2	**PTOUT2**	8-bit timer 2 clock output control	1	On	0	Off	0	R/W	
		D1	**PSET2**	8-bit timer 2 preset	1	Preset	0	Invalid	–	W	0 when being read.
		D0	**PTRUN2**	8-bit timer 2 Run/Stop control	1	Run	0	Stop	0	R/W	
8-bit timer 2	**0040169**	D7	**RLD27**	8-bit timer 2 reload data	0 to 255				X	R/W	
reload data	**(B)**	D6	**RLD26**	RLD27 = MSB					X		
register		D5	**RLD25**	RLD20 = LSB					X		
		D4	**RLD24**						X		
		D3	**RLD23**						X		
		D2	**RLD22**						X		
		D1	**RLD21**						X		
		D0	**RLD20**						X		
8-bit timer 2	**004016A**	D7	**PTD27**	8-bit timer 2 counter data	0 to 255				X	R	
counter data	**(B)**	D6	**PTD26**	PTD27 = MSB					X		
register		D5	**PTD25**	PTD20 = LSB					X		
		D4	**PTD24**						X		
		D3	**PTD23**						X		
		D2	**PTD22**						X		
		D1	**PTD21**						X		
		D0	**PTD20**						X		

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
8-bit timer 3 control register	**004016C (B)**	D7–3	**–**	reserved	–				–	–	0 when being read.
		D2	**PTOUT3**	8-bit timer 3 clock output control	1	On	0	Off	0	R/W	
		D1	**PSET3**	8-bit timer 3 preset	1	Preset	0	Invalid	–	W	0 when being read.
		D0	**PTRUN3**	8-bit timer 3 Run/Stop control	1	Run	0	Stop	0	R/W	
8-bit timer 3 reload data register	**004016D (B)**	D7	**RLD37**	8-bit timer 3 reload data	0 to 255				X	R/W	
		D6	**RLD36**	RLD37 = MSB					X		
		D5	**RLD35**	RLD30 = LSB					X		
		D4	**RLD34**						X		
		D3	**RLD33**						X		
		D2	**RLD32**						X		
		D1	**RLD31**						X		
		D0	**RLD30**						X		
8-bit timer 3 counter data register	**004016E (B)**	D7	**PTD37**	8-bit timer 3 counter data	0 to 255				X	R	
		D6	**PTD36**	PTD37 = MSB					X		
		D5	**PTD35**	PTD30 = LSB					X		
		D4	**PTD34**						X		
		D3	**PTD33**						X		
		D2	**PTD32**						X		
		D1	**PTD31**						X		
		D0	**PTD30**						X		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Watchdog timer write-protect register	**0040170 (B)**	D7	**WRWD**	EWD write protection	1 Write enabled 0 Write-protect	0	R/W	
		D6–0	**–**	–	–	–	–	0 when being read.
Watchdog timer enable register	**0040171 (B)**	D7–2	**–**	–	–	–	–	0 when being read.
		D1	**EWD**	Watchdog timer enable	1 NMI enabled 0 NMI disabled	0	R/W	
		D0	**–**	–	–	–	–	0 when being read.

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Power control register	**0040180 (B)**	D7	**CLKDT1**	System clock division ratio selection	CLKDT[1:0] = 1 1: 1/8	0	R/W	
		D6	**CLKDT0**		CLKDT[1:0] = 1 0: 1/4	0		
					CLKDT[1:0] = 0 1: 1/2			
					CLKDT[1:0] = 0 0: 1/1			
		D5	**PSCON**	Prescaler On/Off control	1: On, 0: Off	1	R/W	
		D4–3	**–**	reserved	–	0	–	Writing 1 not allowed.
		D2	**CLKCHG**	CPU operating clock switch	1: OSC3, 0: OSC1	1	R/W	
		D1	**SOSC3**	High-speed (OSC3) oscillation On/Off	1: On, 0: Off	1	R/W	
		D0	**SOSC1**	Low-speed (OSC1) oscillation On/Off	1: On, 0: Off	1	R/W	
Prescaler clock select register	**0040181 (B)**	D7–1	**–**	reserved	–	0	–	
		D0	**PSCDT0**	Prescaler clock selection	1: OSC1, 0: OSC3/PLL	0	R/W	
Clock option register	**0040190 (B)**	D7–4	**–**	–	–	–	–	0 when being read.
		D3	**HLT2OP**	HALT clock option	1: On, 0: Off	0	R/W	
		D2	**8T1ON**	OSC3-stabilize waiting function	1: Off, 0: On	1	R/W	
		D1	**–**	reserved	–	0	–	Do not write 1.
		D0	**PF1ON**	OSC1 external output control	1: On, 0: Off	0	R/W	
Power control protect register	**004019E (B)**	D7	**CLGP7**	Power control register protect flag	Writing 10010110 (0x96) removes the write protection of the power control register (0x40180). Writing another value set the write protection.	0	R/W	
		D6	**CLGP6**			0		
		D5	**CLGP5**			0		
		D4	**CLGP4**			0		
		D3	**CLGP3**			0		
		D2	**CLGP2**			0		
		D1	**CLGP1**			0		
		D0	**CLGP0**			0		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Serial I/F Ch.0 transmit data register	**00401E0 (B)**	D7	**TXD07**	Serial I/F Ch.0 transmit data	0x0 to 0xFF(0x7F)	X	R/W	7-bit asynchronous mode does not use TXD07.
		D6	**TXD06**	TXD07(06) = MSB		X		
		D5	**TXD05**	TXD00 = LSB		X		
		D4	**TXD04**			X		
		D3	**TXD03**			X		
		D2	**TXD02**			X		
		D1	**TXD01**			X		
		D0	**TXD00**			X		
Serial I/F Ch.0 receive data register	**00401E1 (B)**	D7	**RXD07**	Serial I/F Ch.0 receive data	0x0 to 0xFF(0x7F)	X	R	7-bit asynchronous mode does not use RXD07 (fixed at 0).
		D6	**RXD06**	RXD07(06) = MSB		X		
		D5	**RXD05**	RXD00 = LSB		X		
		D4	**RXD04**			X		
		D3	**RXD03**			X		
		D2	**RXD02**			X		
		D1	**RXD01**			X		
		D0	**RXD00**			X		
Serial I/F Ch.0 status register	**00401E2 (B)**	D7–6	**–**	–	–	–	–	0 when being read.
		D5	**TEND0**	Ch.0 transmit-completion flag	1 Transmitting 0 End	0	R	
		D4	**FER0**	Ch.0 flaming error flag	1 Error 0 Normal	0	R/W	Reset by writing 0.
		D3	**PER0**	Ch.0 parity error flag	1 Error 0 Normal	0	R/W	Reset by writing 0.
		D2	**OER0**	Ch.0 overrun error flag	1 Error 0 Normal	0	R/W	Reset by writing 0.
		D1	**TDBE0**	Ch.0 transmit data buffer empty	1 Empty 0 Buffer full	1	R	
		D0	**RDBF0**	Ch.0 receive data buffer full	1 Buffer full 0 Empty	0	R	
Serial I/F Ch.0 control register	**00401E3 (B)**	D7	**TXEN0**	Ch.0 transmit enable	1 Enabled 0 Disabled	0	R/W	
		D6	**RXEN0**	Ch.0 receive enable	1 Enabled 0 Disabled	0	R/W	
		D5	**EPR0**	Ch.0 parity enable	1 With parity 0 No parity	X	R/W	Valid only in asynchronous mode.
		D4	**PMD0**	Ch.0 parity mode selection	1 Odd 0 Even	X	R/W	
		D3	**STPB0**	Ch.0 stop bit selection	1 2 bits 0 1 bit	X	R/W	
		D2	**SSCK0**	Ch.0 input clock selection	1 #SCLK0 0 Internal clock	X	R/W	
		D1	**SMD01**	Ch.0 transfer mode selection	SMD0[1:0] Transfer mode	X	R/W	
		D0	**SMD00**		1 1 8-bit asynchronous	X		
					1 0 7-bit asynchronous			
					0 1 Clock sync. Slave			
					0 0 Clock sync. Master			
Serial I/F Ch.0 IrDA register	**00401E4 (B)**	D7–5	**–**	–	–	–	–	0 when being read.
		D4	**DIVMD0**	Ch.0 async. clock division ratio	1 1/8 0 1/16	X	R/W	
		D3	**IRTL0**	Ch.0 IrDA I/F output logic inversion	1 Inverted 0 Direct	X	R/W	Valid only in asynchronous mode.
		D2	**IRRL0**	Ch.0 IrDA I/F input logic inversion	1 Inverted 0 Direct	X	R/W	
		D1	**IRMD01**	Ch.0 interface mode selection	IRMD0[1:0] I/F mode	X	R/W	
		D0	**IRMD00**		1 1 reserved	X		
					1 0 IrDA 1.0			
					0 1 reserved			
					0 0 General I/F			

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Serial I/F Ch.1 transmit data register	**00401E5 (B)**	D7	**TXD17**	Serial I/F Ch.1 transmit data	0x0 to 0xFF(0x7F)	X	R/W	7-bit asynchronous mode does not use TXD17.
		D6	**TXD16**	TXD17(16) = MSB		X		
		D5	**TXD15**	TXD10 = LSB		X		
		D4	**TXD14**			X		
		D3	**TXD13**			X		
		D2	**TXD12**			X		
		D1	**TXD11**			X		
		D0	**TXD10**			X		
Serial I/F Ch.1 receive data register	**00401E6 (B)**	D7	**RXD17**	Serial I/F Ch.1 receive data	0x0 to 0xFF(0x7F)	X	R	7-bit asynchronous mode does not use RXD17 (fixed at 0).
		D6	**RXD16**	RXD17(16) = MSB		X		
		D5	**RXD15**	RXD10 = LSB		X		
		D4	**RXD14**			X		
		D3	**RXD13**			X		
		D2	**RXD12**			X		
		D1	**RXD11**			X		
		D0	**RXD10**			X		
Serial I/F Ch.1 status register	**00401E7 (B)**	D7–6	**–**	–	–	–	–	0 when being read.
		D5	**TEND1**	Ch.1 transmit-completion flag	1 Transmitting 0 End	0	R	
		D4	**FER1**	Ch.1 flaming error flag	1 Error 0 Normal	0	R/W	Reset by writing 0.
		D3	**PER1**	Ch.1 parity error flag	1 Error 0 Normal	0	R/W	Reset by writing 0.
		D2	**OER1**	Ch.1 overrun error flag	1 Error 0 Normal	0	R/W	Reset by writing 0.
		D1	**TDBE1**	Ch.1 transmit data buffer empty	1 Empty 0 Buffer full	1	R	
		D0	**RDBF1**	Ch.1 receive data buffer full	1 Buffer full 0 Empty	0	R	
Serial I/F Ch.1 control register	**00401E8 (B)**	D7	**TXEN1**	Ch.1 transmit enable	1 Enabled 0 Disabled	0	R/W	
		D6	**RXEN1**	Ch.1 receive enable	1 Enabled 0 Disabled	0	R/W	
		D5	**EPR1**	Ch.1 parity enable	1 With parity 0 No parity	X	R/W	Valid only in asynchronous mode.
		D4	**PMD1**	Ch.1 parity mode selection	1 Odd 0 Even	X	R/W	
		D3	**STPB1**	Ch.1 stop bit selection	1 2 bits 0 1 bit	X	R/W	
		D2	**SSCK1**	Ch.1 input clock selection	1 #SCLK1 0 Internal clock	X	R/W	
		D1	**SMD11**	Ch.1 transfer mode selection	SMD1[1:0] Transfer mode	X	R/W	
		D0	**SMD10**		1 1 8-bit asynchronous	X		
					1 0 7-bit asynchronous			
					0 1 Clock sync. Slave			
					0 0 Clock sync. Master			
Serial I/F Ch.1 IrDA register	**00401E9 (B)**	D7–5	**–**	–	–	–	–	0 when being read.
		D4	**DIVMD1**	Ch.1 async. clock division ratio	1 1/8 0 1/16	X	R/W	
		D3	**IRTL1**	Ch.1 IrDA I/F output logic inversion	1 Inverted 0 Direct	X	R/W	Valid only in asynchronous mode.
		D2	**IRRL1**	Ch.1 IrDA I/F input logic inversion	1 Inverted 0 Direct	X	R/W	
		D1	**IRMD11**	Ch.1 interface mode selection	IRMD1[1:0] I/F mode	X	R/W	
		D0	**IRMD10**		1 1 reserved	X		
					1 0 IrDA 1.0			
					0 1 reserved			
					0 0 General I/F			

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
A/D conversion result (low-order) register	**0040240 (B)**	D7	**ADD7**	A/D converted data (low-order 8 bits) ADD0 = LSB	0x0 to 0x3FF (low-order 8 bits)	0	R	
		D6	**ADD6**			0		
		D5	**ADD5**			0		
		D4	**ADD4**			0		
		D3	**ADD3**			0		
		D2	**ADD2**			0		
		D1	**ADD1**			0		
		D0	**ADD0**			0		
A/D conversion result (high-order) register	**0040241 (B)**	D7–2	**–**	–	–	–	–	0 when being read.
		D1	**ADD9**	A/D converted data (high-order 2 bits) ADD9 = MSB	0x0 to 0x3FF (high-order 2 bits)	0	R	
		D0	**ADD8**			0		
A/D trigger register	**0040242 (B)**	D7–6	**–**	–	–	–	–	0 when being read.
		D5	**MS**	A/D conversion mode selection	1 Continuous 0 Normal	0	R/W	
		D4	**TS1**	A/D conversion trigger selection	TS[1:0] Trigger: 1 1 #ADTRG pin; 1 0 8-bit timer 0; 0 1 16-bit timer 0; 0 0 Software	0	R/W	
		D3	**TS0**			0		
		D2	**CH2**	A/D conversion channel status	CH[2:0] Channel: 1 1 1 AD7; 1 1 0 AD6; 1 0 1 AD5; 1 0 0 AD4; 0 1 1 AD3; 0 1 0 AD2; 0 0 1 AD1; 0 0 0 AD0	0	R	
		D1	**CH1**			0		
		D0	**CH0**			0		
A/D channel register	**0040243 (B)**	D7–6	**–**	–	–	–	–	0 when being read.
		D5	**CE2**	A/D converter end channel selection	CE[2:0] End channel: 1 1 1 AD7; 1 1 0 AD6; 1 0 1 AD5; 1 0 0 AD4; 0 1 1 AD3; 0 1 0 AD2; 0 0 1 AD1; 0 0 0 AD0	0	R/W	
		D4	**CE1**			0		
		D3	**CE0**			0		
		D2	**CS2**	A/D converter start channel selection	CS[2:0] Start channel: 1 1 1 AD7; 1 1 0 AD6; 1 0 1 AD5; 1 0 0 AD4; 0 1 1 AD3; 0 1 0 AD2; 0 0 1 AD1; 0 0 0 AD0	0	R/W	
		D1	**CS1**			0		
		D0	**CS0**			0		
A/D enable register	**0040244 (B)**	D7–4	**–**	–	–	–	–	0 when being read.
		D3	**ADF**	Conversion-complete flag	1 Completed 0 Run/Standby	0	R	Reset when ADD is read.
		D2	**ADE**	A/D enable	1 Enabled 0 Disabled	0	R/W	
		D1	**ADST**	A/D conversion control/status	1 Start/Run 0 Stop	0	R/W	
		D0	**OWE**	Overwrite error flag	1 Error 0 Normal	0	R/W	Reset by writing 0.
A/D sampling register	**0040245 (B)**	D7–2	**–**	–	–	–	–	0 when being read.
		D1	**ST1**	Input signal sampling time setup	ST[1:0] Sampring time: 1 1 9 clocks; 1 0 7 clocks; 0 1 5 clocks; 0 0 3 clocks	1	R/W	Use with 9 clocks.
		D0	**ST0**			1		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Port input 0/1 interrupt priority register	**0040260 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PP1L2**	Port input 1 interrupt level	0 to 7	X	R/W	
		D5	**PP1L1**			X		
		D4	**PP1L0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PP0L2**	Port input 0 interrupt level	0 to 7	X	R/W	
		D1	**PP0L1**			X		
		D0	**PP0L0**			X		
Port input 2/3 interrupt priority register	**0040261 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PP3L2**	Port input 3 interrupt level	0 to 7	X	R/W	
		D5	**PP3L1**			X		
		D4	**PP3L0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PP2L2**	Port input 2 interrupt level	0 to 7	X	R/W	
		D1	**PP2L1**			X		
		D0	**PP2L0**			X		
Key input interrupt priority register	**0040262 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PK1L2**	Key input 1 interrupt level	0 to 7	X	R/W	
		D5	**PK1L1**			X		
		D4	**PK1L0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PK0L2**	Key input 0 interrupt level	0 to 7	X	R/W	
		D1	**PK0L1**			X		
		D0	**PK0L0**			X		
High-speed DMA Ch.0/1 interrupt priority register	**0040263 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PHSD1L2**	High-speed DMA Ch.1	0 to 7	X	R/W	
		D5	**PHSD1L1**	interrupt level		X		
		D4	**PHSD1L0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PHSD0L2**	High-speed DMA Ch.0	0 to 7	X	R/W	
		D1	**PHSD0L1**	interrupt level		X		
		D0	**PHSD0L0**			X		
High-speed DMA Ch.2/3 interrupt priority register	**0040264 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PHSD3L2**	High-speed DMA Ch.3	0 to 7	X	R/W	
		D5	**PHSD3L1**	interrupt level		X		
		D4	**PHSD3L0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PHSD2L2**	High-speed DMA Ch.2	0 to 7	X	R/W	
		D1	**PHSD2L1**	interrupt level		X		
		D0	**PHSD2L0**			X		
IDMA interrupt priority register	**0040265 (B)**	D7–3	**–**	reserved	–	–	–	0 when being read.
		D2	**PDM2**	IDMA interrupt level	0 to 7	X	R/W	
		D1	**PDM1**			X		
		D0	**PDM0**			X		
16-bit timer 0/1 interrupt priority register	**0040266 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**P16T12**	16-bit timer 1 interrupt level	0 to 7	X	R/W	
		D5	**P16T11**			X		
		D4	**P16T10**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**P16T02**	16-bit timer 0 interrupt level	0 to 7	X	R/W	
		D1	**P16T01**			X		
		D0	**P16T00**			X		
16-bit timer 2/3 interrupt priority register	**0040267 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**P16T32**	16-bit timer 3 interrupt level	0 to 7	X	R/W	
		D5	**P16T31**			X		
		D4	**P16T30**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**P16T22**	16-bit timer 2 interrupt level	0 to 7	X	R/W	
		D1	**P16T21**			X		
		D0	**P16T20**			X		
16-bit timer 4/5 interrupt priority register	**0040268 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**P16T52**	16-bit timer 5 interrupt level	0 to 7	X	R/W	
		D5	**P16T51**			X		
		D4	**P16T50**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**P16T42**	16-bit timer 4 interrupt level	0 to 7	X	R/W	
		D1	**P16T41**			X		
		D0	**P16T40**			X		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
8-bit timer, serial I/F Ch.0 interrupt priority register	**0040269 (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PSIO02**	Serial interface Ch.0	0 to 7	X	R/W	
		D5	**PSIO01**	interrupt level		X		
		D4	**PSIO00**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**P8TM2**	8-bit timer 0–3 interrupt level	0 to 7	X	R/W	
		D1	**P8TM1**			X		
		D0	**P8TM0**			X		
Serial I/F Ch.1, A/D interrupt priority register	**004026A (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PAD2**	A/D converter interrupt level	0 to 7	X	R/W	
		D5	**PAD1**			X		
		D4	**PAD0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PSIO12**	Serial interface Ch.1	0 to 7	X	R/W	
		D1	**PSIO11**	interrupt level		X		
		D0	**PSIO10**			X		
Clock timer interrupt priority register	**004026B (B)**	D7–3	**–**	reserved	–	–	–	Writing 1 not allowed.
		D2	**PCTM2**	Clock timer interrupt level	0 to 7	X	R/W	
		D1	**PCTM1**			X		
		D0	**PCTM0**			X		
Port input 4/5 interrupt priority register	**004026C (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PP5L2**	Port input 5 interrupt level	0 to 7	X	R/W	
		D5	**PP5L1**			X		
		D4	**PP5L0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PP4L2**	Port input 4 interrupt level	0 to 7	X	R/W	
		D1	**PP4L1**			X		
		D0	**PP4L0**			X		
Port input 6/7 interrupt priority register	**004026D (B)**	D7	**–**	reserved	–	–	–	0 when being read.
		D6	**PP7L2**	Port input 7 interrupt level	0 to 7	X	R/W	
		D5	**PP7L1**			X		
		D4	**PP7L0**			X		
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**PP6L2**	Port input 6 interrupt level	0 to 7	X	R/W	
		D1	**PP6L1**			X		
		D0	**PP6L0**			X		

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
Key input, port input 0–3 interrupt enable register	**0040270 (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**EK1**	Key input 1	1	Enabled	0	Disabled	0	R/W	
		D4	**EK0**	Key input 0					0	R/W	
		D3	**EP3**	Port input 3					0	R/W	
		D2	**EP2**	Port input 2					0	R/W	
		D1	**EP1**	Port input 1					0	R/W	
		D0	**EP0**	Port input 0					0	R/W	
DMA interrupt enable register	**0040271 (B)**	D7–5	**–**	reserved	–				–	–	0 when being read.
		D4	**EIDMA**	IDMA	1	Enabled	0	Disabled	0	R/W	
		D3	**EHDM3**	High-speed DMA Ch.3					0	R/W	
		D2	**EHDM2**	High-speed DMA Ch.2					0	R/W	
		D1	**EHDM1**	High-speed DMA Ch.1					0	R/W	
		D0	**EHDM0**	High-speed DMA Ch.0					0	R/W	
16-bit timer 0/1 interrupt enable register	**0040272 (B)**	D7	**E16TC1**	16-bit timer 1 comparison A	1	Enabled	0	Disabled	0	R/W	
		D6	**E16TU1**	16-bit timer 1 comparison B					0	R/W	
		D5–4	**–**	reserved	–				–	–	0 when being read.
		D3	**E16TC0**	16-bit timer 0 comparison A	1	Enabled	0	Disabled	0	R/W	
		D2	**E16TU0**	16-bit timer 0 comparison B					0	R/W	
		D1–0	**–**	reserved	–				–	–	0 when being read.
16-bit timer 2/3 interrupt enable register	**0040273 (B)**	D7	**E16TC3**	16-bit timer 3 comparison A	1	Enabled	0	Disabled	0	R/W	
		D6	**E16TU3**	16-bit timer 3 comparison B					0	R/W	
		D5–4	**–**	reserved	–				–	–	0 when being read.
		D3	**E16TC2**	16-bit timer 2 comparison A	1	Enabled	0	Disabled	0	R/W	
		D2	**E16TU2**	16-bit timer 2 comparison B					0	R/W	
		D1–0	**–**	reserved	–				–	–	0 when being read.
16-bit timer 4/5 interrupt enable register	**0040274 (B)**	D7	**E16TC5**	16-bit timer 5 comparison A	1	Enabled	0	Disabled	0	R/W	
		D6	**E16TU5**	16-bit timer 5 comparison B					0	R/W	
		D5–4	**–**	reserved	–				–	–	0 when being read.
		D3	**E16TC4**	16-bit timer 4 comparison A	1	Enabled	0	Disabled	0	R/W	
		D2	**E16TU4**	16-bit timer 4 comparison B					0	R/W	
		D1–0	**–**	reserved	–				–	–	0 when being read.
8-bit timer interrupt enable register	**0040275 (B)**	D7–4	**–**	reserved	–				–	–	0 when being read.
		D3	**E8TU3**	8-bit timer 3 underflow	1	Enabled	0	Disabled	0	R/W	
		D2	**E8TU2**	8-bit timer 2 underflow					0	R/W	
		D1	**E8TU1**	8-bit timer 1 underflow					0	R/W	
		D0	**E8TU0**	8-bit timer 0 underflow					0	R/W	
Serial I/F interrupt enable register	**0040276 (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**ESTX1**	SIF Ch.1 transmit buffer empty	1	Enabled	0	Disabled	0	R/W	
		D4	**ESRX1**	SIF Ch.1 receive buffer full					0	R/W	
		D3	**ESERR1**	SIF Ch.1 receive error					0	R/W	
		D2	**ESTX0**	SIF Ch.0 transmit buffer empty					0	R/W	
		D1	**ESRX0**	SIF Ch.0 receive buffer full					0	R/W	
		D0	**ESERR0**	SIF Ch.0 receive error					0	R/W	
Port input 4–7, clock timer, A/D interrupt enable register	**0040277 (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**EP7**	Port input 7	1	Enabled	0	Disabled	0	R/W	
		D4	**EP6**	Port input 6					0	R/W	
		D3	**EP5**	Port input 5					0	R/W	
		D2	**EP4**	Port input 4					0	R/W	
		D1	**ECTM**	Clock timer					0	R/W	
		D0	**EADE**	A/D converter					0	R/W	

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
Key input, port input 0–3 interrupt factor flag register	**0040280 (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**FK1**	Key input 1	1	Factor is generated	0	No factor is generated	X	R/W	
		D4	**FK0**	Key input 0					X	R/W	
		D3	**FP3**	Port input 3					X	R/W	
		D2	**FP2**	Port input 2					X	R/W	
		D1	**FP1**	Port input 1					X	R/W	
		D0	**FP0**	Port input 0					X	R/W	
DMA interrupt factor flag register	**0040281 (B)**	D7–5	**–**	reserved	–				–	–	0 when being read.
		D4	**FIDMA**	IDMA	1	Factor is generated	0	No factor is generated	X	R/W	
		D3	**FHDM3**	High-speed DMA Ch.3					X	R/W	
		D2	**FHDM2**	High-speed DMA Ch.2					X	R/W	
		D1	**FHDM1**	High-speed DMA Ch.1					X	R/W	
		D0	**FHDM0**	High-speed DMA Ch.0					X	R/W	
16-bit timer 0/1 interrupt factor flag register	**0040282 (B)**	D7	**F16TC1**	16-bit timer 1 comparison A	1	Factor is generated	0	No factor is generated	X	R/W	
		D6	**F16TU1**	16-bit timer 1 comparison B					X	R/W	
		D5–4	**–**	reserved	–				–	–	0 when being read.
		D3	**F16TC0**	16-bit timer 0 comparison A	1	Factor is generated	0	No factor is generated	X	R/W	
		D2	**F16TU0**	16-bit timer 0 comparison B					X	R/W	
		D1–0	**–**	reserved	–				–	–	0 when being read.
16-bit timer 2/3 interrupt factor flag register	**0040283 (B)**	D7	**F16TC3**	16-bit timer 3 comparison A	1	Factor is generated	0	No factor is generated	X	R/W	
		D6	**F16TU3**	16-bit timer 3 comparison B					X	R/W	
		D5–4	**–**	reserved	–				–	–	0 when being read.
		D3	**F16TC2**	16-bit timer 2 comparison A	1	Factor is generated	0	No factor is generated	X	R/W	
		D2	**F16TU2**	16-bit timer 2 comparison B					X	R/W	
		D1–0	**–**	reserved	–				–	–	0 when being read.
16-bit timer 4/5 interrupt factor flag register	**0040284 (B)**	D7	**F16TC5**	16-bit timer 5 comparison A	1	Factor is generated	0	No factor is generated	X	R/W	
		D6	**F16TU5**	16-bit timer 5 comparison B					X	R/W	
		D5–4	–	reserved	–				–	–	0 when being read.
		D3	**F16TC4**	16-bit timer 4 comparison A	1	Factor is generated	0	No factor is generated	X	R/W	
		D2	**F16TU4**	16-bit timer 4 comparison B					X	R/W	
		D1–0	**–**	reserved	–				–	–	0 when being read.
8-bit timer interrupt factor flag register	**0040285 (B)**	D7–4	**–**	reserved	–				–	–	0 when being read.
		D3	**F8TU3**	8-bit timer 3 underflow	1	Factor is generated	0	No factor is generated	X	R/W	
		D2	**F8TU2**	8-bit timer 2 underflow					X	R/W	
		D1	**F8TU1**	8-bit timer 1 underflow					X	R/W	
		D0	**F8TU0**	8-bit timer 0 underflow					X	R/W	
Serial I/F interrupt factor flag register	**0040286 (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**FSTX1**	SIF Ch.1 transmit buffer empty	1	Factor is generated	0	No factor is generated	X	R/W	
		D4	**FSRX1**	SIF Ch.1 receive buffer full					X	R/W	
		D3	**FSERR1**	SIF Ch.1 receive error					X	R/W	
		D2	**FSTX0**	SIF Ch.0 transmit buffer empty					X	R/W	
		D1	**FSRX0**	SIF Ch.0 receive buffer full					X	R/W	
		D0	**FSERR0**	SIF Ch.0 receive error					X	R/W	
Port input 4–7, clock timer, A/D interrupt factor flag register	**0040287 (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**FP7**	Port input 7	1	Factor is generated	0	No factor is generated	X	R/W	
		D4	**FP6**	Port input 6					X	R/W	
		D3	**FP5**	Port input 5					X	R/W	
		D2	**FP4**	Port input 4					X	R/W	
		D1	**FCTM**	Clock timer					X	R/W	
		D0	**FADE**	A/D converter					X	R/W	

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
Port input 0–3, high-speed DMA, 16-bit timer 0 IDMA request register	**0040290 (B)**	D7	**R16TC0**	16-bit timer 0 comparison A	1	IDMA request	0	Interrupt request	0	R/W	
		D6	**R16TU0**	16-bit timer 0 comparison B					0	R/W	
		D5	**RHDM1**	High-speed DMA Ch.1					0	R/W	
		D4	**RHDM0**	High-speed DMA Ch.0					0	R/W	
		D3	**RP3**	Port input 3					0	R/W	
		D2	**RP2**	Port input 2					0	R/W	
		D1	**RP1**	Port input 1					0	R/W	
		D0	**RP0**	Port input 0					0	R/W	
16-bit timer 1–4 IDMA request register	**0040291 (B)**	D7	**R16TC4**	16-bit timer 4 comparison A	1	IDMA request	0	Interrupt request	0	R/W	
		D6	**R16TU4**	16-bit timer 4 comparison B					0	R/W	
		D5	**R16TC3**	16-bit timer 3 comparison A					0	R/W	
		D4	**R16TU3**	16-bit timer 3 comparison B					0	R/W	
		D3	**R16TC2**	16-bit timer 2 comparison A					0	R/W	
		D2	**R16TU2**	16-bit timer 2 comparison B					0	R/W	
		D1	**R16TC1**	16-bit timer 1 comparison A					0	R/W	
		D0	**R16TU1**	16-bit timer 1 comparison B					0	R/W	
16-bit timer 5, 8-bit timer, serial I/F Ch.0 IDMA request register	**0040292 (B)**	D7	**RSTX0**	SIF Ch.0 transmit buffer empty	1	IDMA request	0	Interrupt request	0	R/W	
		D6	**RSRX0**	SIF Ch.0 receive buffer full					0	R/W	
		D5	**R8TU3**	8-bit timer 3 underflow					0	R/W	
		D4	**R8TU2**	8-bit timer 2 underflow					0	R/W	
		D3	**R8TU1**	8-bit timer 1 underflow					0	R/W	
		D2	**R8TU0**	8-bit timer 0 underflow					0	R/W	
		D1	**R16TC5**	16-bit timer 5 comparison A					0	R/W	
		D0	**R16TU5**	16-bit timer 5 comparison B					0	R/W	
Serial I/F Ch.1, A/D, port input 4–7 IDMA request register	**0040293 (B)**	D7	**RP7**	Port input 7	1	IDMA request	0	Interrupt request	0	R/W	
		D6	**RP6**	Port input 6					0	R/W	
		D5	**RP5**	Port input 5					0	R/W	
		D4	**RP4**	Port input 4					0	R/W	
		D3	**–**	reserved	–				–	–	0 when being read.
		D2	**RADE**	A/D converter	1	IDMA request	0	Interrupt request	0	R/W	
		D1	**RSTX1**	SIF Ch.1 transmit buffer empty					0	R/W	
		D0	**RSRX1**	SIF Ch.1 receive buffer full					0	R/W	
Port input 0–3, high-speed DMA, 16-bit timer 0 IDMA enable register	**0040294 (B)**	D7	**DE16TC0**	16-bit timer 0 comparison A	1	IDMA enabled	0	IDMA disabled	0	R/W	
		D6	**DE16TU0**	16-bit timer 0 comparison B					0	R/W	
		D5	**DEHDM1**	High-speed DMA Ch.1					0	R/W	
		D4	**DEHDM0**	High-speed DMA Ch.0					0	R/W	
		D3	**DEP3**	Port input 3					0	R/W	
		D2	**DEP2**	Port input 2					0	R/W	
		D1	**DEP1**	Port input 1					0	R/W	
		D0	**DEP0**	Port input 0					0	R/W	
16-bit timer 1–4 IDMA enable register	**0040295 (B)**	D7	**DE16TC4**	16-bit timer 4 comparison A	1	IDMA enabled	0	IDMA disabled	0	R/W	
		D6	**DE16TU4**	16-bit timer 4 comparison B					0	R/W	
		D5	**DE16TC3**	16-bit timer 3 comparison A					0	R/W	
		D4	**DE16TU3**	16-bit timer 3 comparison B					0	R/W	
		D3	**DE16TC2**	16-bit timer 2 comparison A					0	R/W	
		D2	**DE16TU2**	16-bit timer 2 comparison B					0	R/W	
		D1	**DE16TC1**	16-bit timer 1 comparison A					0	R/W	
		D0	**DE16TU1**	16-bit timer 1 comparison B					0	R/W	
16-bit timer 5, 8-bit timer, serial I/F Ch.0 IDMA enable register	**0040296 (B)**	D7	**DESTX0**	SIF Ch.0 transmit buffer empty	1	IDMA enabled	0	IDMA disabled	0	R/W	
		D6	**DESRX0**	SIF Ch.0 receive buffer full					0	R/W	
		D5	**DE8TU3**	8-bit timer 3 underflow					0	R/W	
		D4	**DE8TU2**	8-bit timer 2 underflow					0	R/W	
		D3	**DE8TU1**	8-bit timer 1 underflow					0	R/W	
		D2	**DE8TU0**	8-bit timer 0 underflow					0	R/W	
		D1	**DE16TC5**	16-bit timer 5 comparison A					0	R/W	
		D0	**DE16TU5**	16-bit timer 5 comparison B					0	R/W	
Serial I/F Ch.1, A/D, port input 4–7 IDMA enable register	**0040297 (B)**	D7	**DEP7**	Port input 7	1	IDMA enabled	0	IDMA disabled	0	R/W	
		D6	**DEP6**	Port input 6					0	R/W	
		D5	**DEP5**	Port input 5					0	R/W	
		D4	**DEP4**	Port input 4					0	R/W	
		D3	**–**	reserved	–				–	–	0 when being read.
		D2	**DEADE**	A/D converter	1	IDMA enabled	0	IDMA disabled	0	R/W	
		D1	**DESTX1**	SIF Ch.1 transmit buffer empty					0	R/W	
		D0	**DESRX1**	SIF Ch.1 receive buffer full					0	R/W	

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
High-speed DMA Ch.0/1 trigger set-up register	**0040298 (B)**	D7	**HSD1S3**	High-speed DMA Ch.1 trigger set-up	0	Software trigger			0	R/W	
		D6	**HSD1S2**		1	K51 input (falling edge)			0		
		D5	**HSD1S1**		2	K51 input (rising edge)			0		
		D4	**HSD1S0**		3	Port 1 input			0		
					4	Port 5 input					
					5	8-bit timer Ch.1 underflow					
					6	16-bit timer Ch.1 compare B					
					7	16-bit timer Ch.1 compare A					
					8	16-bit timer Ch.5 compare B					
					9	16-bit timer Ch.5 compare A					
					A	SI/F Ch.1 Rx buffer full					
					B	SI/F Ch.1 Tx buffer empty					
					C	A/D conversion completion					
		D3	**HSD0S3**	High-speed DMA Ch.0 trigger set-up	0	Software trigger			0	R/W	
		D2	**HSD0S2**		1	K50 input (falling edge)			0		
		D1	**HSD0S1**		2	K50 input (rising edge)			0		
		D0	**HSD0S0**		3	Port 0 input			0		
					4	Port 4 input					
					5	8-bit timer Ch.0 underflow					
					6	16-bit timer Ch.0 compare B					
					7	16-bit timer Ch.0 compare A					
					8	16-bit timer Ch.4 compare B					
					9	16-bit timer Ch.4 compare A					
					A	SI/F Ch.0 Rx buffer full					
					B	SI/F Ch.0 Tx buffer empty					
					C	A/D conversion completion					
High-speed DMA Ch.2/3 trigger set-up register	**0040299 (B)**	D7	**HSD3S3**	High-speed DMA Ch.3 trigger set-up	0	Software trigger			0	R/W	
		D6	**HSD3S2**		1	K54 input (falling edge)			0		
		D5	**HSD3S1**		2	K54 input (rising edge)			0		
		D4	**HSD3S0**		3	Port 3 input			0		
					4	Port 7 input					
					5	8-bit timer Ch.3 underflow					
					6	16-bit timer Ch.3 compare B					
					7	16-bit timer Ch.3 compare A					
					8	16-bit timer Ch.5 compare B					
					9	16-bit timer Ch.5 compare A					
					A	SI/F Ch.1 Rx buffer full					
					B	SI/F Ch.1 Tx buffer empty					
					C	A/D conversion completion					
		D3	**HSD2S3**	High-speed DMA Ch.2 trigger set-up	0	Software trigger			0	R/W	
		D2	**HSD2S2**		1	K53 input (falling edge)			0		
		D1	**HSD2S1**		2	K53 input (rising edge)			0		
		D0	**HSD2S0**		3	Port 2 input			0		
					4	Port 6 input					
					5	8-bit timer Ch.2 underflow					
					6	16-bit timer Ch.2 compare B					
					7	16-bit timer Ch.2 compare A					
					8	16-bit timer Ch.4 compare B					
					9	16-bit timer Ch.4 compare A					
					A	SI/F Ch.0 Rx buffer full					
					B	SI/F Ch.0 Tx buffer empty					
					C	A/D conversion completion					
High-speed DMA software trigger register	**004029A (B)**	D7–4	**–**	reserved	–				–	–	0 when being read.
		D3	**HST3**	HSDMA Ch.3 software trigger	1	Trigger	0	Invalid	0	W	
		D2	**HST2**	HSDMA Ch.2 software trigger					0	W	
		D1	**HST1**	HSDMA Ch.1 software trigger					0	W	
		D0	**HST0**	HSDMA Ch.0 software trigger					0	W	
Flag set/reset method select register	**004029F (B)**	D7–3	**–**	reserved	–				–	–	
		D2	**DENONLY**	IDMA enable register set method selection	1	Set only	0	RD/WR	1	R/W	
		D1	**IDMAONLY**	IDMA request register set method selection	1	Set only	0	RD/WR	1	R/W	
		D0	**RSTONLY**	Interrupt factor flag reset method selection	1	Reset only	0	RD/WR	1	R/W	

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
K5 function select register	**00402C0 (B)**	D7–5	**–**	reserved	–				–	–	0 when being read.
		D4	**CFK54**	K54 function selection	1	#DMAREQ3	0	K54	0	R/W	
		D3	**CFK53**	K53 function selection	1	#DMAREQ2	0	K53	0	R/W	
		D2	**CFK52**	K52 function selection	1	#ADTRG	0	K52	0	R/W	
		D1	**CFK51**	K51 function selection	1	#DMAREQ1	0	K51	0	R/W	
		D0	**CFK50**	K50 function selection	1	#DMAREQ0	0	K50	0	R/W	
K5 input port data register	**00402C1 (B)**	D7–5	**–**	reserved	–				–	–	0 when being read.
		D4	**K54D**	K54 input port data	1	High	0	Low	–	R	
		D3	**K53D**	K53 input port data					–	R	
		D2	**K52D**	K52 input port data					–	R	
		D1	**K51D**	K51 input port data					–	R	
		D0	**K50D**	K50 input port data					–	R	
K6 function select register	**00402C3 (B)**	D7	**CFK67**	K67 function selection	1	AD7	0	K67	0	R/W	
		D6	**CFK66**	K66 function selection	1	AD6	0	K66	0	R/W	
		D5	**CFK65**	K65 function selection	1	AD5	0	K65	0	R/W	
		D4	**CFK64**	K64 function selection	1	AD4	0	K64	0	R/W	
		D3	**CFK63**	K63 function selection	1	AD3	0	K63	0	R/W	
		D2	**CFK62**	K62 function selection	1	AD2	0	K62	0	R/W	
		D1	**CFK61**	K61 function selection	1	AD1	0	K61	0	R/W	
		D0	**CFK60**	K60 function selection	1	AD0	0	K60	0	R/W	
K6 input port data register	**00402C4 (B)**	D7	**K67D**	K67 input port data	1	High	0	Low	–	R	
		D6	**K66D**	K66 input port data					–	R	
		D5	**K65D**	K65 input port data					–	R	
		D4	**K64D**	K64 input port data					–	R	
		D3	**K63D**	K63 input port data					–	R	
		D2	**K62D**	K62 input port data					–	R	
		D1	**K61D**	K61 input port data					–	R	
		D0	**K60D**	K60 input port data					–	R	

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
Port input interrupt select register 1	**00402C6 (B)**	D7	**SPT31**	FPT3 interrupt input port selection	11	10	01	00	0	R/W	
		D6	**SPT30**		P23	P03	K53	K63	0		
		D5	**SPT21**	FPT2 interrupt input port selection	11	10	01	00	0	R/W	
		D4	**SPT20**		P22	P02	K52	K62	0		
		D3	**SPT11**	FPT1 interrupt input port selection	11	10	01	00	0	R/W	
		D2	**SPT10**		P21	P01	K51	K61	0		
		D1	**SPT01**	FPT0 interrupt input port selection	11	10	01	00	0	R/W	
		D0	**SPT00**		P20	P00	K50	K60	0		
Port input interrupt select register 2	**00402C7 (B)**	D7	**SPT71**	FPT7 interrupt input port selection	11	10	01	00	0	R/W	
		D6	**SPT70**		P27	P07	P33	K67	0		
		D5	**SPT61**	FPT6 interrupt input port selection	11	10	01	00	0	R/W	
		D4	**SPT60**		P26	P06	P32	K66	0		
		D3	**SPT51**	FPT5 interrupt input port selection	11	10	01	00	0	R/W	
		D2	**SPT50**		P25	P05	P31	K65	0		
		D1	**SPT41**	FPT4 interrupt input port selection	11	10	01	00	0	R/W	
		D0	**SPT40**		P24	P04	K54	K64	0		
Port input interrupt input polarity select register	**00402C8 (B)**	D7	**SPPT7**	FPT7 input polarity selection	1	High level	0	Low level	1	R/W	
		D6	**SPPT6**	FPT6 input polarity selection		or		or	1	R/W	
		D5	**SPPT5**	FPT5 input polarity selection		Rising edge		Falling	1	R/W	
		D4	**SPPT4**	FPT4 input polarity selection				edge	1	R/W	
		D3	**SPPT3**	FPT3 input polarity selection					1	R/W	
		D2	**SPPT2**	FPT2 input polarity selection					1	R/W	
		D1	**SPPT1**	FPT1 input polarity selection					1	R/W	
		D0	**SPPT0**	FPT0 input polarity selection					1	R/W	
Port input interrupt edge/level select register	**00402C9 (B)**	D7	**SEPT7**	FPT7 edge/level selection	1	Edge	0	Level	1	R/W	
		D6	**SEPT6**	FPT6 edge/level selection					1	R/W	
		D5	**SEPT5**	FPT5 edge/level selection					1	R/W	
		D4	**SEPT4**	FPT4 edge/level selection					1	R/W	
		D3	**SEPT3**	FPT3 edge/level selection					1	R/W	
		D2	**SEPT2**	FPT2 edge/level selection					1	R/W	
		D1	**SEPT1**	FPT1 edge/level selection					1	R/W	
		D0	**SEPT0**	FPT0 edge/level selection					1	R/W	
Key input interrupt select register	**00402CA (B)**	D7–4	**–**	reserved	–				–	–	0 when being read.
		D3	**SPPK11**	FPK1 nterrupt input port selection	11	10	01	00	0	R/W	
		D2	**SPPK10**		P2[7:4]	P0[7:4]	K6[7:4]	K6[3:0]	0		
		D1	**SPPK01**	FPK0 nterrupt input port selection	11	10	01	00	0	R/W	
		D0	**SPPK00**		P2[4:0]	P0[4:0]	K6[4:0]	K5[4:0]	0		
Key input interrupt (FPK0) input comparison register	**00402CC (B)**	D7–5	**–**	reserved	–				–	–	0 when being read.
		D4	**SCPK04**	FPK04 input comparison	1	High	0	Low	0	R/W	
		D3	**SCPK03**	FPK03 input comparison					0	R/W	
		D2	**SCPK02**	FPK02 input comparison					0	R/W	
		D1	**SCPK01**	FPK01 input comparison					0	R/W	
		D0	**SCPK00**	FPK00 input comparison					0	R/W	
Key input interrupt (FPK1) input comparison register	**00402CD (B)**	D7–4	**–**	reserved	–				–	–	0 when being read.
		D3	**SCPK13**	FPK13 input comparison	1	High	0	Low	0	R/W	
		D2	**SCPK12**	FPK12 input comparison					0	R/W	
		D1	**SCPK11**	FPK11 input comparison					0	R/W	
		D0	**SCPK10**	FPK10 input comparison					0	R/W	
Key input interrupt (FPK0) input mask register	**00402CE (B)**	D7–5	**–**	reserved	–				–	–	0 when being read.
		D4	**SMPK04**	FPK04 input mask	1	Interrupt	0	Interrupt	0	R/W	
		D3	**SMPK03**	FPK03 input mask		enabled		disabled	0	R/W	
		D2	**SMPK02**	FPK02 input mask					0	R/W	
		D1	**SMPK01**	FPK01 input mask					0	R/W	
		D0	**SMPK00**	FPK00 input mask					0	R/W	
Key input interrupt (FPK1) input mask register	**00402CF (B)**	D7–4	**–**	reserved	–				–	–	0 when being read.
		D3	**SMPK13**	FPK13 input mask	1	Interrupt	0	Interrupt	0	R/W	
		D2	**SMPK12**	FPK12 input mask		enabled		disabled	0	R/W	
		D1	**SMPK11**	FPK11 input mask					0	R/W	
		D0	**SMPK10**	FPK10 input mask					0	R/W	

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
P0 function select register	**00402D0 (B)**	D7	**CFP07**	P07 function selection	1	#SRDY1	0	P07	0	R/W	Extended functions (0x402DF)
		D6	**CFP06**	P06 function selection	1	#SCLK1	0	P06	0	R/W	
		D5	**CFP05**	P05 function selection	1	SOUT1	0	P05	0	R/W	
		D4	**CFP04**	P04 function selection	1	SIN1	0	P04	0	R/W	
		D3	**CFP03**	P03 function selection	1	#SRDY0	0	P03	0	R/W	
		D2	**CFP02**	P02 function selection	1	#SCLK0	0	P02	0	R/W	
		D1	**CFP01**	P01 function selection	1	SOUT0	0	P01	0	R/W	
		D0	**CFP00**	P00 function selection	1	SIN0	0	P00	0	R/W	
P0 I/O port data register	**00402D1 (B)**	D7	**P07D**	P07 I/O port data	1	High	0	Low	0	R/W	
		D6	**P06D**	P06 I/O port data					0	R/W	
		D5	**P05D**	P05 I/O port data					0	R/W	
		D4	**P04D**	P04 I/O port data					0	R/W	
		D3	**P03D**	P03 I/O port data					0	R/W	
		D2	**P02D**	P02 I/O port data					0	R/W	
		D1	**P01D**	P01 I/O port data					0	R/W	
		D0	**P00D**	P00 I/O port data					0	R/W	
P0 I/O control register	**00402D2 (B)**	D7	**IOC07**	P07 I/O control	1	Output	0	Input	0	R/W	
		D6	**IOC06**	P06 I/O control					0	R/W	
		D5	**IOC05**	P05 I/O control					0	R/W	
		D4	**IOC04**	P04 I/O control					0	R/W	
		D3	**IOC03**	P03 I/O control					0	R/W	
		D2	**IOC02**	P02 I/O control					0	R/W	
		D1	**IOC01**	P01 I/O control					0	R/W	
		D0	**IOC00**	P00 I/O control					0	R/W	
P1 function select register	**00402D4 (B)**	D7	**–**	reserved	–				–	–	0 when being read.
		D6	**CFP16**	P16 function selection	1	EXCL5 #DMAEND1	0	P16	0	R/W	
		D5	**CFP15**	P15 function selection	1	EXCL4 #DMAEND0	0	P15	0	R/W	
		D4	**CFP14**	P14 function selection	1	FOSC1	0	P14	0	R/W	Extended functions (0x402DF)
		D3	**CFP13**	P13 function selection	1	EXCL3 T8UF3	0	P13	0	R/W	
		D2	**CFP12**	P12 function selection	1	EXCL2 T8UF2	0	P12	0	R/W	
		D1	**CFP11**	P11 function selection	1	EXCL1 T8UF1	0	P11	0	R/W	
		D0	**CFP10**	P10 function selection	1	EXCL0 T8UF0	0	P10	0	R/W	
P1 I/O port data register	**00402D5 (B)**	D7	**–**	reserved	–				–	–	0 when being read.
		D6	**P16D**	P16 I/O port data	1	High	0	Low	0	R/W	
		D5	**P15D**	P15 I/O port data					0	R/W	
		D4	**P14D**	P14 I/O port data					0	R/W	
		D3	**P13D**	P13 I/O port data					0	R/W	
		D2	**P12D**	P12 I/O port data					0	R/W	
		D1	**P11D**	P11 I/O port data					0	R/W	
		D0	**P10D**	P10 I/O port data					0	R/W	
P1 I/O control register	**00402D6 (B)**	D7	**–**	reserved	–				–	–	0 when being read.
		D6	**IOC16**	P16 I/O control	1	Output	0	Input	0	R/W	
		D5	**IOC15**	P15 I/O control					0	R/W	
		D4	**IOC14**	P14 I/O control					0	R/W	
		D3	**IOC13**	P13 I/O control					0	R/W	
		D2	**IOC12**	P12 I/O control					0	R/W	
		D1	**IOC11**	P11 I/O control					0	R/W	
		D0	**IOC10**	P10 I/O control					0	R/W	
P2 function select register	**00402D8 (B)**	D7	**CFP27**	P27 function selection	1	TM5	0	P27	0	R/W	
		D6	**CFP26**	P26 function selection	1	TM4	0	P26	0	R/W	
		D5	**CFP25**	P25 function selection	1	TM3	0	P25	0	R/W	
		D4	**CFP24**	P24 function selection	1	TM2	0	P24	0	R/W	
		D3	**CFP23**	P23 function selection	1	TM1	0	P23	0	R/W	
		D2	**CFP22**	P22 function selection	1	TM0	0	P22	0	R/W	
		D1	**CFP21**	P21 function selection	1	#DWE	0	P21	0	R/W	Ext. func.(0x402DF)
		D0	**CFP20**	P20 function selection	1	#DRD	0	P20	0	R/W	
P2 I/O port data register	**00402D9 (B)**	D7	**P27D**	P27 I/O port data	1	High	0	Low	0	R/W	
		D6	**P26D**	P26 I/O port data					0	R/W	
		D5	**P25D**	P25 I/O port data					0	R/W	
		D4	**P24D**	P24 I/O port data					0	R/W	
		D3	**P23D**	P23 I/O port data					0	R/W	
		D2	**P22D**	P22 I/O port data					0	R/W	
		D1	**P21D**	P21 I/O port data					0	R/W	
		D0	**P20D**	P20 I/O port data					0	R/W	

Register name	Address	Bit	Name	Function	Setting				Init.	R/W	Remarks
P2 I/O control register	**00402DA (B)**	D7	**IOC27**	P27 I/O control	1	Output	0	Input	0	R/W	
		D6	**IOC26**	P26 I/O control					0	R/W	
		D5	**IOC25**	P25 I/O control					0	R/W	
		D4	**IOC24**	P24 I/O control					0	R/W	
		D3	**IOC23**	P23 I/O control					0	R/W	
		D2	**IOC22**	P22 I/O control					0	R/W	
		D1	**IOC21**	P21 I/O control					0	R/W	
		D0	**IOC20**	P20 I/O control					0	R/W	
P3 function select register	**00402DC (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**CFP35**	P35 function selection	1	#BUSACK	0	P35	0	R/W	
		D4	**CFP34**	P34 function selection	1	#BUSREQ #CE6	0	P34	0	R/W	
		D3	**CFP33**	P33 function selection	1	#DMAACK1	0	P33	0	R/W	
		D2	**CFP32**	P32 function selection	1	#DMAACK0	0	P32	0	R/W	
		D1	**CFP31**	P31 function selection	1	#BUSGET	0	P31	0	R/W	Ext. func.(0x402DF)
		D0	**CFP30**	P30 function selection	1	#WAIT #CE4/#CE5	0	P30	0	R/W	
P3 I/O port data register	**00402DD (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**P35D**	P35 I/O port data	1	High	0	Low	0	R/W	
		D4	**P34D**	P34 I/O port data					0	R/W	
		D3	**P33D**	P33 I/O port data					0	R/W	
		D2	**P32D**	P32 I/O port data					0	R/W	
		D1	**P31D**	P31 I/O port data					0	R/W	
		D0	**P30D**	P30 I/O port data					0	R/W	
P3 I/O control register	**00402DE (B)**	D7–6	**–**	reserved	–				–	–	0 when being read.
		D5	**IOC35**	P35 I/O control	1	Output	0	Input	0	R/W	
		D4	**IOC34**	P34 I/O control					0	R/W	
		D3	**IOC33**	P33 I/O control					0	R/W	
		D2	**IOC32**	P32 I/O control					0	R/W	
		D1	**IOC31**	P31 I/O control					0	R/W	
		D0	**IOC30**	P30 I/O control					0	R/W	
Port function extension register	**00402DF (B)**	D7	**CFEX7**	P07 port extended function	1	#DMAEND3	0	P07, etc.	0	R/W	
		D6	**CFEX6**	P06 port extended function	1	#DMAACK3	0	P06, etc.	0	R/W	
		D5	**CFEX5**	P05 port extended function	1	#DMAEND2	0	P05, etc.	0	R/W	
		D4	**CFEX4**	P04 port extended function	1	#DMAACK2	0	P04, etc.	0	R/W	
		D3	**CFEX3**	P31 port extended function	1	#GARD	0	P31, etc.	0	R/W	
		D2	**CFEX2**	P21 port extended function	1	#GAAS	0	P21, etc.	0	R/W	
		D1	**CFEX1**	P10, P11, P13 port extended function	1	DST0 DST1 DPC0	0	P10, etc. P11, etc. P13, etc.	1	R/W	
		D0	**CFEX0**	P12, P14 port extended function	1	DST2 DCLK	0	P12, etc. P14, etc.	1	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Areas 18–15 set-up register	**0048120 (HW)**	DF	**–**	reserved	–	–	–	0 when being read.
		DE	**A18SZ**	Areas 18–17 device size selection	1: 8 bits / 0: 16 bits	0	R/W	
		DD DC	**A18DF1** **A18DF0**	Areas 18–17 output disable delay time	A18DF[1:0] / Number of cycles 1 1: 3.5 1 0: 2.5 0 1: 1.5 0 0: 0.5	1 1	R/W	
		DB	**–**	reserved	–	–	–	0 when being read.
		DA D9 D8	**A18WT2** **A18WT1** **A18WT0**	Areas 18–17 wait control	A18WT[2:0] / Wait cycles 1 1 1: 7 1 1 0: 6 1 0 1: 5 1 0 0: 4 0 1 1: 3 0 1 0: 2 0 0 1: 1 0 0 0: 0	1 1 1	R/W	
		D7	**–**	reserved	–	–	–	0 when being read.
		D6	**A16SZ**	Areas 16–15 device size selection	1: 8 bits / 0: 16 bits	0	R/W	
		D5 D4	**A16DF1** **A16DF0**	Areas 16–15 output disable delay time	A16DF[1:0] / Number of cycles 1 1: 3.5 1 0: 2.5 0 1: 1.5 0 0: 0.5	1 1	R/W	
		D3	**–**	reserved	–	–	–	0 when being read.
		D2 D1 D0	**A16WT2** **A16WT1** **A16WT0**	Areas 16–15 wait control	A16WT[2:0] / Wait cycles 1 1 1: 7 1 1 0: 6 1 0 1: 5 1 0 0: 4 0 1 1: 3 0 1 0: 2 0 0 1: 1 0 0 0: 0	1 1 1	R/W	
Areas 14–13 set-up register	**0048122 (HW)**	DF–9	**–**	reserved	–	–	–	0 when being read.
		D8	**A14DRA**	Area 14 DRAM selection	1: Used / 0: Not used	0	R/W	
		D7	**A13DRA**	Area 13 DRAM selection	1: Used / 0: Not used	0	R/W	
		D6	**A14SZ**	Areas 14–13 device size selection	1: 8 bits / 0: 16 bits	0	R/W	
		D5 D4	**A14DF1** **A14DF0**	Areas 14–13 output disable delay time	A14DF[1:0] / Number of cycles 1 1: 3.5 1 0: 2.5 0 1: 1.5 0 0: 0.5	1 1	R/W	
		D3	**–**	reserved	–	–	–	0 when being read.
		D2 D1 D0	**A14WT2** **A14WT1** **A14WT0**	Areas 14–13 wait control	A14WT[2:0] / Wait cycles 1 1 1: 7 1 1 0: 6 1 0 1: 5 1 0 0: 4 0 1 1: 3 0 1 0: 2 0 0 1: 1 0 0 0: 0	1 1 1	R/W	
Areas 12–11 set-up register	**0048124 (HW)**	DF–7	**–**	reserved	–	–	–	0 when being read.
		D6	**A12SZ**	Areas 12–11 device size selection	1: 8 bits / 0: 16 bits	0	R/W	
		D5 D4	**A12DF1** **A12DF0**	Areas 12–11 output disable delay time	A18DF[1:0] / Number of cycles 1 1: 3.5 1 0: 2.5 0 1: 1.5 0 0: 0.5	1 1	R/W	
		D3	**–**	reserved	–	–	–	0 when being read.
		D2 D1 D0	**A12WT2** **A12WT1** **A12WT0**	Areas 12–11 wait control	A18WT[2:0] / Wait cycles 1 1 1: 7 1 1 0: 6 1 0 1: 5 1 0 0: 4 0 1 1: 3 0 1 0: 2 0 0 1: 1 0 0 0: 0	1 1 1	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Areas 10–9 set-up register	**0048126 (HW)**	DF	**–**	reserved	–	–	–	0 when being read.
		DE	**A10IR2**	Area 10 internal ROM wait control	A10IR[2:0] ROM size	1	R/W	
		DD	**A10IR1**	Area 10 internal ROM size	1 1 1 2MB	1		
		DC	**A10IR0**	selection	1 1 0 1MB	1		
					1 0 1 512KB			
					1 0 0 256KB			
					0 1 1 128KB			
					0 1 0 64KB			
					0 0 1 32KB			
					0 0 0 16KB			
		DB	**–**	reserved	–	–	–	0 when being read.
		DA	**A10BW1**	Areas 10–9	A10BW[1:0] Wait cycles	0	R/W	
		D9	**A10BW0**	burst ROM	1 1 3	0		
				burst read cycle wait control	1 0 2			
					0 1 1			
					0 0 0			
		D8	**A10DRA**	Area 10 burst ROM selection	1 Used 0 Not used	0	R/W	
		D7	**A9DRA**	Area 9 burst ROM selection	1 Used 0 Not used	0	R/W	
		D6	**A10SZ**	Areas 10–9 device size selection	1 8 bits 0 16 bits	0	R/W	
		D5	**A10DF1**	Areas 10–9	A10DF[1:0] Number of cycles	1	R/W	
		D4	**A10DF0**	output disable delay time	1 1 3.5	1		
					1 0 2.5			
					0 1 1.5			
					0 0 0.5			
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**A10WT2**	Areas 10–9 wait control	A10WT[2:0] Wait cycles	1	R/W	
		D1	**A10WT1**		1 1 1 7	1		
		D0	**A10WT0**		1 1 0 6	1		
					1 0 1 5			
					1 0 0 4			
					0 1 1 3			
					0 1 0 2			
					0 0 1 1			
					0 0 0 0			
Areas 8–7 set-up register	**0048128 (HW)**	DF–9	**–**	reserved	–	–	–	0 when being read.
		D8	**A8DRA**	Area 8 DRAM selection	1 Used 0 Not used	0	R/W	
		D7	**A7DRA**	Area 7 DRAM selection	1 Used 0 Not used	0	R/W	
		D6	**A8SZ**	Areas 8–7 device size selection	1 8 bits 0 16 bits	0	R/W	
		D5	**A8DF1**	Areas 8–7	A8DF[1:0] Number of cycles	1	R/W	
		D4	**A8DF0**	output disable delay time	1 1 3.5	1		
					1 0 2.5			
					0 1 1.5			
					0 0 0.5			
		D3	**–**	reserved	–	–	–	0 when being read.
		D2	**A8WT2**	Areas 8–7 wait control	A8WT[2:0] Wait cycles	1	R/W	
		D1	**A8WT1**		1 1 1 7	1		
		D0	**A8WT0**		1 1 0 6	1		
					1 0 1 5			
					1 0 0 4			
					0 1 1 3			
					0 1 0 2			
					0 0 1 1			
					0 0 0 0			

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
Areas 6–4 set-up register	**004812A (HW)**	DF–E	**–**	reserved	–	–	–	0 when being read.
		DD	**A6DF1**	Area 6	A6DF[1:0] Number of cycles	1	R/W	
		DC	**A6DF0**	output disable delay time	1 1 3.5	1		
					1 0 2.5			
					0 1 1.5			
					0 0 0.5			
		DB	**–**	reserved	–	–	–	0 when being read.
		DA	**A6WT2**	Area 6 wait control	A6WT[2:0] Wait cycles	1	R/W	
		D9	**A6WT1**		1 1 1 7	1		
		D8	**A6WT0**		1 1 0 6	1		
					1 0 1 5			
					1 0 0 4			
					0 1 1 3			
					0 1 0 2			
					0 0 1 1			
					0 0 0 0			
		D7	**–**	reserved	–	–	–	0 when being read.
		D6	**A5SZ**	Areas 5–4 device size selection	1 8 bits 0 16 bits	0	R/W	
		D5	**A5DF1**	Areas 5–4	A5DF[1:0] Number of cycles	1	R/W	
		D4	**A5DF0**	output disable delay time	1 1 3.5	1		
					1 0 2.5			
					0 1 1.5			
					0 0 0.5			
		D3	**–**	reserved		–	–	0 when being read.
		D2	**A5WT2**	Areas 5–4 wait control	A5WT[2:0] Wait cycles	1	R/W	
		D1	**A5WT1**		1 1 1 7	1		
		D0	**A5WT0**		1 1 0 6	1		
					1 0 1 5			
					1 0 0 4			
					0 1 1 3			
					0 1 0 2			
					0 0 1 1			
					0 0 0 0			
TTBR write protect register	**004812D (B)**	D7	**TBRP7**	TTBR register write protect	Writing 01011001(0x59)	0	W	Undefined in read.
		D6	**TBRP6**		removes the TTBR (0x48134)	0		
		D5	**TBRP5**		write protection.	0		
		D4	**TBRP4**		Writing other data sets the	0		
		D3	**TBRP3**		write protection.	0		
		D2	**TBRP2**			0		
		D1	**TBRP1**			0		
		D0	**TBRP0**			0		
Bus control register	**004812E (HW)**	DF	**RBCLK**	BCLK output control	1 Fixed at H 0 Enabled	0	R/W	
		DE	**–**	reserved	–	0	–	Writing 1 not allowed.
		DD	**RBST8**	Burst ROM burst mode selection	1 8-successive 0 4-successive	0	R/W	
		DC	**REDO**	DRAM page mode selection	1 EDO 0 Fast page	0	R/W	
		DB	**RCA1**	Column address size selection	RCA[1:0] Size	0	R/W	
		DA	**RCA0**		1 1 11	0		
					1 0 10			
					0 1 9			
					0 0 8			
		D9	**RPC2**	Refresh enable	1 Enabled 0 Disabled	0	R/W	
		D8	**RPC1**	Refresh method selection	1 Self-refresh 0 CBR-refresh	0	R/W	
		D7	**RPC0**	Refresh RPC delay setup	1 2.0 0 1.0	0	R/W	
		D6	**RRA1**	Refresh RAS pulse width	RRA[1:0] Number of cycles	0	R/W	
		D5	**RRA0**	selection	1 1 5	0		
					1 0 4			
					0 1 3			
					0 0 2			
		D4	**–**	reserved	–	0	–	Writing 1 not allowed.
		D3	**SBUSST**	External interface method selection	1 #BSL 0 A0	0	R/W	
		D2	**SEMAS**	External bus master setup	1 Existing 0 Nonexistent	0	R/W	
		D1	**SEPD**	External power-down control	1 Enabled 0 Disabled	0	R/W	
		D0	**SWAITE**	#WAIT enable	1 Enabled 0 Disabled	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
DRAM timing set-up register	**0048130 (HW)**	DF–C	**–**	reserved	–	–	–	0 when being read.
		DB	**A3EEN**	Area 3 emulation	1: Internal ROM, 0: Emulation	1	R/W	
		DA	**CEFUNC1**	#CE pin function selection	CFFUNC[1:0]: #CE output	0	R/W	
		D9	**CEFUNC0**		1 x: #CE7/8..#CE17/18	0		
					0 1: #CE6..#CE17			
					0 0: #CE4..#CE10			
		D8	**CRAS**	Successive RAS mode setup	1: Successive, 0: Normal	0	R/W	
		D7	**RPRC1**	DRAM	RPRC[1:0]: Number of cycles	0	R/W	
		D6	**RPRC0**	RAS precharge cycles selection	1 1: 4	0		
					1 0: 3			
					0 1: 2			
					0 0: 1			
		D5	**–**	reserved	–	–	–	0 when being read.
		D4	**CASC1**	DRAM	CASC[1:0]: Number of cycles	0	R/W	
		D3	**CASC0**	CAS cycles selection	1 1: 4	0		
					1 0: 3			
					0 1: 2			
					0 0: 1			
		D2	**–**	reserved	–	–	–	0 when being read.
		D1	**RASC1**	DRAM	RASC[1:0]: Number of cycles	0	R/W	
		D0	**RASC0**	RAS cycles selection	1 1: 4	0		
					1 0: 3			
					0 1: 2			
					0 0: 1			
Access control register	**0048132 (HW)**	DF	**A18IO**	Area 18, 17 internal/external access	1: Internal access, 0: External access	0	R/W	
		DE	**A16IO**	Area 16, 15 internal/external access		0	R/W	
		DD	**A14IO**	Area 14, 13 internal/external access		0	R/W	
		DC	**A12IO**	Area 12, 11 internal/external access		0	R/W	
		DB	**–**	reserved	–	0	–	0 when being read.
		DA	**A8IO**	Area 8, 7 internal/external access	1: Internal access, 0: External access	0	R/W	
		D9	**A6IO**	Area 6 internal/external access		0	R/W	
		D8	**A5IO**	Area 5, 4 internal/external access		0	R/W	
		D7	**A18EC**	Area 18, 17 endian control	1: Big endian, 0: Little endian	0	R/W	
		D6	**A16EC**	Area 16, 15 endian control		0	R/W	
		D5	**A14EC**	Area 14, 13 endian control		0	R/W	
		D4	**A12EC**	Area 12, 11 endian control		0	R/W	
		D3	**A10EC**	Area 10, 9 endian control		0	R/W	
		D2	**A8EC**	Area 8, 7 endian control		0	R/W	
		D1	**A6EC**	Area 6 endian control		0	R/W	
		D0	**A5EC**	Area 5, 4 endian control		0	R/W	
TTBR low-order register	**0048134 (HW)**	DF	**TTBR15**	Trap table base address [15:10]		0	R/W	
		DE	**TTBR14**			0		
		DD	**TTBR13**			0		
		DC	**TTBR12**			0		
		DB	**TTBR11**			0		
		DA	**TTBR10**			0		
		D9	**TTBR09**	Trap table base address [9:0]	Fixed at 0	0	R	0 when being read.
		D8	**TTBR08**			0		Writing 1 not allowed.
		D7	**TTBR07**			0		
		D6	**TTBR06**			0		
		D5	**TTBR05**			0		
		D4	**TTBR04**			0		
		D3	**TTBR03**			0		
		D2	**TTBR02**			0		
		D1	**TTBR01**			0		
		D0	**TTBR00**			0		
TTBR high-order register	**0048136 (HW)**	DF	**TTBR33**	Trap table base address [31:28]	Fixed at 0	0	R	0 when being read.
		DE	**TTBR32**			0		Writing 1 not allowed.
		DD	**TTBR31**			0		
		DC	**TTBR30**			0		
		DB	**TTBR2B**	Trap table base address [27:16]	The initial value is set according to the BTA3 pin status. BTA3 = "1": 0x008 BTA3 = "0": 0x0C0	←	R/W	
		DA	**TTBR2A**					
		D9	**TTBR29**					
		D8	**TTBR28**					
		D7	**TTBR27**					
		D6	**TTBR26**					
		D5	**TTBR25**					
		D4	**TTBR24**					
		D3	**TTBR23**					
		D2	**TTBR22**					
		D1	**TTBR21**					
		D0	**TTBR20**					

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
G/A read signal control register	**0048138 (HW)**	DF	**A18AS**	Area 18, 17 address strobe signal	1 Enabled 0 Disabled	0	R/W	
		DE	**A16AS**	Area 16, 15 address strobe signal		0	R/W	
		DD	**A14AS**	Area 14, 13 address strobe signal		0	R/W	
		DC	**A12AS**	Area 12, 11 address strobe signal		0	R/W	
		DB	**–**	reserved	–	0	–	0 when being read.
		DA	**A8AS**	Area 8, 7 address strobe signal	1 Enabled 0 Disabled	0	R/W	
		D9	**A6AS**	Area 6 address strobe signal		0	R/W	
		D8	**A5AS**	Area 5, 4 address strobe signal		0	R/W	
		D7	**A18RD**	Area 18, 17 read signal	1 Enabled 0 Disabled	0	R/W	
		D6	**A16RD**	Area 16, 15 read signal		0	R/W	
		D5	**A14RD**	Area 14, 13 read signal		0	R/W	
		D4	**A12RD**	Area 12, 11 read signal		0	R/W	
		D3	**–**	reserved	–	0	–	0 when being read.
		D2	**A8RD**	Area 8, 7 read signal	1 Enabled 0 Disabled	0	R/W	
		D1	**A6RD**	Area 6 read signal		0	R/W	
		D0	**A5RD**	Area 5, 4 read signal		0	R/W	
BCLK select register	**004813A (B)**	D7–4	**–**	reserved	–	0	–	0 when being read.
		D3	**A1X1MD**	Area 1 access-speed	1 2 cycles 0 4 cycles	0	R/W	x2 speed mode only
		D2	**–**	reserved	–	0	–	0 when being read.
		D1	**BCLKSEL1**	BCLK output clock selection	BCLKSEL[1:0] BCLK	0	R/W	
		D0	**BCLKSEL0**		1 1 PLL_CLK	0		
					1 0 OSC3_CLK			
					0 1 BCU_CLK			
					0 0 CPU_CLK			

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
16-bit timer 0 comparison register A	**0048180 (HW)**	DF	**CR0A15**	16-bit timer 0 comparison data A	0 to 65535	X	R/W	
		DE	**CR0A14**	CR0A15 = MSB		X		
		DD	**CR0A13**	CR0A0 = LSB		X		
		DC	**CR0A12**			X		
		DB	**CR0A11**			X		
		DA	**CR0A10**			X		
		D9	**CR0A9**			X		
		D8	**CR0A8**			X		
		D7	**CR0A7**			X		
		D6	**CR0A6**			X		
		D5	**CR0A5**			X		
		D4	**CR0A4**			X		
		D3	**CR0A3**			X		
		D2	**CR0A2**			X		
		D1	**CR0A1**			X		
		D0	**CR0A0**			X		
16-bit timer 0 comparison register B	**0048182 (HW)**	DF	**CR0B15**	16-bit timer 0 comparison data B	0 to 65535	X	R/W	
		DE	**CR0B14**	CR0B15 = MSB		X		
		DD	**CR0B13**	CR0B0 = LSB		X		
		DC	**CR0B12**			X		
		DB	**CR0B11**			X		
		DA	**CR0B10**			X		
		D9	**CR0B9**			X		
		D8	**CR0B8**			X		
		D7	**CR0B7**			X		
		D6	**CR0B6**			X		
		D5	**CR0B5**			X		
		D4	**CR0B4**			X		
		D3	**CR0B3**			X		
		D2	**CR0B2**			X		
		D1	**CR0B1**			X		
		D0	**CR0B0**			X		
16-bit timer 0 counter data register	**0048184 (HW)**	DF	**TC015**	16-bit timer 0 counter data	0 to 65535	X	R	
		DE	**TC014**	TC015 = MSB		X		
		DD	**TC013**	TC00 = LSB		X		
		DC	**TC012**			X		
		DB	**TC011**			X		
		DA	**TC010**			X		
		D9	**TC09**			X		
		D8	**TC08**			X		
		D7	**TC07**			X		
		D6	**TC06**			X		
		D5	**TC05**			X		
		D4	**TC04**			X		
		D3	**TC03**			X		
		D2	**TC02**			X		
		D1	**TC01**			X		
		D0	**TC00**			X		
16-bit timer 0 control register	**0048186 (B)**	D7	**–**	reserved	–	0	–	0 when being read.
		D6	**SELFM0**	16-bit timer 0 fine mode selection	1 Fine mode / 0 Normal	0	R/W	
		D5	**SELCRB0**	16-bit timer 0 comparison buffer	1 Enabled / 0 Disabled	0	R/W	
		D4	**OUTINV0**	16-bit timer 0 output inversion	1 Invert / 0 Normal	0	R/W	
		D3	**CKSL0**	16-bit timer 0 input clock selection	1 External clock / 0 Internal clock	0	R/W	
		D2	**PTM0**	16-bit timer 0 clock output control	1 On / 0 Off	0	R/W	
		D1	**PRESET0**	16-bit timer 0 reset	1 Reset / 0 Invalid	0	W	0 when being read.
		D0	**PRUN0**	16-bit timer 0 Run/Stop control	1 Run / 0 Stop	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
16-bit timer 1 comparison register A	**0048188 (HW)**	DF	**CR1A15**	16-bit timer 1 comparison data A	0 to 65535	X	R/W	
		DE	**CR1A14**	CR1A15 = MSB		X		
		DD	**CR1A13**	CR1A0 = LSB		X		
		DC	**CR1A12**			X		
		DB	**CR1A11**			X		
		DA	**CR1A10**			X		
		D9	**CR1A9**			X		
		D8	**CR1A8**			X		
		D7	**CR1A7**			X		
		D6	**CR1A6**			X		
		D5	**CR1A5**			X		
		D4	**CR1A4**			X		
		D3	**CR1A3**			X		
		D2	**CR1A2**			X		
		D1	**CR1A1**			X		
		D0	**CR1A0**			X		
16-bit timer 1 comparison register B	**004818A (HW)**	DF	**CR1B15**	16-bit timer 1 comparison data B	0 to 65535	X	R/W	
		DE	**CR1B14**	CR1B15 = MSB		X		
		DD	**CR1B13**	CR1B0 = LSB		X		
		DC	**CR1B12**			X		
		DB	**CR1B11**			X		
		DA	**CR1B10**			X		
		D9	**CR1B9**			X		
		D8	**CR1B8**			X		
		D7	**CR1B7**			X		
		D6	**CR1B6**			X		
		D5	**CR1B5**			X		
		D4	**CR1B4**			X		
		D3	**CR1B3**			X		
		D2	**CR1B2**			X		
		D1	**CR1B1**			X		
		D0	**CR1B0**			X		
16-bit timer 1 counter data register	**004818C (HW)**	DF	**TC115**	16-bit timer 1 counter data	0 to 65535	X	R	
		DE	**TC114**	TC115 = MSB		X		
		DD	**TC113**	TC10 = LSB		X		
		DC	**TC112**			X		
		DB	**TC111**			X		
		DA	**TC110**			X		
		D9	**TC19**			X		
		D8	**TC18**			X		
		D7	**TC17**			X		
		D6	**TC16**			X		
		D5	**TC15**			X		
		D4	**TC14**			X		
		D3	**TC13**			X		
		D2	**TC12**			X		
		D1	**TC11**			X		
		D0	**TC10**			X		
16-bit timer 1 control register	**004818E (B)**	D7	**–**	reserved	–	0	–	0 when being read.
		D6	**SELFM1**	16-bit timer 1 fine mode selection	1 Fine mode / 0 Normal	0	R/W	
		D5	**SELCRB1**	16-bit timer 1 comparison buffer	1 Enabled / 0 Disabled	0	R/W	
		D4	**OUTINV1**	16-bit timer 1 output inversion	1 Invert / 0 Normal	0	R/W	
		D3	**CKSL1**	16-bit timer 1 input clock selection	1 External clock / 0 Internal clock	0	R/W	
		D2	**PTM1**	16-bit timer 1 clock output control	1 On / 0 Off	0	R/W	
		D1	**PRESET1**	16-bit timer 1 reset	1 Reset / 0 Invalid	0	W	0 when being read.
		D0	**PRUN1**	16-bit timer 1 Run/Stop control	1 Run / 0 Stop	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
16-bit timer 2 comparison register A	**0048190 (HW)**	DF	**CR2A15**	16-bit timer 2 comparison data A	0 to 65535	X	R/W	
		DE	**CR2A14**	CR2A15 = MSB		X		
		DD	**CR2A13**	CR2A0 = LSB		X		
		DC	**CR2A12**			X		
		DB	**CR2A11**			X		
		DA	**CR2A10**			X		
		D9	**CR2A9**			X		
		D8	**CR2A8**			X		
		D7	**CR2A7**			X		
		D6	**CR2A6**			X		
		D5	**CR2A5**			X		
		D4	**CR2A4**			X		
		D3	**CR2A3**			X		
		D2	**CR2A2**			X		
		D1	**CR2A1**			X		
		D0	**CR2A0**			X		
16-bit timer 2 comparison register B	**0048192 (HW)**	DF	**CR2B15**	16-bit timer 2 comparison data B	0 to 65535	X	R/W	
		DE	**CR2B14**	CR2B15 = MSB		X		
		DD	**CR2B13**	CR2B0 = LSB		X		
		DC	**CR2B12**			X		
		DB	**CR2B11**			X		
		DA	**CR2B10**			X		
		D9	**CR2B9**			X		
		D8	**CR2B8**			X		
		D7	**CR2B7**			X		
		D6	**CR2B6**			X		
		D5	**CR2B5**			X		
		D4	**CR2B4**			X		
		D3	**CR2B3**			X		
		D2	**CR2B2**			X		
		D1	**CR2B1**			X		
		D0	**CR2B0**			X		
16-bit timer 2 counter data register	**0048194 (HW)**	DF	**TC215**	16-bit timer 2 counter data	0 to 65535	X	R	
		DE	**TC214**	TC215 = MSB		X		
		DD	**TC213**	TC20 = LSB		X		
		DC	**TC212**			X		
		DB	**TC211**			X		
		DA	**TC210**			X		
		D9	**TC29**			X		
		D8	**TC28**			X		
		D7	**TC27**			X		
		D6	**TC26**			X		
		D5	**TC25**			X		
		D4	**TC24**			X		
		D3	**TC23**			X		
		D2	**TC22**			X		
		D1	**TC21**			X		
		D0	**TC20**			X		
16-bit timer 2 control register	**0048196 (B)**	D7	**–**	reserved	–	0	–	0 when being read.
		D6	**SELFM2**	16-bit timer 2 fine mode selection	1 Fine mode 0 Normal	0	R/W	
		D5	**SELCRB2**	16-bit timer 2 comparison buffer	1 Enabled 0 Disabled	0	R/W	
		D4	**OUTINV2**	16-bit timer 2 output inversion	1 Invert 0 Normal	0	R/W	
		D3	**CKSL2**	16-bit timer 2 input clock selection	1 External clock 0 Internal clock	0	R/W	
		D2	**PTM2**	16-bit timer 2 clock output control	1 On 0 Off	0	R/W	
		D1	**PRESET2**	16-bit timer 2 reset	1 Reset 0 Invalid	0	W	0 when being read.
		D0	**PRUN2**	16-bit timer 2 Run/Stop control	1 Run 0 Stop	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
16-bit timer 3 comparison register A	**0048198 (HW)**	DF	**CR3A15**	16-bit timer 3 comparison data A	0 to 65535	X	R/W	
		DE	**CR3A14**	CR3A15 = MSB		X		
		DD	**CR3A13**	CR3A0 = LSB		X		
		DC	**CR3A12**			X		
		DB	**CR3A11**			X		
		DA	**CR3A10**			X		
		D9	**CR3A9**			X		
		D8	**CR3A8**			X		
		D7	**CR3A7**			X		
		D6	**CR3A6**			X		
		D5	**CR3A5**			X		
		D4	**CR3A4**			X		
		D3	**CR3A3**			X		
		D2	**CR3A2**			X		
		D1	**CR3A1**			X		
		D0	**CR3A0**			X		
16-bit timer 3 comparison register B	**004819A (HW)**	DF	**CR3B15**	16-bit timer 3 comparison data B	0 to 65535	X	R/W	
		DE	**CR3B14**	CR3B15 = MSB		X		
		DD	**CR3B13**	CR3B0 = LSB		X		
		DC	**CR3B12**			X		
		DB	**CR3B11**			X		
		DA	**CR3B10**			X		
		D9	**CR3B9**			X		
		D8	**CR3B8**			X		
		D7	**CR3B7**			X		
		D6	**CR3B6**			X		
		D5	**CR3B5**			X		
		D4	**CR3B4**			X		
		D3	**CR3B3**			X		
		D2	**CR3B2**			X		
		D1	**CR3B1**			X		
		D0	**CR3B0**			X		
16-bit timer 3 counter data register	**004819C (HW)**	DF	**TC315**	16-bit timer 3 counter data	0 to 65535	X	R	
		DE	**TC314**	TC315 = MSB		X		
		DD	**TC313**	TC30 = LSB		X		
		DC	**TC312**			X		
		DB	**TC311**			X		
		DA	**TC310**			X		
		D9	**TC39**			X		
		D8	**TC38**			X		
		D7	**TC37**			X		
		D6	**TC36**			X		
		D5	**TC35**			X		
		D4	**TC34**			X		
		D3	**TC33**			X		
		D2	**TC32**			X		
		D1	**TC31**			X		
		D0	**TC30**			X		
16-bit timer 3 control register	**004819E (B)**	D7	**–**	reserved	–	0	–	0 when being read.
		D6	**SELFM3**	16-bit timer 3 fine mode selection	1 Fine mode / 0 Normal	0	R/W	
		D5	**SELCRB3**	16-bit timer 3 comparison buffer	1 Enabled / 0 Disabled	0	R/W	
		D4	**OUTINV3**	16-bit timer 3 output inversion	1 Invert / 0 Normal	0	R/W	
		D3	**CKSL3**	16-bit timer 3 input clock selection	1 External clock / 0 Internal clock	0	R/W	
		D2	**PTM3**	16-bit timer 3 clock output control	1 On / 0 Off	0	R/W	
		D1	**PRESET3**	16-bit timer 3 reset	1 Reset / 0 Invalid	0	W	0 when being read.
		D0	**PRUN3**	16-bit timer 3 Run/Stop control	1 Run / 0 Stop	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
16-bit timer 4 comparison register A	**00481A0 (HW)**	DF	**CR4A15**	16-bit timer 4 comparison data A	0 to 65535	X	R/W	
		DE	**CR4A14**	CR4A15 = MSB		X		
		DD	**CR4A13**	CR4A0 = LSB		X		
		DC	**CR4A12**			X		
		DB	**CR4A11**			X		
		DA	**CR4A10**			X		
		D9	**CR4A9**			X		
		D8	**CR4A8**			X		
		D7	**CR4A7**			X		
		D6	**CR4A6**			X		
		D5	**CR4A5**			X		
		D4	**CR4A4**			X		
		D3	**CR4A3**			X		
		D2	**CR4A2**			X		
		D1	**CR4A1**			X		
		D0	**CR4A0**			X		
16-bit timer 4 comparison register B	**00481A2 (HW)**	DF	**CR4B15**	16-bit timer 4 comparison data B	0 to 65535	X	R/W	
		DE	**CR4B14**	CR4B15 = MSB		X		
		DD	**CR4B13**	CR4B0 = LSB		X		
		DC	**CR4B12**			X		
		DB	**CR4B11**			X		
		DA	**CR4B10**			X		
		D9	**CR4B9**			X		
		D8	**CR4B8**			X		
		D7	**CR4B7**			X		
		D6	**CR4B6**			X		
		D5	**CR4B5**			X		
		D4	**CR4B4**			X		
		D3	**CR4B3**			X		
		D2	**CR4B2**			X		
		D1	**CR4B1**			X		
		D0	**CR4B0**			X		
16-bit timer 4 counter data register	**00481A4 (HW)**	DF	**TC415**	16-bit timer 4 counter data	0 to 65535	X	R	
		DE	**TC414**	TC415 = MSB		X		
		DD	**TC413**	TC40 = LSB		X		
		DC	**TC412**			X		
		DB	**TC411**			X		
		DA	**TC410**			X		
		D9	**TC49**			X		
		D8	**TC48**			X		
		D7	**TC47**			X		
		D6	**TC46**			X		
		D5	**TC45**			X		
		D4	**TC44**			X		
		D3	**TC43**			X		
		D2	**TC42**			X		
		D1	**TC41**			X		
		D0	**TC40**			X		
16-bit timer 4 control register	**00481A6 (B)**	D7	**–**	reserved	–	0	–	0 when being read.
		D6	**SELFM4**	16-bit timer 4 fine mode selection	1 Fine mode / 0 Normal	0	R/W	
		D5	**SELCRB4**	16-bit timer 4 comparison buffer	1 Enabled / 0 Disabled	0	R/W	
		D4	**OUTINV4**	16-bit timer 4 output inversion	1 Invert / 0 Normal	0	R/W	
		D3	**CKSL4**	16-bit timer 4 input clock selection	1 External clock / 0 Internal clock	0	R/W	
		D2	**PTM4**	16-bit timer 4 clock output control	1 On / 0 Off	0	R/W	
		D1	**PRESET4**	16-bit timer 4 reset	1 Reset / 0 Invalid	0	W	0 when being read.
		D0	**PRUN4**	16-bit timer 4 Run/Stop control	1 Run / 0 Stop	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
16-bit timer 5 comparison register A	**00481A8 (HW)**	DF	**CR5A15**	16-bit timer 5 comparison data A	0 to 65535	X	R/W	
		DE	**CR5A14**	CR5A15 = MSB		X		
		DD	**CR5A13**	CR5A0 = LSB		X		
		DC	**CR5A12**			X		
		DB	**CR5A11**			X		
		DA	**CR5A10**			X		
		D9	**CR5A9**			X		
		D8	**CR5A8**			X		
		D7	**CR5A7**			X		
		D6	**CR5A6**			X		
		D5	**CR5A5**			X		
		D4	**CR5A4**			X		
		D3	**CR5A3**			X		
		D2	**CR5A2**			X		
		D1	**CR5A1**			X		
		D0	**CR5A0**			X		
16-bit timer 5 comparison register B	**00481AA (HW)**	DF	**CR5B15**	16-bit timer 5 comparison data B	0 to 65535	X	R/W	
		DE	**CR5B14**	CR5B15 = MSB		X		
		DD	**CR5B13**	CR5B0 = LSB		X		
		DC	**CR5B12**			X		
		DB	**CR5B11**			X		
		DA	**CR5B10**			X		
		D9	**CR5B9**			X		
		D8	**CR5B8**			X		
		D7	**CR5B7**			X		
		D6	**CR5B6**			X		
		D5	**CR5B5**			X		
		D4	**CR5B4**			X		
		D3	**CR5B3**			X		
		D2	**CR5B2**			X		
		D1	**CR5B1**			X		
		D0	**CR5B0**			X		
16-bit timer 5 counter data register	**00481AC (HW)**	DF	**TC515**	16-bit timer 5 counter data	0 to 65535	X	R	
		DE	**TC514**	TC515 = MSB		X		
		DD	**TC513**	TC50 = LSB		X		
		DC	**TC512**			X		
		DB	**TC511**			X		
		DA	**TC510**			X		
		D9	**TC59**			X		
		D8	**TC58**			X		
		D7	**TC57**			X		
		D6	**TC56**			X		
		D5	**TC55**			X		
		D4	**TC54**			X		
		D3	**TC53**			X		
		D2	**TC52**			X		
		D1	**TC51**			X		
		D0	**TC50**			X		
16-bit timer 5 control register	**00481AE (B)**	D7	**–**	reserved	–	0	–	0 when being read.
		D6	**SELFM5**	16-bit timer 5 fine mode selection	1 Fine mode / 0 Normal	0	R/W	
		D5	**SELCRB5**	16-bit timer 5 comparison buffer	1 Enabled / 0 Disabled	0	R/W	
		D4	**OUTINV5**	16-bit timer 5 output inversion	1 Invert / 0 Normal	0	R/W	
		D3	**CKSL5**	16-bit timer 5 input clock selection	1 External clock / 0 Internal clock	0	R/W	
		D2	**PTM5**	16-bit timer 5 clock output control	1 On / 0 Off	0	R/W	
		D1	**PRESET5**	16-bit timer 5 reset	1 Reset / 0 Invalid	0	W	0 when being read.
		D0	**PRUN5**	16-bit timer 5 Run/Stop control	1 Run / 0 Stop	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
IDMA base address low-order register	**0048200 (HW)**	DF	**DBASEL15**	IDMA base address low-order 16 bits (Initial value: 0x0C003A0)		0	R/W	
		DE	**DBASEL14**			0		
		DD	**DBASEL13**			0		
		DC	**DBASEL12**			0		
		DB	**DBASEL11**			0		
		DA	**DBASEL10**			0		
		D9	**DBASEL9**			1		
		D8	**DBASEL8**			1		
		D7	**DBASEL7**			1		
		D6	**DBASEL6**			0		
		D5	**DBASEL5**			1		
		D4	**DBASEL4**			0		
		D3	**DBASEL3**			0		
		D2	**DBASEL2**			0		
		D1	**DBASEL1**			0		
		D0	**DBASEL0**			0		
IDMA base address high-order register	**0048202 (HW)**	DF–C	**–**	reserved	–	–	–	Undefined in read.
		DB	**DBASEH11**	IDMA base address high-order 12 bits (Initial value: 0x0C003A0)		0	R/W	
		DA	**DBASEH10**			0		
		D9	**DBASEH9**			0		
		D8	**DBASEH8**			0		
		D7	**DBASEH7**			1		
		D6	**DBASEH6**			1		
		D5	**DBASEH5**			0		
		D4	**DBASEH4**			0		
		D3	**DBASEH3**			0		
		D2	**DBASEH2**			0		
		D1	**DBASEH1**			0		
		D0	**DBASEH0**			0		
IDMA start register	**0048204 (B)**	D7	**DSTART**	IDMA start	1 IDMA start 0 Stop	0	R/W	
		D6–0	**DCHN**	IDMA channel number	0 to 127	0	R/W	
IDMA enable register	**0048205 (B)**	D7–1	**–**	reserved	–	–	–	
		D0	**IDMAEN**	IDMA enable	1 Enabled 0 Disabled	0	R/W	

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.0 transfer counter register	**0048220 (HW)**	DF	**TC0_L7**	Ch.0 transfer counter[7:0]		X	R/W	
		DE	**TC0_L6**	(block transfer mode)		X		
		DD	**TC0_L5**			X		
		DC	**TC0_L4**	Ch.0 transfer counter[15:8]		X		
		DB	**TC0_L3**	(single/successive transfer mode)		X		
		DA	**TC0_L2**			X		
		D9	**TC0_L1**			X		
		D8	**TC0_L0**			X		
		D7	**BLKLEN07**	Ch.0 block length		X	R/W	
		D6	**BLKLEN06**	(block transfer mode)		X		
		D5	**BLKLEN05**			X		
		D4	**BLKLEN04**	Ch.0 transfer counter[7:0]		X		
		D3	**BLKLEN03**	(single/successive transfer mode)		X		
		D2	**BLKLEN02**			X		
		D1	**BLKLEN01**			X		
		D0	**BLKLEN00**			X		
High-speed DMA Ch.0 control register Note: D) Dual address mode S) Single address mode	**0048222 (HW)**	DF	**DUALM0**	Ch.0 address mode selection	1 Dual addr 0 Single addr	0	R/W	
		DE	**D0DIR**	D) Invalid	–	–	–	
				S) Ch.0 transfer direction control	1 Memory WR 0 Memory RD	0	R/W	
		DD–8	**–**	reserved	–	–	–	Undefined in read.
		D7	**TC0_H7**	Ch.0 transfer counter[15:8]		X	R/W	
		D6	**TC0_H6**	(block transfer mode)		X		
		D5	**TC0_H5**			X		
		D4	**TC0_H4**	Ch.0 transfer counter[23:16]		X		
		D3	**TC0_H3**	(single/successive transfer mode)		X		
		D2	**TC0_H2**			X		
		D1	**TC0_H1**			X		
		D0	**TC0_H0**			X		
High-speed DMA Ch.0 low-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048224 (HW)**	DF	**S0ADRL15**	D) Ch.0 source address[15:0]		X	R/W	
		DE	**S0ADRL14**	S) Ch.0 memory address[15:0]		X		
		DD	**S0ADRL13**			X		
		DC	**S0ADRL12**			X		
		DB	**S0ADRL11**			X		
		DA	**S0ADRL10**			X		
		D9	**S0ADRL9**			X		
		A8	**S0ADRL8**			X		
		D7	**S0ADRL7**			X		
		D6	**S0ADRL6**			X		
		D5	**S0ADRL5**			X		
		D4	**S0ADRL4**			X		
		D3	**S0ADRL3**			X		
		D2	**S0ADRL2**			X		
		D1	**S0ADRL1**			X		
		D0	**S0ADRL0**			X		
High-speed DMA Ch.0 high-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048226 (HW)**	DF	**DINTEN0**	Ch.0 interrupt enable	1 Enabled 0 Disabled	0	R/W	
		DE	**DATSIZE0**	Ch.0 transfer data size	1 Half word 0 Byte	0	R/W	
		DD	**S0IN1**	D) Ch.0 source address control	S0IN[1:0] Inc/dec	0	R/W	
		DC	**S0IN0**	S) Ch.0 memory address control	1 1 Inc.(no init) 1 0 Inc.(init) 0 1 Dec.(no init) 0 0 Fixed	0		
		DB	**S0ADRH11**	D) Ch.0 source address[27:16]		X	R/W	
		DA	**S0ADRH10**	S) Ch.0 memory address[27:16]		X		
		D9	**S0ADRH9**			X		
		A8	**S0ADRH8**			X		
		D7	**S0ADRH7**			X		
		D6	**S0ADRH6**			X		
		D5	**S0ADRH5**			X		
		D4	**S0ADRH4**			X		
		D3	**S0ADRH3**			X		
		D2	**S0ADRH2**			X		
		D1	**S0ADRH1**			X		
		D0	**S0ADRH0**			X		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.0 low-order destination address set-up register Note: D) Dual address mode S) Single address mode	**0048228 (HW)**	DF	**D0ADRL15**	D) Ch.0 destination address[15:0]		X	R/W	
		DE	**D0ADRL14**	S) Invalid		X		
		DD	**D0ADRL13**			X		
		DC	**D0ADRL12**			X		
		DB	**D0ADRL11**			X		
		DA	**D0ADRL10**			X		
		D9	**D0ADRL9**			X		
		A8	**D0ADRL8**			X		
		D7	**D0ADRL7**			X		
		D6	**D0ADRL6**			X		
		D5	**D0ADRL5**			X		
		D4	**D0ADRL4**			X		
		D3	**D0ADRL3**			X		
		D2	**D0ADRL2**			X		
		D1	**D0ADRL1**			X		
		D0	**D0ADRL0**			X		
High-speed DMA Ch.0 high-order destination address set-up register Note: D) Dual address mode S) Single address mode	**004822A (HW)**	DF	**D0MOD1**	Ch.0 transfer mode	D0MOD[1:0] Mode 1 1 Invalid 1 0 Block 0 1 Successive 0 0 Single	0	R/W	
		DE	**D0MOD0**			0		
		DD	**D0IN1**	D) Ch.0 destination address control S) Invalid	D0IN[1:0] Inc/dec 1 1 Inc.(no init) 1 0 Inc.(init) 0 1 Dec.(no init) 0 0 Fixed	0	R/W	
		DC	**D0IN0**			0		
		DB	**D0ADRH11**	D) Ch.0 destination address[27:16] S) Invalid		X	R/W	
		DA	**D0ADRH10**			X		
		D9	**D0ADRH9**			X		
		A8	**D0ADRH8**			X		
		D7	**D0ADRH7**			X		
		D6	**D0ADRH6**			X		
		D5	**D0ADRH5**			X		
		D4	**D0ADRH4**			X		
		D3	**D0ADRH3**			X		
		D2	**D0ADRH2**			X		
		D1	**D0ADRH1**			X		
		D0	**D0ADRH0**			X		
High-speed DMA Ch.0 enable register	**004822C (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS0_EN**	Ch.0 enable	1 Enable 0 Disable	0	R/W	
High-speed DMA Ch.0 trigger flag register	**004822E (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS0_TF**	Ch.0 trigger flag clear (writing)	1 Clear 0 No operation	0	R/W	
				Ch.0 trigger flag status (reading)	1 Set 0 Cleared			

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.1 transfer counter register	**0048230 (HW)**	DF	**TC1_L7**	Ch.1 transfer counter[7:0]		X	R/W	
		DE	**TC1_L6**	(block transfer mode)		X		
		DD	**TC1_L5**			X		
		DC	**TC1_L4**	Ch.1 transfer counter[15:8]		X		
		DB	**TC1_L3**	(single/successive transfer mode)		X		
		DA	**TC1_L2**			X		
		D9	**TC1_L1**			X		
		D8	**TC1_L0**			X		
		D7	**BLKLEN17**	Ch.1 block length		X	R/W	
		D6	**BLKLEN16**	(block transfer mode)		X		
		D5	**BLKLEN15**			X		
		D4	**BLKLEN14**	Ch.1 transfer counter[7:0]		X		
		D3	**BLKLEN13**	(single/successive transfer mode)		X		
		D2	**BLKLEN12**			X		
		D1	**BLKLEN11**			X		
		D0	**BLKLEN10**			X		
High-speed DMA Ch.1 control register Note: D) Dual address mode S) Single address mode	**0048232 (HW)**	DF	**DUALM1**	Ch.1 address mode selection	1 Dual addr 0 Single addr	0	R/W	
		DE	**D1DIR**	D) Invalid	–	–	–	
				S) Ch.1 transfer direction control	1 Memory WR 0 Memory RD	0	R/W	
		DD–8	**–**	reserved	–	–	–	Undefined in read.
		D7	**TC1_H7**	Ch.1 transfer counter[15:8]		X	R/W	
		D6	**TC1_H6**	(block transfer mode)		X		
		D5	**TC1_H5**			X		
		D4	**TC1_H4**	Ch.1 transfer counter[23:16]		X		
		D3	**TC1_H3**	(single/successive transfer mode)		X		
		D2	**TC1_H2**			X		
		D1	**TC1_H1**			X		
		D0	**TC1_H0**			X		
High-speed DMA Ch.1 low-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048234 (HW)**	DF	**S1ADRL15**	D) Ch.1 source address[15:0]		X	R/W	
		DE	**S1ADRL14**	S) Ch.1 memory address[15:0]		X		
		DD	**S1ADRL13**			X		
		DC	**S1ADRL12**			X		
		DB	**S1ADRL11**			X		
		DA	**S1ADRL10**			X		
		D9	**S1ADRL9**			X		
		A8	**S1ADRL8**			X		
		D7	**S1ADRL7**			X		
		D6	**S1ADRL6**			X		
		D5	**S1ADRL5**			X		
		D4	**S1ADRL4**			X		
		D3	**S1ADRL3**			X		
		D2	**S1ADRL2**			X		
		D1	**S1ADRL1**			X		
		D0	**S1ADRL0**			X		
High-speed DMA Ch.1 high-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048236 (HW)**	DF	**DINTEN1**	Ch.1 interrupt enable	1 Enabled 0 Disabled	0	R/W	
		DE	**DATSIZE1**	Ch.1 transfer data size	1 Half word 0 Byte	0	R/W	
		DD	**S1IN1**	D) Ch.1 source address control	S1IN[1:0] Inc/dec	0	R/W	
		DC	**S1IN0**	S) Ch.1 memory address control	1 1 Inc.(no init)	0		
					1 0 Inc.(init)			
					0 1 Dec.(no init)			
					0 0 Fixed			
		DB	**S1ADRH11**	D) Ch.1 source address[27:16]		X	R/W	
		DA	**S1ADRH10**	S) Ch.1 memory address[27:16]		X		
		D9	**S1ADRH9**			X		
		A8	**S1ADRH8**			X		
		D7	**S1ADRH7**			X		
		D6	**S1ADRH6**			X		
		D5	**S1ADRH5**			X		
		D4	**S1ADRH4**			X		
		D3	**S1ADRH3**			X		
		D2	**S1ADRH2**			X		
		D1	**S1ADRH1**			X		
		D0	**S1ADRH0**			X		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.1 low-order destination address set-up register Note: D) Dual address mode S) Single address mode	**0048238 (HW)**	DF	**D1ADRL15**	D) Ch.1 destination address[15:0]		X	R/W	
		DE	**D1ADRL14**	S) Invalid		X		
		DD	**D1ADRL13**			X		
		DC	**D1ADRL12**			X		
		DB	**D1ADRL11**			X		
		DA	**D1ADRL10**			X		
		D9	**D1ADRL9**			X		
		A8	**D1ADRL8**			X		
		D7	**D1ADRL7**			X		
		D6	**D1ADRL6**			X		
		D5	**D1ADRL5**			X		
		D4	**D1ADRL4**			X		
		D3	**D1ADRL3**			X		
		D2	**D1ADRL2**			X		
		D1	**D1ADRL1**			X		
		D0	**D1ADRL0**			X		
High-speed DMA Ch.1 high-order destination address set-up register Note: D) Dual address mode S) Single address mode	**004823A (HW)**	DF	**D1MOD1**	Ch.1 transfer mode	D1MOD[1:0]: 1 1 Invalid; 1 0 Block; 0 1 Successive; 0 0 Single	0	R/W	
		DE	**D1MOD0**			0		
		DD	**D1IN1**	D) Ch.1 destination address control S) Invalid	D1IN[1:0]: 1 1 Inc.(no init); 1 0 Inc.(init); 0 1 Dec.(no init); 0 0 Fixed	0	R/W	
		DC	**D1IN0**			0		
		DB	**D1ADRH11**	D) Ch.1 destination address[27:16] S) Invalid		X	R/W	
		DA	**D1ADRH10**			X		
		D9	**D1ADRH9**			X		
		A8	**D1ADRH8**			X		
		D7	**D1ADRH7**			X		
		D6	**D1ADRH6**			X		
		D5	**D1ADRH5**			X		
		D4	**D1ADRH4**			X		
		D3	**D1ADRH3**			X		
		D2	**D1ADRH2**			X		
		D1	**D1ADRH1**			X		
		D0	**D1ADRH0**			X		
High-speed DMA Ch.1 enable register	**004823C (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS1_EN**	Ch.1 enable	1 Enable; 0 Disable	0	R/W	
High-speed DMA Ch.1 trigger flag register	**004823E (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS1_TF**	Ch.1 trigger flag clear (writing)	1 Clear; 0 No operation	0	R/W	
				Ch.1 trigger flag status (reading)	1 Set; 0 Cleared			

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.2 transfer counter register	**0048240 (HW)**	DF	**TC2_L7**	Ch.2 transfer counter[7:0]		X	R/W	
		DE	**TC2_L6**	(block transfer mode)		X		
		DD	**TC2_L5**			X		
		DC	**TC2_L4**	Ch.2 transfer counter[15:8]		X		
		DB	**TC2_L3**	(single/successive transfer mode)		X		
		DA	**TC2_L2**			X		
		D9	**TC2_L1**			X		
		D8	**TC2_L0**			X		
		D7	**BLKLEN27**	Ch.2 block length		X	R/W	
		D6	**BLKLEN26**	(block transfer mode)		X		
		D5	**BLKLEN25**			X		
		D4	**BLKLEN24**	Ch.2 transfer counter[7:0]		X		
		D3	**BLKLEN23**	(single/successive transfer mode)		X		
		D2	**BLKLEN22**			X		
		D1	**BLKLEN21**			X		
		D0	**BLKLEN20**			X		
High-speed DMA Ch.2 control register Note: D) Dual address mode S) Single address mode	**0048242 (HW)**	DF	**DUALM2**	Ch.2 address mode selection	1 Dual addr 0 Single addr	0	R/W	
		DE	**D2DIR**	D) Invalid	–	–	–	
				S) Ch.2 transfer direction control	1 Memory WR 0 Memory RD	0	R/W	
		DD–8	**–**	reserved	–	–	–	Undefined in read.
		D7	**TC2_H7**	Ch.2 transfer counter[15:8]		X	R/W	
		D6	**TC2_H6**	(block transfer mode)		X		
		D5	**TC2_H5**			X		
		D4	**TC2_H4**	Ch.2 transfer counter[23:16]		X		
		D3	**TC2_H3**	(single/successive transfer mode)		X		
		D2	**TC2_H2**			X		
		D1	**TC2_H1**			X		
		D0	**TC2_H0**			X		
High-speed DMA Ch.2 low-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048244 (HW)**	DF	**S2ADRL15**	D) Ch.2 source address[15:0]		X	R/W	
		DE	**S2ADRL14**	S) Ch.2 memory address[15:0]		X		
		DD	**S2ADRL13**			X		
		DC	**S2ADRL12**			X		
		DB	**S2ADRL11**			X		
		DA	**S2ADRL10**			X		
		D9	**S2ADRL9**			X		
		A8	**S2ADRL8**			X		
		D7	**S2ADRL7**			X		
		D6	**S2ADRL6**			X		
		D5	**S2ADRL5**			X		
		D4	**S2ADRL4**			X		
		D3	**S2ADRL3**			X		
		D2	**S2ADRL2**			X		
		D1	**S2ADRL1**			X		
		D0	**S2ADRL0**			X		
High-speed DMA Ch.2 high-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048246 (HW)**	DF	**DINTEN2**	Ch.2 interrupt enable	1 Enabled 0 Disabled	0	R/W	
		DE	**DATSIZE2**	Ch.2 transfer data size	1 Half word 0 Byte	0	R/W	
		DD	**S2IN1**	D) Ch.2 source address control	S2IN[1:0] Inc/dec	0	R/W	
		DC	**S2IN0**	S) Ch.2 memory address control	1 1 Inc.(no init) 1 0 Inc.(init) 0 1 Dec.(no init) 0 0 Fixed	0		
		DB	**S2ADRH11**	D) Ch.2 source address[27:16]		X	R/W	
		DA	**S2ADRH10**	S) Ch.2 memory address[27:16]		X		
		D9	**S2ADRH9**			X		
		A8	**S2ADRH8**			X		
		D7	**S2ADRH7**			X		
		D6	**S2ADRH6**			X		
		D5	**S2ADRH5**			X		
		D4	**S2ADRH4**			X		
		D3	**S2ADRH3**			X		
		D2	**S2ADRH2**			X		
		D1	**S2ADRH1**			X		
		D0	**S2ADRH0**			X		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.2 low-order destination address set-up register Note: D) Dual address mode S) Single address mode	**0048248 (HW)**	DF	**D2ADRL15**	D) Ch.2 destination address[15:0]		X	R/W	
		DE	**D2ADRL14**	S) Invalid		X		
		DD	**D2ADRL13**			X		
		DC	**D2ADRL12**			X		
		DB	**D2ADRL11**			X		
		DA	**D2ADRL10**			X		
		D9	**D2ADRL9**			X		
		A8	**D2ADRL8**			X		
		D7	**D2ADRL7**			X		
		D6	**D2ADRL6**			X		
		D5	**D2ADRL5**			X		
		D4	**D2ADRL4**			X		
		D3	**D2ADRL3**			X		
		D2	**D2ADRL2**			X		
		D1	**D2ADRL1**			X		
		D0	**D2ADRL0**			X		
High-speed DMA Ch.2 high-order destination address set-up register Note: D) Dual address mode S) Single address mode	**004824A (HW)**	DF	**D2MOD1**	Ch.2 transfer mode	D2MOD[1:0]: 1 1 Invalid; 1 0 Block; 0 1 Successive; 0 0 Single	0	R/W	
		DE	**D2MOD0**			0		
		DD	**D2IN1**	D) Ch.2 destination address control S) Invalid	D2IN[1:0]: 1 1 Inc.(no init); 1 0 Inc.(init); 0 1 Dec.(no init); 0 0 Fixed	0	R/W	
		DC	**D2IN0**			0		
		DB	**D2ADRH11**	D) Ch.2 destination address[27:16] S) Invalid		X	R/W	
		DA	**D2ADRH10**			X		
		D9	**D2ADRH9**			X		
		A8	**D2ADRH8**			X		
		D7	**D2ADRH7**			X		
		D6	**D2ADRH6**			X		
		D5	**D2ADRH5**			X		
		D4	**D2ADRH4**			X		
		D3	**D2ADRH3**			X		
		D2	**D2ADRH2**			X		
		D1	**D2ADRH1**			X		
		D0	**D2ADRH0**			X		
High-speed DMA Ch.2 enable register	**004824C (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS2_EN**	Ch.2 enable	1 Enable; 0 Disable	0	R/W	
High-speed DMA Ch.2 trigger flag register	**004824E (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS2_TF**	Ch.2 trigger flag clear (writing)	1 Clear; 0 No operation	0	R/W	
				Ch.2 trigger flag status (reading)	1 Set; 0 Cleared			

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.3 transfer counter register	**0048250 (HW)**	DF	**TC3_L7**	Ch.3 transfer counter[7:0]		X	R/W	
		DE	**TC3_L6**	(block transfer mode)		X		
		DD	**TC3_L5**			X		
		DC	**TC3_L4**	Ch.3 transfer counter[15:8]		X		
		DB	**TC3_L3**	(single/successive transfer mode)		X		
		DA	**TC3_L2**			X		
		D9	**TC3_L1**			X		
		D8	**TC3_L0**			X		
		D7	**BLKLEN37**	Ch.3 block length		X	R/W	
		D6	**BLKLEN36**	(block transfer mode)		X		
		D5	**BLKLEN35**			X		
		D4	**BLKLEN34**	Ch.3 transfer counter[7:0]		X		
		D3	**BLKLEN33**	(single/successive transfer mode)		X		
		D2	**BLKLEN32**			X		
		D1	**BLKLEN31**			X		
		D0	**BLKLEN30**			X		
High-speed DMA Ch.3 control register Note: D) Dual address mode S) Single address mode	**0048252 (HW)**	DF	**DUALM3**	Ch.3 address mode selection	1 Dual addr 0 Single addr	0	R/W	
		DE	**D3DIR**	D) Invalid	–	–	–	
				S) Ch.3 transfer direction control	1 Memory WR 0 Memory RD	0	R/W	
		DD–8	**–**	reserved	–	–	–	Undefined in read.
		D7	**TC3_H7**	Ch.3 transfer counter[15:8]		X	R/W	
		D6	**TC3_H6**	(block transfer mode)		X		
		D5	**TC3_H5**			X		
		D4	**TC3_H4**	Ch.3 transfer counter[23:16]		X		
		D3	**TC3_H3**	(single/successive transfer mode)		X		
		D2	**TC3_H2**			X		
		D1	**TC3_H1**			X		
		D0	**TC3_H0**			X		
High-speed DMA Ch.3 low-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048254 (HW)**	DF	**S3ADRL15**	D) Ch.3 source address[15:0]		X	R/W	
		DE	**S3ADRL14**	S) Ch.3 memory address[15:0]		X		
		DD	**S3ADRL13**			X		
		DC	**S3ADRL12**			X		
		DB	**S3ADRL11**			X		
		DA	**S3ADRL10**			X		
		D9	**S3ADRL9**			X		
		A8	**S3ADRL8**			X		
		D7	**S3ADRL7**			X		
		D6	**S3ADRL6**			X		
		D5	**S3ADRL5**			X		
		D4	**S3ADRL4**			X		
		D3	**S3ADRL3**			X		
		D2	**S3ADRL2**			X		
		D1	**S3ADRL1**			X		
		D0	**S3ADRL0**			X		
High-speed DMA Ch.3 high-order source address set-up register Note: D) Dual address mode S) Single address mode	**0048256 (HW)**	DF	**DINTEN3**	Ch.3 interrupt enable	1 Enabled 0 Disabled	0	R/W	
		DE	**DATSIZE3**	Ch.3 transfer data size	1 Half word 0 Byte	0	R/W	
		DD	**S3IN1**	D) Ch.3 source address control	S3IN[1:0] Inc/dec	0	R/W	
		DC	**S3IN0**	S) Ch.3 memory address control	1 1 Inc.(no init) 1 0 Inc.(init) 0 1 Dec.(no init) 0 0 Fixed	0		
		DB	**S3ADRH11**	D) Ch.3 source address[27:16]		X	R/W	
		DA	**S3ADRH10**	S) Ch.3 memory address[27:16]		X		
		D9	**S3ADRH9**			X		
		A8	**S3ADRH8**			X		
		D7	**S3ADRH7**			X		
		D6	**S3ADRH6**			X		
		D5	**S3ADRH5**			X		
		D4	**S3ADRH4**			X		
		D3	**S3ADRH3**			X		
		D2	**S3ADRH2**			X		
		D1	**S3ADRH1**			X		
		D0	**S3ADRH0**			X		

Register name	Address	Bit	Name	Function	Setting	Init.	R/W	Remarks
High-speed DMA Ch.3 low-order destination address set-up register Note: D) Dual address mode S) Single address mode	**0048258 (HW)**	DF	**D3ADRL15**	D) Ch.3 destination address[15:0]		X	R/W	
		DE	**D3ADRL14**	S) Invalid		X		
		DD	**D3ADRL13**			X		
		DC	**D3ADRL12**			X		
		DB	**D3ADRL11**			X		
		DA	**D3ADRL10**			X		
		D9	**D3ADRL9**			X		
		A8	**D3ADRL8**			X		
		D7	**D3ADRL7**			X		
		D6	**D3ADRL6**			X		
		D5	**D3ADRL5**			X		
		D4	**D3ADRL4**			X		
		D3	**D3ADRL3**			X		
		D2	**D3ADRL2**			X		
		D1	**D3ADRL1**			X		
		D0	**D3ADRL0**			X		
High-speed DMA Ch.3 high-order destination address set-up register Note: D) Dual address mode S) Single address mode	**004825A (HW)**	DF	**D3MOD1**	Ch.3 transfer mode	D3MOD[1:0]: 1 1 Invalid; 1 0 Block; 0 1 Successive; 0 0 Single	0	R/W	
		DE	**D3MOD0**			0		
		DD	**D3IN1**	D) Ch.3 destination address control S) Invalid	D3IN[1:0]: 1 1 Inc.(no init); 1 0 Inc.(init); 0 1 Dec.(no init); 0 0 Fixed	0	R/W	
		DC	**D3IN0**			0		
		DB	**D3ADRH11**	D) Ch.3 destination address[27:16] S) Invalid		X	R/W	
		DA	**D3ADRH10**			X		
		D9	**D3ADRH9**			X		
		A8	**D3ADRH8**			X		
		D7	**D3ADRH7**			X		
		D6	**D3ADRH6**			X		
		D5	**D3ADRH5**			X		
		D4	**D3ADRH4**			X		
		D3	**D3ADRH3**			X		
		D2	**D3ADRH2**			X		
		D1	**D3ADRH1**			X		
		D0	**D3ADRH0**			X		
High-speed DMA Ch.3 enable register	**004825C (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS3_EN**	Ch.3 enable	1 Enable; 0 Disable	0	R/W	
High-speed DMA Ch.3 trigger flag register	**004825E (HW)**	DF–1	**–**	reserved	–	–	–	Undefined in read.
		D0	**HS3_TF**	Ch.3 trigger flag clear (writing)	1 Clear; 0 No operation	0	R/W	
				Ch.3 trigger flag status (reading)	1 Set; 0 Cleared			

Register name	Address	Bit	Name	Setting	Init.	R/W	Remarks
SED1375 REG[00h] Revision code register	**039FFE0 (B)**	D7	Product Code Bit 5	SED1375 = "001001"	0	R	
		D6	Product Code Bit 4		0		
		D5	Product Code Bit 3		1		
		D4	Product Code Bit 2		0		
		D3	Product Code Bit 1		0		
		D2	Product Code Bit 0		1		
		D1	Revision Code Bit 1	Revision = "01"	0	R	
		D0	Revision Code Bit 0		1		
SED1375 REG[01h] Mode register 0	**039FFE1 (B)**	D7	TFT/STN	1 TFT/D-TFD 0 STN	0	R/W	
		D6	Dual/Single	1 Dual 0 Single	0	R/W	
		D5	Color/Mono	1 Color 0 Mono	0	R/W	
		D4	FP Line Polarity	1 Active high 0 Active low	0	R/W	
		D3	FP Flame Polarity	1 Active high 0 Active low	0	R/W	
		D2	Mask FPSHIFT	1 Masked 0 Not masked	0	R/W	
		D1	Data Width Bit 1	See SED1375 Hardware	0	R/W	
		D0	Data Width Bit 0	Functional Specification	0		
SED1375 REG[02h] Mode register 1	**039FFE2 (B)**	D7	Bit-Per-Pixel Bit 1	Bit[1:0] Bit-Per-Pixel	0	R/W	
		D6	Bit-Per-Pixel Bit 0	1 1 8 bpp	0		
				1 0 4 bpp			
				0 1 2 bpp			
				0 0 1 bpp			
		D5	High Performance	1 MClk=PClk 0 MClk=PClk/x	0	R/W	
		D4	Input Clock Divide (Clk / 2)	1 Clk/1 0 Clk/2	0	R/W	
		D3	Display Blank	1 Displayed 0 Blanked	0	R/W	
		D2	Frame Repeat	1 Repeated 0 Not repeated	0	R/W	
		D1	Hardware Video Invert Enable	1 Inverted 0 GPIO4	0	R/W	
		D0	Software Video Invert	1 Inverted 0 Normal	0	R/W	
SED1375 REG[03h] Mode register 2	**039FFE3 (B)**	D7–4	n/a	–	0	R/W	
		D3	LCDPWR Override	1 Inactive 0 Controlled	0	R/W	
		D2	Hardware Power Save Enable	1 Enabled 0 GPIO0	0	R/W	
		D1	Software Power Save Bit 1	Bit[1:0] Mode	0	R/W	
		D0	Software Power Save Bit 0	1 1 Normal operation	0		
				1 0 reserved			
				0 1 reserved			
				0 0 Power save mode			
SED1375 REG[04h] Horizontal panel size register	**039FFE4 (B)**	D7	n/a	–	0	R/W	
		D6	Horizontal Panel Size Bit 6	Value =	0	R/W	
		D5	Horizontal Panel Size Bit 5	(Horizontal panel resolution/8)	0		
		D4	Horizontal Panel Size Bit 4	- 1	0		
		D3	Horizontal Panel Size Bit 3		0		
		D2	Horizontal Panel Size Bit 2		0		
		D1	Horizontal Panel Size Bit 1		0		
		D0	Horizontal Panel Size Bit 0		0		
SED1375 REG[05h] Vertical panel size register (LSB)	**039FFE5 (B)**	D7	Vertical Panel Size Bit 7	Value =	0	R/W	
		D6	Vertical Panel Size Bit 6	Vertical panel resolution - 1	0		
		D5	Vertical Panel Size Bit 5		0		
		D4	Vertical Panel Size Bit 4		0		
		D3	Vertical Panel Size Bit 3		0		
		D2	Vertical Panel Size Bit 2		0		
		D1	Vertical Panel Size Bit 1		0		
		D0	Vertical Panel Size Bit 0		0		
SED1375 REG[06h] Vertical panel size register (MSB)	**039FFE6 (B)**	D7–2	n/a		0	R/W	
		D1	Vertical Panel Size Bit 9	Value =	0	R/W	
		D0	Vertical Panel Size Bit 8	Vertical panel resolution - 1	0		
SED1375 REG[07h] FPLINE start position	**039FFE7 (B)**	D7–5	n/a	–	0	R/W	
		D4	FPLINE Start Position Bit 4	FPLINE start position (pixels)	0	R/W	
		D3	FPLINE Start Position Bit 3	= (REG[07h] + 2) x 8	0		
		D2	FPLINE Start Position Bit 2		0		
		D1	FPLINE Start Position Bit 1		0		
		D0	FPLINE Start Position Bit 0		0		
SED1375 REG[08h] Horizontal non-display period	**039FFE8 (B)**	D7–5	n/a	–	0	R/W	
		D4	Horizontal Non-Display Period Bit 4	Horizontal non-display period	0	R/W	
		D3	Horizontal Non-Display Period Bit 3	(pixels) = (REG[08h] + 4) x 8	0		
		D2	Horizontal Non-Display Period Bit 2		0		
		D1	Horizontal Non-Display Period Bit 1		0		
		D0	Horizontal Non-Display Period Bit 0		0		

Register name	Address	Bit	Name	Setting	Init.	R/W	Remarks
SED1375 REG[09h] FPFRAME start position	**039FFE9 (B)**	D7–6	n/a	–	0	R/W	
		D5	FPFRAME Start Position Bit 5	FPFRAME start position (lines) = REG[09h]	0	R/W	
		D4	FPFRAME Start Position Bit 4		0		
		D3	FPFRAME Start Position Bit 3		0		
		D2	FPFRAME Start Position Bit 2		0		
		D1	FPFRAME Start Position Bit 1		0		
		D0	FPFRAME Start Position Bit 0		0		
SED1375 REG[0Ah] Vertical non-display period	**039FFEA (B)**	D7	Vertical Non-Display Status	1 Non-display 0 Display	0	R	
		D6	n/a	–	0	R/W	
		D5	Vertical Non-Display Period Bit 5	Vertical non-display period (lines) = REG[0Ah] bits [5:0]	0	R/W	
		D4	Vertical Non-Display Period Bit 4		0		
		D3	Vertical Non-Display Period Bit 3		0		
		D2	Vertical Non-Display Period Bit 2		0		
		D1	Vertical Non-Display Period Bit 1		0		
		D0	Vertical Non-Display Period Bit 0		0		
SED1375 REG[0Bh] MOD rate register	**039FFEB (B)**	D7–6	n/a	–	0	R/W	
		D5	MOD Rate Bit 5		0	R/W	
		D4	MOD Rate Bit 4		0		
		D3	MOD Rate Bit 3		0		
		D2	MOD Rate Bit 2		0		
		D1	MOD Rate Bit 1		0		
		D0	MOD Rate Bit 0		0		
SED1375 REG[0Ch] Screen 1 start address register (LSB)	**039FFEC (B)**	D7	Screen 1 Start Address Bit 7		0	R/W	
		D6	Screen 1 Start Address Bit 6		0		
		D5	Screen 1 Start Address Bit 5		0		
		D4	Screen 1 Start Address Bit 4		0		
		D3	Screen 1 Start Address Bit 3		0		
		D2	Screen 1 Start Address Bit 2		0		
		D1	Screen 1 Start Address Bit 1		0		
		D0	Screen 1 Start Address Bit 0		0		
SED1375 REG[0Dh] Screen 1 start address register (MSB)	**039FFED (B)**	D7	Screen 1 Start Address Bit 15		0	R/W	
		D6	Screen 1 Start Address Bit 14		0		
		D5	Screen 1 Start Address Bit 13		0		
		D4	Screen 1 Start Address Bit 12		0		
		D3	Screen 1 Start Address Bit 11		0		
		D2	Screen 1 Start Address Bit 10		0		
		D1	Screen 1 Start Address Bit 9		0		
		D0	Screen 1 Start Address Bit 8		0		
SED1375 REG[0Eh] Screen 2 start address register (LSB)	**039FFEE (B)**	D7	Screen 2 Start Address Bit 7		0	R/W	
		D6	Screen 2 Start Address Bit 6		0		
		D5	Screen 2 Start Address Bit 5		0		
		D4	Screen 2 Start Address Bit 4		0		
		D3	Screen 2 Start Address Bit 3		0		
		D2	Screen 2 Start Address Bit 2		0		
		D1	Screen 2 Start Address Bit 1		0		
		D0	Screen 2 Start Address Bit 0		0		
SED1375 REG[0Fh] Screen 2 start address register (MSB)	**039FFEF (B)**	D7	Screen 2 Start Address Bit 15		0	R/W	
		D6	Screen 2 Start Address Bit 14		0		
		D5	Screen 2 Start Address Bit 13		0		
		D4	Screen 2 Start Address Bit 12		0		
		D3	Screen 2 Start Address Bit 11		0		
		D2	Screen 2 Start Address Bit 10		0		
		D1	Screen 2 Start Address Bit 9		0		
		D0	Screen 2 Start Address Bit 8		0		
SED1375 REG[10h] Screen 1 start address overflow register	**039FFF0 (B)**	D7–1	n/a	–	0	R/W	
		D0	Screen 1 Start Address Bit 16 (for Portrait mode only)		0	R/W	
SED1375 REG[11h] Memory address offset register	**039FFF1 (B)**	D7	Memory Address Offset Bit 7		0	R/W	
		D6	Memory Address Offset Bit 6		0		
		D5	Memory Address Offset Bit 5		0		
		D4	Memory Address Offset Bit 4		0		
		D3	Memory Address Offset Bit 3		0		
		D2	Memory Address Offset Bit 2		0		
		D1	Memory Address Offset Bit 1		0		
		D0	Memory Address Offset Bit 0		0		

Register name	Address	Bit	Name	Setting	Init.	R/W	Remarks
SED1375 REG[12h] Screen 1 vertical size register (LSB)	**039FFF2 (B)**	D7	Screen 1 Vertical Size Bit 7		0	R/W	
		D6	Screen 1 Vertical Size Bit 6		0		
		D5	Screen 1 Vertical Size Bit 5		0		
		D4	Screen 1 Vertical Size Bit 4		0		
		D3	Screen 1 Vertical Size Bit 3		0		
		D2	Screen 1 Vertical Size Bit 2		0		
		D1	Screen 1 Vertical Size Bit 1		0		
		D0	Screen 1 Vertical Size Bit 0		0		
SED1375 REG[13h] Screen 1 vertical size register (MSB)	**039FFF3 (B)**	D7–2	n/a		0	R/W	
		D1	Screen 1 Vertical Size Bit 9		0	R/W	
		D0	Screen 1 Vertical Size Bit 8		0		
SED1375 REG[15h] Look-up table address register	**039FFF5 (B)**	D7	LUT Address Bit 7		0	R/W	
		D6	LUT Address Bit 6		0		
		D5	LUT Address Bit 5		0		
		D4	LUT Address Bit 4		0		
		D3	LUT Address Bit 3		0		
		D2	LUT Address Bit 2		0		
		D1	LUT Address Bit 1		0		
		D0	LUT Address Bit 0		0		
SED1375 REG[17h] Look-up table data register	**039FFF7 (B)**	D7	LUT Data Bit 3		0	R/W	
		D6	LUT Data Bit 2		0		
		D5	LUT Data Bit 1		0		
		D4	LUT Data Bit 0		0		
		D3–0	n/a	–	0	R/W	
SED1375 REG[18h] GPIO configuration control register	**039FFF8 (B)**	D7–5	n/a	–	0	R/W	
		D4	GPIO4 Pin IO Configuration	1 Output 0 Input	0	R/W	
		D3	GPIO3 Pin IO Configuration	1 Output 0 Input	0	R/W	
		D2	GPIO2 Pin IO Configuration	1 Output 0 Input	0	R/W	
		D1	GPIO1 Pin IO Configuration	1 Output 0 Input	0	R/W	
		D0	GPIO0 Pin IO Configuration	1 Output 0 Input	0	R/W	
SED1375 REG[19h] GPIO status/control register	**039FFF9 (B)**	D7–5	n/a	–	0	R/W	
		D4	GPIO4 Pin IO Status	1 1 0 0	0	R/W	
		D3	GPIO3 Pin IO Status	1 1 0 0	0	R/W	
		D2	GPIO2 Pin IO Status	1 1 0 0	0	R/W	
		D1	GPIO1 Pin IO Status	1 1 0 0	0	R/W	
		D0	GPIO0 Pin IO Status	1 1 0 0	0	R/W	
SED1375 REG[1Ah] Scratch pad register	**039FFFA (B)**	D7	Scratch Bit 7	1 1 0 0	0	R/W	
		D6	Scratch Bit 6		0	R/W	
		D5	Scratch Bit 5		0	R/W	
		D4	Scratch Bit 4		0	R/W	
		D3	Scratch Bit 3		0	R/W	
		D2	Scratch Bit 2		0	R/W	
		D1	Scratch Bit 1		0	R/W	
		D0	Scratch Bit 0		0	R/W	
SED1375 REG[1Bh] Portrait mode register	**039FFFB (B)**	D7	Portrait Mode Enable	1 Portrait 0 Landscape	0	R/W	
		D6	Portrait Mode Select	1 Alternate 0 Default	0	R/W	
		D5–3	n/a	–	0	R/W	
		D2	reserved	Fix at 0	0	R/W	
		D1	Portrait Mode Pixel Clock Select Bit 1	See SED1375 Hardware	0	R/W	
		D0	Portrait Mode Pixel Clock Select Bit 0	Functional Specification	0	R/W	
SED1375 REG[1Ch] Line byte count register for portrait mode	**039FFFC (B)**	D7	Line Byte Count Bit 7		0	R/W	
		D6	Line Byte Count Bit 6		0		
		D5	Line Byte Count Bit 5		0		
		D4	Line Byte Count Bit 4		0		
		D3	Line Byte Count Bit 3		0		
		D2	Line Byte Count Bit 2		0		
		D1	Line Byte Count Bit 1		0		
		D0	Line Byte Count Bit 0		0		

4.3 SED1375 LCD Controller Block

The E0C332L01 contains the SED1375 LCD controller block.
This section describes the contents differ from the original SED1375 chip, and notes on usage.
For the SED1375 registers and control method, refer to "SED1375 Hardware Functional Specification".

Address mapping

The SED1375 block is allocated to Area 6.
SED1375 registers: 0x39FFE0 to 0x39FFFF
VRAM (40KB): 0x380000 to 0x389FFF

The base address of the registers and display buffer described in "SED1375 Hardware Functional Specification" is 0x380000.

SED1375 host interface

The SED1375 block in the E0C332L01 has no host bus interface pins and the CNF[2:0] pins that are used to select an interface type, since the interface configuration is fixed in the IC.

Clock input

The SED1375 chip can use only one source clock input to CLKI pin, while the E0C332L01 allows selection of the clock source including the internal clock. Use the CKSEL[2:0] pins for this selection.

Table 4.3.1 Selecting Clock

CKSEL2	CKSEL1	CKSEL0	Source clock for SED1375
0	0	0	PLL output clock
0	0	1	OSC3 oscillation clock
0	1	0	OSC3 oscillation clock × 1/2
0	1	1	OSC3 oscillation clock × 1/3
1	0	0	OSC3 oscillation clock × 1/4
1	0	1	External clock input to the CLKI pin
1	1	0	SED1375 disable mode
1	1	1	reserved

When an internal clock (OSC3 oscillation clock or PLL output clock) is selected as the SED1375 source clock or when SED1375 disable mode is selected, the CLKI pin must be fixed at high or low level.

Setting bus condition

The SED1375 registers and VRAM are accessed via the BCU in the C33 core block. The SED1375 block is interfaced with the BCU by the bus cycle control using the #WAIT signal (output from the SED1375 block). Therefore, set up the BCU registers as follows:

1) Areas 6–4 set-up register (0x4812A)
- Area 6 output disable delay time = 0.5 cycles (A6DF[1:0]/D[D:C] = 0b00)
- Area 6 wait control = 1 wait cycle (A6WT[2:0]/D[A:8] = 0b001)

2) Bus control register (0x4812E)
- External interface method selection = A0 (SBUSST/D3 = 0)
- Enable #WAIT signal input. (SWAITE/D0 = 1)

3) Access control register (0x48132)
- Area 6 internal access (A6IO/D9 = 1)

4) BCLK select register (0x4813A)
- Select BCU_CLK or a 33 MHz or less (if PLL_CLK, OSC3_CLK or CPU_CLK is selected). (BCLKSEL[1:0]/D[1:0])

SED1375 disable mode

When the SED1375 is disabled by setting the CKSEL[2:0] pins to "110", the VRAM is disconnected from the SED1375 but remains connected to the E0C332L01 bus. This allows use of the VRAM as a general-purpose RAM.
The SED1375 enters Power Save Mode by this setting.

When using the VRAM as a general-purpose RAM, set the number of wait cycles for accessing as follows:
1) When the core voltage is 3.3 V ± 0.3 V and the bus clock frequency is lower than 20 MHz: No wait
2) When the core voltage is 3.3 V ± 0.3 V and the bus clock frequency is 20 MHz or higher: 1 wait
3) When the core voltage is 3.0 V ± 0.3 V: 1 wait (bus clock frequency: 33 MHz max.)
4) When the core voltage is 2.0 V ± 0.2 V: 1 wait (bus clock frequency: 20 MHz max.)

The number of wait cycles can be set using the "Area 6 wait control" bit (A6WT[2:0]/D[A:8]) in Areas 6–4 setup register (0x4812A).

Note when using the OSC3 clock

When an internal clock (PLL output or OSC3 clock) is selected as the SED1375 operating clock, be sure to perform the following procedure before stopping the OSC3 oscillation.
1)Set the SED1375 block in the Software Power Save Mode.
2)Wait for 128 frame cycles or more before stopping the OSC3 oscillation.

Even if the external clock (CLKI pin) is selected as the SED1375 operating clock, the same procedure is necessary before stopping the external clock.

5 Power-Down Control

This chapter describes the controls used to reduce power consumption of the device.

Points on power saving

The current consumption of the device varies greatly with the CPU's operation mode, the system clocks used, and the peripheral circuits operated.

Current consumption	low←					→high
CPU/BCU	SLEEP	HALT2	Operating	HALT2	HALT(basic)	Operating
System clock	–	OSC1	OSC1	OSC3	OSC3	OSC3
OSC3 oscillation circuit	OFF	OFF	OFF	ON	ON	ON
Prescaler/peripheral circuit	STOP					RUN
LCD controller	Power save mode					Normal operation mode

To reduce power consumption of the device, it is important that as many unnecessary circuits as possible be turned off. In particular, peripheral circuits operating at a fast-clock rate consume a large amount of current, so design the program so that these circuits are turned off whenever unnecessary.

Power-saving in standby modes

When CPU processing is unnecessary, such as when waiting for an interrupt from key entries or peripheral circuits, place the device in standby mode to reduce current consumption.

Standby mode	Method to enter the mode	Circuits/functions stopped
Basic HALT mode	Execute the halt instruction after setting HLT2OP (D3)/Clock option register (0x40190) to "0". When the #BUSREQ signal is asserted from an external bus master while SEPD (D1)/Bus control register (0x4812E) = "1".	CPU only
HALT2 mode	Execute the halt instruction after setting HLT2OP to "1".	CPU, BCU, bus clock, and DMA
SLEEP mode	Execute the slp instruction.	CPU, BCU, bus clock, DMA, high-speed (OSC3) oscillation circuit, prescaler, and peripheral circuits that use the prescaler output clocks

HLT2OP (D3)/Clock option register (0x40190) that is used to select a HALT mode is set to "0" (basic HALT mode) at initial reset.

Notes: • In systems in which DRAM is connected directly to the device, the refresh function is turned off during HALT2 and SLEEP modes.

• The standby mode is cleared by interrupt generation (except for the basic HALT mode, which is set using an external bus master). Therefore, before entering standby mode, set the related registers to allow an interrupt to be used to clear the standby mode to be generated.

The low-speed (OSC1) oscillation circuit and clock timer continue operating even during SLEEP mode. If they are unnecessary, these circuits can also be turned off.

Function	Control bit	"1"	"0"	Default
Low-speed (OSC1) oscillation ON/OFF control	SOSC1(D0)/ Power control register(0x40180)	ON	OFF	ON

Switching over the system clocks

Normally, the system is clocked by the high-speed (OSC3) oscillation clock. If high-speed operation is unnecessary, switch the system clock to the low-speed (OSC1) oscillation clock and turn off the high-speed (OSC3) oscillation circuit. This helps to reduce current consumption. However, if DRAM is connected directly to the device, note that the refresh function is also turned off.

Even during operation using the high-speed (OSC3) oscillation clock, power reduction can also be achieved through the use of a system clock derived from the OSC3 clock by dividing it (1/1, 1/2, 1/4, or 1/8).

Function	Control bit	"1"	"0"	Default
System clock switch over	CLKCHG(D2)/ Power control register(0x40180)	OSC3	OSC1	OSC3
High-speed (OSC3) oscillation ON/OFF control	SOSC3(D1)/ Power control register(0x40180)	ON	OFF	ON
System clock division ratio selection	CLKDT(D[7:6])/ Power control register(0x40180)	"11" = 1/8 "10" = 1/4 "01" = 1/2 "00" = 1/1		1/1

Turning off the prescaler and peripheral circuits

Current consumption can be reduced by turning off the peripheral circuits operating at high speed as much as possible. The circuits listed below are operated using a clock generated by the prescaler:

- 16-bit programmable timers 0 to 5 (watchdog timer)
- 8-bit programmable timers 0 to 3 (DRAM refresh, serial interface)
- A/D converter

If none of these circuits need to be used, turn off the prescaler. If some of these circuits need to be used, turn off all other unnecessary circuits and stop clock supply from the prescaler to those circuits.

Function	Control bit	"1"	"0"	Default
Prescaler ON/OFF	PSCON(D5)/Power control register(0x40180)	ON	OFF	ON
16-bit timer 0 clock control	P16TON0(D3)/16-bit timer 0 clock control register(0x40147)	ON	OFF	OFF
16-bit timer 0 Run/Stop	PRUN0(D0)/16-bit timer 0 control register(0x48186)	RUN	STOP	STOP
16-bit timer 1 clock control	P16TON1(D3)/16-bit timer 1 clock control register(0x40148)	ON	OFF	OFF
16-bit timer 1 Run/Stop	PRUN1(D0)/16-bit timer 1 control register(0x4818E)	RUN	STOP	STOP
16-bit timer 2 clock control	P16TON2(D3)/16-bit timer 2 clock control register(0x40149)	ON	OFF	OFF
16-bit timer 2 Run/Stop	PRUN2(D0)/16-bit timer 2 control register(0x48196)	RUN	STOP	STOP
16-bit timer 3 clock control	P16TON3(D3)/16-bit timer 3 clock control register(0x4014A)	ON	OFF	OFF
16-bit timer 3 Run/Stop	PRUN3(D0)/16-bit timer 3 control register(0x4819E)	RUN	STOP	STOP
16-bit timer 4 clock control	P16TON4(D3)/16-bit timer 4 clock control register(0x4014B)	ON	OFF	OFF
16-bit timer 4 Run/Stop	PRUN4(D0)/16-bit timer 4 control register(0x481A6)	RUN	STOP	STOP
16-bit timer 5 clock control	P16TON5(D3)/16-bit timer 5 clock control register(0x4014C)	ON	OFF	OFF
16-bit timer 5 Run/Stop	PRUN5(D0)/16-bit timer 5 control register(0x481AE)	RUN	STOP	STOP
8-bit timer 0 clock control	P8TON0(D3)/8-bit timer 0/1 clock control register(0x4014D)	ON	OFF	OFF
8-bit timer 0 Run/Stop	PTRUN0(D0)/8-bit timer 0 control register(0x40160)	RUN	STOP	STOP
8-bit timer 1 clock control	P8TON1(D7)/8-bit timer 0/1 clock control register(0x4014D)	ON	OFF	OFF
8-bit timer 1 Run/Stop	PTRUN1(D0)/8-bit timer 1 control register(0x40164)	RUN	STOP	STOP
8-bit timer 2 clock control	P8TON2(D3)/8-bit timer 2/3 clock control register(0x4014E)	ON	OFF	OFF
8-bit timer 2 Run/Stop	PTRUN2(D0)/8-bit timer 2 control register(0x40168)	RUN	STOP	STOP
8-bit timer 3 clock control	P8TON3(D7)/8-bit timer 2/3 clock control register(0x4014E)	ON	OFF	OFF
8-bit timer 3 Run/Stop	PTRUN3(D0)/8-bit timer 3 control register(0x4016C)	RUN	STOP	STOP
A/D converter clock control	PSONAD(D3)/A/D clock control register(0x4014F)	ON	OFF	OFF
A/D conversion enable	ADE(D2)/A/D enable register(0x40244)	RUN	STOP	STOP

The same clock source must be used for the prescaler operating clock and the CPU operating clock. Therefore, when operating the CPU in low-speed with the OSC1 clock, the prescaler input clock must be switched according to the CPU operating clock. In this case, in order to prevent a malfunction in the peripheral circuit, the prescaler should be turned off before switching the CPU operating clock. After the CPU operating clock has been switched, switch the prescaler operating clock and then turn the prescaler on.

Function	Control bit	"1"	"0"	Default
Prescaler operating clock switch over	PSCDT0 (D0)/Prescaler clock select register(0x40181)	OSC1	OSC3/ PLL	OSC3/ PLL

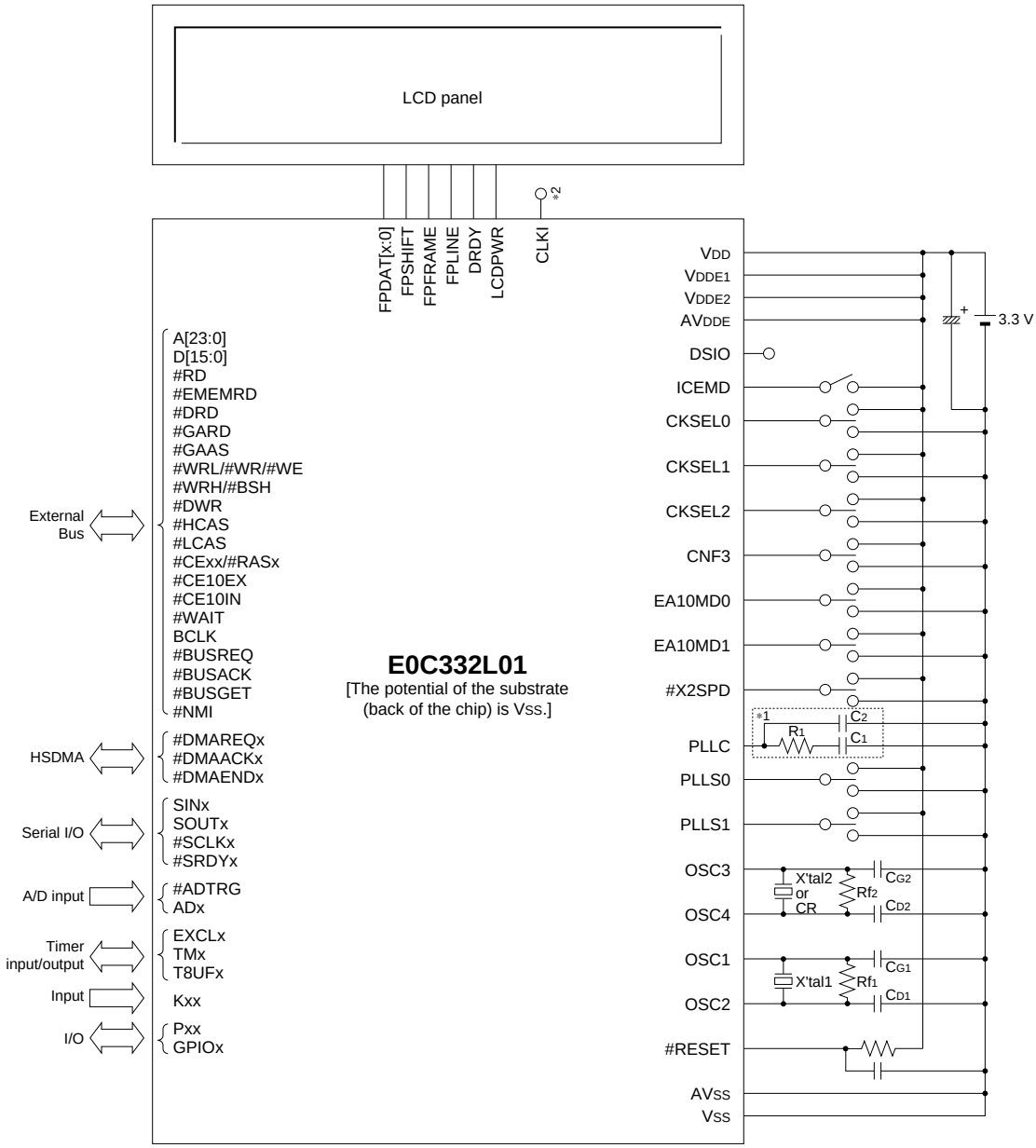
Power-down control of the LCD controller

The SED1375 provides the power save mode on its own. Since the software power save mode can be controlled by software, set the mode when turning the LCD display off.

Function	Control bit	"11"	"00"	Default
Software power save mode	REG[03h](0x39FFE3)•D[1:0]	Normal operation	Software power save mode	Software power save mode

Note: The software power save mode switches the LCD panel power control signal (LCDPWR) to the inactive state. This may cause damage of the LCD panel if the clock supply to the SED1375 is stopped at the same time.
Therefore, do not stop the clock supply for 128 frame cycles or more after setting the SED1375 to software power save mode.

6 Basic External Wiring Diagram



X'tal1	Crystal oscillator	32.768 kHz
C_{G1}	Gate capacitor	10 pF
C_{D1}	Drain capacitor	10 pF
Rf_1	Feedback resistor	10 MΩ
X'tal2	Crystal oscillator	33 MHz (Max.)
CR	Ceramic oscillator	33 MHz (Max.)
C_{G2}	Gate capacitor	10 pF
C_{D2}	Drain capacitor	10 pF
Rf_2	Feedback resistor	1 MΩ
R_1	Resistor	4.7 kΩ
C_1	Capacitor	100 pF
C_2	Capacitor	5 pF

Note: The above table is simply an example, and is not guaranteed to work.

∗1: When the PLL is not used, leave the PLLC pin open.

∗2: When a source clock other than CLKI pin input is selected for the SED1375, the CLKI pin must be fixed at high or low level.

7 Precautions on Mounting

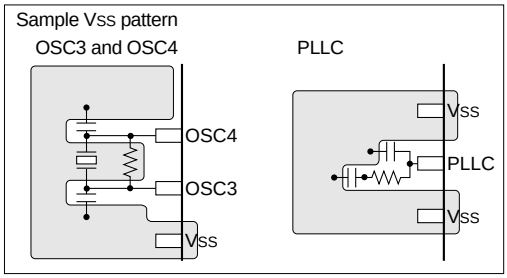
The following shows the precautions when designing the board and mounting the IC.

Oscillation Circuit

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC3 (OSC1), OSC4 (OSC2) and PLLC pins, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the figure below, make a VSS pattern as large as possible at circumscription of the OSC3 (OSC1) and OSC4 (OSC2) pins and the components connected to these pins. The same applies to the PLLC pin.
  Furthermore, do not use this VSS pattern to connect other components than the oscillation system.



  (3) When supplying an external clock to the OSC3 (OSC1) pin, the clock source should be connected to the OSC3 (OSC1) pin in the shortest line.
  Furthermore, do not connect anything else to the OSC4 (OSC2) pin.

- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC3 (OSC1) and VDD, please keep enough distance between OSC3 (OSC1) and VDD or other signals on the board pattern.

Reset Circuit

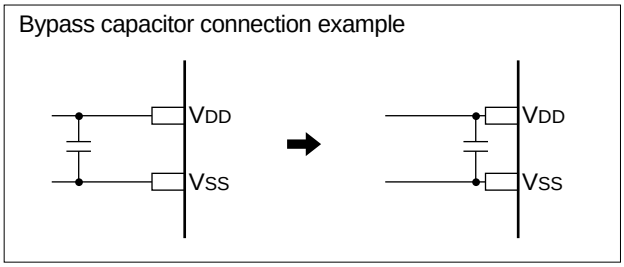
- The power-on reset signal which is input to the #RESET pin changes depending on conditions (power rise time, components used, board pattern, etc.). Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the #RESET pin in the shortest line.

Power Supply Circuit

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the VDD, VDDE1, VDDE2, VSS and AVDDE pins with patterns as short and large as possible.
  In particular, the power supply for AVDDE affects A/D conversion precision.

(2) When connecting between the VDD and VSS pins with a bypass capacitor, the pins should be connected as short as possible.

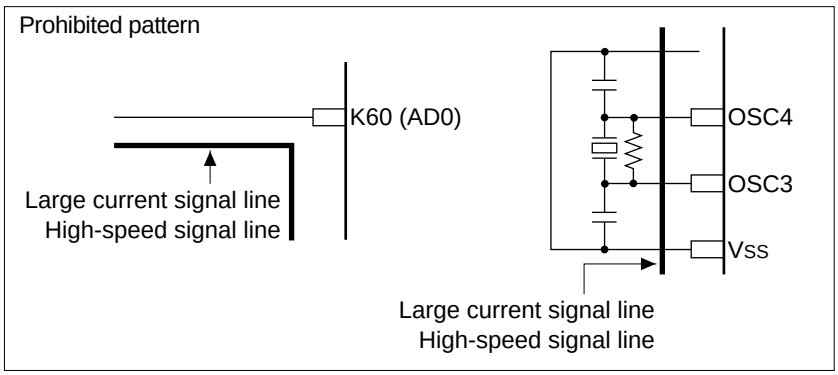


A/D Converter

- When the A/D converter is not used, the power supply pin AVDDE for the analog system should be connected to VDDE1.

Arrangement of Signal Lines

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit and analog input unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit and analog input unit.



8 Electrical Characteristics

8.1 Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Condition	Rated value	Unit	*
Supply voltage	V_{DD}		-0.3 to +4.0	V	
I/O power voltage	V_{DDE1}		-0.3 to +7.0	V	
LCD interface power voltage	V_{DDE2}		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DDE}+0.5	V	
High-level output current	I_{OH}	1 pin	-10	mA	
		Total of all pins	-40	mA	
Low-level output current	I_{OL}	1 pin	10	mA	
		Total of all pins	40	mA	
Analog power voltage	AV_{DDE}		-0.3 to +7.0	V	
Analog input voltage	AV_{IN}		-0.3 to AV_{DDE}+0.3	V	
Storage temperature	T_{STG}		-65 to +150	°C	

8.2 Recommended Operating Conditions

1) 3.3 V/5.0 V dual power source

(V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Supply voltage (high voltage)	V_{DDE1}		4.50	5.00	5.50	V	1
	V_{DDE2}		4.50	5.00	5.50	V	1
Supply voltage (low voltage)	V_{DD}		2.70	–	3.60	V	
Input voltage	HV_I		V_{SS}	–	V_{DDE}	V	
	LV_I		V_{SS}	–	V_{DD}	V	
CPU operating clock frequency	f_{CPU}		–	–	50	MHz	
Low-speed oscillation frequency	f_{OSC1}		–	32.768	–	kHz	
LCD controller operating clock frequency	f_{LCDC}		–	–	25	MHz	
Operating temperature	Ta		-40	25	85	°C	
Input rise time (normal input)	tri		–	–	50	ns	
Input fall time (normal input)	tfi		–	–	50	ns	
Input rise time (schmitt input)	tri		–	–	5	ms	
Input fall time (schmitt input)	tfi		–	–	5	ms	

* note 1) A low-voltage power source (3.3 V) can also be used for either V_{DDE1} or V_{DDE2}.

2) 3.3 V single power source

(V_{DDE1}=V_{DDE2}=V_{DD}, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Supply voltage	V_{DD}		2.70	–	3.60	V	
Input voltage	V_I		V_{SS}	–	V_{DD}	V	
CPU operating clock frequency	f_{CPU}		–	–	50	MHz	
Low-speed oscillation frequency	f_{OSC1}		–	32.768	–	kHz	
LCD controller operating clock frequency	f_{LCDC}		–	–	25	MHz	
Operating temperature	Ta		-40	25	85	°C	
Input rise time (normal input)	tri		–	–	50	ns	
Input fall time (normal input)	tfi		–	–	50	ns	
Input rise time (schmitt input)	tri		–	–	5	ms	
Input fall time (schmitt input)	tfi		–	–	5	ms	

3) 2.0 V single power source

(V_{DDE1}=V_{DDE2}=V_{DD}, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Supply voltage	V_{DD}		1.80	2.00	2.20	V	
Input voltage	V_I		V_{SS}	–	V_{DD}	V	
CPU operating clock frequency	f_{CPU}		–	–	20	MHz	
Low-speed oscillation frequency	f_{OSC1}		–	32.768	–	kHz	
LCD controller operating clock frequency	f_{LCDC}		–	–	10	MHz	
Operating temperature	Ta		-40	25	85	°C	
Input rise time (normal input)	tri		–	–	100	ns	
Input fall time (normal input)	tfi		–	–	100	ns	
Input rise time (schmitt input)	tri		–	–	10	ms	
Input fall time (schmitt input)	tfi		–	–	10	ms	

8.3 DC Characteristics

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Input leakage current	I_{LI}		-1	–	1	µA	
Off-state leakage current	I_{OZ}		-1	–	1	µA	
High-level output voltage	V_{OH}	I_{OH}=-3mA (Type1), I_{OH}=-12mA (Type3), V_{DDE}=Min.	V_{DDE} -0.4	–	–	V	
Low-level output voltage	V_{OL}	I_{OL}=3mA (Type1), I_{OL}=12mA (Type3), V_{DDE}=Min.	–	–	0.4	V	
High-level input voltage	V_{IH}	CMOS level, V_{DDE}=Max.	3.5	–	–	V	
Low-level input voltage	V_{IL}	CMOS level, V_{DDE}=Min.	–	–	1.0	V	
Positive trigger input voltage	V_{T+}	CMOS schmitt	2.0	–	4.0	V	
Negative trigger input voltage	V_{T-}	CMOS schmitt	0.8	–	3.1	V	
Hysteresis voltage	V_H	CMOS schmitt	0.3	–	–	V	
Pull-up resistor	R_{PU}	V_I=0V	60	120	288	kΩ	
Pull-down resistor	R_{PD}	V_I=V_{DDE} (#ICEMD)	30	60	144	kΩ	
Input pin capacitance	C_I	f=1MHz, V_{DDE}=0V	–	–	10	pF	
Output pin capacitance	C_O	f=1MHz, V_{DDE}=0V	–	–	10	pF	
I/O pin capacitance	C_{IO}	f=1MHz, V_{DDE}=0V	–	–	10	pF	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	*
Input leakage current	I_{LI}			-1	–	1	µA	
Off-state leakage current	I_{OZ}			-1	–	1	µA	
High-level output voltage	V_{OH}	I_{OH}=-2mA (Type1), I_{OH}=-6mA (Type2), I_{OH}=-12mA (Type3), V_{DD}=Min.		V_{DD} -0.4	–	–	V	
Low-level output voltage	V_{OL}	I_{OL}=2mA (Type1), I_{OL}=6mA (Type2), I_{OL}=12mA (Type3), V_{DD}=Min.		–	–	0.4	V	
High-level input voltage	V_{IH}	CMOS level, V_{DD}=Max.		2.4	–	–	V	
Low-level input voltage	V_{IL}	CMOS level, V_{DD}=Min.		–	–	0.4	V	
Positive trigger input voltage	V_{T+}	LVTTL schmitt		1.1	–	2.4	V	
Negative trigger input voltage	V_{T-}	LVTTL schmitt		0.6	–	1.8	V	
Hysteresis voltage	V_H	LVTTL schmitt		0.1	–	–	V	
Pull-up resistor	R_{PU}	V_I=0V	Other than DSIO	80	200	480	kΩ	
			DSIO	40	100	240	kΩ	
Pull-down resistor	R_{PD}	V_I=V_{DD} (#ICEMD)		40	100	240	kΩ	
Input pin capacitance	C_I	f=1MHz, V_{DD}=0V		–	–	10	pF	
Output pin capacitance	C_O	f=1MHz, V_{DD}=0V		–	–	10	pF	
I/O pin capacitance	C_{IO}	f=1MHz, V_{DD}=0V		–	–	10	pF	

Note: See Appendix B for pin characteristics.

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	*
Input leakage current	I_{LI}			-1	–	1	µA	
Off-state leakage current	I_{OZ}			-1	–	1	µA	
High-level output voltage	V_{OH}	I_{OH}=-0.6mA (Type1), I_{OH}=-2mA (Type2), I_{OH}=-4mA (Type3), V_{DD}=Min.		V_{DD} -0.2	–	–	V	
Low-level output voltage	V_{OL}	I_{OL}=0.6mA (Type1), I_{OL}=2mA (Type2), I_{OL}=4mA (Type3), V_{DD}=Min.		–	–	0.2	V	
High-level input voltage	V_{IH}	CMOS level, V_{DD}=Max.		1.6	–	–	V	
Low-level input voltage	V_{IL}	CMOS level, V_{DD}=Min.		–	–	0.3	V	
Positive trigger input voltage	V_{T+}	CMOS schmitt		0.4	–	1.6	V	
Negative trigger input voltage	V_{T-}	CMOS schmitt		0.3	–	1.4	V	
Hysteresis voltage	V_H	CMOS schmitt		0	–	–	V	
Pull-up resistor	R_{PU}	V_I=0V	Other than DSIO	120	480	1200	kΩ	
			DSIO	60	240	600	kΩ	
Pull-down resistor	R_{PD}	V_I=V_{DD} (#ICEMD)		60	240	600	kΩ	
Input pin capacitance	C_I	f=1MHz, V_{DD}=0V		–	–	10	pF	
Output pin capacitance	C_O	f=1MHz, V_{DD}=0V		–	–	10	pF	
I/O pin capacitance	C_{IO}	f=1MHz, V_{DD}=0V		–	–	10	pF	

Note: See Appendix B for pin characteristics.

8.4 Current Consumption

1) 3.3 V power source

(Unless otherwise specified: V_{DDE}=2.7V to 5.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	∗
Operating current	I_{DD1}	When CPU is operating	20MHz	–	25	35	mA	1
			33MHz	–	45	60		
			50MHz	–	60	75		
	I_{DD2}	HALT mode	20MHz	–	13	16	mA	2
			33MHz	–	23	30		
			50MHz	–	30	40		
	I_{DD3}	HALT2 mode	20MHz	–	3	5	mA	3
			33MHz	–	5	7		
			50MHz	–	7	9		
	I_{DD4}	SLEEP mode		–	1	30	µA	4
Clock timer operating current	I_{DDCT}	When clock timer only is operating OSC1 oscillation: 32kHz		–	7	–	µA	5

2) 2.0 V power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	∗
Operating current	I_{DD1}	When CPU is operating, 20MHz	–	12	17	mA	1
	I_{DD2}	HALT mode, 20MHz	–	7	10	mA	2
	I_{DD3}	HALT2 mode, 20MHz	–	1.5	2.0	mA	3
	I_{DD4}	SLEEP mode	–	1	30	µA	4
Clock timer operating current	I_{DDCT}	When clock timer only is operating OSC1 oscillation: 32kHz	–	1.5	–	µA	5

3) Analog power current

(Unless otherwise specified: V_{DD}=2.0V±0.2V, V_{DDE}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	∗
A/D converter operating current	AI_{DD1}	V_{DD}=3.6V, V_{DDE}=AV_{DD}=5.0V±0.5V	–	800	1400	µA	6
		V_{DD}=V_{DDE}=AV_{DD}=2.7V to 3.6V	–	500	800		

4) LCD controller operating curent

(Unless otherwise specified: V_{DDE}=2.7V to 5.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	∗
LCD controller operating current	LI_{DD1}	Display resolution = 640 × 480, 1bpp CLK = 25MHz	–	8.5	14	mA	7
	LI_{DD2}	Display resolution = 320 × 240, 1bpp CLK = 6.8MHz	–	2.2	3.5	mA	7
	LI_{DD3}	Display resolution = 320 × 240, 4bpp CLK = 6.8MHz	–	2.7	4.0	mA	7

Current consumption measurement condition: V_{IH}=V_{DD}, V_{IL}=0V, output pins are open, V_{DDE1}/V_{DDE2} current is not included

∗ note)

No.	OSC3	OSC1	CPU	Clock timer	Other peripheral circuits ∗2
1	On	Off	Normal operation ∗1	Stop	Stop
2	On	Off	HALT mode	Stop	Stop
3	On	Off	HALT2 mode	Stop	Stop
4	Off	Off	SLEEP mode	Stop	Stop
5	Off	On	HALT mode	Run	Stop
6	On	Off	HALT mode	Stop	A/D converter only operated, conversion clock frequency=2MHz

∗ note 7) This table shows the operating current values of the LCD controller block only. They may vary according to the display settings and the LCD controller input clock frequency.

∗1: The values of current consumption while the CPU is operating were measured when a test program that consists of 55% load instructions, 23% arithmetic operation instructions, 1% mac instruction, 12% branch instructions and 9% ext instruction is being executed in the built-in ROM continuously.

∗2: The LCD controller is included.

8.5 A/D Converter Characteristics

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=AV_{DD}=4.5V to 5.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C, ST[1:0]=11)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Resolution	–		–	10	–	bit	
Conversion time	–		5	–	–	µs	1
Zero scale error	E_{ZS}		0	2	4	LSB	
Full scale error	E_{FS}		-2	–	2	LSB	
Integral linearity error	E_L		-3	–	3	LSB	
Differential linearity error	E_D		-3	–	3	LSB	
Permissible signal source impedance	–		–	–	5	kΩ	
Analog input capacitance	–		–	–	45	pF	

* note 1) Indicates the minimum value when A/D clock = 4MHz (maximum clock frequency in 5V system).

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=AV_{DD}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C, ST[1:0]=11)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Resolution	–		–	10	–	bit	
Conversion time	–		10	–	–	µs	1
Zero scale error	E_{ZS}		0	2	4	LSB	
Full scale error	E_{FS}		-2	–	2	LSB	
Integral linearity error	E_L		-3	–	3	LSB	
Differential linearity error	E_D		-3	–	3	LSB	
Permissible signal source impedance	–		–	–	5	kΩ	
Analog input capacitance	–		–	–	45	pF	

* note 1) Indicates the minimum value when A/D clock = 2MHz (maximum clock frequency in 3V system).

Note: • Be sure to use as V_{DDE} = AV_{DD}.
• The A/D converter cannot be used when the E0C332L01 is used with a 2V power source.

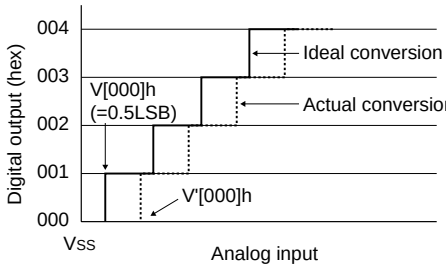
A/D conversion error

V[000]h = Ideal voltage at zero-scale point (=0.5LSB)
V'[000]h = Actual voltage at zero-scale point
V[3FF]h = Ideal voltage at full-scale point (=1022.5LSB)
V'[3FF]h = Actual voltage at full-scale point

$$1LSB = \frac{AV_{DD} - V_{SS}}{2^{10} - 1}$$

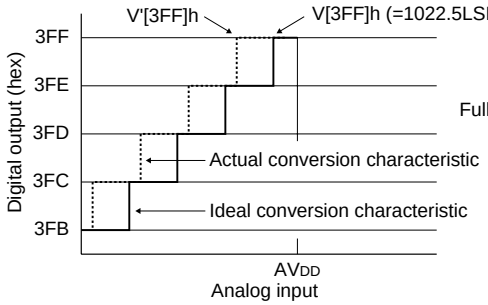
$$1LSB' = \frac{V'[3FF]h - V'[000]h}{2^{10} - 2}$$

■ **Zero scale error**



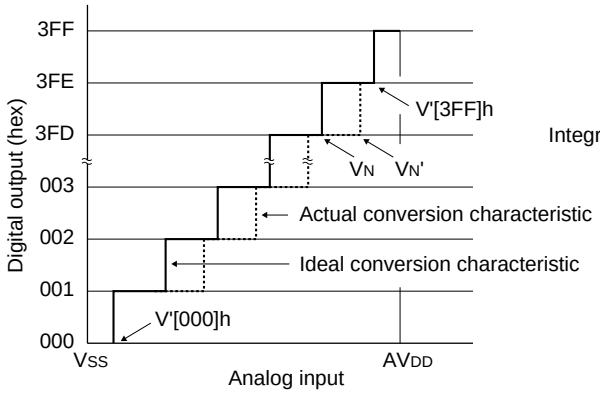
$$\text{Zero scale error } E_{ZS} = \frac{(V'[000]h - 0.5LSB') - (V[000]h - 0.5LSB)}{1LSB} \text{ [LSB]}$$

■ **Full scale error**



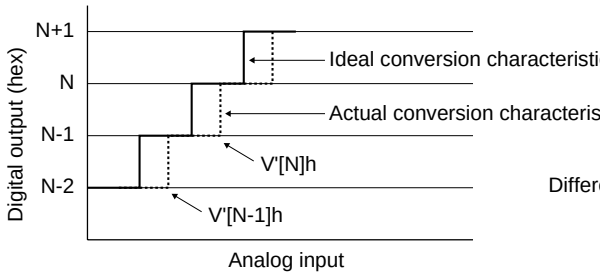
$$\text{Full scale error } E_{FS} = \frac{(V'[3FF]h + 0.5LSB') - (V[3FF]h + 0.5LSB)}{1LSB} \text{ [LSB]}$$

■ Integral linearity error



$$\text{Integral linearity error } E_L = \frac{V_N' - V_N}{1LSB'} \text{ [LSB]}$$

■ Differential linearity error



$$\text{Differential linearity error } E_D = \frac{V'[N]h - V'[N-1]h}{1LSB'} - 1 \text{ [LSB]}$$

8.6 AC Characteristics

8.6.1 Symbol Description

tCYC: Bus-clock cycle time

- In x1 mode, tCYC = 50 ns (20 MHz) when the CPU is operated with a 20-MHz clock
  tCYC = 30 ns (33 MHz) when the CPU is operated with a 33-MHz clock
- In x2 mode, tCYC = 50 ns (20 MHz) when the CPU is operated with a 40-MHz clock
  tCYC = 40 ns (25 MHz) when the CPU is operated with a 50-MHz clock
  tCYC = 33 ns (30 MHz) when the CPU is operated with a 60-MHz clock

WC: Number of wait cycles

Up to 7 cycles can be set for the number of cycles using the BCU control register. Furthermore, it can be extended to a desired number of cycles by setting the #WAIT pin from outside of the IC.

The minimum number of read cycles with no wait (0) inserted is 1 cycle.

The minimum number of write cycles with no wait cycle (0) inserted is 2 cycles. It does not change even if 1-wait cycle is set. The write cycle is actually extended when 2 or more wait cycles are set.

When inserting wait cycles by controlling the #WAIT pin from outside of the IC, pay attention to the timing of the #WAIT signal sampling. Read cycles are terminated at the cycle in which the #WAIT signal is negated. Write cycles are terminated at the following cycle after the #WAIT signal is negated.

C1, C2, C3, Cn: Cycle number

C1 indicates the first cycle when the BCU transfers data from/to an external memory or another device. Similarly, C2 and Cn indicate the second cycle and nth cycle, respectively.

Cw: Wait cycle

Indicates that the cycle is wait cycle inserted.

8.6.2 AC Characteristics Measurement Condition

Signal detection level:	Input signal	High level	$V_{IH} = V_{DDE} - 0.4$ V
		Low level	$V_{IL} = 0.4$ V
	Output signal	High level	$V_{OH} = 1/2\ V_{DDE}$
		Low level	$V_{OL} = 1/2\ V_{DDE}$
	The following applies when OSC3 is external clock input:		
	Input signal	High level	$V_{IH} = 1/2\ V_{DD}$
		Low level	$V_{IL} = 1/2\ V_{DD}$
Input signal waveform:	Rise time (10% → 90% V_{DD})		5 ns
	Fall time (90% → 10% V_{DD})		5 ns
Output load capacitance:	$C_L = 50$ pF		

8.6.3 C33 Block AC Characteristic Tables

External clock input characteristics

(Note) These AC characteristics apply to input signals from outside the IC.
The OSC3 input clock must be within V_{DD} to V_{SS} voltage range.

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
High-speed clock cycle time	t_{C3}	30		ns	
OSC3 clock input duty	t_{C3ED}	45	55	%	
OSC3 clock input rise time	t_{IF}		5	ns	
OSC3 clock input fall time	t_{IR}		5	ns	
BCLK high-level output delay time	t_{CD1}		35	ns	
BCLK low-level output delay time	t_{CD2}		35	ns	
Minimum reset pulse width	t_{RST}	6·t_{CYC}		ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
High-speed clock cycle time	t_{C3}	30		ns	
OSC3 clock input duty	t_{C3ED}	45	55	%	
OSC3 clock input rise time	t_{IF}		5	ns	
OSC3 clock input fall time	t_{IR}		5	ns	
BCLK high-level output delay time	t_{CD1}		35	ns	
BCLK low-level output delay time	t_{CD2}		35	ns	
Minimum reset pulse width	t_{RST}	6·t_{CYC}		ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
High-speed clock cycle time	t_{C3}	50		ns	
OSC3 clock input duty	t_{C3ED}	45	55	%	
OSC3 clock input rise time	t_{IF}		5	ns	
OSC3 clock input fall time	t_{IR}		5	ns	
BCLK high-level output delay time	t_{CD1}		60	ns	
BCLK low-level output delay time	t_{CD2}		60	ns	
Minimum reset pulse width	t_{RST}	6·t_{CYC}		ns	

BCLK clock output characteristics

(Note) These AC characteristic values are applied only when the high-speed oscillation circuit is used.

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
BCLK clock output duty	t_{CBD}	40	60	%	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
BCLK clock output duty	t_{CBD}	40	60	%	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
BCLK clock output duty	t_{CBD}	40	60	%	

Common characteristics

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	∗
Address delay time	t_{AD}	–	8	ns	1
#CEx delay time (1)	t_{CE1}	–	8	ns	
#CEx delay time (2)	t_{CE2}	–	8	ns	
Wait setup time	t_{WTS}	15	–	ns	
Wait hold time	t_{WTH}	0	–	ns	
Read signal delay time (1)	t_{RDD1}		8	ns	2
Read data setup time	t_{RDS}	12		ns	
Read data hold time	t_{RDH}	0		ns	
Write signal delay time (1)	t_{WRD1}		8	ns	3
Write data delay time (1)	t_{WDD1}		10	ns	
Write data delay time (2)	t_{WDD2}	0	10	ns	
Write data hold time	t_{WDH}	0		ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	∗
Address delay time	t_{AD}	–	10	ns	1
#CEx delay time (1)	t_{CE1}	–	10	ns	
#CEx delay time (2)	t_{CE2}	–	10	ns	
Wait setup time	t_{WTS}	15	–	ns	
Wait hold time	t_{WTH}	0	–	ns	
Read signal delay time (1)	t_{RDD1}		10	ns	2
Read data setup time	t_{RDS}	15		ns	
Read data hold time	t_{RDH}	0		ns	
Write signal delay time (1)	t_{WRD1}		10	ns	3
Write data delay time (1)	t_{WDD1}		10	ns	
Write data delay time (2)	t_{WDD2}	0	10	ns	
Write data hold time	t_{WDH}	0		ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	∗
Address delay time	t_{AD}	–	20	ns	1
#CEx delay time (1)	t_{CE1}	–	20	ns	
#CEx delay time (2)	t_{CE2}	–	20	ns	
Wait setup time	t_{WTS}	40	–	ns	
Wait hold time	t_{WTH}	0	–	ns	
Read signal delay time (1)	t_{RDD1}		20	ns	2
Read data setup time	t_{RDS}	40		ns	
Read data hold time	t_{RDH}	0		ns	
Write signal delay time (1)	t_{WRD1}		20	ns	3
Write data delay time (1)	t_{WDD1}		20	ns	
Write data delay time (2)	t_{WDD2}	0	20	ns	
Write data hold time	t_{WDH}	0		ns	

∗ note 1) This applies to the #BSH and #BSL timings.
2) This applies to the #GAAS and #GARD timings.
3) This applies to the #GAAS timing.

SRAM read cycle

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Read signal delay time (2)	t_{RDD2}		8	ns	
Read signal pulse width	t_{RDW}	t_{CYC}(0.5+WC)-8		ns	
Read address access time (1)	t_{ACC1}		t_{CYC}(1+WC)-20	ns	
Chip enable access time (1)	t_{CEAC1}		t_{CYC}(1+WC)-20	ns	
Read signal access time (1)	t_{RDAC1}		t_{CYC}(0.5+WC)-20	ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Read signal delay time (2)	t_{RDD2}		10	ns	
Read signal pulse width	t_{RDW}	t_{CYC}(0.5+WC)-10		ns	
Read address access time (1)	t_{ACC1}		t_{CYC}(1+WC)-25	ns	
Chip enable access time (1)	t_{CEAC1}		t_{CYC}(1+WC)-25	ns	
Read signal access time (1)	t_{RDAC1}		t_{CYC}(0.5+WC)-25	ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Read signal delay time (2)	t_{RDD2}		10	ns	
Read signal pulse width	t_{RDW}	t_{CYC}(0.5+WC)-10		ns	
Read address access time (1)	t_{ACC1}		t_{CYC}(1+WC)-60	ns	
Chip enable access time (1)	t_{CEAC1}		t_{CYC}(1+WC)-60	ns	
Read signal access time (1)	t_{RDAC1}		t_{CYC}(0.5+WC)-60	ns	

SRAM write cycle

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Write signal delay time (2)	t_{WRD2}		8	ns	
Write signal pulse width	t_{WRW}	t_{CYC}(1+WC)-10		ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Write signal delay time (2)	t_{WRD2}		10	ns	
Write signal pulse width	t_{WRW}	t_{CYC}(1+WC)-10		ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Write signal delay time (2)	t_{WRD2}		20	ns	
Write signal pulse width	t_{WRW}	t_{CYC}(1+WC)-20		ns	

DRAM access cycle common characteristics

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
#RAS signal delay time (1)	t_{RASD1}		10	ns	
#RAS signal delay time (2)	t_{RASD2}		10	ns	
#RAS signal pulse width	t_{RASW}	t_{CYC}(2+WC)-10		ns	
#CAS signal delay time (1)	t_{CASD1}		10	ns	
#CAS signal delay time (2)	t_{CASD2}		10	ns	
#CAS signal pulse width	t_{CASW}	t_{CYC}(0.5+WC)-5		ns	
Read signal delay time (3)	t_{RDD3}		10	ns	
Read signal pulse width (2)	t_{RDW2}	t_{CYC}(2+WC)-10		ns	
Write signal delay time (3)	t_{WRD3}		10	ns	
Write signal pulse width (2)	t_{WRW2}	t_{CYC}(2+WC)-10		ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
#RAS signal delay time (1)	t_{RASD1}		10	ns	
#RAS signal delay time (2)	t_{RASD2}		10	ns	
#RAS signal pulse width	t_{RASW}	t_{CYC}(2+WC)-10		ns	
#CAS signal delay time (1)	t_{CASD1}		10	ns	
#CAS signal delay time (2)	t_{CASD2}		10	ns	
#CAS signal pulse width	t_{CASW}	t_{CYC}(0.5+WC)-10		ns	
Read signal delay time (3)	t_{RDD3}		10	ns	
Read signal pulse width (2)	t_{RDW2}	t_{CYC}(2+WC)-10		ns	
Write signal delay time (3)	t_{WRD3}		10	ns	
Write signal pulse width (2)	t_{WRW2}	t_{CYC}(2+WC)-10		ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
#RAS signal delay time (1)	t_{RASD1}		20	ns	
#RAS signal delay time (2)	t_{RASD2}		20	ns	
#RAS signal pulse width	t_{RASW}	t_{CYC}(2+WC)-20		ns	
#CAS signal delay time (1)	t_{CASD1}		20	ns	
#CAS signal delay time (2)	t_{CASD2}		20	ns	
#CAS signal pulse width	t_{CASW}	t_{CYC}(0.5+WC)-20		ns	
Read signal delay time (3)	t_{RDD3}		20	ns	
Read signal pulse width (2)	t_{RDW2}	t_{CYC}(2+WC)-20		ns	
Write signal delay time (3)	t_{WRD3}		20	ns	
Write signal pulse width (2)	t_{WRW2}	t_{CYC}(2+WC)-20		ns	

DRAM random access cycle and DRAM fast-page cycle

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Column address access time	t_{ACCF}		t_{CYC}(1+WC)-25	ns	
#RAS access time	t_{RACF}		t_{CYC}(1.5+WC)-25	ns	
#CAS access time	t_{CACF}		t_{CYC}(0.5+WC)-25	ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Column address access time	t_{ACCF}		t_{CYC}(1+WC)-25	ns	
#RAS access time	t_{RACF}		t_{CYC}(1.5+WC)-25	ns	
#CAS access time	t_{CACF}		t_{CYC}(0.5+WC)-25	ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Column address access time	t_{ACCF}		t_{CYC}(1+WC)-60	ns	
#RAS access time	t_{RACF}		t_{CYC}(1.5+WC)-60	ns	
#CAS access time	t_{CACF}		t_{CYC}(0.5+WC)-60	ns	

EDO DRAM random access cycle and EDO DRAM page cycle

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Column address access time	t_{ACCE}		t_{CYC}(1.5+WC)-25	ns	
#RAS access time	t_{RACE}		t_{CYC}(2+WC)-25	ns	
#CAS access time	t_{CACE}		t_{CYC}(1+WC)-15	ns	
Read data setup time	t_{RDS2}	20		ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Column address access time	t_{ACCE}		t_{CYC}(1.5+WC)-25	ns	
#RAS access time	t_{RACE}		t_{CYC}(2+WC)-25	ns	
#CAS access time	t_{CACE}		t_{CYC}(1+WC)-20	ns	
Read data setup time	t_{RDS2}	20		ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Column address access time	t_{ACCE}		t_{CYC}(1.5+WC)-60	ns	
#RAS access time	t_{RACE}		t_{CYC}(2+WC)-60	ns	
#CAS access time	t_{CACE}		t_{CYC}(1+WC)-60	ns	
Read data setup time	t_{RDS2}	20		ns	

Burst ROM read cycle

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Read address access time (2)	t_{ACC2}		t_{CYC}(1+WC)-20	ns	
Chip enable access time (2)	t_{CEAC2}		t_{CYC}(1+WC)-20	ns	
Read signal access time (2)	t_{RDAC2}		t_{CYC}(0.5+WC)-20	ns	
Burst address access time	t_{ACCB}		t_{CYC}(1+WC)-20	ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Read address access time (2)	t_{ACC2}		t_{CYC}(1+WC)-25	ns	
Chip enable access time (2)	t_{CEAC2}		t_{CYC}(1+WC)-25	ns	
Read signal access time (2)	t_{RDAC2}		t_{CYC}(0.5+WC)-25	ns	
Burst address access time	t_{ACCB}		t_{CYC}(1+WC)-25	ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
Read address access time (2)	t_{ACC2}		t_{CYC}(1+WC)-60	ns	
Chip enable access time (2)	t_{CEAC2}		t_{CYC}(1+WC)-60	ns	
Read signal access time (2)	t_{RDAC2}		t_{CYC}(0.5+WC)-60	ns	
Burst address access time	t_{ACCB}		t_{CYC}(1+WC)-60	ns	

External bus master and NMI

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
#BUSREQ signal setup time	t_{BRQS}	15		ns	
#BUSREQ signal hold time	t_{BRQH}	0		ns	
#BUSACK signal output delay time	t_{BAKD}		10	ns	
High-impedance → output delay time	t_{Z2E}		10	ns	
Output → high-impedance delay time	t_{B2Z}		10	ns	
#NMI pulse width	t_{NMIW}	30		ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
#BUSREQ signal setup time	t_{BRQS}	15		ns	
#BUSREQ signal hold time	t_{BRQH}	0		ns	
#BUSACK signal output delay time	t_{BAKD}		10	ns	
High-impedance → output delay time	t_{Z2E}		10	ns	
Output → high-impedance delay time	t_{B2Z}		10	ns	
#NMI pulse width	t_{NMIW}	30		ns	

3) 2.0 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item	Symbol	Min.	Max.	Unit	*
#BUSREQ signal setup time	t_{BRQS}	40		ns	
#BUSREQ signal hold time	t_{BRQH}	0		ns	
#BUSACK signal output delay time	t_{BAKD}		20	ns	
High-impedance → output delay time	t_{Z2E}		20	ns	
Output → high-impedance delay time	t_{B2Z}		20	ns	
#NMI pulse width	t_{NMIW}	90		ns	

Input, Output and I/O port

1) 3.3 V/5.0 V dual power source

(Unless otherwise specified: V_{DDE}=5.0V±0.5V, V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item		Symbol	Min.	Max.	Unit	*
Input data setup time		t_{INPS}	20		ns	
Input data hold time		t_{INPH}	10		ns	
Output data delay time		t_{OUTD}		20	ns	
K-port interrupt input pulse width	SLEEP, HALT2 mode	t_{KINW}	30		ns	
	Others		2 × t_{CYC}		ns	

2) 3.3 V single power source

(Unless otherwise specified: V_{DDE}=V_{DD}=2.7V to 3.6V, V_{SS}=0V, Ta=-40°C to +85°C)

Item		Symbol	Min.	Max.	Unit	*
Input data setup time		t_{INPS}	20		ns	
Input data hold time		t_{INPH}	10		ns	
Output data delay time		t_{OUTD}		20	ns	
K-port interrupt input pulse width	SLEEP, HALT2 mode	t_{KINW}	30		ns	
	Others		2 × t_{CYC}		ns	

3) 2.0 V single power source

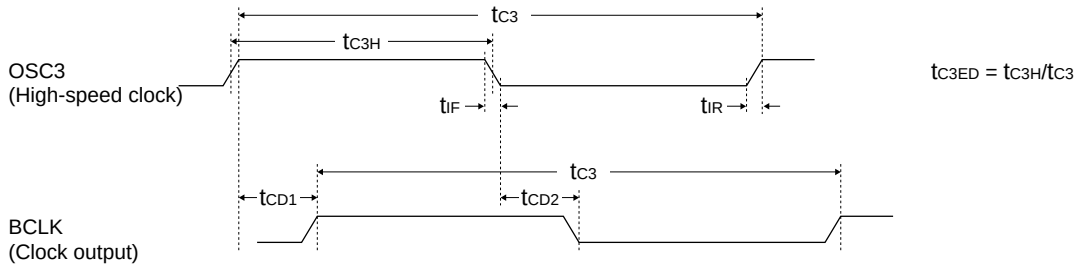
(Unless otherwise specified: V_{DDE}=V_{DD}=2.0V±0.2V, V_{SS}=0V, Ta=-40°C to +85°C)

Item		Symbol	Min.	Max.	Unit	*
Input data setup time		t_{INPS}	40		ns	
Input data hold time		t_{INPH}	20		ns	
Output data delay time		t_{OUTD}		30	ns	
K-port interrupt input pulse width	SLEEP, HALT2 mode	t_{KINW}	90		ns	
	Others		2 × t_{CYC}		ns	

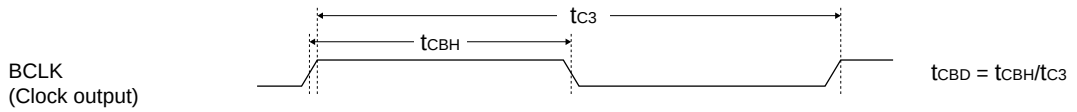
8.6.4 C33 Block AC Characteristic Timing Charts

Clock

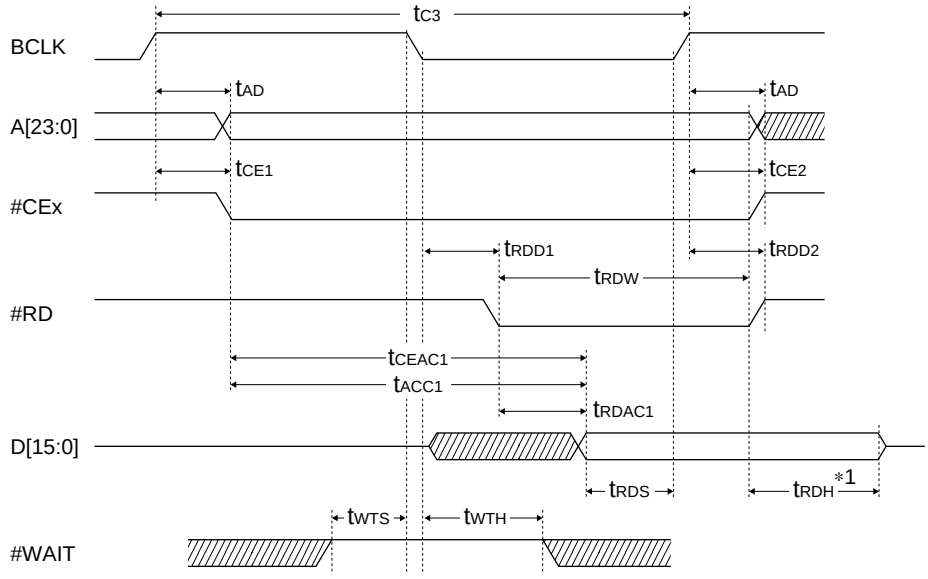
(1) When an external clock is input (in x1 speed mode):



(2) When the high-speed oscillation circuit is used for the operating clock:

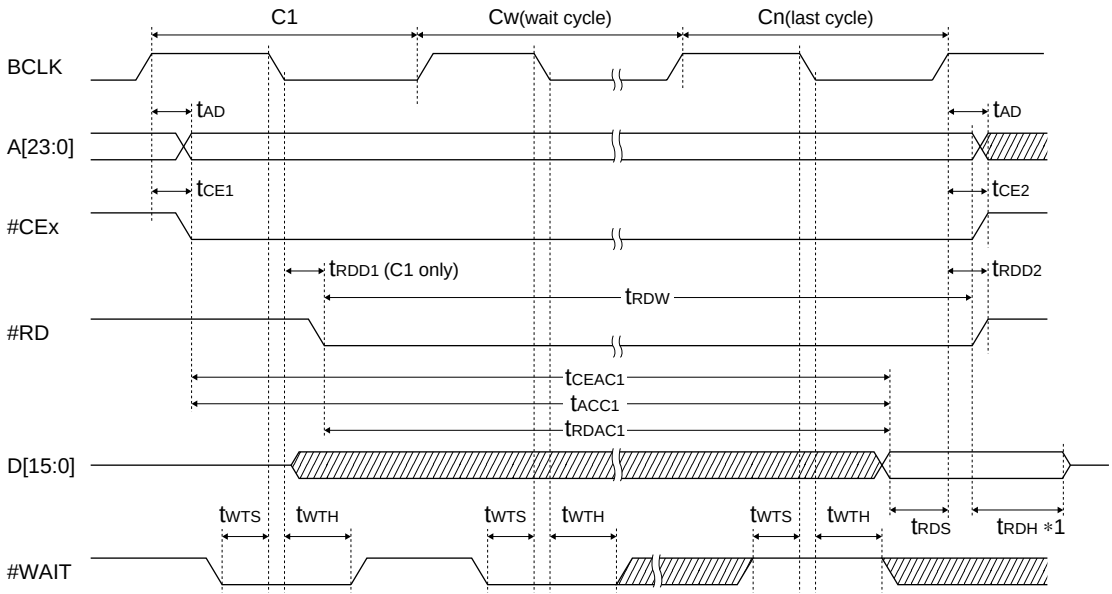


SRAM read cycle (basic cycle: 1 cycle)



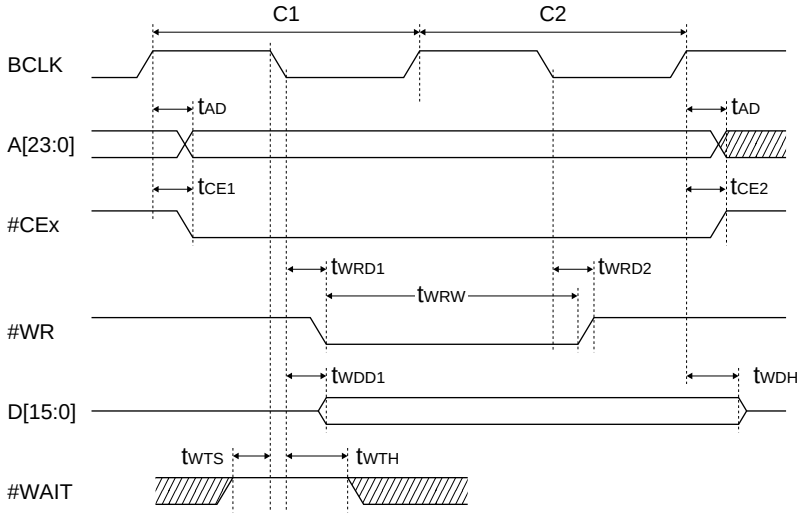
∗1 tRDH is measured with respect to the first signal change (negation) from among the #RD, #CEx and A[23:0] signals.

SRAM read cycle (when a wait cycle is inserted)

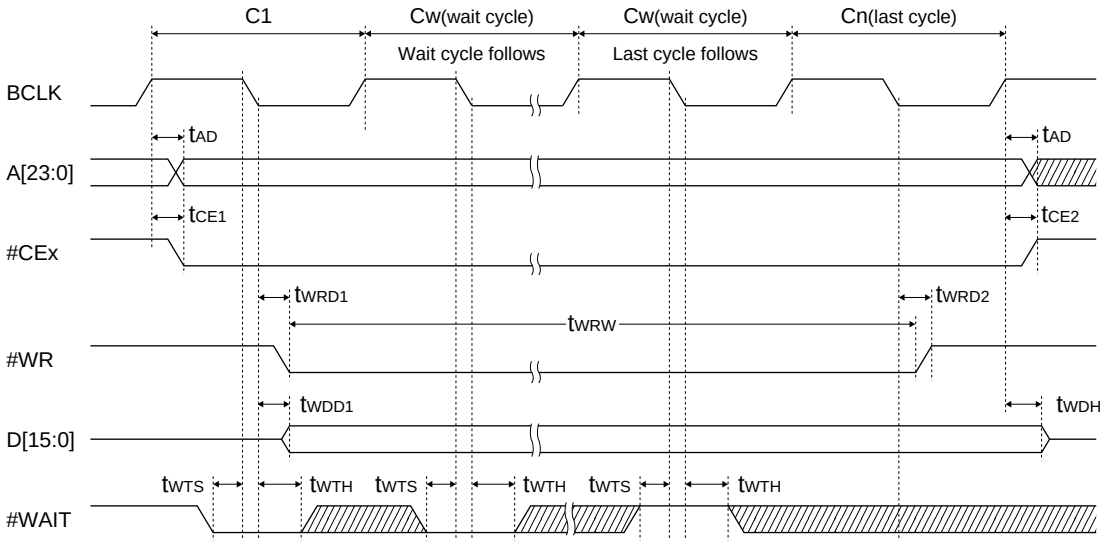


∗1 tRDH is measured with respect to the first signal change (negation) from among the #RD, #CEx and A[23:0] signals.

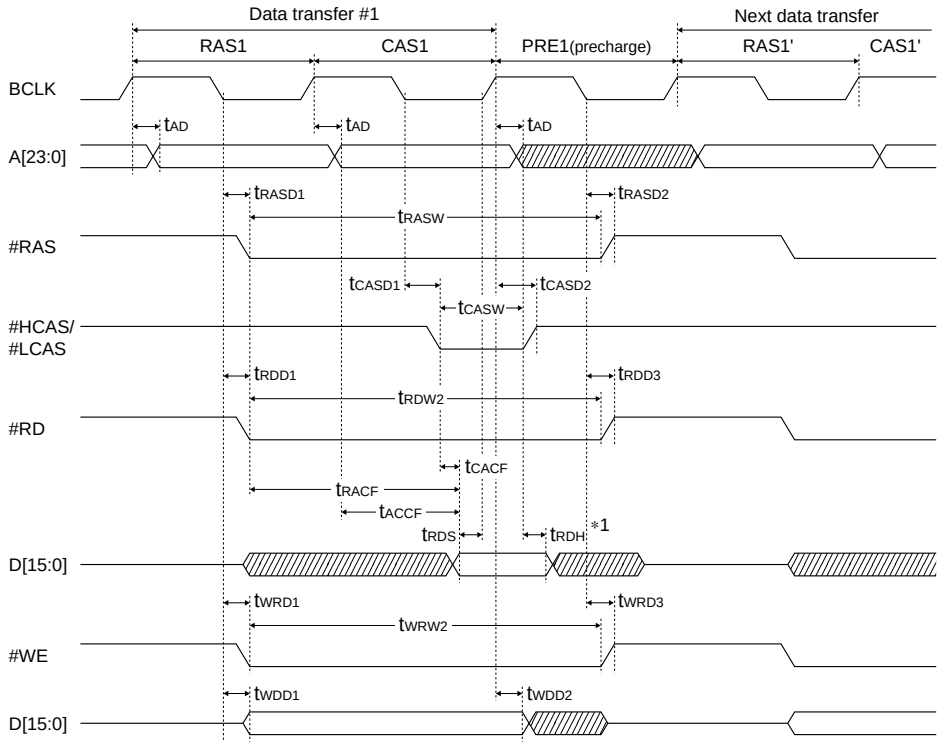
SRAM write cycle (basic cycle: 2 cycles)



SRAM write cycle (when wait cycles are inserted)

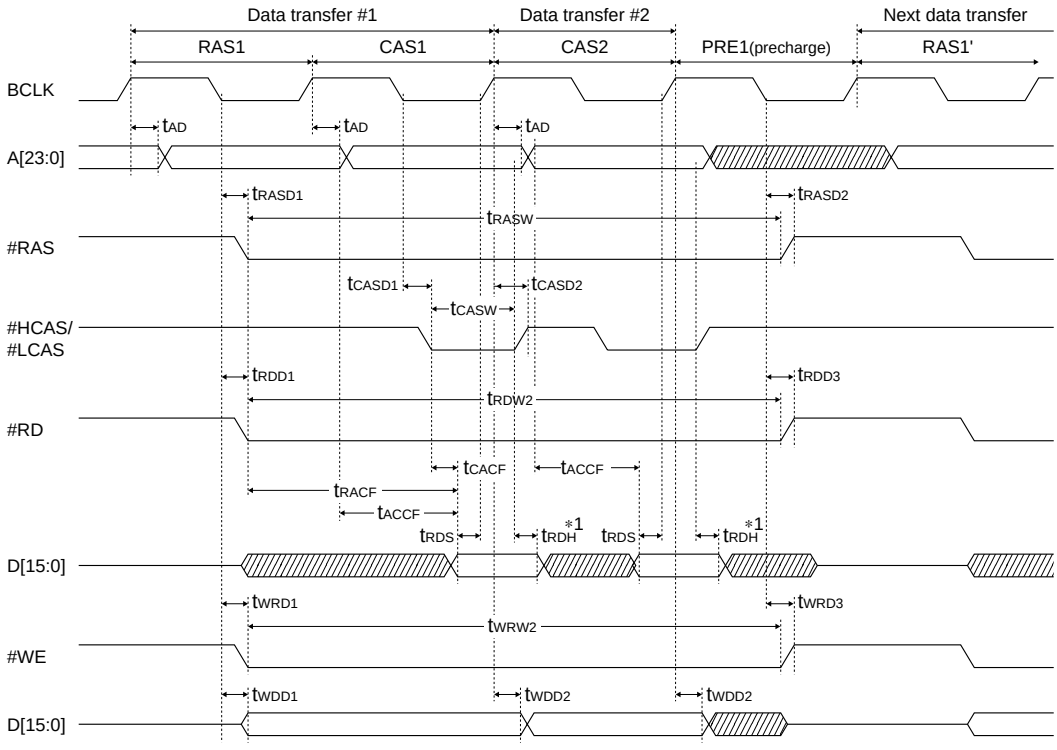


DRAM random access cycle (basic cycle)



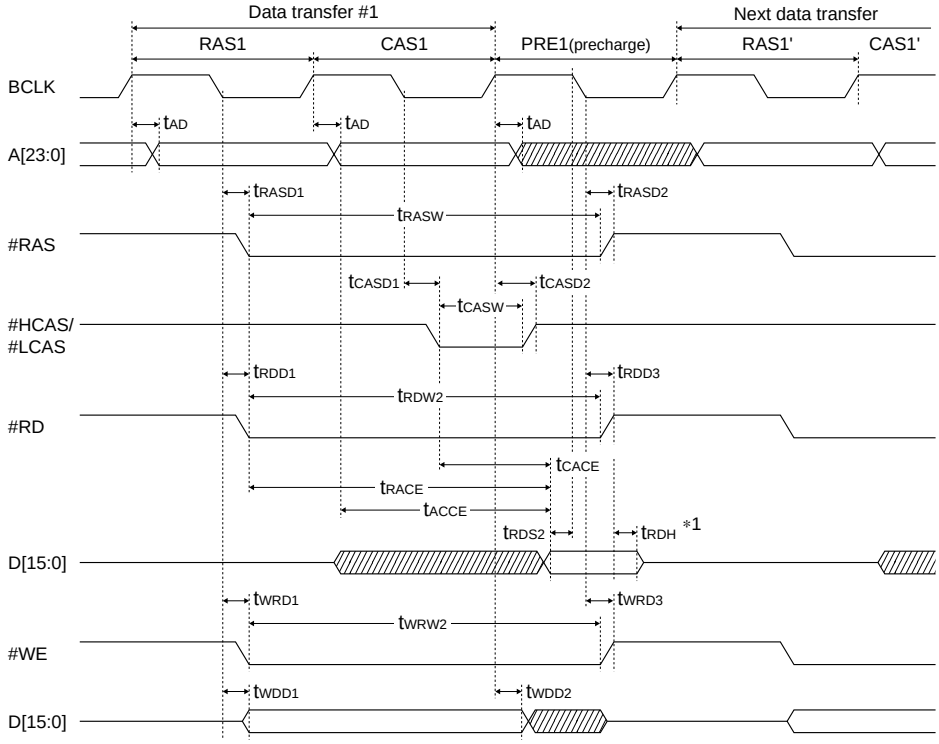
*1 tRDH is measured with respect to the first signal change (negation) of either the #RD or the A[23:0] signals.

DRAM fast-page access cycle



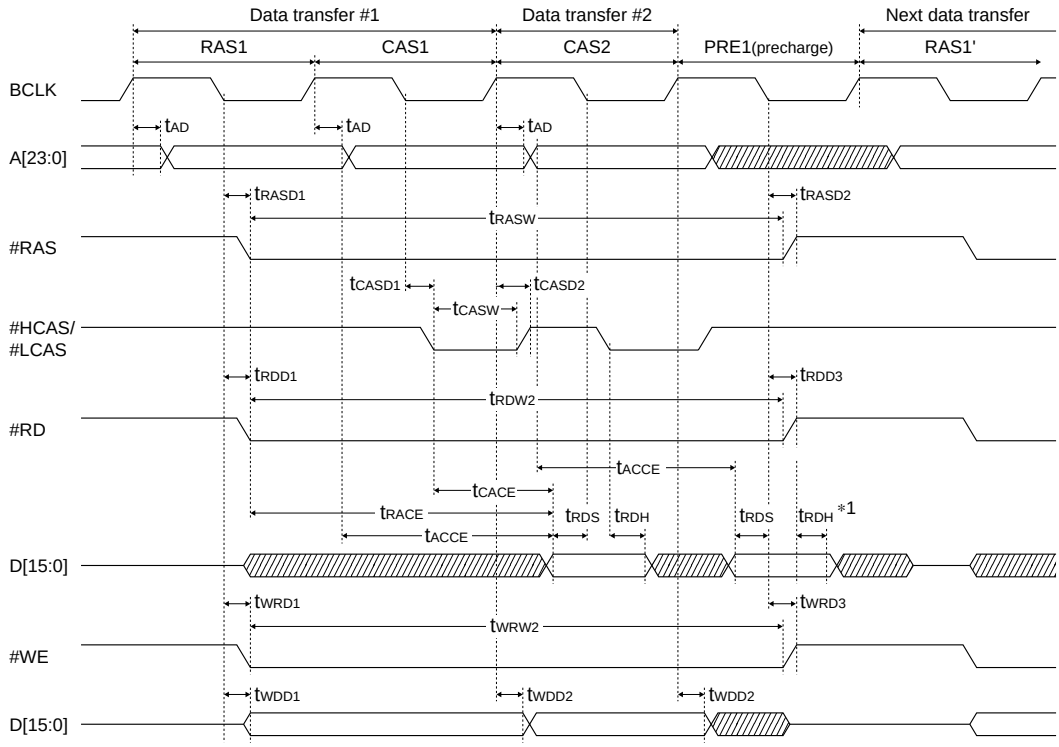
*1 tRDH is measured with respect to the first signal change (negation) of either the #RD or the A[23:0] signals.

EDO DRAM random access cycle (basic cycle)



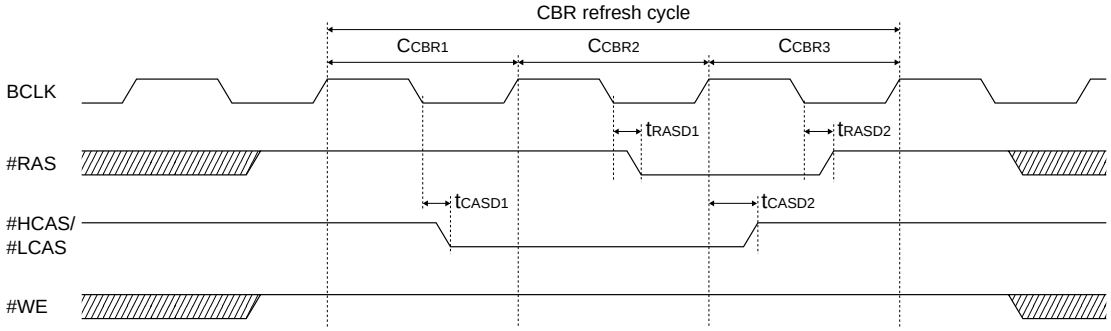
∗1 tRDH is measured with respect to the first signal change (negation) of either the #RD or the #RASx signals.

EDO DRAM page access cycle

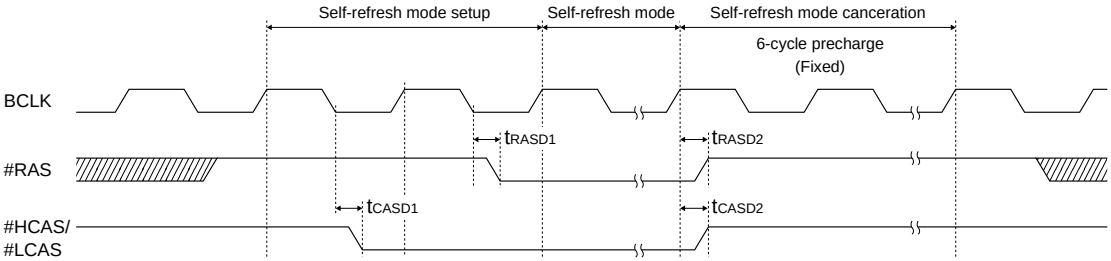


∗1 tRDH is measured with respect to the first signal change from among the #RD (negation), #RASx (negation) and #CAS (rise) signals.

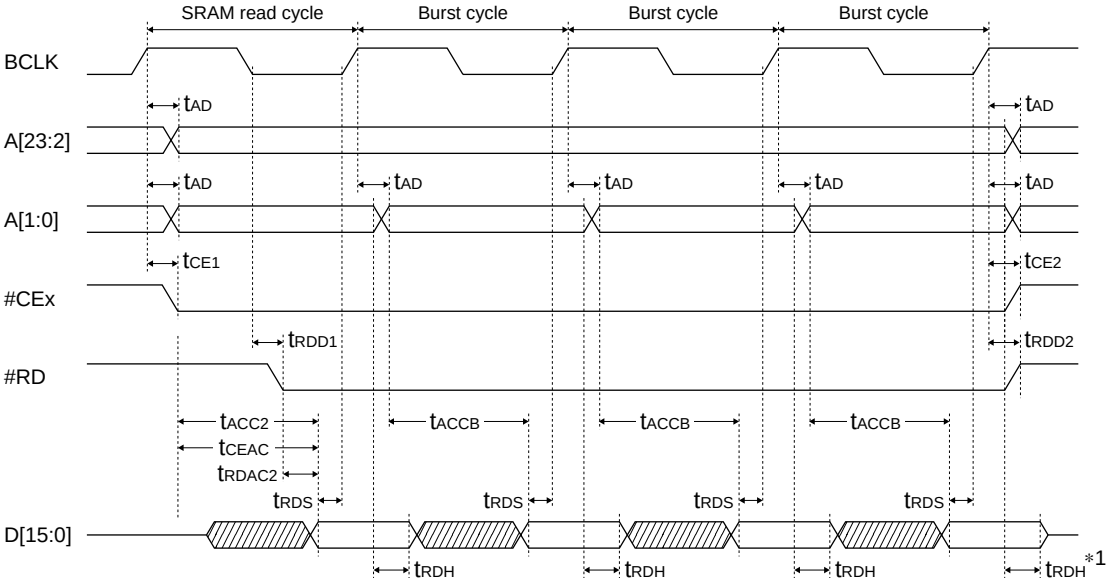
DRAM CAS-before-RAS refresh cycle



DRAM self-refresh cycle

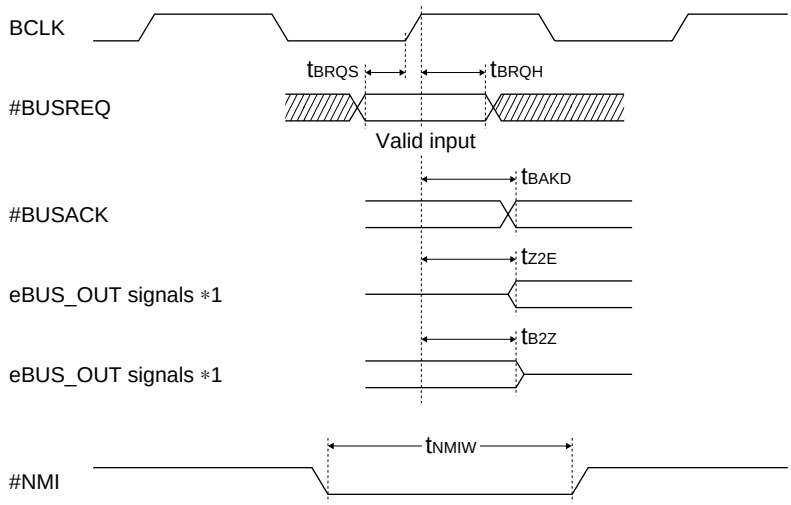


Burst ROM read cycle



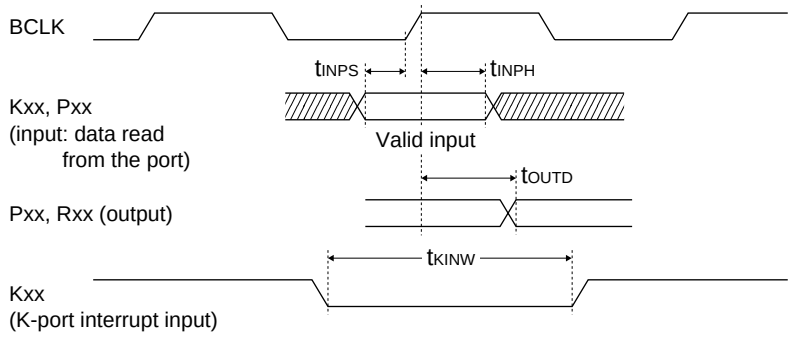
*1 tRDH is measured with respect to the first signal change (negation) from among the #RD, #CEx and A[23:0] signals.

#BUSREQ, #BUSACK and #NMI timing



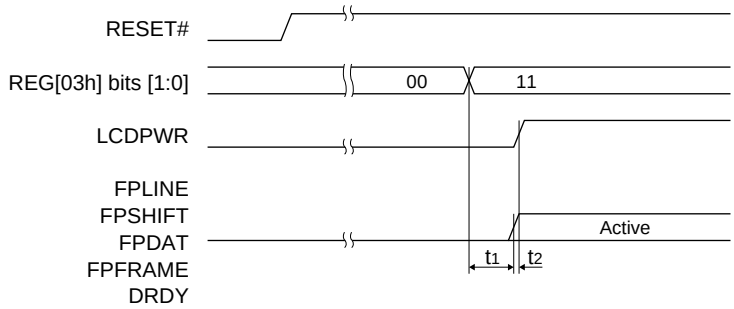
∗1 eBUS_OUT indicates the following pins:
A[23:0], #RD, #WRL, #WRH, #HCAS, #LCAS, #CE[17:4], D[15:0]

Input, output and I/O port timing



8.6.5 LCD Interface AC Characteristics

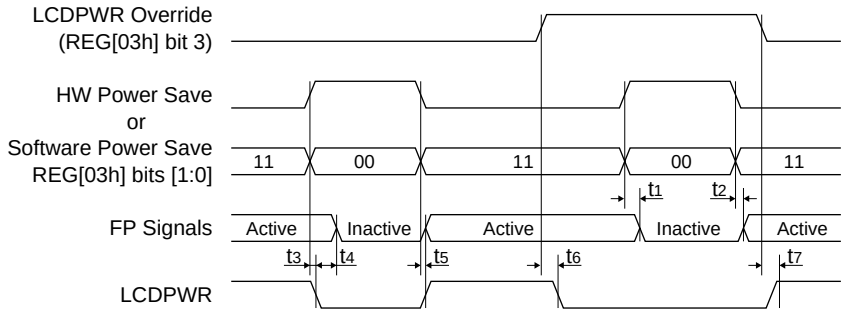
Power on/reset timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	REG[03h] to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY active			$T_{FPFRAME}$	ns
t_2	FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY active to LCDPWR		0		Frame

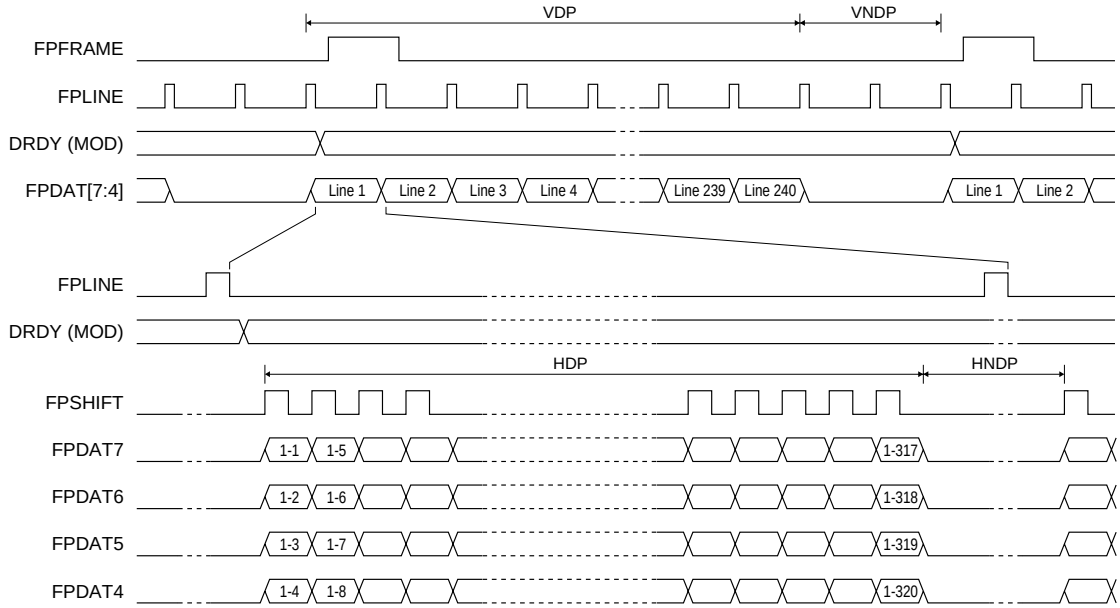
Note: Where $T_{FPFRAME}$ is the period of FPFRAME and T_{PCLK} is the period of the pixel clock.

Power down/up timing



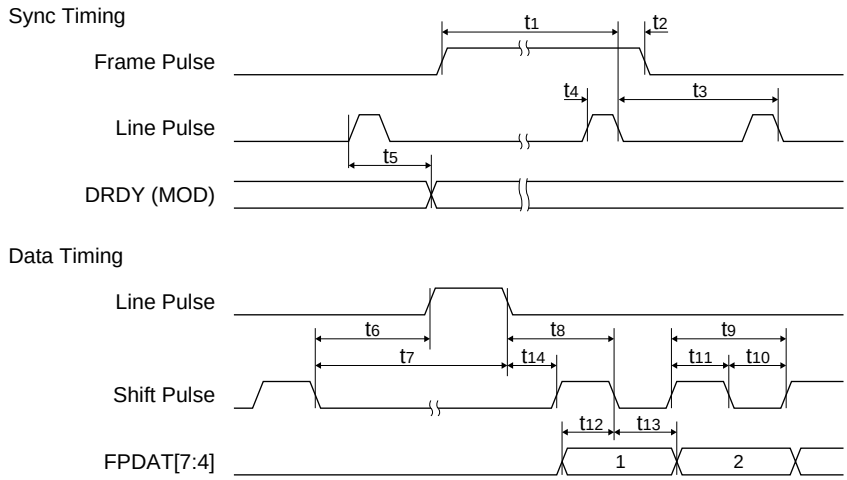
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	HW Power Save active to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY inactive - LCDPWR Override = 1			1	Frame
t_2	HW Power Save inactive to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY active - LCDPWR Override = 1			1	Frame
t_3	HW Power Save active to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY inactive - LCDPWR Override = 0			1	Frame
t_4	LCDPWR low to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY inactive - LCDPWR Override = 0		127		Frame
t_5	HW Power Save inactive to FPLINE, FPFRAME, FPSHIFT, FPDAT, DRDY, LCDPWR active - LCDPWR Override = 0		0		Frame
t_6	LCDPWR Override active (1) to LCDPWR inactive			1	Frame
t_7	LCDPWR Override inactive (1) to LCDPWR active			1	Frame

4-bit single monochrome panel timing



∗ Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 320 × 240 panel
For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

VDP = Vertical Display Period = (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP = Vertical Non-Display Period = REG[0Ah] bits [5:0] Lines
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = (REG[08h] + 4) × 8Ts



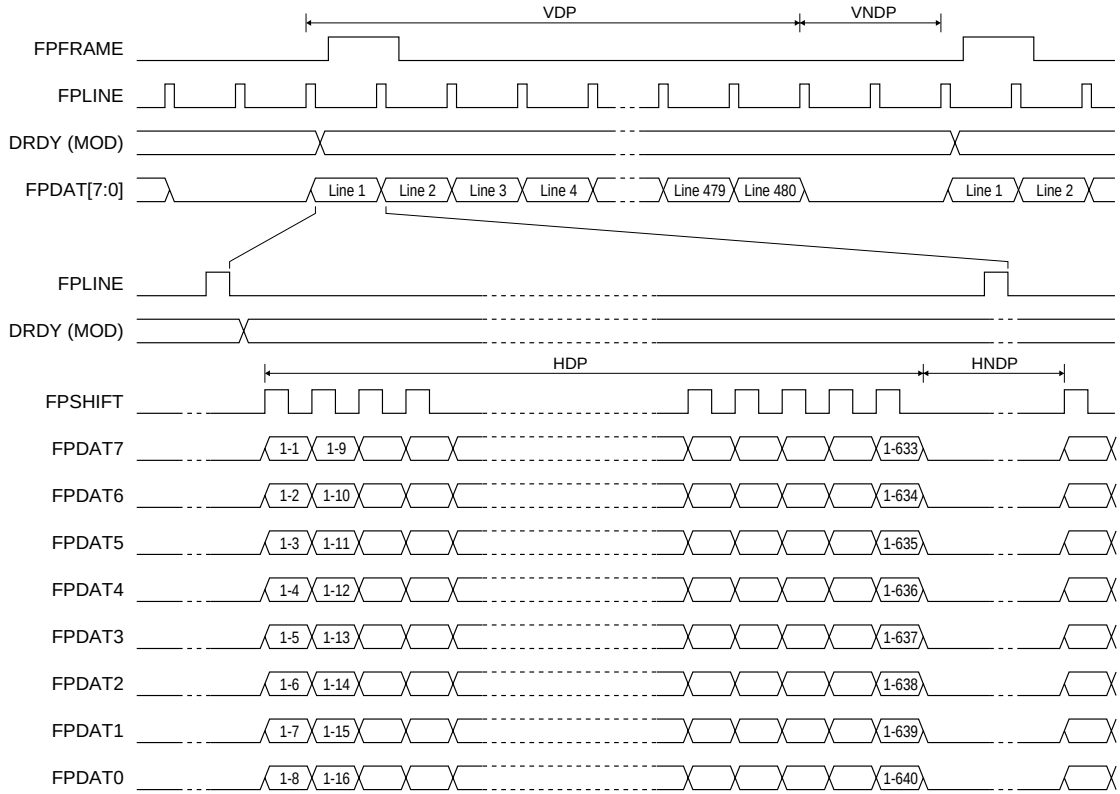
Note: For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

4-bit Single Monochrome Panel AC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t_2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t_3	Line Pulse period	note 3			
t_4	Line Pulse pulse width	9			Ts
t_5	MOD delay from Line Pulse rising edge	1			Ts
t_6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t_7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t_8	Line Pulse falling edge to Shift Pulse falling edge	t_{14}+2			Ts
t_9	Shift Pulse period	4			Ts
t_{10}	Shift Pulse pulse width low	2			Ts
t_{11}	Shift Pulse pulse width high	2			Ts
t_{12}	FPDAT[7:4] setup to Shift Pulse falling edge	2			Ts
t_{13}	FPDAT[7:4] hold from Shift Pulse falling edge	2			Ts
t_{14}	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

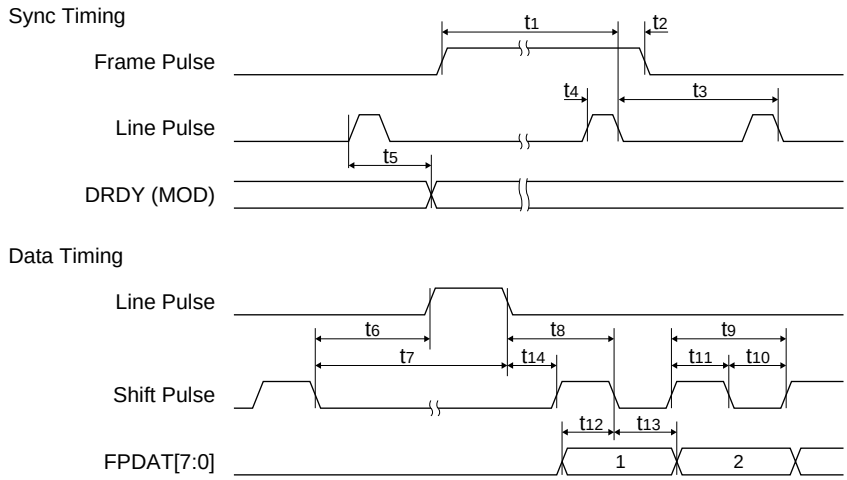
note) 1. Ts = pixel clock period
2. t_{1min} = t_{3min} - 9Ts
3. t_{3min} = [((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8]Ts
4. t_{6min} = [(REG[08h] bits [4:0]) × 8 + 2]Ts
5. t_{7min} = [(REG[08h] bits [4:0]) × 8 + 11]Ts

8-bit single monochrome panel timing



∗ Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640 × 480 panel
For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

VDP = Vertical Display Period = (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP = Vertical Non-Display Period = REG[0Ah] bits [5:0] Lines
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = (REG[08h] + 4) × 8Ts



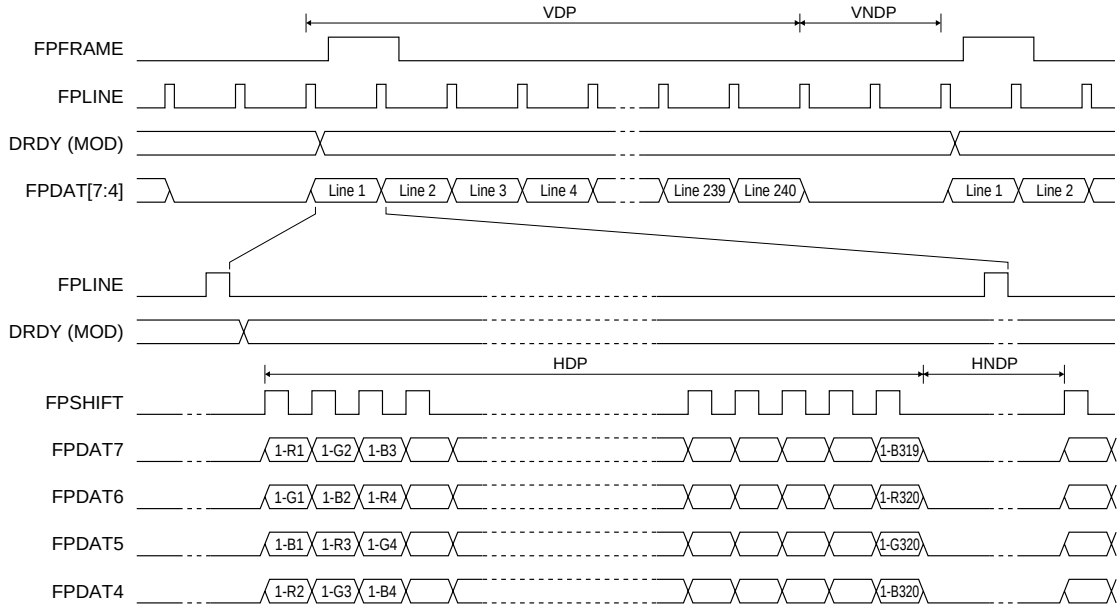
Note: For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

8-bit Single Monochrome Panel AC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t_2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t_3	Line Pulse period	note 3			
t_4	Line Pulse pulse width	9			Ts
t_5	MOD delay from Line Pulse rising edge	1			Ts
t_6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t_7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t_8	Line Pulse falling edge to Shift Pulse falling edge	t_{14}+4			Ts
t_9	Shift Pulse period	8			Ts
t_{10}	Shift Pulse pulse width low	4			Ts
t_{11}	Shift Pulse pulse width high	4			Ts
t_{12}	FPDAT[7:0] setup to Shift Pulse falling edge	4			Ts
t_{13}	FPDAT[7:0] hold from Shift Pulse falling edge	4			Ts
t_{14}	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

note) 1. Ts = pixel clock period
2. t_{1min} = t_{3min} - 9Ts
3. t_{3min} = [((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8]Ts
4. t_{6min} = [(REG[08h] bits [4:0]) × 8 + 4]Ts
5. t_{7min} = [(REG[08h] bits [4:0]) × 8 + 13]Ts

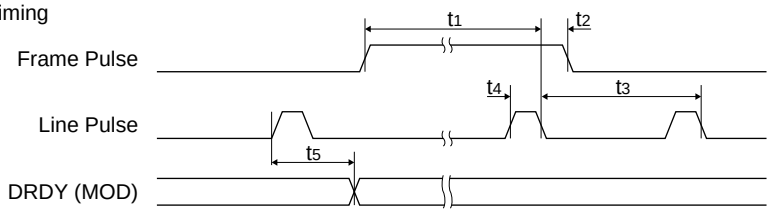
4-bit single color panel timing



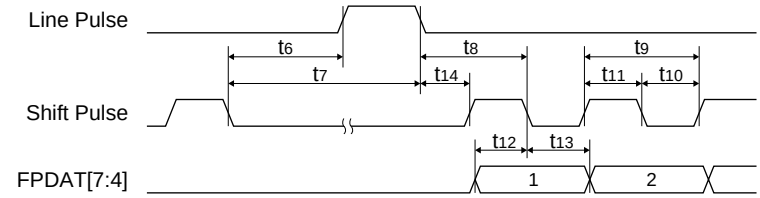
∗ Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 320 × 240 panel

VDP = Vertical Display Period = (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP = Vertical Non-Display Period = REG[0Ah] bits [5:0] Lines
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = (REG[08h] + 4) × 8Ts

Sync Timing



Data Timing

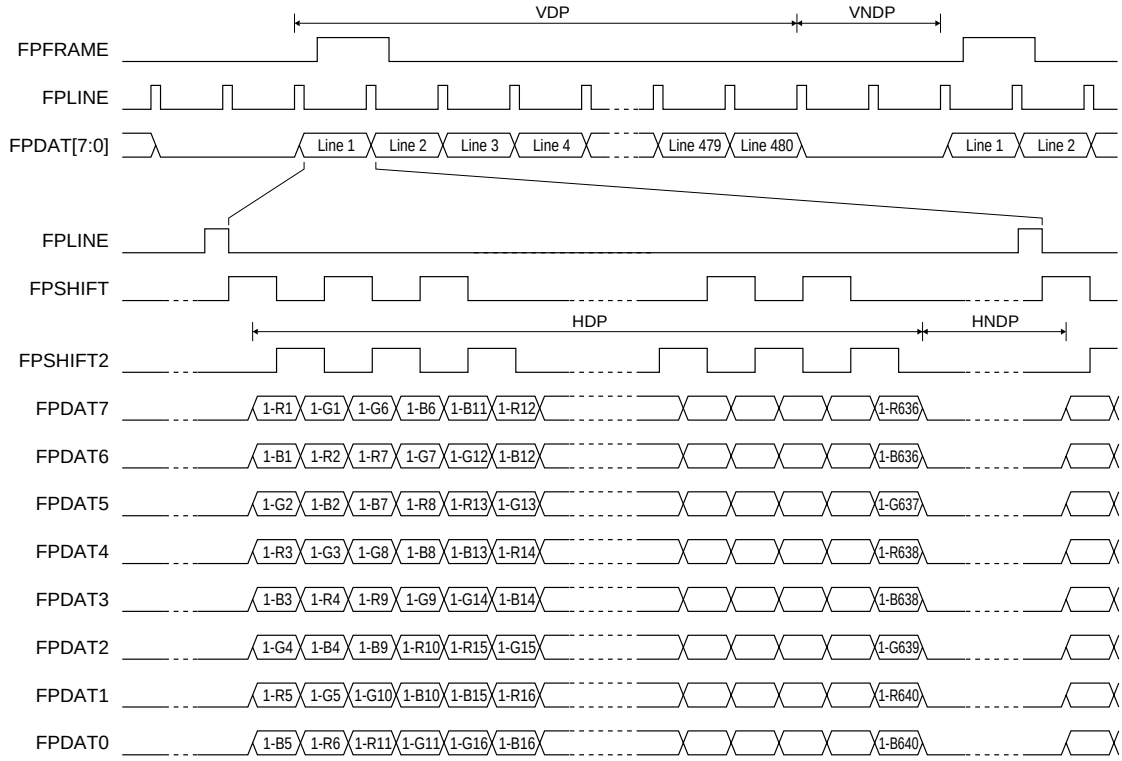


4-bit Single Color Panel AC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t_2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t_3	Line Pulse period	note 3			
t_4	Line Pulse pulse width	9			Ts
t_5	MOD delay from Line Pulse rising edge	1			Ts
t_6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t_7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t_8	Line Pulse falling edge to Shift Pulse falling edge	t_{14}+0.5			Ts
t_9	Shift Pulse period	1			Ts
t_{10}	Shift Pulse pulse width low	0.5			Ts
t_{11}	Shift Pulse pulse width high	0.5			Ts
t_{12}	FPDAT[7:4] setup to Shift Pulse falling edge	0.5			Ts
t_{13}	FPDAT[7:4] hold from Shift Pulse falling edge	0.5			Ts
t_{14}	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

note) 1. Ts = pixel clock period
2. t_{1min} = t_{3min} - 9Ts
3. t_{3min} = [((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8]Ts
4. t_{6min} = [(REG[08h] bits [4:0]) × 8 + 0.5]Ts
5. t_{7min} = [(REG[08h] bits [4:0]) × 8 + 9.5]Ts

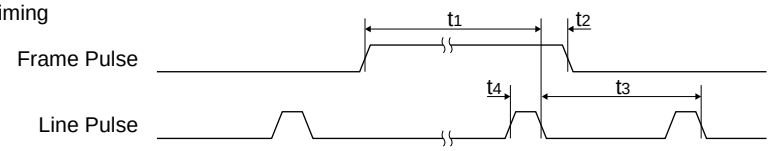
8-bit single color panel timing (Format 1)



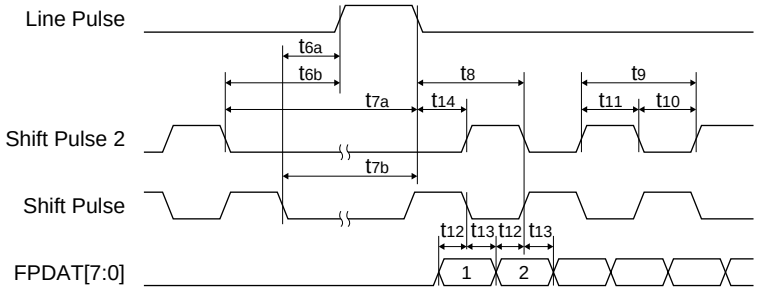
∗ Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640 × 480 panel

VDP = Vertical Display Period = (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP = Vertical Non-Display Period = REG[0Ah] bits [5:0] Lines
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = (REG[08h] + 4) × 8Ts

Sync Timing



Data Timing

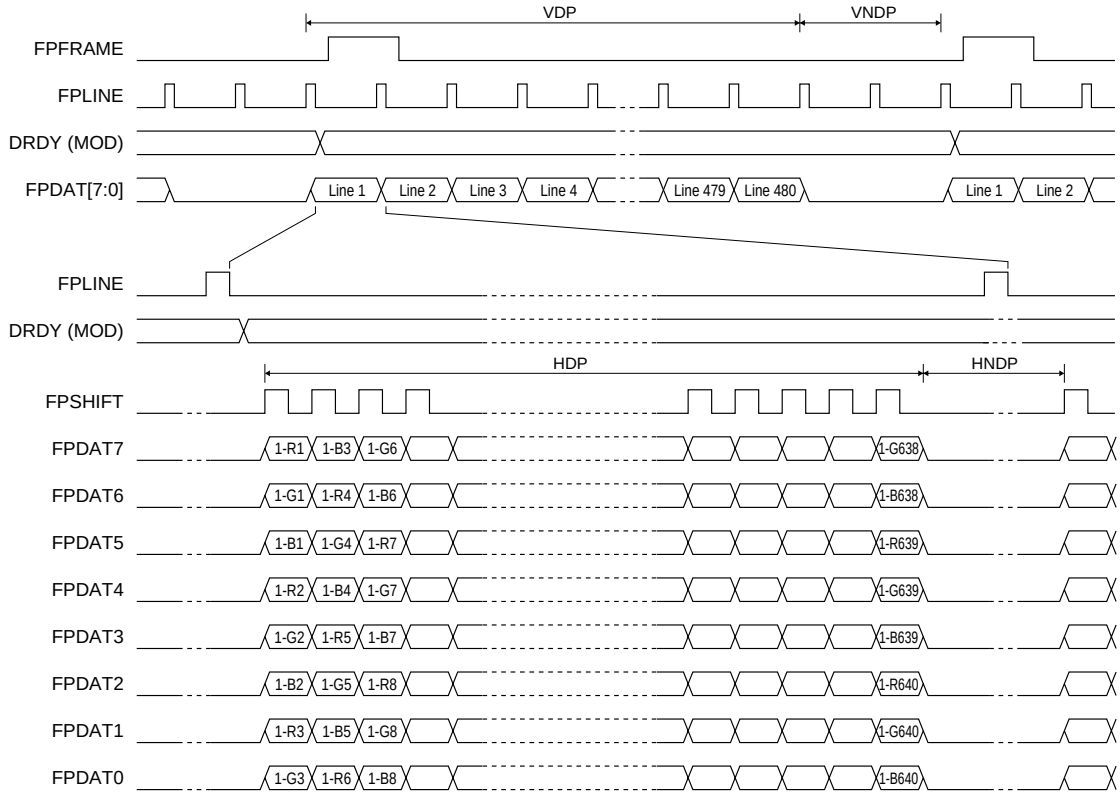


8-bit Single Color Panel AC Timing (Format 1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t_2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t_3	Line Pulse period	note 3			
t_4	Line Pulse pulse width	9			Ts
t_{6a}	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t_{6b}	Shift Pulse 2 falling edge to Line Pulse rising edge	note 5			
t_{7a}	Shift Pulse 2 falling edge to Line Pulse falling edge	note 6			
t_{7b}	Shift Pulse falling edge to Line Pulse falling edge	note 7			
t_8	Line Pulse falling edge to Shift Pulse rising, Shift Pulse 2 falling edge	t_{14}+2			Ts
t_9	Shift Pulse 2, Shift Pulse period	4			Ts
t_{10}	Shift Pulse 2, Shift Pulse pulse width low	2			Ts
t_{11}	Shift Pulse 2, Shift Pulse pulse width high	2			Ts
t_{12}	FPDAT[7:0] setup to Shift Pulse 2, Shift Pulse falling edge	1			Ts
t_{13}	FPDAT[7:0] hold from Shift Pulse 2, Shift Pulse falling edge	1			Ts
t_{14}	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

note) 1. Ts = pixel clock period
2. t_{1min} = t_{3min} - 9Ts
3. t_{3min} = [((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8]Ts
4. t_{6amin} = [(REG[08h] bits [4:0]) × 8 + t_{13} - t_{10}]Ts
5. t_{6bmin} = [(REG[08h] bits [4:0]) × 8 + t_{13}]Ts
6. t_{7amin} = [(REG[08h] bits [4:0]) × 8 + 11]Ts
7. t_{7bmin} = [((REG[08h] bits [4:0]) × 8 + 11) - t_{10}]Ts

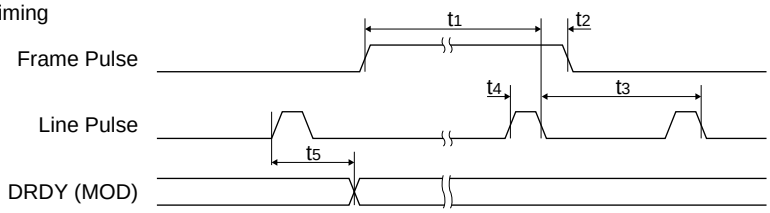
8-bit single color panel timing (Format 2)



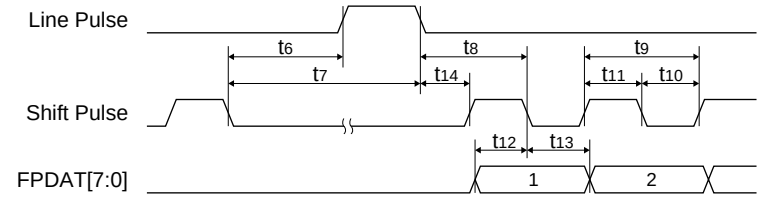
∗ Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640 × 480 panel

VDP = Vertical Display Period = (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP = Vertical Non-Display Period = REG[0Ah] bits [5:0] Lines
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = (REG[08h] + 4) × 8Ts

Sync Timing



Data Timing

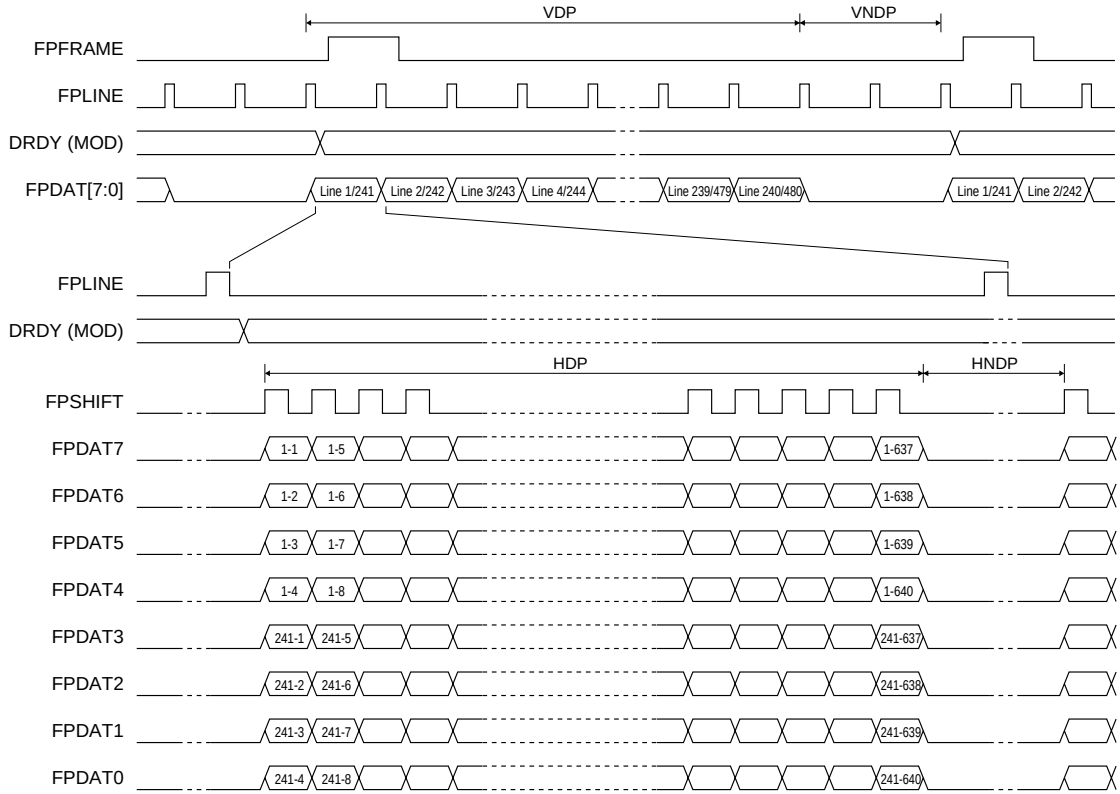


8-bit Single Color Panel AC Timing (Format 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t_2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t_3	Line Pulse period	note 3			
t_4	Line Pulse pulse width	9			Ts
t_5	MOD delay from Line Pulse rising edge	1			Ts
t_6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t_7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t_8	Line Pulse falling edge to Shift Pulse falling edge	t_{14}+2			Ts
t_9	Shift Pulse period	2			Ts
t_{10}	Shift Pulse pulse width low	1			Ts
t_{11}	Shift Pulse pulse width high	1			Ts
t_{12}	FPDAT[7:0] setup to Shift Pulse falling edge	1			Ts
t_{13}	FPDAT[7:0] hold from Shift Pulse falling edge	1			Ts
t_{14}	Line Pulse falling edge to Shift Pulse rising edge	23			Ts

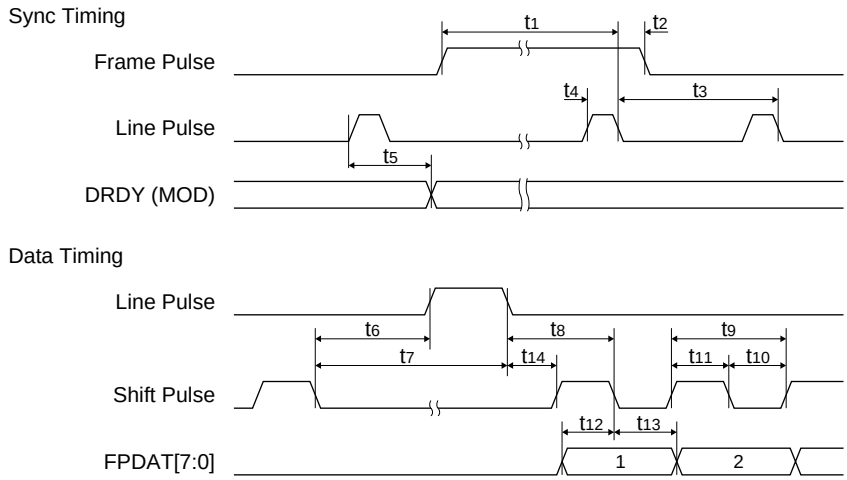
note) 1. Ts = pixel clock period
2. t_{1min} = t_{3min} - 9Ts
3. t_{3min} = [((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8]Ts
4. t_{6min} = [(REG[08h] bits [4:0]) × 8 + 1]Ts
5. t_{7min} = [(REG[08h] bits [4:0]) × 8 + 10]Ts

8-bit dual monochrome panel timing



∗ Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640 × 480 panel

VDP = Vertical Display Period = (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP = Vertical Non-Display Period = REG[0Ah] bits [5:0] Lines
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = (REG[08h] + 4) × 8Ts



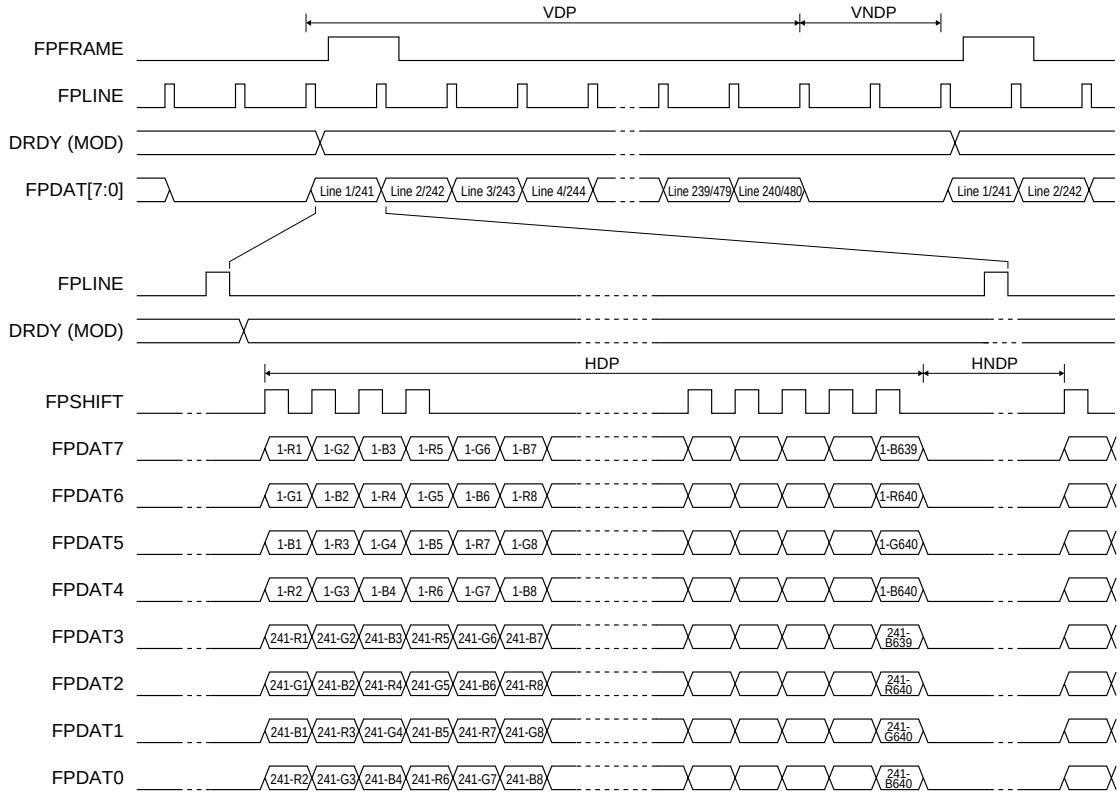
Note: For this timing diagram Mask FPSHIFT, REG[01h] bit 3, is set to 1

8-bit Dual Monochrome Panel AC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t_2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t_3	Line Pulse period	note 3			
t_4	Line Pulse pulse width	9			Ts
t_5	MOD delay from Line Pulse rising edge	1			Ts
t_6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t_7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t_8	Line Pulse falling edge to Shift Pulse falling edge	t_{14}+4			Ts
t_9	Shift Pulse period	8			Ts
t_{10}	Shift Pulse pulse width low	4			Ts
t_{11}	Shift Pulse pulse width high	4			Ts
t_{12}	FPDAT[7:0] setup to Shift Pulse falling edge	4			Ts
t_{13}	FPDAT[7:0] hold from Shift Pulse falling edge	4			Ts
t_{14}	Line Pulse falling edge to Shift Pulse rising edge	39			Ts

note) 1. Ts = pixel clock period
2. t_{1min} = t_{3min} - 9Ts
3. t_{3min} = [(((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8) × 2]Ts
4. t_{6min} = [((REG[08h] bits [4:0]) × 2) × 8 + 20]Ts
5. t_{7min} = [((REG[08h] bits [4:0]) × 2) × 8 + 29]Ts

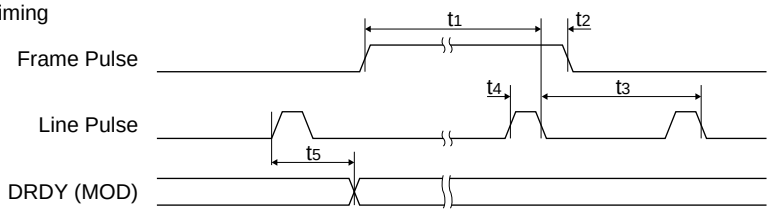
8-bit dual color panel timing



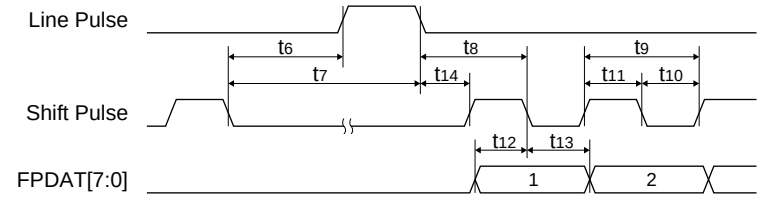
∗ Diagram drawn with 2 FPLINE vertical blank period
Example timing for a 640 × 480 panel

VDP = Vertical Display Period = (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP = Vertical Non-Display Period = REG[0Ah] bits [5:0] Lines
HDP = Horizontal Display Period = ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP = Horizontal Non-Display Period = (REG[08h] + 4) × 8Ts

Sync Timing



Data Timing

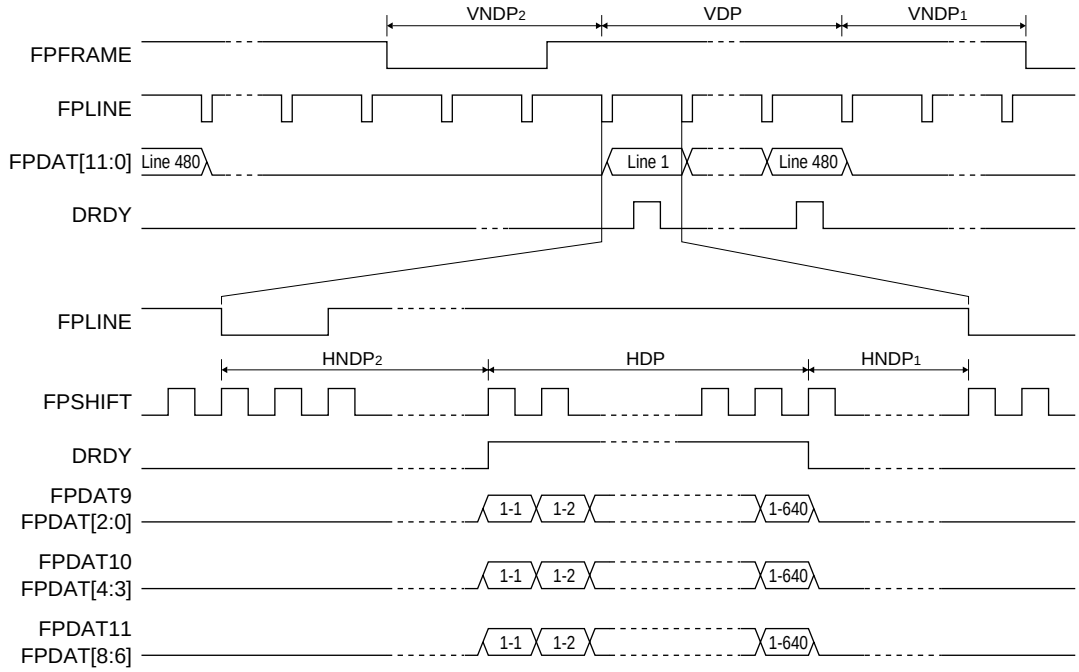


8-bit Dual Color Panel AC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Frame Pulse setup to Line Pulse falling edge	note 2			(note 1)
t_2	Frame Pulse hold from Line Pulse falling edge	9			Ts
t_3	Line Pulse period	note 3			
t_4	Line Pulse pulse width	9			Ts
t_5	MOD delay from Line Pulse rising edge	1			Ts
t_6	Shift Pulse falling edge to Line Pulse rising edge	note 4			
t_7	Shift Pulse falling edge to Line Pulse falling edge	note 5			
t_8	Line Pulse falling edge to Shift Pulse falling edge	t_{14}+1			Ts
t_9	Shift Pulse period	2			Ts
t_{10}	Shift Pulse pulse width low	1			Ts
t_{11}	Shift Pulse pulse width high	1			Ts
t_{12}	FPDAT[7:0] setup to Shift Pulse falling edge	1			Ts
t_{13}	FPDAT[7:0] hold from Shift Pulse falling edge	1			Ts
t_{14}	Line Pulse falling edge to Shift Pulse rising edge	39			Ts

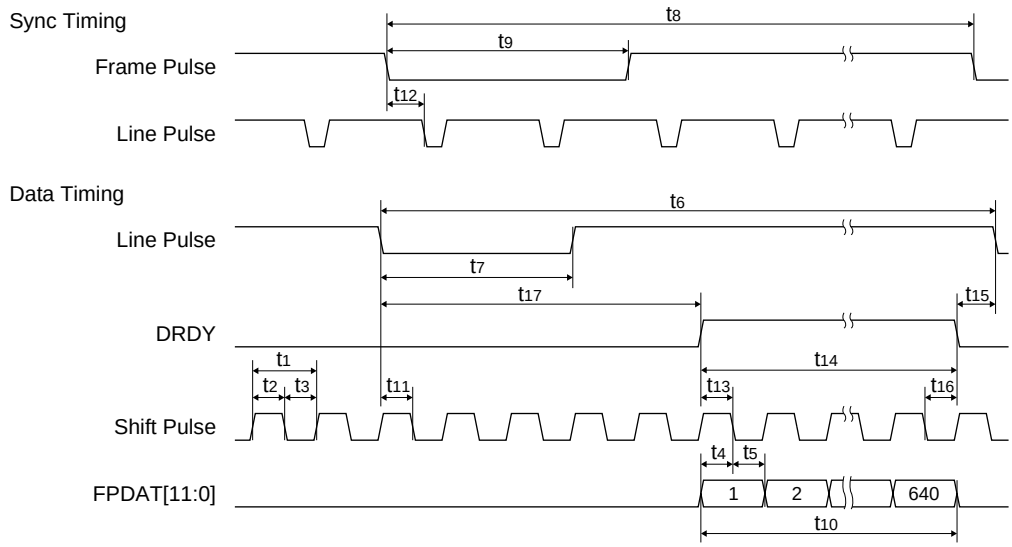
note) 1. Ts = pixel clock period
2. t_{1min} = t_{3min} - 9Ts
3. t_{3min} = [(((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8) × 2]Ts
4. t_{6min} = [((REG[08h] bits [4:0]) × 2) × 8 + 17]Ts
5. t_{7min} = [((REG[08h] bits [4:0]) × 2) × 8 + 26]Ts

12-bit TFT/D-TFD panel timing



∗ DRDY is used to indicate the first pixel
Example timing for a 12-bit 640 × 480 panel

VDP	= Vertical Display Period	= (REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1 Lines
VNDP	= Vertical Non-Display Period	= VNDP1 + VNDP2 = REG[0Ah] bits [5:0] Lines
VNDP1	= Vertical Non-Display Period 1	= REG[09h] bits [5:0] Lines
VNDP2	= Vertical Non-Display Period 2	= (REG[0Ah] bits [5:0]) - (REG[09h] bits [5:0]) Lines
HDP	= Horizontal Display Period	= ((REG[04h] bits [6:0]) + 1) × 8Ts
HNDP	= Horizontal Non-Display Period	= HNDP1 + HNDP2 = (REG[08h] + 4) × 8Ts
HNDP1	= Horizontal Non-Display Period 1	= ((REG[07h] bits [4:0]) × 8) + 16Ts
HNDP2	= Horizontal Non-Display Period 2	= (((REG[08h] bits [4:0]) - (REG[07h] bits [4:0])) × 8) + 16Ts



Note: DRDY is used to indicate the first pixel

TFT/D-TFD Panel AC Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Shift Pulse period	1			(note 1)
t_2	Shift Pulse pulse width high	0.5			Ts
t_3	Shift Pulse pulse width low	0.5			Ts
t_4	Data setup to Shift Pulse falling edge	0.5			Ts
t_5	Data hold from Shift Pulse falling edge	0.5			Ts
t_6	Line Pulse cycle time	note 2			
t_7	Line Pulse pulse width low	9			Ts
t_8	Frame Pulse cycle time	note 3			
t_9	Frame Pulse pulse width low	$2t_6$			Ts
t_{10}	Horizontal display period	note 4			
t_{11}	Line Pulse setup to Shift Pulse falling edge	0.5			Ts
t_{12}	Frame Pulse falling edge to Line Pulse falling edge phase difference	t_6-18Ts			
t_{13}	DRDY to Shift Pulse falling edge setup time	0.5			Ts
t_{14}	DRDY pulse width	note 5			
t_{15}	DRDY falling edge to Line Pulse falling edge	note 6			
t_{16}	DRDY hold from Shift Pulse falling edge	0.5			Ts
t_{17}	Line Pulse falling edge to DRDY active	note 7		250	Ts

note) 1. Ts = pixel clock period
2. t_{6min} = [((REG[04h] bits [6:0]) + 1) × 8 + ((REG[08h] bits [4:0]) + 4) × 8]Ts
3. t_{8min} = [((REG[06h] bits [1:0], REG[05h] bits [7:0]) + 1) + (REG[0Ah] bits [6:0])]Lines
4. t_{10min} = [((REG[04h] bits [6:0]) + 1) × 8]Ts
5. t_{14min} = [((REG[04h] bits [6:0]) + 1) × 8]Ts
6. t_{15min} = [(REG[07h] bits [4:0]) × 8 + 16]Ts
7. t_{17min} = [(REG[08h] bits [4:0]) - (REG[07h] bits [4:0]) × 8 + 16]Ts

8.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic or crystal oscillator is used, use the oscillator manufacturer recommended values for constants such as capacitance and resistance.

OSC1 crystal oscillation

(Unless otherwise specified: crystal=C-002RX#1 32.768kHz, Rf_1=20MΩ, C_{G1}=C_{D1}=15pF#2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Operating temperature	Ta	V_{DD}=2.7V to 3.6V	-40		85	°C	
		V_{DD}=1.9V to 2.2V	-40		85	°C	
		V_{DD}=1.8V to 2.2V	0		70	°C	

#1 C-002RX: Crystal resonator made by Seiko Epson
#2 "C_{G1}=C_{D1}=15pF" includes board capacitance.

(Unless otherwise specified: V_{DD}=3.3V, V_{SS}=0V, crystal=C-002RX#1 32.768kHz, Rf_1=20MΩ, C_{G1}=C_{D1}=15pF#2, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Oscillation start time	t_{STA1}				3	sec	
External gate/drain capacitance	C_{G1}, C_{D1}	C_{G1}=C_{D1}, including board capacitance	5		25	pF	
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm	
Frequency/power voltage deviation	Δf/ΔV		-10		10	ppm/V	
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	50			ppm	

#1 C-002RX: Crystal resonator made by Seiko Epson
#2 "C_{G1}=C_{D1}=15pF" includes board capacitance.

(Unless otherwise specified: V_{DD}=2.0V, V_{SS}=0V, crystal=C-002RX#1 32.768kHz, Rf_1=20MΩ, C_{G1}=C_{D1}=15pF#2, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Oscillation start time	t_{STA1}				20	sec	
External gate/drain capacitance	C_{G1}, C_{D1}	C_{G1}=C_{D1}, including board capacitance	5		25	pF	
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm	
Frequency/power voltage deviation	Δf/ΔV		-10		10	ppm/V	
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	50			ppm	

#1 C-002RX: Crystal resonator made by Seiko Epson
#2 "C_{G1}=C_{D1}=15pF" includes board capacitance.

OSC3 crystal oscillation

Note: A "crystal resonator that uses a fundamental" should be used for the OSC3 crystal oscillation circuit.

(Unless otherwise specified: V_{DD}=3.3V, V_{SS}=0V, crystal=MA-306#1 33.8688MHz, Rf_2=1MΩ, C_{G1}=C_{D1}=15pF#2, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Oscillation start time	t_{STA3}	V_{DD}=3.3V			10	ms	
		V_{DD}=2.0V			25	ms	

#1 MA-306: Crystal resonator made by Seiko Epson
#2 "C_{G1}=C_{D1}=15pF" includes board capacitance.

OSC3 ceramic oscillation

(Unless otherwise specified: V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	∗
Oscillation start time	t_{STA3}	10MHz ceramic oscillator			10	ms	1
		16MHz ceramic oscillator			10	ms	2
		20MHz ceramic oscillator			10	ms	3
		25MHz ceramic oscillator			5	ms	4
		33MHz ceramic oscillator			5	ms	5

∗ note)

No.	Ceramic oscillator	Recommended constants			Power voltage range (V)	Remarks (Manufacturer)
		C_{G2} (pF)	C_{D2} (pF)	Rf_2 (MΩ)		
1	CST10.0MTW	30	30	1	1.8 to 2.2	(Murata Mfg. corporation) ∗1
2	CST16.00MXW0C1	5	5	1	1.8 to 2.2	(Murata Mfg. corporation)
3	CST20.00MXW0H1	5	5	1	1.8 to 2.2	(Murata Mfg. corporation)
4	CST25.00MXW0H1	5	5	1	2.7 to 3.6	(Murata Mfg. corporation)
5	CST33.00MXZ040	Open	Open	1	2.7 to 3.6	(Murata Mfg. corporation)

∗1 This oscillator has a tendency to rise to the frequency of 0.3%.

8.8 PLL Characteristics

Setting the PLLS0 and PLLS1 pins (recommended operating condition)

V_{DD}=2.7V to 3.6V

PLLS1	PLLS0	Mode	Fin (OSC3 clock)	Fout
1	1	x2	10 to 25MHz	20 to 50MHz
0	1	x4	10 to 12.5MHz	40 to 50MHz
0	0	PLL not used	–	–

V_{DD}=2.0V±0.2V

PLLS1	PLLS0	Mode	Fin (OSC3 clock)	Fout
1	1	x2	10MHz	20MHz
0	0	PLL not used	–	–

PLL characteristics

(Unless otherwise specified: V_{DD}=2.7V to 3.6V, V_{SS}=0V, crystal oscillator=SG-8002#1, R_1=4.7kΩ, C_1=100pF, C_2=5pF, Ta=-40°C to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Jitter (peak jitter)	t_{pj}		-1		1	ns	
Lockup time	t_{pll}				1	ms	

#1 SG-8002: Crystal oscillator made by Seiko Epson

(Unless otherwise specified: V_{DD}=2.0V±0.2V, V_{SS}=0V, crystal oscillator=SG-8002#1, R_1=4.7kΩ, C_1=100pF, C_2=5pF, Ta=-40°C to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	*
Jitter (peak jitter)	t_{pj}		-2		2	ns	
Lockup time	t_{pll}				2	ms	

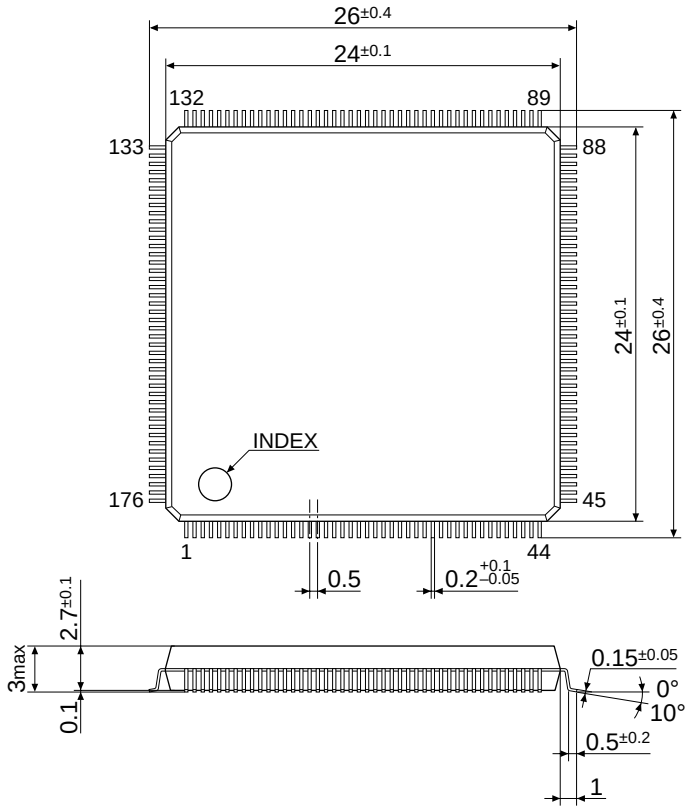
#1 SG-8002: Crystal oscillator made by Seiko Epson

9 Package

9.1 Plastic Package

QFP18-176pin

(Unit: mm)



Limit of power consumption

The chip temperature of an LSI rises according to power consumption. The chip temperature can be calculated from environment temperature (Ta), thermal resistance (θ) and power consumption (P_D).

Chip temperature (Tj) = Ta + ($P_D \times \theta$) (°C)

As a guide, normally keep the chip temperature (Tj) lower than 85°C.
The thermal resistance of the QFP18-176pin package is as follows:

Thermal resistance (°C/W) = 105 to 115°C (75 to 85°C for Cu lead frame)

This thermal resistance is a value under the condition that the measured device is hanging in the air and has no air-cooling. Thermal resistance greatly varies according to the mounting condition on the board and air-cooling condition.

Appendix A <Reference> External Device Interface Timings

This section shows setup examples for setting timing conditions of the external system interface as a reference material used when configuring a system with external devices.
Pay attention to the following precautions when using this material.

- The described AC characteristic values of external devices are standard values. They may differ from those of the devices actually used, so the actual setup values (number of cycles) should be determined by referring the manual or specification of the device to be used.
- It is necessary to set the timing values allowing ample margin according to the load capacitance of the bus and signal lines, number of devices to be connected, operating temperature range, I/O levels and other conditions. The number of cycles described in this section is an example and the conditions are not considered.
- The values described in "Time" column of the tables are simply calculated by multiplying the number of cycles by the cycle time. Conditions such as the output delay time of the device, delay due to wiring and load capacitance, and input setup time are not considered.
- The described contents are reference data and cannot be guaranteed to work.

A.1 DRAM (70ns)

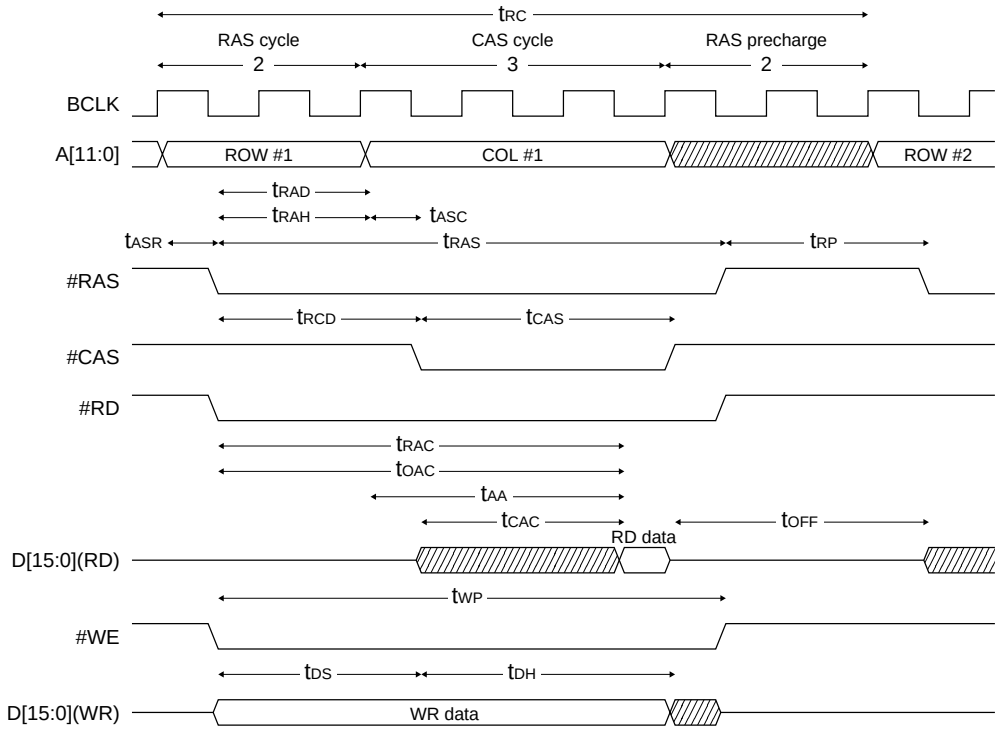
DRAM interface setup examples – 70ns

Operating frequency	RAS precharge cycle	RAS cycle	CAS cycle	Refresh RAS pulse width	Refresh RPC delay
20MHz	2	1	2	2	1
25MHz	2	1	2	2	1
33MHz	2	2	3	3	1

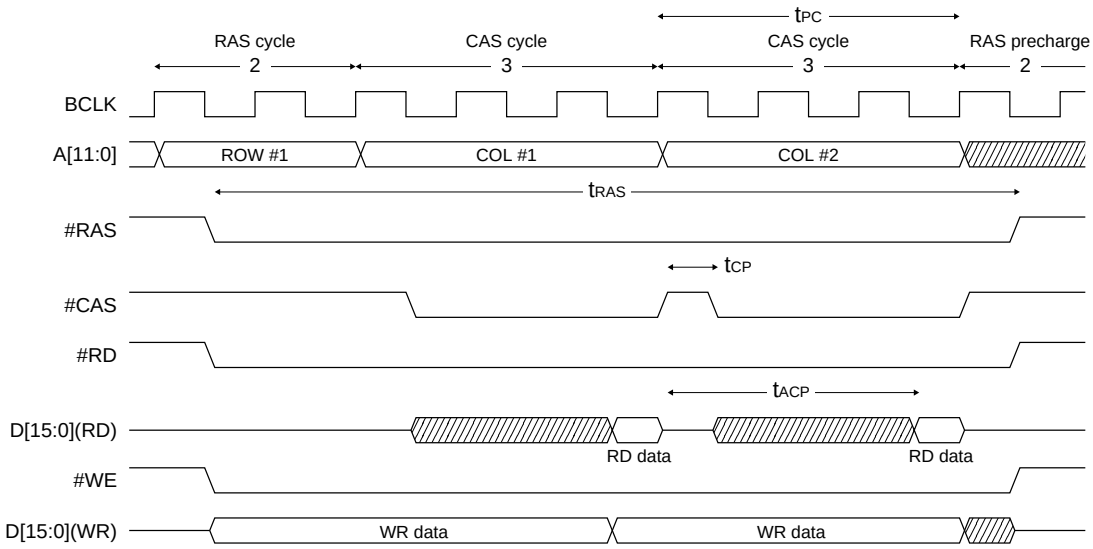
DRAM interface timing – 70ns

DRAM interface		Unit: ns		33MHz		25MHz		20MHz	
Parameter	Symbol	Min.	Max.	Cycle	Time	Cycle	Time	Cycle	Time
<Common parameters>									
Random read/random write cycle time	t_{RC}	130	–	7	210	5	200	5	250
#RAS precharge time	t_{RP}	50	–	2	60	2	80	2	100
#RAS pulse width	t_{RAS}	70	10000	5	150	3	120	3	150
#CAS pulse width	t_{CAS}	20	10000	2.5	75	1.5	60	1.5	75
Row address setup time	t_{ASR}	0	–	0.5	15	0.5	20	0.5	25
Row address hold time	t_{RAH}	10	–	1.5	45	0.5	20	0.5	25
Column address setup time	t_{ASC}	0	–	0.5	15	0.5	20	0.5	25
#RAS→#CAS delay time	t_{RCD}	20	–	2.0	60	1.0	40	1.0	50
#RAS→column address delay time	t_{RAD}	15	–	1.5	45	0.5	20	0.5	25
<Read-cycle parameters>									
#RAS access time	t_{RAC}	–	70	4.5	135	2.5	100	2.5	125
#CAS access time	t_{CAC}	–	20	2.5	75	1.5	60	1.5	75
Address access time	t_{AA}	–	35	3.0	90	2.0	80	2.0	100
#OE access time	t_{OAC}	–	20	4.5	135	2.5	100	2.5	125
Output buffer turn-off time	t_{OFF}	0	20	2	60	2	80	2	100
<Write-cycle parameters>									
Data input hold time	t_{DH}	15	–	2.5	75	1.5	60	1.5	75
<Fast-page mode>									
Fast-page mode cycle time	t_{PC}	45	–	3.0	90	2.0	80	2.0	100
Fast-page mode #CAS precharge time	t_{CP}	10	–	0.5	15	0.5	20	0.5	25
Access time after #CAS precharge	t_{ACP}	–	40	3.0	90	2.0	80	2.0	100
<Refresh cycle>									
#CAS setup time	t_{CSR}	10	–	1.0	30	1.0	40	1.0	50
#CAS hold time	t_{CHR}	10	–	2.5	75	1.5	60	1.5	75
#RAS precharge→#CAS hold time	t_{PPC}	10	–	1.0	30	1.0	40	1.0	50
#RAS pulse width (only in refresh cycle)	t_{RAS}	70	10000	3.0	90	2.0	80	2.0	100

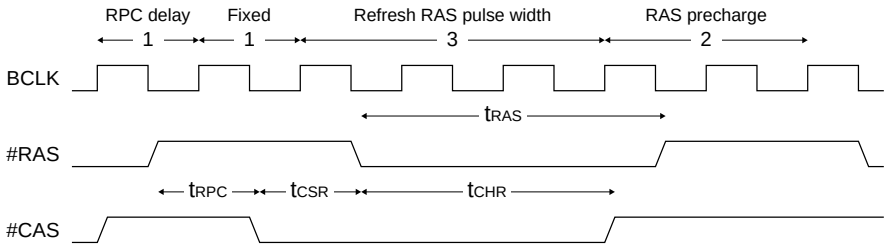
DRAM: 70ns, CPU: 33MHz, random read/write cycle



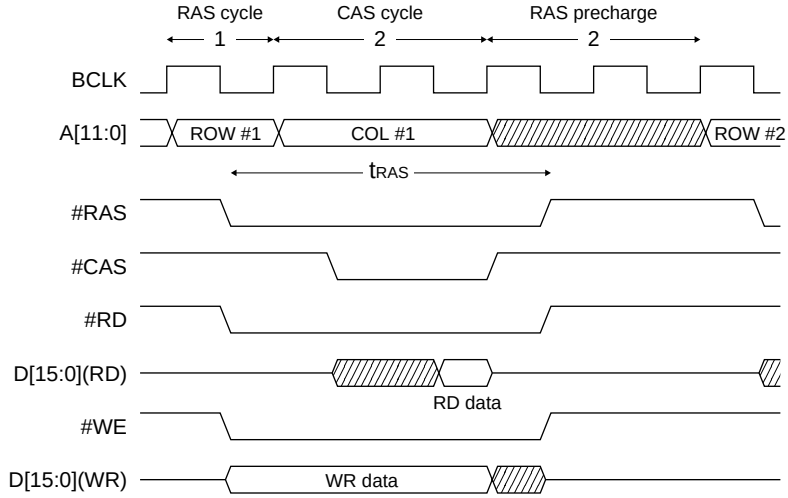
DRAM: 70ns, CPU: 33MHz, page-mode read/write cycle



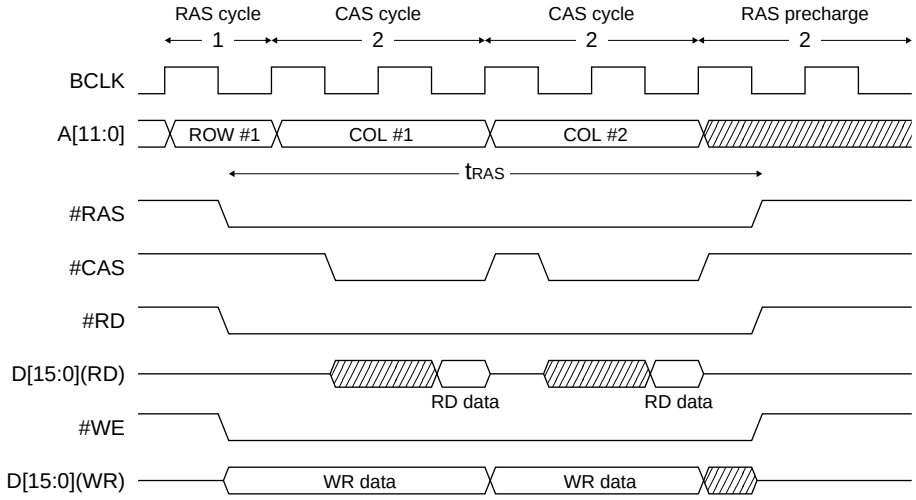
DRAM: 70ns, CPU: 33MHz, CAS-before-RAS refresh cycle



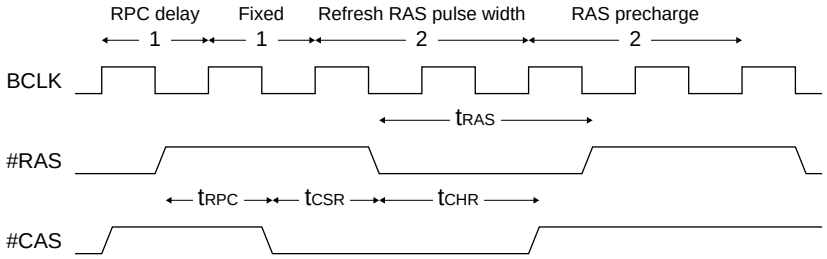
DRAM: 70ns, CPU: 25/20MHz, random read/write cycle



DRAM: 70ns, CPU: 25/20MHz, page-mode read/write cycle



DRAM: 70ns, CPU: 25/20MHz, CAS-before-RAS refresh cycle



A.2 DRAM (60ns)

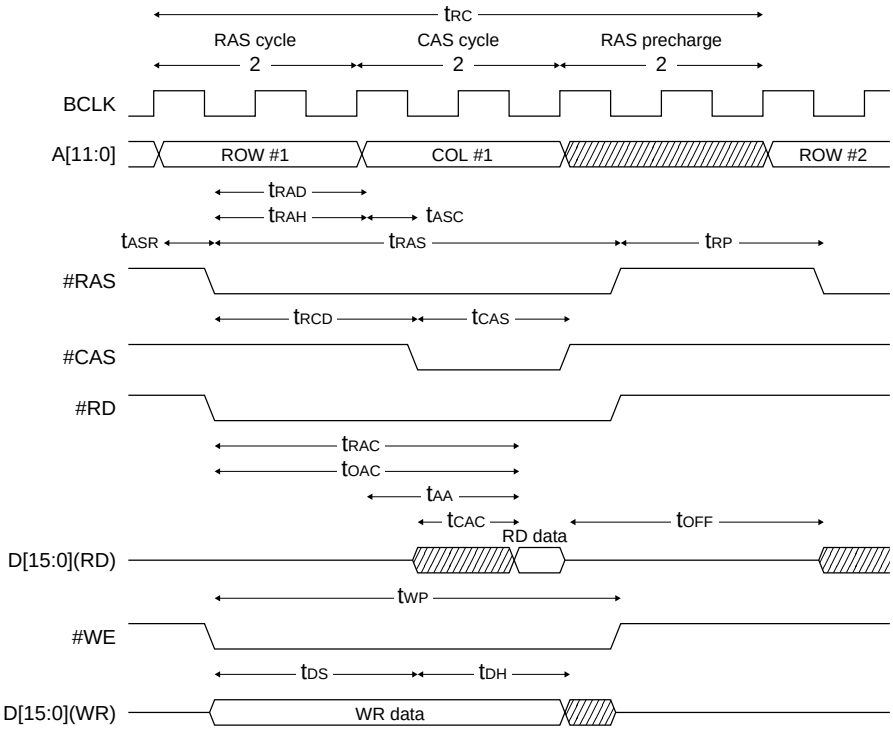
DRAM interface setup examples – 60ns

Operating frequency	RAS precharge cycle	RAS cycle	CAS cycle	Refresh RAS pulse width	Refresh RPC delay
20MHz	1	1	2	2	1
25MHz	2	1	2	2	1
33MHz	2	2	2	3	1

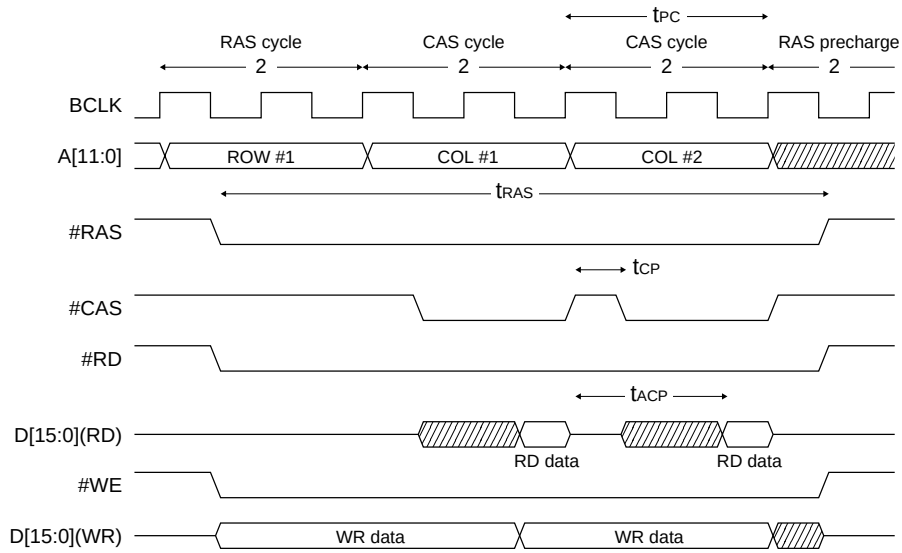
DRAM interface timing – 60ns

DRAM interface		Unit: ns		33MHz		25MHz		20MHz	
Parameter	Symbol	Min.	Max.	Cycle	Time	Cycle	Time	Cycle	Time
<Common parameters>									
Random read/random write cycle time	t_{RC}	110	–	6	180	5	200	4	200
#RAS precharge time	t_{RP}	40	–	2	60	2	80	1	50
#RAS pulse width	t_{RAS}	60	10000	4	120	3	120	3	150
#CAS pulse width	t_{CAS}	15	10000	1.5	45	1.5	60	1.5	75
Row address setup time	t_{ASR}	0	–	0.5	15	0.5	20	0.5	25
Row address hold time	t_{RAH}	10	–	1.5	45	0.5	20	0.5	25
Column address setup time	t_{ASC}	0	–	0.5	15	0.5	20	0.5	25
#RAS→#CAS delay time	t_{RCD}	20	–	2.0	60	1.0	40	1.0	50
#RAS→column address delay time	t_{RAD}	15	–	1.5	45	0.5	20	0.5	25
<Read-cycle parameters>									
#RAS access time	t_{RAC}	–	60	3.5	105	2.5	100	2.5	125
#CAS access time	t_{CAC}	–	15	1.5	45	1.5	60	1.5	75
Address access time	t_{AA}	–	30	2.0	60	2.0	80	2.0	100
#OE access time	t_{OAC}	–	15	3.5	105	2.5	100	2.5	125
Output buffer turn-off time	t_{OFF}	0	15	2	60	2	80	1	50
<Write-cycle parameters>									
Data input hold time	t_{DH}	10	–	1.5	45	1.5	60	1.5	75
<Fast-page mode>									
Fast-page mode cycle time	t_{PC}	40	–	2.0	60	2.0	80	2.0	100
Fast-page mode #CAS precharge time	t_{CP}	10	–	0.5	15	0.5	20	0.5	25
Access time after #CAS precharge	t_{ACP}	–	35	2.0	60	2.0	80	2.0	100
<Refresh cycle>									
#CAS setup time	t_{CSR}	10	–	1.0	30	1.0	40	1.0	50
#CAS hold time	t_{CHR}	10	–	2.5	75	1.5	60	1.5	75
#RAS precharge→#CAS hold time	t_{PPC}	10	–	1.0	30	1.0	40	1.0	50
#RAS pulse width (only in refresh cycle)	t_{RAS}	60	10000	3.0	90	2.0	80	2.0	100

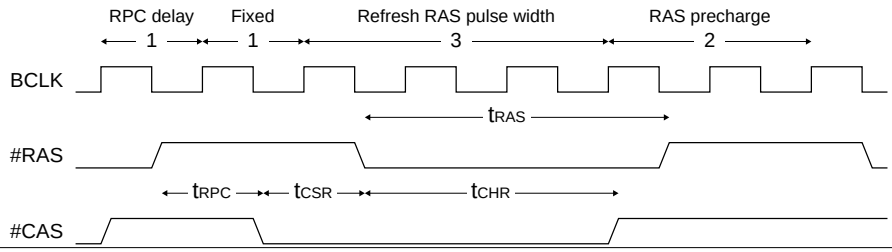
DRAM: 60ns, CPU: 33MHz, random read/write cycle



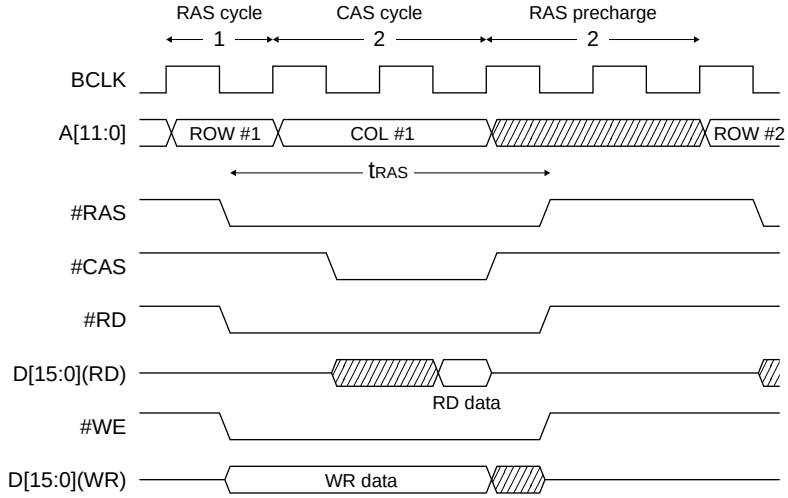
DRAM: 60ns, CPU: 33MHz, page-mode read/write cycle



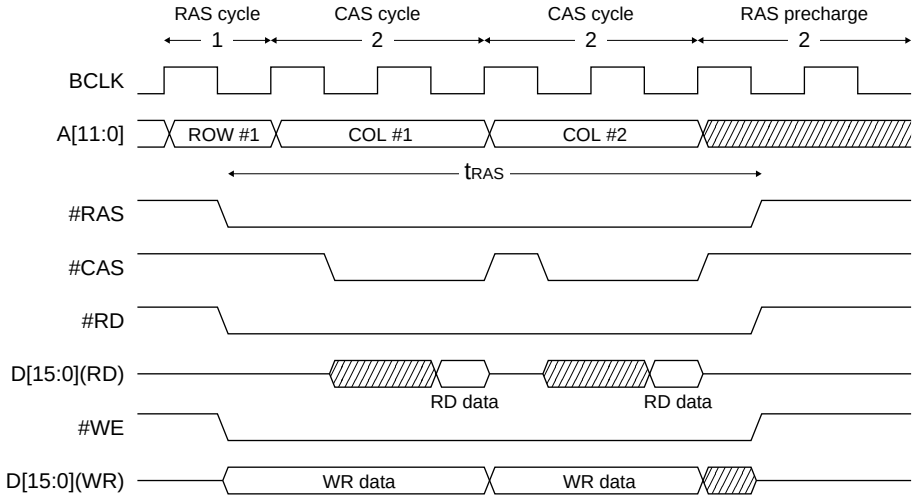
DRAM: 60ns, CPU: 33MHz, CAS-before-RAS refresh cycle



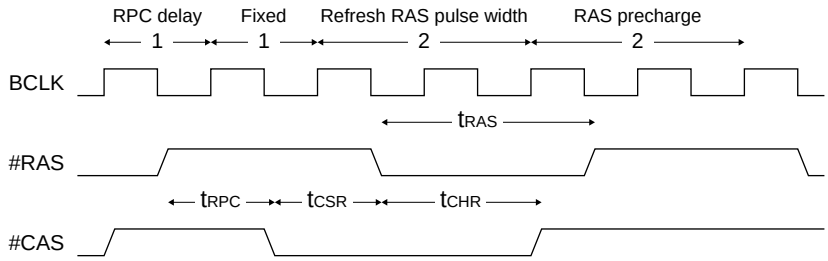
DRAM: 60ns, CPU: 25MHz, random read/write cycle



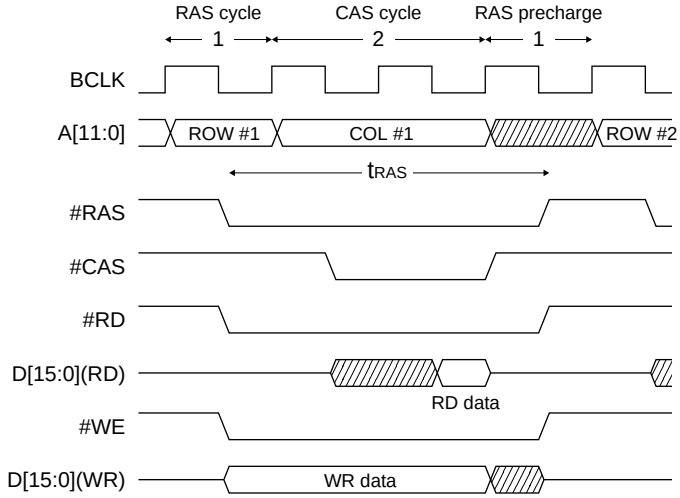
DRAM: 60ns, CPU: 25MHz, page-mode read/write cycle



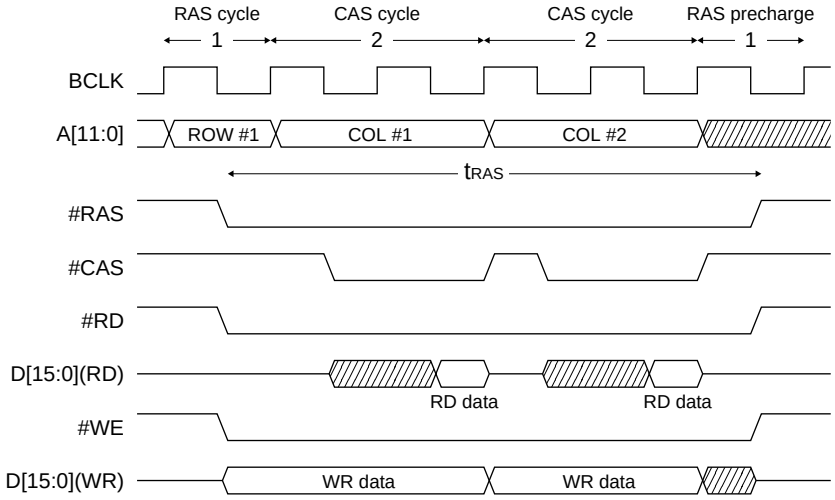
DRAM: 60ns, CPU: 25MHz, CAS-before-RAS refresh cycle



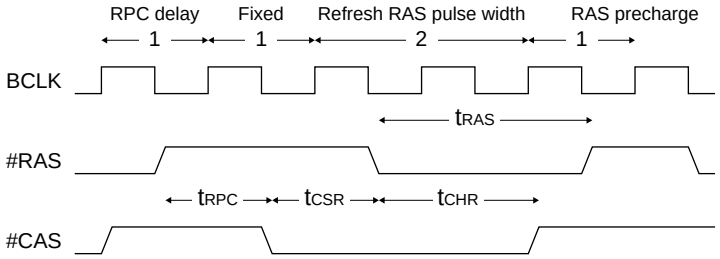
DRAM: 60ns, CPU: 20MHz, random read/write cycle



DRAM: 60ns, CPU: 20MHz, page-mode read/write cycle



DRAM: 60ns, CPU: 20MHz, CAS-before-RAS refresh cycle



A.3 ROM and Burst ROM

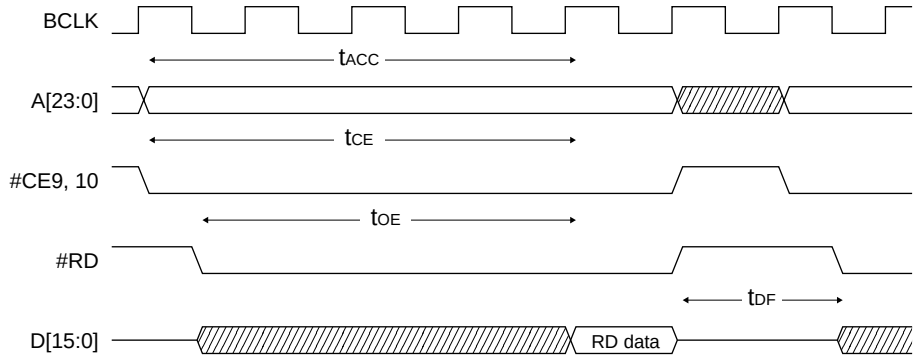
Burst ROM and mask ROM interface setup examples

Operating frequency	Normal read cycle		Burst read cycle		Output disable delay cycle
	Wait cycle	Read cycle	Wait cycle	Read cycle	
20MHz	2	3	1	2	1.5
25MHz	3	4	1	2	1.5
33MHz	4	5	2	3	1.5

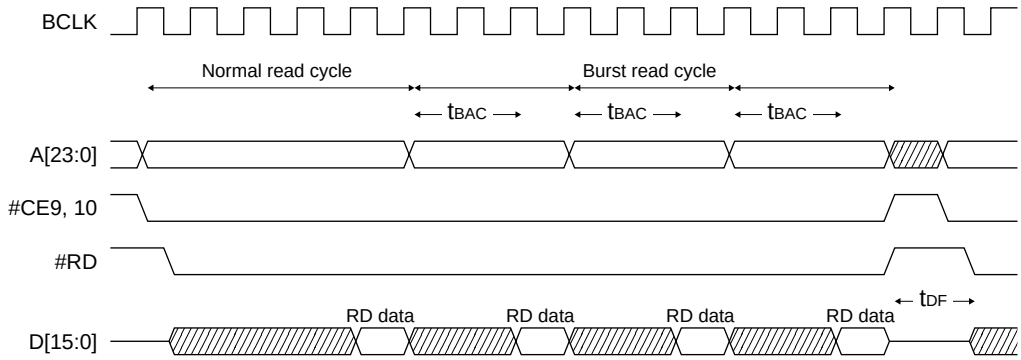
Burst ROM and mask ROM interface timing

Burst ROM and mask ROM interface				33MHz		25MHz		20MHz	
Parameter	Symbol	Min.	Max.	Cycle	Time	Cycle	Time	Cycle	Time
Access time	t_{ACC}	–	100	5	150	4	160	3	150
#CE output delay time	t_{CE}	–	100	5	150	4	160	3	150
#OE output delay time	t_{OE}	–	50	4.5	135	3.5	140	2.5	125
Burst access time	t_{BAC}	–	50	3	90	2	80	2	100
Output disable delay time	t_{DF}	0	40	1.5	45	1.5	60	1.5	75

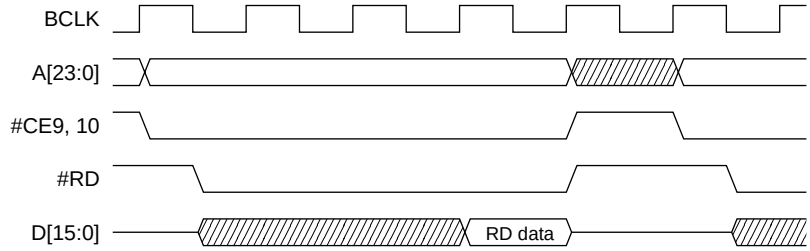
ROM: 100ns, CPU: 33MHz, normal read



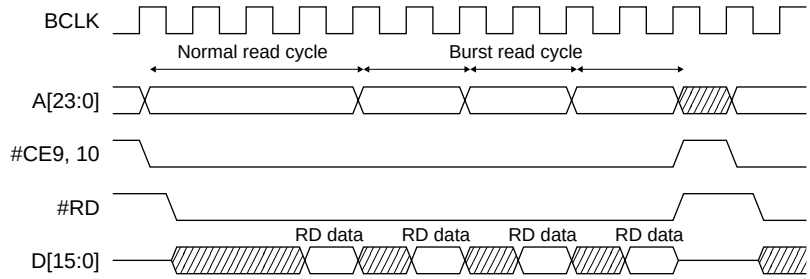
ROM: 100ns, CPU: 33MHz, burst read



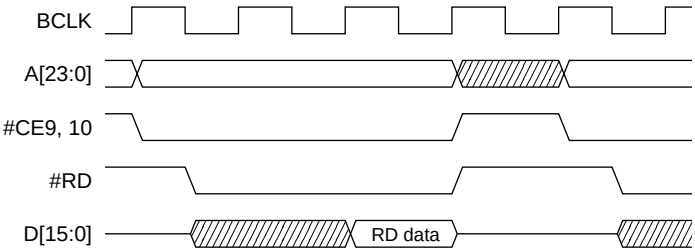
ROM: 100ns, CPU: 25MHz, normal read



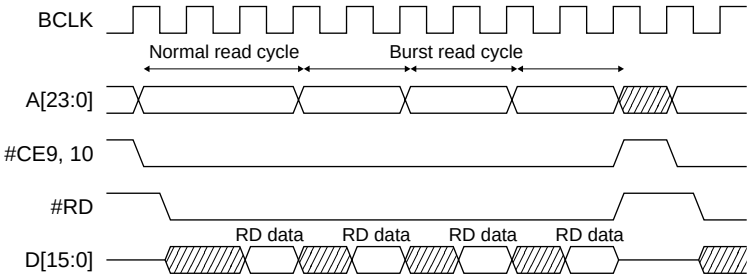
ROM: 100ns, CPU: 25MHz, burst read



ROM: 100ns, CPU: 20MHz, normal read



ROM: 100ns, CPU: 20MHz, burst read



A.4 SRAM (55ns)

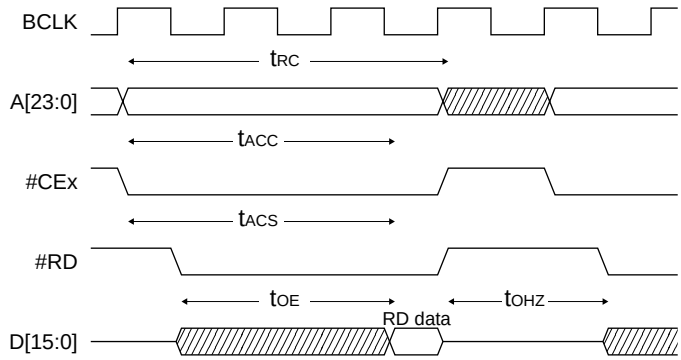
SRAM interface setup examples – 55ns

Operating frequency	Read cycle		Write cycle	Output disable delay time
	Wait cycle	Read cycle		
20MHz	1	2	2	1.5
25MHz	2	3	3	1.5
33MHz	2	3	3	1.5

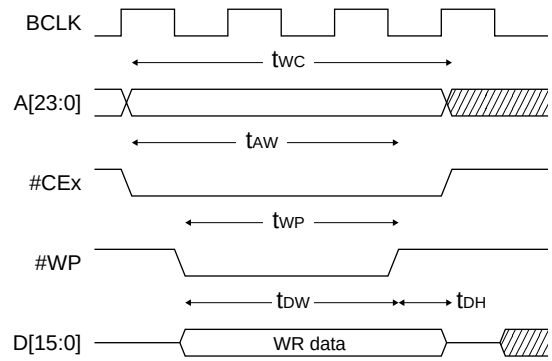
SRAM interface timing – 55ns

SRAM interface				33MHz		25MHz		20MHz	
Parameter	Symbol	Min.	Max.	Cycle	Time	Cycle	Time	Cycle	Time
<Read cycle>									
Read cycle time	t_{RC}	55	–	3	90	3	120	2	100
Address access time	t_{ACC}	–	55	3	90	3	120	2	100
#CE access time	t_{ACS}	–	55	3	90	3	120	2	100
#OE access time	t_{OE}	–	30	2.5	75	2.5	100	1.5	75
Output disable delay time	t_{OHZ}	0	30	1.5	45	1.5	60	1.5	75
<Write cycle>									
Write cycle time	t_{WC}	55	–	3	90	3	120	2	100
Address enable time	t_{AW}	50	–	2.5	75	2.5	100	1.5	75
Write pulse width	t_{WP}	45	–	2	60	2	80	1	50
Input data setup time	t_{DW}	30	–	2	60	2	80	1	50
Input data hold time	t_{DH}	0	–	0.5	15	0.5	20	0.5	25

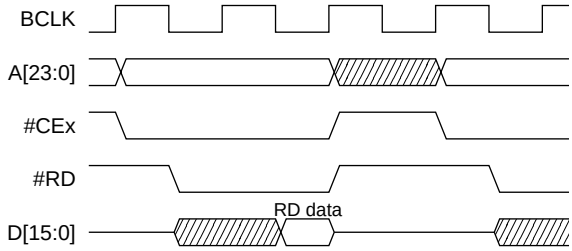
SRAM: 55ns, CPU: 33/25MHz, read cycle



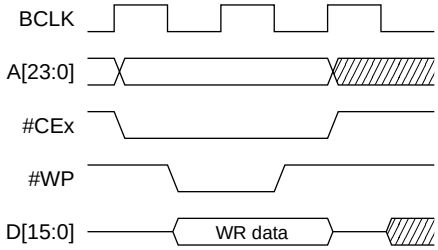
SRAM: 55ns, CPU: 33/25MHz, write cycle



SRAM: 55ns, CPU: 20MHz, read cycle



SRAM: 55ns, CPU: 20MHz, write cycle



A.5 SRAM (70ns)

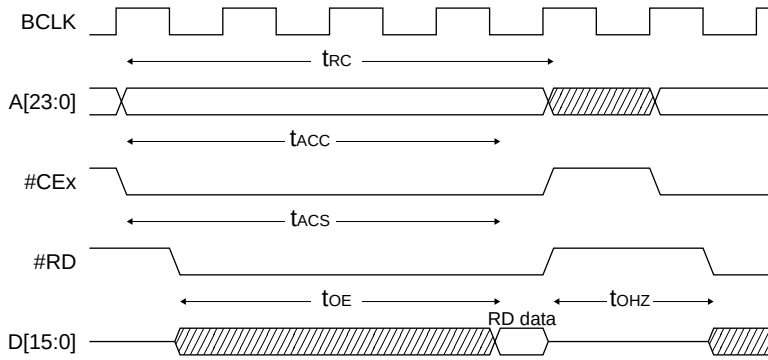
SRAM interface setup examples – 70ns

Operating frequency	Read cycle		Write cycle	Output disable delay time
	Wait cycle	Read cycle		
20MHz	2	3	3	1.5
25MHz	2	3	3	1.5
33MHz	3	4	4	1.5

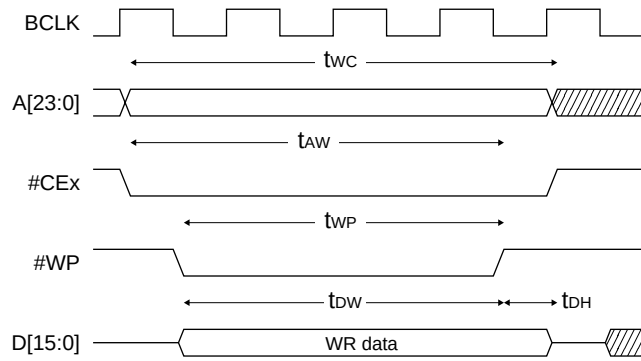
SRAM interface timing – 70ns

SRAM interface				33MHz		25MHz		20MHz	
Parameter	Symbol	Min.	Max.	Cycle	Time	Cycle	Time	Cycle	Time
<Read cycle>									
Read cycle time	t_{RC}	70	–	4	120	3	120	3	150
Address access time	t_{ACC}	–	70	4	120	3	120	3	150
#CE access time	t_{ACS}	–	70	4	120	3	120	3	150
#OE access time	t_{OE}	–	40	3.5	105	2.5	100	2.5	125
Output disable delay time	t_{OHZ}	0	30	1.5	45	1.5	60	1.5	75
<Write cycle>									
Write cycle time	t_{WC}	70	–	4	120	3	120	3	150
Address enable time	t_{AW}	60	–	3.5	105	2.5	100	2.5	125
Write pulse width	t_{WP}	55	–	3	90	2	80	2	100
Input data setup time	t_{DW}	30	–	3	90	2	80	2	100
Input data hold time	t_{DH}	0	–	0.5	15	0.5	20	0.5	25

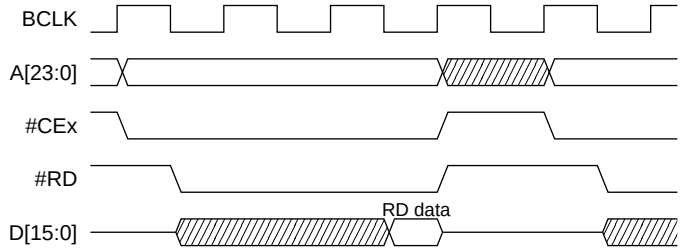
SRAM: 70ns, CPU: 33MHz, read cycle



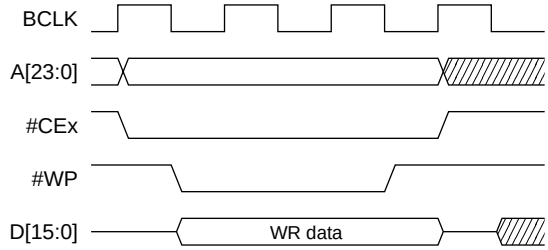
SRAM: 70ns, CPU: 33MHz, write cycle



SRAM: 70ns, CPU: 25/20MHz, read cycle



SRAM: 70ns, CPU: 25/20MHz, write cycle



A.6 8255A

8255A interface setup examples

Operating frequency	Read cycle		Write cycle	Output disable delay time
	Wait cycle	Read cycle		
20MHz	9 ∗1	10	10	3.5
25MHz	11	12	12	3.5
33MHz	14	15	15	3.5 ∗2

8255A interface timing

SRAM interface				33MHz		25MHz		20MHz	
Parameter	Symbol	Min.	Max.	Cycle	Time	Cycle	Time	Cycle	Time
<Read cycle>									
Read cycle time	t_{RC}	300	–	15	450	12	480	10	500
Address access time	t_{ACC}	–	250	15	450	12	480	10	500
#CE access time	t_{ACS}	–	250	15	450	12	480	10	500
#OE access time	t_{OE}	–	250	14.5	435	11.5	460	9.5	475
Output disable delay time	t_{OHZ}	10	150	3.5	105	3.5	140	3.5	175
<Write cycle>									
Write cycle time	t_{WC}	430	–	15	450	12	480	10	500
Address enable time	t_{AW}	400	–	14.5	435	11.5	460	9.5	475
Write pulse width	t_{WP}	400	–	14	420	11	440	9	450
Input data setup time	t_{DW}	100	–	14	420	11	440	9	450
Input data hold time ∗3	t_{DH}	30	–	0.5	15	0.5	20	0.5	25

∗1 The E0C332L01 enables up to 7 cycles of wait-cycle insertion. If a number of wait cycles more than 7 cycles needs to be inserted, input the #WAIT signal from external hardware. Note that the interface must be set for SRAM type devices to insert wait cycles using the #WAIT pin. (Refer to "BCU (Bus Control Unit)" in the "C33 ASIC Macro Manual", for more information.)

∗2 This setting cannot satisfy the 150 ns of output-disable delay time specification required for the 8255A. When implementing such a low-speed device in the system, the external bus must be separated by inserting a 3-state bus buffer at the output side (when viewed from the CPU) of the external system bus.

∗3 If the data hold time that can be set is sufficient for the device, secure it by connecting a bus repeater to the external data bus D[15:0] or by inserting a latch at the output side of the external system interface.

Appendix B Pin Characteristics

Pin No.	Signal name	I/O cell name	Characteristic		Pull-up /down	Power supply	Remarks
			Input	Output			
1	A23	XHBC1T	note 1	Type1		V_{DDE1}	
2	A22	XHBC1T	note 1	Type1		V_{DDE1}	
3	A21	XHBC1T	note 1	Type1		V_{DDE1}	
4	A20	XHBC1T	note 1	Type1		V_{DDE1}	
5	V_{DDE1}	XHVDD					
6	A19	XHBC1T	note 1	Type1		V_{DDE1}	
7	A18	XHBC1T	note 1	Type1		V_{DDE1}	
8	A17	XHBC1T	note 1	Type1		V_{DDE1}	
9	A16	XHBC1T	note 1	Type1		V_{DDE1}	
10	A15	XHBC1T	note 1	Type1		V_{DDE1}	
11	V_{SS}	XVSS					
12	A14	XHBC1T	note 1	Type1		V_{DDE1}	
13	A13	XHBC1T	note 1	Type1		V_{DDE1}	
14	A12	XHBC1T	note 1	Type1		V_{DDE1}	
15	A11	XHBC1T	note 1	Type1		V_{DDE1}	
16	A10	XHBC1T	note 1	Type1		V_{DDE1}	
17	V_{DD}	XLVDD					
18	A9	XHBC1T	note 1	Type1		V_{DDE1}	
19	A8	XHBC1T	note 1	Type1		V_{DDE1}	
20	A7	XHBC1T	note 1	Type1		V_{DDE1}	
21	A6	XHBC1T	note 1	Type1		V_{DDE1}	
22	A5	XHBC1T	note 1	Type1		V_{DDE1}	
23	V_{SS}	XVSS					
24	A4	XHBC1T	note 1	Type1		V_{DDE1}	
25	A3	XHBC1T	note 1	Type1		V_{DDE1}	
26	A2	XHBC1T	note 1	Type1		V_{DDE1}	
27	A1	XHBC1T	note 1	Type1		V_{DDE1}	
28	A0/#BSL	XHBC1T	note 1	Type1		V_{DDE1}	
29	V_{DDE1}	XHVDD					
30	D15	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
31	D14	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
32	D13	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
33	D12	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
34	D11	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
35	V_{SS}	XVSS					
36	D10	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
37	D9	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
38	D8	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
39	D7	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
40	D6	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
41	V_{DD}	XLVDD					
42	D5	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
43	D4	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
44	D3	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
45	D2	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
46	D1	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
47	D0	XHBC1T	CMOS/LVTTL	Type1		V_{DDE1}	
48	V_{SS}	XVSS					
49	BCLK	XHTB1T		Type1		V_{DDE1}	
50	#EMEMRD	XHTB1T		Type1		V_{DDE1}	

Pin No.	Signal name	I/O cell name	Characteristic		Pull-up /down	Power supply	Remarks
			Input	Output			
51	#RD	XHBC1T	note 1	Type1		V_{DDE1}	
52	#WRL/#WR/#WE	XHBC1T	note 1	Type1		V_{DDE1}	
53	#WRH/#BSH	XHBC1T	note 1	Type1		V_{DDE1}	
54	V_{DDE1}	XHVDD					
55	#CE10EX/#CE9&10EX	XHBC1T	note 1	Type1		V_{DDE1}	
56	#CE10IN	XHTB1T		Type1		V_{DDE1}	
57	#CE3	XHTB1T		Type1		V_{DDE1}	
58	V_{SS}	XVSS					
59	K67/AD7	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
60	K66/AD6	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
61	K65/AD5	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
62	AV_{DDE}	XHVDD					
63	K64/AD4	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
64	K63/AD3	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
65	K62/AD2	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
66	V_{SS}	XVSS					
67	K61/AD1	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
68	K60/AD0	XHIBCLIN	CMOS/LVTTL			AV_{DDE}	note 2
69	K54/#DMAREQ3	XHIBHP2	CMOS/LVTTL SCHMITT		Pull-up	V_{DDE1}	
70	K53/#DMAREQ2	XHIBHP2	CMOS/LVTTL SCHMITT		Pull-up	V_{DDE1}	
71	K52/#ADTRG	XHIBHP2	CMOS/LVTTL SCHMITT		Pull-up	V_{DDE1}	
72	V_{DD}	XLVDD					
73	K51/#DMAREQ1	XHIBHP2	CMOS/LVTTL SCHMITT		Pull-up	V_{DDE1}	
74	K50/#DMAREQ0	XHIBHP2	CMOS/LVTTL SCHMITT		Pull-up	AV_{DDE}	
75	#LCAS	XHTB1T		Type1		V_{DDE1}	
76	#HCAS	XHTB1T		Type1		V_{DDE1}	
77	#CE9/#CE17/#CE17&18	XHBC1T	note 1	Type1		V_{DDE1}	
78	V_{SS}	XVSS					
79	#CE8/#RAS1/#CE14/#RAS3	XHBC1T	note 1	Type1		V_{DDE1}	
80	#CE7/#RAS0/#CE13/#RAS2	XHBC1T	note 1	Type1		V_{DDE1}	
81	#CE5/#CE15/#CE15&16	XHBC1T	note 1	Type1		V_{DDE1}	
82	#CE4/#CE11/#CE11&12	XHBC1T	note 1	Type1		V_{DDE1}	
83	#CE6/#CE7&8	XHBC1T	note 1	Type1		V_{DDE1}	
84	V_{DDE1}	XHVDD					
90	V_{SS}	XVSS					
91	GPIO0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE2}	
92	FPDAT11/GPIO4/INVERSE	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
93	FPDAT10/GPIO3	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
94	FPDAT9/GPIO2	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
95	V_{DDE2}	XHVDD					
96	FPDAT8/GPIO1	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
97	FPSHIFT	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
98	FPDAT7	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
99	FPDAT6	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
100	FPDAT5	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
101	V_{DD}	XLVDD					
102	FPDAT4	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
103	FPDAT3	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
104	FPDAT2	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
105	FPDAT1	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
106	V_{SS}	XVSS					
107	FPDAT0	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
108	FPLINE	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
109	FPFRAME	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	
110	DRDY/MOD/FPSHIFT2	XHBC3BT	CMOS/LVTTL	Type3		V_{DDE2}	

Pin No.	Signal name	I/O cell name	Characteristic		Pull-up /down	Power supply	Remarks
			Input	Output			
111	V_{DDE2}	XHVDD					
112	LCDPWR	XHTB1T		Type1		V_{DDE2}	
118	V_{SS}	XVSS					
119	P35/#BUSACK	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
120	P34/#BUSREQ/#CE6	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
121	P33/#DMAACK1	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
122	P32/#DMAACK0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
123	P31/#BUSGET/#GARD	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
124	P30/#WAIT/#CE4&5	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
125	V_{DD}	XLVDD					
126	P27/TM5	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
127	P26/TM4	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
128	P25/TM3	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
129	P24/TM2	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
130	P23/TM1	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
131	V_{SS}	XVSS					
132	P22/TM0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
133	P21/#DWE/#GAAS	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
134	P20/#DRD	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
135	P16/EXCL5/#DMAEND1	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
136	P15/EXCL4/#DMAEND0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
137	V_{DDE1}	XHVDD					
138	P14/FOSC1/DCLK	XLBH2T	CMOS/LVTTL SCHMITT	Type2		V_{DD}	note 3
139	P13/EXCL3/T8UF3/DPCO	XLBH2T	CMOS/LVTTL SCHMITT	Type2		V_{DD}	note 3
140	P12/EXCL2/T8UF2/DST2	XLBH2T	CMOS/LVTTL SCHMITT	Type2		V_{DD}	note 3
141	P11/EXCL1/T8UF1/DST1	XLBH2T	CMOS/LVTTL SCHMITT	Type2		V_{DD}	note 3
142	P10/EXCL0/T8UF0/DST0	XLBH2T	CMOS/LVTTL SCHMITT	Type2		V_{DD}	note 3
143	V_{SS}	XVSS					
144	P07/#SRDY1/#DMAEND3	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
145	P06/#SCLK1/#DMAACK3	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
146	P05/SOUT1/#DMAEND2	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
147	P04/SIN1/#DMAACK2	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
148	V_{DD}	XLVDD					
149	OSC2	XLLOT				V_{DD}	
150	OSC1	XLLIN				V_{DD}	note 3
151	V_{SS}	XVSS					
152	P03/#SRDY0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
153	P02/#SCLK0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
154	P01/SOUT0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
155	P00/SIN0	XHBH1T	CMOS/LVTTL SCHMITT	Type1		V_{DDE1}	
156	CNF3	XHIBC	CMOS/LVTTL			V_{DDE1}	
157	CKSEL2	XHIBC	CMOS/LVTTL			V_{DDE1}	
158	CKSEL1	XHIBC	CMOS/LVTTL			V_{DDE1}	
159	CKSEL0	XHIBC	CMOS/LVTTL			V_{DDE1}	
160	V_{DDE1}	XHVDD					
161	CLKI	XHIBC	CMOS/LVTTL			V_{DDE1}	
162	ICEMD	XITST1			Pull-down		Test pin
163	V_{SS}	XVSS					
164	OSC4	XLLOT				V_{DD}	
165	OSC3	XLLIN				V_{DD}	note 3
166	EA10MD1	XHIBCP2	CMOS/LVTTL		Pull-up	V_{DDE1}	
167	EA10MD0	XHIBC	CMOS/LVTTL			V_{DDE1}	
168	#X2SPD	XHIBC	CMOS/LVTTL			V_{DDE1}	
169	V_{DD}	XLVDD					

Pin No.	Signal name	I/O cell name	Characteristic		Pull-up /down	Power supply	Remarks
			Input	Output			
170	PLLS1	XHIBC	CMOS/LVTTL			V_{DDE1}	
171	PLLS0	XHIBC	CMOS/LVTTL			V_{DDE1}	
172	#NMI	XHIBHP2	CMOS/LVTTL SCHMITT		Pull-up	V_{DDE1}	
173	V_{SS}	XVSS					
174	PLLC	XLLIN					
175	#RESET	XHIBHP2	CMOS/LVTTL SCHMITT		Pull-up	V_{DDE1}	
176	DSIO	XLBH2P2T	CMOS/LVTTL SCHMITT	Type2	Pull-up	V_{DD}	note 3

note 1) This pin is set as an input pin during device testing. Normally it is an output pin.
note 2) The voltage applied to this pin must be $0V \leq V_{IN} \leq AV_{DDE}$.
Note that the input voltage range for the K50 pin differs from other K5 pins.
note 3) The voltage applied to this pin must be $0V \leq V_{IN} \leq V_{DD}$.

The following table lists output current characteristics.

Output current (I_{OL}/I_{OH})

	5.0 V	3.3 V	2.0 V
Type1	3 mA	2 mA	0.6 mA
Type2	–	6 mA	2 mA
Type3	12 mA	12 mA	4 mA

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

- SALES OFFICES -

West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

- GERMANY -
SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0 Fax: +49-(0)2171-5045-10

- UNITED KINGDOM -
UK BRANCH OFFICE
Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

- FRANCE -
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

ASIA

- CHINA -
EPSON (CHINA) CO., LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107319

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

- HONG KONG, CHINA -
EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

- TAIWAN -
EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei, TAIWAN
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN
Phone: 03-573-9900 Fax: 03-573-9169

- SINGAPORE -
EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

- KOREA -
SEIKO EPSON CORPORATION KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

- JAPAN -
SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

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