**EPSON**

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

# E0C6003 TECHNICAL MANUAL

## E0C6003 Technical Hardware

ENERGY
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**SEIKO EPSON CORPORATION**

# CONTENTS

# CHAPTER 1 INTRODUCTION

The E0C6003 Series single-chip microcomputer features an E0C6200B CMOS 4-bit CPU as the core. It contains a 768 (words) × 12 (bits) ROM, 64 (words) × 4 (bits) RAM, LCD driver , 4-bit input port (K00–K03), 4-bit output port (R00–R03) and a timer.
The E0C6003 Series is configured as follows, depending on the supply voltage.

**E0C6003:**   3.0 V (1.8 to 3.6 V)
**E0C60L03:**   1.5 V (1.2 to 2.0 V)

## 1.1 Features

**Core CPU** ........................................... E0C6200B

**Built-in oscillation circuit** ............. Crystal 32.768 kHz (Typ.) or CR oscillation circuit 65 kHz (Typ.)

**Instruction set** ................................... 100 instructions

**ROM capacity** ................................... 768 words × 12 bits

**RAM capacity** ................................... 64 words × 4 bits

**Input port** .......................................... 4 bits   (pull-down resistors are available by mask option)

**Output ports** ..................................... 4 bits   (clock and buzzer outputs are possible by mask option)

**LCD driver** ........................................ 15 segments × 4, 3 or 2 commons
(1/4, 1/3 or 1/2 duty are selectable by mask option)

**Timer** .................................................. 1 system (clock timer) built-in

**Interrupt** ........................................... External:  Input port interrupt     1 system
Internal:   Timer interrupt          1 system

**Supply voltage** ................................. 1.5 V (1.2 to 2.0 V)  E0C60L03
3.0 V (1.8 to 3.6 V)  E0C6003

**Current consumption (Typ.)** ......... During HALT:        1.0 $\mu$A (32 kHz crystal, with power divider OFF)
During execution:  2.5 $\mu$A (32 kHz crystal, with power divider OFF)
15 $\mu$A  (32 kHz crystal, with power divider ON)

**Supply form** ..................................... Chip

## *1.2  Block Diagram*
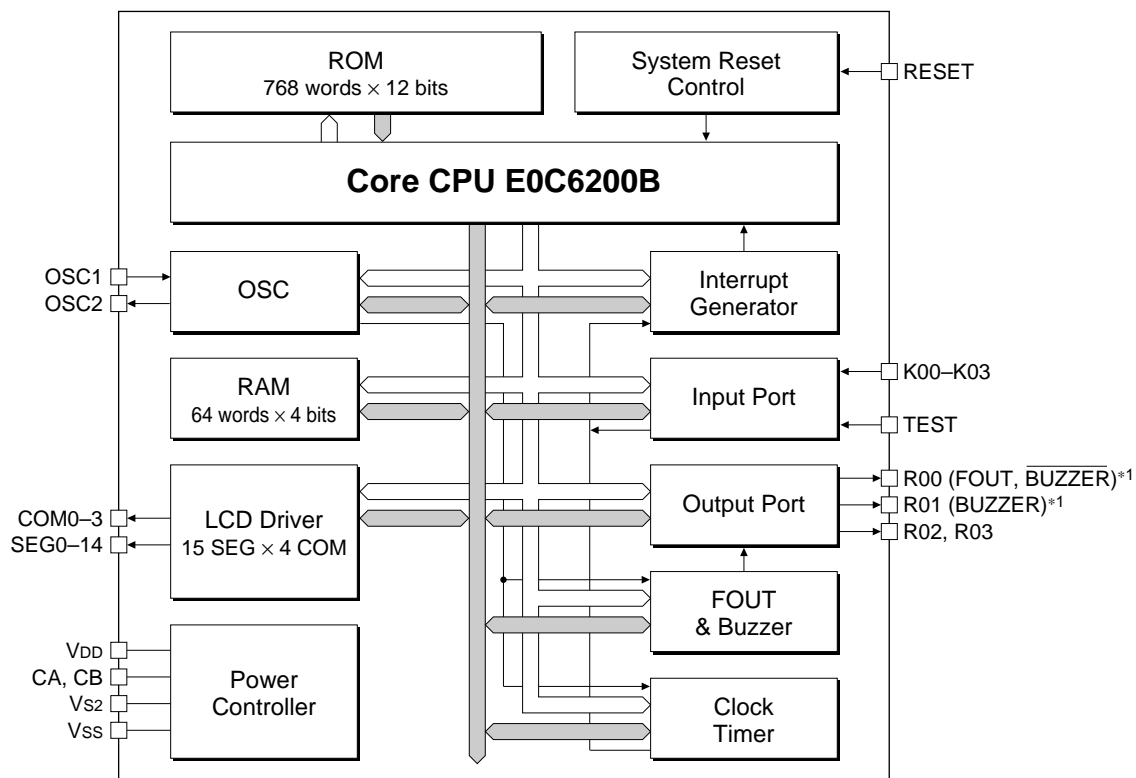


∗1: Terminal specifications can be selected by mask option.

*Fig. 1.2.1  E0C6003 block diagram*

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## 1.3   Pad Layout

### 1.3.1 Pad layout diagram
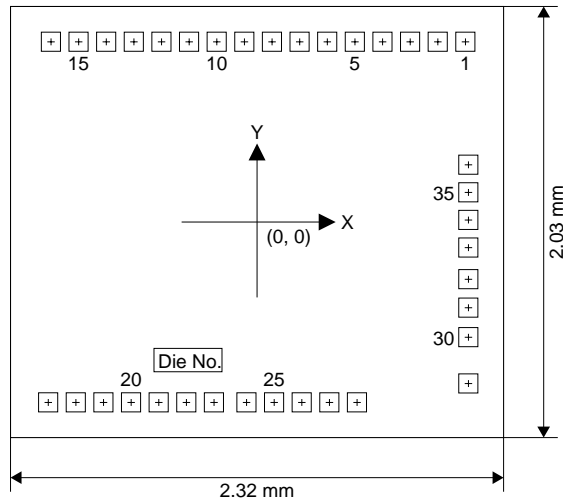


*Fig. 1.3.1.1  Pad layout*

Chip thickness:  400 $\mu$m
Pad opening:      95 $\mu$m

### 1.3.2 Pad coordinates

*Table 1.3.2.1  Pad coordinates (unit: μm)*

| No. | Pad name | X | Y | No. | Pad name | X | Y | No. | Pad name | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | TEST | 980 | 849 | 13 | SEG3 | -580 | 849 | 25 | OSC2 | 80 | -849 |
| 2 | SEG14 | 850 | 849 | 14 | SEG2 | -710 | 849 | 26 | OSC1 | 210 | -849 |
| 3 | SEG13 | 720 | 849 | 15 | SEG1 | -840 | 849 | 27 | V$_{DD}$ | 340 | -849 |
| 4 | SEG12 | 590 | 849 | 16 | SEG0 | -970 | 849 | 28 | RESET | 470 | -849 |
| 5 | SEG11 | 460 | 849 | 17 | COM0 | -983 | -849 | 29 | R00 | 994 | -760 |
| 6 | SEG10 | 330 | 849 | 18 | COM1 | -853 | -849 | 30 | R01 | 994 | -542 |
| 7 | SEG9 | 200 | 849 | 19 | COM2 | -723 | -849 | 31 | R02 | 994 | -403 |
| 8 | SEG8 | 70 | 849 | 20 | COM3 | -593 | -849 | 32 | R03 | 994 | -269 |
| 9 | SEG7 | -60 | 849 | 21 | CA | -463 | -849 | 33 | K00 | 994 | -120 |
| 10 | SEG6 | -190 | 849 | 22 | CB | -333 | -849 | 34 | K01 | 994 | 10 |
| 11 | SEG5 | -320 | 849 | 23 | V$_{S2}$ | -203 | -849 | 35 | K02 | 994 | 140 |
| 12 | SEG4 | -450 | 849 | 24 | V$_{SS}$ | -50 | -849 | 36 | K03 | 994 | 270 |

## 1.4   Pad Description

*Table 1.4.1  Pan description*

| Pad name | Pad No. | I/O | Function |
|---|---|---|---|
| V$_{DD}$ | 27 | (I) | Power supply terminal (+) |
| V$_{SS}$ | 24 | (I) | Power supply terminal (-) |
| V$_{S2}$ | 23 | O | LCD system voltage doubler (2·Vss)/halver (Vss/2) output |
| CA, CB | 21, 22 | – | Booster capacitor connecting terminal |
| OSC1 | 26 | I | Crystal or CR oscillation input terminal * |
| OSC2 | 25 | O | Crystal or CR oscillation output terminal * |
| K00–03 | 33–36 | I | Input port terminal |
| R00 | 29 | O | Output port terminal, $\overline{\text{BUZZER}}$ or FOUT output terminal * |
| R01 | 30 | O | Output port terminal or BUZZER output terminal * |
| R02, R03 | 31, 32 | O | Output port terminal |
| SEG0–14 | 2–16 | O | LCD segment output or DC output terminal * |
| COM0–3 | 17–20 | O | LCD common output terminal (1/4, 1/3 or 1/2 duty are selectable *) |
| RESET | 28 | I | Initial reset input terminal |
| TEST | 1 | I | Test input terminal |

∗ Can be selected by mask option

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# CHAPTER 2   POWER SUPPLY AND INITIAL RESET

## 2.1  Power Supply

With a single external power supply (∗) supplied to $V_{DD}$ through $V_{SS}$, the E0C6003 Series generates the necessary internal voltages with the voltage doubler/halver and power divider.

∗ Supply voltage: E0C6003 ... 3.0 V    E0C60L03 ... 1.5 V

Figure 2.1.1 shows the basic configuration of the power divider and voltage doubler/halver.
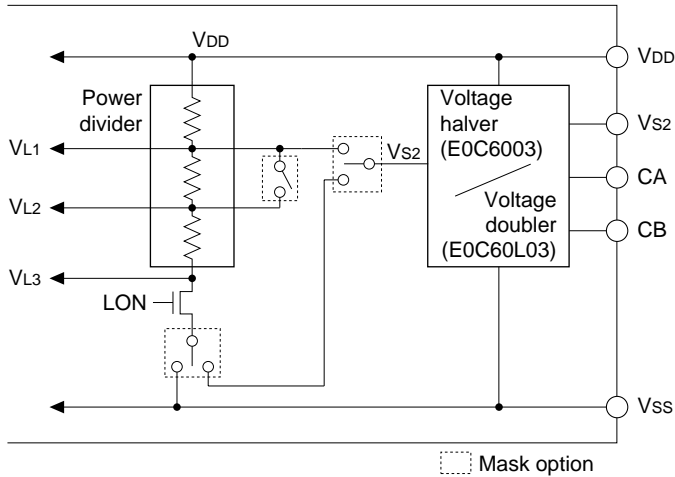


*Fig. 2.1.1  Basic configuration of the power divider and voltage doubler/halver*

The power divider and voltage doubler/halver generate the LCD drive voltage ($V_{L1}$, $V_{L2}$, $V_{L3}$). The circuit is configured according to the model and the LCD drive bias selected by mask option. The LCD drive bias can be selected from 1/3 bias, 1/2 bias (A) and 1/2 bias (B).

### For E0C6003

When 1/3 bias or 1/2 bias (A) is selected, the power divider is used to generate $V_{L1}$ and $V_{L2}$ by dividing the source voltage with the resistors. The voltage doubler/halver is not used. In the E0C6003, this selection can reduce the external component count.
When 1/2 bias (B) is selected in the E0C6003, the voltage halver is used to generate $V_{L1}$ and $V_{L2}$ and the power divider is disconnected. This selection can reduce current consumption, but two external capacitors are necessary for the voltage halver.
In the E0C6003, the voltage doubler is not used.
Figure 2.1.2 shows the power circuit configuration of the E0C6003 according to the selected mask option.

### For E0C60L03

The E0C60L03 always uses the voltage doubler to generate the LCD drive voltage from 1.5 V source voltage. The voltage halver is not used.
When 1/3 bias or 1/2 bias (A) is selected, the power divider is used to generate $V_{L1}$ and $V_{L2}$ by dividing the $V_{S2}$ voltage generated by the voltage doubler.
When 1/2 bias (B) is selected in the E0C60L03, the power divider is not used.
Figure 2.1.3 shows the power circuit configuration of the E0C60L03 according to the selected mask option.

## E0C6003

3 V LCD Panel
1/4, 1/3 or 1/2 duty, 1/3 bias
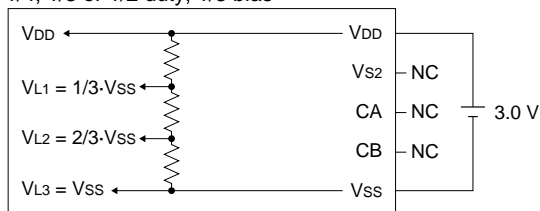


Note: $V_{L3}$ is shorted to $V_{SS}$ internally.

3 V LCD Panel
1/4, 1/3 or 1/2 duty, 1/2 bias (A)
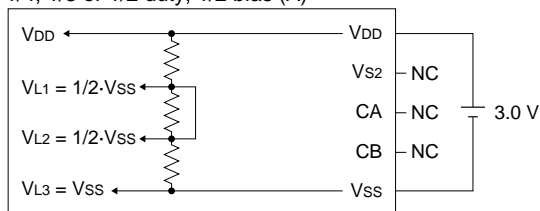


Note: $V_{L3}$–$V_{SS}$ and $V_{L1}$–$V_{L2}$ are shorted internally.

3 V LCD Panel
1/4, 1/3 or 1/2 duty, 1/2 bias (B)
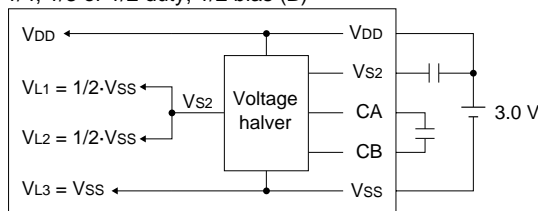


Note: $V_{L3}$–$V_{SS}$ and $V_{L1}$–$V_{L2}$ are shorted internally.

*Fig. 2.1.2  Power circuit configuration of E0C6003*

## E0C60L03

3 V LCD Panel
1/4, 1/3 or 1/2 duty, 1/3 bias
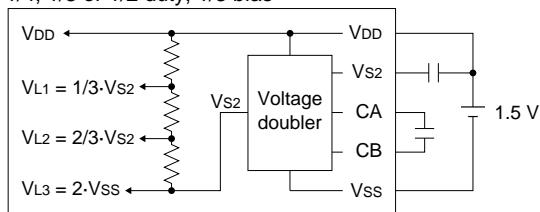


Note: $V_{L3}$ is shorted to $V_{S2}$ internally.

3 V LCD Panel
1/4, 1/3 or 1/2 duty, 1/2 bias (A)
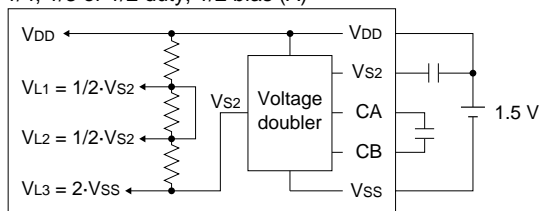


Note: $V_{L3}$–$V_{S2}$ and $V_{L1}$–$V_{L2}$ are shorted internally.

3 V LCD Panel
1/4, 1/3 or 1/2 duty, 1/2 bias (B)
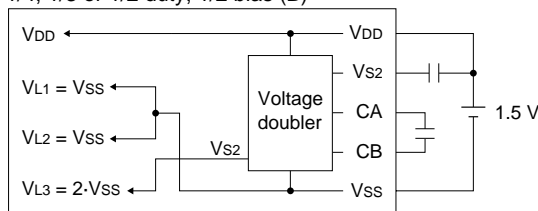


Note: $V_{L3}$–$V_{S2}$ and $V_{L1}$–$V_{L2}$ are shorted internally.

*Fig. 2.1.3  Power circuit configuration of E0C60L03*

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## 2.2 Initial Reset

To initialize the E0C6003 Series circuits, an initial reset must be executed. There are three ways of doing this.

(1) Initial reset by the oscillation detection circuit (Note)
(2) External initial reset via the RESET terminal
(3) External initial reset by simultaneous high input to K00–K03 (depending on mask option)

Figure 2.2.1 shows the configuration of the initial reset circuit.
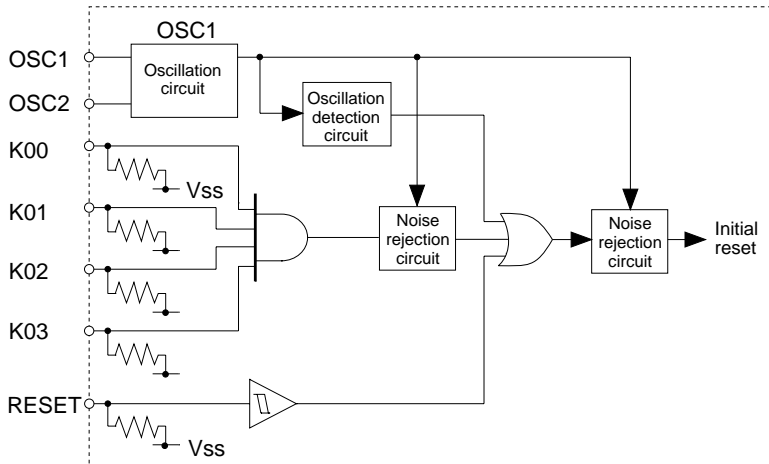


*Fig. 2.2.1  Configuration of initial reset circuit*

*Note:  Be sure to use reset function (2) or (3) at power-on because the initial reset function by the
oscillation detection circuit (1) may not operate normally depending on the power-on procedure.*

### 2.2.1 Oscillation detection circuit

The oscillation detection circuit outputs the initial reset signal at power-on until the oscillation circuit starts oscillating, or when the oscillation circuit stops oscillating for some reason.
However, use the following reset functions at power-on because the initial reset function by the oscillation detection circuit may not operate normally depending on the power-on procedure.

### 2.2.2 Reset terminal (RESET)

An initial reset can be invoked externally by making the reset terminal high. This high level must be maintained for at least 5 msec (when oscillating frequency fosc = 32 kHz), because the initial reset circuit contains a noise rejection circuit. When the reset terminal goes low the CPU begins to operate.

### 2.2.3 Simultaneous high input to input ports (K00–K03)

Another way of invoking an initial reset externally is to input a high signal simultaneously to the input ports (K00–K03) selected with the mask option. The specified input port terminals must be kept high for at least 4 sec (when oscillating frequency fosc = 32 kHz), because of the noise rejection circuit. Table 2.2.3.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

*Table 2.2.3.1  Input port combinations*

| A | Not used |
|---|---|
| B | K00*K01 |
| C | K00*K01*K02 |
| D | K00*K01*K02*K03 |

When, for instance, mask option D (K00*K01*K02*K03) is selected, an initial reset is executed when the signals input to the four ports K00–K03 are all high at the same time.
When this function is used, make sure that the specified ports do not go high at the same time during normal operation.

### *2.2.4 Internal register following initialization*

An initial reset initializes the CPU as shown in the table below.

*Table 2.2.4.1  Initial values*

| CPU Core | | | |
|---|---|---|---|
| Name | Symbol | Bit size | Initial value |
| Program counter step | PCS | 8 | 00H |
| Program counter page | PCP | 4 | 1H |
| New page pointer | NPP | 4 | 1H |
| Stack pointer | SP | 8 | Undefined |
| Index register X | X | 8 | Undefined |
| Index register Y | Y | 8 | Undefined |
| Register pointer | RP | 4 | Undefined |
| General-purpose register A | A | 4 | Undefined |
| General-purpose register B | B | 4 | Undefined |
| Interrupt flag | I | 1 | 0 |
| Decimal flag | D | 1 | 0 |
| Zero flag | Z | 1 | Undefined |
| Carry flag | C | 1 | Undefined |

| Peripheral Circuits | | |
|---|---|---|
| Name | Bit size | Initial value |
| RAM | $64 \times 4$ | Undefined |
| Display memory | $16 \times 4$ | Undefined |
| Other peripheral circuits | – | * |

∗ See Section 4.1, "Memory Map".

## 2.3   *Test Terminal (TEST)*

This terminal is used when IC is inspected for shipment. During normal operation connect it to V$_{SS}$.

# CHAPTER 3  CPU, ROM, RAM

## 3.1  CPU

The E0C6003 Series employs the E0C6200B core CPU, so that register configuration, instructions, and so forth are virtually identical to those in other processors in the family using the E0C6200/6200A/6200B. Refer to the "E0C6200/6200A Core CPU Manual" for details of the E0C6200B.

Note the following points with regard to the E0C6003 Series:

(1) Since the E0C6003 Series don't provides the SLEEP function, the SLP instruction can not be used.

(2) Because the ROM capacity is 768 words, 12 bits per word, bank bits are unnecessary, and PCB and NBP are not used.

(3) The RAM page is set to 0 only, so the page part (XP, YP) of the index register that specifies addresses is invalid.
    PUSH  XP      POP  XP      LD  XP,r      LD  r,XP
    PUSH  YP      POP  YP      LD  YP,r      LD  r,YP

## 3.2  ROM

The built-in ROM, a mask ROM for the program, has a capacity of 768 × 12-bit steps. The program area is 3 pages (0–2), each consisting of 256 steps (00H–FFH). After an initial reset, the program start address is set to page 1, step 00H. The interrupt vectors are allocated to page l, steps 01H–07H.
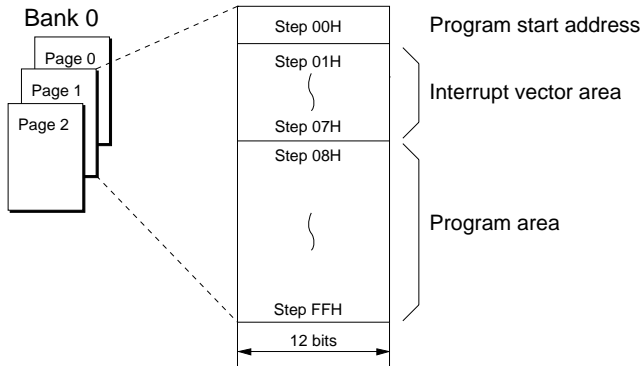


*Fig. 3.2.1  ROM configuration*

## 3.3  RAM

The RAM, a data memory for storing a variety of data, has a capacity of 64 words, 4-bit words. When programming, keep the following points in mind:

(1) Part of the data memory is used as stack area when saving subroutine return addresses and registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words on the stack.

(3) Data memory 000H–00FH is the memory area pointed by the register pointer (RP).

# CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C6003 Series are memory mapped. Thus, all the peripheral circuits can be controlled by using memory operations to access the I/O memory. The following sections describe how the peripheral circuits operate.

## 4.1 Memory Map

The data memory of the E0C6003 Series has an address space of 89 words, of which 16 words are allocated to display memory and 9 words, to I/O memory. Figure 4.1.1 show the overall memory map for the E0C6003 Series, and Table 4.1.1, the memory maps for the peripheral circuits (I/O space).

| Address | | Low | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---------|---|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Page | | High | | | | | | | | | | | | | | | | |
| | | 0 | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | MA | MB | MC | MD | ME | MF |
| | | 1 | RAM area (000H–03FH) 64 words × 4 bits (R/W) | | | | | | | | | | | | | | | |
| | | 2 | | | | | | | | | | | | | | | | |
| | | 3 | | | | | | | | | | | | | | | | |
| | | 4 | | | | | | | | | | | | | | | | |
| | | 5 | | | | | | | | | | | | | | | | |
| | | 6 | | | | | | | | | | | | | | | | |
| 0 | | 7 | | | | | | | | | | | | | | | | |
| | | 8 | | | | | | | | | | | | | | | | |
| | | 9 | | | | | | | | | | | | | | | | |
| | | A | | | | | | | | | | | | | | | | |
| | | B | | | | | | | | | | | | | | | | |
| | | C | | | | | | | | | | | | | | | | |
| | | D | | | | | | | | | | | | | | | | |
| | | E | Display memory ares (0E0H–0EFH)  16 words × 4 bits (W only) | | | | | | | | | | | | | | | |
| | | F | I/O memory    See Table 4.1.1 | | | | | | | | | | | | | | | |

☐ Unused area

*Fig. 4.1.1  Memory map*

*Note:  Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

*Table 4.1.1 I/O memory map*

| Address | Register D3 | Register D2 | Register D1 | Register D0 | Name | Init *1 | 1 | 0 | Comment |
|---------|----|----|----|----|------|---------|---|---|---------|
| 0F0H | K03 | K02 | K01 | K00 | K03 | – *2 | High | Low | |
| | | | | | K02 | – *2 | High | Low | |
| | R | R | R | R | K01 | – *2 | High | Low | K0 input port data |
| | | | | | K00 | – *2 | High | Low | |
| 0F1H | R03 | R02 | R01 / BUZZER | R00 / FOUT / BUZZER | R03 | 0 | High | Low | R03 output port data |
| | | | | | R02 | 0 | High | Low | R02 output port data |
| | | | | | R01 | 0 | High | Low | R01 output port data |
| | | | | | BUZZER | 0 | On | Off | Buzzer output On/Off control |
| | R/W | R/W | R/W | R/W | R00 | 0 | High | Low | R00 output port data |
| | | | | | FOUT | 0 | On | Off | FOUT output On/Off control |
| | | | | | BUZZER | 0 | On | Off | Buzzer inverted output On/Off control |
| 0F2H | TM3 | TM2 | TM1 | TM0 | TM3 | – *2 | | | Clock timer data (2 Hz) |
| | | | | | TM2 | – *2 | | | Clock timer data (4 Hz) |
| | R | R | R | R | TM1 | – *2 | | | Clock timer data (8 Hz) |
| | | | | | TM0 | – *2 | | | Clock timer data (16 Hz) |
| 0F3H | EIK03 | EIK02 | EIK01 | EIK00 | EIK03 | 0 | Enable | Mask | Interrupt mask register (K03) |
| | | | | | EIK02 | 0 | Enable | Mask | Interrupt mask register (K02) |
| | R/W | R/W | R/W | R/W | EIK01 | 0 | Enable | Mask | Interrupt mask register (K01) |
| | | | | | EIK00 | 0 | Enable | Mask | Interrupt mask register (K00) |
| 0F4H | TMRST | EIT2 | EIT16 | EIT32 | TMRST *3 | Reset | Reset | – | Clock timer reset |
| | | | | | EIT2 | 0 | Enable | Mask | Interrupt mask register (clock timer 2 Hz) |
| | W | R/W | R/W | R/W | EIT16 | 0 | Enable | Mask | Interrupt mask register (clock timer 16 Hz) |
| | | | | | EIT32 | 0 | Enable | Mask | Interrupt mask register (clock timer 32 Hz) |
| 0F5H | 0 | 0 | 0 | IK0 | 0 *3 | – *2 | – | – | Unused |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | R | R | R | R | 0 *3 | – *2 | – | – | Unused |
| | | | | | IK0 *4 | 0 | Yes | No | Interrupt factor flag (K00–K03) |
| 0F6H | 0 | IT2 | IT16 | IT32 | 0 *3 | – *2 | – | – | Unused |
| | | | | | IT2 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 2 Hz) |
| | R | R | R | R | IT16 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 16 Hz) |
| | | | | | IT32 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 32 Hz) |
| 0F7H | XBZR | 0 | XFOUT1 | XFOUT0 | XBZR | 0 | 2 kHz | 4 kHz | Buzzer frequency control |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | R/W | R | R/W | R/W | XFOUT1 | 0 | | | FOUT frequency control |
| | | | | | XFOUT0 | 0 | | | 0: F1, 1: F2, 2: F3, 3: F4 |
| 0F8H | LON | 0 | 0 | CSDC | LON | 0 | On | Off | LCD power and display On/Off conrol |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | R/W | R | R | R/W | 0 *3 | – *2 | – | – | Unused |
| | | | | | CSDC | 0 | Static | Dynamic | LCD drive switch |

*1 Initial value at initial reset  *3 Always "0" being read

*2 Not set in the circuit  *4 Reset (0) immediately after being read

## *4.2   Oscillation Circuit*

The E0C6003 Series has a built-in oscillation circuit that generates the operating clock of the CPU and the peripheral circuit. Either crystal oscillation or CR oscillation can be selected for the oscillation circuit by mask option.

### *4.2.1 Crystal oscillation circuit*

The crystal oscillation circuit can be selected by mask option. The oscillation frequency (fosc) is 32.768 kHz (Typ.).

Figure 4.2.1.1 shows the configuration of the crystal oscillation circuit.



*Fig. 4.2.1.1   Configuration of crystal oscillation circuit*

As Figure 4.2.1.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator X'tal (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals and the trimmer capacitor $C_G$ (5–25 pF) between the OSC1 and $V_{DD}$ terminals.

*Note:   The OSC1 and OSC2 terminals on the board should be shielded with the $V_{DD}$ (+ side).*

### *4.2.2 CR oscillation circuit*

The CR oscillation circuit can also be selected by mask option. The oscillation frequency (fosc) is 65 kHz (Typ.).

Figure 4.2.2.1 shows the configuration of the CR oscillation circuit.



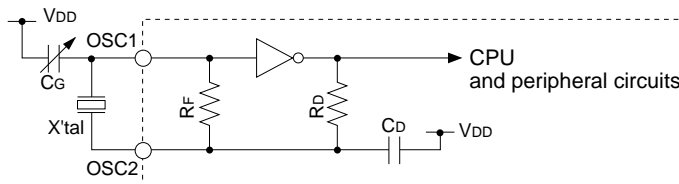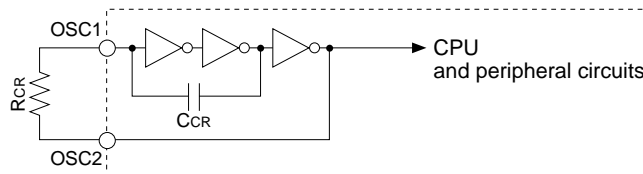*Fig. 4.2.2.1   Configuration of CR oscillation circuit*

As Figure 4.2.2.1 indicates, the CR oscillation circuit can be configured simply by connecting the resistor $R_{CR}$ between terminals OSC1 and OSC2 since capacity ($C_{CR}$) is built-in.

See Chapter 6, "Electrical Characteristics" for $R_{CR}$ value.

## 4.3 Input Port (K00–K03)

### 4.3.1 Configuration of input port

The E0C6003 Series has a 4-bit general-purpose input port. Each of the input port terminals (K00–K03) has an internal pull-down resistor. The pull-down resistor can be selected for each bit with the mask option.

Figure 4.3.1.1 shows the configuration of input port.
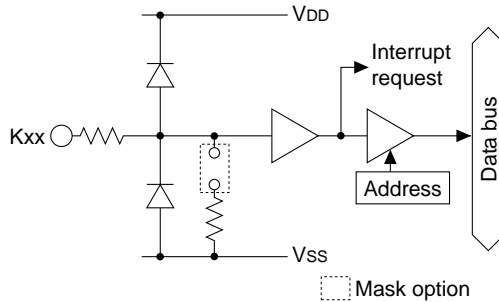


*Fig. 4.3.1.1  Configuration of input port*

Selecting "pull-down resistor enabled" with the mask option allows input from a push button, key matrix, and so forth. When "pull-down resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs.

### 4.3.2 Interrupt function

All four input port bits (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software for the four bits. Also, whether to mask the interrupt function can be selected individually for all four bits by the software. Figure 4.3.2.1 shows the configuration of K00–K03.
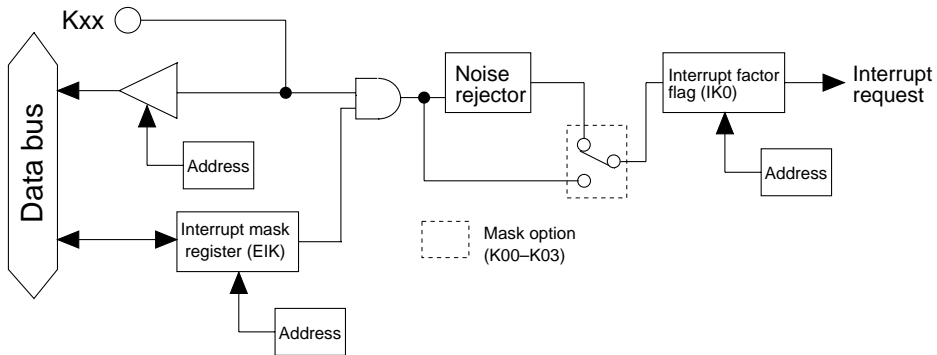


*Fig. 4.3.2.1  Input interrupt circuit configuration (K00–K03)*

The interrupt mask registers (EIK00–EIK03) enable the interrupt mask to be selected individually for K00–K03. An interrupt occurs when the input value which are not masked change and the interrupt factor flag (IK0) is set to 1.

**Input interrupt programming related precautions**
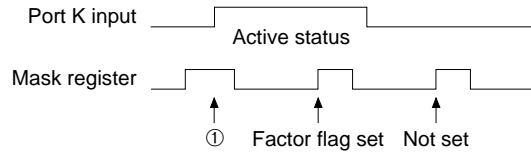


When the content of the mask register is rewritten, while the port
K input is in the active status. The input interrupt factor flag is
set at ①.

*Fig. 4.3.2.2  Input interrupt timing*

When using an input interrupt, if you rewrite the content of the mask register, when the value of the
input terminal which becomes the interrupt input is in the active status (input terminal = high status), the
factor flag for input interrupt may be set.

For example, a factor flag is set with the timing of ① shown in Figure 4.3.2.2. However, when clearing the
content of the mask register with the input terminal kept in the high status and then setting it, the factor
flag of the input ir5rrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (high status), do not rewrite the mask
register (clearing, then setting the mask register), so that a factor flag will only set at the rising edge in
this case. When clearing, then setting the mask register, set the mask register, when the input terminal is
not in the active status (low status).

## 4.3.3 Mask option

The contents that can be selected with the input port mask option are as follows:

(1) An internal pull-down resistor can be selected for each of the four bits of the input ports (K00–K03).
Having selected "pull-down resistor disabled", take care that the input does not float. Select "pull-
down resistor enabled" for input ports that are not being used.

(2) The input interrupt circuit contains a noise rejection circuit to prevent interrupts form occurring
through noise. The mask option enables selection of the noise rejection circuit for each separate
terminal series. When "use" is selected, a maximum delay of 0.5 msec (fosc = 32 kHz) occurs from the
time an interrupt condition is established until the interrupt factor flag (IK0) is set to 1.

## 4.3.4 I/O memory of input port

Table 4.3.4.1 list the input port control bits and their addresses.

*Table 4.3.4.1  Input port control bits*

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|------|------|------|------|------|---------|---|---|---------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0F0H | K03 | K02 | K01 | K00 | K03 | – *2 | High | Low | K0 input port data |
| | | | | | K02 | – *2 | High | Low | |
| | R | | | | K01 | – *2 | High | Low | |
| | | | | | K00 | – *2 | High | Low | |
| 0F3H | EIK03 | EIK02 | EIK01 | EIK00 | EIK03 | 0 | Enable | Mask | Interrupt mask register (K03) |
| | | | | | EIK02 | 0 | Enable | Mask | Interrupt mask register (K02) |
| | R/W | | | | EIK01 | 0 | Enable | Mask | Interrupt mask register (K01) |
| | | | | | EIK00 | 0 | Enable | Mask | Interrupt mask register (K00) |
| 0F5H | 0 | 0 | 0 | IK0 | 0 *3 | – *2 | – | – | Unused |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | R | | | | 0 *3 | – *2 | – | – | Unused |
| | | | | | IK0 *4 | 0 | Yes | No | Interrupt factor flag (K00–K03) |

∗1  Initial value at initial reset      ∗3  Always "0" being read
∗2  Not set in the circuit         ∗4  Reset (0) immediately after being read

### K00–K03: Input port data (0F0H)

The input data of the input port terminals can be read with these registers.

> When 1 is read:  High level
> When 0 is read:  Low level
> Writing:  Invalid

The value read is 1 when the terminal voltage of the input port (K00–K03) goes high ($V_{DD}$), and 0 when the voltage goes low ($V_{SS}$). These are read only bits, so writing cannot be done.

### EIK00–EIK03: Interrupt mask registers (0F3H)

Masking the interrupt of the input port terminals can be done with these registers.

> When 1 is written:  Enable
> When 0 is written:  Mask
> Reading:  Valid

With these registers, masking of the input port bits can be done for each of the four bits.
After an initial reset, these registers are all set to 0.

### IK0: Interrupt factor flag (0F5H•D0)

This flag indicates the occurrence of an input interrupt.

> When 1 is read:  Interrupt has occurred
> When 0 is read:  Interrupt has not occurred
> Writing:  Invalid

The interrupt factor flag IK0 is associated with K00–K03. From the status of this flag, the software can decide whether an input interrupt has occurred.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
After an initial reset, this flag is set to 0.

## 4.3.5 Programming note

When modifying the input port from high level to low level with pull-down resistor, a delay will occur at the fall of the waveform due to time constant of the pull-down resistor and input gate capacities. Provide appropriate waiting time in the program when performing input port reading.

# 4.4  Output Port (R00–R03)

## 4.4.1 Configuration of output port

The E0C6003 Series has a 4-bit general output port (R00–R03).
Output specification of the output port can be selected in a bit units with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output. Also, the mask option enables the output ports R00 and R01 to be used as special output ports. Figure 4.4.1.1 shows the configuration of the output port.
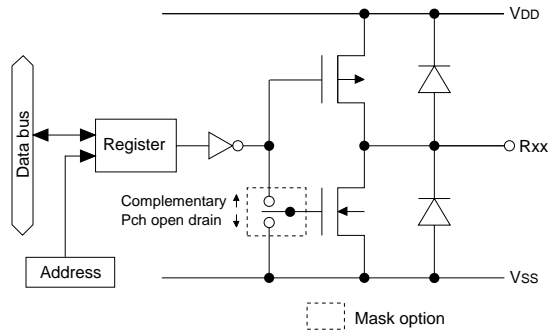
*Fig. 4.4.1.1  Configuration of output port*

## 4.4.2 Mask option

The mask option enables the following output port selection.

### (1) Output specification of output port

The output specifications for the output port (R00–R03) may be either complementary output or Pch open drain output for each of the two bits. However, even when Pch open drain output is selected, a voltage exceeding the source voltage must not be applied to the output port.

### (2) Special output

In addition to the regular DC output, special output can be selected for output ports R00 and R01, as shown in Table 4.4.2.1. Figure 4.4.2.1 shows the structure of output ports R00–R03.

*Table 4.4.2.1  Special output*

| Output port | Special output |
|---|---|
| R00 | FOUT or $\overline{\text{BUZZER}}$ output |
| R01 | BUZZER output |

*Fig. 4.4.2.1  Structire of output ports R00–R03*

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## FOUT (R00)

When the output port R00 is set as the FOUT output port, the R00 will output the fosc (CPU operating clock frequency) clock or the clock that is generated by dividing the fosc clock. The clock frequency can be selected individually for F1–F4, from among 5 types by mask option; one among F1–F4 is selected by software (XFOUT register) and used.

The types of frequency which can be selected are shown in Table 4.4.2.2.

*Table 4.4.2.2  FOUT clock frequency*

| Mask option set | Clock frequency (Hz) | | | |
|---|---|---|---|---|
| | F1 (XFOUT)=(0, 0) | F2 (XFOUT)=(0, 1) | F3 (XFOUT)=(1, 0) | F4 (XFOUT)=(1, 1) |
| Set 1 | 256   (fosc/128) | 512   (fosc/64) | 1,024   (fosc/32) | 2,048   (fosc/16) |
| Set 2 | 512   (fosc/64) | 1,024   (fosc/32) | 2,048   (fosc/16) | 4,096   (fosc/8) |
| Set 3 | 1,024   (fosc/32) | 2,048   (fosc/16) | 4,096   (fosc/8) | 8,192   (fosc/4) |
| Set 4 | 2,048   (fosc/16) | 4,096   (fosc/8) | 8,192   (fosc/4) | 16,384  (fosc/2) |
| Set 5 | 4,096   (fosc/8) | 8,192   (fosc/4) | 16,384  (fosc/2) | 32,768  (fosc/1) |

fosc = 32.768 kHz

*Note:  A hazard may occur when the FOUT signal is turned on or off.*

## BUZZER, $\overline{\text{BUZZER}}$ (R01, R00)

Output ports R01 and R00 may be set to BUZZER output and $\overline{\text{BUZZER}}$ output (BUZZER reverse output), respectively, allowing for direct driving of the piezo-electric buzzer.

The $\overline{\text{BUZZER}}$ signal is controlled by the R00 register and the BUZZER signal is controlled by the R01 register.

The frequency of buzzer output may be selected by software to be either 2 kHz or 4 kHz.

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## 4.4.3 I/O memory of output port

Table 4.4.3.1 lists the output port control bits and their addresses.

*Table 4.4.3.1  Control bits of output port*

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | | | | | |
| 0F1H | R03 | R02 | R01 / BUZZER | R00 / FOUT / BUZZER | R03 | 0 | High | Low | R03 output port data |
| | | | | | R02 | 0 | High | Low | R02 output port data |
| | | | | | R01 | 0 | High | Low | R01 output port data |
| | R/W | | | | BUZZER | 0 | On | Off | Buzzer output On/Off control |
| | | | | | R00 | 0 | High | Low | R00 output port data |
| | | | | | FOUT | 0 | On | Off | FOUT output On/Off control |
| | | | | | BUZZER | 0 | On | Off | Buzzer inverted output On/Off control |
| 0F7H | XBZR | 0 | XFOUT1 | XFOUT0 | XBZR | 0 | 2 kHz | 4 kHz | Buzzer frequency control |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | R/W | R | R/W | | XFOUT1 | 0 | | | FOUT frequency control |
| | | | | | XFOUT0 | 0 | | | 0: F1, 1: F2, 2: F3, 3: F4 |

*1  Initial value at initial reset      *3  Always "0" being read
*2  Not set in the circuit      *4  Reset (0) immediately after being read

### R00–R03: Output port data (0F1H)

Sets the output data for the output ports.

> When 1 is written:  High output
> When 0 is written:  Low output
> Reading:  Valid

The output port terminals output the data written to the corresponding registers (R00–R03) without changing it. When 1 is written to the register, the output port terminal goes high (VDD), and when 0 is written, the output port terminal goes low (VSS).
After an initial reset, all the registers are set to 0.

### R00 (when FOUT is selected): Special output port data (0F1H•D0)

Controls the FOUT (fosc clock) output.

> When 1 is written:  Clock output
> When 0 is written:  Low level (DC) output
> Reading:  Valid

FOUT output can be controlled by writing data to R00.
After an initial reset, this register is set to 0.
Figure 4.4.3.1 shows the output waveform for FOUT output.
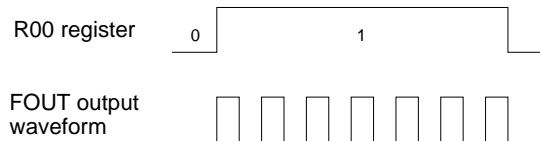


*Fig. 4.4.3.1  FOUT output waveform*

### XFOUT0, XFOUT1: FOUT frequency control (0F7H•D0, D1)

Selects the output frequency when the R00 port is set for FOUT output.

*Table 4.4.3.2  FOUT frequency selection*

| XFOUT1 | XFOUT0 | Frequency selected |
|---|---|---|
| 0 | 0 | F1 |
| 0 | 1 | F2 |
| 1 | 0 | F3 |
| 1 | 1 | F4 |

After an initial reset, these registers are set to 0.

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**R00, R01 (when buzzer output is selected): Special output port data (0F1H•D0, D1)**

Controls the buzzer output.

When 1 is written: Buzzer output
When 0 is written: Low level (DC) output
Reading: Valid

$\overline{\text{BUZZER}}$ and BUZZER output can be controlled by writing data to R00 and R01.
After an initial reset, these registers are set to 0.
Figure 4.4.3.2 shows the output waveform for buzzer output.
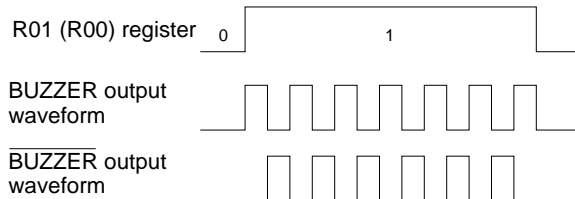


*Fig. 4.4.3.2  Buzzer output waveform*

**XBZR: Buzzer frequency control (0F7H•D3)**

Selects the frequency of the buzzer signal.

When 1 is written: 2 kHz
When 0 is written: 4 kHz
Reading: Valid

When R00 and R01 port is set to buzzer output, the frequency of the buzzer signal can be selected by this register.
When 1 is written to this register, the frequency is set in 2 kHz, and in 4 kHz when 0 is written.
After an initial reset, this register is set to 0.

### *4.4.4 Programming note*

The buzzer or FOUT signal may produce hazards when the output ports R00 and R01 are turned on or off.

# 4.5   LCD Driver (COM0–COM3, SEG0–SEG14)

## 4.5.1 Configuration of LCD driver

The E0C6003 Series has four common terminals and 15 (SEG0–SEG14) segment terminals, so that an LCD with a maximum of 60 ($15 \times 4$) segments can be driven. The power for driving the LCD is generated by the CPU internal circuit, so there is no need to supply power externally.

The driving method is 1/4 duty (or 1/3, 1/2 duty by mask option) dynamic drive, adopting the four types of potential (1/3 bias), $V_{DD}$, $V_{L1}$, $V_{L2}$ and $V_{L3}$. Moreover, the 1/2 bias dynamic drive that uses three types of potential, $V_{DD}$, $V_{L1} = V_{L2}$ and $V_{L3}$, can be selected by setting the mask option (drive duty can also be selected from 1/4, 1/3 or 1/2).

The LCD drive voltages $V_{L1}$ to $V_{L3}$ are generated by the power divider and/or voltage doubler/halver as shown in Table 4.5.1.1.

*Table 4.5.1.1   LCD drive voltage*

| Model | Bias selection | Drive voltage | | | |
|---|---|---|---|---|---|
| | | $V_{L1}$ | $V_{L2}$ | $V_{L3}$ | $V_{S2}$ |
| E0C6003 | 1/3 bias | 1/3 $V_{SS}$ | 2/3 $V_{SS}$ | $V_{SS}$ | – |
| | 1/2 bias (A) | 1/2 $V_{SS}$ | 1/2 $V_{SS}$ | $V_{SS}$ | – |
| | 1/2 bias (B) | $V_{S2}$ | $V_{S2}$ | $V_{SS}$ | 1/2 $V_{SS}$ |
| E0C60L03 | 1/3 bias | 1/3 $V_{S2}$ | 2/3 $V_{S2}$ | $V_{S2}$ | 2 $V_{SS}$ |
| | 1/2 bias (A) | 1/2 $V_{S2}$ | 1/2 $V_{S2}$ | $V_{S2}$ | 2 $V_{SS}$ |
| | 1/2 bias (B) | $V_{SS}$ | $V_{SS}$ | $V_{S2}$ | 2 $V_{SS}$ |

Refer to Section 2.1, "Power Supply", for details of the power supply circuit.

The frame frequency is 32 Hz for 1/4 duty and 1/2 duty, and 42.7 Hz for 1/3 duty (in the case of fosc = 32 kHz).

Figures 4.5.1.1 to 4.5.1.6 show the drive waveform for each duty and bias.

Note:   "fosc" indicates the oscillation frequency of the oscillation circuit.
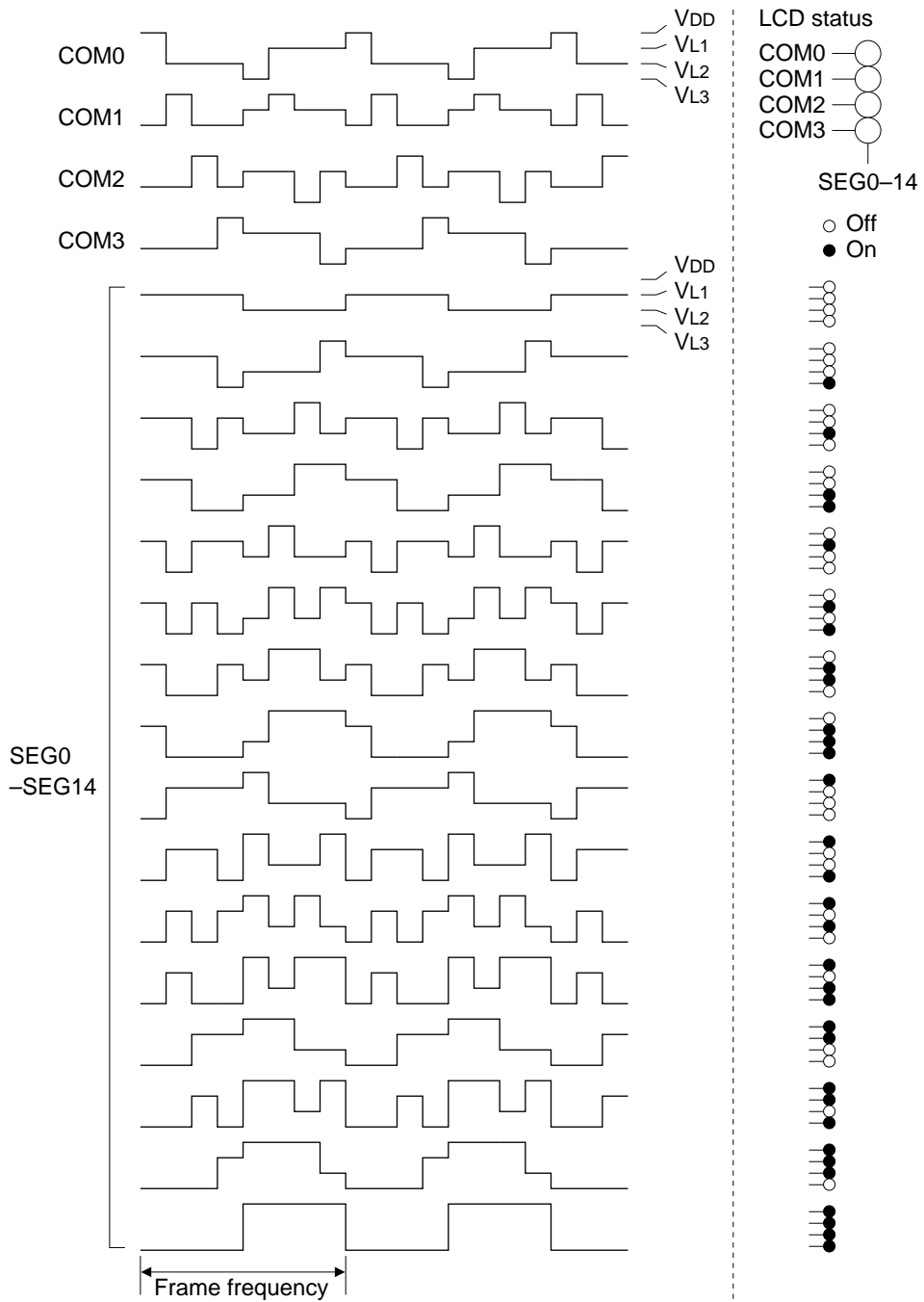
*Fig. 4.5.1.1 Drive waveform for 1/4 duty (1/3 bias)*
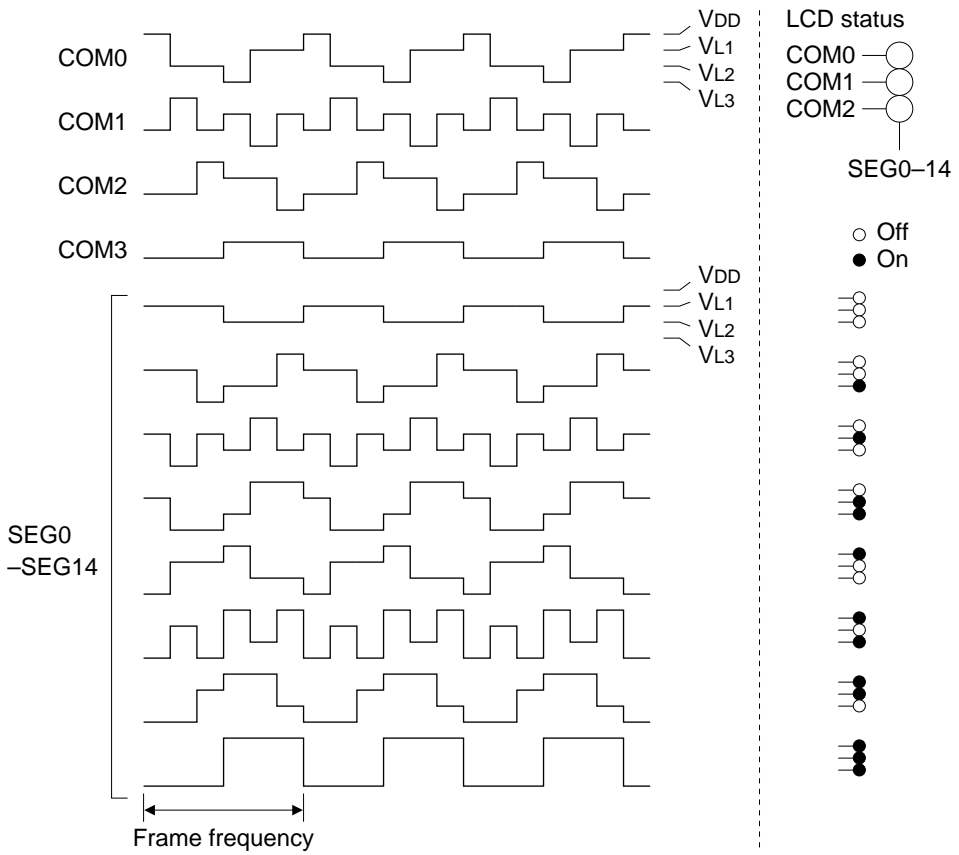
*Fig. 4.5.1.2  Drive waveform for 1/3 duty (1/3 bias)*
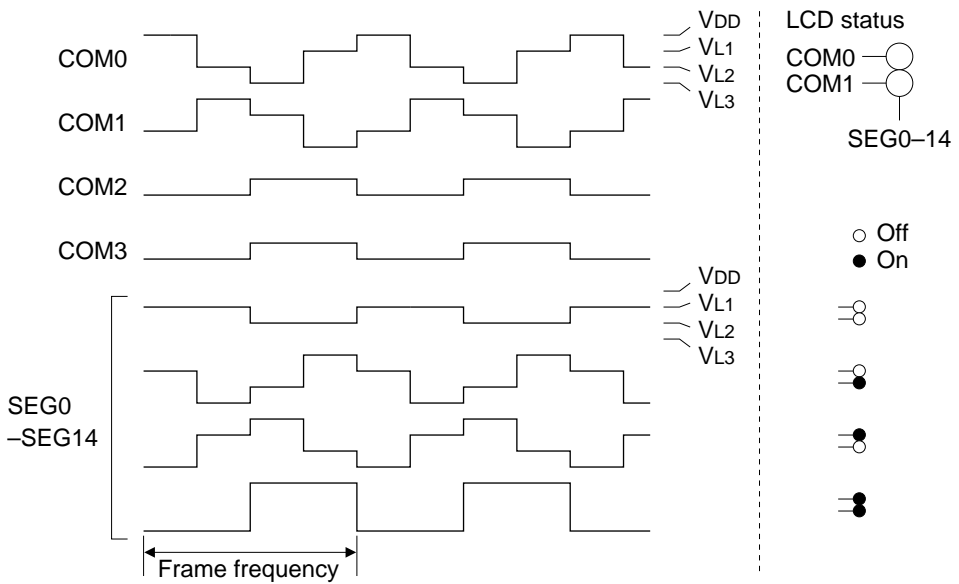


*Fig. 4.5.1.3  Drive waveform for 1/2 duty (1/3 bias)*
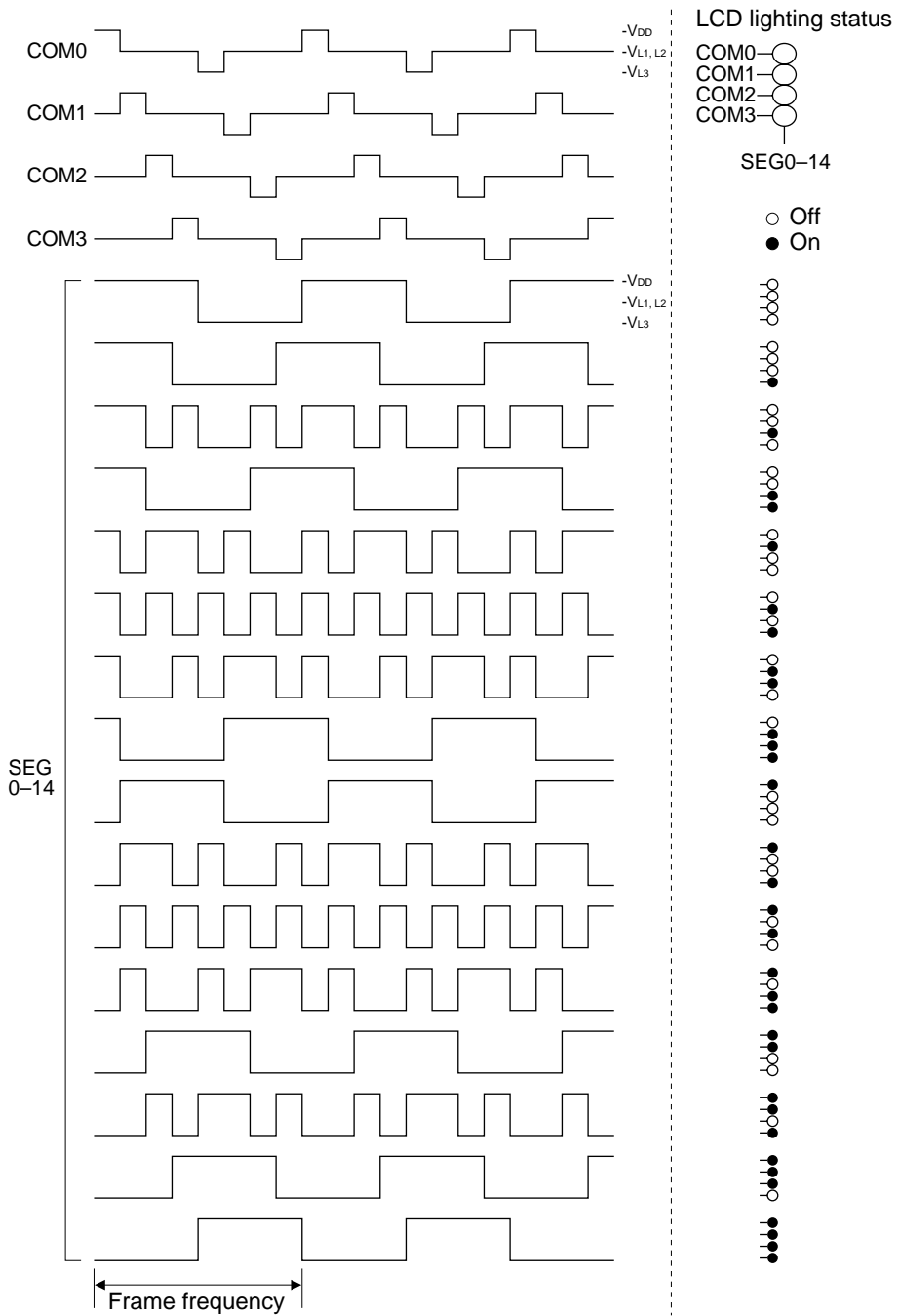
*Fig. 4.5.1.4  Drive waveform for 1/4 duty (1/2 bias)*
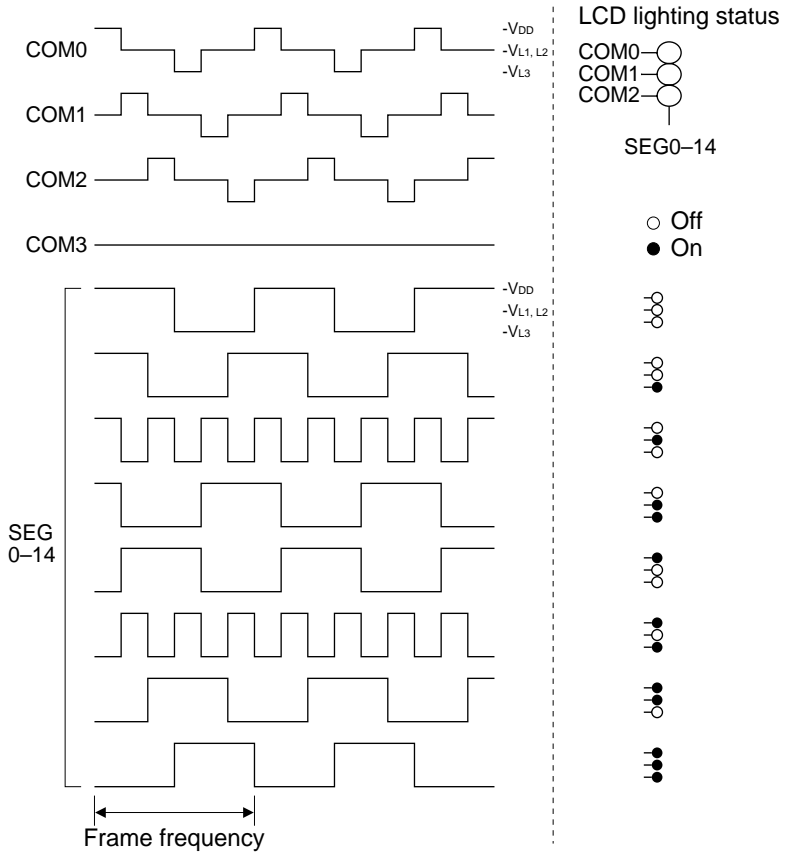
*Fig. 4.5.1.5  Drive waveform for 1/3 duty (1/2 bias)*
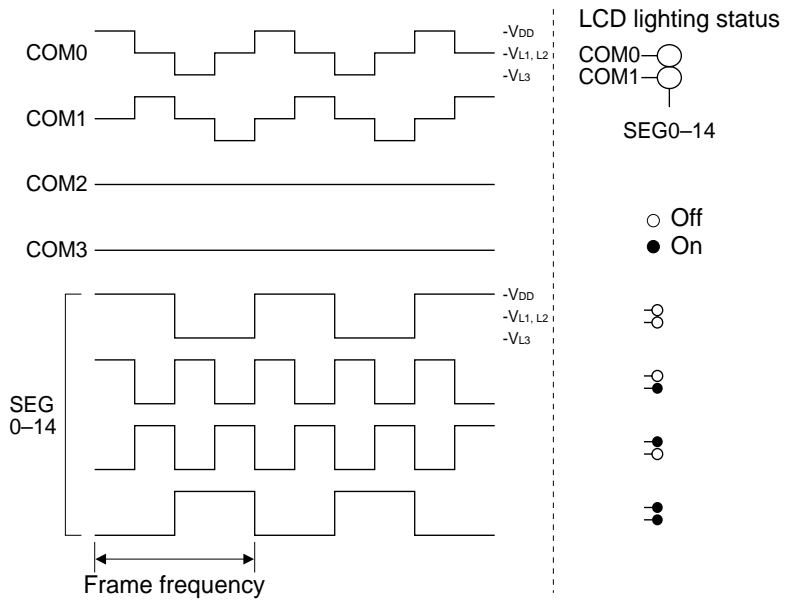


*Fig. 4.5.1.6  Drive waveform for 1/2 duty (1/2 bias)*

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## *4.5.2 Cadence adjustment of oscillation frequency*

In the E0C6003 Series, the LCD drive duty can be set to 1/1 duty by software. This function enables easy adjustment (cadence adjustment) of the oscillation frequency of the oscillation circuit.
The procedure to set to 1/1 duty drive is as follows:

① Write 1 to the CSDC register at address 0F8H•D0.

② Write the same value to all registers corresponding to COMs 0 through 3 of the display memory.

The frame frequency is 32 Hz (fosc/1024, when fosc = 32.768 kHz).

*Note: • Even when l/3 or 1/2 duty is selected by the mask option, the display data corresponding to all COM are valid during 1/1 duty driving. Hence, for 1/1 duty drive, set the same value for all display memory corresponding to COMs 0 through 3.*

*• For cadence adjustment, set the display data corresponding to COMs 0 through 3, so that all the LCD segments go on.*

Figures 4.5.2.1 and 4.5.2.2 show the 1/1 duty drive waveform in 1/3 bias and 1/2 bias driving.
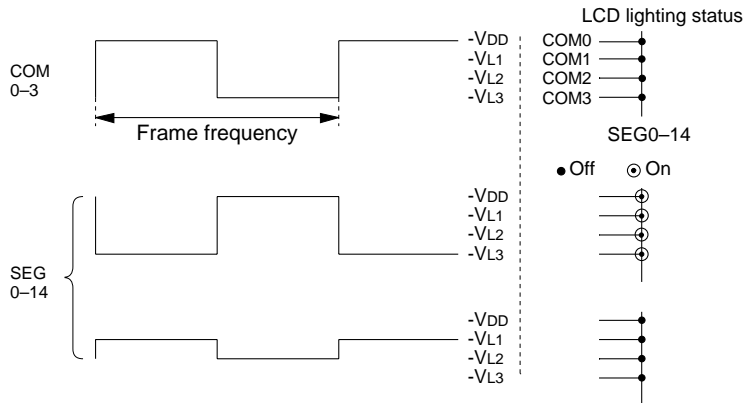


*Fig. 4.5.2.1  Drive waveform for 1/1 duty (1/3 bias)*
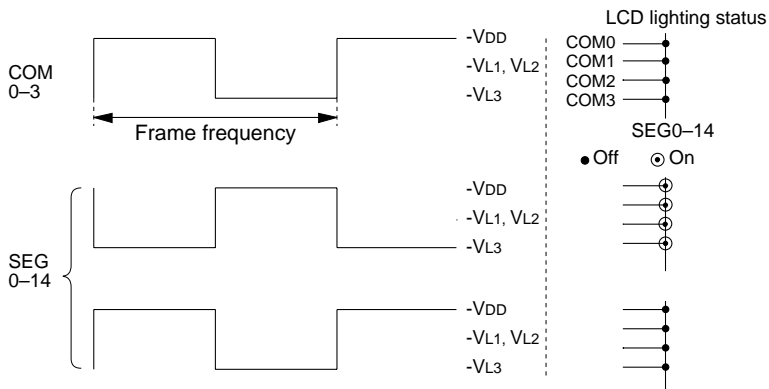


*Fig. 4.5.2.2  Drive waveform for 1/1 duty (1/2 bias)*

### *4.5.3 Mask option*

#### (1) Segment allocation

As shown in Figure 4.l.1, display data is decided by the data written to the display memory (write-only) at address 0E0H–0EFH.

The address and bits of the display memory can be made to correspond to the segment terminals (SEG0–SEG14) in any combination through mask option. This simplifies design by increasing the degree of freedom with which the liquid crystal panel can be designed.

Figure 4.5.3.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory in the case of 1/3 duty.

| Address | Data | | | |
|---------|------|------|------|------|
| | D3 | D2 | D1 | D0 |
| 0EAH | d | c | b | a |
| 0EBH | p | g | f | e |
| 0ECH | d' | c' | b' | a' |
| 0EDH | p' | g' | f' | e' |

Display data memory allocation

| | Common 0 | Common 1 | Common 2 |
|------|----------|----------|----------|
| SEG10 | EA, D0 | EB, D1 | EB, D0 |
| | (a) | (f) | (e) |
| SEG11 | EA, D1 | EB, D2 | EA, D3 |
| | (b) | (g) | (d) |
| SEG12 | ED, D1 | EA, D2 | EB, D3 |
| | (f') | (c) | (p) |

Pin address allocation
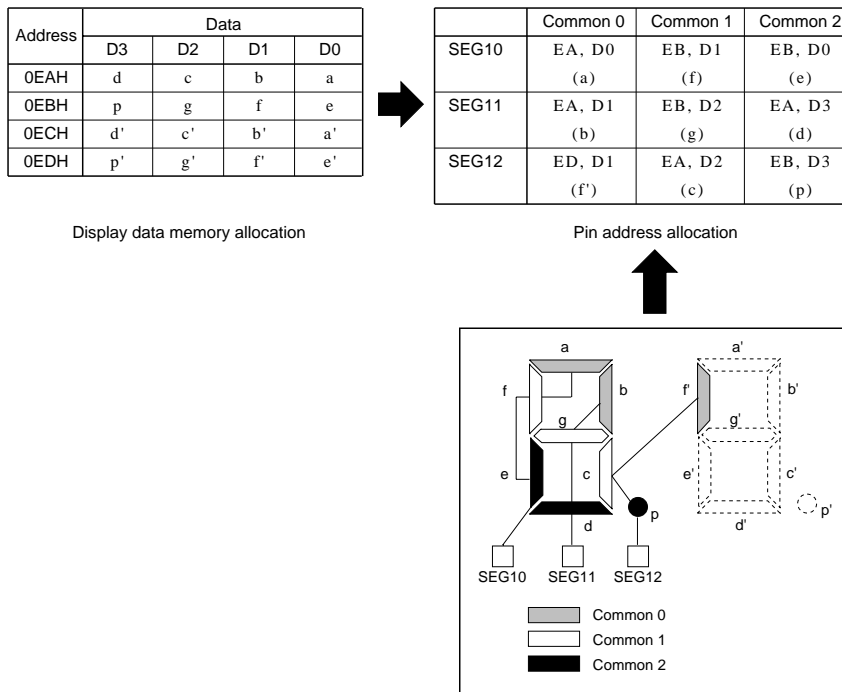


*Fig. 4.5.3.1  Segment allocation*

#### (2) Drive duty

According to the mask option, either 1/4, 1/3 or 1/2 duty can be selected as the LCD drive duty. Table 4.5.3.1 shows the differences in the number of segments according to the selected duty.

*Table 4.5.3.1  Differences according to selected duty*

| Duty | COM used | Max. number of segments | Frame frequency * |
|------|----------|-------------------------|-------------------|
| 1/4 | COM0–COM3 | 60 (15 × 4) | 32 Hz |
| 1/3 | COM0–COM2 | 45 (15 × 3) | 42.7 Hz |
| 1/2 | COM0–COM1 | 30 (15 × 2) | 32 Hz |

∗ When f$_{OSC}$ = 32 kHz

#### (3) Output specification

① The segment terminals (SEG0–SEG14) are selected by mask option in pairs for either segment signal output or DC output (V$_{DD}$ and V$_{SS}$ binary output). When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or Pch open drain output can be selected for each terminal by mask option.

*Note: The terminal pairs are the combination of SEG (2∗n) and SEG (2∗n + 1) (where n is an integer from 0 to 6).*

#### (4) Drive bias

For the drive bias, either 1/3 bias or 1/2 bias can be selected by the mask option.

## 4.5.4 I/O memory of LCD driver

Table 4.5.4.1 shows the control bits of the LCD driver and their addresses. Figure 4.5.4.1 shows the display memory map.

*Table 4.5.4.1  Control bits of LCD driver*

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|------|------|------|------|------|---------|---|---|---------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0F8H | LON | 0 | 0 | CSDC | LON | 0 | On | Off | LCD power and display On/Off conrol |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | R/W | R | | R/W | CSDC | 0 | Static | Dynamic | LCD drive switch |

*1  Initial value at initial reset      *3  Always "0" being read

*2  Not set in the circuit        *4  Reset (0) immediately after being read

| Address | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0E0 | Display memory (Write only) 16 words x 4 bits | | | | | | | | | | | | | | | |

*Fig. 4.5.4.1  Display memory map*

### LON: LCD display and power divider On/Off control (0F8H•D3)

The LCD display can be turned on or off with this switch. It also controls the power divider on or off if the power divider is selected for the LCD power generator.

> When 1 is written:  LCD displayed
> When 0 is written:  LCD is all off
>          Reading:  Valid

When the power divider is selected for the LCD power generator, power current consumption will increase if this switch is turned on.

Keep this switch off (LON = 0) when LCD display is not necessary.

After an initial reset, LCD and the power divider is turned off.

### CSDC: LCD drive switch (0F8H•D0)

The LCD drive format can be selected with this switch.

> When 1 is written:  Static drive
> When 0 is written:  Dynamic drive
>          Reading:  Valid

After an initial reset, dynamic drive (CSDC = 0) is selected.

### Display memory (0E0H–0EFH)

The LCD segments are turned on or off according to this data.

> When 1 is written:  On
> When 0 is written:  Off
>          Reading:  Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be turned on or off. After an initial reset, the contents of the display memory are undefined.

## 4.5.5 Programming note

Because the display memory is for writing only, re-writing the contents with computing instructions (e.g., AND, OR, etc.) which come with read-out operations is not possible. To perform bit operations, a buffer to hold the display data is required on the RAM.

## 4.6 Clock Timer

### 4.6.1 Configuration of clock timer

The E0C6003 Series has a built-in clock timer that uses the oscillation circuit as the clock source. The clock timer is configured as a 7-bit binary counter that counts with a 256 Hz source clock from the divider. The high-order 4 bits of the counter (16 Hz–2 Hz) can be read by the software.

Figure 4.6.1.1 is the block diagram of the clock timer.
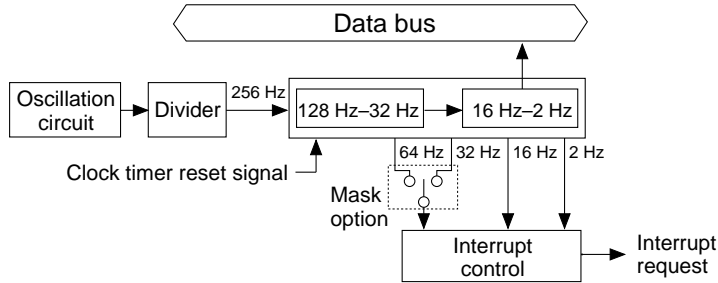


*Fig. 4.6.1.1  Block diagram of clock timer*

Normally, this clock timer is used for all kinds of timing purpose, such as clocks.

### 4.6.2 Interrupt function

The clock timer can generate interrupts at the falling edge of the 32 Hz (or 64 Hz), 16 Hz, and 2 Hz signals. The software can mask any of these interrupt signals.

Figure 4.6.2.1 is the timing chart of the clock timer.
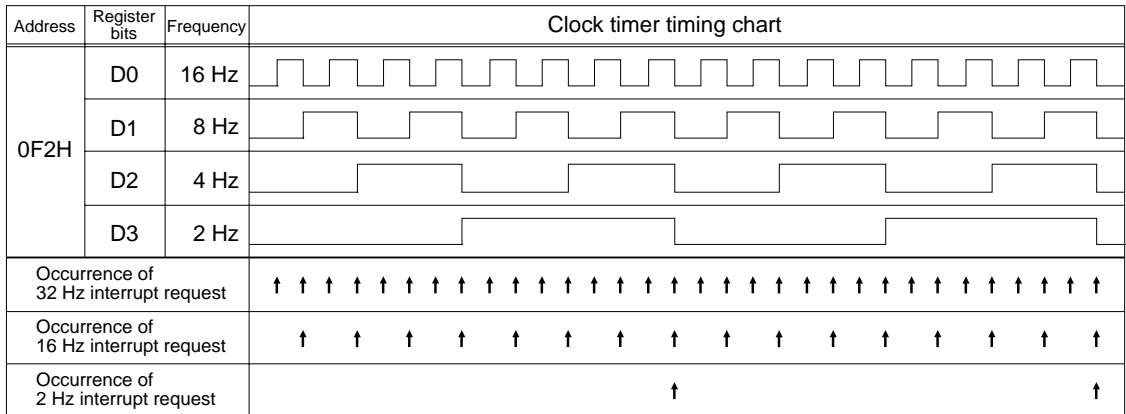


*Fig. 4.6.2.1  Timing chart of the clock timer*

As shown in Figure 4.6.2.1, an interrupt is generated at the falling edge of the 32 Hz, 16 Hz, and 2 Hz signals. At this point, the corresponding interrupt factor flag (IT32, IT16, IT2) is set to 1. The interrupts can be masked individually with the interrupt mask register (EIT32, EIT16, EIT2). However, regardless of the interrupt mask register setting, the interrupt factor flags will be set to 1 at the falling edge of their corresponding signal (e.g. the falling edge of the 2 Hz signal sets the 2 Hz interrupt factor flag to 1).

*Note:  Write to the interrupt mask registers (EIT32, EIT16, EIT2) and read the interrupt factor flags (IT32, IT16, IT2) only in the DI status (interrupt flag = 0). Otherwise, it causes malfunction.*

### 4.6.3 Mask option

The 32 Hz timer interrupt can be changed to 64 Hz by mask option.
When 64 Hz is selected by mask option, the falling edge of the 64 Hz signal sets the IT32 interrupt factor flag (0F6H•D0) and the interrupt is controlled with the EIT32 interrupt mask register (0F4H•D0).

### 4.6.4 I/O memory of clock timer

Table 4.6.4.1 shows the clock timer control bits and their addresses.

*Table 4.6.4.1  Control bits of clock timer*

| Address | Register | | | | Name | Init *1 | 1 | 0 | Comment |
|---------|------|------|------|------|------|---------|---|---|---------|
| | D3 | D2 | D1 | D0 | | | | | |
| 0F2H | TM3 | TM2 | TM1 | TM0 | TM3 | – *2 | | | Clock timer data (2 Hz) |
| | | | | | TM2 | – *2 | | | Clock timer data (4 Hz) |
| | R | | | | TM1 | – *2 | | | Clock timer data (8 Hz) |
| | | | | | TM0 | – *2 | | | Clock timer data (16 Hz) |
| 0F4H | TMRST | EIT2 | EIT16 | EIT32 | TMRST*3 | Reset | Reset | – | Clock timer reset |
| | | | | | EIT2 | 0 | Enable | Mask | Interrupt mask register (clock timer 2 Hz) |
| | W | R/W | | | EIT16 | 0 | Enable | Mask | Interrupt mask register (clock timer 16 Hz) |
| | | | | | EIT32 | 0 | Enable | Mask | Interrupt mask register (clock timer 32 Hz) |
| 0F6H | 0 | IT2 | IT16 | IT32 | 0 *3 | – *2 | – | – | Unused |
| | | | | | IT2 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 2 Hz) |
| | R | | | | IT16 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 16 Hz) |
| | | | | | IT32 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 32 Hz) |

∗1 Initial value at initial reset  ∗3 Always "0" being read
∗2 Not set in the circuit  ∗4 Reset (0) immediately after being read

**TM0–TM3: Timer data (0F2H)**

The l6 Hz to 2 Hz timer data of the clock timer can be read from this register. These four bits are read-only, and write operations are invalid.
After an initial reset, the timer data is initialized to "0H".

**EIT32, EIT16, EIT2: Interrupt mask registers (0F4H•D0–D2)**

These registers are used to mask the clock timer interrupt.

　　　When 1 is written:  Enabled
　　　When 0 is written:  Masked
　　　　　　Reading:  Valid

The interrupt mask registers (EIT32, EIT16, EIT2) mask the corresponding interrupt frequencies (32 Hz/ 64 Hz, 16 Hz, 2 Hz).
At initial reset, these registers are all set to 0.

**IT32, IT16, IT2: Interrupt factor flags (0F6H•D0–D2)**

These flags indicate the status of the clock timer interrupt.

　　　When 1 is read:  Interrupt has occurred
　　　When 0 is read:  Interrupt has not occurred
　　　　　Writing:  Invalid

The interrupt factor flags (IT32, IT16, IT2) correspond to the clock timer interrupts (32 Hz/64 Hz, 16 Hz, 2 Hz). The software can determine from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to 1 at the falling edge of the signal. These flags can be reset when the register is read by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to 0.

**TMRST: Clock timer reset (0F4H•D3)**

This bit resets the clock timer.

> When 1 is written:  Clock timer reset
> When 0 is written:  No operation
> Reading:  Always 0

The clock timer is reset by writing 1 to TMRST. The clock timer starts immediately after this. No operation results when 0 is written to TMRST.
This bit is write-only, and so is always 0 when read.

## 4.6.5 Programming notes

(1) Note that the frequencies and times differ from the description in this section when the oscillation frequency is not 32.768 kHz.

(2) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

## *4.7 Interrupt and HALT*

The E0C6003 Series provides the following interrupt settings, each of which is maskable.

External interrupt:    Input port interrupt (one)
Internal interrupt:    Timer interrupt (one)

To enable interrupts, the interrupt flag must be set to 1 (EI) and the necessary related interrupt mask registers must be set to 1 (enable). When an interrupt occurs, the interrupt flag is automatically reset to 0 (DI) and interrupts after that are inhibited.
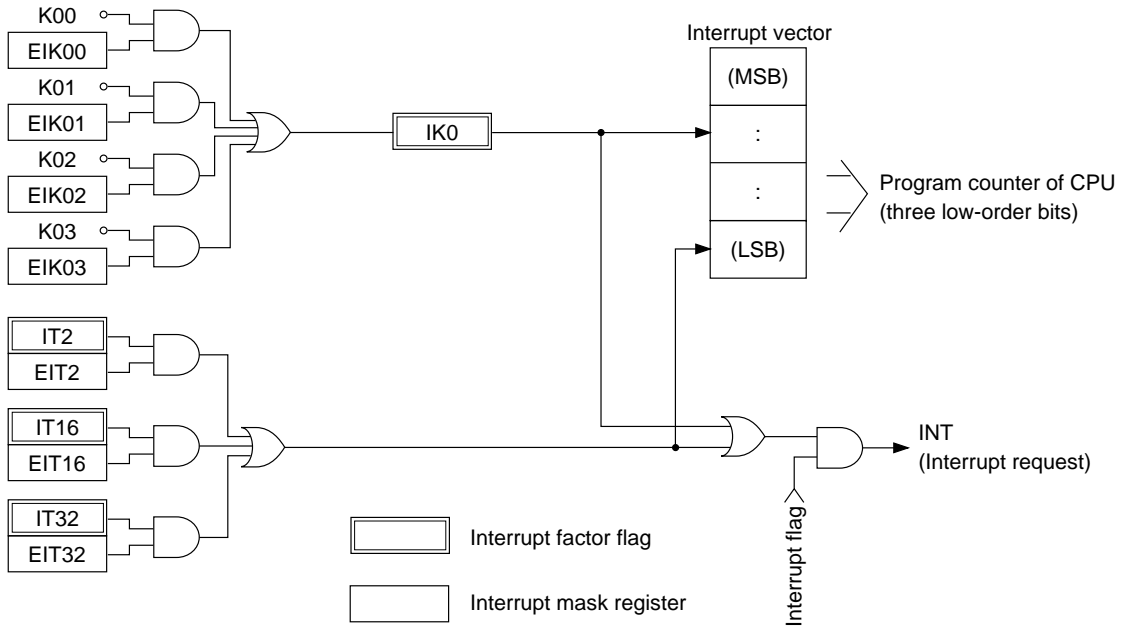Figure 4.7.1 shows the configuration of the interrupt circuit.



*Fig. 4.7.1  Configuration of interrupt circuit*

### HALT mode

When the HALT instruction is executed, the CPU stops operating and enters the HALT mode. The oscillation circuit and the peripheral circuits operate in the HALT mode. By an interrupt, the CPU exits the HALT mode and resumes operating.

### 4.7.1 Interrupt factors

Table 4.7.1.1 shows the factors that generate interrupt requests.

The interrupt factor flags are set to 1 depending on the corresponding interrupt factors.
The CPU is interrupted when the following two conditions occur and an interrupt factor flag is set to 1.

• The corresponding mask register is 1 (enabled)
• The interrupt flag is 1 (EI)

The interrupt factor flag is a read-only register, but can be reset to 0 when the register data is read.
At initial reset, the interrupt factor flags are reset to 0.

*Note:   Reading of interrupt factor flag is available at EI, but be careful in the following cases.*
*If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1,*
*an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request*
*will not be generated. Be very careful when interrupt factor flags are in the same address.*

*Table 4.7.1.1  Interrupt factors*

| Interrupt factor | Interrupt factor flag | |
|---|---|---|
| Clock timer 2 Hz falling edge | IT2 | (0F6H•D2) |
| Clock timer 16 Hz falling edge | IT16 | (0F6H•D1) |
| Clock timer 32 (or 64) Hz falling edge | IT32 | (0F6H•D0) |
| Input (K00–K03) port rising edge | IK0 | (0F5H•D0) |

### 4.7.2 Specific masks for interrupt

The interrupt factor flags can be masked by the corresponding interrupt mask registers. The interrupt
mask registers are read / write registers. The interrupts are enabled when 1 is written to them, and
masked (interrupt disabled) when 0 is written to them.
At initial reset, the interrupt mask register is set to 0.
Table 4.7.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

*Table 4.7.2.1  Interrupt mask registers and interrupt factor flags*

| Interrupt mask register | | Interrupt factor flag | |
|---|---|---|---|
| EIT2 | (0F4H•D2) | IT2 | (0F6H•D2) |
| EIT16 | (0F4H•D1) | IT16 | (0F6H•D1) |
| EIT32 | (0F4H•D0) | IT32 | (0F6H•D0) |
| EIK03* | (0F3H•D3) | | |
| EIK02* | (0F3H•D2) | IK0 | (0F5H•D0) |
| EIK01* | (0F3H•D1) | | |
| EIK00* | (0F3H•D0) | | |

∗ There is an interrupt mask register for each input port terminal.

### 4.7.3 Interrupt vectors

When an interrupt request is input to the CPU, the CPU starts interrupt processing. After the program being executed is suspended, interrupt processing is executed in the following order:

① The address data (value of the program counter) of the program step to be executed next is saved on the stack (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 01H–07H) to be loaded into the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine).

*Note: The processing in steps 1 and 2, above, takes 12 cycles of the CPU system clock.*

*Table 4.7.3.1  Interrupt vector addresses*

| Page | Step | Interrupt vector |
|------|------|------------------|
| 1 | 00H | Initial reset |
| | 01H | Clock timer interrupt |
| | 04H | Input (K00–K03) interrupt |

### 4.7.4 I/O memory of interrupt

Table 4.7.4.1 shows the interrupt control bits and their addresses.

*Table 4.7.4.1  Control bits of interrupt*

| Address | Register D3 | D2 | D1 | D0 | Name | Init *1 | 1 | 0 | Comment |
|---------|-----|-----|-----|-----|------|--------|-----|-----|---------|
| 0F3H | EIK03 | EIK02 | EIK01 | EIK00 | EIK03 | 0 | Enable | Mask | Interrupt mask register (K03) |
| | | | | | EIK02 | 0 | Enable | Mask | Interrupt mask register (K02) |
| | R/W | | | | EIK01 | 0 | Enable | Mask | Interrupt mask register (K01) |
| | | | | | EIK00 | 0 | Enable | Mask | Interrupt mask register (K00) |
| 0F4H | TMRST | EIT2 | EIT16 | EIT32 | TMRST*3 | Reset | Reset | – | Clock timer reset |
| | | | | | EIT2 | 0 | Enable | Mask | Interrupt mask register (clock timer 2 Hz) |
| | W | R/W | | | EIT16 | 0 | Enable | Mask | Interrupt mask register (clock timer 16 Hz) |
| | | | | | EIT32 | 0 | Enable | Mask | Interrupt mask register (clock timer 32 Hz) |
| 0F5H | 0 | 0 | 0 | IK0 | 0 *3 | – *2 | – | – | Unused |
| | | | | | 0 *3 | – *2 | – | – | Unused |
| | R | | | | 0 *3 | – *2 | – | – | Unused |
| | | | | | IK0 *4 | 0 | Yes | No | Interrupt factor flag (K00–K03) |
| 0F6H | 0 | IT2 | IT16 | IT32 | 0 *3 | – *2 | – | – | Unused |
| | | | | | IT2 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 2 Hz) |
| | R | | | | IT16 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 16 Hz) |
| | | | | | IT32 *4 | 0 | Yes | No | Interrupt factor flag (clock timer 32 Hz) |

∗1  Initial value at initial reset
∗2  Not set in the circuit
∗3  Always "0" being read
∗4  Reset (0) immediately after being read

**EIT32, EIT16, EIT2: Interrupt mask registers (0F4H•D0–D2)**
**IT32, IT16, IT2: Interrupt factor flags (0F6H•D0–D2)**
                ...See Section 4.6, "Clock Timer".

**EIK00–EIK03: Interrupt mask registers (0F3H)**
**IK0: Interrupt factor flag (0F5H•D0)**
                ...See Section 4.3, "Input Port".

## *4.7.5 Programming notes*

(1) Restart from the HALT mode is performed by an interrupt. The return address after completion of the interrupt processing will be the address following the HALT instruction.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to 1, the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to 1, an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

# CHAPTER 5    BASIC EXTERNAL WIRING DIAGRAM

**Piezo Buzzer Single Terminal Driving**
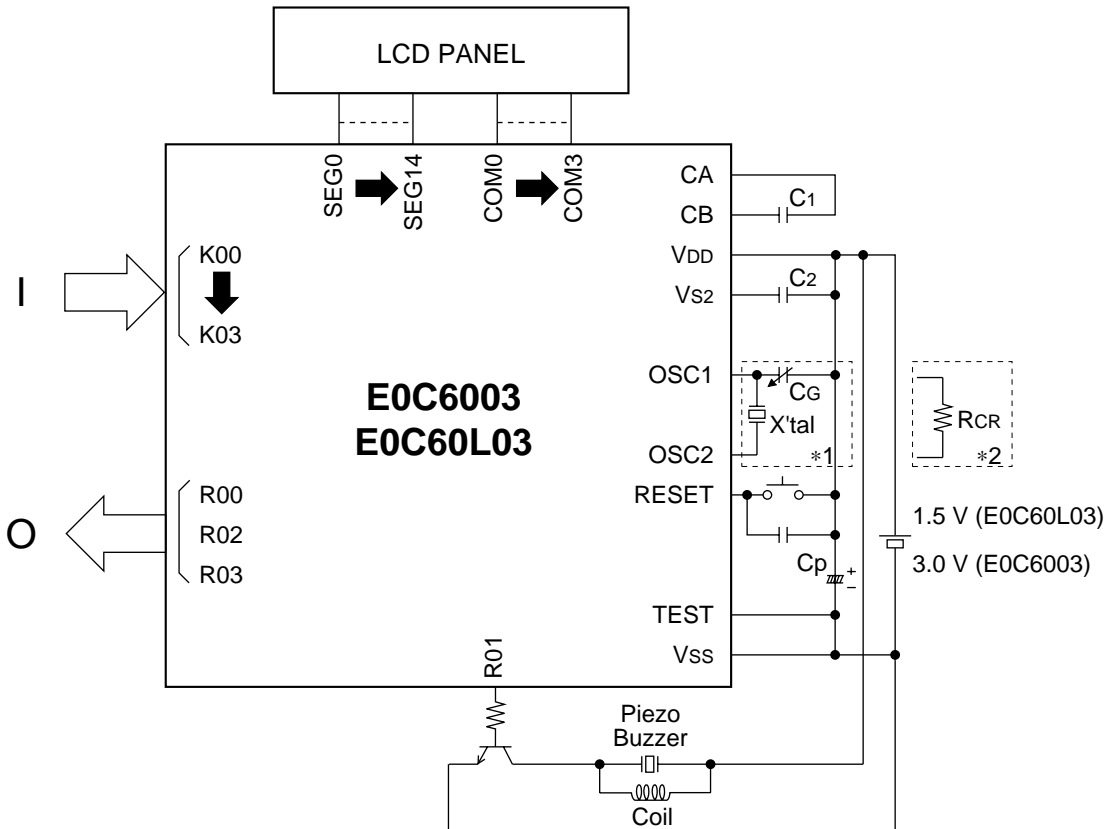


*1 Crystal oscillation
*2 CR oscillation

| X'tal | Crystal oscillator | 32.768 kHz, $C_I$ (Max.) = 35 k$\Omega$ |
|-------|-------------------|--------------------------------------|
| $C_G$ | Trimmer capacitor | 5–25 pF |
| $R_{CR}$ | Resistor for CR oscillation | 470 k$\Omega$ (65 kHz) |
| $C_1$, $C_2$ | Capacitor | 1 $\mu$F (see Note) |
| $C_p$ | Capacitor | 3.3 $\mu$F |

*Note:   Use a 1 $\mu$F capacitor for $C_1$ and $C_2$ when "E0C60L03 1/3 bias" is selected, or a 0.1 $\mu$F capacitor
when "E0C6003 1/2 bias" or "E0C60L03 1/2 bias (A), (B)" is selected.
No capacitor is required for $C_1$ and $C_2$ when another specification is selected.*

**Piezo Buzzer Direct Driving**



| X'tal | Crystal oscillator | 32.768 kHz, $C_I$ (Max.) = 35 k$\Omega$ |
|---|---|---|
| $C_G$ | Trimmer capacitor | 5–25 pF |
| $R_{CR}$ | Resistor for CR oscillation | 470 k$\Omega$ (65 kHz) |
| $C_1$, $C_2$ | Capacitor | 1 $\mu$F (see Note) |
| $C_p$ | Capacitor | 3.3 $\mu$F |

*Note:  Use a 1 µF capacitor for $C_1$ and $C_2$ when "E0C60L03 1/3 bias" is selected, or a 0.1 µF capacitor when "E0C6003 1/2 bias" or "E0C60L03 1/2 bias (A), (B)" is selected.*
*No capacitor is required for $C_1$ and $C_2$ when another specification is selected.*

# CHAPTER 6 ELECTRICAL CHARACTERISTICS

## 6.1 Absolute Maximum Rating

(VDD=0V)

| Item | Symbol | Rated value | Unit |
|------|--------|-------------|------|
| Supply voltage | VSS | -5.0 to 0.5 | V |
| Input voltage (1) | VI | VSS - 0.3 to 0.5 | V |
| Input voltage (2) | VIOSC | VSS - 0.3 to 0.5 | V |
| Permissible total output current ∗1 | ΣIVSS | 10 | mA |
| Operating temperature | Topr | -20 to 70 | °C |
| Storage temperature | Tstg | -65 to 150 | °C |
| Soldering temperature / time | Tsol | 260°C, 10sec (lead section) | – |
| Permissible dissipation | PD | 250 | mW |

∗1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

## 6.2 Recommended Operating Conditions

**E0C6003**

(Ta=-20 to 70°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------|--------|-----------|------|------|------|------|
| Supply voltage | VSS | VDD=0V | -3.6 | -3.0 | -1.8 | V |
| Oscillation frequency | fOSC | Crystal oscillation | | 32.768 | | kHz |
| | | CR oscillation, RCR=470kΩ | 50 | 65 | 80 | kHz |
| Booster capacitor | C1 | | 0.1 | | | μF |
| Capacitor betwen VDD and VS2 | C2 | | 0.1 | | | μF |

**E0C60L03**

(Ta=-20 to 70°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------|--------|-----------|------|------|------|------|
| Supply voltage | VSS | VDD=0V | -2.0 | -1.5 | -1.2 | V |
| Oscillation frequency | fOSC | Crystal oscillation | | 32.768 | | kHz |
| | | CR oscillation, RCR=470kΩ | 50 | 65 | 80 | kHz |
| Booster capacitor | C1 | | 0.1 | | | μF |
| Capacitor betwen VDD and VS2 | C2 | | 0.1 | | | μF |

## *6.3   DC Characteristics*

**E0C6003**

Unless otherwise specified:

$V_{DD}$=0V, $V_{SS}$=-3.0V, fosc=32.768kHz, Ta=25°C, $V_{S2}$ is internal voltage, $C_1$=$C_2$=0.1μF

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|------|--------|-----------|--|------|------|------|------|
| High level input voltage (1) | $V_{IH1}$ | | K00–03 | 0.2·$V_{SS}$ | | 0 | V |
| High level input voltage (2) | $V_{IH2}$ | | RESET | 0.15·$V_{SS}$ | | 0 | V |
| Low level input voltage (1) | $V_{IL1}$ | | K00–03 | $V_{SS}$ | | 0.8·$V_{SS}$ | V |
| Low level input voltage (2) | $V_{IL2}$ | | RESET | $V_{SS}$ | | 0.85·$V_{SS}$ | V |
| High level input current (1) | $I_{IH1}$ | $V_{IH1}$=0V, No pull-down | K00–03 | 0 | | 0.5 | μA |
| High level input current (2) | $I_{IH2}$ | $V_{IH2}$=0V, Pull-down | K00–03 | 10 | | 40 | μA |
| High level input current (3) | $I_{IH3}$ | $V_{IH3}$=0V, Pull-down | RESET | 30 | | 100 | μA |
| Low level input current | $I_{IL}$ | $V_{IL}$=$V_{SS}$ | K00–03 RESET, TEST | -0.5 | | 0 | μA |
| High level output current (1) | $I_{OH1}$ | $V_{OH1}$=0.1·$V_{SS}$ | R02, R03 | | | -1.0 | mA |
| High level output current (2) | $I_{OH2}$ | $V_{OH2}$=0.1·$V_{SS}$ (with protection resistor) | R00, R01 | | | -1.0 | mA |
| Low level output current (1) | $I_{OL1}$ | $V_{OL1}$=0.9·$V_{SS}$ | R02, R03 | 3.0 | | | mA |
| Low level output current (2) | $I_{OL2}$ | $V_{OL2}$=0.9·$V_{SS}$ (with protection resistor) | R00, R01 | 3.0 | | | mA |
| Common output current | $I_{OH3}$ | $V_{OH3}$=-0.05V | COM0–3 | | | -3 | μA |
| | $I_{OL3}$ | $V_{OL3}$=$V_{L3}$+0.05V | | 3 | | | μA |
| Segment output current (during LCD output) | $I_{OH4}$ | $V_{OH4}$=-0.05V | SEG0–14 | | | -3 | μA |
| | $I_{OL4}$ | $V_{OL4}$=$V_{L3}$+0.05V | | 3 | | | μA |
| Segment output current (during DC output) | $I_{OH5}$ | $V_{OH5}$=0.1·$V_{SS}$ | SEG0–14 | | | -300 | μA |
| | $I_{OL5}$ | $V_{OL5}$=0.9·$V_{SS}$ | | 300 | | | μA |

**E0C60L03**

Unless otherwise specified:

$V_{DD}$=0V, $V_{SS}$=-1.5V, fosc=32.768kHz, Ta=25°C, $V_{S2}$ is internal voltage, $C_1$=$C_2$=0.1μF

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|------|--------|-----------|--|------|------|------|------|
| High level input voltage (1) | $V_{IH1}$ | | K00–03 | 0.2·$V_{SS}$ | | 0 | V |
| High level input voltage (2) | $V_{IH2}$ | | RESET | 0.15·$V_{SS}$ | | 0 | V |
| Low level input voltage (1) | $V_{IL1}$ | | K00–03 | $V_{SS}$ | | 0.8·$V_{SS}$ | V |
| Low level input voltage (2) | $V_{IL2}$ | | RESET | $V_{SS}$ | | 0.85·$V_{SS}$ | V |
| High level input current (1) | $I_{IH1}$ | $V_{IH1}$=0V, No pull-down | K00–03 | 0 | | 0.5 | μA |
| High level input current (2) | $I_{IH2}$ | $V_{IH2}$=0V, Pull-down | K00–03 | 5.0 | | 20 | μA |
| High level input current (3) | $I_{IH3}$ | $V_{IH3}$=0V, Pull-down | RESET | 9.0 | | 100 | μA |
| Low level input current | $I_{IL}$ | $V_{IL}$=$V_{SS}$ | K00–03 RESET, TEST | -0.5 | | 0 | μA |
| High level output current (1) | $I_{OH1}$ | $V_{OH1}$=0.1·$V_{SS}$ | R02, R03 | | | -200 | μA |
| High level output current (2) | $I_{OH2}$ | $V_{OH2}$=0.1·$V_{SS}$ (with protection resistor) | R00, R01 | | | -200 | μA |
| Low level output current (1) | $I_{OL1}$ | $V_{OL1}$=0.9·$V_{SS}$ | R02, R03 | 700 | | | μA |
| Low level output current (2) | $I_{OL2}$ | $V_{OL2}$=0.9·$V_{SS}$ (with protection resistor) | R00, R01 | 700 | | | μA |
| Common output current | $I_{OH3}$ | $V_{OH3}$=-0.05V | COM0–3 | | | -3 | μA |
| | $I_{OL3}$ | $V_{OL3}$=$V_{L3}$+0.05V | | 3 | | | μA |
| Segment output current (during LCD output) | $I_{OH4}$ | $V_{OH4}$=-0.05V | SEG0–14 | | | -3 | μA |
| | $I_{OL4}$ | $V_{OL4}$=$V_{L3}$+0.05V | | 3 | | | μA |
| Segment output current (during DC output) | $I_{OH5}$ | $V_{OH5}$=0.1·$V_{SS}$ | SEG0–14 | | | -100 | μA |
| | $I_{OL5}$ | $V_{OL5}$=0.9·$V_{SS}$ | | 130 | | | μA |

## *6.4 Analog Circuit Characteristics and Current Consumption*

### E0C6003 (Crystal Oscillation)

Unless otherwise specified:

$V_{DD}$=0V, $V_{SS}$=-3.0V, $f_{OSC}$=32.768kHz, Ta=25°C, $C_G$=25pF, $V_{S2}$ is internal voltage, $C_1$=$C_2$=0.1µF

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|------|--------|-----------|--|------|------|------|------|
| LCD drive voltage | $V_{L1}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L1}$ | | $1/3 \cdot V_{SS}$ - 0.1 | $1/3 \cdot V_{SS}$ | $1/3 \cdot V_{SS}$ ×0.9 | V |
| | $V_{L2}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L2}$ | | $2/3 \cdot V_{SS}$ - 0.1 | $2/3 \cdot V_{SS}$ | $2/3 \cdot V_{SS}$ ×0.9 | V |
| | $V_{L3}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L3}$ | | | $V_{SS}$ | | V |
| Current consumption | $I_{HLT}$ | During HALT with LCD OFF | No panel load | | 1.0 | 2.5 | µA |
| | $I_{EXE1}$ | During operation with LCD OFF | | | 2.0 | 5.0 | µA |
| | $I_{EXE2}$ | During operation with power divider ON | | | 15 | 20 | µA |

### E0C60L03 (Crystal Oscillation)

Unless otherwise specified:

$V_{DD}$=0V, $V_{SS}$=-1.5V, $f_{OSC}$=32.768kHz, Ta=25°C, $C_G$=25pF, $V_{S2}$ is internal voltage, $C_1$=$C_2$=0.1µF

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|------|--------|-----------|--|------|------|------|------|
| LCD drive voltage | $V_{L1}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L1}$ | | $1/3 \cdot V_{S2}$ - 0.1 | $1/3 \cdot V_{S2}$ | $1/3 \cdot V_{S2}$ ×0.9 | V |
| | $V_{L2}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L2}$ | | $2/3 \cdot V_{S2}$ - 0.1 | $2/3 \cdot V_{S2}$ | $2/3 \cdot V_{S2}$ ×0.9 | V |
| | $V_{L3}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L3}$ | | $V_{S2}$ - 0.1 | $V_{S2}$ | $V_{S2}$ ×0.9 | V |
| Current consumption | $I_{HLT}$ | During HALT with LCD OFF | No panel load | | 1.0 | 2.5 | µA |
| | $I_{EXE1}$ | During operation with LCD OFF | | | 2.0 | 5.0 | µA |
| | $I_{EXE2}$ | During operation with power divider ON | | | 15 | 20 | µA |

## E0C6003 (CR Oscillation)

Unless otherwise specified:

$V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC}=65kHz$, $Ta=25°C$, $R_{CR}=470k\Omega$, $V_{S2}$ is internal voltage, $C_1=C_2=0.1\mu F$

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|------|--------|-----------|---|------|------|------|------|
| LCD drive voltage | $V_{L1}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L1}$ | | $1/3 \cdot V_{SS}$ - 0.1 | $1/3 \cdot V_{SS}$ | $1/3 \cdot V_{SS}$ ×0.9 | V |
| | $V_{L2}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L2}$ | | $2/3 \cdot V_{SS}$ - 0.1 | $2/3 \cdot V_{SS}$ | $2/3 \cdot V_{SS}$ ×0.9 | V |
| | $V_{L3}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L3}$ | | | $V_{SS}$ | | V |
| Current consumption | $I_{HLT}$ | During HALT with LCD OFF | No panel | | 8 | 15 | μA |
| | $I_{EXE1}$ | During operation with LCD OFF | load | | 15 | 20 | μA |
| | $I_{EXE2}$ | During operation with power divider ON | | | 25 | 30 | μA |

## E0C60L03 (CR Oscillation)

Unless otherwise specified:

$V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{OSC}=65kHz$, $Ta=25°C$, $R_{CR}=470k\Omega$, $V_{S2}$ is internal voltage, $C_1=C_2=0.1\mu F$

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|------|--------|-----------|---|------|------|------|------|
| LCD drive voltage | $V_{L1}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L1}$ | | $1/3 \cdot V_{S2}$ - 0.1 | $1/3 \cdot V_{S2}$ | $1/3 \cdot V_{S2}$ ×0.9 | V |
| | $V_{L2}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L2}$ | | $2/3 \cdot V_{S2}$ - 0.1 | $2/3 \cdot V_{S2}$ | $2/3 \cdot V_{S2}$ ×0.9 | V |
| | $V_{L3}$ | Connect 1 MΩ load resistor between $V_{DD}$ and segment driver (SEG0–SEG14) when segment driver's level is $V_{L3}$ | | $V_{S2}$ - 0.1 | $V_{S2}$ | $V_{S2}$ ×0.9 | V |
| Current consumption | $I_{HLT}$ | During HALT with LCD OFF | No panel | | 8 | 15 | μA |
| | $I_{EXE1}$ | During operation with LCD OFF | load | | 15 | 20 | μA |
| | $I_{EXE2}$ | During operation with power divider ON | | | 25 | 30 | μA |

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## *6.5 Oscillation Characteristics*

Oscillation characteristics will vary according to different conditions (elements used, board pattern). Use the following characteristics are as reference values.

### E0C6003 Crystal Oscillation

Unless otherwise specified:

$V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC}=32.768kHz$, Crystal: C-002R ($C_I=35k\Omega$), $C_G=25pF$, $C_D$=built-in, Ta=25°C

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation start voltage | Vsta | tsta≤5sec (Vss) | -1.8 | | | V |
| Oscillation stop voltage | Vstp | tstp≤10sec (Vss) | -1.8 | | | V |
| Built-in capacitance (drain) | $C_D$ | Including the parasitic capacitance inside the IC (in chip) | | 20 | | pF |
| Frequency/voltage deviation | ∂f/∂V | Vss=-1.8 to -3.6V | | | 5 | ppm |
| Frequency/IC deviation | ∂f/∂IC | | -10 | | 10 | ppm |
| Frequency adjustment range | ∂f/∂CG | CG=5 to 25pF | 40 | | | ppm |
| Harmonic oscillation start voltage | Vhho | CG=5pF (Vss) | | | -3.6 | V |
| Permitted leak resistance | Rleak | Between OSC1 and VDD | 200 | | | MΩ |

### E0C60L03 Crystal Oscillation

Unless otherwise specified:

$V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{OSC}=32.768kHz$, Crystal: C-002R ($C_I=35k\Omega$), $C_G=25pF$, $C_D$=built-in, Ta=25°C

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation start voltage | Vsta | tsta≤5sec (Vss) | -1.2 | | | V |
| Oscillation stop voltage | Vstp | tstp≤10sec (Vss) | -1.2 | | | V |
| Built-in capacitance (drain) | $C_D$ | Including the parasitic capacitance inside the IC (in chip) | | 20 | | pF |
| Frequency/voltage deviation | ∂f/∂V | Vss=-1.2 to -2.0V | | | 5 | ppm |
| Frequency/IC deviation | ∂f/∂IC | | -10 | | 10 | ppm |
| Frequency adjustment range | ∂f/∂CG | CG=5 to 25pF | 40 | | | ppm |
| Harmonic oscillation start voltage | Vhho | CG=5pF (Vss) | | | -2.0 | V |
| Permitted leak resistance | Rleak | Between OSC1 and VDD | 200 | | | MΩ |

### E0C6003 CR Oscillation

Unless otherwise specified:

$V_{DD}=0V$, $V_{SS}=-3.0V$, $R_{CR}=470k\Omega$, Ta=25°C

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency dispersion | fosc | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | Vsta | (Vss) | -1.8 | | | V |
| Oscillation start time | tsta | Vss=-1.8 to -3.6V | | 3 | | mS |
| Oscillation stop voltage | Vstp | (Vss) | -1.8 | | | V |

### E0C60L03 CR Oscillation

Unless otherwise specified:

$V_{DD}=0V$, $V_{SS}=-1.5V$, $R_{CR}=470k\Omega$, Ta=25°C

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency dispersion | fosc | | -20 | 65kHz | 20 | % |
| Oscillation start voltage | Vsta | (Vss) | -1.2 | | | V |
| Oscillation start time | tsta | Vss=-1.2 to -2.0V | | 3 | | mS |
| Oscillation stop voltage | Vstp | (Vss) | -1.2 | | | V |

# CHAPTER 7    CERAMIC PACKAGE FOR TEST SAMPLES
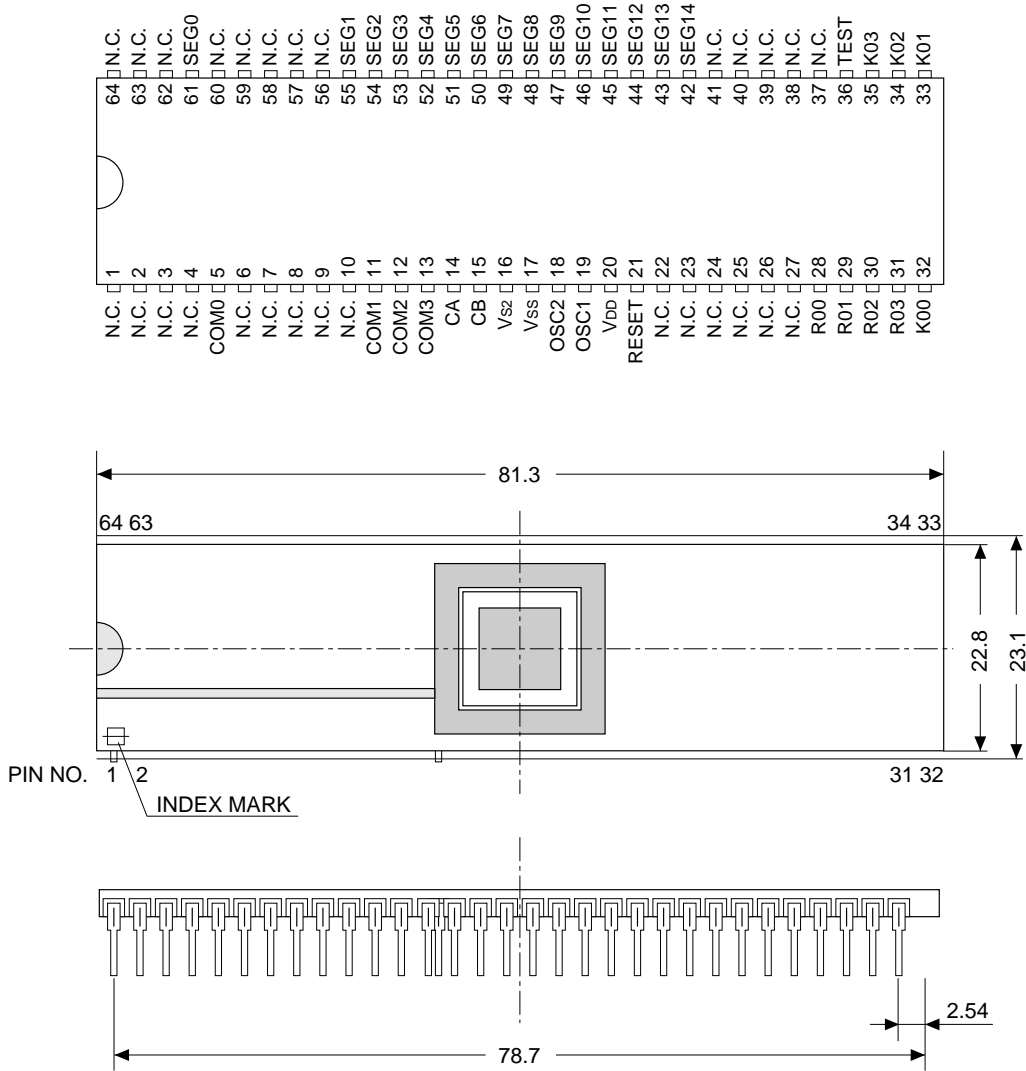


(Unit: mm)

# CHAPTER *8* PRECAUTIONS ON MOUNTING

## <Oscillation Circuit>

● Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when using a crystal oscillator, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

● Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

(1) Components which are connected to the OSC1 and OSC2 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

(2) As shown in the right hand figure, make a $V_{DD}$ pattern as large as possible at circumscription of the OSC1 and OSC2 terminals and the components connected to these terminals.
Furthermore, do not use this $V_{DD}$ pattern for any purpose other than the oscillation system.



Sample $V_{DD}$ pattern

● In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 and $V_{SS}$, please keep enough distance between OSC1 and $V_{SS}$ or other signals on the board pattern.

## <Reset Circuit>
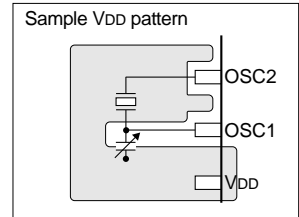
● The power-on reset signal which is input to the RESET terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
When the built-in pull-down resistor is added to the RESET terminal by mask option, take into consideration dispersion of the resistance for setting the constant.

● In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the RESET terminal in the shortest line.

## <Power Supply Circuit>

● Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

(1) The power supply should be connected to the $V_{DD}$ and $V_{SS}$ terminal with patterns as short and large as possible.

(2) When connecting between the $V_{DD}$ and $V_{SS}$ terminals with a bypass capacitor, the terminals should be connected as short as possible.



Bypass capacitor connection example
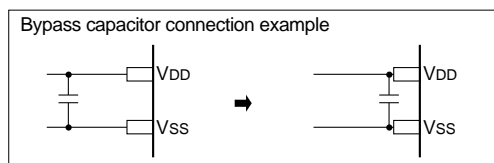
(3) Components which are connected to the $V_{S2}$ terminal, such as a capacitor, should be connected in the shortest line.

### <Arrangement of Signal Lines>

● In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.

● When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



### <Precautions for Visible Radiation (when bare chip is mounted)>
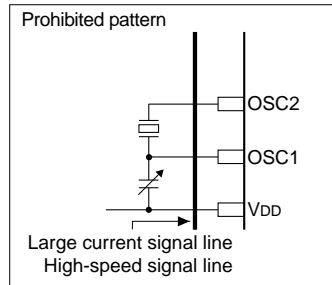
● Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

   (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

   (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

   (3) As well as the face of the IC, shield the back and side too.

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# EPSON International Sales Operations

## AMERICA

**EPSON ELECTRONICS AMERICA, INC.**

**- HEADQUARTERS -**
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Phone: +1-310-955-5300   Fax: +1-310-955-5400

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Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020   Fax: +1-770-777-2637

## EUROPE

**EPSON EUROPE ELECTRONICS GmbH**

**- HEADQUARTERS -**
Riesstrasse 15
80992 Muenchen, GERMANY
Phone: +49-(0)89-14005-0   Fax: +49-(0)89-14005-110

**- GERMANY -**
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**- CHINA -**
**EPSON (CHINA) CO., LTD.**
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**- HONG KONG, CHINA -**
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Telex: 24444 EPSONTB

**HSINCHU OFFICE**
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HsinChu 300, TAIWAN, R.O.C.
Phone: 03-573-9900   Fax: 03-573-9169

**- SINGAPORE -**
**EPSON SINGAPORE PTE., LTD.**
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911   Fax: +65-334-2716

**- KOREA -**
**SEIKO EPSON CORPORATION KOREA OFFICE**
50F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone: 02-784-6027   Fax: 02-767-3677

**- JAPAN -**
**SEIKO EPSON CORPORATION**
**ELECTRONIC DEVICES MARKETING DIVISION**

**Electronic Device Marketing Department**
**IC Marketing & Engineering Group**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816   Fax: +81-(0)42-587-5624

**ED International Marketing Department I (Europe & U.S.A.)**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812   Fax: +81-(0)42-587-5564

**ED International Marketing Department II (Asia)**
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814   Fax: +81-(0)42-587-5110

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