MF1007-02

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C62M2 TECHNICAL MANUAL

E0C62M2 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

CHAPTER 1 OVERVIEW

The E0C62M2 is a CMOS 4-bit single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM (1,536 words, 12 bits to a word), RAM (128 words, 4 bits to a word), dual slope type A/D converter, attenuator circuit for various measurement modes, LCD driver, serial interface, and other circuits. It is especially suitable for measurement and LCD display systems such as a digital multimeter.

1.1 Features

CMOS LSI 4-bit parallel processing

Clock ..... 32.768 kHz (Typ.)

Instruction set ..... 100 types

Instruction execution time ..... 153 µsec, 214 µsec, 366 µsec

ROM capacity ..... 1,536 words × 12 bits

RAM capacity ..... 128 words × 4 bits

A/D converter ..... Dual slope type
Resolution : Conversion time (2 stages)
4,370 counts : 400 msec
A/D conversion precision: ±0.1% (operating temperature range: 20°C to 40°C)
441 counts : 100 msec (High speed mode)
3 integral resistors can be connected
Current, voltage and resistance can be measured
AC voltage/AC current can be measured using an external rectifier circuit
Continuity check mode built-in (measurement value can be displayed)
Reference voltage generation circuit built-in

Input port ..... 8 bits (pull down resistors can be supplemented by mask option)

Output port ..... 4 bits

Buzzer output ..... 2 ports (BZ, $\overline{BZ}$) [1 system]

I/O port ..... 4 bits

Serial interface ..... 1 port for data input
1 port for data output
1 port for clock input/output
} These ports can be switched to general I/O port

LCD driver ..... 16 segments × 3 or 4 commons (can be switched using software)
LCD drive voltage generation circuit built-in (V_{L1}, V_{L2}, V_{L3})
Compatible with 3 V LCD panel

Timer ..... Built-in

Watchdog timer ..... Built-in

SVD circuit ..... 2.3 ± 0.15 V
(supply voltage detection)

External interrupt ..... Input port interrupt: 2 systems

Internal interrupt ..... A/D interrupt: 1 system
Timer interrupt: 1 system
Serial interface interrupt: 1 system

Supply voltage ..... 3 V (2.15 V to 3.5 V)

Current consumption (Typ.) ..... During HALT: 3 µA (3 V)
During A/D operation: 0.9 mA (3 V, in DC measurement)
1.1 mA (3 V, in AC measurement)

Package ..... QFP5-80pin (plastic/ceramic), QFP14-80pin (plastic) or chip

1.2 Block Diagram

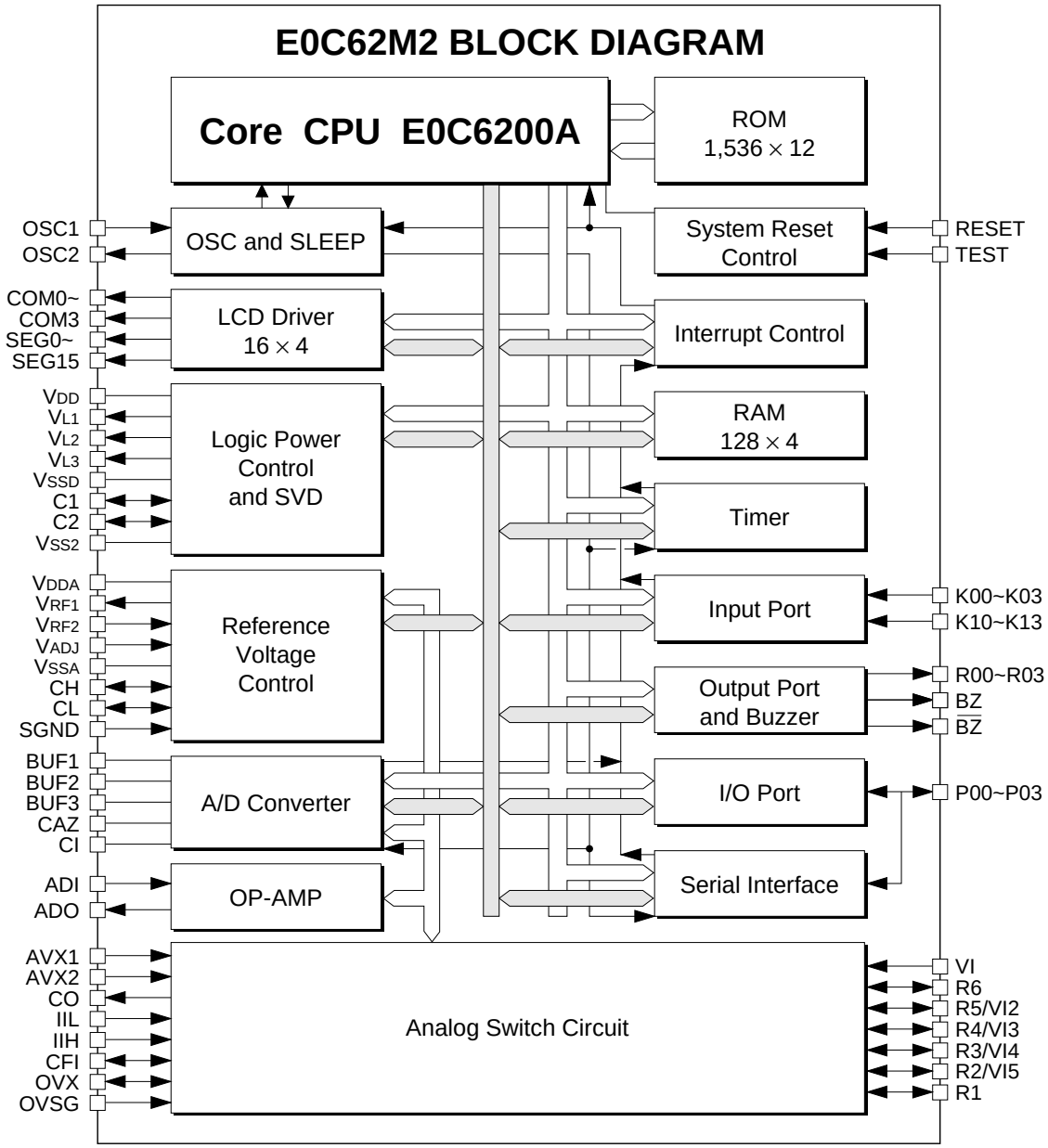
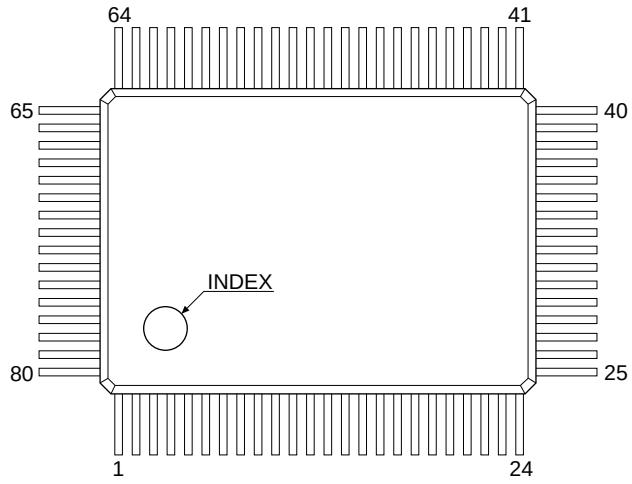


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

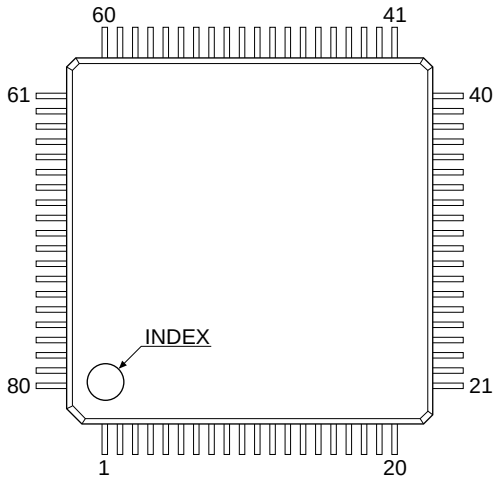
QFP5-80pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG15	21	V_{RF1}	41	OVSG	61	$\overline{BZ}$
2	COM0	22	V_{RF2}	42	R1	62	P00/SIN
3	COM1	23	CH	43	R2/VI5	63	P01/SOUT
4	COM2	24	CL	44	R3/VI4	64	P02/SCLK
5	COM3	25	ADI	45	R4/VI3	65	P03/SRDY
6	V_{L1}	26	ADO	46	R5/VI2	66	SEG0
7	V_{L2}	27	AVX1	47	R6	67	SEG1
8	V_{L3}	28	AVX2	48	K00	68	SEG2
9	V_{DD}	29	CO	49	K01	69	SEG3
10	OSC1	30	CAZ	50	K02	70	SEG4
11	OSC2	31	CI	51	K03	71	SEG5
12	RESET	32	BUF1	52	K10	72	SEG6
13	TEST	33	BUF2	53	K11	73	SEG7
14	V_{SSD}	34	BUF3	54	K12	74	SEG8
15	C1	35	IIL	55	K13	75	SEG9
16	C2	36	IIH	56	R00	76	SEG10
17	V_{SS2}	37	CFI	57	R01	77	SEG11
18	V_{DDA}	38	SGND	58	R02	78	SEG12
19	V_{SSA}	39	VI	59	R03	79	SEG13
20	V_{ADJ}	40	OVX	60	BZ	80	SEG14

Fig. 1.3.1 Pin layout diagram (QFP5-80pin)

QFP14-80pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	COM2	21	CL	41	R3/VI4	61	P02/SCLK
2	COM3	22	ADI	42	R4/VI3	62	P03/SRDY
3	V_{L1}	23	ADO	43	R5/VI2	63	SEG0
4	V_{L2}	24	AVX1	44	R6	64	SEG1
5	V_{L3}	25	AVX2	45	K00	65	SEG2
6	V_{DD}	26	CO	46	K01	66	SEG3
7	OSC1	27	CAZ	47	K02	67	SEG4
8	OSC2	28	CI	48	K03	68	SEG5
9	RESET	29	BUF1	49	K10	69	SEG6
10	TEST	30	BUF2	50	K11	70	SEG7
11	V_{SSD}	31	BUF3	51	K12	71	SEG8
12	C1	32	IIL	52	K13	72	SEG9
13	C2	33	IIH	53	R00	73	SEG10
14	V_{SS2}	34	CFI	54	R01	74	SEG11
15	V_{DDA}	35	SGND	55	R02	75	SEG12
16	V_{SSA}	36	VI	56	R03	76	SEG13
17	V_{ADJ}	37	OVX	57	BZ	77	SEG14
18	V_{RF1}	38	OVSG	58	$\overline{BZ}$	78	SEG15
19	V_{RF2}	39	R1	59	P00/SIN	79	COM0
20	CH	40	R2/VI5	60	P01/SOUT	80	COM1

Fig. 1.3.2 Pin layout diagram (QFP14-80pin)

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No. (QFP5)	Pin No. (QFP14)	In/Out	Function
V_{DD}	9	6	(I)	Digital system power supply pin (+)
V_{DDA}	18	15	(I)	Analog system power supply pin (+)
V_{SSD}	14	11	(I)	Digital system power supply pin (–)
V_{SSA}	19	16	(I)	Analog system GND pin (same voltage with V_{SSD})
V_{SS2}	17	14	(O)	Analog system power supply pin (boosted voltage)
C1, C2	15, 16	12, 13	O	Booster capacitor connecting pins for analog system power supply (V_{SS2})
OSC1	10	7	I	Crystal oscillation input pin: 32.768 kHz
OSC2	11	8	O	Crystal oscillation output pin
K00~K13	48~55	45~52	I	Input pins
R00~R03	56~59	53~56	O	Output pins
BZ, $\overline{BZ}$	60, 61	57, 58	O	Buzzer signal output pins
P00~P03	62~65	59~62	I/O	I/O pins
V_{L1}~V_{L3}	6~8	3~5	O	LCD system voltage output pin
COM0~3	2~5	79, 80, 1, 2	O	LCD common output pins (1/3, 1/4 duty, programmable)
SEG0~15	66~80, 1	63~78	O	LCD segment output pin (DC output may be selected by mask option)
V_{ADJ}	20	17	–	Reference voltage adjustment pin
V_{RF1}	21	18	–	Reference voltage output pin
V_{RF2}	22	19	–	Reference voltage output pin
ADI	25	22	I	OP-AMP inverted input pin for AC-DC conversion
ADO	26	23	O	OP-AMP output pin for AC-DC conversion
AVX1	27	24	–	AC-DC converted voltage input pin
AVX2	28	25	–	AC-DC converted voltage input pin
IIL, IIH	35, 36	32, 33	–	Input pins for current measurement
VI	39	36	–	Input pin for voltage measurement
R1	42	39	–	Reference resistor connecting pin (100 Ω)
R2/VI5	43	40	–	Reference resistor connecting pin (1 kΩ)
R3/VI4	44	41	–	Reference resistor connecting pin (10 kΩ)
R4/VI3	45	42	–	Reference resistor connecting pin (101 kΩ)
R5/VI2	46	43	–	Reference resistor connecting pin (1.11 MΩ)
R6	47	44	–	Reference resistor connecting pin (10 MΩ)
OVX	40	37	–	Reference resistor voltage input pin for resistance measurement
OVSG	41	38	–	Reference resistor voltage input pin for resistance measurement
SGND	38	35	–	GND for measurement
CO	29	26	–	Dummy pad
CAZ	30	27	–	Capacitor connecting pin for offset voltage zero adjustment
CI	31	28	–	Integral capacitor connecting pin
BUF1~3	32~34	29~31	–	Buffer AMP output, integral resistor connecting pin
CFI	37	34	–	Noise rejection filter connecting pin
CH	23	20	–	Capacitor connecting pin for reference voltage control
CL	24	21	–	Capacitor connecting pin for reference voltage control
TEST	13	10	I	Testing input pin
RESET	12	9	I	Initial reset input pin

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

With a single external power supply (3 V *1) supplied to VDD/VDDA through VSSD/VSSA, the E0C62M2 generates the necessary internal voltage with the regulated voltage circuit (<VL1, VL2, VL3> for LCD driving), the voltage booster (<VSS2> for analog system) and the reference voltage generator (<VRF1> for A/D converter).
Figure 2.1.1 shows the configuration of power supply.

*1 Supply voltage: 2.15 to 3.5 V

Note: • *External loads cannot be driven by the regulated voltage and voltage booster circuit's output voltage.*

• *See Chapter 7, "ELECTRICAL CHARACTERISTICS" for voltage values.*

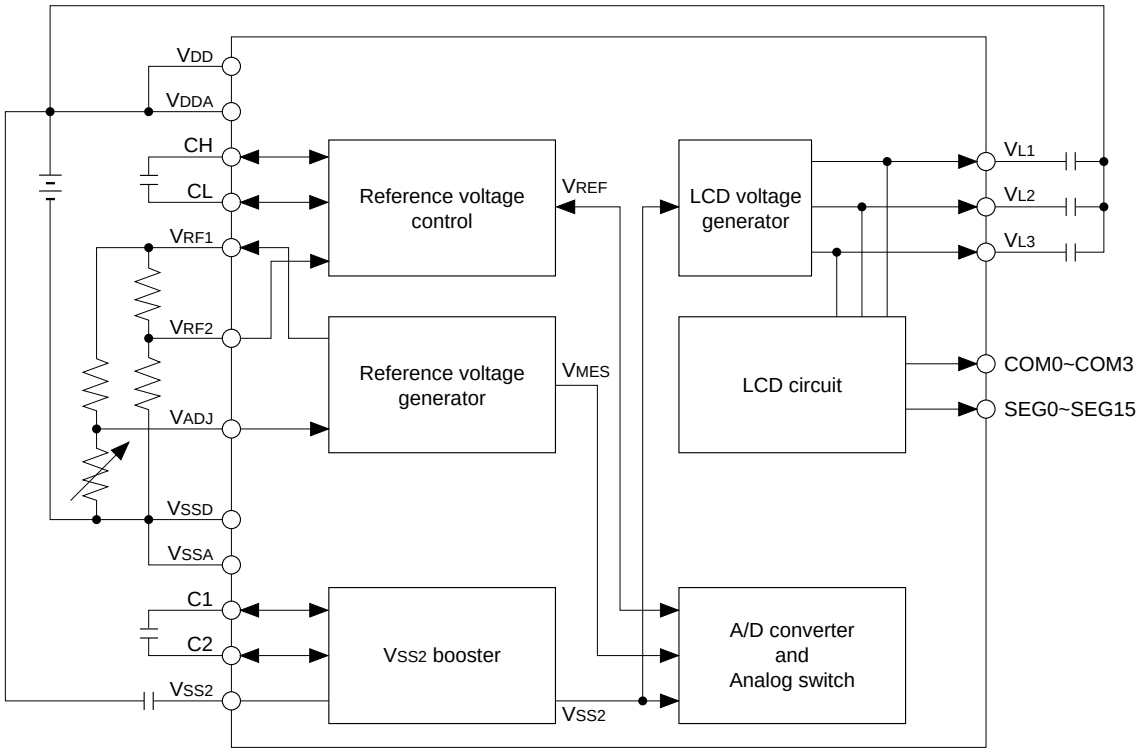


Fig. 2.1.1 Configuration of power supply

2.1.1 Boosted voltage <VSS2> for analog system

Making VDD the standard (GND), the E0C62M2 voltage booster doubles the supply voltage input from the VDD–VSSD terminals to generate VSS2.
VSS2 is used to operate the analog circuits (A/D converter, analog switch circuit, reference voltage generator and LCD power generator) in the E0C62M2. This voltage can be turned ON and OFF by programming. The VSS2 booster circuit also supplies the clock to the A/D converter and the LCD driver after dividing the clock (32.768 kHz) from the crystal oscillation circuit. Therefore, the VSS2 booster should be turned ON before starting the A/D converter and/or the LCD driver operations. See Section 4.13, "VSS2 Booster" for details.

Figure 2.1.1.1 shows the configuration of the VSS2 circuit.

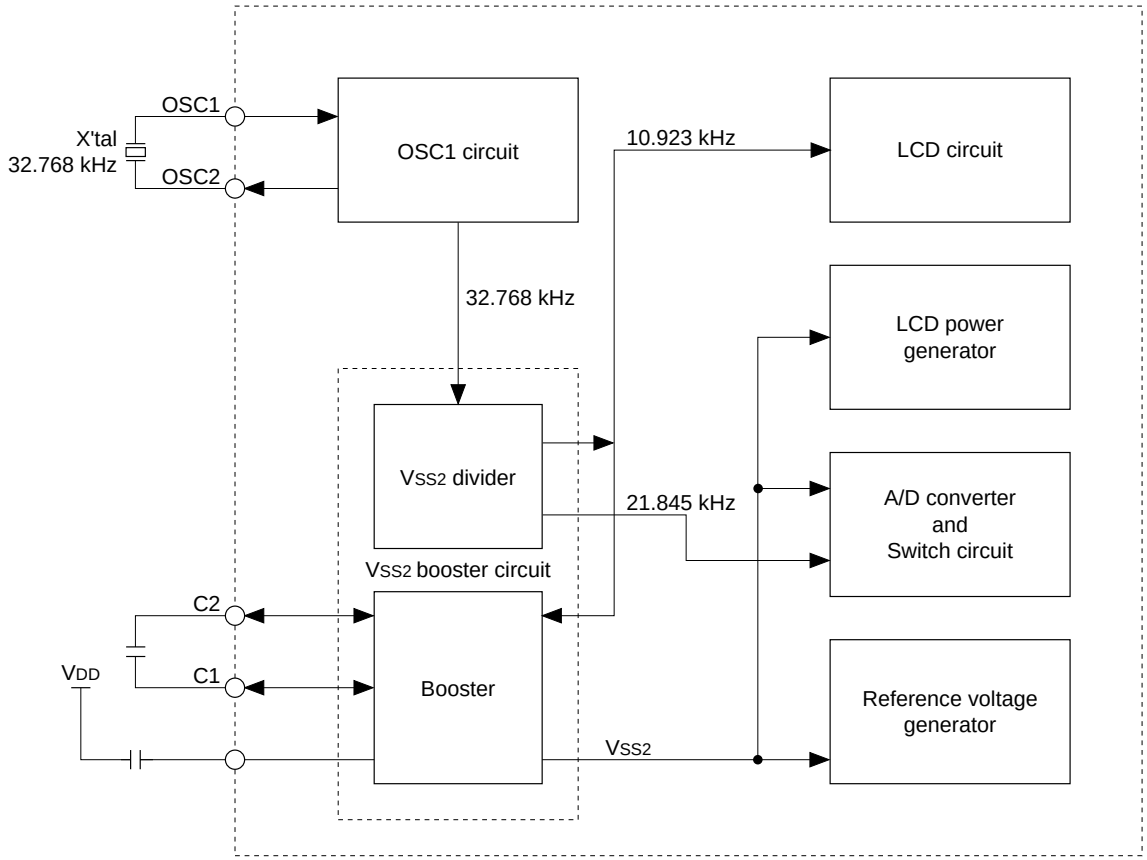


Fig. 2.1.1.1 Configuration of VSS2 circuit

2.1.2 Voltage <VL1, VL2 and VL3> for LCD driving

VL1, VL2 and VL3 are the voltages for LCD driving, and are generated by the internal LCD power generator with VDD as the standard (GND). The LCD power generator operates with the VSS2 voltage as the power supply, and can be turned ON and OFF by programming.
See Chapter 7, "ELECTRICAL CHARACTERISTICS" for the output voltage values.

2.1.3 Reference voltage <VRF1, VRF2> for A/D converter

VRF1 and VRF2 are reference voltage for the A/D converter. The VRF1 voltage is generated by the reference voltage generator in the E0C62M2, and the VRF2 voltage is generated by dividing using resisters outside of the E0C62M2.
The reference voltage generator automatically starts to operate and outputs VRF1 and VRF2 by turning the A/D converter ON.
See Section 4.11, "A/D Converter" for details of the circuit configuration and the operation.

2.2 Initial Reset

To initialize the E0C62M2 circuits, initial reset must be executed. There are two ways of doing this.

(1) External initial reset using the RESET terminal
(2) Initial reset by the watchdog timer

Be sure to use reset function (1) when turning the power ON and be sure to initialize securely. In normal operation, the circuits may be initialized by any of the above two types.

Figure 2.2.1 shows the configuration of the initial reset circuit.

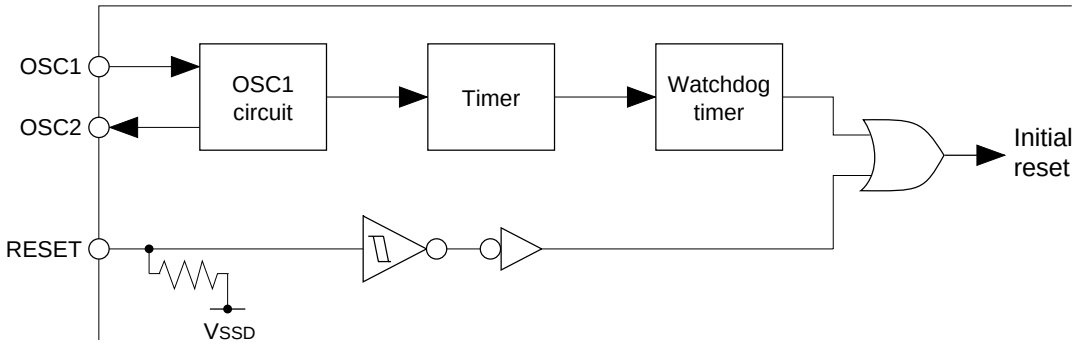


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal (RESET)

Initial reset can be executed externally by setting the reset terminal to a high level. After that, when the reset terminal goes low, the initial reset is released. However, the clock is not supplied to the CPU until the 1 Hz signal from the timer goes high after an initial reset is released. When the 1 Hz signal goes high, the CPU clock is supplied and the CPU starts to operate.
Maintain the reset terminal at a high level at least 2.0 msec to securely perform the initial reset after turning the power ON.

Figure 2.2.1.1 shows the initial reset timing with the power ON.

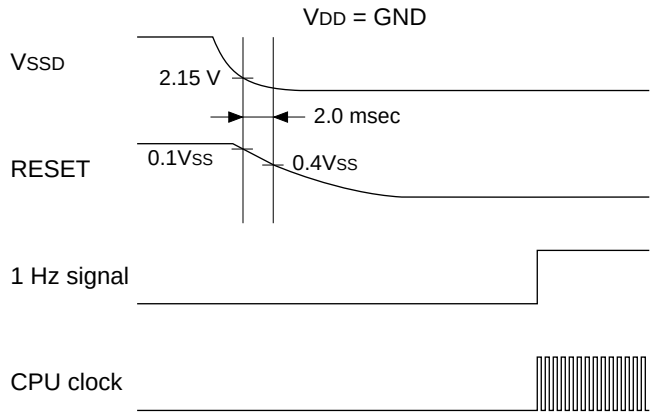


Fig. 2.2.1.1 Initial reset at power ON

2.2.2 Watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See Section 4.2, "Resetting Watchdog Timer" for details.
However, do not perform an initial reset when turning the power ON by this function.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in the table below.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
New page pointer	NPP	4	1H
Stack pointer	SP	8	Undefined
Index register IX	IX	8	Undefined
Index register IY	IY	8	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	—	*1

*1 See Section 4.1, "Memory Map".

2.3 Test Terminal (TEST)

This is the terminal that is used at the time of the factory inspection of the IC. During normal operation, connect the TEST terminal to V_{SSD}/V_{SSA}.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C62M2 employs the 4-bit core CPU E0C6200A for the CPU, so that register configuration, instructions and so forth are virtually identical to those in other family processors using the E0C6200A.
Refer to "E0C6200/6200A Core CPU Manual" for details about the E0C6200A.
Note the following points with regard to the E0C62M2:

(1) Because the ROM capacity is 1,536 words, bank bits are unnecessary and PCB and NBP are not used.

(2) RAM is set up to one page only, so the page portion (XP, YP) of the index register that specifies addresses is invalid. (The four bits of XP and YP are ignored.)

3.2 ROM

The built-in ROM, a mask ROM for storing the program, has a capacity of 1,536 steps, 12 bits each. The program area is 6 pages (0–5), each of 256 steps (00H–FFH). After initial reset, the program beginning address is page 1, step 00H. The interrupt vector is allocated to page 1, steps 02H–0FH.

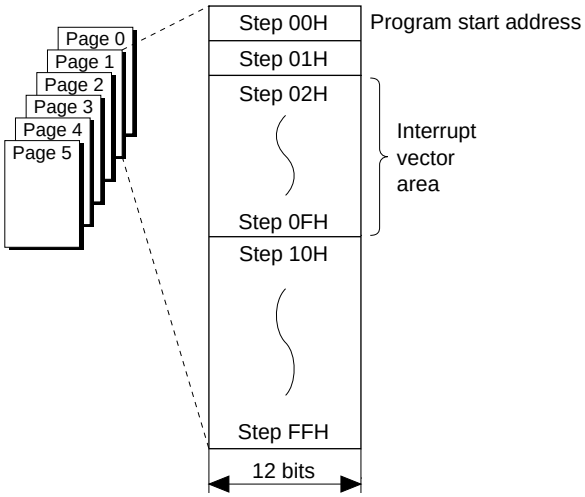


Fig. 3.2.1 ROM configuration

3.3 RAM

The RAM, a data memory storing a variety of data, has a capacity of 128 words, each of four bits. When programming, keep the following points in mind.

(1) Part of the data memory can be used as stack area when subroutine calls and saving registers, so be careful not to overlap the data area and stack area.

(2) Subroutine calls and interrupts take up three words of the stack area.

(3) The data memory 000H–00FH is for the register pointers (RP), and is the addressable memory register area.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

Peripheral circuits (timer, I/O, and so on) of the E0C62M2 are memory mapped, and interfaced with the CPU. Thus, all the peripheral circuits can be controlled by using the memory operation command to access the I/O memory in the memory map.
The following sections describe how the peripheral circuits operation.

4.1 Memory Map

Data memory of the E0C62M2 has an address space of 180 words, of which 16 words are allocated to display memory and 36 words to I/O memory.
Figure 4.1.1 present the overall memory maps of the E0C62M2, and Tables 4.1.1(a)–(e) the peripheral circuits' (I/O space) memory maps.
Table 4.1.2 shows the A/D converter measurement function list and Table 4.1.3 shows the A/D converter measurement range list.

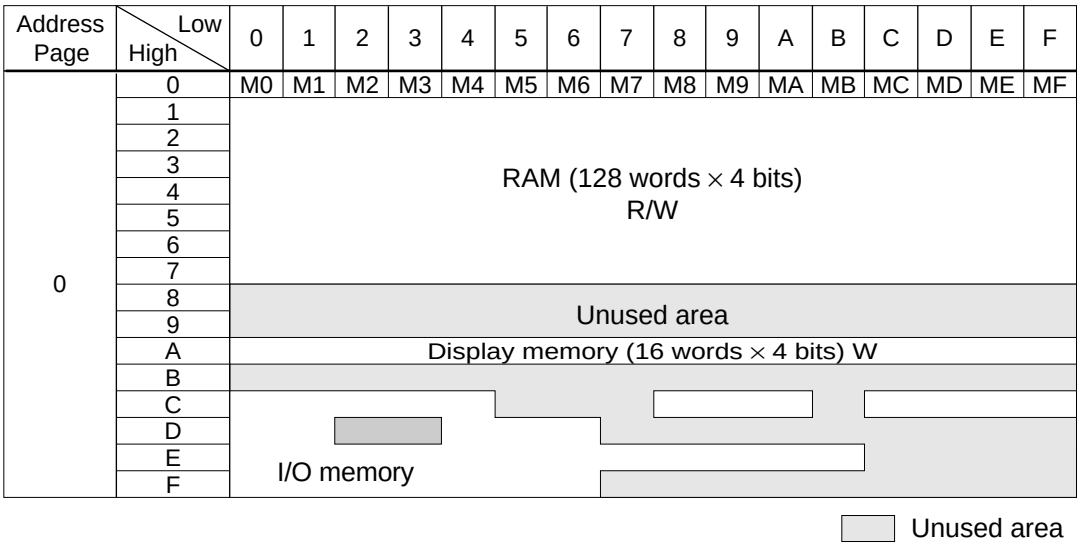


Fig. 4.1.1 Memory map

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these area.

Table 4.1.1(a) I/O memory map (C0H–CAH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
					SIK02	0	Enable	Disable	Interrupt selection register (K02)
	R/W				SIK01	0	Enable	Disable	Interrupt selection register (K01)
					SIK00	0	Enable	Disable	Interrupt selection register (K00)
C1H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
C2H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
					SIK12	0	Enable	Disable	Interrupt selection register (K12)
	R/W				SIK11	0	Enable	Disable	Interrupt selection register (K11)
					SIK10	0	Enable	Disable	Interrupt selection register (K10)
C3H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
C4H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00–R03)
					R02	0	High	Low	
	R/W				R01	0	High	Low	
					R00	0	High	Low	
C8H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03) (ESIF = 0)
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
	When the serial I/F is used (ESIF = 1):				IOC03	0	Output	Input	Master mode: P03 I/O control register
	P00 = SIN (in), P01 = SOUT (out),				IOC03	0	1	0	Slave mode: General-purpose register
	P02 = SCLK (master: out, slave: in),				IOC02	0	1	0	General-purpose register
	P03 = SRDY (slave: out),				IOC01	0	1	0	
	P03 = I/O port (master: in/out)				IOC00	0	1	0	
C9H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Pull down control register (P00–P03) (ESIF = 0)
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
	When the serial I/F is used (ESIF = 1):				PUL03	1	On	Off	Master mode: P03 pull down control register
	P00 = SIN (in), P01 = SOUT (out),				PUL03	1	1	0	Slave mode: General-purpose register
	P02 = SCLK (master: out, slave: in),				PUL02	1	1	0	Master mode: General-purpose register
	P03 = SRDY (slave: out),				PUL02	1	On	Off	Slave mode: SCKL pull down control register
	P03 = I/O port (master: in/out)				PUL01	1	1	0	General-purpose register
					PUL00	1	On	Off	SIN pull down control register
CAH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port (P00–P03) (ESIF = 0)
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
	When the serial I/F is used (ESIF = 1):				P03	– *2	High	Low	Master mode: I/O port P03
	P00 = SIN (in), P01 = SOUT (out),				P03	– *2	1	0	Slave mode: General-purpose register
	P02 = SCLK (master: out, slave: in),				P02	– *2	1	0	General-purpose register
	P03 = SRDY (slave: out),				P01	– *2	1	0	
	P03 = I/O port (master: in/out)				P00	– *2	1	0	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read

Table 4.1.1(b) I/O memory map (CCH–CFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CCH	0	0	SCTRG	ESIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		SCTRG(W)	– *2	Trigger	–	Serial interface clock trigger (writing)
					SCTRG(R)	0	Run	Stop	Serial interface clock status (reading)
					ESIF	0	SIF port	I/O port	P0 port function selection
CDH	SDP	SCPS	SCS1	SCS0	SDP	0	LSB first	MSB first	Serial data input/output permutation
					SCPS	0	↑	↓	Serial interface clock phase selection
	R/W				SCS1	0			Serial interface clock mode selection
					SCS0	0			0: Slave, 1: CLK/2, 2: CLK, 3: CLK
CEH	SD3	SD2	SD1	SD0	SD3	– *2			MSB
					SD2	– *2			Serial interface data (low-order 4 bits)
	R/W				SD1	– *2			
					SD0	– *2			LSB
CFH	SD7	SD6	SD5	SD4	SD7	– *2			MSB
					SD6	– *2			Serial interface data (high-order 4 bits)
	R/W				SD5	– *2			
					SD4	– *2			LSB

Table 4.1.1(c) I/O memory map (D0H–D6H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
D0H	0	0	BZFQ	R	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		BZFQ	0	2 kHz	4 kHz	Buzzer signal frequency selection
					R	0	1	0	1 bit general-purpose register
D1H	0	BSHOT	BZFNC	BZON	0 *5	– *2			Unused
					BSHOT*5	– *2	One-shot	–	One-shot buzzer signal (31 msec) output trigger
	R	W	R/W		BZFNC	0	Intermittent	Continuous	Continuous/intermittent output selection
					BZON	0	On	Off	Buzzer signal output control
D4H	0	0	WDRST	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		W		WDRST*5	– *2	Reset	–	Watchdog timer reset
					TMRST*5	– *2	Reset	–	Clock timer and watchdog timer reset
D5H	TM3	TM2	TM1	TM0	TM3	– *3			Clock timer data (16 Hz)
					TM2	– *3			Clock timer data (32 Hz)
	R				TM1	– *3			Clock timer data (64 Hz)
					TM0	– *3			Clock timer data (128 Hz)
D6H	TM7	TM6	TM5	TM4	TM7	– *3			Clock timer data (1 Hz)
					TM6	– *3			Clock timer data (2 Hz)
	R				TM5	– *3			Clock timer data (4 Hz)
					TM4	– *3			Clock timer data (8 Hz)

Table 4.1.1(d) I/O memory map (E0H–EBH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
E0H	–	–	–	VSS2	–	– *3			Unused (Undefined when reading)
					–	– *3			Unused (Undefined when reading)
	R			R/W	–	– *3			Unused (Undefined when reading)
					VSS2	0	On	Off	VSS2 booster control
E1H	LOFF	0	LDTY	LPWR	LOFF	0	All off	Normal	LCD display all off / normal switch
					0 *5	– *2			Unused
	R/W	R	R/W		LDTY	0	1/3	1/4	LCD drive duty selection
					LPWR	0	On	Off	LCD driver On/Off
E2H	BUFF	IIN	ADSPD	ADON	BUFF	0	–	–	Fix at 0
					IIN	0	IIH	IIL	Current measurement terminal switching
	R/W				ADSPD	0	100 mS	400 mS	A/D conversion speed switching
					ADON	0	On	Off	A/D converter On/Off
E3H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off
E4H	0	FNC2	FNC1	FNC0	0 *5	– *2			Unused
					FNC2	0			Measurement function selection (See Table 4.1.2)
	R	R/W			FNC1	0			
					FNC0	0			
E5H	0	RNG2	RNG1	RNG0	0 *5	– *2			Unused
					RNG2	0			Measurement range selection (See Table 4.1.3)
	R	R/W			RNG1	0			
					RNG0	0			
E6H	0	0	0	ADP	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ADP	1	Positive	Negative	A/D converter polarity judgment
E7H	DSC03	DSC02	DSC01	DSC00	DSC03	0	1	0	A/D conversion data (00–03)
					DSC02	0	1	0	
	R				DSC01	0	1	0	
					DSC00	0	1	0	
E8H	DSC13	DSC12	DSC11	DSC10	DSC13	0	1	0	A/D conversion data (10–13)
					DSC12	0	1	0	
	R				DSC11	0	1	0	
					DSC10	0	1	0	
E9H	DSC23	DSC22	DSC21	DSC20	DSC23	0	1	0	A/D conversion data (20–23)
					DSC22	0	1	0	
	R				DSC21	0	1	0	
					DSC20	0	1	0	
EAH	0	DSC32	DSC31	DSC30	0 *5	– *2			Unused
					DSC32	0	1	0	A/D conversion data (30–32)
	R				DSC31	0	1	0	
					DSC30	0	1	0	
EBH	0	IDR	STS1	STS0	0 *5	– *2			Unused
					IDR	0	Invalid	Effective	Read data status
	R				STS1	0			A/D conversion status 0: auto zero adjustment,
					STS0	0			1: input integral, 3: reverse integral

Table 4.1.1(e) I/O memory map (F0H–F6H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	EIK1	EIK0	EISIF	EIAD	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
	R/W				EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT16	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F2H	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F3H	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
F4H	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial interface)
F5H	IT1	IT2	IT16	IT32	IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT16 *4	0	Yes	No	Interrupt factor flag (Clock timer 16 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)
F6H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)

Table 4.1.2 A/D converter measurement function list

Address	D3	D2 FNC2	D1 FNC1	D0 FNC0	Measurement function	Integral resistor normal mode (400 ms)	Integral resistor high speed mode (100 ms)	General amplifier	Comparator
E4H	–	0	0	0	DC voltmeter mode	BUF1 terminal	BUF3 terminal	OFF	OFF
	–	0	0	1	AC voltmeter mode			ON	OFF
	–	0	1	0	DC ammeter mode			OFF	OFF
	–	0	1	1	AC ammeter mode			ON	OFF
	–	1	0	0	Resistance measurement mode	Input integral: BUF1 terminal		OFF	OFF
	–	1	0	1	Continuity check mode	Reverse integral: BUF1 and BUF2 terminals parallel		OFF	ON
	–	1	1	0	–	BUF1 terminal	BUF3 terminal	OFF	OFF
	–	1	1	1	ADPT mode			OFF	OFF

* In the resistance measurement mode and continuity check mode, switching between input integral (BUF1 terminal) and reverse integral (BUF1 and BUF2 terminals parallel) is automatically done by the hardware.

Table 4.1.3 A/D converter measurement range list

Address	D3	D2 RNG2	D1 RNG1	D0 RNG0	Measurement function DC voltmeter	AC voltmeter	Resistance	Continuity check	Current
E5H	–	0	0	0	400 mV	400 mV	400 Ω	50 Ω judgment	Switching outside of IC
	–	0	0	1	4 V	4 V	4 kΩ	100 Ω judgment	
	–	0	1	0	40 V	40 V	40 kΩ	500 Ω judgment	
	–	0	1	1	400 V	400 V	400 kΩ	1 kΩ judgment	
	–	1	0	0	1000 V	750 V	4 MΩ	↑	
	–	1	0	1	↑	↑	40 MΩ	↑	
	–	1	1	0	↑	↑	↑	↑	
	–	1	1	1	↑	↑	↑	↑	

* In the current measurement mode, the E0C62M2 performs an A/D conversion using a voltage value (within ±437 mV) input from the IIL terminal or IIH terminal. Consequently, it is not necessary to switch the range.

4.2 Resetting Watchdog Timer

4.2.1 Configuration of watchdog timer

The E0C62M2 incorporates a watchdog timer as the source oscillator for OSC1 (clock timer 1 Hz signal). The watchdog timer must be reset cyclically by the software. If reset is not executed in at least 3 seconds, the initial reset signal is output automatically for the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

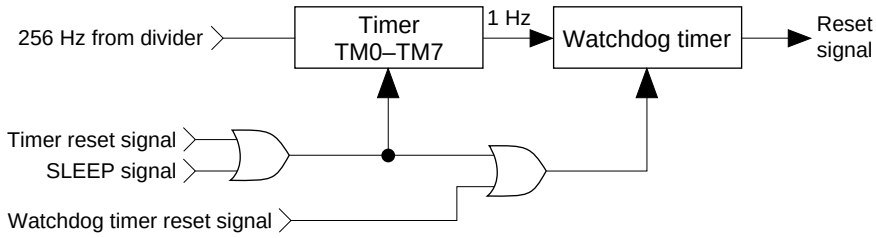


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer, configured of a two-bit binary counter, generates the initial reset signal internally by overflow of the counter.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer can also be reset by the resetting of the clock timer.
The watchdog timer operates in the HALT mode. If the watchdog timer is not reset within 3 or 4 seconds including the HALT status, the IC reactivates from initial reset status.
When the E0C62M2 enters SLEEP status by the SLP instruction, the watchdog timer and the clock timer are reset. Therefore, when SLEEP status is released, the watchdog timer and the clock timer operate the same as that after releasing an initial reset.

4.2.2 Control of watchdog timer

Table 4.2.2.1 lists the watchdog timer's control bits and their address.

Table 4.2.2.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
D4H	0	0	WDRST	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		W		WDRST *5	– *2	Reset	–	Watchdog timer reset
					TMRST *5	– *2	Reset	–	Clock timer and watchdog timer reset

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

WDRST: Watchdog timer reset (D4H•D1)
This is the bit for resetting the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset, and the operation restarts immediately after this. When "0" is written to WDRST, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

TMRST: Clock timer reset (D4H•D0)
This is the bit for resetting the clock timer and the watchdog timer.

When "1" is written:	Clock timer and watchdog timer are reset
When "0" is written:	No operation
Reading:	Always "0"

When "1" is written to TMRST, the clock timer and the watchdog timer are reset, and the operation restarts immediately after this. When "0" is written to TMRST, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.3 Programming note

The watchdog timer must be reset within 3-second cycles.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The E0C62M2 has a oscillation circuit (OSC1). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits.
Figure 4.3.1.1 is the block diagram of this oscillation system.

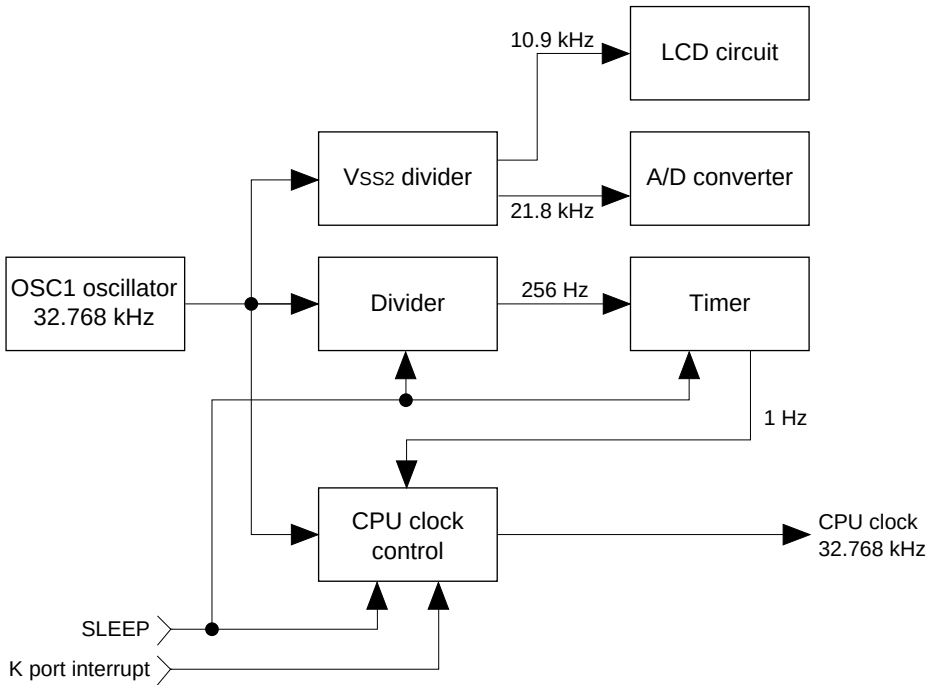


Fig. 4.3.1.1 Oscillation system

4.3.2 Crystal oscillation circuit

The E0C62M2 has a built-in crystal oscillation circuit. The OSC1 oscillation circuit generates the operating clock for the CPU and peripheral circuitry by connecting the crystal oscillator (Typ. 32.768 kHz) as an external element.
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

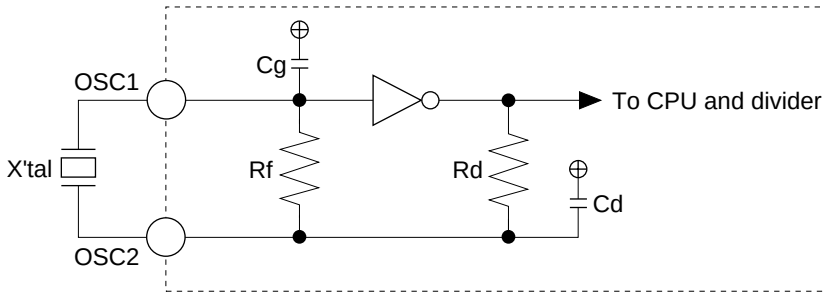


Fig. 4.3.2.1 OSC1 oscillation circuit

As Figure 4.3.2.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) between terminals OSC1 and OSC2.

The OSC1 oscillation circuit starts to operate immediately after turning the power ON, so programming is not necessary to control the circuit. However, be aware that the system clock is not supplied to the CPU until the 1 Hz signal from the timer goes high after initial resetting.

In the E0C62M2, the OSC1 oscillation circuit does not stop even when the CPU enters SLEEP status. However, SLEEP stops supplying the clock to the peripheral circuits (timer and watchdog timer).

4.3.3 Clock frequency and instruction execution time

Table 4.3.3.1 shows the instruction execution time according to the system clock from the OSC1 oscillation circuit.

Table 4.3.3.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	5-clock instruction	7-clock instruction	12-clock instruction
OSC1: 32.768 kHz	152.6	213.6	366.2

4.4 Input Ports (K00–K03, K10–K13)

4.4.1 Configuration of input ports

The E0C62M2 has eight bits general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13) provides internal pull down resistor. Pull down resistor can be selected for each bit with the mask option.
Further, a Schmitt buffer is provided on each input line of all input terminals (K00–K03, K10–K13).
Figure 4.4.1.1 shows the configuration of input port.

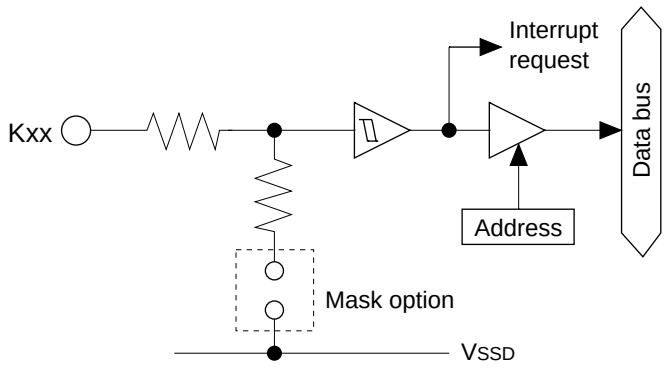


Fig. 4.4.1.1 Configuration of input port

Selection of "With pull down resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

Further, all the input port terminals (K00–K03, K10–K13) are used as the interrupt port for releasing the SLEEP mode. See Section 4.15, "Interrupt and HALT/SLEEP" for details.

4.4.2 Interrupt function

All eight bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software.
Figure 4.4.2.1 shows the configuration of input interrupt circuit.

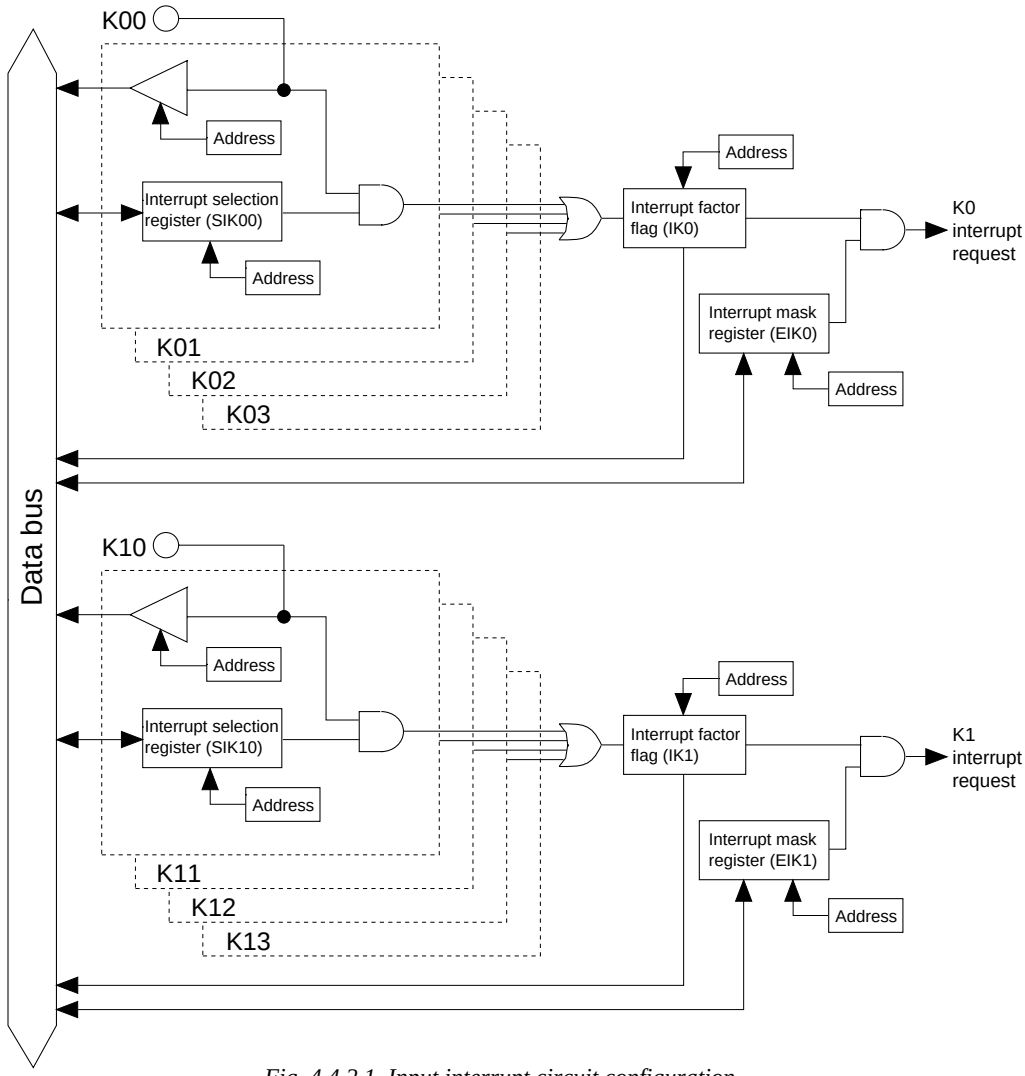


Fig. 4.4.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) is individually set for the input ports (K00–K03, K10–K13) and can specify the terminal for generating interrupt.
The interrupt selection registers (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.
The input interrupt is generated at the rising edge of the input.
The K00–K03 and K10–K13 interrupts are separated as two interrupt factors. Therefore, two interrupt factor flags (IK0, IK1) and two interrupt mask registers (EIK0, EIK1) are provided. (IK0 and EIK0 correspond to K00–K10. IK1 and EIK1 correspond to K10–K13.)
When the interrupt is generated, the interrupt factor flag (IK0, IK1) is set to "1".
Each interrupt request to the CPU by the interrupt factors can be masked using the interrupt mask registers (EIK0, EIK1).

The K00–K03 and K10–K13 input interrupts are used to release the SLEEP mode.

4.4.3 Mask option

Internal pull down resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13) with the input port mask option.
When "Gate direct" (without pull down resistor) is selected, take care that the floating status does not occur for the input. Select "With pull down resistor" for input ports that are not being used.

4.4.4 Control of input ports

Table 4.4.4.1 lists the input ports control bits and their addresses.

Table 4.4.4.1 Input port control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C0H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	Interrupt selection register (K03)
					SIK02	0	Enable	Disable	Interrupt selection register (K02)
					SIK01	0	Enable	Disable	Interrupt selection register (K01)
	R/W				SIK00	0	Enable	Disable	Interrupt selection register (K00)
C1H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
					K01	– *2	High	Low	
	R				K00	– *2	High	Low	
C2H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	Interrupt selection register (K13)
					SIK12	0	Enable	Disable	Interrupt selection register (K12)
					SIK11	0	Enable	Disable	Interrupt selection register (K11)
	R/W				SIK10	0	Enable	Disable	Interrupt selection register (K10)
C3H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
					K11	– *2	High	Low	
	R				K10	– *2	High	Low	
F0H	EIK1	EIK0	EISIF	EIAD	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
					EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
	R/W				EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F2H	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F3H	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

K00–K03, K10–K13: Input port data (C1H, C3H)

Input data of the input port terminals can be read.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the eight bits of the input ports (K00–K03, K10–K13) goes high (V_{DD}), and "0" when the voltage goes low (V_{SSD}).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03, SIK10–SIK13: Interrupt selection register (C0H, C2H)

Selects the port to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection register (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.
At initial reset, these registers are set to "0".

EIK0, EIK1: Interrupt mask registers (F0H•D2, D3)
Masking the interrupt of the input port can be selected with these registers.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

With these registers, masking of the input interrupt can be selected for each of the two systems (K00–K03, K10–K13).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are set to "0".

IK0, IK1: Interrupt factor flags (F3H•D0, F2H•D0)
These flags indicate the occurrence of input interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
These flags are reset when the software reads them.
At initial reset, these flags are set to "0".

4.4.5 Programming notes

(1) When input ports are changed from high to low by pull down resistor, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull down resistance 300 kΩ

(2) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

(3) Write the interrupt mask register (EIK0, EIK1) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.5 Output Ports (R00–R03)

4.5.1 Configuration of output ports

The E0C62M2 has four bits general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and Pch open drain output.
Figure 4.5.1.1 shows the configuration of the output port.

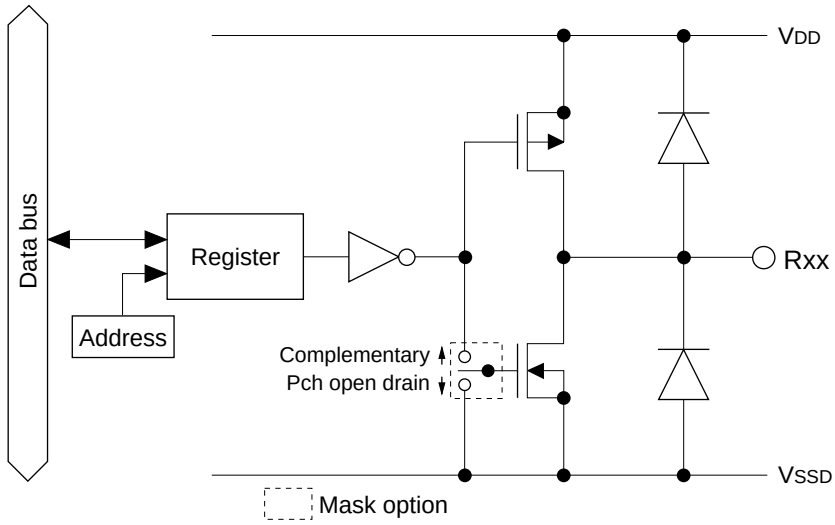


Fig. 4.5.1.1 Configuration of output port

4.5.2 Mask option

Output specifications of the output ports can be selected with the mask option.
Output specifications for the output ports (R00–R03) enable selection of either complementary output or Pch open drain output for each of the four bits.
However, even when Pch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

4.5.3 Control of output ports

Table 4.5.3.1 lists the output ports' control bits and their address.

Table 4.5.3.1 Control bits of output ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
C4H	R03	R02	R01	R00	R03	0	High	Low	Output port (R00–R03)
					R02	0	High	Low	
	R/W				R01	0	High	Low	
					R00	0	High	Low	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

R00–R03: Output port data (C4H)
Sets the output data for the output ports.

When "1" is written: High output
When "0" is written: Low output
Reading: Valid

The output port terminals output the data written in the corresponding registers (R00–R03) without changing it. When "1" is written in the register, the output port terminal goes high (VDD), and when "0" is written, the output port terminal goes low (VSSD).
At initial reset, these registers are set to "0".

4.6 Buzzer Output Ports (BZ, $\overline{BZ}$)

4.6.1 Configuration of buzzer output ports

The E0C62M2 has two special output ports: a buzzer output (BZ terminal) and a buzzer inverted output ($\overline{BZ}$ terminal). Output specification of the buzzer output ports is a complementary output.
Figure 4.6.1.1 shows the configuration of the buzzer output port.

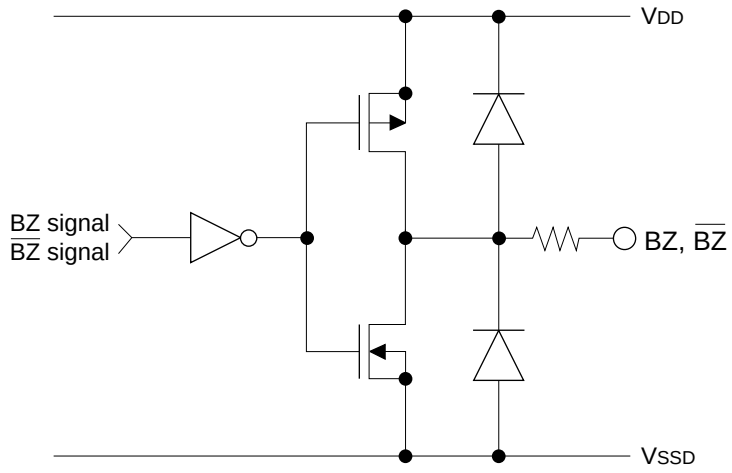


Fig. 4.6.1.1 Configuration of buzzer output port

4.6.2 Buzzer output

BZ and $\overline{BZ}$ are the buzzer signal outputs for driving the piezo-electric buzzer.
By setting the BZON register to "1", the BZ (buzzer signal output) terminal and the $\overline{BZ}$ (buzzer inverted signal output) terminal output the buzzer signal.
The buzzer signal frequency can be selected as 2 kHz or 4 kHz by setting the BZFQ register.
The following four output modes are set in the buzzer output function.

- Continuous buzzer signal output
- Intermittent buzzer signal output
- One-shot buzzer signal output
- Buzzer signal output during the continuity check mode

(1) Continuous buzzer signal output

By setting the BZFNC register to "0" and the BZON register to "1", the buzzer signal is continuously output from the BZ terminal and the $\overline{BZ}$ terminal.
Figure 4.6.2.1 shows the output waveform of a continuous buzzer signal.

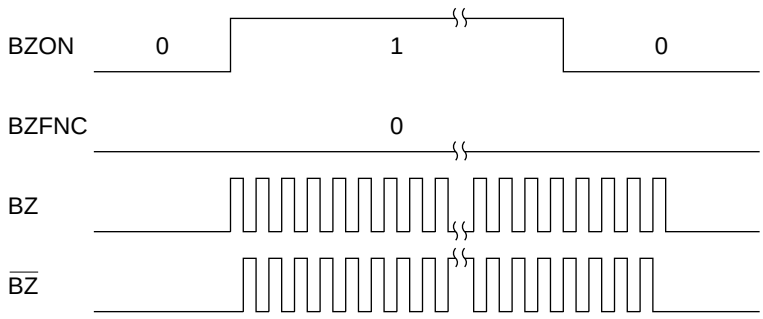


Fig. 4.6.2.1 Continuous buzzer signal output waveform

The buzzer signal output stops by writing "0" to the BZON register. However, it may take up to 31 msec for the buzzer signal output to actually stop depending on the status of the counter built into the buzzer signal output control circuit.

(2) Intermittent buzzer signal output

By setting the BZFNC register to "1" and the BZON register to "1", the buzzer signal is intermittently output from the BZ terminal and the $\overline{BZ}$ terminal.
In this mode, the buzzer signal goes ON and OFF in 8 Hz cycles.
The buzzer signal output stops by writing "0" to the BZON register. However, it may take up to 31 msec for the buzzer signal output to actually stop depending on the status of the counter built into the buzzer signal output control circuit.
Figure 4.6.2.2 shows the output waveform of an intermittent buzzer signal.

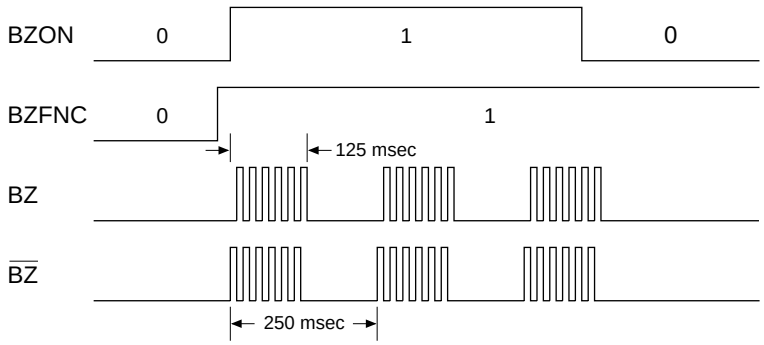


Fig. 4.6.2.2 Intermittent buzzer signal output waveform

(3) One-shot buzzer signal output

By writing "1" to the BSHOT register, a buzzer signal is output for approximately 31 msec immediately after writing.
Figure 4.6.2.3 shows the output waveform of one-shot buzzer signal.

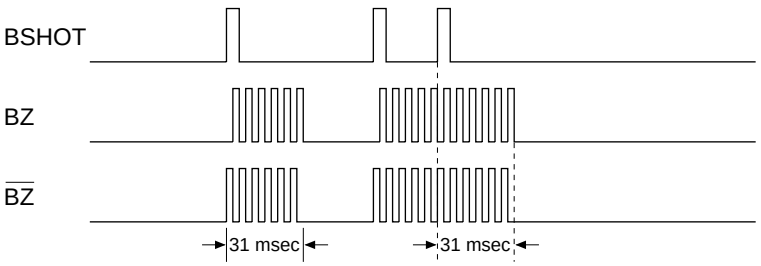


Fig. 4.6.2.3 One-shot buzzer signal output waveform

When "1" is written to the BSHOT register again while the previous one-shot buzzer signal is being output, the buzzer signal is output again for 31 msec from the time of rewriting "1".
This output is effective when the BZON register is set to "0".

(4) Buzzer signal output during the continuity check mode

If the measured resistance value is less than the judgment resistance setting value during measurement in the continuity check mode of the E0C62M2 measurement function, a buzzer signal is output. The continuity judgment and the buzzer signal output are automatically done by the hardware.
This auto buzzer signal output is done only in the continuity check mode. See Section 4.12, "Measurement Circuit and Measurement Procedure" for details of the continuity check mode.

4.6.3 Control of buzzer output

Table 4.6.3.1 lists the buzzer output control bits and their addresses.

Table 4.6.3.1 Control bits for buzzer output

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
D0H	0	0	BZFQ	R	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		R/W		BZFQ	0	2 kHz	4 kHz	Buzzer signal frequency selection
					R	0	1	0	1 bit general-purpose register
D1H	0	BSHOT	BZFNC	BZON	0 *5	– *2			Unused
					BSHOT*5	– *2	One-shot	–	One-shot buzzer signal (31 msec) output trigger
	R	W	R/W		BZFNC	0	Intermittent	Continuous	Continuous/intermittent output selection
					BZON	0	On	Off	Buzzer signal output control

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

BZFQ: Buzzer signal frequency selection register (D0H•D1)
Selects the frequency of the buzzer signal.

When "1" is written: 2 kHz
When "0" is written: 4 kHz
Reading: Valid

When "1" is written to this register, the frequency of the buzzer signal is set in 2 kHz, and in 4 kHz when "0" is written. Buzzer signal output (ON/OFF) is controlled using the BZON register.
At initial reset, this register is set to "0".

BSHOT: One-shot buzzer signal output trigger (D1H•D2)
Outputs a one-shot buzzer signal from the BZ and $\overline{BZ}$ terminals.

When "1" is written: Output
When "0" is written: Invalid
Reading: Always "0"

When "1" is written to this trigger bit, a buzzer signal is output for approximately 31 msec immediately after writing. When "1" is written again while the previous one-shot buzzer signal is being output, the buzzer signal is output again for 31 msec from the time of rewriting "1".
This output is effective when the BZON register is set to "0".

BZFNC: Continuous/intermittent output selection register (D1H•D1)
Selects a buzzer signal output mode.

When "1" is written: Continuous buzzer signal output
When "0" is written: Intermittent buzzer signal output
Reading: Valid

When "1" is written to this register, continuous buzzer signal output is selected as the output mode, and when "0" is written, intermittent buzzer signal output is selected.
Buzzer signal output (ON/OFF) is controlled using the BZON register.
In the intermittent buzzer signal output mode, the buzzer signal goes ON and OFF in 125 msec cycles while the BZON register is set to ON.
At initial reset, this register is set to "0".

BZON: Buzzer signal output control (D1H•D0)
Controls turning buzzer signal output ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to this register, the buzzer signal is output in the output mode set by the BZFNC register. After that, when "0" is written, the buzzer signal output stops.
At initial reset, this register is set to "0".

4.7 I/O Ports (P00–P03)

4.7.1 Configuration of I/O ports

The E0C62M2 has 4 bits general-purpose I/O ports. Figure 4.7.1.1 shows the configuration of the I/O port. The four bits of the I/O ports P00–P03 can be set to either input mode or output mode. Modes can be set by writing data to the I/O control register.
Moreover, pull down resistor which is turned ON during input mode can be controlled through the software.

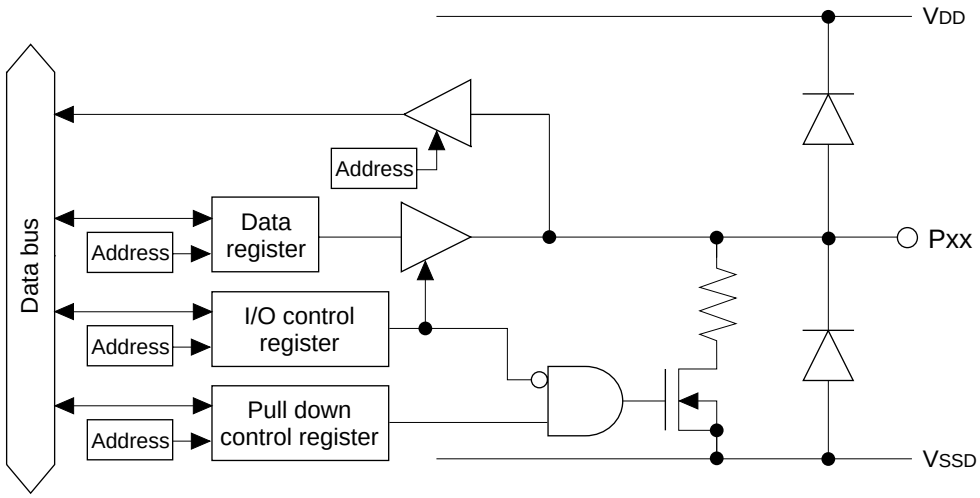


Fig. 4.7.1.1 Configuration of I/O port

The I/O ports P00–P03 are common used with the input/output ports of the serial interface, and function of these ports can be selected through the software.
See Section 4.10, "Serial Interface", for details of the serial interface.

4.7.2 I/O control registers and input/output mode

Input or output mode can be set for the four bits of I/O ports P00–P03 by writing data into the corresponding I/O control registers IOC00–IOC03.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull down explained in the following section has been set by software, the input line is pulled down only during this input mode.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SSD}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O port enters the input mode.

4.7.3 Pull down during input mode

A pull down resistor that operates during the input mode is built into the I/O ports of the E0C62M2. Software can set the use or non-use of this pull down. The pull down resistor becomes effective by writing "1" into the pull down control registers PUL00–PUL03 that correspond to each of P00–P03, and the input line is pulled down during the input mode. When "0" has been written, no pull down is done.
At initial reset, the pull down control registers are set to "1".

4.7.4 Mask option

Output specifications during the output mode (IOC = "1") can be selected with the mask option.
Output specifications for the I/O ports (P00–P03) enable selection of either complementary output or Pch open drain output for each of the 4 bits.
However, even when Pch open drain output is selected, voltage exceeding source voltage must not be applied to the output port.

4.7.5 Control of I/O ports

Table 4.7.5.1 lists the I/O ports' control bits and their addresses.

Table 4.7.5.1 Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
C8H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	I/O control register (P00–P03) (ESIF = 0)
	R/W				IOC02	0	Output	Input	
					IOC01	0	Output	Input	
					IOC00	0	Output	Input	
	When the serial I/F is used (ESIF = 1):				IOC03	0	Output	Input	Master mode: P03 I/O control register
	P00 = SIN (in), P01 = SOUT (out),				IOC03	0	1	0	Slave mode: General-purpose register
	P02 = SCLK (master: out, slave: in),				IOC02	0	1	0	General-purpose register
	P03 = SRDY (slave: out),				IOC01	0	1	0	
	P03 = I/O port (master: in/out)				IOC00	0	1	0	
C9H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Pull down control register (P00–P03) (ESIF = 0)
	R/W				PUL02	1	On	Off	
					PUL01	1	On	Off	
					PUL00	1	On	Off	
	When the serial I/F is used (ESIF = 1):				PUL03	1	On	Off	Master mode: P03 pull down control register
	P00 = SIN (in), P01 = SOUT (out),				PUL03	1	1	0	Slave mode: General-purpose register
	P02 = SCLK (master: out, slave: in),				PUL02	1	1	0	Master mode: General-purpose register
	P03 = SRDY (slave: out),				PUL02	1	On	Off	Slave mode: SCKL pull down control register
	P03 = I/O port (master: in/out)				PUL01	1	1	0	General-purpose register
					PUL00	1	On	Off	SIN pull down control register
CAH	P03	P02	P01	P00	P03	– *2	High	Low	I/O port (P00–P03) (ESIF = 0)
	R/W				P02	– *2	High	Low	
					P01	– *2	High	Low	
					P00	– *2	High	Low	
	When the serial I/F is used (ESIF = 1):				P03	– *2	High	Low	Master mode: I/O port P03
	P00 = SIN (in), P01 = SOUT (out),				P03	– *2	1	0	Slave mode: General-purpose register
	P02 = SCLK (master: out, slave: in),				P02	– *2	1	0	General-purpose register
	P03 = SRDY (slave: out),				P01	– *2	1	0	
	P03 = I/O port (master: in/out)				P00	– *2	1	0	

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

P00–P03: I/O port data (CAH)

I/O port data can be read and output data can be set through these ports.

- ***When writing data***

  When "1" is written: High level
  When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the level goes low (V_{SSD}).
Port data can be written also in the input mode.

• ***When reading data***

When "1" is read: High level
When "0" is read: Low level

When the I/O port is in the input mode, the voltage level being input to the port terminal can be read out. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SSD}) the data is "0".
When the I/O port is in the output mode, the P00–P03 register value can be read.
When PUL register is set to "1", the built-in pull down resistor goes ON during input mode, so that the I/O port terminal is pulled down.

When the serial input/output function is selected for P00–P03 ports, the registers P00–P03 in the slave mode and the registers P00–P02 in the master mode can be used as a general register having both read and write functions, and data of these registers exert no affect on input/output signal. In the master mode, since P03 is not used for the serial interface and can be used as an I/O port, the P03 register becomes the I/O port data register.

IOC00–IOC03: I/O control registers (C8H)

The input and output modes of the I/O ports can be set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in one bit unit. IOC00, IOC01, IOC02 and IOC03 set the mode for P00, P01, P02 and P03, respectively.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are set to "0", so the I/O ports are in the input mode.

When the serial input/output function is selected for P00–P03 ports, the registers IOC00–IOC03 in the slave mode and the registers IOC00–IOC02 in the master mode can be used as a general register having both read and write functions, and data of this registers exerts no affect on input/output control. In the master mode, since P03 is not used for the serial interface and can be used as an I/O port, the IOC03 register becomes the I/O control register.

PUL00–PUL03: Pull down control registers (C9H)

The pull down during the input mode can be set with these registers.

When "1" is written: Pull down ON
When "0" is written: Pull down OFF
Reading: Valid

The built-in pull down resistor which is turned ON during input mode is set to enable in units of four bits. PUL00, PUL01, PUL02 and PUL03 set the pull down for P00, P01, P02 and P03, respectively.
By writing "1" to the pull down control register, the corresponding I/O ports are pulled down (during input mode), while writing "0" turns the pull down function OFF.
At initial reset, these registers are set to "1", so the pull down function is set to ON.

When the serial input/output function is selected for P00–P03 ports, the PUL01 register, the PUL02 register in the master mode and the PUL03 register in the slave mode can be used as general registers having both read and write functions, and data of this registers exerts no affect on pull down control. In the master mode, since P03 is not used for the serial interface and can be used as an I/O port, the PUL03 register becomes the pull down control register.

4.7.6 Programming note

When in the input mode, I/O ports are changed from high to low by pull down resistor, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 10 pF + parasitic□capacitance ? pF
R: pull down resistance 300 kΩ

4.8 LCD Driver (COM0–COM3, SEG0–SEG15)

4.8.1 Configuration of LCD driver

The E0C62M2 has four common terminals (COM0–COM3) and 16 segment terminals (SEG0–SEG15), so that it can drive an LCD with a maximum of 64 (16 × 4) segments.
The power for driving the LCD is generated by the E0C62M2 internal circuit so that there is no need to apply power especially from outside.
The driving method is 1/4 duty dynamic drive depending on the four types of potential, V_{DD}, V_{L1}, V_{L2} and V_{L3}. In addition to the 1/4 duty, 1/3 drive duty can be selected through the software. The frame frequency is 42.7 Hz for 1/4 duty, and 56.9 Hz for 1/3 duty (f_{OSC1} = 32.768 kHz).
LCD display ON/OFF can be controlled by the software.
Figures 4.8.1.1 and 4.8.1.2 show the drive waveform for 1/4 duty and 1/3 duty.

Note: "f_{OSC1}" indicates the oscillation frequency of the OSC1 oscillation circuit.

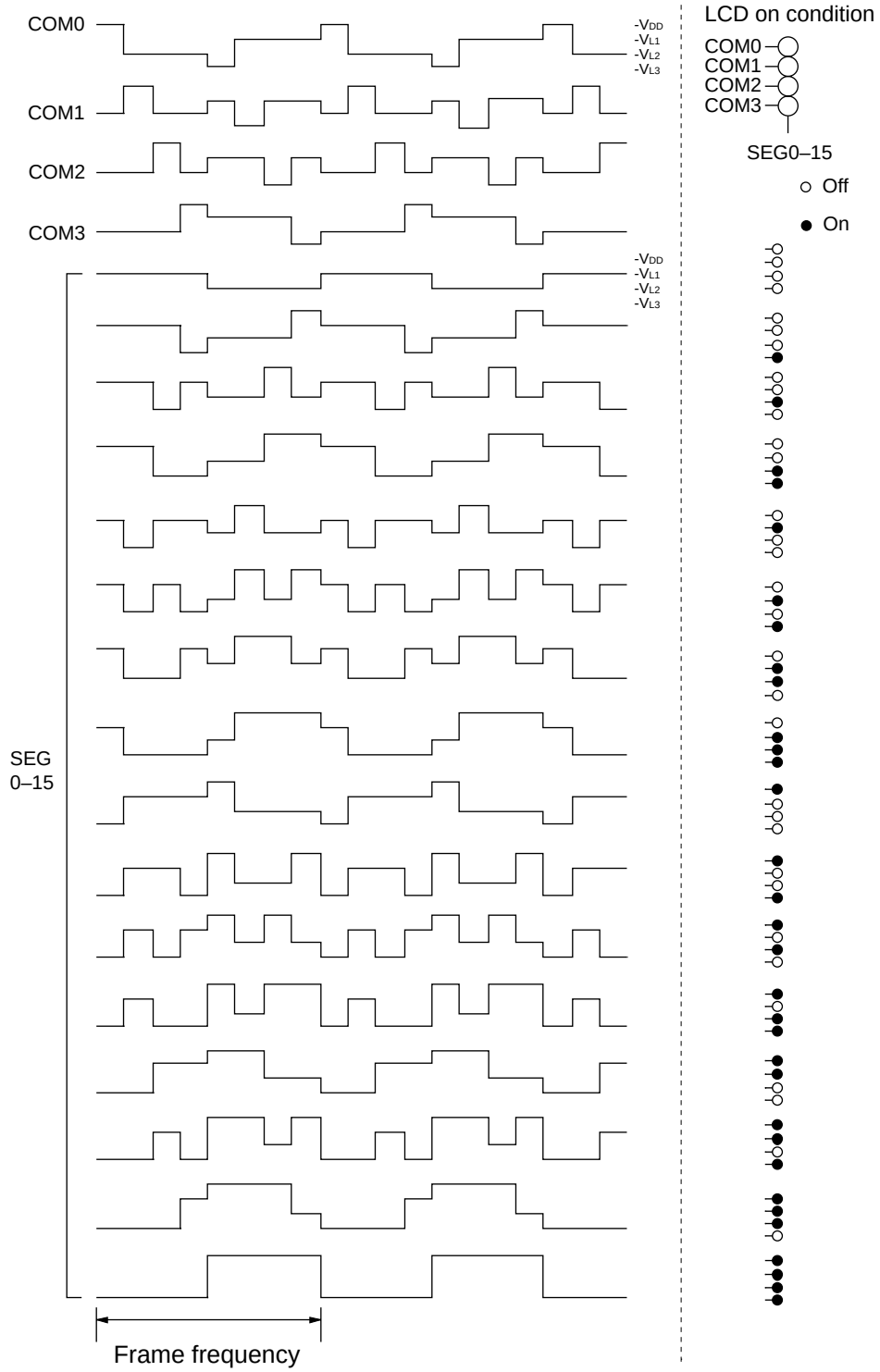


Fig. 4.8.1.1 Drive waveform for 1/4 duty

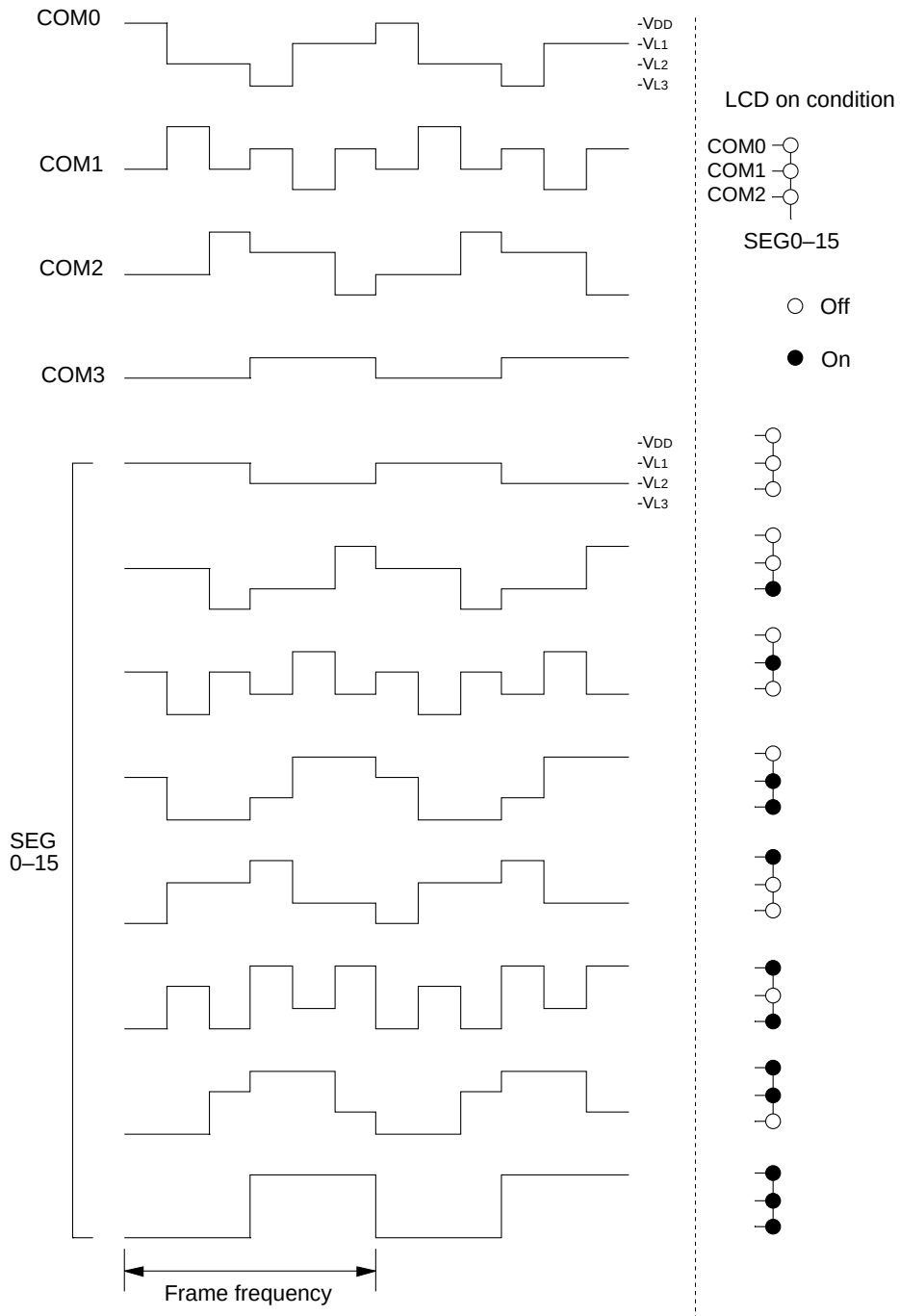


Fig. 4.8.1.2 Drive waveform for 1/3 duty

4.8.2 LCD display control and duty switching

(1) LCD drive power

The E0C62M2 has a built-in LCD power generator. The LCD power generator operates with the boosted voltage VSS2 (VDD standard) and generates the LCD voltage (VL1, VL2, VL3). Therefore, turn the VSS2 booster ON to generate boosted voltage VSS2 before displaying LCD.
See Section 4.13, "VSS2 Booster", for details of the VSS2 booster.
Figure 4.8.2.1 shows the configuration of the LCD drive power circuit.

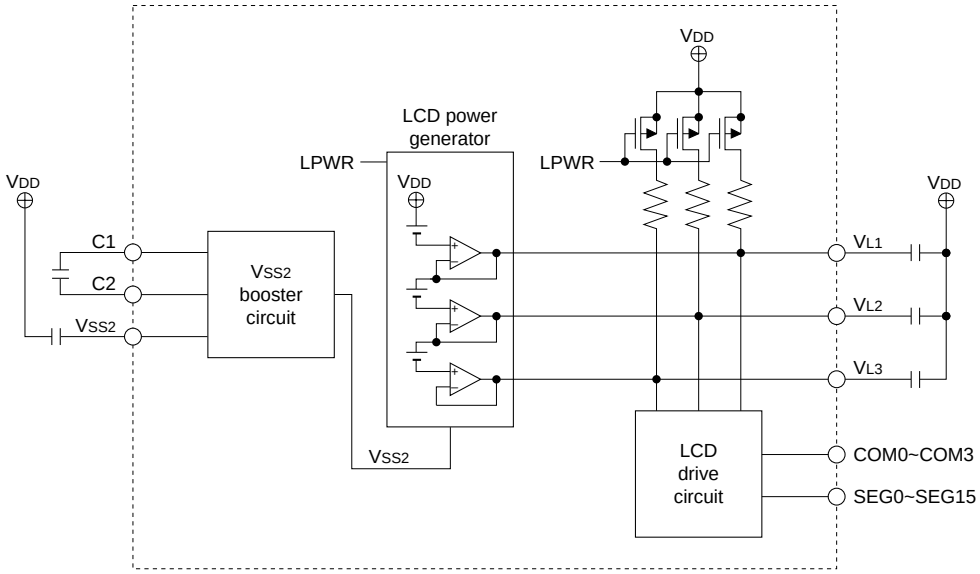


Fig. 4.8.2.1 Configuration of LCD drive power circuit

(2) Control of LCD driver

In the E0C62M2, turning ON/OFF of the LCD display can be controlled using the LPWR register. At initial reset, LPWR is set to "0", and the LCD display is set to the OFF status. In this time, the VL1, VL2, VL3, COM and SEG (*) terminals goes to VDD level.
To set the LCD display ON, write "1" to the LPWR register.

* Except for the SEG terminals that have been set to DC output by the mask option.

(3) Switching of drive duty

By settings of LDTY register, the LCD drive duty can be selected either 1/4 or 1/3 duty. Table 4.8.2.1 shows the LCD drive duty setting.

Table 4.8.2.1 LCD drive duty setting

LDTY	Duty	Terminals used in common	Maximum number of segments	Frame frequency *
0	1/4	COM0–COM3	64 (16 × 4)	fOSC1/768 (42.7 Hz)
1	1/3	COM0–COM2	48 (16 × 3)	fOSC1/576 (56.9 Hz)

* In case of fOSC1 = 32.768 kHz

Basically the LCD drive duty should be selected according to the LCD panel to be used. Select 1/3 duty if the segment number is 48 segments or less or select 1/4 duty if it is 49 segments or more.

(4) LCD display all OFF

In the E0C62M2, switching from normal display to display all OFF can be controlled using the LOFF register. By writing "1" to the LOFF register, all the LCD display can be turned OFF unless written to the segment memory. It returns to the normal display when "0" is written to the LOFF register. This operation does not affect the contents of the display memory.

(5) LCD driver in SLEEP status

When the E0C62M2 enters SLEEP status, it resets the LCD driver control registers (on the address E1H) to the initial status. However, it does not change the data in the display memory.

4.8.3 Mask option (segment allocation)

(1) Segment allocation

The LCD driver has a segment decoder built-in, and the data bit of the optional address in the display memory area (A0H–AFH) can be allocated to the optional segment. This makes design easy by increasing the degree of freedom with which the liquid crystal panel can be designed.
The allocated segment displays when the bit for the display memory is set to "1", and goes out when bit is set to "0".

Figure 4.8.3.1 shows an example of the relationship between the LCD segments (on the panel) and the display memory for the case of 1/3 duty.

Address	Data			
	D3	D2	D1	D0
AAH	d	c	b	a
ABH	p	g	f	e
ACH	d'	c'	b'	a'
ADH	p'	g'	f'	e'

Display memory allocation

	Common 0	Common 1	Common 2
SEG10	AA, D0 (a)	AB, D1 (f)	AB, D0 (e)
SEG11	AA, D1 (b)	AB, D2 (g)	AA, D3 (d)
SEG12	AD, D1 (f')	AA, D2 (c)	AB, D3 (p)

Pin address allocation

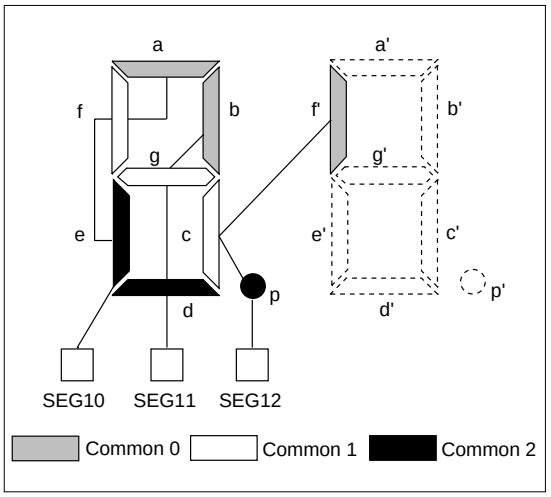


Fig. 4.8.3.1 Segment allocation

(2) Output specification

① The segment terminals (SEG0–SEG15) are selected with the mask option in pairs for either segment signal output or DC output (V_{DD} and V_{SSD} binary output).
When DC output is selected, the data corresponding to COM0 of each segment terminal is output.

② When DC output is selected, either complementary output or Pch open drain output can be selected for each terminal with the mask option.

Note: The terminal pairs are the combination of SEG2 × n and SEG2 × n + 1 (where n is an integer from 0 to 7).

4.8.4 Control of LCD driver

Table 4.8.4.1 shows the LCD driver's control bits and their address. Figure 4.8.4.1 shows the display memory map.

Table 4.8.4.1 LCD driver control bits

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
E1H	LOFF	0	LDTY	LPWR	LOFF	0	All off	Normal	LCD display all off / normal switch
					0 *5	– *2			Unused
	R/W	R	R/W		LDTY	0	1/3	1/4	LCD drive duty selection
					LPWR	0	On	Off	LCD driver On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	A	Display memory (16 words × 4 bits)															

Fig. 4.8.4.1 Display memory map

LPWR: LCD driver ON/OFF (E1H•D0)

Turns the LCD driver ON and OFF.

When "1" is written: LCD driver ON
When "0" is written: LCD driver OFF
Reading: Valid

By writing "1" to LPWR, the LCD driver goes ON. The voltage (V_{L1}, V_{L2}, V_{L3}) that is needed to drive the LCD and the signals are generated and the LCD panel displays according to the display data set in the display memory.
When "0" is written to LPWR, the LCD driver goes OFF and the terminals V_{L1}, V_{L2}, V_{L3}, COM and SEG (except for SEG terminals that are set to DC output by mask option) go to V_{DD} level.
At initial reset and in SLEEP status, this register is set to "0".

LDTY: LCD drive duty selection (E1H•D1)

Sets the LCD drive duty as shown in Table 4.8.4.2.

Table 4.8.4.2 LCD drive duty setting

LDTY	Duty	Terminals used in common	Maximum number of segments	Frame frequency *
0	1/4	COM0–COM3	64 (16 × 4)	f_{OSC1}/768 (42.7 Hz)
1	1/3	COM0–COM2	48 (16 × 3)	f_{OSC1}/576 (56.9 Hz)

* In case of f_{OSC1} = 32.768 kHz

The LDTY register can be read.
At initial reset and in SLEEP status, this register is set to "0".

Display memory (A0H–AFH)

The LCD segments are lit or turned off depending on this data.

When "1" is written: Lit
When "0" is written: Not lit
Reading: Invalid

By writing data into the display memory allocated to the LCD segment (on the panel), the segment can be lit or put out.
At initial reset, the contents of the display memory for COM0 is set to "0", and COM1–COM3 are undefined. Accordingly, when DC output is selected, the output level at initial reset is a low (V_{SSD}) level.

LOFF: LCD display all OFF (E1H•D3)

Turns LCD display all OFF.

When "1" is written:	LCD display all OFF
When "0" is written:	Normal display (according to the Display memory)
Reading:	Valid

When "1" is written to LOFF, all the LCD display goes OFF, and it returns to the normal display according to the display memory when "0" is written.
This operation does not affect the contents of the display memory.
At initial reset and in SLEEP status, this register is set to "0".

4.8.5 Programming notes

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) The power source for the LCD power generator (V_{L1}, V_{L2} and V_{L3} generation circuit) and the operating clock for the LCD drive timing generator are supplied from the V_{SS2} booster. Therefore, be sure to turn the V_{SS2} booster ON by setting the VSS2 register to "1" before turning the LCD driver ON (LPWR = "1").

(4) The control registers (LOFF, LDTY, LPWR) for the LCD driver are automatically set to the initial status when the CPU enters SLEEP status using the SLP instruction. Therefore, after returning from SLEEP status, set the registers' value again.
In SLEEP status, the V_{SS2} booster turns OFF.

4.9 Clock Timer

4.9.1 Configuration of clock timer

The E0C62M2 has a built-in clock timer as the source oscillator for OSC1 (crystal oscillator). The clock timer is configured of a 8-bit binary counter that serves as the input clock, a 256 Hz signal output by the OSC1 oscillation circuit. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.9.1.1 is the block diagram for the clock timer.

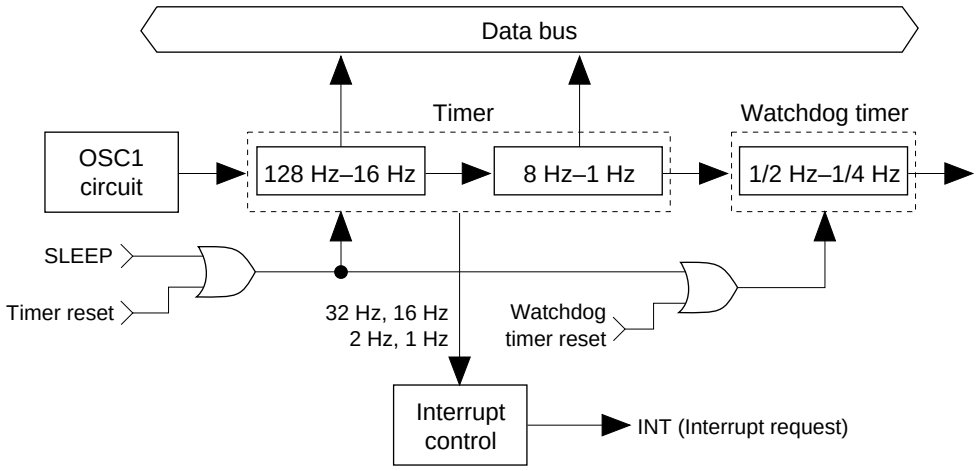


Fig. 4.9.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

4.9.2 Data reading and hold function

The 8 bits timer data are allocated to the addresses D5H and D6H.

D5H	D0: TM0 (128 Hz)	D1: TM1 (64 Hz)	D2: TM2 (32 Hz)	D3: TM3 (16 Hz)
D6H	D0: TM4 (8 Hz)	D1: TM5 (4 Hz)	D2: TM6 (2 Hz)	D3: TM7 (1 Hz)

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the E0C62M2 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

Note: When the high-order data has previously been read, since the low-order data is not held, you should be sure to first read from the low-order data.

4.9.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 16 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.9.3.1 is the timing chart of the clock timer.

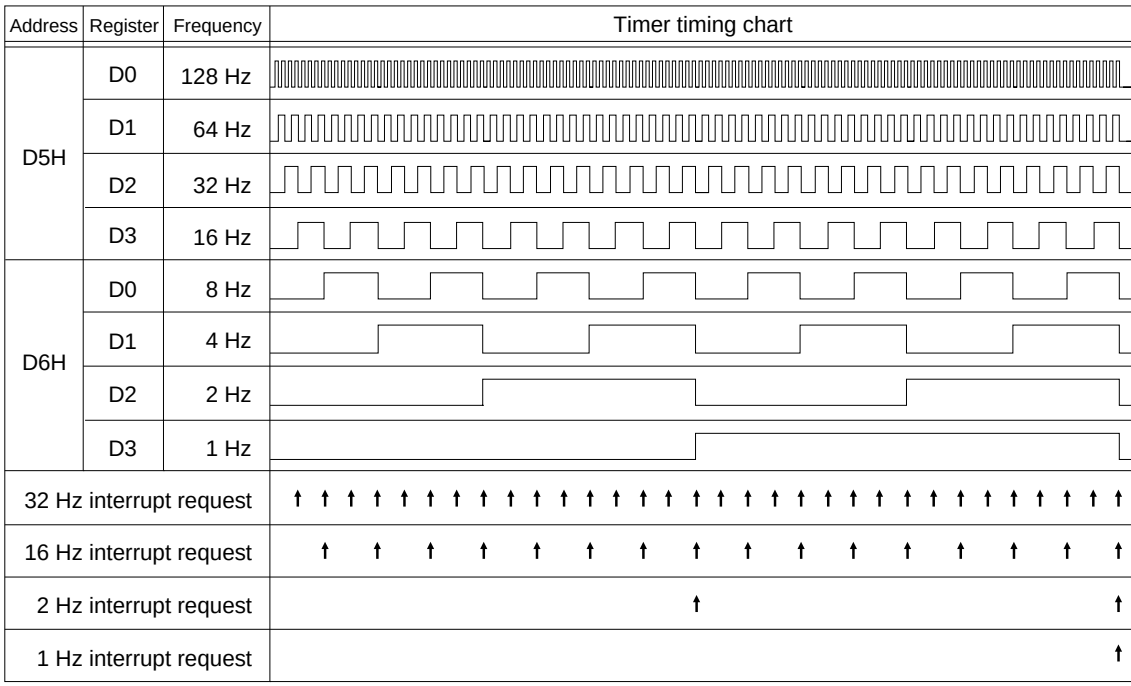


Fig. 4.9.3.1 Timing chart of clock timer

As shown in Figure 4.9.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 16 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT16, IT2, IT1) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT16, EIT2, EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

Note:
- *Reading of interrupt factor flags is available at EI, but be careful in the following cases. If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.*
- *Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.*

4.9.4 Control of clock timer

Table 4.9.4.1 shows the clock timer control bits and their addresses.

Table 4.9.4.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
D4H	0	0	WDRST	TMRST	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R		W		WDRST *5	– *2	Reset	–	Watchdog timer reset
					TMRST *5	– *2	Reset	–	Clock timer and watchdog timer reset
D5H	TM3	TM2	TM1	TM0	TM3	– *3			Clock timer data (16 Hz)
					TM2	– *3			Clock timer data (32 Hz)
	R				TM1	– *3			Clock timer data (64 Hz)
					TM0	– *3			Clock timer data (128 Hz)
D6H	TM7	TM6	TM5	TM4	TM7	– *3			Clock timer data (1 Hz)
					TM6	– *3			Clock timer data (2 Hz)
	R				TM5	– *3			Clock timer data (4 Hz)
					TM4	– *3			Clock timer data (8 Hz)
F1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT16	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F5H	IT1	IT2	IT16	IT32	IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R				IT16 *4	0	Yes	No	Interrupt factor flag (Clock timer 16 Hz)
					IT32 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

TM0–TM7: Timer data (D5H, D6H)

The 128 Hz–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.
By reading the low-order data (D5H), the high-order data (D6H) is held while the shorter of the two indicated below.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (varies due to the timing of the reading)

At initial reset, the timer data is initialized to "00H".

EIT32, EIT16, EIT2, EIT1: Interrupt mask register (F1H)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT32, EIT16, EIT2, EIT1) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 16 Hz, 2 Hz, 1 Hz).
Writing to the interrupt mask registers can be done only in the DI status (interrupt flag = "0").
At initial reset, these registers are all set to "0".

IT32, IT16, IT2, IT1: Interrupt factor flag (F5H)
These flags indicate the status of the clock timer interrupt.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

The interrupt factor flags (IT32, IT16, IT2, IT1) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 16 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags can be reset through being read out by the software.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.
At initial reset, these flags are set to "0".

TMRST: Clock timer reset (D4H•D0)
This bit resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to TMRST. The clock timer starts immediately after this. No operation results when "0" is written to TMRST.
TMRST also resets the watchdog timer.
This bit is write-only, and so is always "0" at reading.

4.9.5 Programming notes

(1) Be sure to read data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(3) The clock timer is reset when the CPU enters SLEEP status by the SLP instruction.

(4) When the clock timer has been reset, the watchdog timer is also reset.

(5) Write the interrupt mask register (EIT) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(6) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.10 Serial Interface (SIN, SOUT, SCLK, SRDY)

4.10.1 Configuration of serial interface

The E0C62M2 has a synchronous clock type 8-bit serial interface built-in.
The configuration of the serial interface is shown in Figure 4.10.1.1.
The CPU, via the 8-bit shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of two types of master mode (internal clock mode: when the E0C62M2 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C62M2 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, SRDY signal which indicates whether or not the serial interface is available to transmit or receive can be output to the SRDY terminal.

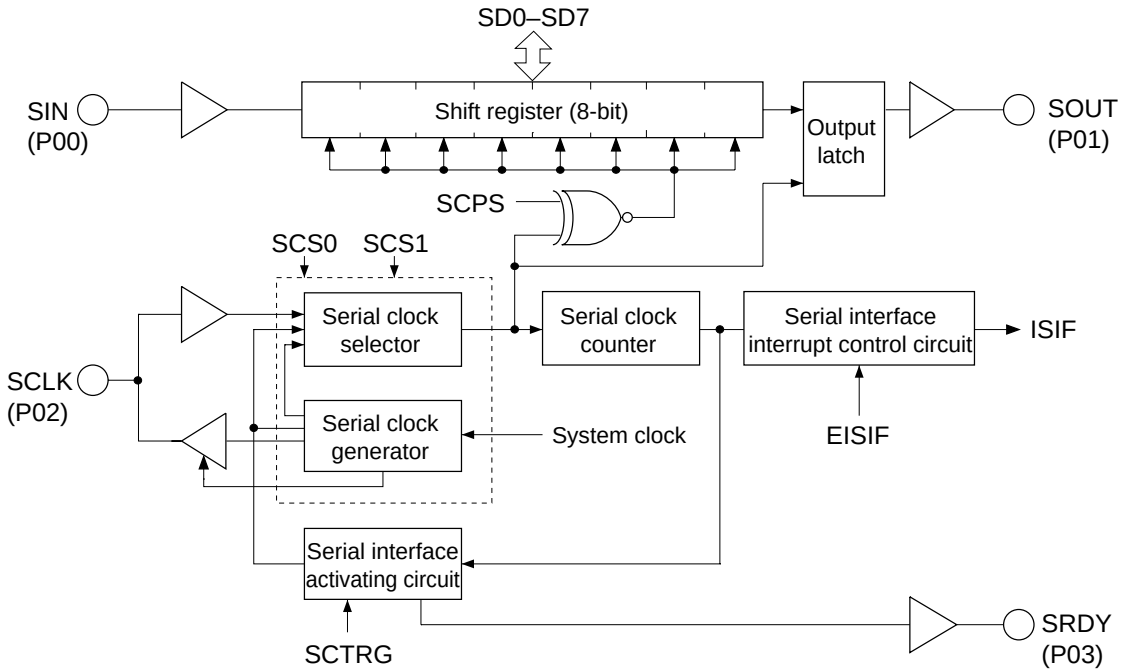


Fig. 4.10.1.1 Configuration of serial interface

The input/output ports of the serial interface are common used with the I/O ports P00–P03, and function of these ports can be selected through the software.
P00–P03 terminals and serial input/output correspondence are as follows:

Master mode	***Slave mode***
P00 = SIN (I)	P00 = SIN (I)
P01 = SOUT (O)	P01 = SOUT (O)
P02 = SCLK (O)	P02 = SCLK (I)
P03 = I/O port (I/O)	P03 = SRDY (O)

Note: At initial reset, P00–P03 are set to I/O ports.
When using the serial interface, switch the function (ESIF = "1") in the initial routine.

4.10.2 Master mode and slave mode of serial interface

The serial interface of the E0C62M2 has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the SCLK (P02) terminal and controls the external (slave side) serial device.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the SCLK (P02) terminal and uses it as the synchronous clock to the built-in shift register.
The master mode and slave mode are selected by writing data to registers SCS0 and SCS1.
When the master mode is selected, a synchronous clock may be selected from among two types as shown in Table 4.10.2.1.

Table 4.10.2.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK
0	1		CLK/2
0	0	Slave mode	External clock

CLK: CPU system clock (32.768 kHz)
CLK/2: CPU system clock/2

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8-bit serial data, is controlled as follows:

- At master mode, after output of 8 clocks from the SCLK (P02) terminal, clock output is automatically suspended and SCLK (P02) terminal is fixed at low level.
- At slave mode, after input of 8 clocks to the SCLK (P02) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.10.2.1.

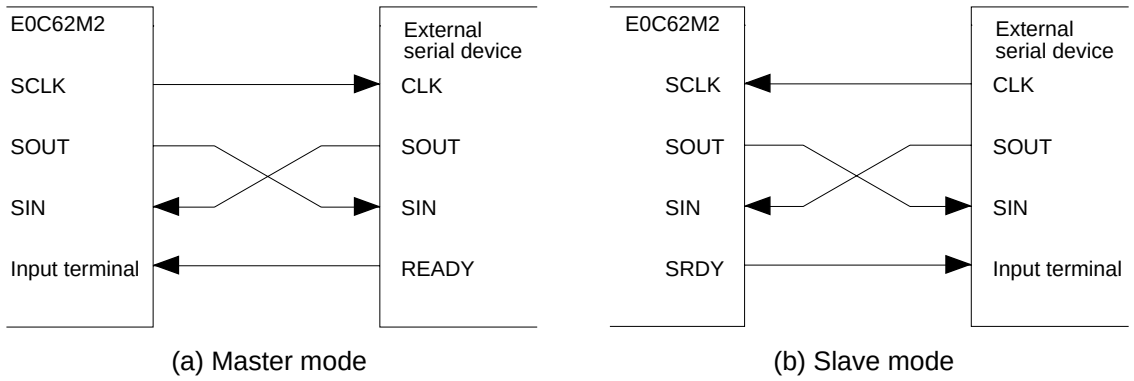


Fig. 4.10.2.1 Sample basic connection of serial input/output section

4.10.3 Data input/output and interrupt function

The serial interface of E0C62M2 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from SCLK (P02) terminal (master mode), or the synchronous clock input to SCLK (P02) terminal (slave mode).
The serial interface generates interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock SCLK; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure and interrupt

The E0C62M2 serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to 4-bit registers SD0–SD3 (CEH) and SD4–SD7 (CFH) individually and writing "1" to SCTRG bit (CCH•D1), it synchronizes with the synchronous clock and serial data is output at the SOUT (P01) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P02) terminal while in the slave mode, external clock which is input from the SCLK (P02) terminal. The serial output of the SOUT (P01) terminal changes with the rising edge of the clock that is input or output from the SCLK (P02) terminal.

When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (F4H•D0) is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF (F0H•D1). Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after output of the 8-bit data.

(2) Serial data input procedure and interrupt

The E0C62M2 serial interface is capable of inputting serial data as parallel data, in units of 8 bits.
The serial data is input from the SIN (P00) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the SCLK (P02) terminal while in the slave mode, external clock which is input from the SCLK (P02) terminal.
The serial data to the built-in shift register is read with the rising edge of the SCLK signal when the SCPS register is "1" and is read with the falling edge of the SCLK signal when the SCPS register is "0". Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8-bit data.

The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

E0C62M2 allows the input/output permutation of serial data to be selected by register SDP (CDH•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.10.3.1.

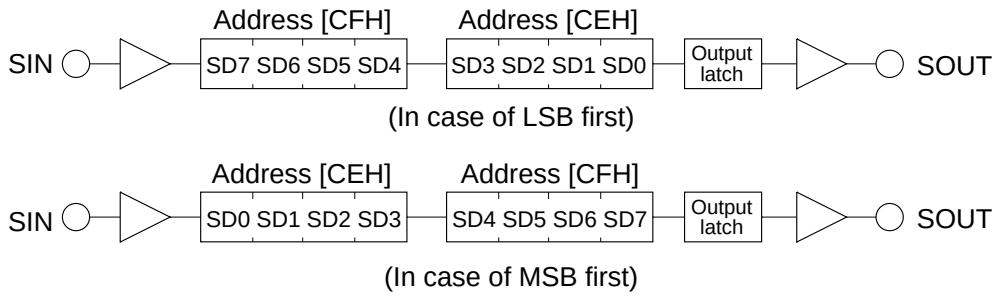


Fig. 4.10.3.1 Serial data input/output permutation

(4) SRDY signal

When the E0C62M2 serial interface is used in the slave mode (external clock mode), SRDY is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. SRDY signal is output from the SRDY (P03) terminal.
SRDY signal becomes "1" (high: V_{DD} level) when the E0C62M2 serial interface becomes available to transmit or receive data; normally, it is at "0" (low: V_{SSD} level).
SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRG and returns from "1" to "0" when "1" is input to the SCLK (P02) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when data is read from or written to SD4–SD7, the SRDY signal returns to "0".

(5) Timing chart

The E0C62M2 serial interface timing chart is shown in Figure 4.10.3.2.

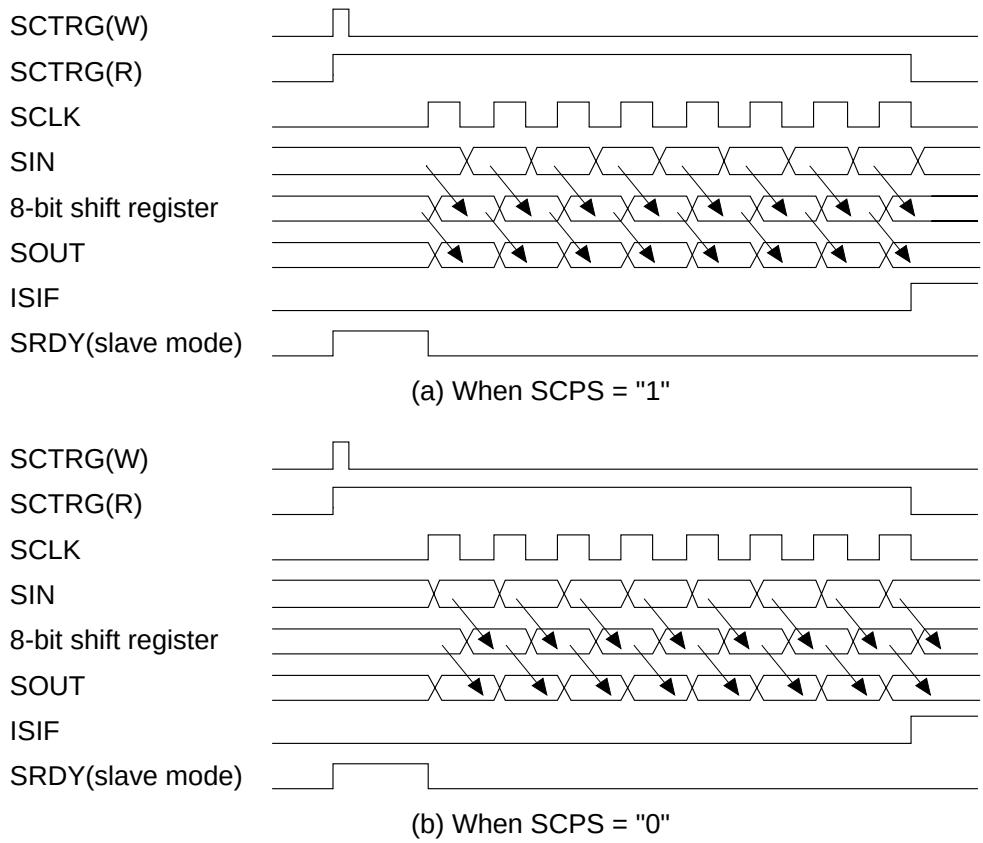


Fig. 4.10.3.2 Serial interface timing chart

4.10.4 Mask option

Since the input/output terminal of the serial interface is dual used with the I/O ports (P00–P03), the mask option that selects the output specification for the I/O port is also applied to the serial interface.

The output specification of the terminals SOUT, SCLK (during the master mode) and SRDY (during the slave mode) that are used as output in the input/output port of the serial interface is respectively selected by the mask options of P01, P02 and P03.
Either complementary output or P channel (Pch) open drain as output specification may be selected. However, even if Pch open drain has been selected, application on the terminal of voltage exceeding power source voltage is not permitted.
Select complementary output for the output specification of the SIN (P00) terminal.

4.10.5 Control of serial interface

Table 4.10.5.1 list the serial interface control bits and their addresses.

Table 4.10.5.1 Control bits of serial interface

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
CCH	0	0	SCTRG	ESIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
					SCTRG(W)	– *2	Trigger	–	Serial interface clock trigger (writing)
	R		R/W		SCTRG(R)	0	Run	Stop	Serial interface clock status (reading)
					ESIF	0	SIF port	I/O port	P0 port function selection
CDH	SDP	SCPS	SCS1	SCS0	SDP	0	LSB first	MSB first	Serial data input/output permutation
					SCPS	0	⌐	¬	Serial interface clock phase selection
	R/W				SCS1	0			Serial interface clock mode selection
					SCS0	0			0: Slave, 1: CLK/2, 2: CLK, 3: CLK
CEH	SD3	SD2	SD1	SD0	SD3	– *2			MSB
					SD2	– *2			Serial interface data (low-order 4 bits)
	R/W				SD1	– *2			
					SD0	– *2			LSB
CFH	SD7	SD6	SD5	SD4	SD7	– *2			MSB
					SD6	– *2			Serial interface data (high-order 4 bits)
	R/W				SD5	– *2			
					SD4	– *2			LSB
C9H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	Master mode: P03 pull down control register
					PUL03	1	1	0	Slave mode: General-purpose register
					PUL02	1	1	0	Master mode: General-purpose register
	R/W				PUL02	1	On	Off	Slave mode: SCKL pull down control register
					PUL01	1	1	0	General-purpose register
					PUL00	1	On	Off	SIN pull down control register
F0H	EIK1	EIK0	EISIF	EIAD	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
	R/W				EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F4H	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ISIF *4	0	Yes	No	Interrupt factor flag (Serial interface)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

ESIF: P0 port function selection (CCH•D0)

Sets P00–P03 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

P00, P01, P02 and P03 will function as SIN, SOUT, SCLK, SRDY, respectively.
In the slave mode, the P03 terminal functions as the SRDY output terminal, and in the master mode, it functions as the I/O port terminal.
At initial reset, this register is set to "0".

PUL00, PUL02: Pull down control register (C9H•D0, D2)

Sets the pull down of SIN terminal and SCLK terminal (in the slave mode).

When "1" is written: Pull down ON
When "0" is written: Pull down OFF
Reading: Valid

Sets the pull down resistor built into the SIN (P00) and SCLK (P02) ports to ON or OFF. SCLK pull down is effective during the slave mode.
At initial reset, these registers are set to "1".

SCS0, SCS1: Cock mode selection (CDH•D0, D1)

Selects the synchronous clock for the serial interface (SCLK).

Table 4.10.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK
0	1		CLK/2
0	0	Slave mode	External clock

CLK: CPU system clock (32.768 kHz)
CLK/2: CPU system clock/2

Synchronous clock (SCLK) is selected from among the above 3 types: 2 types of internal clock and external clock. At initial reset, external clock is selected.

SCPS: Shift clock phase selection (CDH•D2)

Selects the timing for reading in the serial data input from SIN (P00) terminal.

When "1" is written: Rising edge of SCLK
When "0" is written: Falling edge of SCLK
Reading: Valid

Selects whether the fetching for the serial input data to the registers (SD0–SD7) at the rising edge (at "1" writing) or falling edge (at "0" writing) of the SCLK signal.
The input data fetching timing may be selected but output timing for output data is fixed at SCLK rising edge.
When the internal clock is selected as the synchronous clock (SCLK), a hazard occurs in the synchronous clock (SCLK) when data is written to the SCPS register.
At initial reset, this register is set to "0".

SDP: Data input/output permutation selection (CDH•D3)

Selects the serial data input/output permutation.

When "1" is written: LSB first
When "0" is written: MSB first
Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first.
At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (CCH•D1)

This is a trigger to start input/output of synchronous clock (SCLK).

• ***When data is written***

When "1" is written: Trigger
When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock (SCLK) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.
Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

• ***When data is read***

When "1" is read: RUN status
When "0" is read: STOP status

When read out this bit, it indicates the status of serial interface clock.
After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.
When the synchronous clock input/output is completed, this latch is reset to "0".
At initial reset, this bit is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (CEH, CFH)
These registers are used for writing and reading serial data.

• ***When data is written***
When "1" is written: High level
When "0" is written: Low level

Writes serial data will be output to SOUT (P01) terminal. From the SOUT (P01) terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SSD}) level bit for bits set at "0".

• ***When data is read***
When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN (P00) terminal can be read by this register.
The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SSD}) level bit "0" input from SIN (P00) terminal. Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers will be undefined.

EISIF: Interrupt mask register (F0H•D1)
This is the interrupt mask register of the serial interface.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

With this register, masking of the serial interface interrupt can be selected.
At initial reset, this register is set to "0".

ISIF: Interrupt mask register (F4H•D0)
This is the interrupt factor flag of the serial interface.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.
The interrupt factor flag is reset when it has been read out.
Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8-bit data input/output.
Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.
At initial reset, this flag is set to "0".

4.10.6 Programming notes

(1) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

(3) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated.

4.11 A/D Converter

4.11.1 Configuration of A/D converter

The E0C62M2 has a built-in dual slope type A/D converter and an analog switch circuit. Combination of the A/D converter and the analog switch circuit make up the DMM (digital multimeter), and can measure various items. See Section 4.12, "Measurement Circuit and Measurement Procedure", for measurement when using these circuits as DMM.
Two types of resolution and conversion time are set in the E0C62M2 A/D converter as follows:

Mode	*Resolution (count)*	*Conversion time (msec)*
Normal mode	4,370	400
High-speed mode	441	100

See Chapter 7, "ELECTRICAL CHARACTERISTICS", for the conversion precision.
Figure 4.11.1.1 shows the A/D converter block diagram.

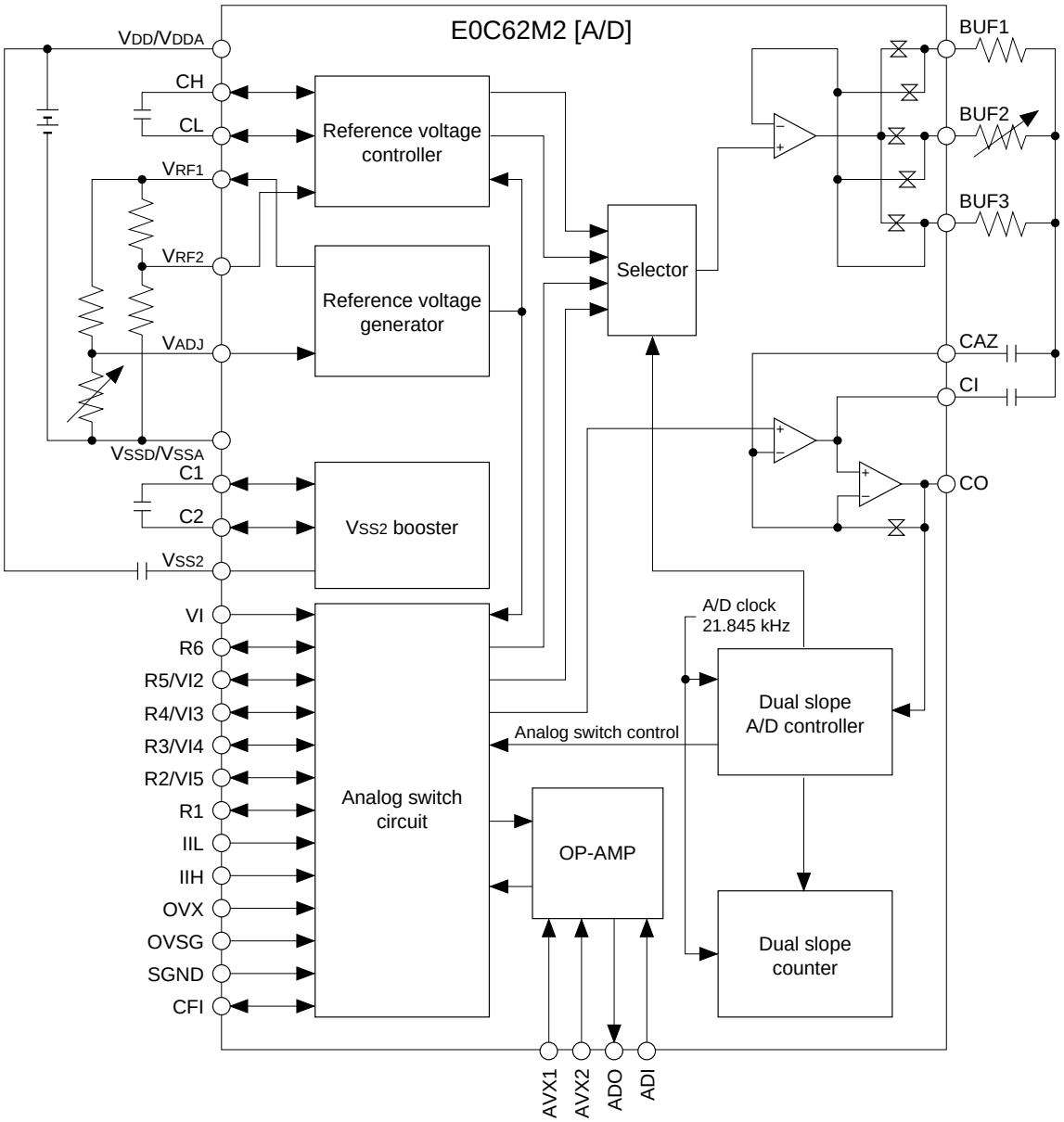


Fig. 4.11.1.1 A/D converter block diagram

4.11.2 Power supply and reference voltage generator for A/D converter

The A/D converter operates with VSSA as the analog GND, VDDA as the positive power and VSS2 as the negative power. VSS2 is the voltage generated by the voltage booster built into the E0C62M2. Therefore, be sure to turn the VSS2 booster ON before operating the A/D converter. See Section 4.13, "VSS2 Booster" for details of the VSS2 booster.
Figure 4.11.2.1 shows the configuration of the A/D converter power supply system.

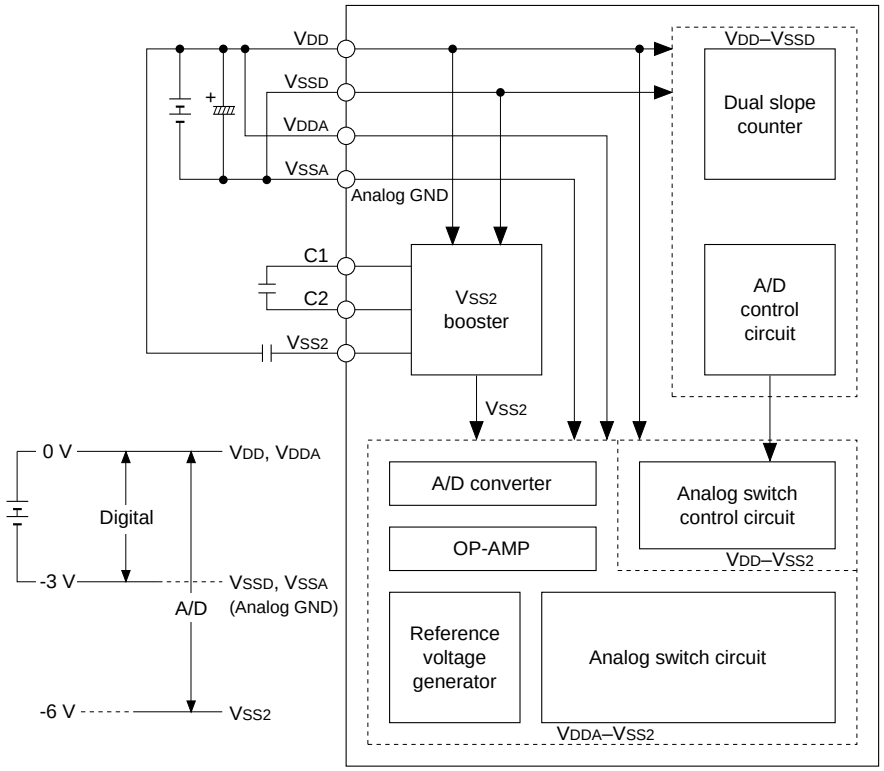


Fig. 4.11.2.1 Configuration of A/D converter power supply system

The E0C62M2 generates the reference voltage VRF1 by turning the A/D converter ON. Another reference voltage VRF2 that is needed for A/D conversion is generated by dividing with resistors connected to the E0C62M2 externally.
Figure 4.11.2.2 shows the circuit diagram of the reference voltage generator.

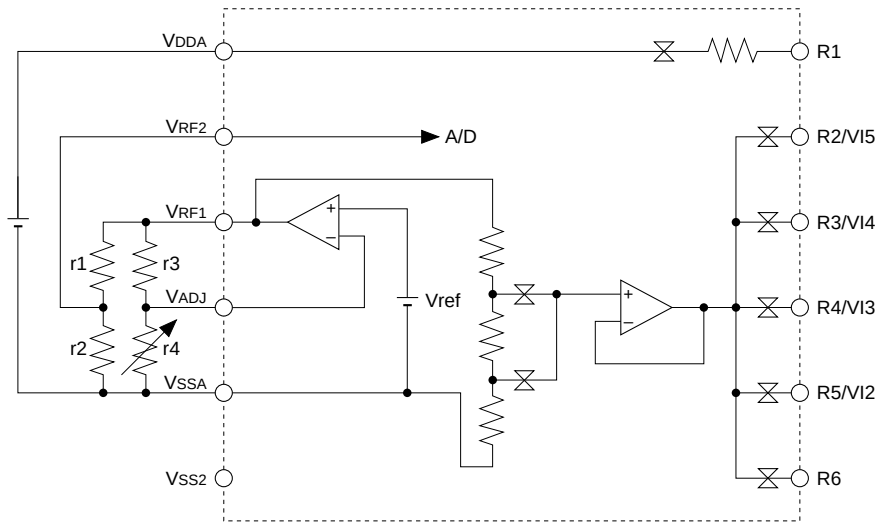


Fig. 4.11.2.2 Circuit diagram of reference voltage generator

The reference voltage V_{RF2} (218.5 mV) after dividing with external resistors is supplied to inside of the E0C62M2 from the V_{RF2} terminal and is used as the reference voltage for the A/D converter. The V_{RF1} and V_{RF2} voltage values can be adjusted using the variable resistor r4 shown in Figure 4.11.2.2. The V_{RF1} and V_{RF2} voltage values should be set as below.

V_{RF1} = 1.0 to 1.2 V (V_{RF1}–V_{SSA})
$V_{RF2} \approx$ 218.5 mV (V_{RF2}–V_{SSA})

The following shows the voltage values of r1 to r4 (shown in Figure 4.11.2.2) for reference.

r1 = 82 kΩ r2 = 22 kΩ r3 = 120 kΩ r4 = 75 k–412 kΩ

The V_{RF1} voltage is used as the reference voltage for generating the measurement voltage at the time of resistance measurements. The V_{RF2} voltage is supplied to the A/D converter as the positive reference voltage (+V_R) and the negative reference voltage (-V_R) via the reference voltage controller.

4.11.3 Clock for A/D converter

The E0C62M2 uses a 21.845 kHz clock for the A/D converter. This clock is generated by dividing the clock from the OSC1 oscillation circuit (32.768 kHz).

[32.768 kHz × 2/3 = 21.845 kHz (A/D conversion clock)]

The divider is built into the V_{SS2} booster, so be sure to turn the V_{SS2} booster ON before turning the A/D converter ON. See Section 4.13, "V_{SS2} Booster" for details.

4.11.4 A/D converter control circuit (Dual slope A/D controller)

The E0C62M2 has a built-in timing circuit (clock counter), that sets the time (period) of the auto zero adjustment, the input integral and the reverse integral, within the A/D converter control circuit (dual slope A/D controller). The A/D converter is controlled with the signal from the timing circuit. The timing circuit uses a 21.845 kHz clock from the V_{SS2} booster.
Table 4.11.4.1 shows the clock numbers that are taken for each period (auto zero adjustment, input integral and reverse integral).

Table 4.11.4.1 Number of clocks for A/D conversion

Mode	Auto zero adjustment	Input integral	Reverse integral	Total
High speed mode	1526	218	441	2185
Normal mode	2185	2185	4370	8740

1 clock: 1/21845 sec

4.11.5 Operation of dual slope type A/D converter

Figure 4.11.5.1 shows the circuit diagram of the A/D converter built into the E0C62M2.

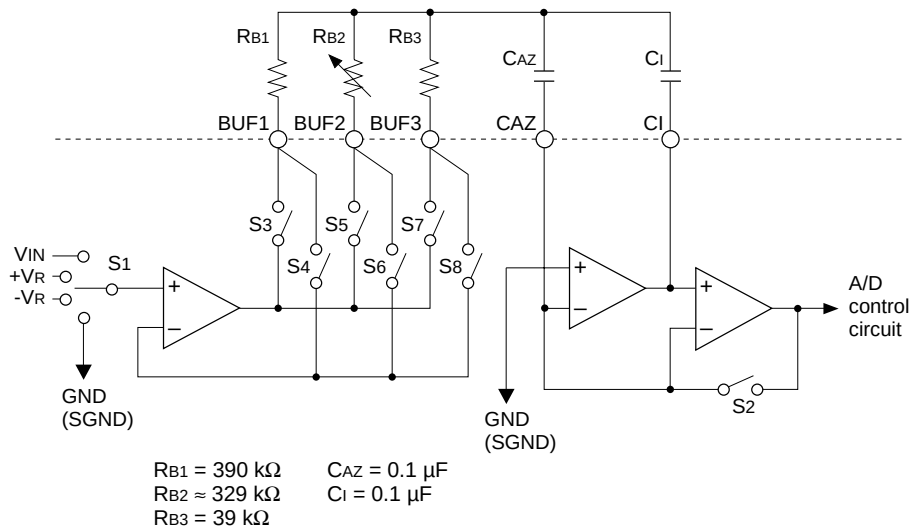


Fig. 4.11.5.1 Circuit diagram of A/D converter

This A/D converter performs A/D conversion according to the following three sequences.

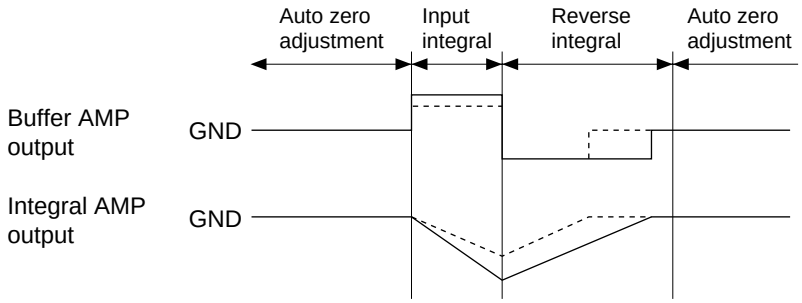
- Auto zero adjustment period
- Input integral period
- Reference voltage reverse integral period

The time of respective periods becomes as shown in Table 4.11.5.1 according to the high-speed mode and normal mode (setting of ADSPD, E2H•D1 in the I/O memory).

Table 4.11.5.1 A/D conversion time

ADSPS	Resolution	Auto zero adjustment	Input integral	Reverse integral	Total time
0	4370	100 msec	100 msec	200 msec	400 msec
1	441	70 msec	10 msec	20 msec	100 msec

• ***When input voltage is positive pole (V_{SSA} = GND)***



• ***When input voltage is negative pole (V_{SSA} = GND)***

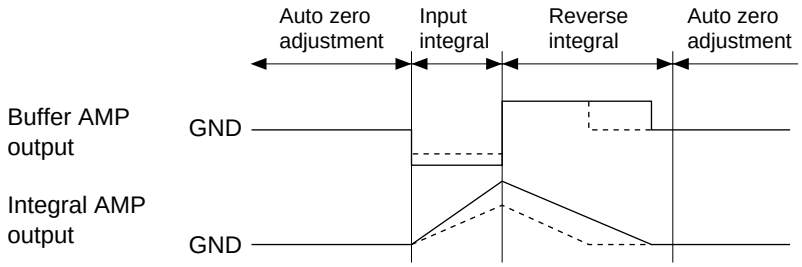


Fig. 4.11.5.2 Output waveform during A/D conversion

The following will explain the outline of A/D operations in the respective period. However in the resistance measurement mode, there are differences in the operation in the reverse integral period, operation in the high-speed mode, and the reference voltage that is used during reverse integral. See Section 4.12, "Measurement Circuit and Measurement Procedure", for details.

(1) A/D conversion in normal mode

1. Auto zero adjustment period

Auto zero adjustment is the sequence initially effected in order to compensate for error in the A/D conversion results, due to the offset voltage of the buffer AMP (BUF), integral AMP (INT) and comparator (CMP).

The switch S1 in Figure 4.11.5.1 is connected to the GND at the beginning of this period and the switches S2, S3, S4, S7 and S8 go ON to discharge the capacitor C_I. At this time, the resistors (R_{B1} and R_{B3}) that are connected to the BUF1 and BUF3 terminals are used in parallel for discharge.

Then the switches S7 and S8 go OFF, and voltage is charged into C_{AZ} to correct the offset.

2. Input integral period

When the auto zero adjustment period terminates, the A/D converter starts the integral of the input voltage by connecting the switch S1 to the V_{IN} side, turning the switch S2 OFF and turning the switches S3 and S4 ON. The input voltage of the integral AMP changes according to the time constant of the integral resistance R_{B1} and the capacitor C_I, and the waveform indicated in Figure 4.11.5.2 is output from the integral AMP. The slope of this integral output waveform changes in proportion to the input voltage. The portion charged into the C_{AZ} due to the previous auto zero adjustment is added to the input voltage of the integral AMP and negates the offset voltage.
The time of the input integral period is obtained by counting the A/D clock (21.845 kHz) 2,185 times. (The A/D clock is generated from the V_{SS2} booster in dividing the OSC1 clock by 1.5.)

$$tx = \frac{1}{32{,}768 \times (2/3)} \times 2185 \approx 100 \text{ msec} \qquad \text{(Equation 4.11.5.1)}$$

Relation between the integral AMP output voltage V_{INT} and time t is indicated by the following equation.

$$V_{INT} = -V_{IN} \times \frac{t}{C_I \times R_B} \qquad \text{(Equation 4.11.5.2)}$$

V_{IN}: Input voltage
t: Integral time
C_I: Integral capacity
R_B: Integral resistance

3. Reference voltage reverse integral period

When the input integral period is completed, the A/D converter shifts into the reverse integral period using the reference voltage. The switch S1 is connected to the $+V_R$ or $-V_R$ side and the switch S2 is kept in OFF.
The side of opposite polarity to the input voltage that effected the integral in step 2 is selected for the polarity of the reference voltage V_R.

- When the input voltage V_{IN} is positive: Switch S1 connects to the $-V_R$ side
- When the input voltage V_{IN} is negative: Switch S1 connects to the $+V_R$ side

For this purpose, the polarity of the input voltage is checked by a comparator for the input integral period, and which of the polarities to be used is selected in advance.

At the same time as it begins the reverse integral by the reference voltage, the dual slope counter begins counting up using the 21.845 kHz clock. The content of this counter is reset to the input integral period and hence counts up from "0".
Reverse integral continues until the comparator detects that the output of the integral AMP has become "0" (GND) and at that point the dual slope counter stops, then shifts to the next A/D conversion sequence (auto zero adjustment period).
Since the slope of the reverse integral waveform is fixed (except for the resistance measurement mode), the counter value according to the integral result of the input voltage in step 2 is obtained from the dual slope counter. The counter value n at this time is indicated by the following equations.

Output voltage V_X of the integral AMP when an input integral period has finished is

$$V_X = -V_{IN} \times \frac{tx}{C_I \times R_B} \qquad \text{(Equation 4.11.5.3)}$$

V_{IN}: Input voltage
tx: Integral time (1/21.845 kHz) × (2,185 counts)
C_I: Integral capacity
R_B: Integral resistance

The reverse integral is done using the reference voltage V_R. If a counter value when the reverse integral has completed is n, the voltage change V_S during the reverse integral is

$$V_S = -V_R \times \frac{1/21{,}845 \times n}{C_I \times R_B} \qquad \text{(Equation 4.11.5.4)}$$

Since the output voltage V_{INT} of the integral AMP when the reverse integral has completed becomes "0" (GND),

$$V_{INT} = V_X - V_S = 0 \qquad V_X = V_S \qquad \text{(Equation 4.11.5.5)}$$

According to Equations 4.11.5.3, 4.11.5.4 and 4.11.5.5,

$$n = \frac{V_{IN} \times 2185}{V_R} \qquad \text{(Equation 4.11.5.6)}$$

Since the reference voltage V_R is set to 218.5 mV in the E0C62M2, n becomes as below.

$$n = V_{IN} \times 1000$$

The dual slope counter is a decimal counter. Consequently, if 120 mV is input to the V_{IN} terminal, the counter value becomes "1,200". (Actually it may not become "1,200" because a conversion error occurs. See Chapter 7, "ELECTRICAL CHARACTERISTICS", for the conversion error.)
The counter data is loaded into the registers of addresses E7H to EAH when an A/D conversion has finished (when the reverse integral has finished) and is maintained until the next A/D conversion is finished. A/D conversion results can be obtained by reading the addresses E7H to EAH.

(2) A/D conversion in high speed mode

1. Auto zero adjustment period

In the auto zero adjustment period during the high speed mode, the switch S1 in Figure 4.11.5.1 is connected to the GND at the beginning of this period and the switches S2, S7 and S8 go ON. In this status, the capacitor C_I is discharged and the capacitor C_{AZ} is charged to correct the offset.
This period in the high speed mode is 70 msec.

2. Input integral period

The input integral period in the high speed mode differs from the normal mode in the following two points: one is the integral resistance R_{B3} that is connected to the BUF3 terminal is used, and another is it takes 10 msec for an input integral period.
The time of the input integral period is obtained by counting the A/D clock (21.845 kHz) 218 times. (The A/D clock is generated from the V_{SS2} booster in dividing the OSC1 clock by 1.5.)

$$tx = \frac{1}{32{,}768 \times (2/3)} \times 218 \approx 10 \text{ msec} \qquad \text{(Equation 4.11.5.7)}$$

The high speed mode uses the resistor R_{B3} connected to the BUF3 terminal for integration. The slope of the integral waveform output from the integral AMP (Figure 4.11.5.2) steepens than that of the normal mode because the R_{B3} is set smaller than the integral resistance R_{B1} used in the normal mode.

3. Reverse integral period

Output voltage V_X of the integral AMP when an input integral period during the high speed mode has finished is

$$V_X = -V_{IN} \times \frac{tx}{C_I \times R_B} \qquad \text{(Equation 4.11.5.8)}$$

V_{IN}: Input voltage
tx: Integral time (1/21.845 kHz) × (218 counts)
C_I: Integral capacity
R_B: Integral resistance

The value of the reference voltage V_R that is used for the reverse integral in the high speed mode is the same as the normal mode.
According to Equations 4.11.5.6 and 4.11.5.8, nH (counter value in the high speed mode) is calculated as below.

$$nH = \frac{V_{IN} \times 218}{V_R} \qquad \text{(Equation 4.11.5.9)}$$

Since the value of the reference voltage V_R is the same as the normal mode, conversion errors in the high speed mode occurs more frequently than in the normal mode.
The counter data is loaded into the registers of addresses E7H to EAH even in the high speed mode. However in the high speed mode, the register value of the address E7H is always "0", and the upper three digits are effective for the conversion results.

Table 4.11.5.2 Example of A/D conversion result

When the input voltage V_{IN} = 234.2 [mV]

Mode	Maximum count number	A/D data register			
		EAH	E9H	E8H	E7H
Normal mode	4370	2	3	4	2
High speed mode	441	2	3	4	0

* In the high speed mode, E7H is always "0".
* Data in the above table is for reference, and is not guaranteed.

4.11.6 A/D conversion and interrupt

This section explains about the control and interrupt of the A/D conversion and reading of data.

(1) Turning A/D converter ON/OFF

The power supply to the circuit of the A/D converter is normally kept OFF, in order to reduce current consumption. The A/D converter starts when "1" is written into the register ADON and continues to operate until a "0" has been written. It terminates A/D conversion when a "0"is written into the ADON and the circuit also goes OFF.
The ADON can be read and is "1" while the circuit is operating and is "0" when it is stopped.
When "1" is written into the ADON, it resets the A/D converter (resets the dual slope counter to "0") and executes the A/D conversion sequence from the auto zero adjustment. Writing "1" into ADON is also effective during A/D conversion and it terminates the sequence during the current execution and starts a new A/D conversion sequence.

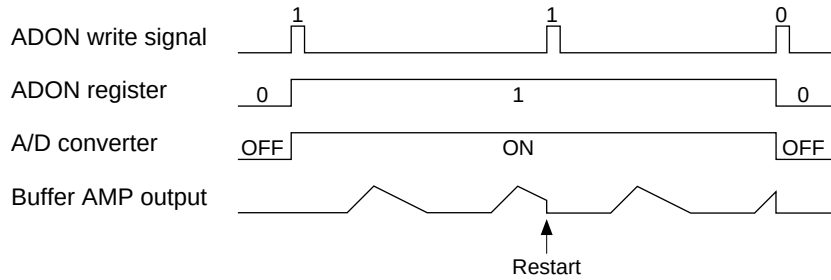


Fig. 4.11.6.1 Control of A/D conversion by the ADON register

(2) A/D interrupt

When an input integral period has terminated and the reverse integral starts according to the reference voltage, the dual slope counter is counted up from "0". At the point where the integral AMP output due to the reverse integral has crossed "0", the count stops and the data of the dual slope counter is latched. When the reverse integral period has terminated, the A/D interrupt factor flag IAD is set to "1" and an interrupt occurs.
The A/D interrupt can also be masked by writing a "0" into the interrupt mask register EIAD. When EIAD is set to "1", an interrupt occurs.
The interrupt factor flag IAD is set to "1" when the reverse integration period has terminated, regardless of the setting of the interrupt mask register and is reset to "0" by reading.
Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause a malfunction.

(3) Reading of A/D conversion result

The dual slope counter is a four-digit decimal counter and is configured with three 4-bit data corresponding to E7H, E8H and E9H, and one 3-bit data corresponding to EAH. This counter counts up from "0" in decimals during the reverse integration period. The result that has been counted is latched upon completion of the reverse integral period and the data from that latch can be read. This data (DSC00–DSC32) is allocated to the addresses E7H–EAH. The register ADP that indicates the polarity of inputs during the input integral period is allocated to E6H. When an input is positive (+) the ADP becomes "1" and when it is negative (-) it becomes "0".

The latched data is effective until the next A/D conversion is completed and it is necessary to read up to that point. Basically the read processing should be done using the A/D interrupt. Moreover, the data should read in order of E7H → E8H → E9H → EAH from the lower side. This is because to the following reason.
When the following A/D conversion terminates during data reading, the latched data is just rewritten. For this reason, the IDR bit is set into the address EBH, so that it can decide whether the data read is effective or invalid, by reading the IDR bit following the reading of data. When the reading of the data in the above sequence has been completed prior to the termination of the next A/D conversion, the IDR becomes "0", indicating that the data is effective. When the following A/D conversion has been terminated and the latch rewritten before the reading terminates, the IDR becomes "1", indicating that the data is invalid.
The circuit that sets this IDR decides whether the data has been read and the reading terminated by the above mentioned data read address. Consequently, data reading should be done in the above mentioned sequence and then decide whether the data is effective or invalid by reading the IDR.
Further, be sure to read the data while the A/D converter is ON (ADON = "1"). Be aware that conversion data may sometimes become invalid by turning the A/D converter OFF. In addition, the latched data is cleared when the CPU enters SLEEP mode.
Figure 4.11.6.2 shows a timing chart for the A/D conversion.

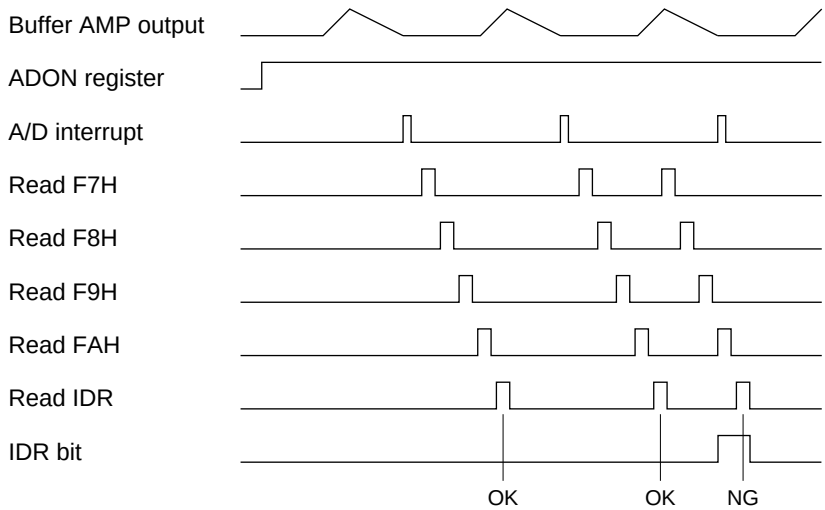


Fig. 4.11.6.2 A/D conversion timing chart

Note: The A/D converter automatically restarts from the auto zero adjustment period when writing is done to the registers on the addresses listed below.

E2H ...A/D converter setting registers (ADON, ADSPD, IIN, BUFF)
E4H ...Measurement function selection registers (FNC0, FNC1, FNC2)
E5H ...Measurement range selection registers (RNG0, RNG1, RNG2)

The auto restart is done by writing with software only.
Furthermore, these registers are set to the initial status when the CPU enters SLEEP mode (A/D converter is OFF status). Therefore, set the above registers again when the CPU reactivates from SLEEP status.

4.11.7 Control of A/D converter

Table 4.11.7.1 lists the A/D converter's control bits and their addresses.

Table 4.11.7.1 Control bits of A/D converter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E2H	BUFF	IIN	ADSPD	ADON	BUFF	0	–	–	Fix at 0
					IIN	0	IIH	IIL	Current measurement terminal switching
	R/W				ADSPD	0	100 mS	400 mS	A/D conversion speed switching
					ADON	0	On	Off	A/D converter On/Off
E6H	0	0	0	ADP	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					ADP	1	Positive	Negative	A/D converter polarity judgment
E7H	DSC03	DSC02	DSC01	DSC00	DSC03	0	1	0	A/D conversion data (00–03)
					DSC02	0	1	0	
	R				DSC01	0	1	0	
					DSC00	0	1	0	
E8H	DSC13	DSC12	DSC11	DSC10	DSC13	0	1	0	A/D conversion data (10–13)
					DSC12	0	1	0	
	R				DSC11	0	1	0	
					DSC10	0	1	0	
E9H	DSC23	DSC22	DSC21	DSC20	DSC23	0	1	0	A/D conversion data (20–23)
					DSC22	0	1	0	
	R				DSC21	0	1	0	
					DSC20	0	1	0	
EAH	0	DSC32	DSC31	DSC30	0 *5	– *2			Unused
					DSC32	0	1	0	A/D conversion data (30–32)
	R				DSC31	0	1	0	
					DSC30	0	1	0	
EBH	0	IDR	STS1	STS0	0 *5	– *2			Unused
					IDR	0	Invalid	Effective	Read data status
	R				STS1	0			A/D conversion status 0: auto zero adjustment,
					STS0	0			1: input integral, 3: reverse integral
F0H	EIK1	EIK0	EISIF	EIAD	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
	R/W				EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
					EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F6H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				0 *5	– *2			Unused
					IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

ADON: A/D converter control (E2H•D0)

Turns the A/D converter ON/OFF and restarts it.

When "1" is written: ON and restart
When "0" is written: OFF
Reading: Valid

When "1" is written to the ADON register while the A/D converter is in the stop status, the A/D converter and the reference voltage generator start operating. If "1" is written to the ADON register during an A/D conversion, the A/D conversion is interrupted and a new A/D conversion cycle (from the auto zero adjustment) starts.
When "0" is written to the ADON register, the A/D conversion is terminated and the A/D converter goes OFF.
At initial reset and in SLEEP mode, this register is set to "0".

ADSPD: A/D conversion speed switching (E2H•D1)

Switches the conversion mode of the A/D converter.

When "1" is written: High speed mode (100 msec)
When "0" is written: Normal mode (400 msec)
Reading: Valid

When "1" is written to the ADSPD register, the A/D conversion mode is set to the high speed mode. If the A/D conversion mode is changed to the high speed mode during A/D conversion in the normal mode by writing "1" to this register, the A/D conversion in the normal mode is interrupted and it restarts from the auto zero adjustment in the high speed mode.
At initial reset and in SLEEP mode, this register is set to "0".

IIN: Current measurement terminal switching (E2H•D2)
BUFF: (E2H•D3)

...See Section 4.12, "Measurement Circuit and Measurement procedure".

ADP: A/D converter polarity judgment (E6H•D0)

Indicates the polarity of the input voltage.

When "1" is read: Positive pole
When "0" is read: Negative pole
Writing: Invalid

By reading this register with software, the polarity of the input voltage that is input to the A/D converter during the input integral period can be checked. When the A/D converter input voltage during the input integral period is positive (+), the ADP becomes "1" and when it is negative (-), it becomes "0".
This data is rewritten at the same time with the A/D conversion data (E7H–EAH)
At initial reset and in SLEEP mode, this register is set to "1".

DSC00–DSC32: A/D conversion data (E7H–EAH•D2)

Decimal data of an A/D conversion result that is counted during the reverse integral period by the dual slope counter.
This data is effective from the time when the reverse integral period has terminated until the next reverse integral period is terminated. Read the data during this period in the order of the address E7H→E8H→E9H→EAH.
At initial reset and in SLEEP mode, these registers are set to "0".

STS0, STS1: A/D conversion status (EBH•D0, D1)

Indicates the A/D converter status.

Reading:

STS1	STS0	Status
0	0	During auto zero adjustment
0	1	During input integral execution
1	1	During reverse integral execution

There is no setting of (STS1, STS0) = (1, 0)

Writing: Invalid

By reading these bits, the execution status of the A/D converter can be checked as in the above table.When the A/D converter terminates a reverse integral period, the status indication becomes "during auto zero adjustment".
At initial reset and in SLEEP mode, STS0 and STS1 are set to "0".

IDR: Read data status (EBH•D2)

Indicates whether the data that has been read is effective or invalid.

When "1" is read: Data invalid
When "0" is read: Data effective
Writing: Invalid

It can decide whether the data that has been read is effective or invalid by reading the IDR after data has been read.

When the reading of the data has completed before the next A/D conversion terminates, the IDR is set to "0". When the next A/D conversion terminates before the previous data is read, the IDR is set to "1" to indicate data invalid, so that the data will be rewritten. The IDR that has been set to "1" is reset to "0" by reading.
At initial reset and in SLEEP status, the IDR is set to "0".

EIAD: Interrupt mask register (F0H•D0)
Select whether to mask interrupt with the A/D converter.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

The A/D interrupt is permitted when "1" is written in the EIAD. When "0" is written, the interrupt is masked.
At initial reset, this register is set to "0".

IAD: Interrupt factor flag (F6H•D0)
This flag indicates interrupt caused by the A/D converter.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

From the status of this flag, the software can decide whether an A/D interrupt has occurred.
This flag is reset when the software has read it.
Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.
The IAD is set to "1" when a reverse integral period has finished even if the interrupt has been masked.
The interrupt factor flag may be set when the A/D conversion setting is changed or the CPU enters SLEEP status. Therefore, read (clear) the flag if necessary.
See Section 4.12, "Measurement Circuit and Measurement Procedure", for details of E4H (A/D conversion function switching) and E5H (Range switching).
At initial reset, this flag is set to "0".

4.11.8 Programming notes

(1) Be sure to check whether the data is effective or invalid by reading the A/D conversion data in the order F7H → F8H → F9H → FAH and immediately thereafter reading the IDR.

(2) The interrupt factor flag may be set when the A/D conversion setting is changed (writing to E2H, E4H or E5H) or the CPU enters SLEEP status. Therefore, read (clear) the flag if necessary.

(3) The A/D converter is automatically set to the auto zero adjustment period when writing is done to the addresses E2H, E4H (function switching) and E5H (range switching). If the ADON register has been set to "1" (A/D converter is ON) at this time, the A/D conversion restarts with the new settings from the auto zero adjustment.

(4) The registers on the addresses E2H and E4H to EBH are set to initial status when the CPU enters SLEEP mode. Therefore, set the registers again when the CPU reactivates from SLEEP status.

(5) Write the interrupt mask register (EIAD) only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause a malfunction.

(6) Reading of interrupt factor flag is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flag to be read is set to "1", an interrupt request will be generated by the interrupt factor flag set timing, or an interrupt request will not be generated.

4.12 Measurement Circuit and Measurement Procedure

4.12.1 Sort of measurement

The E0C62M2 has a built-in dual slope type A/D converter and an analog switch circuit. Combination of the A/D converter and the analog switch circuit make up the DMM (digital multimeter), and can measure various items. The measurement mode can be set using the measurement function selection register (FNC0–FNC2) on the address E4H. Table 4.12.1.1 shows the relationship of the measurement function selection register and the measurement mode that are available in the E0C62M2.

Table 4.12.1.1 Measurement mode on E0C62M2

Address	D3	D2	D1	D0	Measurement mode	Range	Remarks
E4H	*	0	0	0	DC voltmeter mode (DCV)	5	400 mV range to 1000 V
	*	0	0	1	AC voltmeter mode (ACV)	5	400 mV range to 750 V
	*	0	1	0	DC ammeter mode (DCA)	–	Measurement terminal 2 systems
	*	0	1	1	AC ammeter mode (ACA)	–	Measurement terminal 2 systems
	*	1	0	0	Resistance measurement mode (Ω)	6	400 Ω range to 40 MΩ
	*	1	0	1	Continuity check mode (CONT)	4	50, 100, 500, 1 kΩ
	*	1	1	0	–	Fixed	Fixed at 4 V range
	*	1	1	1	ADPT mode (ADPT)	Fixed	Fixed at DCV 400 mV range

* Bit D3 is invalid

The E0C62M2 automatically controls the general amplifier (for AC-DC conversion), comparator (for continuity check) and integral resistors (BUF1 to BUF3 terminals) according to the switching of the above measurement modes.
Table 4.12.1.2 shows the relationship of the measurement modes and the peripheral circuits.

Table 4.12.1.2 Measurement modes and peripheral circuits

Measurement function	Input terminal	General amplifier	Comparator	Integral resistor		Polarity judgment (ADP)
				Normal mode	High speed mode	
DCV	VI	OFF	OFF	BUF1 terminal	BUF3 terminal	Available
ACV	VI	ON	OFF			Fixed at (+)
DCA	IIL or IIH	OFF	OFF	*1		Available
ACA	IIL or IIH	ON	OFF			Fixed at (+)
Ω	OVX, OVSG	OFF	OFF	Input integral: BUF1		Fixed at (+)
CONT	OVX, OVSG	OFF	ON	Reverse integral: BUF1+ BUF2		Fixed at (+)
–	VI	OFF	OFF	BUF1 terminal	BUF3 terminal	Fixed at (+)
ADPT	VI	OFF	OFF			Fixed at (+)

*1 See Section 4.12.4, "Current measurement".

The general AMP (amplifier) goes ON during the AC ammeter mode or AC voltmeter mode.
The comparator goes ON during the continuity check mode.
The polarity judgment register ADP is available only in the DC voltmeter mode or DC ammeter mode. In the other modes, it is always fixed at "1" (positive pole).
In the DC/AC ammeter mode, either the IIH terminal or IIL terminal can be selected as the input terminal using the IIN register.
For the integral resistor in the resistance measurement mode, the resistor that connected to the BUF1 terminal is used during the input integral period, and the resisters that are connected to the BUF1 and BUF2 terminals are used in parallel during the reverse integral period. It is the same with the normal mode and high speed mode of the A/D converter.
The continuity check mode measures resistance too. The settings of the integral resistors are the same as the resistance measurement mode.
See each of the following sections for range settings.

Figure 4.12.1.1 shows the measurement circuit for the E0C62M2.

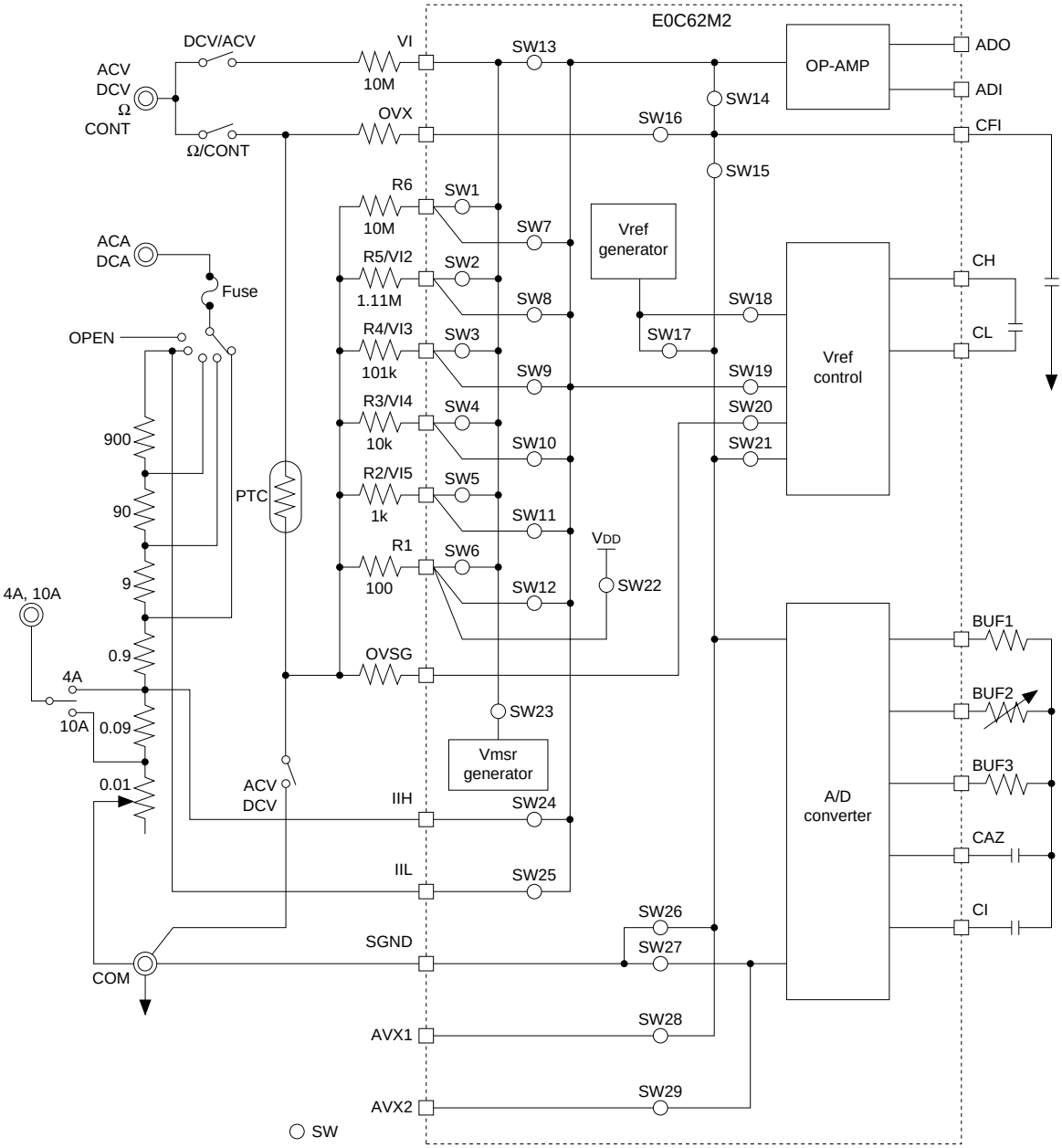


Fig. 4.12.1.1 Measurement circuit

4.12.2 General AMP

The E0C62M2 has a built-in general AMP (amplifier). It is used for AC/DC conversion in the AC voltmeter mode or AC ammeter mode. Turning the general AMP ON and OFF can be controlled using the measurement function selection register on the address E4H. When the ACV or ACA mode is selected using the register, the general AMP goes ON and when another mode is selected, it goes OFF.
The AC/DC conversion can be done by connecting an external rectification circuit to the E0C62M2. The AVX1 and AVX2 terminals are used for input to the A/D converter after AC/DC converting.
Figure 4.12.2.1 shows the configuration of the general AMP.

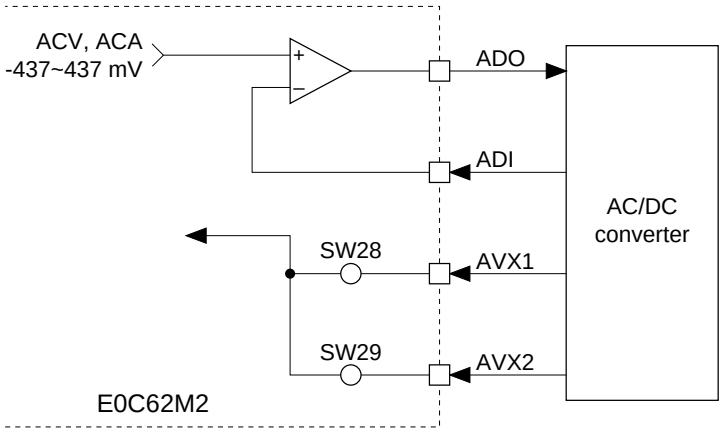


Fig. 4.12.2.1 Configuration of general AMP

4.12.3 Voltage measurement

Voltage measurement is done by A/D converting the voltage divided with the external resistors, 10 MΩ resistor that is connected to the VI terminal and the reference resistor that is connected to the R5/VI2–R2/VI5 terminal.
Figure 4.12.3.1 shows the circuit configuration for voltage measurements.

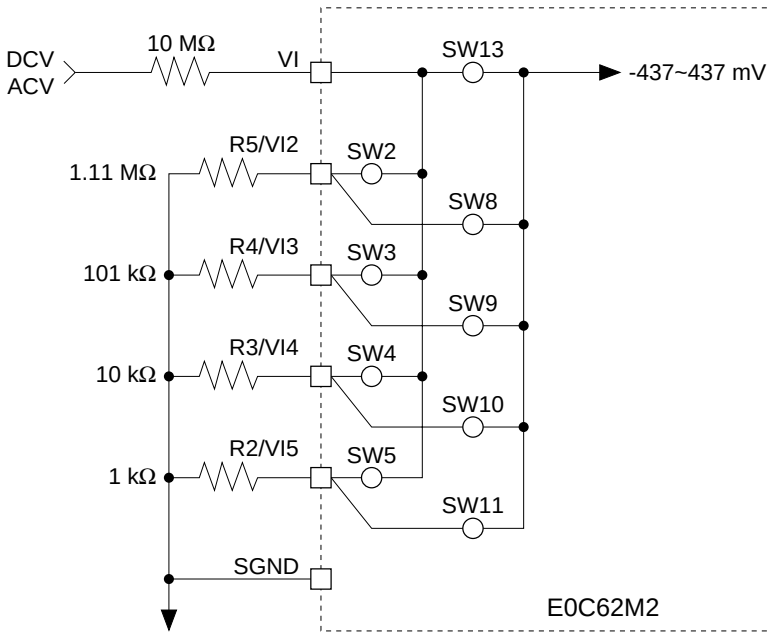


Fig. 4.12.3.1 Circuit configuration for voltage measurements

Table 4.12.3.1 shows the condition on the range settings during voltage measurement.

Table 4.12.3.1 Range settings during voltage measurement

Measurement range	E5H			Switches to be ON	Input to A/D converter	Dividing terminal
	D2	D1	D0			
	RNG2	RNG1	RNG0			
400 mV	0	0	0	SW13	Direct input from VI terminal	–
4 V	0	0	1	SW2, SW8	$V_{IN} \times \{1.11\ M\Omega / (10\ M\Omega + 1.11\ M\Omega)\}$	R5/VI2
40 V	0	1	0	SW3, SW9	$V_{IN} \times \{101\ k\Omega / (10\ M\Omega + 101\ k\Omega)\}$	R4/VI3
400 V	0	1	1	SW4, SW10	$V_{IN} \times \{10\ k\Omega / (10\ M\Omega + 10\ k\Omega)\}$	R3/VI4
1000 V	1	0	0	SW5, SW11	$V_{IN} \times \{1\ k\Omega / (10\ M\Omega + 1\ k\Omega)\}$	R2/VI5

V_{IN}: Voltage to be measured

In the voltmeter mode, voltage to be measured is input to the A/D converter after dividing it with the resistor on the VI terminal (10 kΩ) and one of the reference resistors on the R5/VI2 through R2/VI5 terminals as shown in the above table.
In the DC voltmeter mode, the divided voltage is directly input to the A/D converter. In the AC voltmeter mode, the divided voltage is input to the A/D converter via the AVX1 and AVX2 terminals after inputting it to the general AMP to convert from AC to DC.
The A/D converter uses the input from the SGND terminal as the GND level input. Therefore, the input to the SGND terminal should be directly connected to the COM port of the DMM (digital multimeter).

4.12.4 Current measurement

Current measurement is done by A/D converting the voltage that is converted from the current on the outside of the E0C62M2. Two analog input terminals, IIH terminal and IIL terminal, are provided for current measurements and the terminal to be used can be selected by software.
Figure 4.12.4.1 shows the measurement circuit for current measurements.

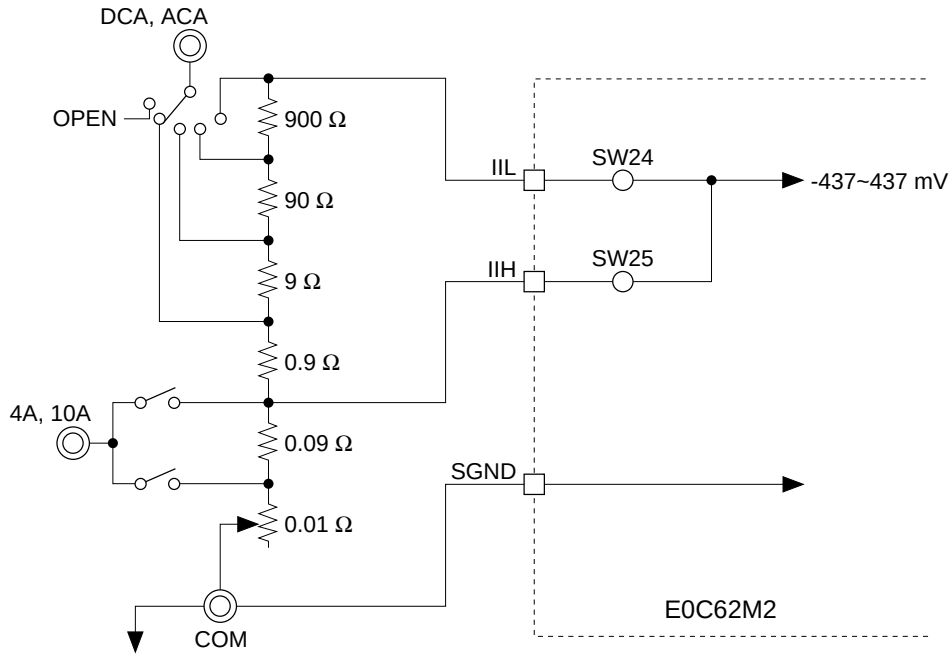


Fig. 4.12.4.1 Measurement circuit for current measurements

Table 4.12.4.1 shows the relationship of the register settings for the ammeter mode and A/D conversion.

Table 4.12.4.1 Register for ammeter mode and A/D convertor settings

E2H			Input terminal	A/D conversion maximum input voltage (mV)	Conversion speed (msec)	Maximum count number (count)	Resolution (μV)
D3	D2	D1					
BUFF	IIN	ADSPD					
0	0	0	IIL	± 437	400	4370	100
0	0	1	IIL	± 437	100	441	100
0	1	0	IIH	± 437	400	4370	100
0	1	1	IIH	± 437	100	441	100
1	0	0	Cannot be used				
1	0	1					
1	1	0					
1	1	1					

Note: "BUFF" (bit D3 on address E2H) must be set to "0". If it is "1", A/D conversion will not be done correctly.

4.12.5 Resistance measurement

Resistance measurement is done by A/D converting the voltage of both sides of the external reference resistor connected to the R1–R6 terminal and the resistor to be measured.
Input to the A/D converter is switched in the input integral period and the reverse integral period as below.

Input integral period: Voltage of both sides of the resistor to be measured
Reverse integral period: Voltage of both sides of the reference resistor

The E0C62M2 generates the voltage needed for measurement and output to the R1–R6 terminals according to the measurement range.
Figure 4.12.5.1 shows the circuit configuration for the resistance measurement mode.

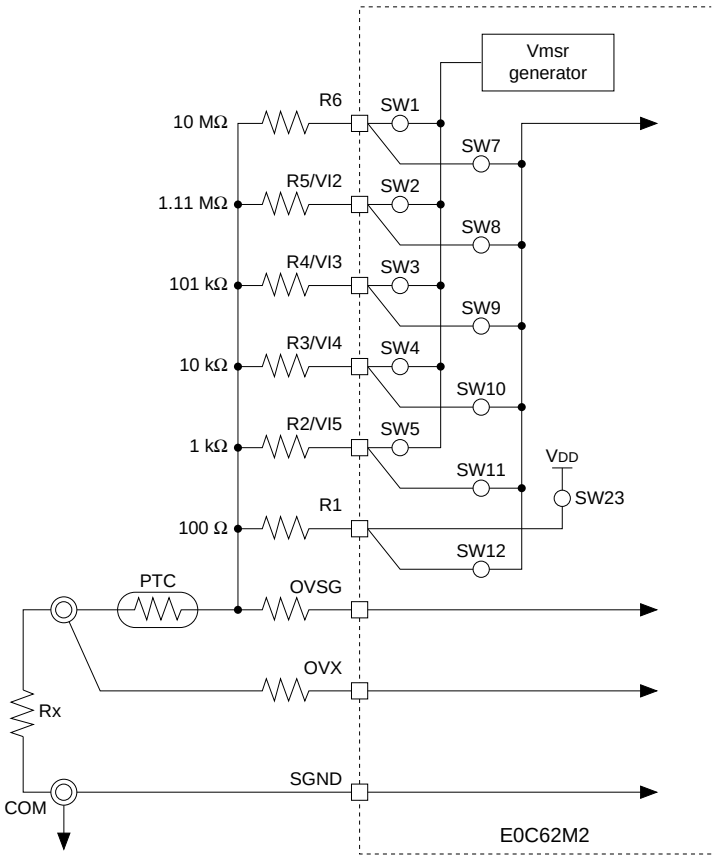


Fig. 4.12.5.1 Circuit configuration for resistance measurement mode

Table 4.12.5.1 shows the condition on the range settings during resistance measurement.

Table 4.12.5.1 Range settings during resistance measurement

Measurement range	E5H			Reference resistor terminal	Reference resistance
	D2	D1	D0		
	RNG2	RNG1	RNG0		
400 Ω	0	0	0	R1	100 Ω
4 kΩ	0	0	1	R2/VI5	1 kΩ
40 kΩ	0	1	0	R3/VI4	10 kΩ
400 kΩ	0	1	1	R4/VI3, R6	$(1/101\ k\Omega + 1/10\ M\Omega)^{-1}$
4 MΩ	1	0	0	R5/VI2, R6	$(1/1.11\ M\Omega + 1/10\ M\Omega)^{-1}$
40 MΩ	1	0	1	R6	10 MΩ

The A/D converter changes the integral resistor setting in the input integral period and the reverse integral period to perform A/D conversion for resistance measurement. In each period, the following integral resistor is used.

Input integral period: Integral resistor on the BUF1 terminal
Reverse integral period: Parallel connected integral resistors on the BUF1 and BUF2 terminals

Usually a variable resistor should be used as the integral resistor on the BUF2 terminal and it should be adjusted by actually measuring resistance. Further the resistance on the BUF2 terminal can be found with the following equation.

$$R_{B2} = \frac{R_{B1} \times Rr/10^{-4}}{N - Rr/10^{-4}}\ [\Omega] \qquad \text{(Equation 4.12.5.1)}$$

R_{B1}: Integral resistance on the BUF1 terminal (390 kΩ)
R_{B2}: Integral resistance on the BUF2 terminal
Rr: Reference resistance on the R6 terminal (10 MΩ)
N: Number of clocks during the input integral period (N = fixed at 2185)

The value that is obtained with the above equation is a theoretical value but actually an error is made.
The A/D converter uses the input from the SGND terminal as the GND level input to integrate the voltage of the measured resistor during the input integral period. Therefore, the input to the SGND terminal should be directly connected to the COM port of the DMM (digital multimeter).

4.12.6 Continuity check

Continuity check is done with the same circuit configuration of the 400 Ω range and 4 kΩ range in the resistance measurement mode. The difference from the resistance measurement mode is that the buzzer signal is generated according to the measured resistance. The continuity judgment and buzzer signal generation are automatically done by the internal hardware of the E0C62M2, so software control is not necessary.
The E0C62M2 judges continuity by comparing both voltage on the measured resistor and reference resistor using the comparator. The continuity judgment signal from the comparator is input to the buzzer circuit and then the buzzer signal is generated.
The comparator for continuity judgment goes ON by setting the address E4H (FNC0–FNC2) to the continuity check mode.
The measurement circuit is the same as the 400 Ω range and 4 kΩ range in the resistance measurement mode.

Figure 4.12.6.1 shows the circuit configuration of the continuity check mode.
Measured resistance can be displayed in this mode as the same as the resistance measurement mode.

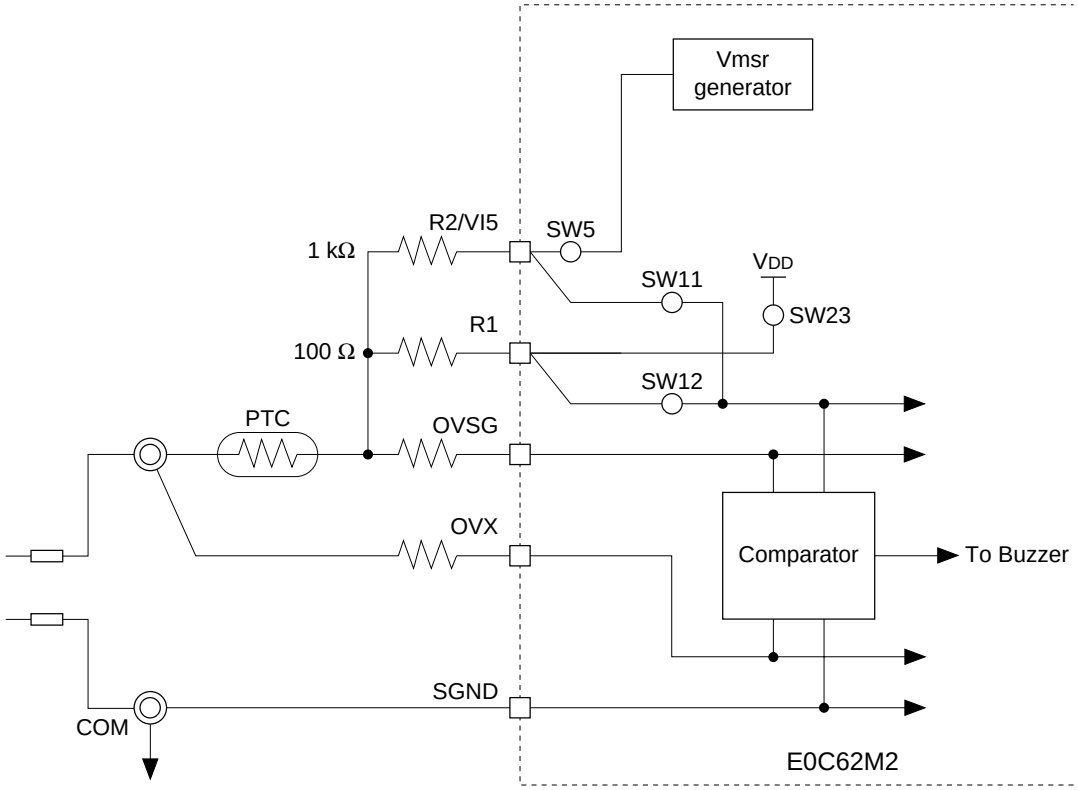


Fig. 4.12.6.1 Circuit configuration of continuity check mode

Table 4.12.6.1 shows the range settings during continuity check mode.

Table 4.12.6.1 Range settings during continuity check mode

Judgment resistance	E5H			Reference resistor	Measurement range
	D2	D1	D0		
	RNG2	RNG1	RNG0		
50 Ω	0	0	0	R1 (100 Ω)	400 Ω
100 Ω	0	0	1	R1 (100 Ω)	
500 Ω	0	1	0	R2/VI5 (1 kΩ)	4 kΩ
1 kΩ	0	1	1	R2/VI5 (1 kΩ)	

When the judgment resistance is 50 Ω or 100 Ω, the circuit configuration is the same as the 400 Ω range in the resistance measurement mode, and when the judgment resistance is 500 kΩ or 1 kΩ, it is the same as the 4 kΩ range in the resistance measurement mode.

4.12.7 ADPT (adapter)

This mode functions the same as the 400 mV range in the DC voltmeter mode and performs the A/D conversion of the voltage input from the VI terminal. However, ADPT mode does not judge polarity, and the measurement range is fixed at 400 mV. Therefore, setting the address E5H (RNG0–RNG2) is invalid and it does not affect the A/D conversion results.

4.12.8 Control method

Table 4.12.8.1 lists the A/D converter's control bits and their addresses.

Table 4.12.8.1 Control bits of A/D converter

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
E2H	BUFF	IIN	ADSPD	ADON	BUFF	0	–	–	Fix at 0
					IIN	0	IIH	IIL	Current measurement terminal switching
	R/W				ADSPD	0	100 mS	400 mS	A/D conversion speed switching
					ADON	0	On	Off	A/D converter On/Off
E4H	0	FNC2	FNC1	FNC0	0 *5	– *2			Unused
					FNC2	0			Measurement function selection *6
	R	R/W			FNC1	0			
					FNC0	0			
E5H	0	RNG2	RNG1	RNG0	0 *5	– *2			Unused
					RNG2	0			Measurement range selection *6
	R	R/W			RNG1	0			
					RNG0	0			

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

BUFF: (E2H•D3)
This bit must be set to "0". If it is "1", A/D conversion will not be done correctly.

IIN: Current measurement terminal switching (E2H•D2)
Selects the input terminal for current measurement.

When "1" is written: Input from IIH terminal
When "0" is written: Input from IIL terminal
Reading: Valid

This register is effective only in the ammeter (current measurement) mode.
Either the IIL terminal or the IIH terminal can be selected as an analog input terminal for current measurement. When "1" is written to this register, input from the IIH terminal is A/D converted. When "0" is written, input from the IIL terminal is A/D converted.
By writing to this register, the A/D converter restarts from the auto zero adjustment period.
At initial reset and in SLEEP mode, this register is set to "0".

FNC0–FNC2: Measurement function selection (E4H•D0–D2)
Switches the measurement function of the E0C62M2. Table 4.12.8.2 shows the measurement function and the register setting.

Table 4.12.8.2 E0C62M2 measurement function

Address	D3 0	D2 FNC2	D1 FNC1	D0 FNC0	Measurement mode
E4H	–	0	0	0	DC voltmeter mode (DCV)
	–	0	0	1	AC voltmeter mode (ACV)
	–	0	1	0	DC ammeter mode (DCA)
	–	0	1	1	AC ammeter mode (ACA)
	–	1	0	0	Resistance measurement mode (Ω)
	–	1	0	1	Continuity check mode (CONT)
	–	1	1	0	–
	–	1	1	1	ADPT mode (ADPT)

* Bit D3 is invalid

The measurement function can be switched by writing data to the registers FNC0–FNC2. These registers can be read.
By writing to this address (E4H), the A/D converter restarts from the auto zero adjustment period.
At initial reset and in SLEEP mode, these registers are set to "0".
When SLEEP mode is canceled, set these registers again.

RNG0–RNG2: Measurement range selection (E5H•D0–D2)
Selects the measurement range as shown in Table 4.12.8.3.

Table 4.12.8.3 Measurement range selection

Address	D3 0	D2 RNG2	D1 RNG1	D0 RNG0	DCV	ACV	DCA	ACA	Resistance	Continuity check	ADPT
E5H	–	0	0	0	400 mV	400 mV	Invalid	Invalid	400 Ω	50 Ω	Fixed at DCV 400 mV range
	–	0	0	1	4 V	4 V			4 kΩ	100 Ω	
	–	0	1	0	40 V	40 V			40 kΩ	500 Ω	
	–	0	1	1	400 V	400 V			400 kΩ	1 kΩ	
	–	1	0	0	1000 V	750 V			4 MΩ	↑	
	–	1	0	1	↑	↑			40 MΩ	↑	
	–	1	1	0	↑	↑			↑	↑	
	–	1	1	1	↑	↑			↑	↑	

* Bit D3 is invalid

The measurement range can be switched by writing data to the registers RNG0–RNG2. These registers can be read.
By writing to this address (E5H), the A/D converter restarts from the auto zero adjustment period.
At initial reset and in SLEEP mode, these registers are set to "0".
When SLEEP mode is canceled, set these registers again.

4.12.9 Programming notes

(1) The interrupt factor flag may be set when the A/D conversion setting is changed (writing to E2H, E4H or E5H) or the CPU enters SLEEP status. Therefore, read (clear) the flag if necessary.

(2) The A/D converter is automatically set to the auto zero adjustment period when writing is done to the addresses E2H, E4H (function switching) and E5H (range switching). If the ADON register has been set to "1" (A/D converter is ON) at this time, the A/D conversion restarts with the new settings from the auto zero adjustment.

(3) The registers on the addresses E2H and E4H to EBH are set to the initial status when the CPU enters SLEEP mode. Therefore, set the registers again when the CPU reactivates from SLEEP status.

(4) "BUFF" (bit D3 on address E2H) must be set to "0" (initial value). If it is "1", A/D conversion will not be done correctly.

4.13 VSS2 Booster

4.13.1 Configuration of VSS2 booster

The E0C62M2 has a built-in voltage booster that doubles the supply voltage (VDD–VSSD). This booster generates the boosted voltage VSS2 by connecting an external capacitor.
The boosted voltage VSS2 is used as the power source for the A/D converter, analog switch circuit and LCD driver. Therefore, turn the VSS2 booster ON before turning the A/D converter or LCD driver ON.
Figure 4.13.1.1 shows the configuration of the VSS2 booster.

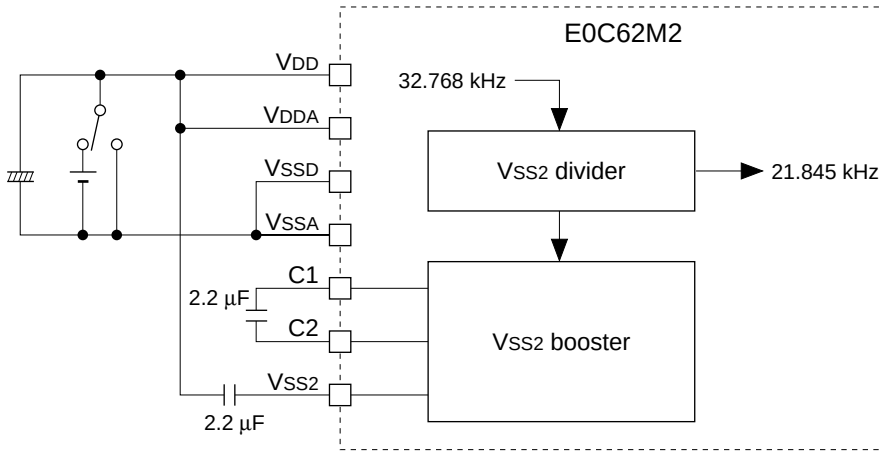


Fig. 4.13.1.1 VSS2 booster

The VSS2 booster uses the booster clock generated from the OSC1 oscillation clock (32.768 kHz) by dividing it by 1/3. Besides the VSS2 booster, this divided clock (21.845 kHz) is also used in the A/D converter and LCD driver.

4.13.2 Control of VSS2 booster

Table 4.13.2.1 lists the VSS2 booster's control bit and its address.

Table 4.13.2.1 Control bit of VSS2 booster

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
E0H	–	–	–	VSS2	–	– *3			Unused (Undefined when reading)
					–	– *3			Unused (Undefined when reading)
	R			R/W	–	– *3			Unused (Undefined when reading)
					VSS2	0	On	Off	VSS2 booster control

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

VSS2: VSS2 booster control (E0H•D0)
Turns the VSS2 booster ON and OFF.

When "1" is written: VSS2 booster ON
When "0" is written: VSS2 booster OFF
Reading: Valid

When "1" is written to the VSS2 register, the VSS2 booster starts operating and generates the boosted voltage VSS2. When "0" is written, the VSS2 booster goes OFF.
At initial reset and in SLEEP mode, this register is set to "0". When SLEEP mode is canceled, set this register again.
Be aware that the other bits (D1–D3) on the address E0H are undefined when they are read.

4.13.3 Programming notes

(1) The A/D converter and LCD driver use the boosted voltage VSS2. Therefore, turn the VSS2 booster ON before turning the A/D converter or LCD driver ON.
Further it is necessary to wait until the VSS2 voltage stabilizes after turning the VSS2 booster ON. Set at least 30 msec of wait time before turning the A/D converter or LCD driver ON after turning the VSS2 booster ON (VSS2 = "1").

(2) The bits other than VSS2 (D0) on the address E0H are undefined when reading. Take care when programming.

(3) When the CPU enters SLEEP status by the SLP instruction, the VSS2 booster is reset to the initial status.

4.14 SVD (Supply Voltage Detection) Circuit

4.14.1 Configuration of SVD circuit

The E0C62M2 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. Turning the SVD circuit ON/OFF can be controlled through the software.
Figure 4.14.1.1 shows the configuration of the SVD circuit.

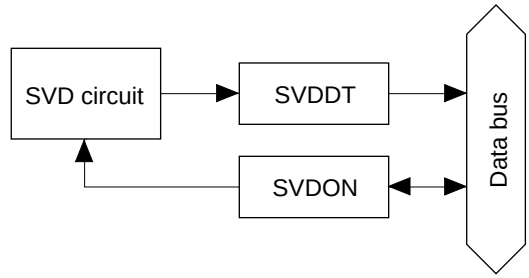


Fig. 4.14.1.1 Configuration of the SVD circuit

4.14.2 Operation of SVD circuit

The SVD circuit compares the criteria voltage set in the E0C62M2 and the supply voltage (V_{DD}–V_{SSD}) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage (V_{SVD}) has been set to 2.3 V.

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to the SVDDT register and SVD circuit goes OFF.
To obtain a stable SVD detection result, the SVD circuit must be on for at least l00 μsec. However, the E0C62M2 uses 32.768 kHz CPU system clock, the instruction cycles are long enough, so there is no need to worry about maintaining 100 μsec.
When SVD is on, the IC draws a large current, so keep SVD off unless it is.

4.14.3 Control of SVD circuit

Table 4.14.3.1 shows the control bits and the address for the SVD circuit.

Table 4.14.3.1 Control bits for SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
E3H	0	0	SVDDT	SVDON	0 *5	– *2			Unused
					0 *5	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	Supply voltage detection data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

SVDON: SVD circuit ON/OFF (E3H•D0)
Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When SVDON is set to "1", source voltage detection by the SVD circuit is executed. As soon as SVDON is reset to "0", the result is loaded to the SVDDT register.
At initial reset, this register is set to "0".

SVDDT: SVD data (E3H•D1)

This is the result of supply voltage detection.

When "0" is read:	Supply voltage ≥ Criteria voltage
When "1" is read:	Supply voltage < Criteria voltage
Writing:	Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this register.
At initial reset, SVDDT is set to "0".

4.14.4 Programming note

The SVD circuit should normally be turned OFF as the current consumption of the IC becomes large when it is ON. Turn the SVD circuit OFF when shifting to SLEEP mode in particular.

4.15 Interrupt and HALT/SLEEP

<Interrupt types>

The E0C62M2 provides the following interrupt settings, each of which is maskable.

External interrupt: •Input interrupt (2 systems)

Internal interrupt: •Timer interrupt (4 systems)
•Serial interface interrupt (1 system)
•A/D converter interrupt (1 system)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.
Figure 4.15.1 shows the configuration of the interrupt circuit.

<HALT and SLEEP>

The E0C62M2 has HALT and SLEEP functions that considerably reduce the current consumption when it is not necessary.

The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped. However, the oscillation circuit and timer operate. Reactivating the CPU from HALT status is done by generating an interrupt request. When it does not reactivate upon an interrupt request, the watchdog timer will cause it to restart from the initial reset status.

When shifted into SLEEP as the result of the SLP instruction, the operation of the CPU is stopped, the same as for HALT status, and timer also stops. However, the oscillation circuit operates.
Reactivation from SLEEP status can only be done by generation of K port input interrupt request. Consequently, when it shifts to SLEEP status, you must invariably set the input interrupt (K00–K03, K10–K13) to enable.
When SLEEP status is canceled by a K port input interrupt, the CPU starts operating.

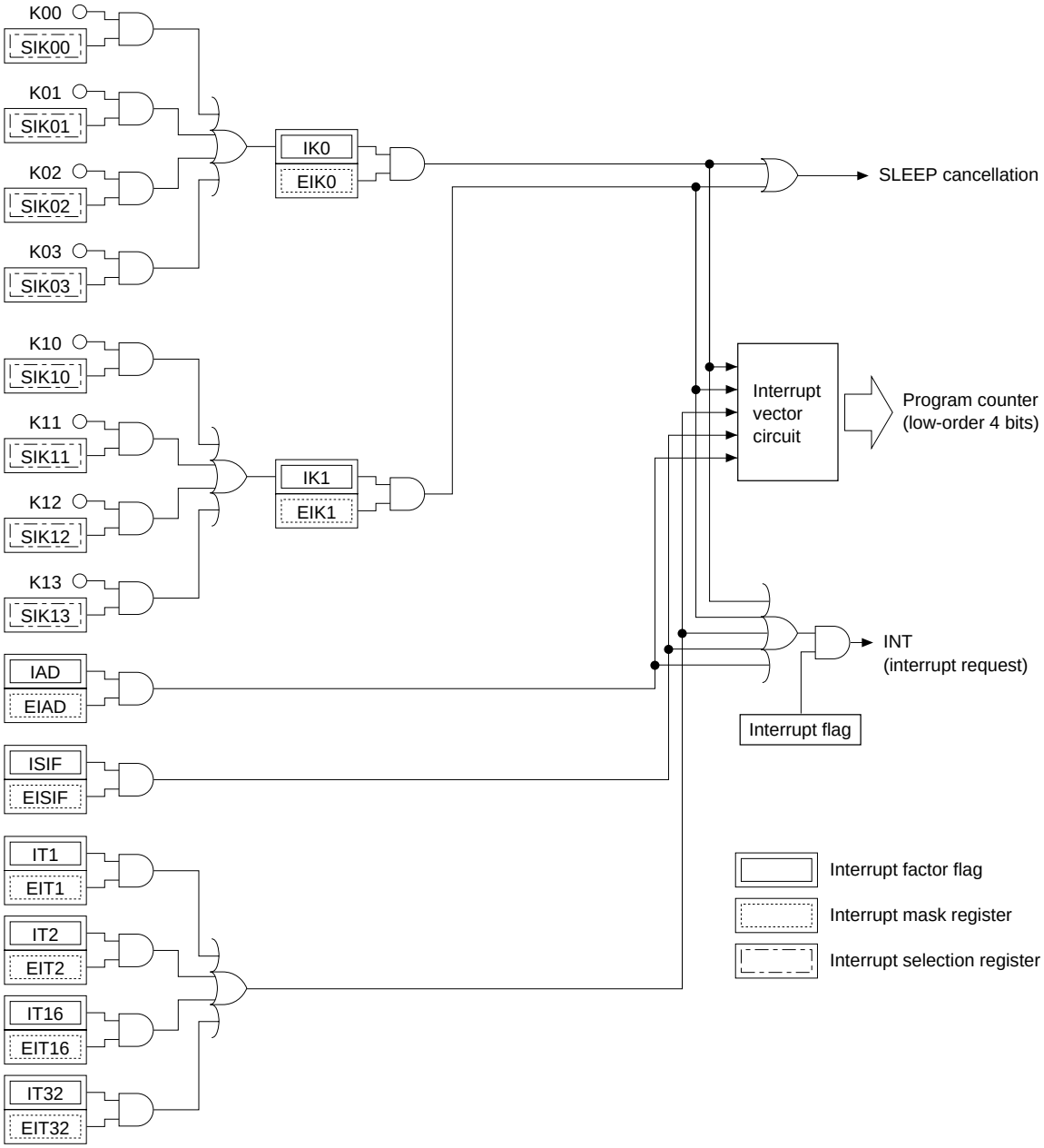


Fig. 4.15.1 Configuration of the interrupt circuit

4.15.1 Interrupt factor

Table 4.15.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when any of the conditions below set an interrupt factor flag to "1".

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is a read-only register, but can be reset to "0" when the register data is read out.
At initial reset, the interrupt factor flags are reset to "0".

Table 4.15.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Clock timer 1 Hz (falling edge)	IT1	(F5H•D3)
Clock timer 2 Hz (falling edge)	IT2	(F5H•D2)
Clock timer 16 Hz (falling edge)	IT16	(F5H•D1)
Clock timer 32 Hz (falling edge)	IT32	(F5H•D0)
K10–K13 input (rising edge)	IK1	(F2H•D0)
K00–K03 input (rising edge)	IK0	(F3H•D0)
Serial interface (8-bit data input/output has completed)	ISIF	(F4H•D0)
A/D converter (reverse integral has completed)	IAD	(F6H•D0)

Note: Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

4.15.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.15.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.15.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIT1	(F1H•D3)	IT1	(F5H•D3)
EIT2	(F1H•D2)	IT2	(F5H•D2)
EIT16	(F1H•D1)	IT16	(F5H•D1)
EIT32	(F1H•D0)	IT32	(F5H•D0)
EIK1	(F0H•D3)	IK1	(F2H•D0)
EIK0	(F0H•D2)	IK0	(F3H•D0)
EISIF	(F0H•D1)	ISIF	(F4H•D0)
EIAD	(F0H•D0)	IAD	(F6H•D0)

Note: Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

4.15.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

① The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

② The interrupt request causes the value of the interrupt vector (page 1, 02H–0AH) to be set in the program counter.

③ The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.15.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Note: The processing in ① and ② above take 12 cycles of the CPU system clock.

Table 4.15.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt request	Priority
102H	K10–K13 input	High
104H	K00–K03 input	↑
106H	Serial interface	
108H	Clock timer	↓
10AH	A/D converter	Low

When multiple interrupts simultaneously occur, processing is done from the high priority interrupt. The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.15.4 Control of interrupt

Tables 4.15.4.1 shows the interrupt control bits and their addresses.

Table 4.15.4.1 Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F0H	EIK1	EIK0	EISIF	EIAD	EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
					EISIF	0	Enable	Mask	Interrupt mask register (Serial interface)
	R/W				EIAD	0	Enable	Mask	Interrupt mask register (A/D converter)
F1H	EIT1	EIT2	EIT16	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT16	0	Enable	Mask	Interrupt mask register (Clock timer 16 Hz)
	R/W				EIT32	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
F2H	0	0	0	IK1	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F3H	0	0	0	IK0	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				IK0 *4	0	Yes	No	Interrupt factor flag (K00–K03)
F4H	0	0	0	ISIF	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				ISIF *4	0	Yes	No	Interrupt factor flag (Serial interface)
F5H	IT1	IT2	IT16	IT32	IT1 *4	0	Yes	No	Interrupt factor flag (Clock timer 1 Hz)
					IT2 *4	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
					IT16 *4	0	Yes	No	Interrupt factor flag (Clock timer 16 Hz)
	R				IT32 *4	0	Yes	No	Interrupt factor flag (Clock timer 32 Hz)
F6H	0	0	0	IAD	0 *5	– *2			Unused
					0 *5	– *2			Unused
					0 *5	– *2			Unused
	R				IAD *4	0	Yes	No	Interrupt factor flag (A/D converter)

*1 Initial value at the time of initial reset
*2 Not set in the circuit
*3 Undefined
*4 Resets (0) immediately after being read
*5 Constantly "0" when being read
*6 Refer to main manual

For control of the registers, see the following sections:

Section 4.4, "Input Port"
Section 4.9, "Clock Timer"
Section 4.10, "Serial Interface"
Section 4.11, "A/D Converter"

4.15.5 Programming notes

(1) When shifting to SLEEP status, at least either K00–K03 or K10–K13 interrupt must be set to enable canceling SLEEP status.

(2) In the E0C62M2, the OSC1 oscillation circuit keeps operating even in SLEEP status.

(3) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(4) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

(5) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(6) When the CPU enters SLEEP status, the following circuits are set to the initial status.

- Clock timer / Watchdog timer
- V_{SS2} booster
- LCD driver
- A/D converter

These circuits should be re-set after returning from SLEEP status.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C62M2 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following explains the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and Item)	Control register
CPU	SLP instruction, HALT instruction
V_{SS2} booster	VSS2
LCD driver	LPWR
A/D converter	ADON
SVD circuit	SVDON

See Chapter 7, "ELECTRICAL CHARACTERISTICS", for order of current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status
V_{SS2} booster: OFF status
LCD driver: OFF status
A/D converter: OFF status
SVD circuit: OFF status

When the CPU enters SLEEP status, the following circuits are set to the initial status.

- Clock timer/ Watchdog timer
- V_{SS2} booster
- LCD driver
- A/D converter

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these area.

Watchdog timer

The watchdog timer must be reset within 3-second cycles.

Oscillation circuit

In the E0C62M2, the OSC1 oscillation circuit does not stop even when the CPU enters SLEEP status. However, SLEEP stops supplying the clock to the peripheral circuits (timer and watchdog timer).

Input ports

When input ports are changed from high to low by pull down resistor, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull down resistance 300 kΩ

I/O ports

When in the input mode, I/O ports are changed from high to low by pull down resistor, the fall of the waveform is delayed on account of the time constant of the pull down resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 10 pF + parasitic capacitance ? pF
R: pull down resistance 300 kΩ

LCD driver

(1) The contents of the display memory are undefined until the area is initialized (through, for instance, memory clear processing by the CPU). Initialize the display memory by executing initial processing.

(2) Since the display memory area is write-only, display data cannot be rewritten by arithmetic operations (such as AND, OR, ADD, SUB).

(3) The power source for the LCD power generator (V_{L1}, V_{L2} and V_{L3} generation circuit) and the operating clock for the LCD drive timing generator are supplied from the V_{SS2} booster. Therefore, be sure to turn the V_{SS2} booster ON by setting the VSS2 register to "1" before turning the LCD driver ON (LPWR = "1").

(4) The control registers (LOFF, LDTY, LPWR) for the LCD driver are automatically set to the initial status when the CPU enters SLEEP status using the SLP instruction. Therefore, after returning from SLEEP status, set the registers' value again.
In SLEEP status, the V_{SS2} booster turns OFF.

Clock timer

(1) Be sure to read data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag reading (reset the flag) as necessary at reset.

(3) The clock timer is reset when the CPU enters SLEEP status by the SLP instruction.

(4) When the clock timer has been reset, the watchdog timer is also reset.

Serial interface

(1) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock SCLK is external clock, start to input the external clock after the trigger.

A/D converter

(1) Be sure to check whether the data is effective or invalid by reading the A/D conversion data in the order F7H → F8H → F9H → FAH and immediately thereafter reading the IDR.

(2) The interrupt factor flag may be set when the A/D conversion setting is changed (writing to E2H, E4H or E5H) or the CPU enters SLEEP status. Therefore, read (clear) the flag if necessary.

(3) The A/D converter is automatically set to the auto zero adjustment period when writing is done to the addresses E2H, E4H (function switching) and E5H (range switching). If the ADON register has been set to "1" (A/D converter is ON) at this time, the A/D conversion restarts with the new settings from the auto zero adjustment.

(4) The registers on the addresses E2H and E4H to EBH are set to initial status when the CPU enters SLEEP mode. Therefore, set the registers again when the CPU reactivates from SLEEP status.

Measurment circuit and measurment procedure

(1) The interrupt factor flag may be set when the A/D conversion setting is changed (writing to E2H, E4H or E5H) or the CPU enters SLEEP status. Therefore, read (clear) the flag if necessary.

(2) The A/D converter is automatically set to the auto zero adjustment period when writing is done to the addresses E2H, E4H (function switching) and E5H (range switching). If the ADON register has been set to "1" (A/D converter is ON) at this time, the A/D conversion restarts with the new settings from the auto zero adjustment.

(3) The registers on the addresses E2H and E4H to EBH are set to the initial status when the CPU enters SLEEP mode. Therefore, set the registers again when the CPU reactivates from SLEEP status.

V_{SS2} booster

(1) The A/D converter and LCD driver use the boosted voltage V_{SS2}. Therefore, turn the V_{SS2} booster ON before turning the A/D converter or LCD driver ON.
Further it is necessary to wait until the V_{SS2} voltage stabilizes after turning the V_{SS2} booster ON. Set at least 30 msec of wait time before turning the A/D converter or LCD driver ON after turning the V_{SS2} booster ON (VSS2 = "1").

(2) The bits other than VSS2 (D0) on the address E0H are undefined when reading. Take care when programming.

(3) When the CPU enters SLEEP status by the SLP instruction, the V_{SS2} booster is reset to the initial status.

SVD circuit

The SVD circuit should normally be turned OFF as the current consumption of the IC becomes large when it is ON. Turn the SVD circuit OFF when shifting to SLEEP mode in particular.

Interrupt and HALT/SLEEP

(1) When shifting to SLEEP status, at least either K00–K03 or K10–K13 interrupt must be set to enable canceling SLEEP status.

(2) In the E0C62M2, the OSC1 oscillation circuit keeps operating even in SLEEP status.

(3) The interrupt factor flags are set when the timing condition is established, even if the interrupt mask registers are set to "0".

(4) Write the interrupt mask register only in the DI status (interrupt flag = "0"). Writing during EI status (interrupt flag = "1") will cause malfunction.

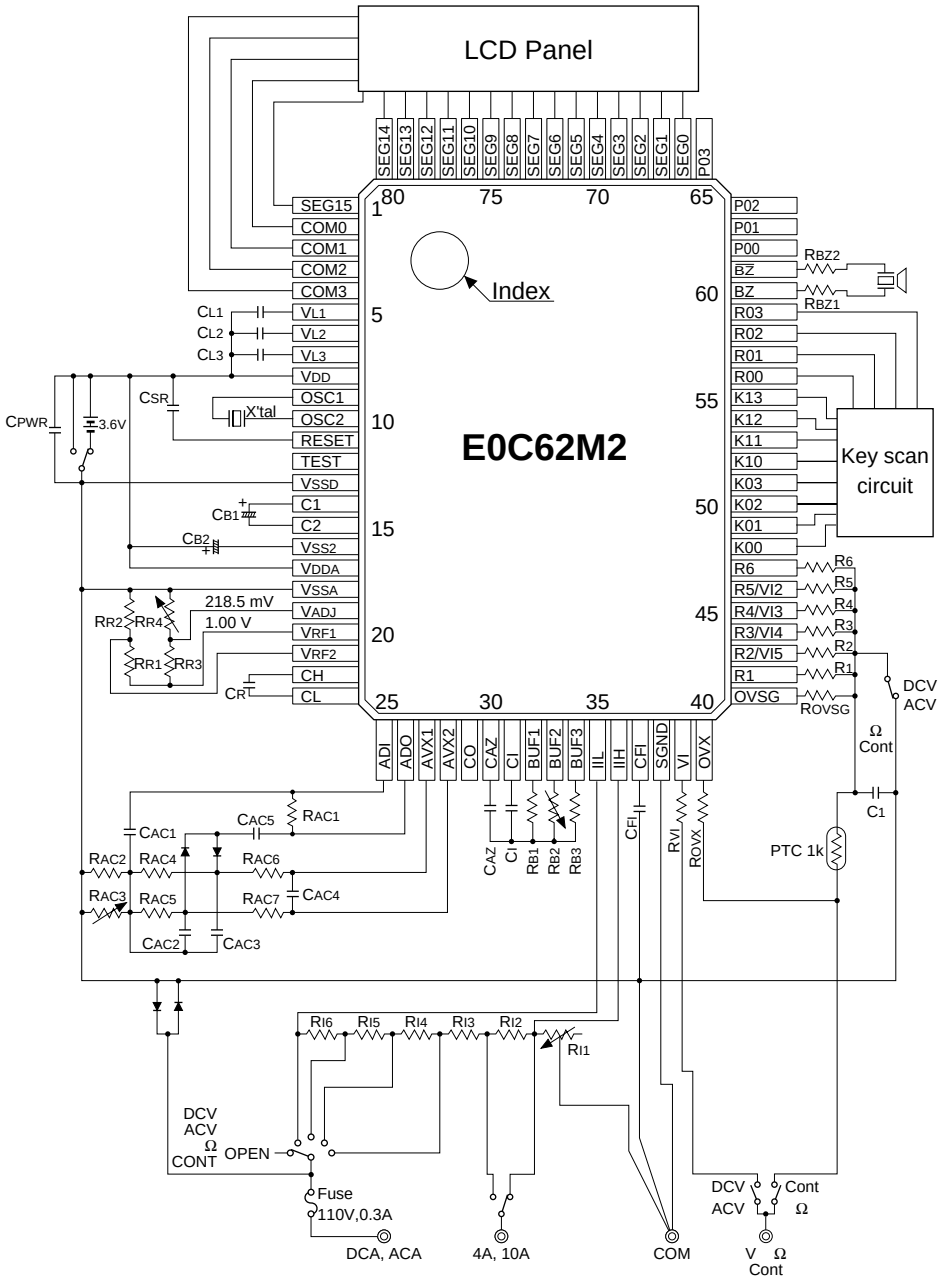
(5) Reading of interrupt factor flags is available at EI, but be careful in the following cases.
If the interrupt mask register value corresponding to the interrupt factor flags to be read is set to "1", an interrupt request will be generated by the interrupt factor flags set timing, or an interrupt request will not be generated. Be very careful when interrupt factor flags are in the same address.

(6) When the CPU enters SLEEP status, the following circuits are set to the initial status.

- Clock timer / Watchdog timer
- V_{SS2} booster
- LCD driver
- A/D converter

These circuits should be re-set after returning from SLEEP status.

CHAPTER 6 DIAGRAM OF BASIC EXTERNAL CONNECTIONS



Parts	Value	SR
C_{L1}	0.047 µF	
C_{L2}	0.047 µF	
C_{L3}	0.047 µF	
C_{SR}	0.33 µF	
C_{B1}	2.2 µF	
C_{B2}	2.2 µF	
C_R	0.22 µF	
C_{AC1}	0.1 µF	
C_{AC2}	2.2 µF	
C_{AC3}	2.2 µF	
C_{AC4}	0.22 µF	
C_{AC5}	0.1 µF	
C_{AZ}	0.1 µF	
C_1	0.1 µF	
C_{FI}	0.01 µF	
C_I	0.1 µF	
R_{R1}	82 kΩ	1.0 %
R_{R2}	22 kΩ	1.0 %
R_{R3}	120 kΩ	1.0 %
R_{R4}	75~412 kΩ	
R_{AC1}	22 MΩ	1.0 %
R_{AC2}	21 kΩ	1.0 %
R_{AC3}	500 kΩ	
R_{AC4}	22 kΩ	1.0 %
R_{AC5}	22 kΩ	1.0 %
R_{AC6}	330 kΩ	1.0 %
R_{AC7}	330 kΩ	1.0 %
R_{B1}	390 kΩ	0.1 %
R_{B2}	-329 kΩ	
R_{B3}	39 kΩ	0.1 %
R_{VI}	10 MΩ	0.1 %
R_{OVX}	1 MΩ	
R_{OVSG}	680 kΩ	
R_1	100 Ω	0.1 %
R_2	1 kΩ	0.1 %
R_3	10 kΩ	0.1 %
R_4	101 kΩ	0.1 %
R_5	1.11 MΩ	0.1 %
R_6	10 MΩ	0.1 %
R_{BZ1}	100 Ω	
R_{BZ2}	100 Ω	
R_{I1}	0.01 Ω	0.5 %
R_{I2}	0.09 Ω	0.5 %
R_{I3}	0.9 Ω	0.5 %
R_{I4}	9 Ω	0.5 %
R_{I5}	90 Ω	0.5 %
R_{I6}	900 Ω	0.5 %
PTC	1 kΩ	

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{DD}/V_{DDA} = 0 V)

Item		Symbol	Rated value	Unit
Power voltage		V_{DD}/V_{DDA}	0	V
		V_{SSD}/V_{SSA}	-3.5	V
		V_{SS2}	-7.0	V
Input voltage	V_{SSD} system	V_{I1}	(V_{SSD}/V_{SSA} - 0.3) to (V_{DD}/V_{DDA} + 0.3)	V
	V_{SS2} system	V_{I2}	(V_{SS2} - 0.3) to (V_{DD}/V_{DDA} + 0.3)	V
Permissible total output current *1		ΣI	10	mA
Operating temperature (1)		$Topr_1$	-20 to 70	°C
Operating temperature (2) *2		$Topr_2$	0 to 40	°C
Strage temperature		Tstg	-65 to 150	°C
Soldering temperature / time		Tsol	260°C, 10sec (lead section)	–
Permissible disspation *3		P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2 The A/D converter is ON status.

*3 In case of plastic package (QFP5-80pin, QFP14-80pin).

7.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{SSD}/V_{SSA}	V_{DD}/V_{DDA} = 0 V	-3.5	-3.0	-2.15	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz
Measurement system operating temperature	Tmes	During measurment by the A/D converter	15	25	35	°C

7.3 DC Characteristics

Unless otherwise specified:

V_{DD}/V_{DDA} = 0 V, V_{SSD}/V_{SSA} = -3.0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, $V_{L1}/V_{L2}/V_{L3}$ are internal voltage

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10–K13 RESET, TEST	0.1·V_{SSD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		P00–P03	0.1·V_{SSD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10–K13 RESET, TEST	V_{SSD}		0.9·V_{SSD}	V
Low level input voltage (2)	V_{IL2}		P00–P03	V_{SSD}		0.9·V_{SSD}	V
High level input current (1)	I_{IH1}	V_{IH1} = V_{DD} V_{SSD} = -3.0 V Without pull down resistor	K00–K03, K10–K13 P00–P03 RESET, TEST	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2} = V_{DD} V_{SSD} = -3.0 V With pull down resistor	K00–K03, K10–K13 P00–P03 RESET, TEST	5	10	20	µA
Low level input current	I_{IL}	V_{IL} = V_{SSD} = -3.0 V	K00–K03, K10–K13 P00–P03 RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1} = 0.1·V_{SSD} V_{SSD} = -3.0 V	R00–R03 P00–P03			-0.9	mA
High level output current (2)	I_{OH2}	V_{OH2} = 0.1·V_{SSD} V_{SSD} = -3.0 V	BZ, $\overline{BZ}$			-1.2	mA
Low level output current (1)	I_{OL1}	V_{OL1} = 0.9·V_{SSD} V_{SSD} = -3.0 V	R00–R03 P00–P03	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2} = 0.9·V_{SSD} V_{SSD} = -3.0 V	BZ, $\overline{BZ}$	3.5			mA
Common output current	I_{OH3}	V_{OH3} = V_{DD} - 0.05 V	COM0–COM3			-3.0	µA
	I_{OL3}	V_{OL3} = V_{L3} + 0.05 V		3.0			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4} = V_{DD} - 0.05 V	SEG0–SEG15			-3.0	µA
	I_{OL4}	V_{OL4} = V_{L3} + 0.05 V		3.0			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5} = 0.1·V_{SSD}	SEG0–SEG15			50	µA
	I_{OL5}	V_{OL5} = 0.9·V_{SSD}		-70			µA

7.4 Analog Characteristics and Current Consumption

Unless otherwise specified:

V_{DD}/V_{DDA} = 0 V, V_{SSD}/V_{SSA} = -3.0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, $V_{L1}/V_{L2}/V_{L3}$ are internal voltage

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect 1 MΩ load resistor between V_{DD} and V_{L1} C_{L1} = 0.047 µF	-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1 MΩ load resistor between V_{DD} and V_{L2} C_{L2} = 0.047 µF	-2.20	-2.10	-2.00	V
	V_{L3}	Connect 1 MΩ load resistor between V_{DD} and V_{L3} C_{L3} = 0.047 µF	-3.25	-3.15	-3.05	V
SVD voltage	V_{SVD}		-2.45	-2.30	-2.15	V
SVD circuit response time	t_{SVD}				100	µS
Power current consumption	I_{OP}	During SLEEP V_{SSD}/V_{SSA} = -3.0 V		1.5	4.0	µA
		During HALT V_{SSD}/V_{SSA} = -3.0 V		3.0	6.0	µA
		During A/D operation *1 V_{SSD}/V_{SSA} = -3.0 V		0.9	2.0	mA
		During A/D operation *2 V_{SSD}/V_{SSA} = -3.0 V		1.1	2.2	mA

*1 DCV and DCA measurement mode.

*2 ACV and ACA measurement mode. (The general AMP is ON status.)

A/D converter (Characteristics of A/D converter unit only)

Unless otherwise specified:

V_{DD}/V_{DDA} = 0 V, V_{SSD}/V_{SSA} = -3.0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, $V_{L1}/V_{L2}/V_{L3}$ are internal voltage

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Sampling time	St_1	A/D conversion in normal mode		100		mS
	St_2	A/D conversion in high speed mode		10		mS
Sampling rate	Sr_1	A/D conversion in normal mode		2.5		/S
	Sr_2	A/D conversion in high speed mode		10		/S
Linearity error	L_{IN}	A/D conversion in normal mode	-0.2		0.2	%FS
Polarity error	E_P	A/D conversion in normal mode	-2		+2	dgt
Zero point error	Z_{OFF}	A/D conversion in normal mode	-2		+2	dgt
Voltage range	V_{SSD}/V_{SSA}	$V_{DD} = V_{DDA}$ = 0 V	-3.5		V_{SVD} *1	V

*1 V_{SVD}: SVD judgment voltage

Reference voltage generator

Unless otherwise specified:

V_{DD}/V_{DDA} = 0 V, V_{SSD}/V_{SSA} = -3.0 V, f_{OSC1} = 32.768 kHz, Ta = 25°C, $V_{L1}/V_{L2}/V_{L3}$ are internal voltage

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Temperature characteristics	V_{refT}	0 to 40°C		-300	0	300	ppm/deg
Supply voltage characteristics	V_{refV}	V_{SSA} (V_{SSD}) = -2.15 to -3.5 V		-0.1		0.1	%
Reference voltage output	V_{ref1}	Short-circuit between V_{RF1} and V_{ADJ} terminals Voltage between V_{RF1} and V_{SSA} Connect 70 kΩ load resistor between V_{RF1} and V_{SSA}		400		780	mV
Output voltage during resistance measurement	Vrmes	V_{RF1} - V_{SSA} = 1.0 V (Output voltages are values in case of V_{SSA} standard)	400 Ω range		V_{DDA}		V
			4 kΩ range		0.7		V
			40 kΩ range		0.47		V
			400 kΩ range		0.47		V
			4 MΩ range		0.47		V
			40 MΩ range		0.47		V

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

Unless otherwise specified:

V_{DD}/V_{DDA} = 0 V, V_{SSD}/V_{SSA} = -3.0 V, Crystal: C-002R (CI = 35 kΩ), C_G = C_D = built-in, f_{OSC1} = 32.768 kHz, Ta = 25°C

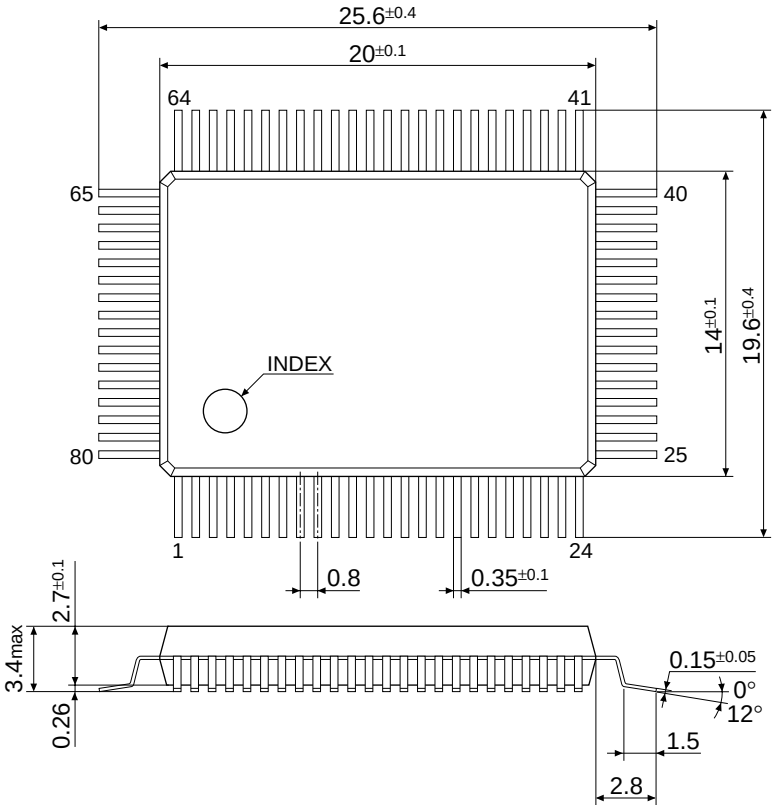
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta ≤ 3 sec			-2.15	V
Oscillation stop voltage	Vstp	tstp ≤ 10 sec			-1.8	V
Built-in capacitance (gate)	C_G			20		pF
Built-in capacitance (drain)	C_D			15		pF
Harmonic oscillation start voltage	V_{hho}				-3.5	V
Permitted leak resistance	R_{leak}		200			MΩ

CHAPTER 8 PACKAGE

8.1 Plastic Package

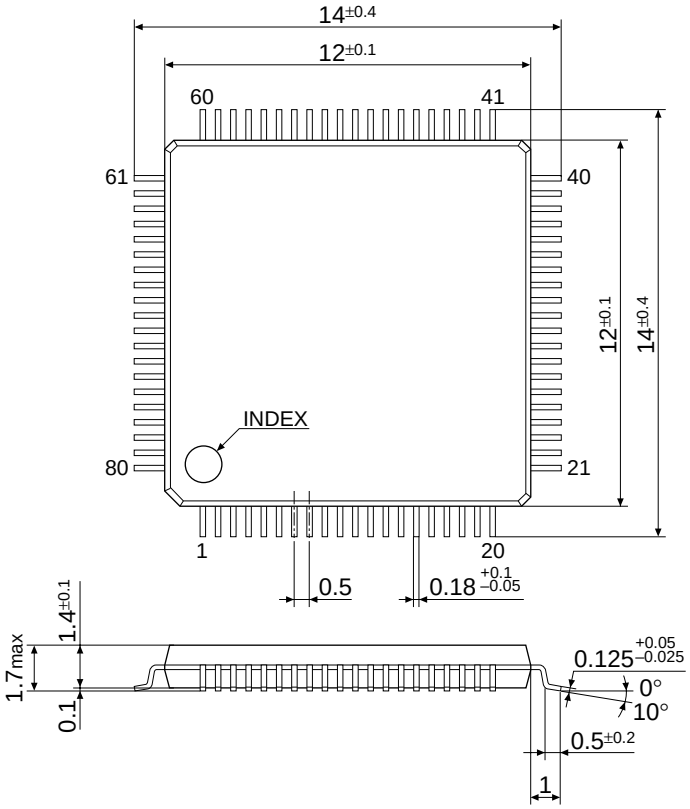
QFP5-80pin

(Unit: mm)



QFP14-80pin

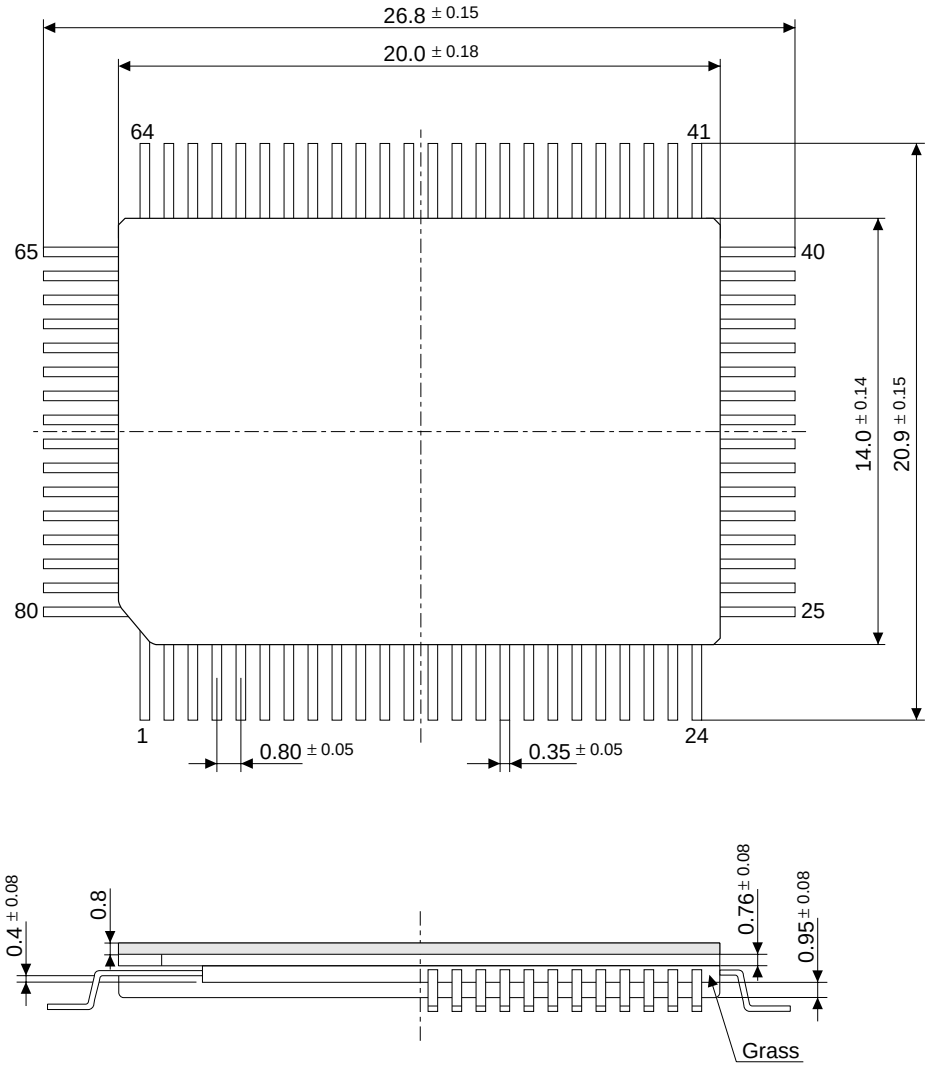
(Unit: mm)



8.2 Ceramic Package for Test Samples

QFP5-80pin

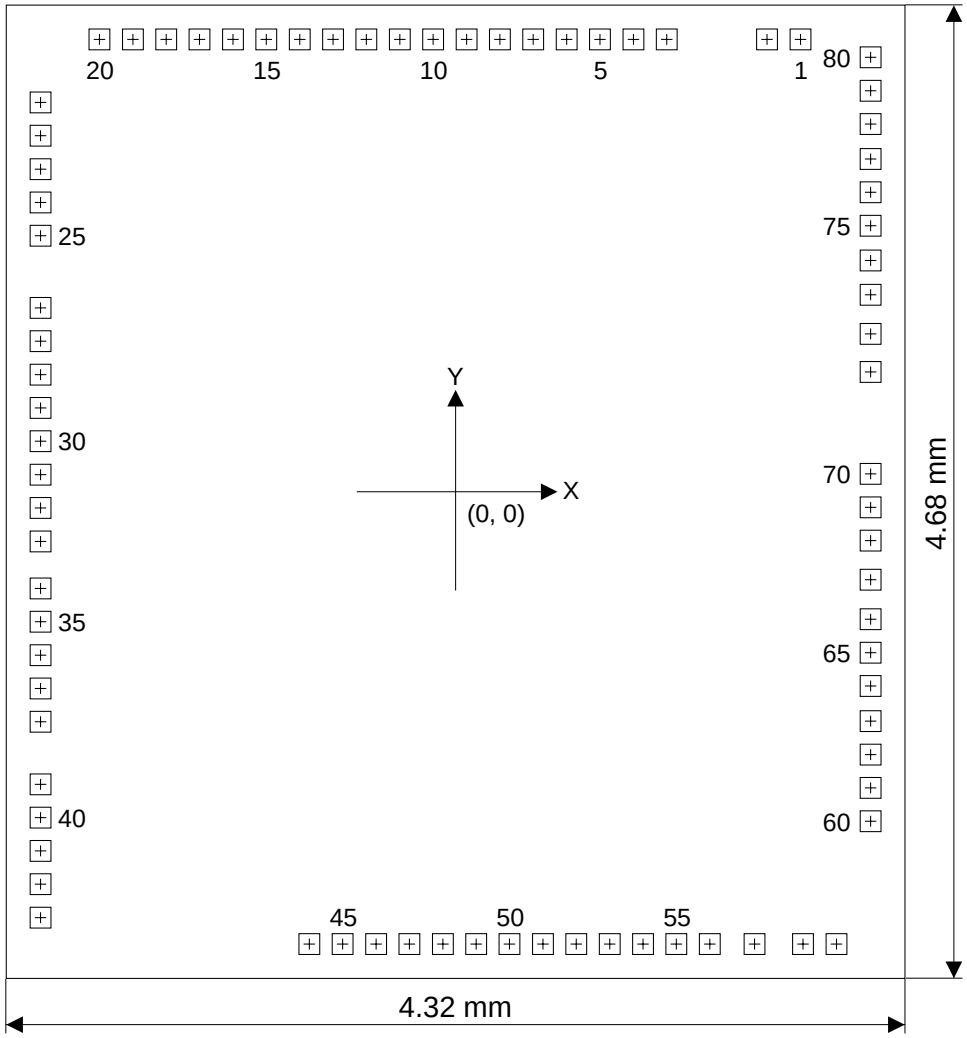
(Unit: mm)



Note: The QFP14-80pin ceramic package is not available for test samples.

CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

An N channel silicon wafer is used, therefore the potential of the back of the IC should be the same as the VDD when mounting the chip.

9.2 Pad Coordinates

(Unit: mm)

Pad		Coordinate		Pad		Coordinate	
No.	Name	X	Y	No.	Name	X	Y
1	CH	1.658	2.175	41	P01/SOUT	-1.995	-1.727
2	CL	1.497	2.175	42	P02/SCLK	-1.995	-1.887
3	ADI	1.015	2.175	43	P03/SRDY	-1.995	-2.048
4	ADO	0.855	2.175	44	SEG0	-0.703	-2.175
5	AVX1	0.694	2.175	45	SEG1	-0.543	-2.175
6	AVX2	0.534	2.175	46	SEG2	-0.382	-2.175
7	CO	0.373	2.175	47	SEG3	-0.222	-2.175
8	CAZ	0.213	2.175	48	SEG4	-0.061	-2.175
9	CI	0.053	2.175	49	SEG5	0.099	-2.175
10	BUF1	-0.108	2.175	50	SEG6	0.259	-2.175
11	BUF2	-0.268	2.175	51	SEG7	0.420	-2.175
12	BUF3	-0.429	2.175	52	SEG8	0.580	-2.175
13	IIL	-0.589	2.175	53	SEG9	0.741	-2.175
14	IIH	-0.749	2.175	54	SEG10	0.901	-2.175
15	CFI	-0.910	2.175	55	SEG11	1.061	-2.175
16	SGND	-1.070	2.175	56	SEG12	1.222	-2.175
17	VI	-1.231	2.175	57	SEG13	1.437	-2.175
18	OVX	-1.391	2.175	58	SEG14	1.670	-2.175
19	OVSG	-1.551	2.175	59	SEG15	1.831	-2.175
20	R1	-1.712	2.175	60	COM0	1.995	-1.585
21	R2/VI5	-1.995	1.872	61	COM1	1.995	-1.424
22	R3/VI4	-1.995	1.712	62	COM2	1.995	-1.264
23	R4/VI3	-1.995	1.551	63	COM3	1.995	-1.103
24	R5/VI2	-1.995	1.391	64	V_{L1}	1.995	-0.934
25	R6	-1.995	1.231	65	V_{L2}	1.995	-0.774
26	K00	-1.995	0.884	66	V_{L3}	1.995	-0.613
27	K01	-1.995	0.724	67	V_{DD}	1.995	-0.423
28	K02	-1.995	0.563	68	OSC1	1.995	-0.235
29	K03	-1.995	0.403	69	OSC2	1.995	-0.075
30	K10	-1.995	0.243	70	RESET	1.995	0.086
31	K11	-1.995	0.082	71	TEST	1.995	0.576
32	K12	-1.995	-0.078	72	V_{SSD}	1.995	0.759
33	K13	-1.995	-0.239	73	C1	1.995	0.947
34	R00	-1.995	-0.465	74	C2	1.995	1.112
35	R01	-1.995	-0.625	75	V_{SS2}	1.995	1.279
36	R02	-1.995	-0.786	76	V_{DDA}	1.995	1.440
37	R03	-1.995	-0.946	77	V_{SSA}	1.995	1.600
38	BZ	-1.995	-1.106	78	V_{ADJ}	1.995	1.768
39	$\overline{BZ}$	-1.995	-1.407	79	V_{RF1}	1.995	1.928
40	P00/SIN	-1.995	-1.567	80	V_{RF2}	1.995	2.089

REFERENCE DATA

This section presents an example of the DMM specification that can be realized by the E0C62M2. (Note that data does not guaranty the characteristics.)

1. Electrical Specification

Temperature: 18°C to 35°C (except for 40 MΩ range in resistance measurement)
Humidity: 80%
Operating voltage: (V_{DD}/V_{DDA}) - (V_{SSD}/V_{SSA}) = V_{SVD} to 3.5 [V]

Note: 1. Accuracy .... ± % of reading, ± number of least digits
2. This accuracy is an efficiency value for finished goods. (When reference resistors and other parts which have precision reading shown in Chapter 6, "DIAGRAM OF BASIC CONNECTIONS" are used.
3. V_{SVD} .... SVD judgment voltage

1.1 DC Voltmeter

Reading (Max. reading)	Resolution	Accuracy
399.9 mV	100 µV	± (0.5% + 1)
3.999 V	1 mV	± (0.8% + 1)
39.99 V	10 mV	± (0.8% + 1)
399.9 V	100 mV	± (0.8% + 1)
1000 V	1 V	± (0.8% + 1)

Input impedance: 10 MΩ
Precision for reference resistor: 0.1%
Response time: 2 seconds maximum

1.2 AC Voltmeter

Reading (Max. reading)	Resolution	Accuracy	Frequency (Hz)
399.9 mV	100 µV	± (1.5% + 3)	40–100
3.999 V	1 mV	± (1.2% + 3)	40–500
39.99 V	10 mV	± (1.2% + 3)	40–500
399.9 V	100 mV	± (1.2% + 3)	40–500
750 V	1 V	± (1.2% + 3)	40–500

Input impedance: 10 MΩ
Precision for reference resistor: 0.1%
Response time: 2 seconds maximum
AC-DC conversion rectification method: Mean value detection, effective value indication

1.3 DC Ammeter

Reading (Max. reading)	Resolution	Accuracy	Input resistor
399.9 µA	100 nA	± (1.0% + 2)	1 kΩ
3.999 mA	1 µA	± (1.0% + 2)	100 Ω
39.99 mA	10 µA	± (1.0% + 2)	10 Ω
399.9 mA	100 µA	± (1.0% + 2)	1 Ω
3.999 A	1 mA	± (1.5% + 2)	0.1 Ω
10.00 A	10 mA	± (1.5% + 2)	0.01 Ω

Maximum input current: 400 µA to 400 mA ... protected by fuse 0.5A
4 A, 10 A ..... Unfused
Precision for reference resistor: 0.5%

1.4 AC Ammeter

Reading (Max. reading)	Resolution	Accuracy	Input resistor
399.9 µA	100 nA	± (1.3% + 5)	1 kΩ
3.999 mA	1 µA	± (1.3% + 5)	100 Ω
39.99 mA	10 µA	± (1.3% + 5)	10 Ω
399.9 mA	100 µA	± (1.3% + 5)	1 Ω
3.999 A	1 mA	± (1.8% + 5)	0.1 Ω
10.00 A	10 mA	± (1.8% + 5)	0.01 Ω

Maximum input current: 400 µA to 400 mA ... protected by fuse 0.5A
4 A, 10 A ..... Unfused
Precision for reference resistor: 0.5%
AC-DC conversion rectification method: Mean value detection, effective value indication

1.5 Resistance

Reading (Max. reading)	Resolution	Accuracy	Measurement voltage / current
399.9 Ω	100 mΩ	± (0.7% + 2)	V_{DDA} 1.2 mA or less
3.999 kΩ	1 Ω	± (0.7% + 2)	0.7 V (TYP) 0.7 mA or less
39.99 kΩ	10 Ω	± (0.7% + 2)	0.47 V (TYP) 0.7 mA or less
399.9 kΩ	100 Ω	± (0.7% + 2)	0.47 V (TYP) 0.7 mA or less
3.999 MΩ	1 kΩ	± (1.0% + 2)	0.47 V (TYP) 0.7 mA or less
39.99 MΩ	10 kΩ	± (1.5% + 2)	0.47 V (TYP) 0.7 mA or less

Precision for reference resistor: 0.1%
Response time: 5 seconds maximum on 40 MΩ range
2 seconds maximum on all other ranges

Note: Temperature range for 40 MΩ is 18°C to 30°C.

1.6 Continuity check

Continuity check is done within the 400 Ω range or 4 kΩ range in the resistance measurement mode. Buzzer control during the continuity check is done by the hardware. The hardware judges continuity when the measured resistance is less than the threshold resistance for continuity sound generation, and generates continuity sound.

Reading (Max. reading)	Resolution	Continuity sound generation resistance	Release voltage
399.9 Ω	100 mΩ	50 Ω ± 30 Ω	V_{DDA}

Note: 50 Ω, 100 Ω, 500 Ω or 1 kΩ can be selected for the continuity sound generation resistance by the software.

2. Notes

The following shows the notes when using the E0C62M2 for DMM.

2.1 40 MΩ range during resistance measurement

When a resistance of about 40 MΩ is measured in the 40 MΩ range, the measurement error increases under the influence of the diode leak inside of the E0C62M2 if the temperature becomes high. Therefore, the measurable temperature range of the 40 MΩ range narrows on the high temperature side.

2.2 Frequency characteristic of AC voltage

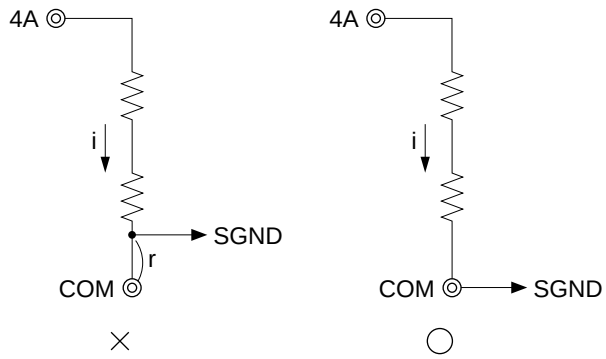
In the 400 mV range during AC voltage measurement, the frequency characteristic is 40 Hz to 100 Hz. The other ranges are 40 Hz to 500 Hz.

2.3 Reference voltage setting

The reference voltage should be set as follows: V_{RF1} = 1.0 V and V_{RF2} = 218.5 mV.
If the V_{RF1} voltage is too higher, measurement error increases during resistance measurement. If the V_{RF1} voltage is too low, measurement result does not stabilize during resistance measurement.
The V_{RF1} output voltage when the V_{RF1} terminal and V_{ADJ} terminal are shorted is 0.40 to 0.78 V.

2.4 Connection of SGND

The E0C62M2 uses the input from the SGND terminal as the GND level input to the A/D converter. The SGND terminal should be connected directly to the COM port of the DMM to increase the accuracy of A/D conversion. Measurement accuracy decreases if the COM port is connected to the SGND terminal via the line in which the large current flows, particularly during current measurement.



EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300 Fax: +1-310-955-5400

- SALES OFFICES -

West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630 Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600 Fax: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020 Fax: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Muenchen, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

- GERMANY -
SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)217-15045-0 Fax: +49-(0)217-15045-10

- UNITED KINGDOM -
UK BRANCH OFFICE
2.4 Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

- FRANCE -
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

ASIA

- CHINA -
EPSON (CHINA) CO., LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655 Fax: 64107320

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

- HONG KONG, CHINA -
EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

- TAIWAN, R.O.C. -
EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei, TAIWAN, R.O.C.
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN, R.O.C.
Phone: 03-573-9900 Fax: 03-573-9169

- SINGAPORE -
EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

- KOREA -
SEIKO EPSON CORPORATION KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

- JAPAN -
SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

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