

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER
E0C63466 TECHNICAL MANUAL

E0C63466 Technical Hardware



SEIKO EPSON CORPORATION

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CHAPTER 1 OUTLINE

The E0C63466 is a microcomputer which has a high-performance 4-bit CPU E0C63000 as the core CPU, ROM (16,384 words \times 13 bits), RAM (1,792 words \times 4 bits), serial interface, watchdog timer, programmable timer, time base counters (2 systems), SVD circuit, a dot-matrix LCD driver that can drive a maximum 60 segments \times 17 commons and sound generator built-in. The E0C63466 features high speed operation and low current consumption in a wide operating voltage range (2.2 V to 6.4 V), this makes it suitable for applications working with batteries. It is also suitable for LCD game because it has a large capacity of ROM built-in.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) crystal or 60 kHz (Typ.) CR oscillation circuit (*1)
OSC3 oscillation circuit	1.8 MHz (Typ.) CR or 4 MHz (Max.) ceramic oscillation circuit (*1)
Instruction set	Basic instruction: 46 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 μ sec 122 μ sec 183 μ sec During operation at 60 kHz: 33 μ sec 67 μ sec 100 μ sec During operation at 4 MHz: 0.5 μ sec 1 μ sec 1.5 μ sec
ROM capacity	Code ROM: 16,384 words \times 13 bits Data ROM: 2,048 words \times 4 bits (= 8K bits)
RAM capacity	Data memory: 1,792 words \times 4 bits Display memory: 1,020 bits (240 words \times 4 bits + 60 \times 1 bit)
Input port	8 bits (Pull-up resistors may be supplemented *1)
Output port	12 bits (It is possible to switch the 2 bits to special output *2)
I/O port	12 bits (It is possible to switch the 2 bits to special output and the 4 bits to serial I/F input/output *2)
Serial interface	1 port (8-bit clock synchronous system)
LCD driver	60 segments \times 8, 16 or 17 commons (*2)
Time base counter	2 systems (Clock timer, stopwatch timer)
Programmable timer	Built-in, 2 inputs \times 8 bits, with event counter function
Watchdog timer	Built-in
Sound generator	With envelope and 1-shot output functions
Supply voltage detection (SVD) circuit ..	16 values, programmable (1.85 V to 3.30 V) (It is possible to switch 1 value to the external voltage detection *1)
External interrupt	Input port interrupt: 2 systems
Internal interrupt	Clock timer interrupt: 4 systems Stopwatch timer interrupt: 2 systems Programmable timer interrupt: 2 systems Serial interface interrupt: 1 system
Power supply voltage	2.2 V to 6.4 V (Min. 1.8 V when the OSC3 oscillation circuit is not used)
Operating temperature range	-20°C to 70°C

Current consumption (Typ.)	Single clock (OSC1: Crystal oscillation):		
	During HALT (32 kHz)		
	3.0 V (LCD power OFF)		1 μ A
	3.0 V (LCD power ON, Vc1 standard)		6 μ A
	3.0 V (LCD power ON, Vc2 standard)		4 μ A
	During operation (32 kHz)		
	3.0 V (LCD power ON, Vc1 standard)		10 μ A
Twin clock:	During operation (4 MHz)		
	3.0 V (LCD power ON, Vc1 standard)		1,200 μ A
Package	QFP8-144pin, QFP17-144pin, QFP5-128pin (plastic) or chip		
	*1: Can be selected with mask option *2: Can be selected with software		

1.2 Block Diagram

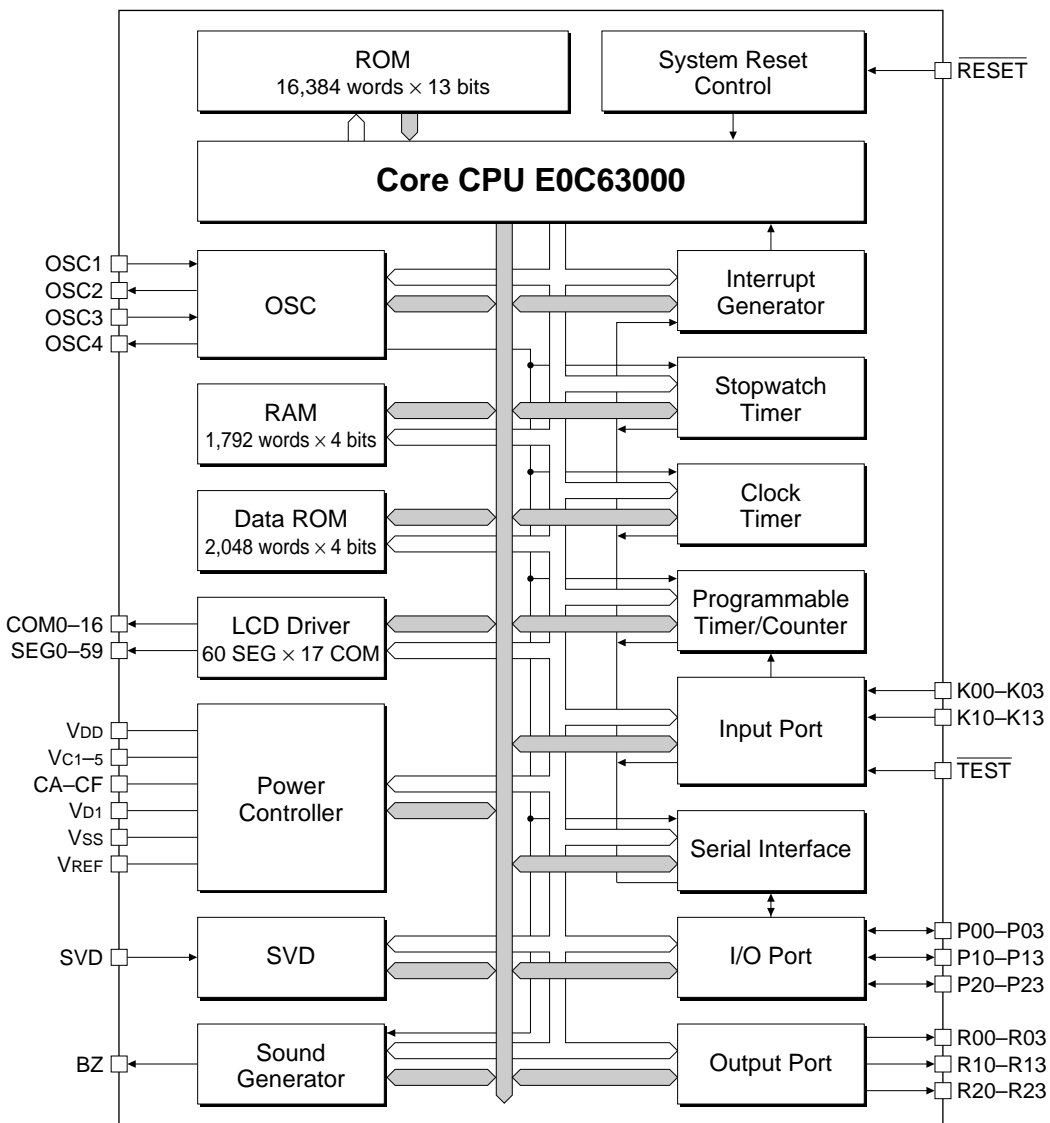
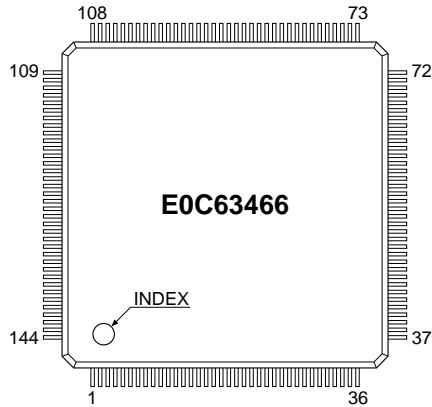


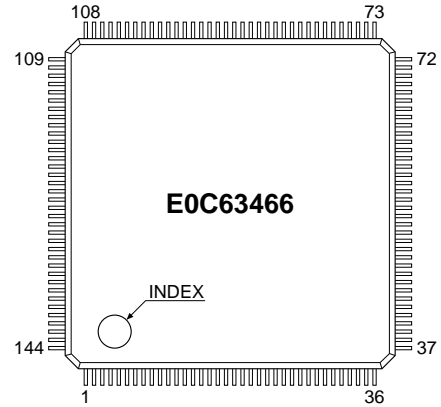
Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP8-144pin



QFP17-144pin



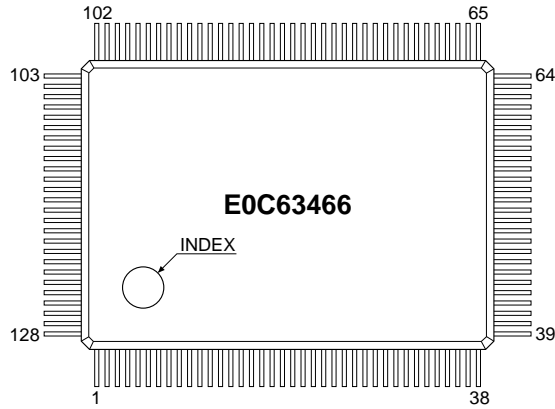
No.	Name	No.	Name	No.	Name	No.	Name
1	SEG13	37	N.C.	73	N.C.	109	N.C.
2	SEG12	38	N.C.	74	SVD	110	SEG47
3	SEG11	39	R23	75	Vc1	111	SEG46
4	SEG10	40	R22	76	Vc2	112	SEG45
5	SEG9	41	R21	77	Vc3	113	SEG44
6	SEG8	42	R20	78	Vc4	114	SEG43
7	SEG7	43	R13	79	Vc5	115	SEG42
8	SEG6	44	R12	80	CF	116	SEG41
9	SEG5	45	R11	81	CE	117	SEG40
10	SEG4	46	R10	82	CD	118	SEG39
11	SEG3	47	R03	83	CC	119	SEG38
12	SEG2	48	R02	84	CB	120	SEG37
13	SEG1	49	R01	85	CA	121	SEG36
14	SEG0	50	R00	86	COM8	122	SEG35
15	COM7	51	P23	87	COM9	123	SEG34
16	COM6	52	P22	88	COM10	124	SEG33
17	COM5	53	P21	89	COM11	125	SEG32
18	COM4	54	P20	90	COM12	126	SEG31
19	N.C.	55	P13	91	COM13	127	SEG30
20	COM3	56	P12	92	COM14	128	SEG29
21	COM2	57	P11	93	COM15	129	SEG28
22	COM1	58	P10	94	COM16	130	SEG27
23	COM0	59	P03	95	SEG59	131	SEG26
24	BZ	60	P02	96	SEG58	132	SEG25
25	Vss	61	P01	97	SEG57	133	SEG24
26	OSC1	62	P00	98	SEG56	134	SEG23
27	OSC2	63	K13	99	SEG55	135	SEG22
28	Vd1	64	K12	100	SEG54	136	SEG21
29	OSC3	65	K11	101	SEG53	137	SEG20
30	OSC4	66	K10	102	SEG52	138	SEG19
31	VDD	67	K03	103	SEG51	139	SEG18
32	RESET	68	K02	104	SEG50	140	SEG17
33	TEST	69	K01	105	SEG49	141	SEG16
34	VREF	70	K00	106	SEG48	142	SEG15
35	N.C.	71	N.C.	107	N.C.	143	SEG14
36	N.C.	72	N.C.	108	N.C.	144	N.C.

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram

Note: The pin layout diagram of the both package is same.

QFP5-128pin



No.	Name	No.	Name	No.	Name	No.	Name
1	SEG49	33	SEG17	65	RESET	97	K02
2	SEG48	34	SEG16	66	TEST	98	K01
3	SEG47	35	SEG15	67	VREF	99	K00
4	SEG46	36	SEG14	68	N.C.	100	SVD
5	SEG45	37	SEG13	69	R23	101	VC1
6	SEG44	38	SEG12	70	R22	102	VC2
7	SEG43	39	SEG11	71	R21	103	VC3
8	SEG42	40	SEG10	72	R20	104	VC4
9	SEG41	41	SEG9	73	R13	105	VC5
10	SEG40	42	SEG8	74	R12	106	CF
11	SEG39	43	SEG7	75	R11	107	CE
12	SEG38	44	SEG6	76	R10	108	CD
13	SEG37	45	SEG5	77	R03	109	CC
14	SEG36	46	SEG4	78	R02	110	CB
15	SEG35	47	SEG3	79	R01	111	CA
16	SEG34	48	SEG2	80	R00	112	COM8
17	SEG33	49	SEG1	81	P23	113	COM9
18	SEG32	50	SEG0	82	P22	114	COM10
19	SEG31	51	COM7	83	P21	115	COM11
20	SEG30	52	COM6	84	P20	116	COM12
21	SEG29	53	COM5	85	P13	117	COM13
22	SEG28	54	COM4	86	P12	118	COM14
23	SEG27	55	COM3	87	P11	119	SEG59
24	SEG26	56	COM2	88	P10	120	SEG58
25	SEG25	57	BZ	89	P03	121	SEG57
26	SEG24	58	Vss	90	P02	122	SEG56
27	SEG23	59	OSC1	91	P01	123	SEG55
28	SEG22	60	OSC2	92	P00	124	SEG54
29	SEG21	61	VD1	93	K13	125	SEG53
30	SEG20	62	OSC3	94	K11	126	SEG52
31	SEG19	63	OSC4	95	K10	127	SEG51
32	SEG18	64	VDD	96	K03	128	SEG50

N.C. : No Connection

Fig. 1.3.2 Pin layout diagram

Note: This package does not have the K12 terminal. For the K12 mask option, "With pull-up resistor" should be chosen when using this package.

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.		In/Out	Function
	QFP8-144,QFP17-144	QFP5-128		
VDD	31	64	–	Power (+) supply pin
VSS	25	58	–	Power (–) supply pin
VDI	28	61	–	Oscillation/internal logic system regulated voltage output pin
VC1–VC5	75–79	101–105	–	LCD system power supply pin 1/4 bias generated internally, 1/5 bias supplied externally (selected by mask option)
VREF	34	67	O	LCD system power supply testing pin
CA–CF	85–80	111–106	–	LCD system boosting/reducing capacitor connecting pin
OSC1	26	59	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	27	60	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	29	62	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	30	63	O	Ceramic or CR oscillation output pin (selected by mask option)
K00–K03	70–67	99–96	I	Input port
K10, K11	66,65	95,94	I	Input port
K12	64	–	I	Input port
K13	63	93	I	Input port
P00–P03	62–59	92–89	I/O	I/O port
P10–P13	58–55	88–85	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20	54	84	I/O	I/O port
P21	53	83	I/O	I/O port
P22	52	82	I/O	I/O port (switching to CL signal output is possible by software)
P23	51	81	I/O	I/O port (switching to FR signal output is possible by software)
R00	50	80	O	Output port
R01	49	79	O	Output port
R02	48	78	O	Output port (switching to TOUT signal output is possible by software)
R03	47	77	O	Output port (switching to FOUT signal output is possible by software)
R10–R13	46–43	76–73	O	Output port
R20–R23	42–39	72–69	O	Output port
COM0, COM1	23,22	–	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
COM2–COM14	21,20,18–15,86–92	56–51,112–118		
COM15, COM16	93,94	–		
SEG0–SEG59	14–1,143–110,106–95	50–1,128–119	O	LCD segment output pin
BZ	24	57	O	Sound output pin
SVD	74	100	I	SVD external voltage input pin
RESET	32	65	I	Initial reset input pin
TEST	33	66	I	Testing input pin

1.5 Mask Option

Mask options shown below are provided for the E0C63466. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator FOG63466, that has been prepared as the development software tool of E0C63466, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the FOG63466. Refer to the "E0C63466 Development Tool Manual" for the FOG63466.

<Functions selectable with E0C63466 mask options>

(1) *External reset by simultaneous LOW input to the input port (K00–K03)*

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(2) *Time authorize circuit for the simultaneous LOW input reset function*

When using the external reset function (shown in 1 above), using the time authorize circuit or not can be selected by the mask option. The reset function works only when the input time of simultaneous LOW is more than the rule time if the time authorize circuit is being used. Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(3) *Input port pull-up resistor*

The mask option is used to select whether the pull-up resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports. When using the QFP5-128pin package, "With pull-up resistor" option should be chosen for the K12 input port. Refer to Section 4.4.3, "Mask option", for details.

(4) *Output specification of the output port*

Either complementary output or N-channel open drain output can be selected as the output specification for the output ports R10–R13 and R20–R23. The selection is done in 4-bit units (R10–R13 and R20–R23). The output ports R00–R03 can only be used as complementary output. Refer to Section 4.5.2, "Mask option", for details.

(5) *Output specification / pull-up resistor of the I/O ports*

Either complementary output or N-channel open drain output can be selected as the output specification when the P10–P13 and P20–P23 are in the output mode. The selection is done in 1-bit units or 4-bit units depending on the I/O port.

1-bit unit: P20, P21, P22, P23

4-bit unit: P10–P13

Note that the P00–P03 can only be used as complementary output.

Further, whether or not the pull-up resistors working in the input mode are supplemented can be selected. The selection is done in 1-bit units or 4-bit units depending on the I/O port.

1-bit unit: P20, P21, P22, P23

4-bit unit: P10–P13

Refer to Section 4.6.2, "Mask option", for details.

(6) *LCD drive bias*

Either the internal power supply (1/4 bias) or an external power supply (1/5 bias) can be selected as the LCD system power supply.

Refer to Section 4.7.3, "Mask option", for details.

(7) Synchronous clock polarity in the serial interface

The polarity of the synchronous clock SCLK and the $\overline{\text{SRDY}}$ signal in slave mode of the serial interface is selected by the mask option. Either positive polarity or negative polarity can be selected. Refer to Section 4.11.2, "Mask option", for details.

(8) Buzzer output specification of the sound generator

It is possible to select the polarity of the buzzer signal output from the BZ terminal. Select either positive polarity or negative polarity according to the external drive transistor to be used. Refer to Section 4.12.2, "Mask option", for details.

(9) External voltage detection of SVD circuit

External voltage (SVD terminal–V_{SS} terminal) detection can be selected in addition to supply voltage (V_{DD} terminal–V_{SS} terminal) detection. The SVD terminal is used to input the external voltage to be detected.

Refer to Section 4.13.2, "Mask option", for details.

(10) OSC1 oscillation circuit

Either crystal oscillation circuit or CR oscillation circuit can be selected as the OSC1 oscillation circuit. Refer to Section 4.3.2, "OSC1 oscillation circuit", for details.

(11) OSC3 oscillation circuit

Either CR oscillation circuit or ceramic oscillation circuit can be selected as the OSC3 oscillation circuit. Refer to Section 4.3.3, "OSC3 oscillation circuit", for details.

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The E0C63466 operating power voltage is as follows:

Table 2.1.1 Operating power voltage

OSC1 oscillation circuit	OSC3 oscillation circuit	Operating power voltage
Crystal oscillation	Not use	1.8 V–6.4 V
Crystal oscillation	Use	2.2 V–6.4 V
CR oscillation	–	2.2 V–6.4 V

The E0C63466 operates by applying a single power supply within the above range between VDD and VSS. The E0C63466 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.2.

Table 2.1.2 Power supply circuits

Circuit	Power supply circuit	Output voltage
Oscillation and internal circuits	Oscillation system voltage regulator	VD1
LCD driver	LCD system voltage circuit	VC1–VC5

- Note:
- Do not drive external loads with the output voltage from the internal power supply circuits.
 - Vc3 should be used only when the LCD drive voltage is supplied externally (1/5 bias); when using the internal LCD system voltage circuit (1/4 bias), short between Vc3 and Vc2 terminals.
 - See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.

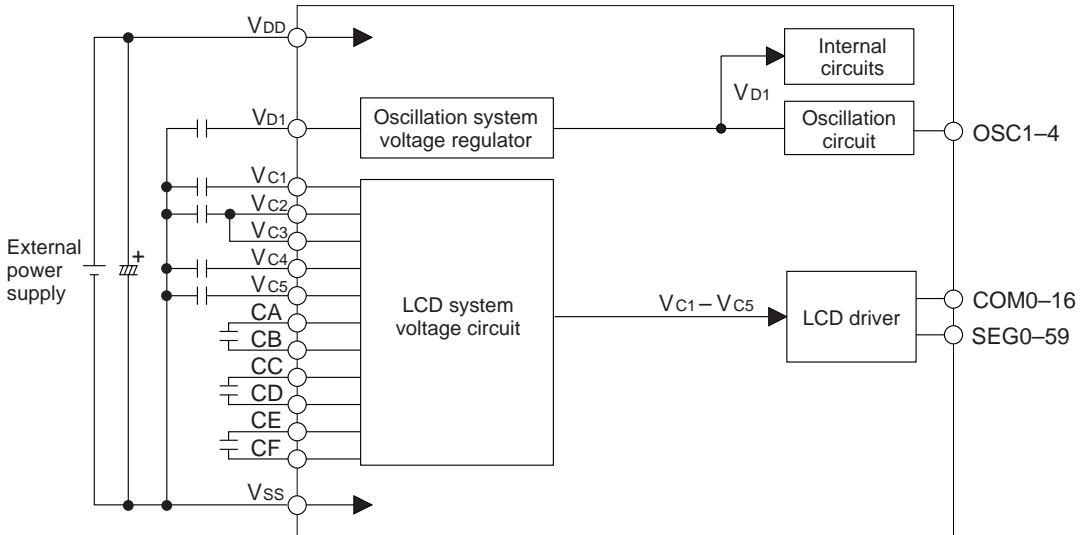


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <VD1> for oscillation circuit and internal circuits

VD1 is a voltage for the oscillation circuit and the internal logic circuits, and is generated by the oscillation system voltage regulator for stabilizing the oscillation.

The E0C63466 is designed with twin clock specification; it has two types of oscillation circuits OSC1 and OSC3 built-in. Use OSC1 clock for normal operation, and switch it to OSC3 by the software when high-speed operation is necessary. When switching the clock, the operating voltage VD1 must be switched by the software to stabilize the operation of the oscillation circuit and internal circuits.

The oscillation system voltage regulator can output the following two types of VD1 voltage. It should be set at the value according to the oscillation circuit and oscillation frequency by the software.

Single clock operation (OSC1 crystal oscillation):	VD1 = 1.3 V
Single clock operation (OSC1 CR oscillation):	VD1 = 2.2 V
Twin clock operation (OSC3, 4 MHz):	VD1 = 2.2 V

Refer to Section 4.3, "Oscillation Circuit", for the VD1 switching procedure.

However, since the VD1 voltage value is fixed at 2.2 V when the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, it is not necessary to switch VD1 by software.

2.1.2 Voltage <VC1–VC5> for LCD driving

VC1–VC5 are the LCD drive voltages for which either the voltage generated by the LCD system voltage circuit or voltage to be supplied from outside can be used. The built-in LCD system voltage circuit generates four voltages (1/4 bias) VC1, VC2, VC4 and VC5 (excluding VC3). These four output voltages can only be supplied to the externally expanded LCD driver.

When external voltages are supplied, 1/5 bias driving can be done by inputting drive voltage to the VC1–VC5 terminals (including VC3).

Either the internal generated voltages or external voltages used for the LCD drive voltage can be selected by a mask option.

The LCD system voltage circuit generates VC1 or VC2 with the voltage regulator built-in, and generates three other voltages by boosting or reducing the voltage of VC1 or VC2. Table 2.1.2.1 shows the VC1, VC2, VC4 and VC5 voltage values and boost/reduce status.

Table 2.1.2.1 LCD drive voltage when generated internally

LCD drive voltage	VDD = 1.8–6.4 V	VDD = 2.6–6.4 V
VC1 (0.975–1.2 V)	VC1 (standard)	1/2 × VC2
VC2 (1.950–2.4 V)	2 × VC1	VC2 (standard)
VC4 (2.925–3.6 V)	3 × VC1	3/2 × VC2
VC5 (3.900–4.8 V)	4 × VC1	2 × VC2

Note: The LCD drive voltage can be adjusted by the software (see Section 4.7.6). Values in the above table are typical values.

Either the VC1 or VC2 used for the standard is selected according to the supply voltage by the software. The VC2 standard improves the display quality and reduces current consumption, however, the power supply voltage VDD must be 2.6 V or more.

Refer to Section 4.7, "LCD Driver", for control of the LCD drive voltage.

2.2 Initial Reset

To initialize the E0C63466 circuits, initial reset must be executed. There are two ways of doing this.

- (1) External initial reset by the $\overline{\text{RESET}}$ terminal
- (2) External initial reset by simultaneous low input to terminals K00–K03 (mask option setting)

The circuits are initialized by either (1) or (2). When the power is turned on, be sure to initialize using the reset function. It is not guaranteed that the circuits are initialized by only turning the power on.

Figure 2.2.1 shows the configuration of the initial reset circuit.

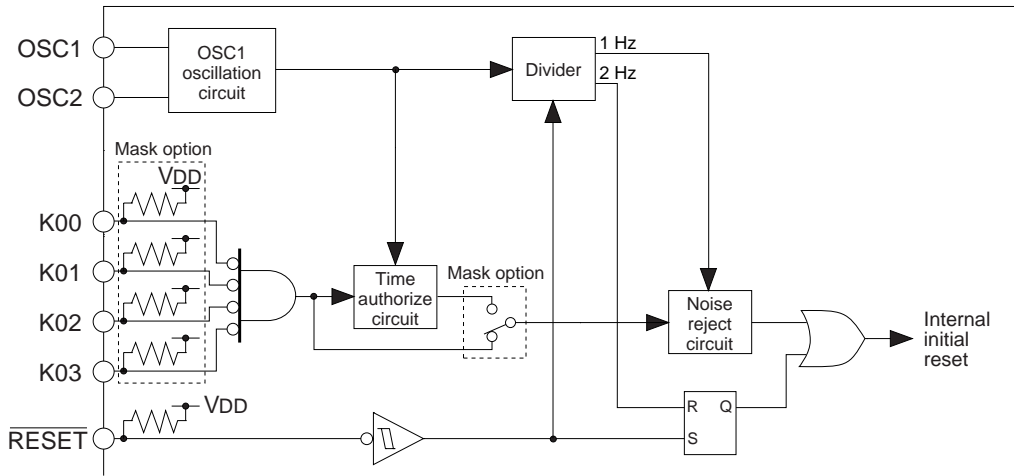


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal ($\overline{\text{RESET}}$)

Initial reset can be executed externally by setting the reset terminal to a low level (V_{SS}). After that the initial reset is released by setting the reset terminal to a high level (V_{DD}) and the CPU starts operation. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when $f_{OSC1} = 32.768 \text{ kHz}$) is needed until the internal initial reset is released after the reset terminal goes to high level. Be sure to maintain a reset input of 0.1 msec or more.

However, when turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 2.2.1.1.

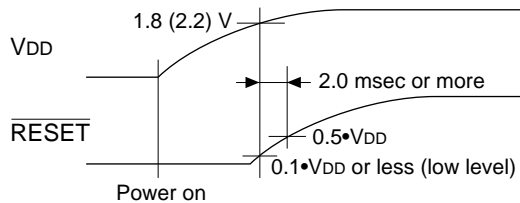


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to $0.1 \cdot V_{DD}$ or less (low level) until the supply voltage becomes 1.8 V or more (until the supply voltage becomes 2.2 V or more when the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option).

After that, a level of $0.5 \cdot V_{DD}$ or less should be maintained more than 2.0 msec.

2.2.2 Simultaneous low input to terminals K00–K03

Another way of executing initial reset externally is to input a low signal simultaneously to the input ports (K00–K03) selected with the mask option.

Since this initial reset passes through the noise reject circuit, maintain the specified input port terminals at low level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) during normal operation. The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input port terminals at low level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) after oscillation starts.

Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00*K01*K02*K03
3	K00*K01*K02
4	K00*K01

When, for instance, mask option 2 (K00*K01*K02*K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. When 3 or 4 is selected, the initial reset is done when a key entry including a combination of selected input ports is made.

Further, the time authorize circuit can be selected with the mask option. The time authorize circuit checks the input time of the simultaneous low input and performs initial reset if that time is the defined time (1 to 2 sec) or more.

If using this function, make sure that the specified ports do not go low at the same time during ordinary operation.

2.2.3 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.3.1.

The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.

In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.

When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.

Refer to the "E0C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.3.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other peripheral circuits	–	*

* See Section 4.1, "Memory Map".

2.2.4 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.

Table 2.2.4.1 shows the list of the shared terminal settings.

Table 2.2.4.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output				Serial I/F	
		TOUT	FOUT	CL	FR	Master	Slave
R00	R00 (High output)						
R01	R01 (High output)						
R02	R02 (High output)	TOUT					
R03	R03 (High output)		FOUT				
R10–R13	R10–R13 (High output)						
R20–R23	R20–R23 (High output)						
P00–P03	P00–P03 (Input & Pull-up *)						
P10	P10 (Input & Pull-up *)					SIN(I)	SIN(I)
P11	P11 (Input & Pull-up *)					SOUT(O)	SOUT(O)
P12	P12 (Input & Pull-up *)					SCLK(O)	SCLK(I)
P13	P13 (Input & Pull-up *)						SRDY(O)
P20	P20 (Input & Pull-up *)						
P21	P21 (Input & Pull-up *)						
P22	P22 (Input & Pull-up *)			CL			
P23	P23 (Input & Pull-up *)				FR		

* When "with pull-up" is selected by mask option (high impedance when "gate direct" is selected)

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal (TEST)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the TEST terminal to VDD.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The E0C63466 has a 4-bit core CPU E0C63000 built-in as its CPU part. Refer to the "E0C63000 Core CPU Manual" for the E0C63000.

Note: The SLP instruction cannot be used because the SLEEP operation is not assumed in the E0C63466.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 16,384 steps \times 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the E0C63466 is step 0000H to step 3FFFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0104H–010EH, respectively.

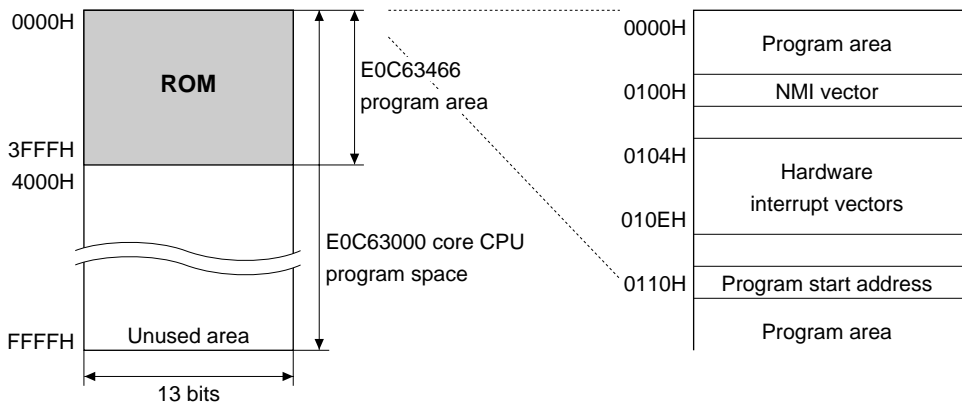


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 1,792 words \times 4 bits. The RAM area is assigned to addresses 0000H to 06FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit/16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

- (1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.
- (2) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the E0C63466 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

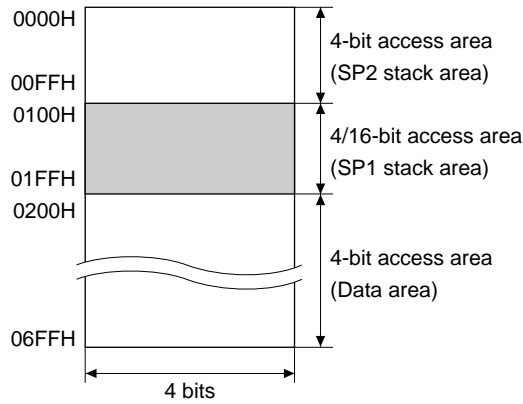


Fig. 3.3.1 Configuration of data RAM

3.4 Data ROM

The data ROM is a mask ROM for loading various static data such as a character generator, and has a capacity of 2,048 words \times 4 bits. The data ROM is assigned to addresses 8000H to 87FFH on the data memory map, and the data can be read using the same data memory access instructions as the RAM.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of E0C63466 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The E0C63466 data memory consists of 1,792-word RAM, 2,048-word data ROM, 1,020-bit display memory and 67-word peripheral I/O memory. Figure 4.1.1 shows the overall memory map of the E0C63466, and Tables 4.1.1(a)–(e) the peripheral circuits' (I/O space) memory maps.

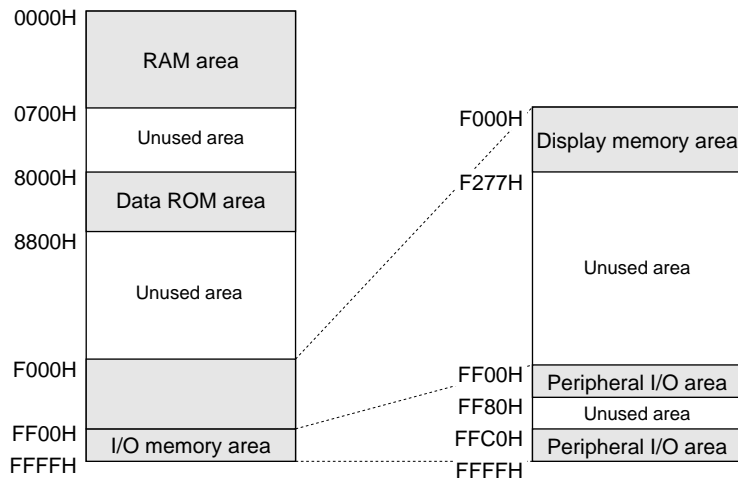


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the display memory area and the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to Section 4.7.5, "Display memory", for the display memory, and the I/O memory maps shown in Tables 4.1.1 (a)–(e) for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF00H–FF31H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch OSC3 oscillation On/Off Unused CPU operating voltage switch (1.3 V: OSC1, 2.2 V: OSC3)
					OSCC	0	On	Off	
	R/W		R	R/W	0 *3	- *2			
					VDC	0	2.2 V	1.3 V	
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting [SVDS3-0] 0 1 2 3 4 5 6 7 Voltage(V) 1.85/1.05 1.90 2.00 2.10 2.20 2.30 2.40 2.50 [SVDS3-0] 8 9 10 11 12 13 14 15 Voltage(V) 2.60 2.70 2.80 2.90 3.00 3.10 3.20 3.30
					SVDS2	0			
	R/W				SVDS1	0			
					SVDS0	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	- *2			Unused Unused SVD evaluation data SVD circuit On/Off
					0 *3	- *2			
	R			R/W	SVDDT	0	Low	Normal	
					SVDON	0	On	Off	
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable Unused FOUT frequency selection [FOFQ1, 0] 0 1 2 3 Frequency fosc1/64 fosc1/8 fosc1 fosc3
					0 *3	- *2			
	R/W	R	R/W		FOFQ1	0			
					FOFQ0	0			
FF07H	0	0	WDEN	WDRST	0 *3	- *2			Unused Unused Watchdog timer enable Watchdog timer reset (writing)
					0 *3	- *2			
	R		R/W	W	WDEN	1	Enable	Disable	
					WDRST *3	Reset	Reset	Invalid	
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	- *2	High	Low	K00–K03 input port data
					K02	- *2	High	Low	
	R				K01	- *2	High	Low	
					K00	- *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1			K00–K03 input comparison register
					KCP02	1			
	R/W				KCP01	1			
					KCP00	1			
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	- *2	High	Low	K10–K13 input port data
					K12	- *2	High	Low	
	R				K11	- *2	High	Low	
					K10	- *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1			K10–K13 input comparison register
					KCP12	1			
	R/W				KCP11	1			
					KCP10	1			
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) FOUT output high impedance control (FOUTE=1) R02 output high impedance control (PTOUT=0) TOUT output high impedance control (PTOUT=1) R01 output high impedance control R00 output high impedance control
					R02HIZ	0	High-Z	Output	
	R/W				R01HIZ	0	High-Z	Output	
					R00HIZ	0	High-Z	Output	
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used R02 output port data (PTOUT=0) Fix at "1" when TOUT is used R01 output port data R00 output port data
					R02	1	High	Low	
	R/W				R01	1	High	Low	
					R00	1	High	Low	

Remarks

- *1 Initial value at initial reset
- *2 Not set in the circuit
- *3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF32H–FF46H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF32H	0	0	0	R1HIZ	0 *3 0 *3 0 *3	- *2 - *2 - *2			Unused Unused Unused
	R			R/W	R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13 R12 R11 R10	1 1 1 1	High High High High	Low Low Low Low	R10–R13 output port data
	R/W								
FF34H	0	0	0	R2HIZ	0 *3 0 *3 0 *3	- *2 - *2 - *2			Unused Unused Unused
	R			R/W	R2HIZ	0	High-Z	Output	R2 output high impedance control
FF35H	R23	R22	R21	R20	R23 R22 R21 R20	1 1 1 1	High High High High	Low Low Low Low	R20–R23 output port data
	R/W								
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03 IOC02 IOC01 IOC00	0 0 0 0	Output Output Output Output	Input Input Input Input	P00–P03 I/O control register
	R/W								
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03 PUL02 PUL01 PUL00	1 1 1 1	On On On On	Off Off Off Off	P00–P03 pull-up control register
	R/W								
FF42H	P03	P02	P01	P00	P03 P02 P01 P00	- *2 - *2 - *2 - *2	High High High High	Low Low Low Low	P00–P03 I/O port data
	R/W								
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13 IOC12 IOC11 IOC10	0 0 0 0	Output Output Output Output	Input Input Input Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected P12 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected P11 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected P10 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
	R/W								
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13 PUL12 PUL11 PUL10	1 1 1 1	On On On On	Off Off Off Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected P12 pull-up control register (EISF=0) functions as a general-purpose register when SIF (master) is selected $\overline{\text{SCLK}}$ (I) pull-up control register when SIF (slave) is selected P11 pull-up control register (EISF=0) functions as a general-purpose register when SIF is selected P10 pull-up control register (EISF=0) SIN pull-up control register when SIF is selected
	R/W								
FF46H	P13	P12	P11	P10	P13 P12 P11 P10	- *2 - *2 - *2 - *2	High High High High	Low Low Low Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected P12 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected P11 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected P10 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
	R/W								

Table 4.1.1 (c) I/O memory map (FF48H–FF71H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register (EXLCDC=0) functions as a general-purpose register when FR output is selected P22 I/O control register (EXLCDC=0) functions as a general-purpose register when CL output is selected P21 I/O control register P20 I/O control register
	R/W				IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
	R/W				IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-up control register (EXLCDC=0) functions as a general-purpose register when FR output is selected P22 pull-up control register (EXLCDC=0) functions as a general-purpose register when CL output is selected P21 pull-up control register P20 pull-up control register
	R/W				PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
	R/W				PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	–*2	High	Low	P23 I/O port data (EXLCDC=0) functions as a general-purpose register when FR output is selected P22 I/O port data (EXLCDC=0) functions as a general-purpose register when CL output is selected P21 I/O port data P20 I/O port data
	R/W				P22	–*2	High	Low	
	R/W				P21	–*2	High	Low	
	R/W				P20	–*2	High	Low	
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty [LDUTY1, 0] 0 1 2, 3 switch Duty 1/17 1/16 1/8 LCD regulated voltage switch LCD power On/Off
	R/W				LDUTY0	0			
	R/W				VCCHG	0	Vc2	Vc1	
	R/W				LPWR	0	On	Off	
FF61H	EXLCDC	ALOFF	ALON	LPAGE	EXLCDC	0	Enable	Disable	Expanded LCD driver signal control LCD all OFF control LCD all ON control Display memory area selection (when 1/8 duty is selected) functions as a general-purpose register when 1/16, 1/17 duty is selected
	R/W				ALOFF	1	All Off	Normal	
	R/W				ALON	0	All On	Normal	
	R/W				LPAGE	0	F100-F177	F000-F077	
FF62H	LC3	LC2	LC1	LC0	LC3	–*2			LCD contrast adjustment [LC3–0] 0 – 15 Contrast Light – Dark
	R/W				LC2	–*2			
	R/W				LC1	–*2			
	R/W				LC0	–*2			
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time Envelope reset (writing) Envelope On/Off Buzzer output enable
	R/W				ENRST*3	Reset	Reset	Invalid	
	R/W				ENON	0	On	Off	
	R/W				BZE	0	Enable	Disable	
FF6DH	0	BZSTP	BZSHT	SHTPW	0*3	–*2			Unused 1-shot buzzer stop (writing) 1-shot buzzer trigger (writing) 1-shot buzzer status (reading) 1-shot buzzer pulse width setting
	R				BZSTP*3	0	Stop	Invalid	
	R/W				BZSHT	0	Trigger	Invalid	
	R/W				SHTPW	0	125 msec	31.25 msec	
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0*3	–*2			Unused Buzzer [BZFQ2, 1, 0] 0 1 2 3 frequency Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 frequency [BZFQ2, 1, 0] 4 5 6 7 selection Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
	R				BZFQ2	0			
	R/W				BZFQ1	0			
	R/W				BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0*3	–*2			Unused Buzzer signal duty ratio selection (refer to main manual)
	R				BDTY2	0			
	R/W				BDTY1	0			
	R/W				BDTY0	0			
FF70H	0	0	SCTRGR	ESIF	0*3	–*2			Unused Unused Serial I/F clock trigger (writing) Serial I/F clock status (reading) Serial I/F enable (P1 port function selection)
	R				0*3	–*2			
	R/W				SCTRGR	0	Trigger	Invalid	
	R/W				ESIF	0	Run	I/O	
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation Serial I/F clock phase selection –Negative polarity (mask option) –Positive polarity (mask option) Serial I/F [SCS1, 0] 0 1 Clock Slave PT [SCS1, 0] 2 3 clock mode selection Clock OSC1/2 OSC1
	R/W				SCPS	0			
	R/W				SCS1	0			
	R/W				SCS0	0			

Table 4.1.1 (d) I/O memory map (FF72H–FFC7H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB Serial I/F transmit/receive data (low-order 4 bits) LSB
	R/W				SD2	– *2	High	Low	
	R/W				SD1	– *2	High	Low	
	R/W				SD0	– *2	High	Low	
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB Serial I/F transmit/receive data (high-order 4 bits) LSB
	R/W				SD6	– *2	High	Low	
	R/W				SD5	– *2	High	Low	
	R/W				SD4	– *2	High	Low	
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused Unused Clock timer reset (writing) Clock timer Run/Stop
	R		W	R/W	0 *3	– *2			
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	
	R		W	R/W	TMRUN	0	Run	Stop	
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz) Clock timer data (32 Hz) Clock timer data (64 Hz) Clock timer data (128 Hz)
	R				TM2	0			
	R				TM1	0			
	R				TM0	0			
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz) Clock timer data (2 Hz) Clock timer data (4 Hz) Clock timer data (8 Hz)
	R				TM6	0			
	R				TM5	0			
	R				TM4	0			
FF7CH	0	0	SWRST	SWRUN	0 *3	– *2			Unused Unused Stopwatch timer reset (writing) Stopwatch timer Run/Stop
	R		W	R/W	0 *3	– *2			
	R		W	R/W	SWRST*3	Reset	Reset	Invalid	
	R		W	R/W	SWRUN	0	Run	Stop	
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/100 sec)
	R				SWD2	0			
	R				SWD1	0			
	R				SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/10 sec)
	R				SWD6	0			
	R				SWD5	0			
	R				SWD4	0			
FFC0H	0	EVCNT	FCSEL	PLPOL	0 *3	– *2			Unused Timer 0 counter mode selection Timer 0 function selection (for event counter mode) Timer 0 pulse polarity selection (for event counter mode)
	R		R/W		EVCNT	0	Event ct.	Timer	
	R		R/W		FCSEL	0	With NR	No NR	
	R		R/W		PLPOL	0	↑	↓	
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection TOUT output control Prescaler 1 source clock selection Prescaler 0 source clock selection
	R/W				PTOUT	0	On	Off	
	R/W				CKSEL1	0	OSC3	OSC1	
	R/W				CKSEL0	0	OSC3	OSC1	
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection Division ratio 1/1 1/4 1/32 1/256 Timer 0 reset (reload) Timer 0 Run/Stop
	R/W		W	R/W	PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	
	R/W		W	R/W	PTRUN0	0	Run	Stop	
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection Division ratio 1/1 1/4 1/32 1/256 Timer 1 reset (reload) Timer 1 Run/Stop
	R/W		W	R/W	PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	
	R/W		W	R/W	PTRUN1	0	Run	Stop	
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB Programmable timer 0 reload data (low-order 4 bits) LSB
	R/W				RLD02	0			
	R/W				RLD01	0			
	R/W				RLD00	0			
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB Programmable timer 0 reload data (high-order 4 bits) LSB
	R/W				RLD06	0			
	R/W				RLD05	0			
	R/W				RLD04	0			
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB Programmable timer 1 reload data (low-order 4 bits) LSB
	R/W				RLD12	0			
	R/W				RLD11	0			
	R/W				RLD10	0			
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB Programmable timer 1 reload data (high-order 4 bits) LSB
	R/W				RLD16	0			
	R/W				RLD15	0			
	R/W				RLD14	0			

Table 4.1.1 (e) I/O memory map (FFC8H–FFF7H)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB Programmable timer 0 data (low-order 4 bits) LSB
	R				PTD02	0			
					PTD01	0			
					PTD00	0			
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB Programmable timer 0 data (high-order 4 bits) LSB
	R				PTD06	0			
					PTD05	0			
					PTD04	0			
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB Programmable timer 1 data (low-order 4 bits) LSB
	R				PTD12	0			
					PTD11	0			
					PTD10	0			
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB Programmable timer 1 data (high-order 4 bits) LSB
	R				PTD16	0			
					PTD15	0			
					PTD14	0			
FFE2H	0	0	EIPT1	EIPT0	0 *3	- *2			Unused Unused Interrupt mask register (Programmable timer 1) Interrupt mask register (Programmable timer 0)
	R		R/W		EIPT1	0	Enable	Mask	
					EIPT0	0	Enable	Mask	
FFE3H	0	0	0	EISIF	0 *3	- *2			Unused Unused Unused Interrupt mask register (Serial I/F)
	R			R/W	0 *3	- *2			
					EISIF	0	Enable	Mask	
FFE4H	0	0	0	EIK0	0 *3	- *2			Unused Unused Unused Interrupt mask register (K00–K03)
	R			R/W	0 *3	- *2			
					EIK0	0	Enable	Mask	
FFE5H	0	0	0	EIK1	0 *3	- *2			Unused Unused Unused Interrupt mask register (K10–K13)
	R			R/W	0 *3	- *2			
					EIK1	0	Enable	Mask	
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz) Interrupt mask register (Clock timer 2 Hz) Interrupt mask register (Clock timer 8 Hz) Interrupt mask register (Clock timer 32 Hz)
	R/W				EIT2	0	Enable	Mask	
					EIT1	0	Enable	Mask	
					EIT0	0	Enable	Mask	
FFE7H	0	0	EISW1	EISW10	0 *3	- *2			Unused Unused Interrupt mask register (Stopwatch timer 1 Hz) Interrupt mask register (Stopwatch timer 10 Hz)
	R		R/W		0 *3	- *2			
					EISW1	0	Enable	Mask	
					EISW10	0	Enable	Mask	
FFF2H	0	0	IPT1	IPT0	0 *3	- *2	(R)	(R)	Unused Unused Interrupt factor flag (Programmable timer 1) Interrupt factor flag (Programmable timer 0)
	R			R/W	0 *3	- *2	Yes	No	
					IPT1	0	(W)	(W)	
					IPT0	0	Reset	Invalid	
FFF3H	0	0	0	ISIF	0 *3	- *2	(R)	(R)	Unused Unused Unused Interrupt factor flag (Serial I/F)
	R			R/W	0 *3	- *2	Yes	No	
					0 *3	- *2	(W)	(W)	
					ISIF	0	Reset	Invalid	
FFF4H	0	0	0	IK0	0 *3	- *2	(R)	(R)	Unused Unused Unused Interrupt factor flag (K00–K03)
	R			R/W	0 *3	- *2	Yes	No	
					0 *3	- *2	(W)	(W)	
					IK0	0	Reset	Invalid	
FFF5H	0	0	0	IK1	0 *3	- *2	(R)	(R)	Unused Unused Unused Interrupt factor flag (K10–K13)
	R			R/W	0 *3	- *2	Yes	No	
					0 *3	- *2	(W)	(W)	
					IK1	0	Reset	Invalid	
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz) Interrupt factor flag (Clock timer 2 Hz) Interrupt factor flag (Clock timer 8 Hz) Interrupt factor flag (Clock timer 32 Hz)
	R/W				IT2	0	Yes	No	
					IT1	0	(W)	(W)	
					IT0	0	Reset	Invalid	
FFF7H	0	0	ISW1	ISW10	0 *3	- *2	(R)	(R)	Unused Unused Interrupt factor flag (Stopwatch timer 1 Hz) Interrupt factor flag (Stopwatch timer 10 Hz)
	R		R/W		0 *3	- *2	Yes	No	
					ISW1	0	(W)	(W)	
					ISW10	0	Reset	Invalid	

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

The E0C63466 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.

Figure 4.2.1.1 is the block diagram of the watchdog timer.

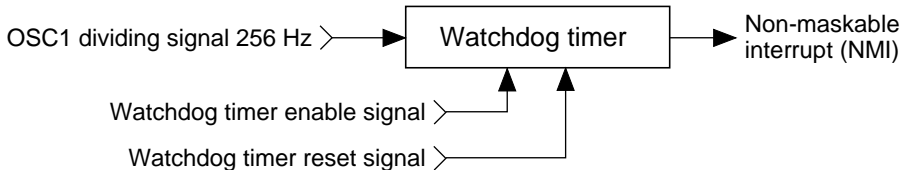


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.

Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.

The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.2.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "1"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.2.3 I/O memory of watchdog timer

Table 4.2.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	0	0	WDEN	WDRST	0 *3	- *2			Unused
					0 *3	- *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled

When "0" is written: Disabled

Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).

At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset

When "0" is written: No operation

Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.

This bit is dedicated for writing, and is always "0" for reading.

4.2.4 Programming notes

- (1) When the watchdog timer is being used, the software must reset it within 3-second cycles.
- (2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The E0C63466 has two oscillation circuits (OSC1 and OSC3). OSC1 is either a crystal or a CR oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the E0C63466 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage VD1 must be switched according to the oscillation circuit to be used. Figure 4.3.1.1 is the block diagram of this oscillation system.

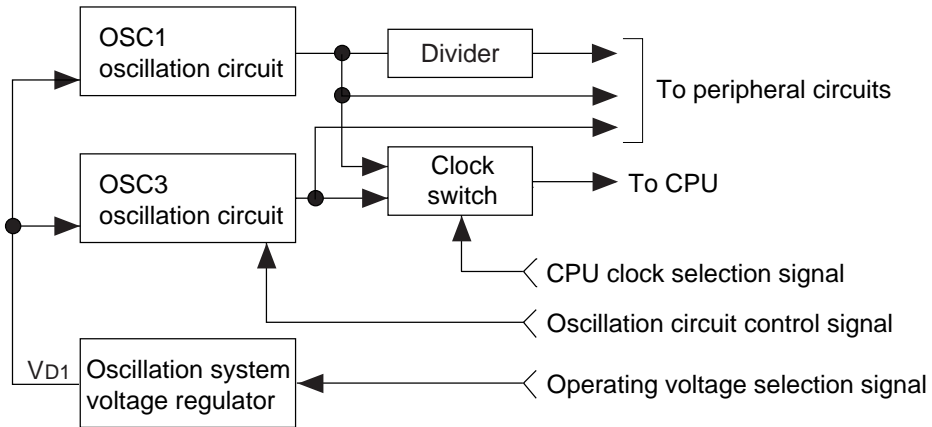


Fig. 4.3.1.1 Oscillation system block diagram

4.3.2 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. Either the crystal oscillation circuit or the CR oscillation circuit can be selected as the circuit type by mask option. The oscillation frequency of the crystal oscillation circuit is 32.768 kHz (Typ.) and the CR oscillation circuit is 60 kHz (Typ.).

Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.

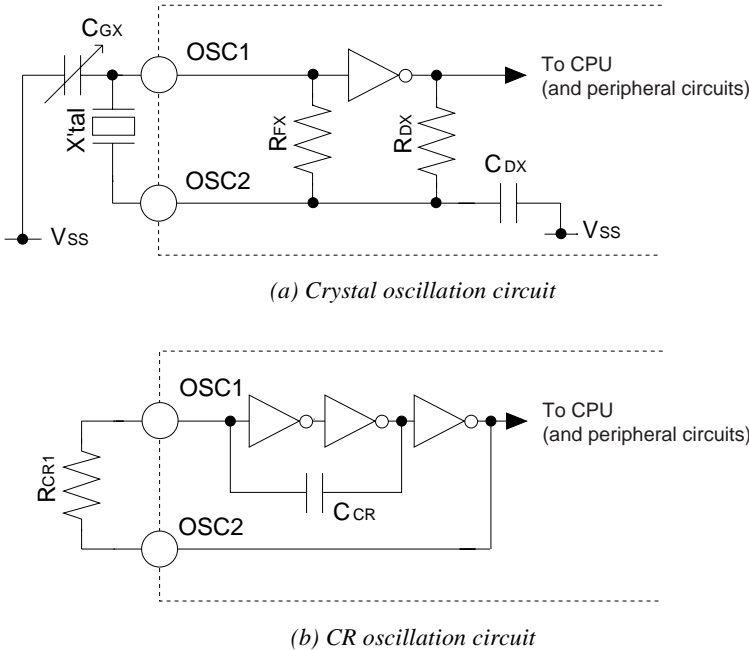


Fig. 4.3.2.1 OSC1 oscillation circuit

As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (CGX) between the OSC1 and VSS terminals when crystal oscillation is selected.

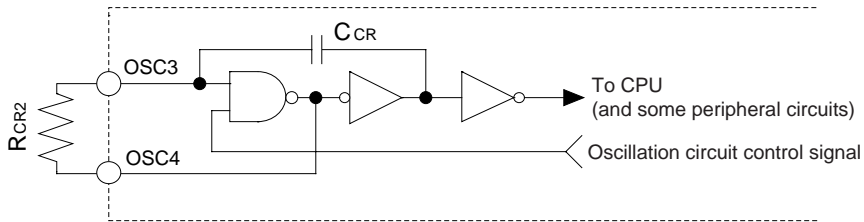
The CR oscillation circuit can be configured simply by connecting the resistor RCR1 between the OSC1 and OSC2 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of RCR1.

- Note:**
- The current consumption of CR oscillation is larger than crystal oscillation.
 - Be aware that the CR oscillation frequency changes slightly.
Pay special attention to the circuits that use fOSC1 as the source clock, such as the timer (time lag), the LCD frame frequency (display quality, flicker in low frequency) and the sound generator (sound quality).

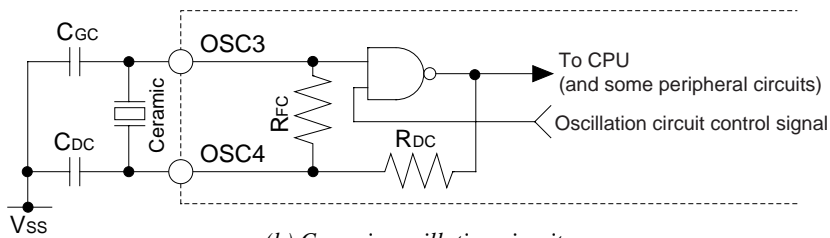
4.3.3 OSC3 oscillation circuit

The E0C63466 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 4 MHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). The mask option enables selection of either the CR or ceramic oscillation circuit. When CR oscillation is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required.

Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit



(b) Ceramic oscillation circuit

Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit can be configured simply by connecting the resistor R_{CR2} between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of R_{CR2} .

When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 4 MHz) between the OSC3 and OSC4 terminals, capacitor C_{GC} between the OSC3 and OSC4 terminals, and capacitor C_{DC} between the OSC4 and V_{SS} terminals. For both C_{GC} and C_{DC} , connect capacitors that are about 30 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

4.3.4 Switching of operating voltage

(1) When OSC1 crystal oscillation circuit is used

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register). In this case, to obtain stable operation, the operating voltage VD1 for the internal circuits must be switched by the software (VDC register).

OSC1 (crystal oscillation) operation: VD1 = 1.3 V (VDC = "0")
 OSC3 operation: VD1 = 2.2 V (VDC = "1")

When OSC3 is to be used as the CPU system clock, it should be done as the following procedure using the software: first switch the operating voltage VD1, turn the OSC3 oscillation ON after waiting 2.5 msec or more for the above operation to stabilize, switch the clock after waiting 5 msec or more for oscillation stabilization.

When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock then set the operating voltage VD1 to 1.3 V.

OSC1 → OSC3

1. Set VDC to "1" (1.3 V → 2.2 V).
2. Maintain 2.5 msec or more.
3. Set OSCC to "1" (OSC3 oscillation ON).
4. Maintain 5 msec or more.
5. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).
3. Set VDC to "0" (2.2 V → 1.3 V).

(2) When OSC1 CR oscillation circuit is used

When the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, 2.2 V of VD1 necessary to operate with OSC1 and OSC3.

OSC1 (CR oscillation) operation: VD1 = 2.2 V
 OSC3 operation: VD1 = 2.2 V

Since the E0C63466 fixes the VD1 voltage value at 2.2 V when the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, it is not necessary to switch the operating voltage VD1 by software (VDC register). However, software control to switch the CPU system clock using the CLKCHG register is necessary.

When OSC3 is to be used as the CPU system clock, it should be done as the following procedure using the software: turn the OSC3 oscillation ON, switch the clock after waiting 5 msec or more for oscillation stabilization.

When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock.

OSC1 → OSC3

1. Set OSCC to "1" (OSC3 oscillation ON).
2. Maintain 5 msec or more.
3. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC1: 60 kHz	33	67	100
OSC3: 4 MHz	0.5	1	1.5

4.3.6 I/O memory of oscillation circuit

Table 4.3.6.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.3.6.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
					0 *3	- *2			Unused
		R/W	R	R/W	VDC	0	2.2 V	1.3 V	CPU operating voltage switch (1.3 V: OSC1, 2.2 V: OSC3)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

VDC: CPU operating voltage switching register (FF00H•D0)

It is used to switch the operating voltage V_{D1} , when the crystal oscillation circuit has been selected as the OSC1 oscillation circuit by mask option.

When "1" is written: 2.2 V (for OSC3 operation)

When "0" is written: 1.3 V (for OSC1 operation)

Reading: Valid

When switching the CPU system clock, the operating voltage V_{D1} should also be switched according to the clock.

When switching from OSC1 to OSC3, first set V_{D1} to 2.2 V. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.

When switching from OSC3 to OSC1, set V_{D1} to 1.3 V after switching to OSC1 and turning the OSC3 oscillation OFF.

When the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, setting of this register does not affect the operating voltage V_{D1} , and the V_{D1} voltage is fixed at 2.2 V.

At initial reset, this register is set to "0".

OSCC: OSC3 oscillation control register (FF00H•D2)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON

When "0" is written: OSC3 oscillation OFF

Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption. Furthermore, when the crystal oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, it is necessary to switch the operating voltage V_{D1} when turning the OSC3 oscillation circuit ON and OFF

At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF00H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected

When "0" is written: OSC1 clock is selected

Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".

After turning the OSC3 oscillation ON (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.

When V_{D1} is 1.3 V (VDC = "0") and when OSC3 oscillation is OFF (OSCC = "0"), setting of CLKCHG = "1" becomes invalid and switching to OSC3 is not performed. When the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, setting VDC to "0" makes no difference.

At initial reset, this register is set to "0".

4.3.7 Programming notes

- (1) When switching the CPU system clock from OSC1 to OSC3, first set VD1. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set VD1 after switching to OSC1 and turning the OSC3 oscillation OFF. However, when the CR oscillation circuit has been selected as the OSC1 oscillation circuit, it is not necessary to set VD1.
- (2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.
- (3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.
- (4) When the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, it is not necessary to switch the operating voltage VD1 using the VDC register and the VD1 voltage is fixed at 2.2 V. The VD1 level does not change even if any data is written to the VDC register.

4.4 Input Ports (K00–K03 and K10–K13)

4.4.1 Configuration of input ports

The E0C63466 has eight bits general-purpose input ports. Each of the input port terminals (K00–K03, K10–K13) provides internal pull-up resistor. Pull-up resistor can be selected for each bit with the mask option.

Figure 4.4.1.1 shows the configuration of input port.

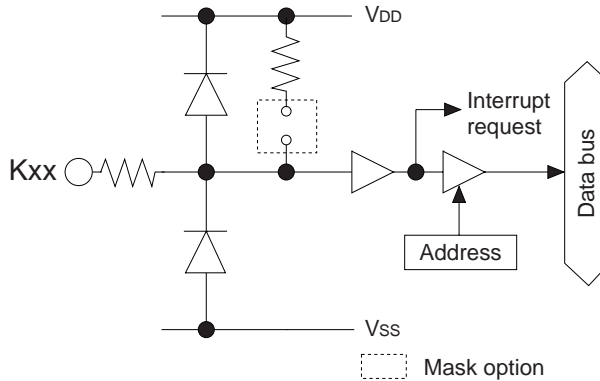


Fig. 4.4.1.1 Configuration of input port

Selection of "With pull-up resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

4.4.2 Interrupt function

All eight bits of the input ports (K00–K03, K10–K13) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.

Figure 4.4.2.1 shows the configuration of K00–K03 (K10–K13) interrupt circuit.

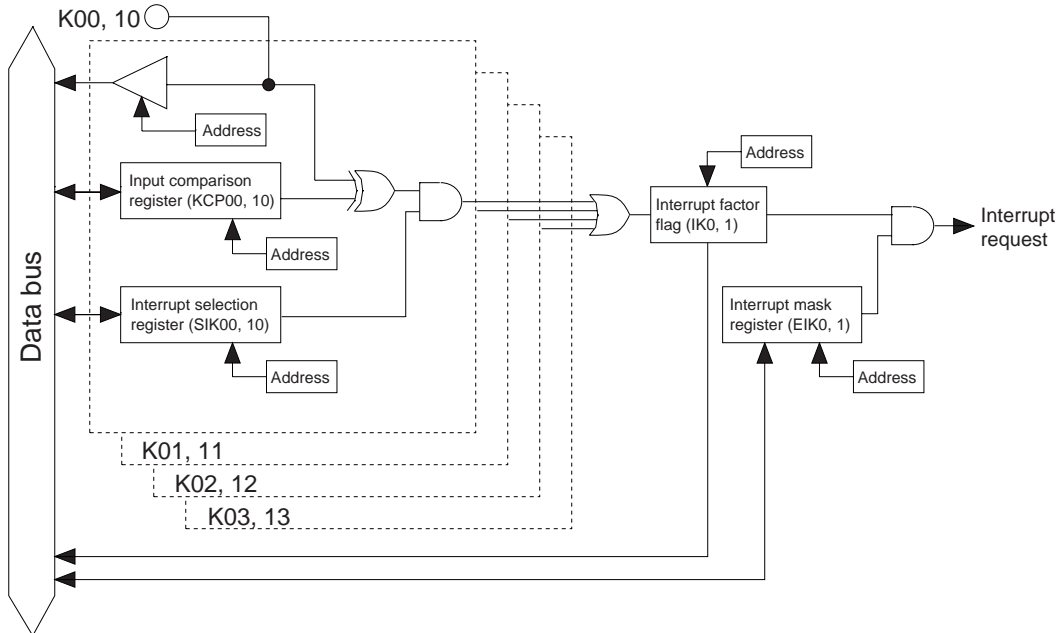


Fig. 4.4.2.1 Input interrupt circuit configuration

The interrupt selection register (SIK) and input comparison register (KCP) are individually set for the input ports K00–K03 and K10–K13, and can specify the terminals for generating interrupt and interrupt timing.

The interrupt selection registers (SIK00–SIK03, SIK10–SIK13) select what input of K00–K03 and K10–K13 to use for the interrupt. Writing "1" into an interrupt selection register incorporates that input port into the interrupt generation conditions. The changing the input port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.

The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP00–KCP03, KCP10–KCP13).

By setting these two conditions, the interrupt for K00–K03 or K10–K13 is generated when input ports in which an interrupt has been enabled by the input selection registers and the contents of the input comparison registers have been changed from matching to no matching.

The interrupt mask registers (EIK0, EIK1) enable the interrupt mask to be selected for K00–K03 and K10–K13.

When the interrupt is generated, the interrupt factor flag (IK0, IK1) is set to "1".

Figure 4.4.2.2 shows an example of an interrupt for K00–K03.

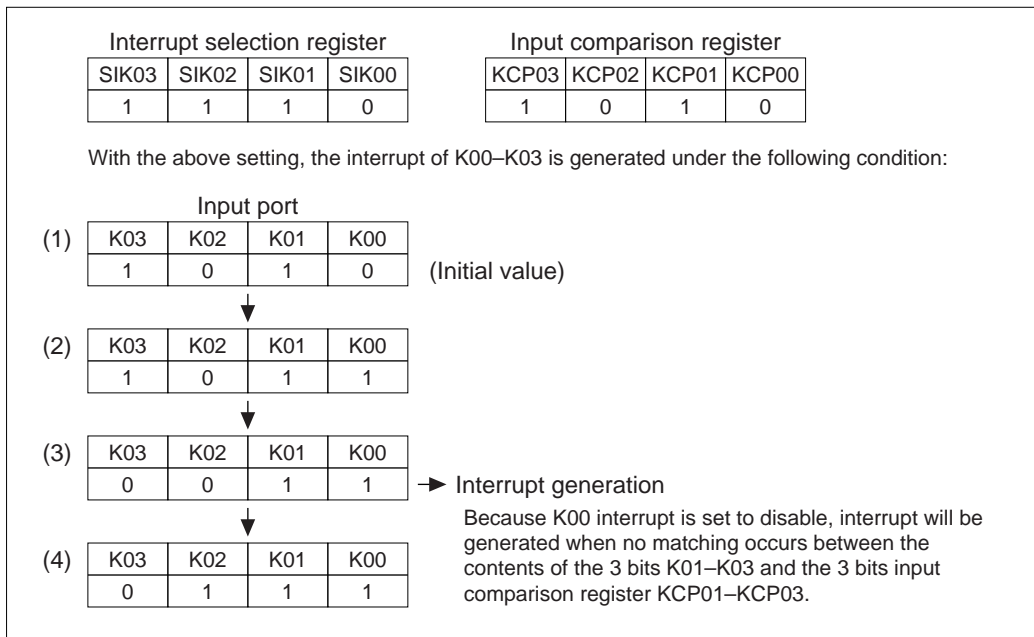


Fig. 4.4.2.2 Example of interrupt of K00–K03

K00 interrupt is disabled by the interrupt selection register (SIK00), so that an interrupt does not occur at (2). At (3), K03 changes to "0"; the data of the terminals that are interrupt enabled no longer match the data of the input comparison registers, so that interrupt occurs. As already explained, the condition for the interrupt to occur is the change in the port data and contents of the input comparison registers from matching to no matching. Hence, in (4), when the no matching status changes to another no matching status, an interrupt does not occur. Further, terminals that have been masked for interrupt do not affect the conditions for interrupt generation.

4.4.3 Mask option

Internal pull-up resistor can be selected for each of the eight bits of the input ports (K00–K03, K10–K13) with the input port mask option.

When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-up resistor" for input ports that are not being used. When using the QFP5-128pin package, "With pull-up resistor" option should be chosen for the K12 input port.

4.4.4 I/O memory of input ports

Table 4.4.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.4.4.1 Control bits of input ports

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
	R/W				SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	–*2	High	Low	K00–K03 input port data
	R				K02	–*2	High	Low	
	R				K01	–*2	High	Low	
	R				K00	–*2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
	R/W				KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
	R/W				SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
	R/W				SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	–*2	High	Low	K10–K13 input port data
	R				K12	–*2	High	Low	
	R				K11	–*2	High	Low	
	R				K10	–*2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
	R/W				KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
	R/W				KCP10	1	↓	↑	
FFE4H	0	0	0	EIK0	0 *3	–*2			Unused
	R				0 *3	–*2			Unused
	R/W				0 *3	–*2			Unused
	R/W				EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	–*2			Unused
	R				0 *3	–*2			Unused
	R/W				0 *3	–*2			Unused
	R/W				EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFF4H	0	0	0	IK0	0 *3	–*2	(R)	(R)	Unused
	R				0 *3	–*2	Yes	No	Unused
	R/W				0 *3	–*2	(W)	(W)	Unused
	R/W				IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	–*2	(R)	(R)	Unused
	R				0 *3	–*2	Yes	No	Unused
	R/W				0 *3	–*2	(W)	(W)	Unused
	R/W				IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

K00–K03: K0 port input port data (FF21H)

K10–K13: K1 port input port data (FF25H)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level

When "0" is read: Low level

Writing: Invalid

The reading is "1" when the terminal voltage of the eight bits of the input ports (K00–K03, K10–K13) goes high (VDD), and "0" when the voltage goes low (VSS).

These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF20H)**SIK10–SIK13: K1 port interrupt selection register (FF24H)**

Selects the ports to be used for the K00–K03 and K10–K13 input interrupts.

When "1" is written: Enable
 When "0" is written: Disable
 Reading: Valid

Enables the interrupt for the input ports (K00–K03, K10–K13) for which "1" has been written into the interrupt selection registers (SIK00–SIK03, SIK10–SIK13). The input port set for "0" does not affect the interrupt generation condition.

At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF22H)**KCP10–KCP13: K1 port input comparison register (FF26H)**

Interrupt conditions for terminals K00–K03 and K10–K13 can be set with these registers.

When "1" is written: Falling edge
 When "0" is written: Rising edge
 Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the eight bits (K00–K03 and K10–K13), through the input comparison registers (KCP00–KCP03 and KCP10–KCP13). For KCP00–KCP03, a comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers. For KCP10–KCP13, a comparison is done only with the ports that are enabled by the interrupt among K10–K13 by means of the SIK10–SIK13 registers.

At initial reset, these registers are set to "0".

EIK0: K0 input interrupt mask register (FFE4H•D0)**EIK1: K1 input interrupt mask register (FFE5H•D0)**

Masking the interrupt of the input port can be selected with these registers.

When "1" is written: Enable
 When "0" is written: Mask
 Reading: Valid

With these registers, masking of the input port interrupt can be selected for each of the two systems (K00–K03, K10–K13).

At initial reset, these registers are set to "0".

IK0: K0 input interrupt factor flag (FFF4H•D0)**IK1: K1 input interrupt factor flag (FFF5H•D0)**

These flags indicate the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
 When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
 When "0" is written: Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.

The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".

4.4.5 Programming notes

- (1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance? pF
R: pull-up resistance 330 k Ω
- (2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.
- (3) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.5 Output Ports (R00–R03, R10–R13 and R20–R23)

4.5.1 Configuration of output ports

The E0C63466 has 12 bits general output ports.

Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and N-channel open drain output.

Figure 4.5.1.1 shows the configuration of the output port.

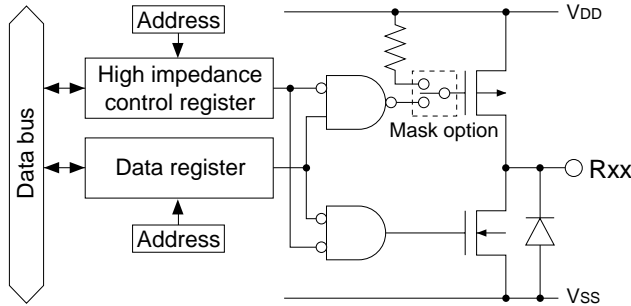


Fig. 4.5.1.1 Configuration of output port

The R02 and R03 output terminals are shared with special output terminals (TOUT, FOUT), and this function is selected by the software.

At initial reset, these are all set to the general purpose output port.

Table 4.5.1.1 shows the setting of the output terminals by function selection.

Table 4.5.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R00	R00 (High output)	R00	R00
R01	R01 (High output)	R01	R01
R02	R02 (High output)	TOUT	
R03	R03 (High output)		FOUT
R10–R13	R10–R13 (High output)	R10–R13	R10–R13
R20–R23	R20–R23 (High output)	R20–R23	R20–R23

When using the output port (R02, R03) as the special output port, the data register must be fixed at "1" and the high impedance control register must be fixed at "0" (data output).

4.5.2 Mask option

Output specifications of the output ports can be selected with the mask option.

The output specifications of the output ports R10–R13 and R20–R23 can be selected from either complementary output or N-channel open drain output individually (each of 4bits). The output ports R00–R03 can only be used as complementary output.

However, when N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the output port.

4.5.3 High impedance control

The terminal output status of the output ports can be set to a high impedance status. This control is done using the high impedance control registers.

The high impedance control registers are provided to correspond with the output ports as shown below.

High impedance control register	Corresponding output port
R00HIZ	R00 (1-bit)
R01HIZ	R01 (1-bit)
R02HIZ	R02 (1-bit)
R03HIZ	R03 (1-bit)
R1HIZ	R10–R13 (4-bit)
R2HIZ	R20–R23 (4-bit)

When "1" is written to the high impedance control register, the corresponding output port terminal goes into high impedance status. When "0" is written, the port outputs a signal according to the data register.

4.5.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R02 and R03 as shown in Table 4.5.4.1 with the software.

Figure 4.5.4.1 shows the configuration of the R02 and R03 output ports.

Table 4.5.4.1 Special output

Terminal	Special output	Output control register
R03	FOUT	FOUTE
R02	TOUT	PTOUT

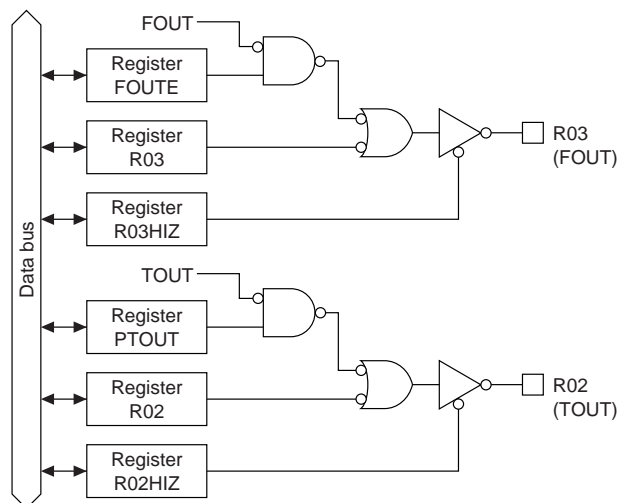


Fig. 4.5.4.1 Configuration of R02 and R03 output ports

At initial reset, the output port data register is set to "1" and the high impedance control register is set to "0". Consequently, the output terminal goes high (VDD).

When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output). The respective signal should be turned ON and OFF using the special output control register.

- Note:
- Be aware that the output terminal is fixed at a low (Vss) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
 - Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

• **TOUT (R02)**

The R02 terminal can output a TOUT signal.

The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.

To output the TOUT signal, fix the R02 register at "1" and the R02HIZ register at "0", and turn the signal ON and OFF using the PTOUT register. It is, however, necessary to control the programmable timer.

Refer to Section 4.10, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned ON and OFF.

Figure 4.5.4.2 shows the output waveform of the TOUT signal.

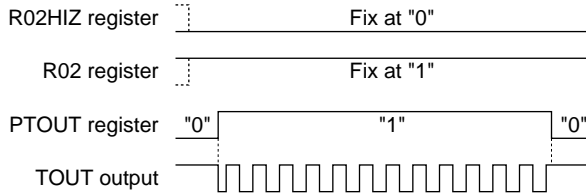


Fig. 4.5.4.2 Output waveform of TOUT signal

• **FOUT (R03)**

The R03 terminal can output a FOUT signal.

The FOUT signal is a clock (fosc1 or fosc3) that is output from the oscillation circuit or a clock that the fosc1 clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.

To output the FOUT signal, fix the R03 register at "1" and the R03HIZ register at "0", and turn the signal ON and OFF using the FOUTE register.

The frequency of the output clock may be selected from among 4 types shown in Table 4.5.4.2 by setting the FOFQ0 and FOFQ1 registers.

Table 4.5.4.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	fosc3
1	0	fosc1
0	1	fosc1 × 1/8
0	0	fosc1 × 1/64

fosc1: Clock that is output from the OSC1 oscillation circuit

fosc3: Clock that is output from the OSC3 oscillation circuit

When fosc3 is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.

Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

Note: A hazard may occur when the FOUT signal is turned ON and OFF.

Figure 4.5.4.3 shows the output waveform of the FOUT signal.

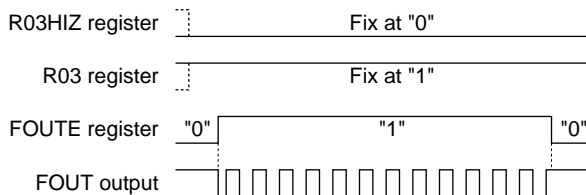


Fig. 4.5.4.3 Output waveform of FOUT signal

4.5.5 I/O memory of output ports

Table 4.5.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.5.5.1 Control bits of output ports

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE 0 *3	- *2	Enable	Disable	FOUT output enable
	R/W	R	R/W		FOFQ1 FOFQ0	0 0			Unused FOUT frequency selection
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0)
	R/W				R02HIZ	0	High-Z	Output	FOUT output high impedance control (FOUTE=1)
	R/W				R01HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0)
	R/W				R00HIZ	0	High-Z	Output	TOUT output high impedance control (PTOUT=1)
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
	R/W				R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
	R/W				R01	1	High	Low	R01 output port data
	R/W				R00	1	High	Low	R00 output port data
FF32H	0	0	0	R1HIZ	0 *3	- *2			Unused
	R			R/W	0 *3	- *2			Unused
FF33H	R13	R12	R11	R10	R1HIZ	0	High-Z	Output	Unused
	R/W				R13	1	High	Low	R10–R13 output port data
	R/W				R12	1	High	Low	
	R/W				R11	1	High	Low	
R/W				R10	1	High	Low		
FF34H	0	0	0	R2HIZ	0 *3	- *2			Unused
	R			R/W	0 *3	- *2			Unused
FF35H	R23	R22	R21	R20	R2HIZ	0	High-Z	Output	Unused
	R/W				R23	1	High	Low	R20–R23 output port data
	R/W				R22	1	High	Low	
	R/W				R21	1	High	Low	
R/W				R20	1	High	Low		
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
	R/W				PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
	R/W				CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

R00HIZ–R03HIZ: R0 port high impedance control register (FF30H)

R1HIZ: R1 port high impedance control register (FF32H•D0)

R2HIZ: R2 port high impedance control register (FF34H•D0)

Controls high impedance output of the output port.

When "1" is written: High impedance

When "0" is written: Data output

Reading: Valid

By writing "0" to the high impedance control register, the corresponding output terminal outputs according to the data register. When "1" is written, it shifts into high impedance status.

When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02HIZ register and the R03HIZ register at "0" (data output).

At initial reset, these registers are set to "0".

R00–R03: R0 output port data register (FF31H)

R10–R13: R1 output port data register (FF33H)

R20–R23: R2 output port data register (FF35H)

Set the output data for the output ports.

When "1" is written: High level output

When "0" is written: Low level output

Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (VDD), and when "0" is written, the output port terminal goes low (Vss).

When the output ports R02 and R03 are used for special output (TOUT, FOUT), fix the R02 register and the R03 register at "1".

At initial reset, these registers are all set to "1".

FOUTE: FOUT output control register (FF06H•D3)

Controls the FOUT output.

When "1" is written: FOUT output ON

When "0" is written: FOUT output OFF

Reading: Valid

By writing "1" to the FOUTE register when the R03 register has been set to "1" and the R03HIZ register has been set to "0", an FOUT signal is output from the R03 terminal. When "0" is written, the R03 terminal goes high (VDD).

When using the R03 output port for DC output, fix this register at "0".

At initial reset, this register is set to "0".

FOFQ0, FOFQ1: FOUT frequency selection register (FF06H•D0, D1)

Selects a frequency of the FOUT signal.

Table 4.5.5.2 FOUT clock frequency

FOFQ1	FOFQ0	Clock frequency
1	1	fosc3
1	0	fosc1
0	1	fosc1 × 1/8
0	0	fosc1 × 1/64

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)

Controls the TOUT output.

When "1" is written: TOUT output ON

When "0" is written: TOUT output OFF

Reading: Valid

By writing "1" to the PTOUT register when the R02 register has been set to "1" and the R02HIZ register has been set to "0", the TOUT signal is output from the R02 terminal. When "0" is written, the R02 terminal goes high (VDD).

When using the R02 output port for DC output, fix this register at "0".

At initial reset, this register is set to "0".

4.5.6 Programming notes

- (1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).
Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.
Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).
- (2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.
- (3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

4.6 I/O Ports (P00–P03, P10–P13 and P20–P23)

4.6.1 Configuration of I/O ports

The E0C63466 has 12 bits general-purpose I/O ports. Figure 4.6.1.1 shows the configuration of the I/O port.

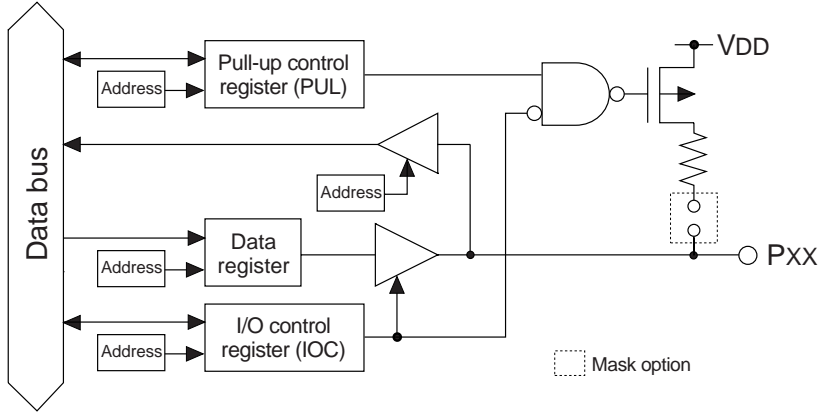


Fig. 4.6.1.1 Configuration of I/O port

The I/O port terminals P10 to P13 are shared with the serial interface input/output terminals. The P22 and P23 terminals are shared with the special output (CL, FR) terminals. The software can select the function to be used.

At initial reset, these are all set to the I/O port.

Table 4.6.1.1 shows the setting of the input/output terminals by function selection.

Table 4.6.1.1 Function setting of input/output terminals

Terminal	Terminal status at initial reset	Special output		Serial I/F	
		CL	FR	Master	Slave
P00–P03	P00–P03 (Input & pull-up *)	P00–P03	P00–P03	P00–P03	P00–P03
P10	P10 (Input & pull-up *)			SIN(I)	SIN(I)
P11	P11 (Input & pull-up *)			SOUT(O)	SOUT(O)
P12	P12 (Input & pull-up *)			SCLK(O)	SCLK(I)
P13	P13 (Input & pull-up *)			P13	SRDY(O)
P20	P20 (Input & pull-up *)	P20	P20	P20	P20
P21	P21 (Input & pull-up *)	P21	P21	P21	P21
P22	P22 (Input & pull-up *)	CL			
P23	P23 (Input & pull-up *)		FR		

* When "with pull-up resistor" is selected by the mask option (high impedance when "gate direct" is set)

When these ports are used as I/O ports, the ports can be set to either input mode or output mode individually (in 1-bit unit). Modes can be set by writing data to the I/O control registers.

Refer to Section 4.11, "Serial Interface", for control of the serial interface.

4.6.2 Mask option

In the I/O ports P10–P13 and P20–P23, the output specification during output mode can be selected from either complementary output or N-channel open drain output by mask option. They are selected in 1-bit units or 4-bit units depending on the terminal group. Note that the P00–P03 can be only used as complementary output.

Ports to be selected in 1-bit units: P20, P21, P22, P23

Ports to be selected in 4-bit units: P10–P13

The mask option also permits selection of whether the pull-up resistor is used or not during input mode. They are selected in 1-bit units or 4-bit units depending on the terminal group.

Ports to be selected in 1-bit units: P20, P21, P22, P23

Ports to be selected in 4-bit units: P10–P13

When N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

When "without pull-up" during the input mode is selected, take care that the floating status does not occur.

This option is effective even when I/O ports are used for special output or input/output of the serial interface.

4.6.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOCxx.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.

However, when the pull-up explained in the following section has been set by software, the input line is pulled up only during this input mode.

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode, it works as an output port, it outputs a high level (VDD) when the port output data is "1", and a low level (Vss) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

The I/O control registers of the ports that are set as special output or input/output for the serial interface can be used as general purpose registers that do not affect the I/O control. (See Table 4.6.1.1.)

4.6.4 Pull-up during input mode

A pull-up resistor that operates during the input mode is built into each I/O port of the E0C63466. Mask option can set the use or non-use of this pull-up.

The pull-up resistor becomes effective by writing "1" to the pull-up control register PULxx that corresponds to each port, and the input line is pulled up during the input mode. When "0" has been written, no pull-up is done.

At initial reset, the pull-up control registers are set to "1".

The pull-up control registers of the ports in which "without pull-up" have been selected can be used as general purpose registers.

Even when "with pull-up" has been selected, the pull-up control registers of the ports, that are set as special output or output for the serial interface, can be used as general purpose registers that do not affect the pull-up control. (See Table 4.6.1.1.)

The pull-up control registers of the port, that are set as input for the serial interface, function the same as the I/O port.

4.6.5 Special outputs (CL, FR)

The I/O ports P22 and P23 can be used as special output ports that output CL and FR signals by switching the function with software. Since P22 and P23 are set to I/O port (input mode) at initial reset, when using the special outputs, select the special output function using the EXLDCDC register. The data registers, I/O control registers and pull-up control registers of the ports set in the special output can be used as general purpose registers that do not affect the output.

When "1" is written to the EXLDCDC register, P22 is set to the CL output port and P23 is set to the FR output port.

The CL and FR signals are LCD synchronous signal (CL) and LCD flame signal (FR) for externally expanded LCD driver, and are output from the P22 terminal and P23 terminal when the functions are switched by the EXLDCDC register.

The following tables show the frequencies of the CL and FR signals.

Table 4.6.5.1 CL signal frequency

OSC1 oscillation frequency	When 1/8 duty is selected	When 1/16 duty is selected	When 1/17 duty is selected
32.768 kHz	512 Hz	1,024 Hz	1,024 Hz
60 kHz	937.5 Hz	1,875 Hz	1,875 Hz

Table 4.6.5.2 FR signal frequency

OSC1 oscillation frequency	When 1/8 duty is selected	When 1/16 duty is selected	When 1/17 duty is selected
32.768 kHz	32 Hz	32 Hz	30.12 Hz
60 kHz	58.6 Hz	58.6 Hz	55.2 Hz

Refer to Section 4.7, "LCD Driver", for control of the LCD drive duty.

Note: A hazard may occur when the CL signal or FR signal is turned ON or OFF (when the port function is switched).

Figure 4.6.5.1 shows the output waveforms of CL and FR signals.

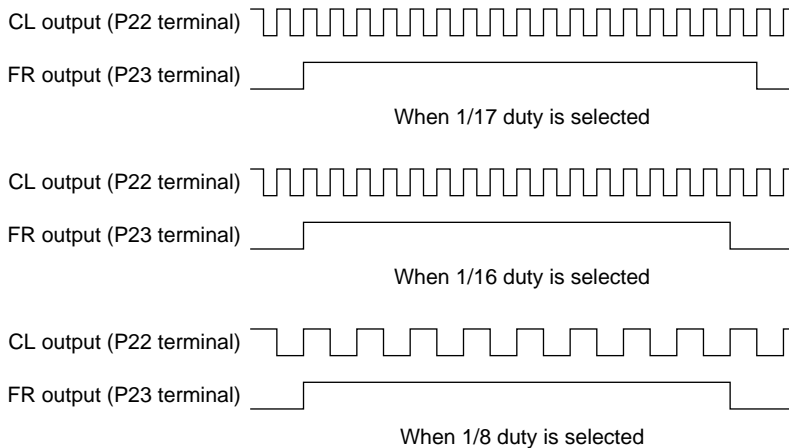


Fig. 4.6.5.1 Output waveforms of CL and FR signals

4.6.6 I/O memory of I/O ports

Tables 4.6.6.1(a) and (b) show the I/O addresses and the control bits for the I/O ports.

Table 4.6.6.1(a) Control bits of I/O ports

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	–*2	High	Low	P00–P03 I/O port data
					P02	–*2	High	Low	
	R/W				P01	–*2	High	Low	
					P00	–*2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected P12 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected P11 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected P10 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
					IOC12	0	Output	Input	
	R/W				IOC11	0	Output	Input	
					IOC10	0	Output	Input	
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected P12 pull-up control register (EISF=0) functions as a general-purpose register when SIF (master) is selected $\overline{\text{SCLK}}$ (1) pull-up control register when SIF (slave) is selected P11 pull-up control register (EISF=0) functions as a general-purpose register when SIF is selected P10 pull-up control register (EISF=0) SIN pull-up control register when SIF is selected
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
					PUL10	1	On	Off	
FF46H	P13	P12	P11	P10	P13	–*2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected P12 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected P11 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected P10 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
					P12	–*2	High	Low	
	R/W				P11	–*2	High	Low	
					P10	–*2	High	Low	
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register (EXLCDC=0) functions as a general-purpose register when FR output is selected P22 I/O control register (EXLCDC=0) functions as a general-purpose register when CL output is selected P21 I/O control register P20 I/O control register
					IOC22	0	Output	Input	
	R/W				IOC21	0	Output	Input	
					IOC20	0	Output	Input	
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-up control register (EXLCDC=0) functions as a general-purpose register when FR output is selected P22 pull-up control register (EXLCDC=0) functions as a general-purpose register when CL output is selected P21 pull-up control register P20 pull-up control register
					PUL22	1	On	Off	
	R/W				PUL21	1	On	Off	
					PUL20	1	On	Off	
FF4AH	P23	P22	P21	P20	P23	–*2	High	Low	P23 I/O port data (EXLCDC=0) functions as a general-purpose register when FR output is selected P22 I/O port data (EXLCDC=0) functions as a general-purpose register when CL output is selected P21 I/O port data P20 I/O port data
					P22	–*2	High	Low	
	R/W				P21	–*2	High	Low	
					P20	–*2	High	Low	

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

Table 4.6.6.1(b) Control bits of I/O ports

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF61H	EXLCDC	ALOFF	ALON	LPAGE	EXLCDC	0	Enable	Disable	Expanded LCD driver signal control
					ALOFF	1	All Off	Normal	LCD all OFF control
					ALON	0	All On	Normal	LCD all ON control
					LPAGE	0	F100-F177	F000-F077	Display memory area selection (when 1/8 duty is selected) functions as a general-purpose register when 1/16, 1/17 duty is selected
FF70H	R/W								
	0	0	SCTRG	ESIF	0 *3	- *2			Unused
					0 *3	- *2			Unused
	R		R/W		SCTRG	0	Trigger Run	Invalid Stop	Serial I/F clock trigger (writing) Serial I/F clock status (reading)
				ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)	

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

(1) Selection of port function

EXLCDC: Expanded LCD driver signal control register (FF61H•D3)

Sets P22 and P23 to the CL signal and the FR signal output ports.

When "1" is written: CL/FR signal output

When "0" is written: I/O port

Reading: Valid

When setting P22 to the CL (LCD synchronous signal) output and P23 to the FR (LCD frame signal) output, write "1" to this register and when they are used as I/O ports, write "0".

The CL and FR signals are output from the P22 terminal and P23 terminal immediately after the functions are switched by the EXLCDC register. In this case, the control registers for P22 and P23 can be used as general purpose registers that do not affect the output.

At initial reset, this register is set to "0".

ESIF: Serial interface enable register (FF70H•D0)

Selects function for P10–P13.

When "1" is written: Serial interface input/output port

When "0" is written: I/O port

Reading: Valid

When using the serial interface, write "1" to this register and when P10–P13 are used as the I/O port, write "0". The configuration of the terminals within P10–P13 that are used for the serial interface is decided by the mode selected with the SCS1 and SCS0 registers (see Section 4.11).

In the slave mode, all the P10–P13 ports are set to the serial interface input/output port. In the master mode, P10–P12 are set to the serial interface input/output port and P13 can be used as the I/O port.

At initial reset, this register is set to "0".

(2) I/O port control**P00–P03: P0 I/O port data register (FF42H)****P10–P13: P1 I/O port data register (FF46H)****P20–P23: P2 I/O port data register (FF4AH)**

I/O port data can be read and output data can be set through these registers.

• When writing data

When "1" is written: High level

When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (VDD), and when "0" is written, the terminal goes low (VSS).

Port data can be written also in the input mode.

• When reading data

When "1" is read: High level

When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (VDD) the port data that can be read is "1", and when the terminal voltage is low (VSS) the data is "0".

When "with pull-up resistor" has been selected with the mask option and the PUL register is set to "1", the built-in pull-up resistor goes ON during input mode, so that the I/O port terminal is pulled up.

The data registers of the port, which are set for the special output (P22, P23) or input/output of the serial interface (P10–P12 or P10–P13), become general-purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF

R: pull-up resistance 330 kΩ

IOC00–IOC03: P0 port I/O control register (FF40H)**IOC10–IOC13: P1 port I/O control register (FF44H)****IOC20–IOC23: P2 port I/O control register (FF48H)**

The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode

When "0" is written: Input mode

Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.

Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.

At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.

The I/O control registers of the port, which are set for the special output (P22, P23) or input/output of the serial interface (P10–P12 or P10–P13), become general-purpose registers that do not affect the input/output.

PUL00–PUL03: P0 port pull-up control register (FF41H)

PUL10–PUL13: P1 port pull-up control register (FF45H)

PUL20–PUL23: P2 port pull-up control register (FF49H)

The pull-up during the input mode are set with these registers.

When "1" is written: Pull-up ON

When "0" is written: Pull-up OFF

Reading: Valid

The built-in pull-up resistor which is turned ON during input mode is set to enable in 1-bit units. (The pull-up resistor is included into the ports selected by the mask option.)

By writing "1" to the pull-up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.

At initial reset, these registers are all set to "1", so the pull-up function is set to ON.

The pull-up control registers of the ports in which the pull-up resistor is not included become the general purpose register. The registers of the ports that are set as special output or output for the serial interface can also be used as general purpose registers that do not affect the pull-up control.

The pull-up control registers of the port that are set as input for the serial interface function the same as the I/O port.

4.6.7 Programming notes

- (1) When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF

R: pull-up resistance 330 kΩ

- (2) When special output (CL, FR) has been selected, a hazard may occur when the signal is turned ON or OFF.

4.7 LCD Driver (COM0–COM16, SEG0–SEG59)

4.7.1 Configuration of LCD driver

The E0C63466 has 17 common terminals (COM0–COM16) and 60 segment terminals (SEG0–SEG59), so that it can drive a dot matrix type LCD with a maximum of 1,020 (60 × 17) dots.

The driving method is 1/17 duty, 1/16 duty or 1/8 duty dynamic drive with four voltages (1/4 bias), VC1, VC2, VC4 and VC5 (1/5 bias driving can be set by impressing five voltages from outside).

LCD display ON/OFF can be controlled by the software.

4.7.2 Power supply for LCD driving

VC1–VC5 are driving voltages for the LCD, and for which either the voltages generated by the LCD system voltage circuit or voltages to be supplied from outside can be used. The built-in LCD system voltage circuit generates four voltages (1/4 bias) VC1, VC2, VC4 and VC5 except for VC3. These four output voltages can be supplied to the outside only for driving the externally expanded LCD driver.

When external voltages are supplied, 1/5 bias driving can be made by inputting five voltages to the VC1–VC5 terminals (including VC3).

Either the internal generated voltages or external voltages used for the LCD drive voltage can be selected by the mask option.

Turning the LCD system voltage circuit ON or OFF is controlled with the LPWR register. This control is also necessary when supplying the voltage from outside. When LPWR is set to "1", the LCD system voltage circuit outputs the LCD drive voltages VC1–VC5 to the LCD driver.

When "internal voltage" is selected by the mask option, the LCD system voltage circuit generates VC1 or VC2 with the voltage regulator incorporated in itself, and generates three other voltages by boosting or reducing the voltage VC1 or VC2. Table 4.7.2.1 shows the VC1, VC2, VC4 and VC5 voltage values and boost/reduce status.

Table 4.7.2.1 LCD drive voltage when generated internally

LCD drive voltage	V _{DD} = 1.8–6.4 V	V _{DD} = 2.6–6.4 V
VC1 (0.975–1.2 V)	VC1 (standard)	1/2 × VC2
VC2 (1.950–2.4 V)	2 × VC1	VC2 (standard)
VC4 (2.925–3.6 V)	3 × VC1	3/2 × VC2
VC5 (3.900–4.8 V)	4 × VC1	2 × VC2

Note: The LCD drive voltage can be adjusted by the software (see Section 4.7.6). Values in the table are typical values.

Select either VC1 standard or VC2 standard using the VCCHG register.

When "1" is written to the VCCHG register, VC2 standard is selected and when "0" is written, VC1 standard is selected. At initial reset, VC1 standard (VCCHG = "0") is set.

4.7.3 Mask option

Disconnecting the internal power supply for LCD driving will enable voltages to be supplied externally. In such case, the five voltages are entered in VC1, VC2, VC3, VC4 and VC5 terminals and 1/5 bias driving may then be set. Since 1/5 bias driving provides better display quality, when low power current consumption is not required (i.e., when power is supplied from AC outlet), select external power mode. However, note that in order to maintain a stable display, power source must be one which will remain stable even when heavy load such as buzzer, etc. is driven.

Moreover, in the external power mode, the contrast adjustment function cannot be used. Accommodate this limitation by utilizing the external circuit as necessary.

A sample circuit of external power for LCD driving when power is supplied externally is shown in Figure 4.7.3.1.

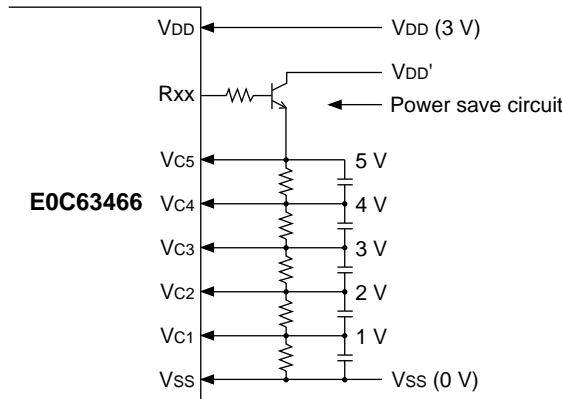


Fig. 4.7.3.1 Sample circuit of external power for LCD driving when power is supplied externally

4.7.4 LCD display control (ON/OFF) and switching of duty

(1) Display ON/OFF control

The E0C63466 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the dots go ON, and when "1" is written to ALOFF, all the dots go OFF. At such a time, an ON waveform or an OFF waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all ON) has priority over the ALOFF (all OFF).

(2) Switching of drive duty

In the E0C63466, the drive duty can be set to 1/17, 1/16 or 1/8 by the software. This setting is done using the LDUTY1 and LDUTY0 registers as shown in Table 4.7.4.1.

Table 4.7.4.1 LCD drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/8	COM0–COM7	480 (60 × 8)
0	1	1/16	COM0–COM15	960 (60 × 16)
0	0	1/17	COM0–COM16	1,020 (60 × 17)

Table 4.7.4.2 shows the frame frequencies corresponding to the OSC1 oscillation frequency and drive duty.

Table 4.7.4.2 Frame frequency

OSC1 oscillation frequency	When 1/8 duty is selected	When 1/16 duty is selected	When 1/17 duty is selected
32.768 kHz	32 Hz	32 Hz	30.12 Hz
60 kHz	58.6 Hz	58.6 Hz	55.2 Hz

Figures 4.7.4.1 and 4.7.4.2 show the dynamic drive waveform for 1/4 bias and 1/5 bias.

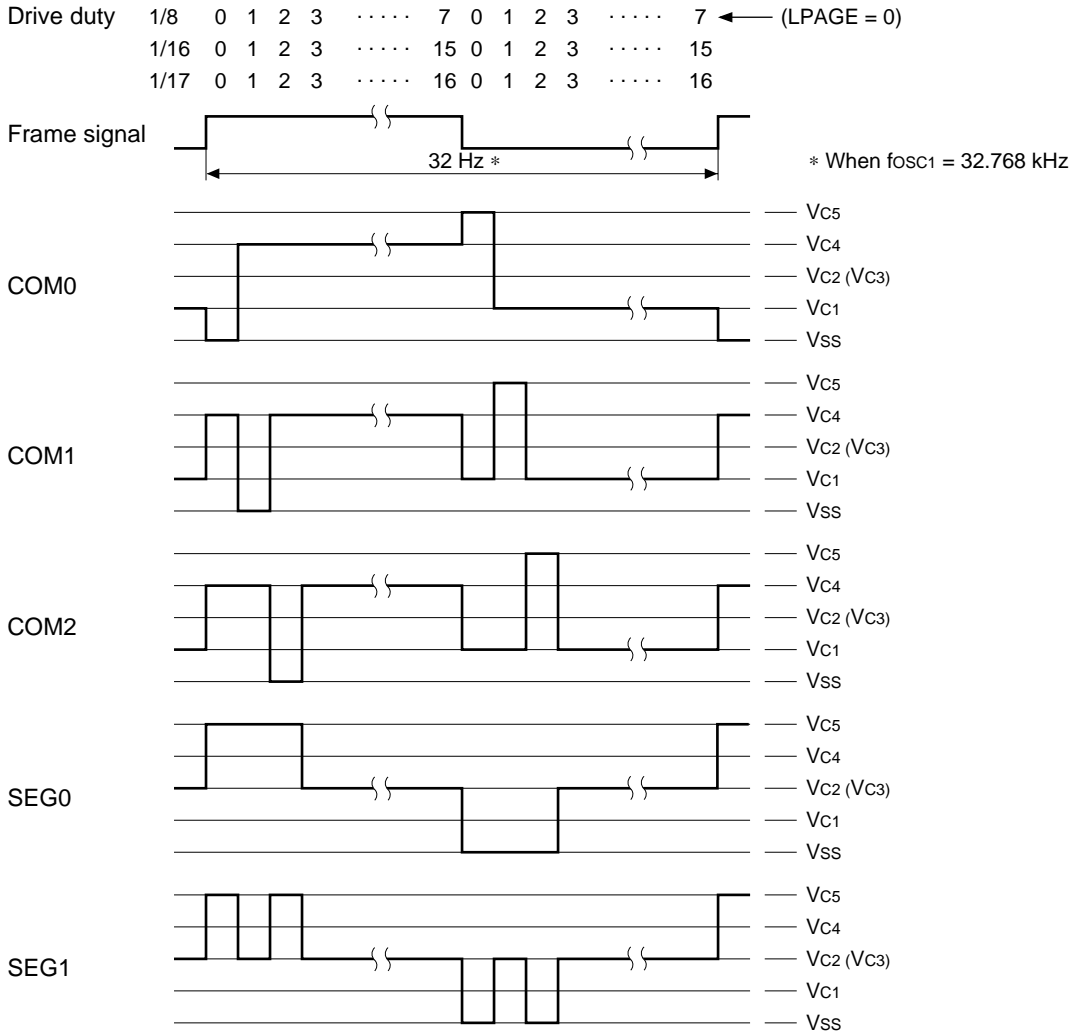


Fig. 4.7.4.1 Drive waveform for 1/4 bias

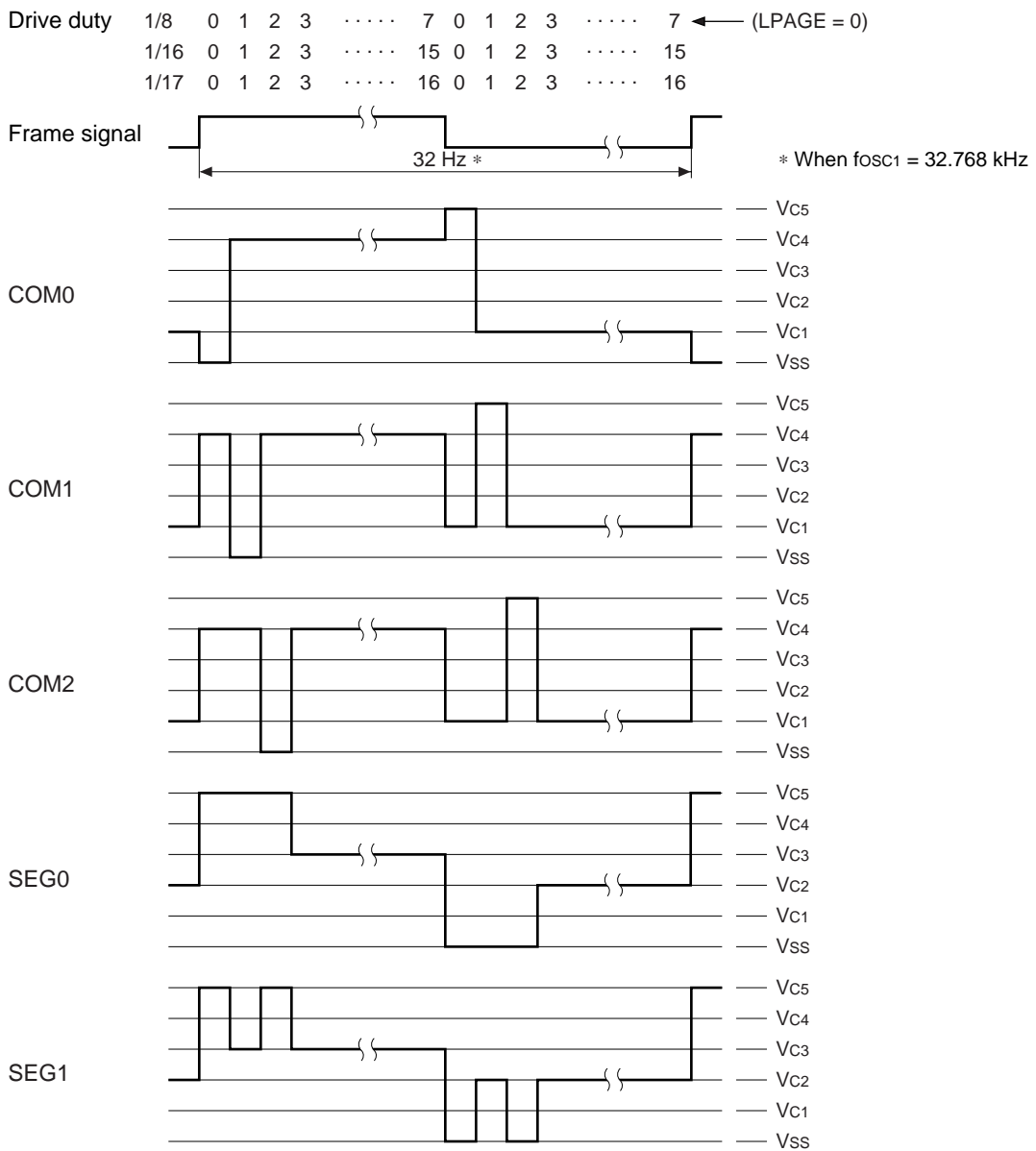
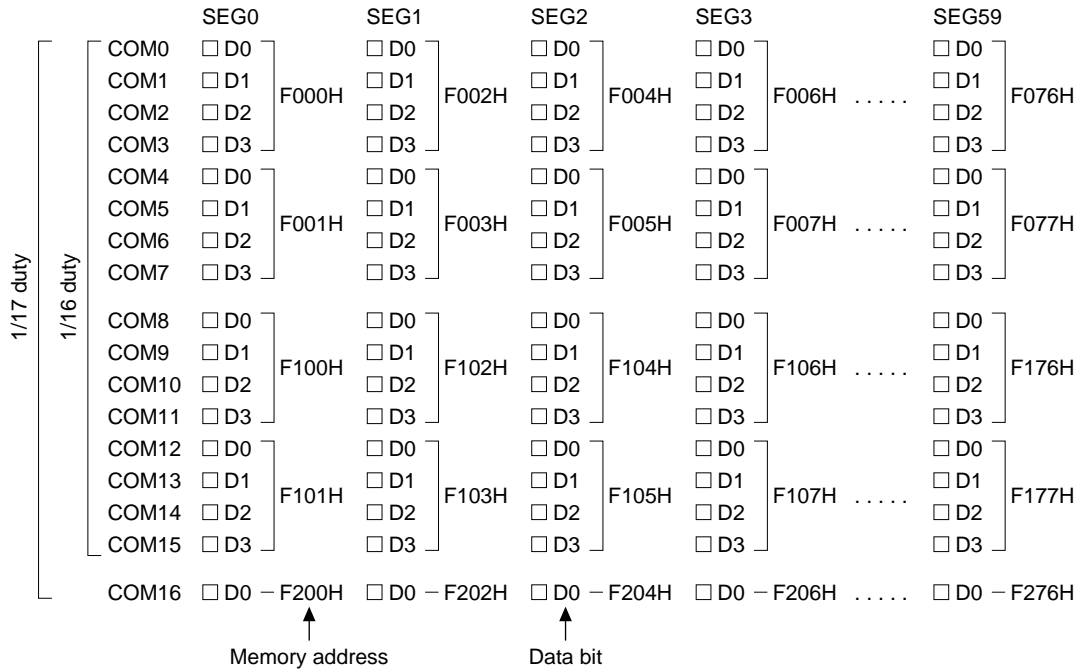


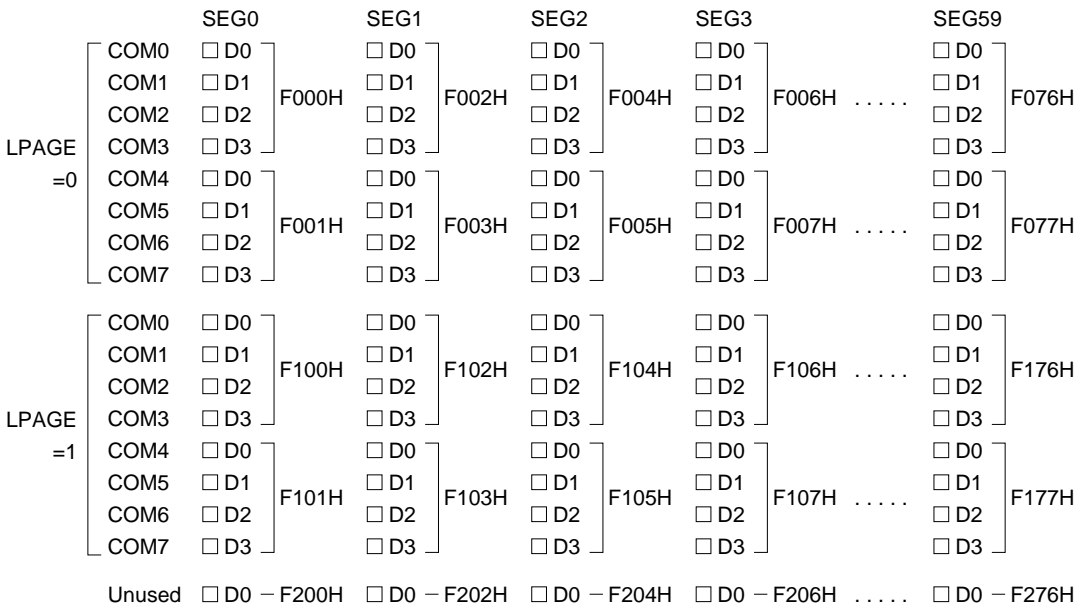
Fig. 4.7.4.2 Drive waveform for 1/5 bias

4.7.5 Display memory

The display memory is allocated to F000H–F276H in the data memory area and the addresses and the data bits correspond to COM and SEG outputs as shown in Figure 4.7.5.1.



(a) When 1/17 or 1/16 duty is selected



(b) When 1/8 duty is selected

Fig. 4.7.5.1 Correspondence between display memory and LCD dot matrix

When a bit in the display memory is set to "1", the corresponding LCD dot goes ON, and when it is set to "0", the dot goes OFF.

At 1/17 (1/16) duty drive, all data of COM0–COM16 (15) is output.

At 1/8 duty drive, data only corresponding to COM0–COM7 is output. However, since the display memory has capacity for two screens, it is designed so that the memory for COM8–COM15 shown in Figure 4.7.5.1 (b) can also be used as COM0–COM7. Select either F000H–F077H or F100H–F177H for the area to be displayed (to be output from COM0–COM7 terminals) using the LPAGE register. It can switch the screen in an instant.

At initial reset, the data memory content becomes undefined hence, there is need to initialize using the software.

The display memory has read/write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

Note: When a program that access no memory mounted area (F078H–F0FFH, F178H–F1FFH, F201H, F203H, . . . , F277H) is made, the operation is not guaranteed.

4.7.6 LCD contrast adjustment

In the E0C63466, the LCD contrast can be adjusted by the software.

It is realized by controlling the voltages VC1, VC2, VC4 and VC5 output from the LCD system voltage circuit. When these voltages are supplied to the externally expanded LCD driver, the expanded LCD contrast is adjusted at the same time. However, when the LCD drive voltage is supplied from outside by the mask option selection, this adjustment becomes invalid.

The contrast can be adjusted to 16 levels as shown in Table 4.7.6.1. When VCCHG = "0", VC1 is changed within the range from 0.975 V to 1.2 V, and other voltages change according to VC1. When VCCHG = "1", VC2 is changed within the range from 1.950 V to 2.4 V, and other voltages change according to VC2.

Table 4.7.6.1 LCD contrast

No.	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light ↑
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	↓ dark
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

At room temperature, use setting number 7 or 8 as standard.

Since the contents of LC0–LC3 are undefined at initial reset, initialize it by the software.

4.7.7 I/O memory of LCD driver

Table 4.7.7.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.7.7.1 shows the display memory map.

Table 4.7.7.1 LCD driver control bits

Address	Register				Register				Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0] 0 1 2, 3 Duty 1/17 1/16 1/8
					LDUTY0	0			
	R/W				VCCHG	0	Vc2	Vc1	LCD regulated voltage switch
	R/W				LPWR	0	On	Off	LCD power On/Off
FF61H	EXLCDC	ALOFF	ALON	LPAGE	EXLCDC	0	Enable	Disable	Expanded LCD driver signal control
					ALOFF	1	All Off	Normal	
	R/W				ALON	0	All On	Normal	LCD all ON control
	R/W				LPAGE	0	F100-F177	F000-F077	Display memory area selection (when 1/8 duty is selected) functions as a general-purpose register when 1/16, 1/17 duty is selected
FF62H	LC3	LC2	LC1	LC0	LC3	- *2			LCD contrast adjustment [LC3-0] 0 - 15 Contrast Light - Dark
					LC2	- *2			
	R/W				LC1	- *2			
	R/W				LC0	- *2			

- *1 Initial value at initial reset
- *2 Not set in the circuit
- *3 Constantly "0" when being read

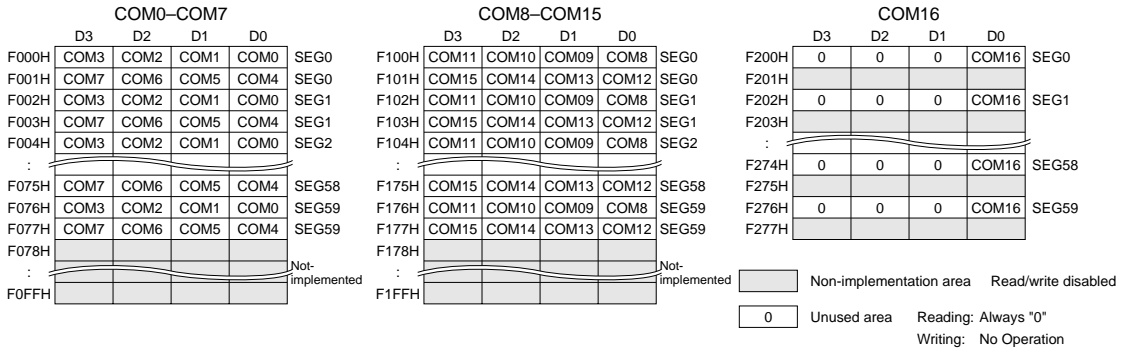


Fig. 4.7.7.1 Display memory map

LPWR: LCD power control (ON/OFF) register (FF60H•D0)

Turns the LCD system voltage circuit ON and OFF.

- When "1" is written: ON
- When "0" is written: OFF
- Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes ON and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to Vss level.

It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.

At initial reset, this register is set to "0".

VCCHG: LCD regulated voltage switching register (FF60H•D1)

Selects the reference voltage for the LCD drive voltage.

- When "1" is written: VC2
- When "0" is written: VC1
- Reading: Valid

When "1" is written to the VCCHG register, the LCD system voltage circuit generates the LCD drive voltage as VC2 standard. When "0" is written, it becomes VC1 standard. Select VC2 when power supply voltage is 2.6 V or more, otherwise, select VC1.

When external power mode is selected by the mask option, this control is unnecessary. At initial reset, this register is set to "0".

LDUTY0, LDUTY1: LCD drive duty switching register (FF60H•D2, D3)

Selects the LCD drive duty.

Table 4.7.7.2 Drive duty setting

LDUTY1	LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	*	1/8	COM0–COM7	480 (60 × 8)
0	1	1/16	COM0–COM15	960 (60 × 16)
0	0	1/17	COM0–COM16	1,020 (60 × 17)

At initial reset, this register is set to "0".

ALON: LCD all ON control register (FF61H•D1)

Displays the all LCD dots ON.

- When "1" is written: All LCD dots displayed
- When "0" is written: Normal display
- Reading: Valid

By writing "1" to the ALON register, all the LCD dots goes ON, and when "0" is written, it returns to normal display.

This function outputs an ON waveform to the SEG terminals, and does not affect the content of the display memory.

ALON has priority over ALOFF.

At initial reset, this register is set to "0".

ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD dots.

- When "1" is written: All LCD dots fade out
- When "0" is written: Normal display
- Reading: Valid

By writing "1" to the ALOFF register, all the LCD dots goes OFF, and when "0" is written, it returns to normal display.

This function outputs an OFF waveform to the SEG terminals, and does not affect the content of the display memory.

At initial reset, this register is set to "0".

LPAGE: LCD display memory selection register (FF61H•D0)

Selects the display memory area at 1/8 duty drive.

When "1" is written: F100H–F177H

When "0" is written: F000H–F077H

Reading: Valid

By writing "1" to the LPAGE register, the data set in F100H–F177H (the second half of the display memory) is displayed, and when "0" is written, the data set in F000H–F077H (the first half of the display memory) is displayed.

This function is valid only when 1/8 duty is selected, and when 1/16 or 1/17 duty is selected, this register can be used as a general purpose register.

At initial reset, this register is set to "0".

LC3–LC0: LCD contrast adjustment register (FF62H)

Adjusts the LCD contrast.

LC3–LC0 = 0000B light

: :

LC3–LC0 = 1111B dark

At room temperature, use setting number 7 or 8 as standard.

When the LCD drive voltage is supplied from outside by the mask option selection, this adjustment becomes invalid.

At initial reset, LC0–LC3 are undefined.

4.7.8 Programming notes

- (1) When a program that access no memory mounted area (F078H–F0FFH, F178H–F1FFH, F201H, F203H, . . . , F277H) is made, the operation is not guaranteed.
- (2) Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

4.8 Clock Timer

4.8.1 Configuration of clock timer

The E0C63466 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.

Figure 4.8.1.1 is the block diagram for the clock timer.

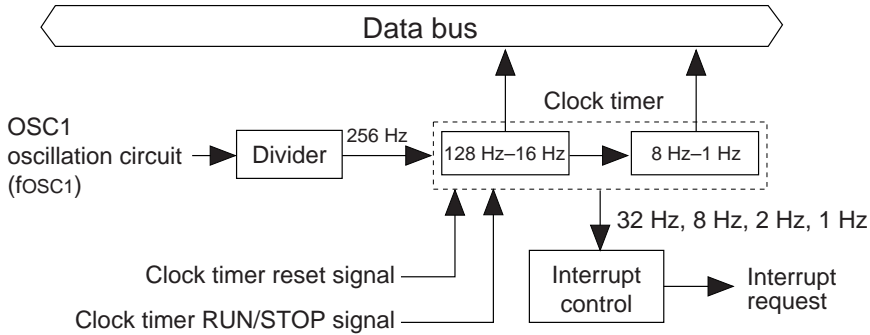


Fig. 4.8.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

Note: When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

4.8.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF79H and FF7AH.

<FF79H> D0: TM0 = 128 Hz D1: TM1 = 64 Hz D2: TM2 = 32 Hz D3: TM3 = 16 Hz
 <FF7AH> D0: TM4 = 8 Hz D1: TM5 = 4 Hz D2: TM6 = 2 Hz D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).

The high-order data hold function in the E0C63466 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (Varies due to the read timing.)

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.8.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.

Figure 4.8.3.1 is the timing chart of the clock timer.

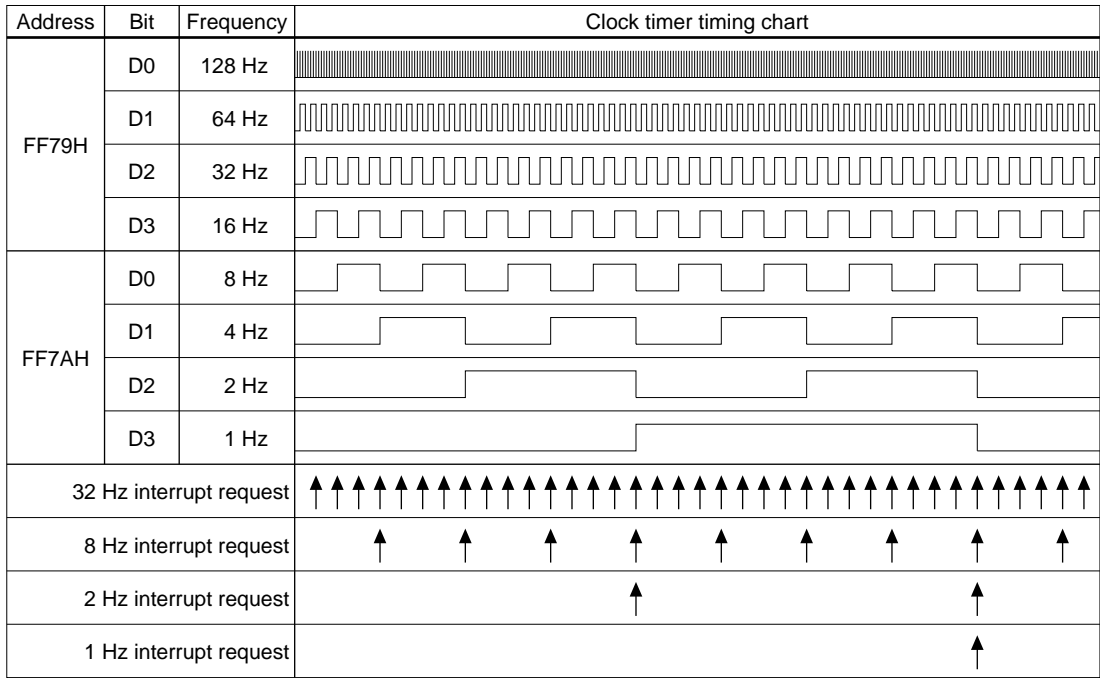


Fig. 4.8.3.1 Timing chart of clock timer

As shown in Figure 4.8.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.8.4 I/O memory of clock timer

Table 4.8.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.8.4.1 Control bits of clock timer

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF78H	0	0	TMRST	TMRUN	0 *3 0 *3	- *2 - *2			Unused Unused
	R		W	R/W	TMRST*3 TMRUN	Reset 0	Reset Run	Invalid Stop	Clock timer reset (writing) Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3 TM2 TM1 TM0	0 0 0 0			Clock timer data (16 Hz) Clock timer data (32 Hz) Clock timer data (64 Hz) Clock timer data (128 Hz)
	R								
FF7AH	TM7	TM6	TM5	TM4	TM7 TM6 TM5 TM4	0 0 0 0			Clock timer data (1 Hz) Clock timer data (2 Hz) Clock timer data (4 Hz) Clock timer data (8 Hz)
	R								
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3 EIT2 EIT1 EIT0	0 0 0 0	Enable Enable Enable Enable	Mask Mask Mask Mask	Interrupt mask register (Clock timer 1 Hz) Interrupt mask register (Clock timer 2 Hz) Interrupt mask register (Clock timer 8 Hz) Interrupt mask register (Clock timer 32 Hz)
	R/W								
FFF6H	IT3	IT2	IT1	IT0	IT3 IT2 IT1 IT0	0 0 0 0	(R) Yes (W)	(R) No (W)	Interrupt factor flag (Clock timer 1 Hz) Interrupt factor flag (Clock timer 2 Hz) Interrupt factor flag (Clock timer 8 Hz) Interrupt factor flag (Clock timer 32 Hz)
	R/W						Reset	Invalid	

- *1 Initial value at initial reset
- *2 Not set in the circuit
- *3 Constantly "0" when being read

TM0–TM7: Timer data (FF79H, FF7AH)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF79H), the high-order data (FF7AH) is held until reading or for 0.48–1.5 msec (one of shorter of them).

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF78H•D1)

This bit resets the clock timer.

- When "1" is written: Clock timer reset
- When "0" is written: No operation
- Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF78H•D0)

Controls RUN/STOP of the clock timer.

When "1" is written: RUN
 When "0" is written: STOP
 Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written.

In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.

At initial reset, this register is set to "0".

EIT0: 32 Hz interrupt mask register (FFE6H•D0)**EIT1: 8 Hz interrupt mask register (FFE6H•D1)****EIT2: 2 Hz interrupt mask register (FFE6H•D2)****EIT3: 1 Hz interrupt mask register (FFE6H•D3)**

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
 When "0" is written: Masked
 Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz).

At initial reset, these registers are set to "0".

IT0: 32 Hz interrupt factor flag (FFF6H•D0)**IT1: 8 Hz interrupt factor flag (FFF6H•D1)****IT2: 2 Hz interrupt factor flag (FFF6H•D2)****IT3: 1 Hz interrupt factor flag (FFF6H•D3)**

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
 When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
 When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".

4.8.5 Programming notes

- (1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

4.9 Stopwatch Timer

4.9.1 Configuration of stopwatch timer

The E0C63466 has 1/100 sec unit and 1/10 sec unit stopwatch timer built-in. The stopwatch timer is configured with a 2 levels 4-bit BCD counter which has an input clock approximating 100 Hz signal (signal divided from OSC1 to the closest 100 Hz) and data can be read in units of 4 bits by software. Figure 4.9.1.1 shows the configuration of the stopwatch timer.

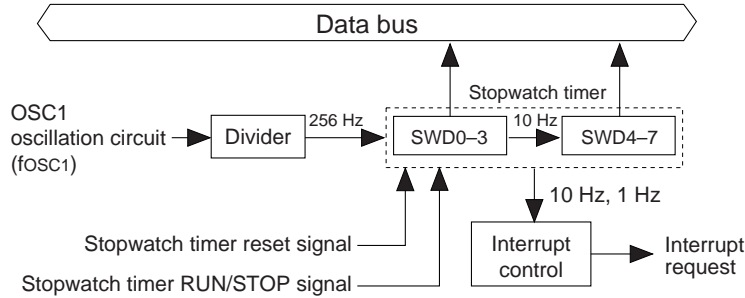


Fig. 4.9.1.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

Note: When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, this timer can not be used for the stopwatch function.

4.9.2 Count-up pattern

The stopwatch timer is configured of 4-bit BCD counters SWD0–SWD3 and SWD4–SWD7. The counter SWD0–SWD3, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWD4–SWD7 has an approximated 10 Hz signal generated by the counter SWD0–SWD3 for the input clock. In count-up every 1/10 sec, and generated 1 Hz signal.

Figure 4.9.2.1 shows the count-up pattern of the stopwatch timer.

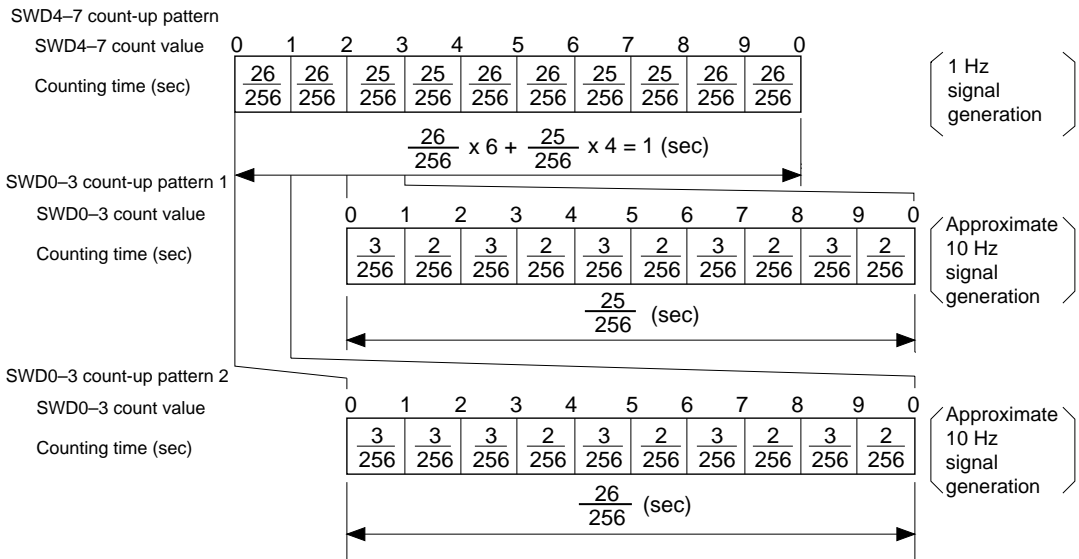


Fig. 4.9.2.1 Count-up pattern of stopwatch timer

SWD0–SWD3 generates an approximated 10 Hz signal from the basic 256 Hz signal (f_{OSC1} dividing clock). The count-up intervals are $2/256$ sec and $3/256$ sec, so that finally two patterns are generated: $25/256$ sec and $26/256$ sec intervals. Consequently, these patterns do not amount to an accurate $1/100$ sec. SWD4–SWD7 counts the approximated 10 Hz signals generated by the $25/256$ sec and $26/256$ sec intervals in the ratio of 4 : 6, to generate a 1 Hz signal. The count-up intervals are $25/256$ sec and $26/256$ sec, which do not amount to an accurate $1/10$ sec.

4.9.3 Interrupt function

The stopwatch timers SWD0–SWD3 and SWD4–SWD7, through their respective overflows, can generate 10 Hz (approximate 10 Hz) and 1 Hz interrupts.

Figure 4.9.3.1 shows the timing chart for the stopwatch timer.

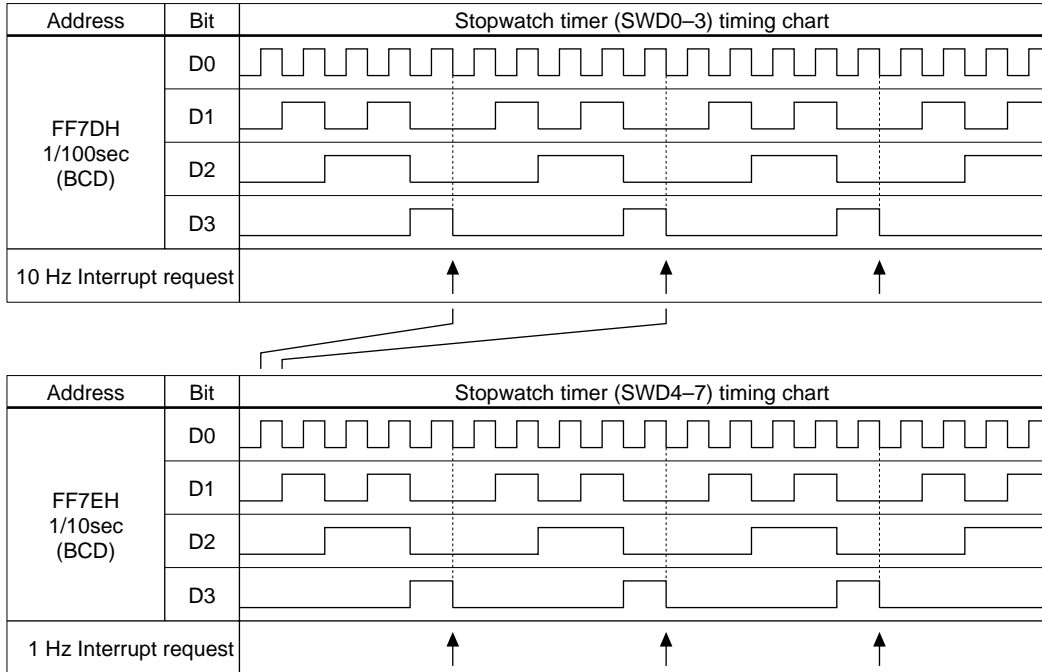


Fig. 4.9.3.1 Timing chart for stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWD0–SWD3 and SWD4–SWD7 (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW10 and ISW1) are set to "1".

The respective interrupts can be masked separately using the interrupt mask registers (EISW10 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

4.9.4 I/O memory of stopwatch timer

Table 4.9.4.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 4.9.4.1 Control bits of stopwatch timer

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF7CH	0	0	SWRST	SWRUN	0 *3 0 *3	- *2 - *2			Unused Unused
	R		W	R/W	SWRST*3 SWRUN	Reset 0	Reset Run	Invalid Stop	Stopwatch timer reset (writing) Stopwatch timer Run/Stop
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3 SWD2 SWD1 SWD0	0 0 0 0			Stopwatch timer data BCD (1/100 sec)
	R								
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7 SWD6 SWD5 SWD4	0 0 0 0			Stopwatch timer data BCD (1/10 sec)
	R								
FFE7H	0	0	EISW1	EISW10	0 *3 0 *3	- *2 - *2			Unused Unused
	R		R/W		EISW1 EISW10	0 0	Enable Enable	Mask Mask	Interrupt mask register (Stopwatch timer 1 Hz) Interrupt mask register (Stopwatch timer 10 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3 0 *3	- *2 - *2	(R) Yes	(R) No	Unused Unused
	R		R/W		ISW1 ISW10	0 0	(W) Reset	(W) Invalid	Interrupt factor flag (Stopwatch timer 1 Hz) Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SWD0–SWD7: Stopwatch timer data (FF7DH, FF7EH)

The 1/100 sec and the 1/10 sec data (BCD) can be read from SWD0–SWD3 and SWD4–SWD7, respectively. These eight bits are read only, and writing operations are invalid.

At initial reset, the timer data is initialized to "00H".

SWRST: Stopwatch timer reset (FF7CH•D1)

When "1" is written: Stopwatch timer reset

When "0" is written: No operation

Reading: Always "0"

The stopwatch timer is reset by writing "1" to SWRST. All timer data is set to "0". When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to SWRST.

This bit is write-only, and so is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP control register (FF7CH•D0)

Controls RUN/STOP of the stopwatch timer.

When "1" is written: RUN

When "0" is written: STOP

Reading: Valid

The stopwatch timer enters the RUN status when "1" is written to the SWRUN register, and the STOP status when "0" is written.

In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.

When data of the counter is read at run mode, proper reading may not be obtained due to the carry from low-order digits (SWD0–SWD3) into high-order digits (SWD4–SWD7) (i.e., in case SWD0–SWD3 and SWD4–SWD7 reading span the timing of the carry). To avoid this occurrence, perform the reading after suspending the counter once and then set the SWRUN to "1" again.

Moreover, it is required that the suspension period not exceed 976 μ sec (1/4 cycle of 256 Hz).

At initial reset, this register is set to "0".

EISW10: 10Hz interrupt mask register (FFE7H•D0)

EISW1: 1Hz interrupt mask register (FFE7H•D1)

These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled

When "0" is written: Masked

Reading: Valid

The interrupt mask registers (EISW10, EISW1) are used to select whether to mask the interrupt to the separate frequencies (10 Hz, 1 Hz).

At initial reset, these registers are set to "0".

ISW10: 10 Hz interrupt factor flag (FFF7H•D0)

ISW1: 1 Hz interrupt factor flag (FFF7H•D1)

These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

The interrupt factor flags ISW10 and ISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively. The software can judge from these flags whether there is a stopwatch timer interrupt.

However, even if the interrupt is masked, the flags are set to "1" by the overflow of the corresponding counters.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".

4.9.5 Programming notes

- (1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 μ sec (1/4 cycle of 256 Hz).
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, this timer can not be used for the stopwatch function.

4.10 Programmable Timer

4.10.1 Configuration of programmable timer

The E0C63466 has two 8-bit programmable timer systems (timer 0 and timer 1) built-in.

Timer 0 and timer 1 are composed of 8-bit presetable down counters and they can be used as 8-bit × 2 channel programmable timers. Timer 0 also has an event counter function using the K13 input port terminal.

Figure 4.10.1.1 shows the configuration of the programmable timer.

The programmable timer is designed to count down from the initial value set in the counter with software. An underflow according to the initial value occurs by counting down and is used for the following functions:

- Presetting the initial value to the counter to generate the periodical underflow signal
- Generating an interrupt
- Generating a TOUT signal output from the R02 output port terminal
- Generating the synchronous clock source for the serial interface (timer 1 underflow is used, and it is possible to set the transfer rate)

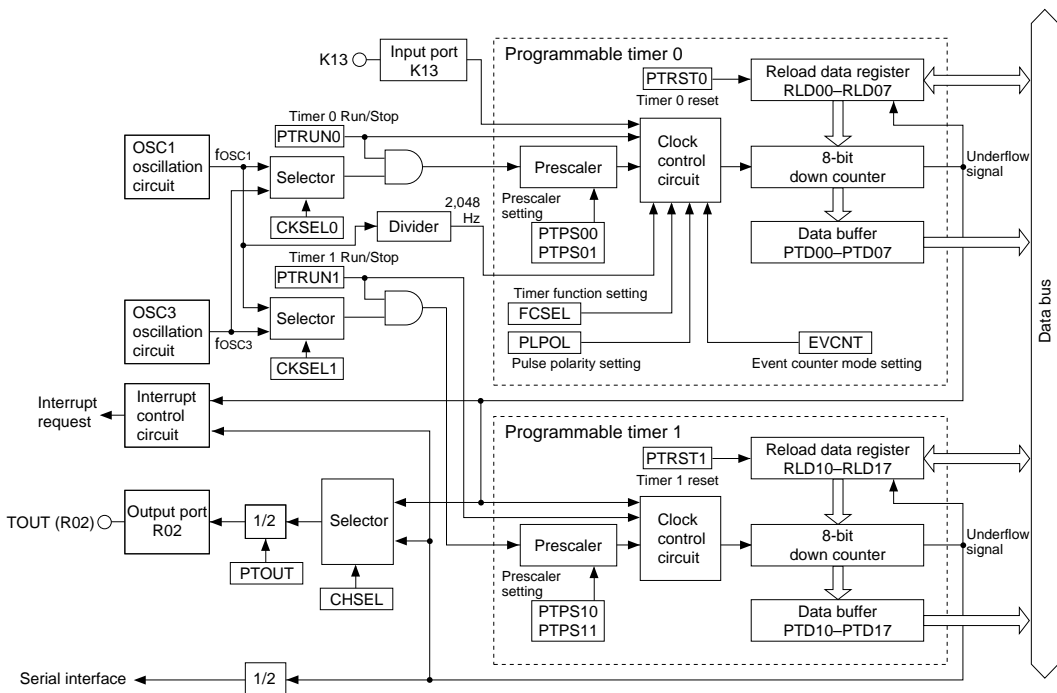


Fig. 4.10.1.1 Configuration of programmable timer

4.10.2 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.

By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The registers PTRUN0 (timer 0) and PTRUN1 (timer 1) are provided to control the RUN/STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.

In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

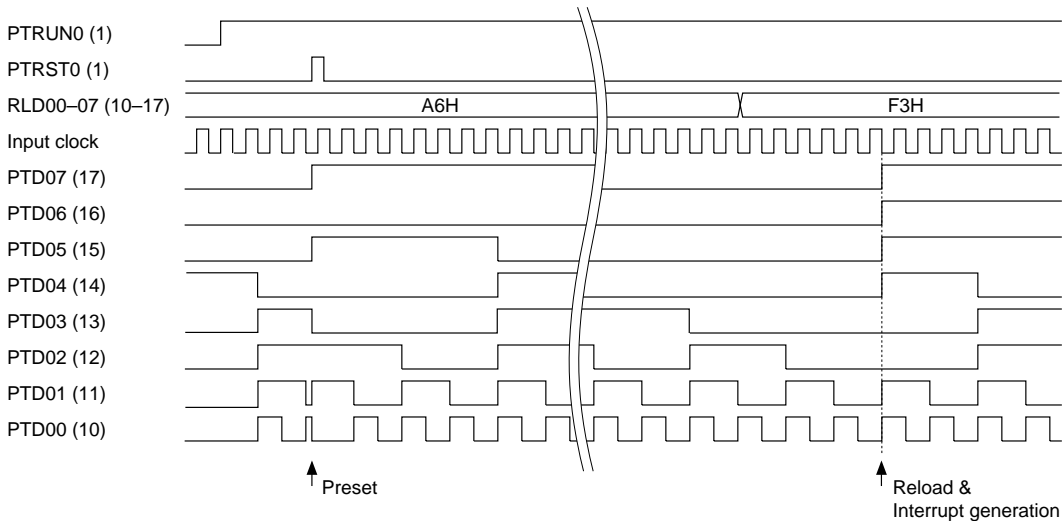


Fig. 4.10.2.1 Basic operation timing of down counter

4.10.3 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source. Timer 0 can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", timer 0 operates in the timer mode.

Timer 1 operates only in the timer mode.

At initial reset, this mode is set.

Refer to Section 4.10.2, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The timer 0 has an event counter function that counts an external clock input to the input port K13. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT. The timer 1 operates only in the timer mode, and cannot be used as an event counter.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.10.3.1.

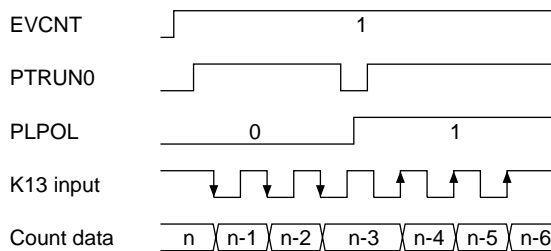


Fig. 4.10.3.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K13 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.

When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec* or more to count reliably. The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less. (*: $f_{OSC1} = 32.768 \text{ kHz}$).

Figure 4.10.3.2 shows the count down timing with noise rejecter.

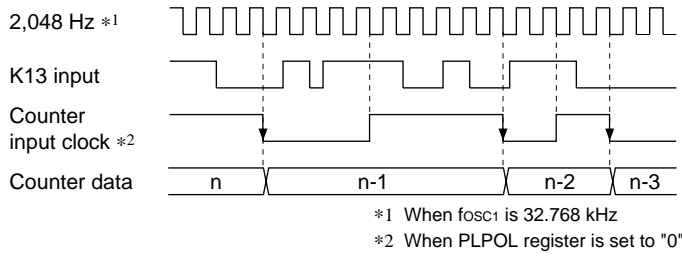


Fig. 4.10.3.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K13 input as the clock.

Refer to Section 4.10.2, "Setting of initial value and counting down" for basic operation and control.

4.10.4 Setting of input clock in timer mode

Timer 0 and timer 1 each include a prescaler. The prescalers generate the input clock for each timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.

The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for timer 0 and timer 1 individually.

The set input clock is used for the count clock during operation in the timer mode. When the timer 0 is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection registers CKSEL0 (timer 0) and CKSEL1 (timer 1); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.

When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.

At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00/PTPSC01 (timer 0) and PTPS10/PTPS11 (timer 1). Table 4.10.4.1 shows the correspondence between the setting value and the division ratio.

Table 4.10.4.1 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0) or PTRUN1 (timer 1), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.10.5 Interrupt function

The programmable timer can generate an interrupt due to an underflow of the timer 0 and timer 1. See Figure 4.10.2.1 for the interrupt timing.

An underflow of timer 0 and timer 1 sets the corresponding interrupt factor flag IPT0 (timer 0) or IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT0 (timer 0) or EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.10.6 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of timer 0 or timer 1. The TOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the TOUT output channel selection register CHSEL. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected.

Figure 4.10.6.1 shows the TOUT signal waveform when the channel is changed.

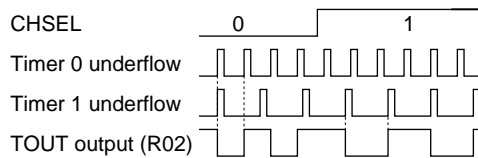


Fig. 4.10.6.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R02 output port terminal. Programmable clocks can be supplied to external devices.

Figure 4.10.6.2 shows the configuration of the output port R02.

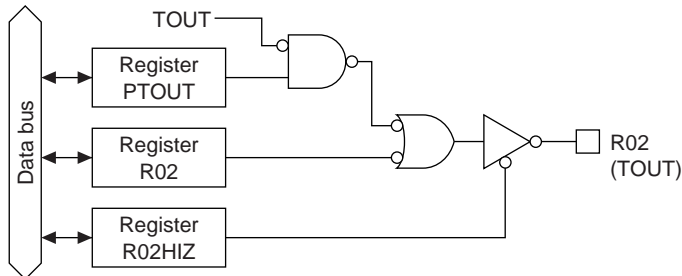


Fig. 4.10.6.2 Configuration of R02

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R02 output port terminal and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

Figure 4.10.6.3 shows the output waveform of the TOUT signal.

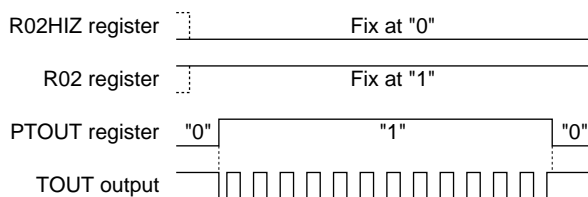


Fig. 4.10.6.3 Output waveform of the TOUT signal

4.10.7 Transfer rate setting for serial interface

The signal that is made from underflows of timer 1 by dividing them in 1/2, can be used as the clock source for the serial interface.

The programmable timer outputs the clock to the serial interface by setting timer 1 into RUN state (PTRUN = "1"). It is not necessary to control with the PTOUT register.

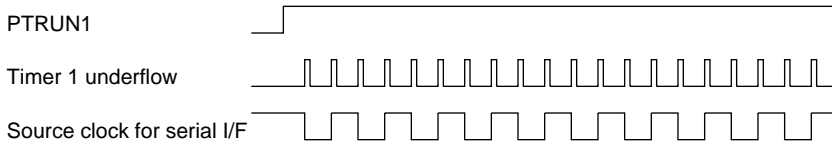


Fig. 4.10.7.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

$$RLD1X = fosc / (2 * bps * \text{division ratio of the prescaler}) - 1$$

fosc: Oscillation frequency (OSC1/OSC3)

bps: Transfer rate

(00H can be set to RLD1X)

Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source.

4.10.8 I/O memory of programmable timer

Table 4.10.8.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.10.8.1 Control bits of programmable timer

Address	Register								Comment	
	D3	D2	D1	D0	Name	Init *1	1	0		
FFC0H	0	EVCNT	FCSEL	PLPOL	EVCNT	0	Event ct.	Timer	Unused Timer 0 counter mode selection	
	R	R/W			FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)	
		R/W			PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)	
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection	
	R/W				PTOUT	0	On	Off	TOUT output control	
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection	
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0	Reset	Invalid] Prescaler 0 division ratio selection Division ratio	
	R/W		W	R/W	PTPS00	0				0 1 2 3
	R/W		W	R/W	PTPS0*3	- *2				1/1 1/4 1/32 1/256
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0	Reset	Invalid] Prescaler 1 division ratio selection Division ratio	
	R/W		W	R/W	PTPS10	0				0 1 2 3
	R/W		W	R/W	PTPS1*3	- *2				1/1 1/4 1/32 1/256
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0	Run	Stop] MSB Programmable timer 0 reload data (low-order 4 bits)] LSB	
	R/W				RLD02	0				
	R/W				RLD01	0				
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0	Run	Stop] MSB Programmable timer 0 reload data (high-order 4 bits)] LSB	
	R/W				RLD06	0				
	R/W				RLD05	0				
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0	Run	Stop] MSB Programmable timer 1 reload data (low-order 4 bits)] LSB	
	R/W				RLD12	0				
	R/W				RLD11	0				
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0	Run	Stop] MSB Programmable timer 1 reload data (high-order 4 bits)] LSB	
	R/W				RLD16	0				
	R/W				RLD15	0				
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0	Run	Stop] MSB Programmable timer 0 data (low-order 4 bits)] LSB	
	R				PTD02	0				
	R				PTD01	0				
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0	Run	Stop] MSB Programmable timer 0 data (high-order 4 bits)] LSB	
	R				PTD06	0				
	R				PTD05	0				
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0	Run	Stop] MSB Programmable timer 1 data (low-order 4 bits)] LSB	
	R				PTD12	0				
	R				PTD11	0				
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0	Run	Stop] MSB Programmable timer 1 data (high-order 4 bits)] LSB	
	R				PTD16	0				
	R				PTD15	0				
FFE2H	0	0	EIPT1	EIPT0	0 *3	- *2	Enable	Mask	Unused Unused Interrupt mask register (Programmable timer 1) Interrupt mask register (Programmable timer 0)	
	R		R/W		EIPT1	0				
	R		R/W		EIPT0	0				
FFF2H	0	0	IPT1	IPT0	0 *3	- *2	(R)	(R)	Unused Unused Interrupt factor flag (Programmable timer 1) Interrupt factor flag (Programmable timer 0)	
	R		R/W		0 *3	- *2				
	R		R/W		IPT1	0				
R		R/W		IPT0	0	(W)	(W)	Reset	Invalid	

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC1H•D0)

CKSEL1: Prescaler 1 source clock selection register (FFC1H•D1)

Selects the source clock of the prescaler.

- When "1" is written: OSC3 clock
- When "0" is written: OSC1 clock
- Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSEL0 register, the OSC1 clock is selected as the input clock for the prescaler 0 (for timer 0) and when "1" is written, the OSC3 clock is selected.

Same as above, the source clock for prescaler 1 is selected by the CKSEL1 register.

When the event counter mode is selected to timer 0, the setting of the CKSEL0 register becomes invalid.

At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC2H•D2, D3)

PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC3H•D2, D3)

Selects the division ratio of the prescaler.

Two bits of PSC00 and PSC01 are the prescaler division ratio selection register for timer 0, and two bits of PSC10 and PSC11 are for timer 1. The prescaler division ratios that can be set by these registers are shown in Table 4.10.8.2.

Table 4.10.8.2 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of the PTPS00 and PTPS01 becomes invalid.

At initial reset, these registers are set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)

Selects a counter mode for timer 0.

- When "1" is written: Event counter mode
- When "0" is written: Timer mode
- Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.

At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejector

When "0" is written: Without noise rejector

Reading: Valid

When "1" is written to the FCSEL register, the noise rejector is used and counting is done by an external clock (K13) with 0.98 msec* or more pulse width. The noise rejector allows the counter to input the clock at the second falling edge of the internal 2,048 Hz* signal after changing the input level of the K13 input port terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec* or less. (*: $f_{OSC1} = 32.768 \text{ kHz}$).

When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K13 input port terminal.

Setting of this register is effective only when timer 0 is used in the event counter mode.

At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge

When "0" is written: Falling edge

Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K10 input port terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.

Setting of this register is effective only when timer 0 is used in the event counter mode.

At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC4H, FFC5H)**RLD10–RLD17: Timer 1 reload data register (FFC6H, FFC7H)**

Sets the initial value for the counter.

The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.

Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRST0 or PTRST1 register, or when counter underflow occurs.

At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFC8H, FFC9H)**PTD10–PTD17: Timer 1 counter data (FFCAH, FFCBH)**

Count data in the programmable timer can be read from these latches.

The low-order 4 bits of the count data in timer 0 can be read from PTD00–PTD03, and the high-order data can be read from PTD04–PTD07. Similarly, for timer 1, the low-order 4 bits can be read from PTD10–PTD13, and the high-order data can be read from PTD14–PTD17.

Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.

Since these latches are exclusively for reading, the writing operation is invalid.

At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC2H•D1)

PTRST1: Timer 1 reset (reload) (FFC3H•D1)

Resets the timer and presets reload data to the counter.

When "1" is written: Reset

When "0" is written: No operation

Reading: Always "0"

By writing "1" to PTRST0, the reload data in the reload register PLD00–PLD07 is preset to the counter in timer 0. Similarly, the reload data in PLD10–PLD17 is preset to the counter in timer 1 by PTRST1.

When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.

No operation results when "0" is written.

Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC2H•D0)

PTRUN1: Timer 1 RUN/STOP control register (FFC3H•D0)

Controls the RUN/STOP of the counter.

When "1" is written: RUN

When "0" is written: STOP

Reading: Valid

The counter in timer 0 starts counting down by writing "1" to the PTRUN0 register and stops by writing "0".

In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.

Same as above, the timer 1 counter is controlled by the PTRUN1 register.

At initial reset, these registers are set to "0".

CHSEL: TOUT output channel selection register (FFC1H•D3)

Selects the channel used for TOUT signal output.

When "1" is written: Timer 1

When "0" is written: Timer 0

Reading: Valid

This register selects which timer's underflow (timer 0 or timer 1) is used to generate a TOUT signal. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected.

At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)

Turns TOUT signal output ON and OFF.

When "1" is written: ON

When "0" is written: OFF

Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the output port terminal R02 and when "0" is written, the terminal goes to a high (VDD) level. However, the data register R02 must always be "1" and the high impedance control register R02HIZ must always be "0" (data output state).

At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE2H•D0)**EIPT1: Timer 1 interrupt mask register (FFE2H•D1)**

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled

When "0" is written: Masked

Reading: Valid

Timer 0 and timer 1 interrupts can be masked individually by the interrupt mask registers EIPT0 (timer 0) and EIPT1 (timer 1).

At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF2H•D0)**IPT1: Timer 1 interrupt factor flag (FFF2H•D1)**

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred

When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset

When "0" is written: Invalid

The interrupt factor flags IPT0 and IPT1 correspond to timer 0 and timer 1 interrupts, respectively. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.

These flags are reset to "0" by writing "1" to them.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, these flags are set to "0".

4.10.9 Programming notes

- (1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec (when fOSC1 is 32.768 kHz) of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).
- (2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops.

Figure 4.10.9.1 shows the timing chart for the RUN/STOP control.

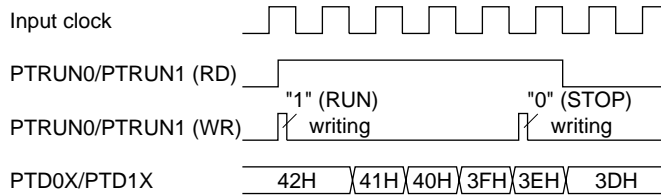


Fig. 4.10.9.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

- (3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
- (4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the OFF state.
- (5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.11 Serial Interface (\overline{SIN} , \overline{SOUT} , \overline{SCLK} , \overline{SRDY})

4.11.1 Configuration of serial interface

The E0C63466 has a synchronous clock type 8 bits serial interface built-in.

The configuration of the serial interface is shown in Figure 4.11.1.1.

The CPU, via the 8-bit shift register, can read the serial input data from the \overline{SIN} terminal. Moreover, via the same 8-bit shift register, it can convert parallel data to serial data and output it to the \overline{SOUT} terminal. The synchronous clock for serial data input/output may be set by selecting by software any one of three types of master mode (internal clock mode: when the E0C63466 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C63466 is to be the slave for serial input/output).

Also, when the serial interface is used at slave mode, \overline{SRDY} signal which indicates whether or not the serial interface is available to transmit or receive can be output to the \overline{SRDY} terminal.

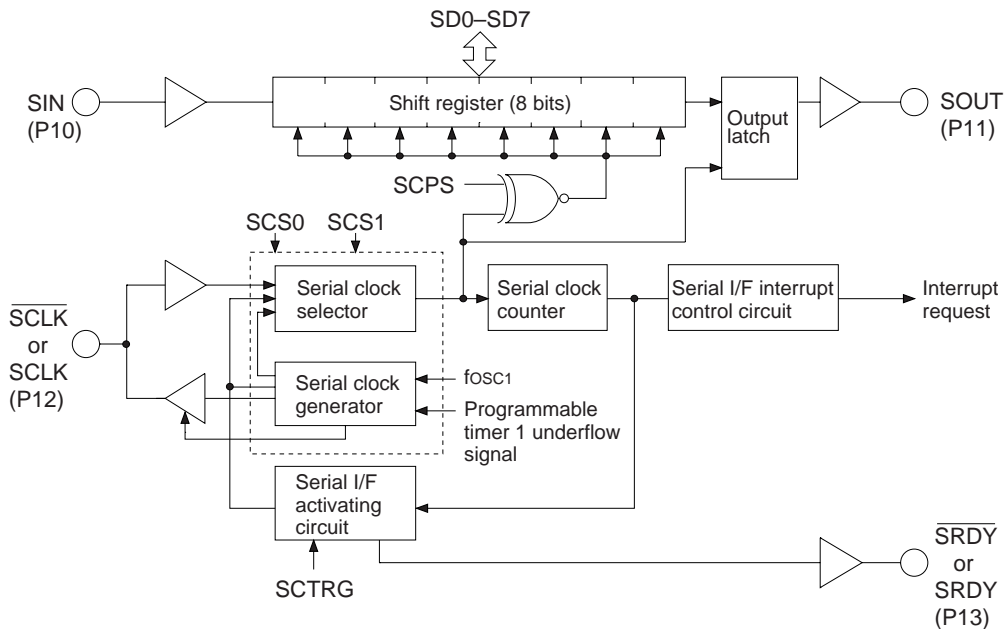


Fig. 4.11.1.1 Configuration of serial interface

The input/output ports of the serial interface are shared with the I/O ports P10–P13, and function of these ports can be selected through the software.

P10–P13 terminals and serial input/output correspondence are as follows:

<u>Master mode</u>	<u>Slave mode</u>
P10 = \overline{SIN} (I)	P10 = \overline{SIN} (I)
P11 = \overline{SOUT} (O)	P11 = \overline{SOUT} (O)
P12 = \overline{SCLK} (O)	P12 = \overline{SCLK} (I)
P13 = I/O port (I/O)	P13 = \overline{SRDY} (O)

Note: At initial reset, P10–P13 are set to I/O ports.

When using the serial interface, switch the function (ESIF = "1") in the initial routine.

4.11.2 Mask option

(1) Terminal specification

Since the input/output terminals of the serial interface is shared with the I/O ports (P10–P13), the mask option that selects the output specification for the I/O port is also applied to the serial interface. The output specification of the terminals SOUT, $\overline{\text{SCLK}}$ (during the master mode) and SRDY (during the slave mode) that are used as output in the input/output port of the serial interface is respectively selected by the mask options of P11, P12 and P13. Either complementary output or N-channel open drain output can be selected as the output specification. However, when N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the terminal.

Furthermore, the pull-up resistor for the SIN terminal and the $\overline{\text{SCLK}}$ terminal (during slave mode) that are used as input terminals can be selected by the mask options of P10 and P12. When "without pull-up" is selected, take care that the floating status does not occur.

(2) Polarity of synchronous clock and ready signal

Polarity of the synchronous clock and the ready signal that is output in the slave mode can be selected from either positive polarity (high active, SCLK & SRDY) or negative polarity (low active, $\overline{\text{SCLK}}$ & $\overline{\text{SRDY}}$).

When operating the serial interface in the slave mode, the synchronous clock is input from an external device. Be aware that the terminal specification is pull-up only and a pull-down resistor cannot be built in if positive polarity is selected.

In the following explanation, it is assumed that negative polarity ($\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$) has been selected.

4.11.3 Master mode and slave mode of serial interface

The serial interface of the E0C63466 has two types of operation mode: master mode and slave mode.

The master mode uses an internal clock as the synchronous clock for the built-in shift register, and outputs this internal clock from the $\overline{\text{SCLK}}$ (P12) terminal to control the external (slave side) serial device.

In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{\text{SCLK}}$ (P12) terminal and it is used as the synchronous clock for the built-in shift register.

The master mode and slave mode are selected by writing data to the SCS1 and SCS0 registers.

When the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 4.11.3.1.

Table 4.11.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	OSC1
1	0		OSC1 /2
0	1		Programmable timer *
0	0	Slave mode	External clock *

* The maximum clock is limited to 1 MHz.

When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.10, "Programmable Timer" for the control of the programmable timer.

At initial reset, the slave mode (external clock mode) is selected.

Moreover, the synchronous clock, along with the input/output of the 8-bit serial data, is controlled as follows:

- In the master mode, after output of 8 clocks from the $\overline{\text{SCLK}}$ (P12) terminal, clock output is automatically suspended and the $\overline{\text{SCLK}}$ (P12) terminal is fixed at high level.
- In the slave mode, after input of 8 clocks to the $\overline{\text{SCLK}}$ (P12) terminal, subsequent clock inputs are masked.

A sample basic serial input/output portion connection is shown in Figure 4.11.3.1.

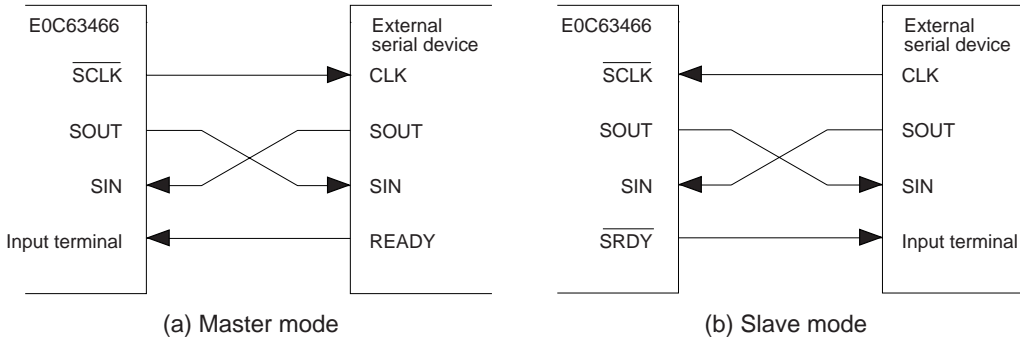


Fig. 4.11.3.1 Sample basic connection of serial input/output section

4.11.4 Data input/output and interrupt function

The serial interface of E0C63466 can input/output data via the internal 8-bit shift register. The shift register operates by synchronizing with either the synchronous clock output from the $\overline{\text{SCLK}}$ (P12) terminal (master mode), or the synchronous clock input to the $\overline{\text{SCLK}}$ (P12) terminal (slave mode). The serial interface generates an interrupt on completion of the 8-bit serial data input/output. Detection of serial data input/output is done by counting of the synchronous clock $\overline{\text{SCLK}}$; the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates an interrupt.

The serial data input/output procedure is explained below:

(1) Serial data output procedure and interrupt

The E0C63466 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to the data registers SD0–SD3 (FF72H) and SD4–SD7 (FF73H) and writing "1" to SCTR_G bit (FF70H•D1), it synchronizes with the synchronous clock and the serial data is output to the SOUT (P11) terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ (P12) terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ (P12) terminal.

Shift timing of serial data is as follows:

- **When negative polarity is selected for the synchronous clock (mask option):**

The serial data output to the SOUT (P11) terminal changes at the falling edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P12) terminal. The data in the shift register is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register (FF71H•D2) is "1" and is shifted at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0".

- **When positive polarity is selected for the synchronous clock (mask option):**

The serial data output to the SOUT (P11) terminal changes at the rising edge of the clock input or output from/to the $\overline{\text{SCLK}}$ (P12) terminal. The data in the shift register is shifted at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "1" and is shifted at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0".

When the output of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF (FFF3H•D0) is set to "1" and an interrupt occurs. Moreover, the interrupt can be masked by the interrupt mask register EISIF (FFE3H•D0). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after output of the 8-bit data.

(2) Serial data input procedure and interrupt

The E0C63466 serial interface is capable of inputting serial data as parallel data, in units of 8 bits.

The serial data is input from the SIN (P10) terminal, synchronizes with the synchronous clock, and is sequentially read in the 8-bit shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ (P12) terminal while in the slave mode, external clock which is input from the SCLK (P12) terminal.

Shift timing of serial data is as follows:

- **When negative polarity is selected for the synchronous clock (mask option):**

The serial data is read into the built-in shift register at the falling edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "1" and is read at the rising edge of the $\overline{\text{SCLK}}$ signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

- **When positive polarity is selected for the synchronous clock (mask option):**

The serial data is read into the built-in shift register at the rising edge of the SCLK signal when the SCPS register is "1" and is read at the falling edge of the SCLK signal when the SCPS register is "0". The shift register is sequentially shifted as the data is fetched.

When the input of the 8-bit data from SD0 to SD7 is completed, the interrupt factor flag ISIF is set to "1" and an interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIF. However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" after input of the 8-bit data.

The data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The E0C63466 allows the input/output permutation of serial data to be selected by the SDP register (FF71H•D3) as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 4.11.4.1. The SDP register should be set before setting data to SD0–SD7.

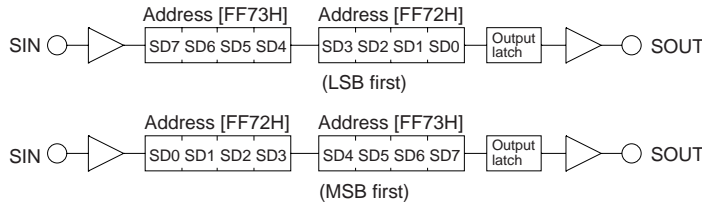


Fig. 4.11.4.1 Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

When the E0C63466 serial interface is used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ signal is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{\text{SRDY}}$ signal is output from the $\overline{\text{SRDY}}$ (P13) terminal.

Output timing of $\overline{\text{SRDY}}$ signal is as follows:

- **When negative polarity is selected (mask option):**

$\overline{\text{SRDY}}$ signal goes "0" (low) when the E0C63466 serial interface is available to transmit or receive data; normally, it is at "1" (high).

$\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRГ and returns from "0" to "1" when "0" is input to the $\overline{\text{SCLK}}$ (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

- **When positive polarity is selected (mask option):**

SRDY signal goes "1" (high) when the E0C63466 serial interface is available to transmit or receive data; normally, it is at "0" (low).

SRDY signal changes from "0" to "1" immediately after "1" is written to SCTRГ and returns from "1" to "0" when "1" is input to the SCLK (P12) terminal (i.e., when the serial input/output begins transmitting or receiving data). Moreover, when high-order data is read from or written to SD4–SD7, the SRDY signal returns to "0".

(5) Timing chart

The E0C63466 serial interface timing charts are shown in Figures 4.11.4.2 and 4.11.4.3.

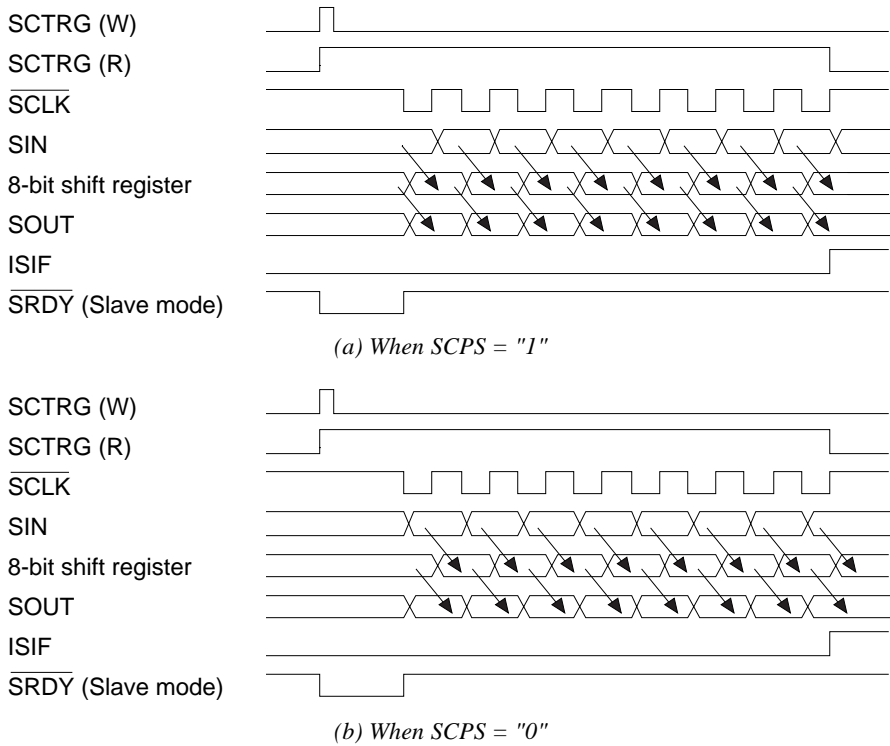


Fig. 4.11.4.2 Serial interface timing chart (when synchronous clock is negative polarity \overline{SCLK})

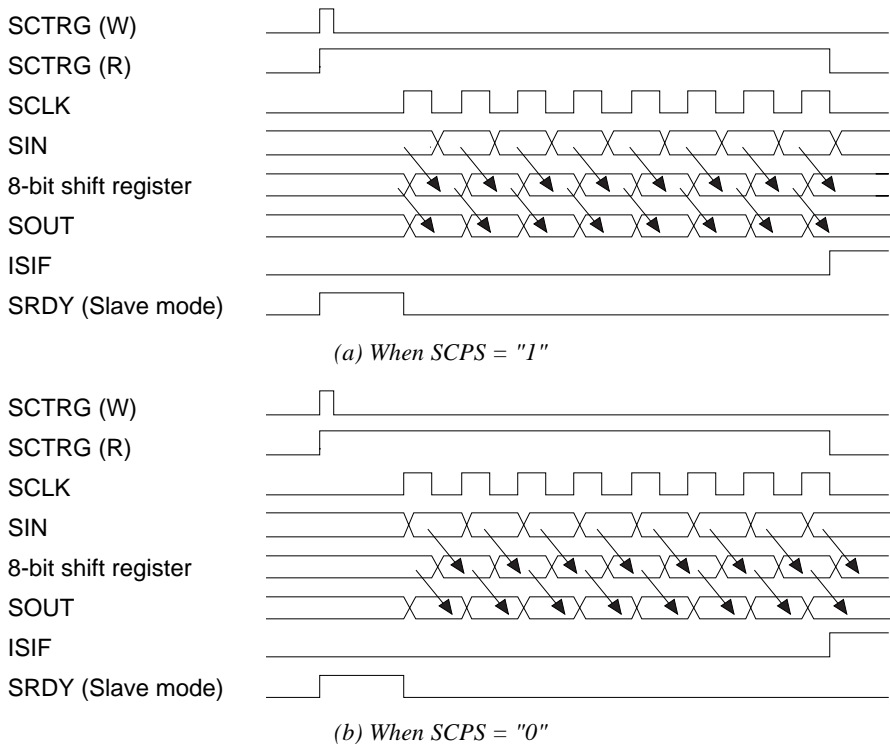


Fig. 4.11.4.3 Serial interface timing chart (when synchronous clock is positive polarity SCLK)

4.11.5 I/O memory of serial interface

Table 4.11.5.1 shows the I/O addresses and the control bits for the serial interface.

Table 4.11.5.1 Control bits of serial interface

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected P12 pull-up control register (EISF=0) functions as a general-purpose register when SIF (master) is selected SCLK (I) pull-up control register when SIF (slave) is selected P11 pull-up control register (EISF=0) functions as a general-purpose register when SIF is selected P10 pull-up control register (EISF=0) SIN pull-up control register when SIF is selected
					PUL12	1	On	Off	
	R/W				PUL11	1	On	Off	
	R/W				PUL10	1	On	Off	
FF70H	0	0	SCTRG	ESIF	0 *3	- *2			Unused Unused Serial I/F clock trigger (writing) Serial I/F clock status (reading) Serial I/F enable (P1 port function selection)
	R		R/W		SCTRG	0	Trigger Run	Invalid Stop	
	R		R/W		ESIF	0	SIF	I/O	
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation Serial I/F clock phase selection -Negative polarity (mask option) -Positive polarity (mask option) Serial I/F clock mode selection [SCS1, 0] 0 1 Clock Slave PT [SCS1, 0] 2 3 Clock OSC1/2 OSC1
	R/W				SCPS	0			
	R/W				SCS1	0			
	R/W				SCS0	0			
FF72H	SD3	SD2	SD1	SD0	SD3	- *2	High	Low	MSB Serial I/F transmit/receive data (low-order 4 bits) LSB
	R/W				SD2	- *2	High	Low	
	R/W				SD1	- *2	High	Low	
	R/W				SD0	- *2	High	Low	
FF73H	SD7	SD6	SD5	SD4	SD7	- *2	High	Low	MSB Serial I/F transmit/receive data (high-order 4 bits) LSB
	R/W				SD6	- *2	High	Low	
	R/W				SD5	- *2	High	Low	
	R/W				SD4	- *2	High	Low	
FFE3H	0	0	0	EISIF	0 *3	- *2			Unused Unused Unused Interrupt mask register (Serial I/F)
	R			R/W	0 *3	- *2			
	R			R/W	EISIF	0	Enable	Mask	
FFF3H	0	0	0	ISIF	0 *3	- *2	(R)	(R)	Unused Unused Unused Interrupt factor flag (Serial I/F)
	R			R/W	0 *3	- *2	Yes	No	
	R			R/W	ISIF	0	Reset	Invalid	

- *1 Initial value at initial reset
- *2 Not set in the circuit
- *3 Constantly "0" when being read

ESIF: Serial interface enable register (P1 port function selection) (FF70H•D0)

Sets P10–P13 to the input/output port for the serial interface.

When "1" is written: Serial interface
 When "0" is written: I/O port
 Reading: Valid

When "1" is written to the ESIF register, P10, P11, P12 and P13 function as SIN, SOUT, SCLK, SRDY, respectively.

In the slave mode, the P13 terminal functions as SRDY output terminal, while in the master mode, it functions as the I/O port terminal.

At initial reset, this register is set to "0".

PUL10: SIN (P10) pull-up control register (FF45H•D0)**PUL12: SCLK (P12) pull-up control register (FF45H•D2)**

Sets the pull-up of the SIN terminal and the $\overline{\text{SCLK}}$ terminals (in the slave mode).

When "1" is written: Pull-up ON

When "0" is written: Pull-up OFF

Reading: Valid

Sets the pull-up resistor built into the SIN (P10) and $\overline{\text{SCLK}}$ (P12) terminals to ON or OFF. (Pull-up resistor is only built in the port selected by mask option.)

$\overline{\text{SCLK}}$ pull-up is effective only in the slave mode. In the master mode, the PUL12 register can be used as a general purpose register.

At initial reset, these registers are set to "1" and pull-up goes ON.

SCS1, SCS0: Clock mode selection register (FF71H•D0, D1)

Selects the synchronous clock ($\overline{\text{SCLK}}$) for the serial interface.

Table 4.11.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1		OSC1
1	0	Master mode	OSC1 /2
0	1		Programmable timer *
0	0	Slave mode	External clock *

* The maximum clock is limited to 1 MHz.

Synchronous clock ($\overline{\text{SCLK}}$) is selected from among the above 4 types: 3 types of internal clock and external clock.

When the programmable timer is selected, the signal that is generated by dividing the underflow signal of the programmable timer (timer 1) in 1/2 is used as the synchronous clock. In this case, the programmable timer must be controlled before operating the serial interface. Refer to Section 4.10, "Programmable Timer" for the control of the programmable timer.

At initial reset, external clock is selected.

SCPS: Clock phase selection register (FF71H•D2)

Selects the timing for reading in the serial data input from the SIN (P10) terminal.

- **When negative polarity is selected:**

When "1" is written: Falling edge of $\overline{\text{SCLK}}$

When "0" is written: Rising edge of $\overline{\text{SCLK}}$

Reading: Valid

- **When positive polarity is selected:**

When "1" is written: Rising edge of SCLK

When "0" is written: Falling edge of SCLK

Reading: Valid

Select whether the fetching for the serial input data to registers (SD0–SD7) at the rising edge or falling edge of the synchronous signal.

Pay attention to the polarity of the synchronous clock selected by the mask option because the selection content is different.

The input data fetch timing may be selected but output timing for output data is fixed at the falling edge of SCLK (when negative polarity is selected) or at the rising edge of SCLK (when positive polarity is selected).

At initial reset, this register is set to "0".

SDP: Data input/output permutation selection register (FF71H•D3)

Selects the serial data input/output permutation.

- When "1" is written: MSB first
- When "0" is written: LSB first
- Reading: Valid

Select whether the data input/output permutation will be MSB first or LSB first. At initial reset, this register is set to "0".

SCTRG: Clock trigger/status (FF70H•D1)

This is a trigger to start input/output of synchronous clock ($\overline{\text{SCLK}}$).

• When writing

- When "1" is written: Trigger
- When "0" is written: No operation

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{\text{SCLK}}$) input/output is started.

As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.

Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning.

Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

• When reading

- When "1" is read: RUN (during input/output the synchronous clock)
- When "0" is read: STOP (the synchronous clock stops)
- Writing: Invalid

When this bit is read, it indicates the status of serial interface clock.

After "1" is written to SCTRG, this value is latched till serial interface clock stops (8 clock counts). Therefore, if "1" is read, it indicates that the synchronous clock is in input/output operation.

When the synchronous clock input/output is completed, this latch is reset to "0".

At initial reset, this bit is set to "0".

SD0–SD3, SD4–SD7: Serial interface data register (FF72H, FF73H)

These registers are used for writing and reading serial data.

• When writing

- When "1" is written: High level
- When "0" is written: Low level

Write data to be output in these registers. The register data is converted into serial data and output from the SOUT (P11) terminal; data bits set at "1" are output as high (V_{DD}) level and data bits set at "0" are output as low (V_{SS}) level.

• When reading

- When "1" is read: High level
- When "0" is read: Low level

The serial data input from the SIN (P10) terminal can be read from these registers.

The serial data input from the SIN (P10) terminal is converted into parallel data, as a high (V_{DD}) level bit into "1" and as a low (V_{SS}) level bit into "0", and is loaded to these registers. Perform data reading only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).

At initial reset, these registers are undefined.

EISIF: Interrupt mask register (FFE3H•D0)

Masking the interrupt of the serial interface can be selected with this register.

When "1" is written: Enabled
 When "0" is written: Masked
 Reading: Valid

With this register, it is possible to select whether the serial interface interrupt is to be masked or not. At initial reset, this register is set to "0".

ISIF: Interrupt factor flag (FFF3H•D0)

This flag indicates the occurrence of serial interface interrupt.

When "1" is read: Interrupt has occurred
 When "0" is read: Interrupt has not occurred
 Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt.

This flag is set to "1" after an 8-bit data input/output even if the interrupt is masked.

This flag is reset to "0" by writing "1" to it.

After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

At initial reset, this flag is set to "0".

4.11.6 Programming notes

- (1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is not running (i.e., the synchronous clock is neither being input or output).
- (2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTR. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before setting the trigger.
 Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock \overline{SCLK} is external clock, start to input the external clock after the trigger.
- (3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.
- (4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.
- (5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.12 Sound Generator

4.12.1 Configuration of sound generator

The E0C63466 has a built-in sound generator for generating buzzer signals. Hence, generated buzzer signals (BZ) can be output from the BZ terminal. Aside permitting the respective setting of the buzzer signal frequency and sound level to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds. Figure 4.12.1.1 shows the configuration of the sound generator.

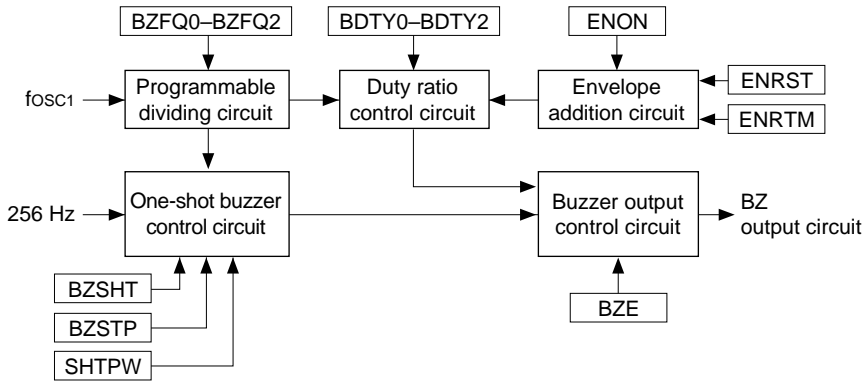


Fig. 4.12.1.1 Configuration of sound generator

Note: The buzzer signal is generated by dividing the OSC1 oscillation clock. Since the frequencies and times that are described in this section are the values in the case of crystal oscillation (32.768 kHz, Typ.), they differ when CR oscillation (60 kHz, Typ.) is selected.

4.12.2 Mask option

Polarity of the BZ signal output from the BZ terminal can be selected as either positive polarity or negative polarity by mask option. Figure 4.12.2.1 shows each output circuit configuration and the output waveform.

When positive polarity is selected, the BZ terminal goes to a low (Vss) level when the BZ signal is OFF. Select positive polarity when driving a piezo buzzer by externally connecting an NPN transistor. When negative polarity is selected, the BZ terminal goes to a high (VDD) level when the BZ signal is OFF. Select negative polarity when driving a piezo buzzer by externally connecting a PNP transistor.

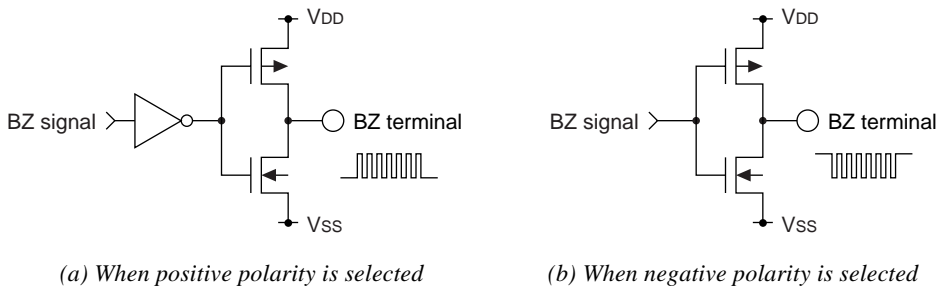


Fig. 4.12.2.1 Configuration of output circuit

4.12.3 Control of buzzer output

The BZ signal generated by the sound generator is output from the BZ terminal by setting "1" for the buzzer output enable register BZE. When "0" is set to BZE register, the output terminal shifts to the low (Vss) level (negative polarity) or high (VDD) level (positive polarity).

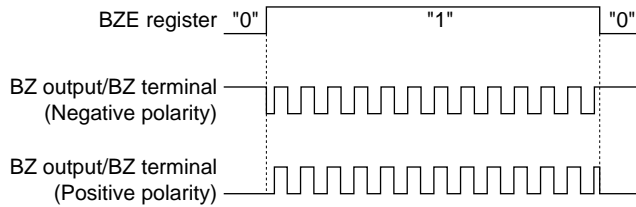


Fig. 4.12.3.1 Buzzer signal output timing chart

Note: Since it generates a BZ signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZE register.

4.12.4 Setting of buzzer frequency and sound level

The divided signal of the OSC1 oscillation clock (32.768 kHz) is used for the buzzer (BZ) signal and it is set up such that 8 types of frequencies can be selected by changing this division ratio. Frequency selection is done by setting the buzzer frequency selection registers BZFQ0–BZFQ2 as shown in Table 4.12.4.1.

Table 4.12.4.1 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer sound level is changed by controlling the duty ratio of the buzzer signal.

The duty ratio can be selected from among the 8 types shown in Table 4.12.4.2 according to the setting of the buzzer duty selection registers BDTY0–BDTY2.

Table 4.12.4.2 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

When the HIGH level output time has been made TH and when the LOW level output time has been made TL due to the ratio of the pulse width to the pulse synchronization, the duty ratio becomes $TL/(TH+TL)$ for negative polarity or $TH/(TH+TL)$ for positive polarity.

When BDTY0–BDTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum. Conversely, when BDTY0–BDTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.

The duty ratio that can be set is different depending on the frequency that has been set, so see Table 4.12.4.2.

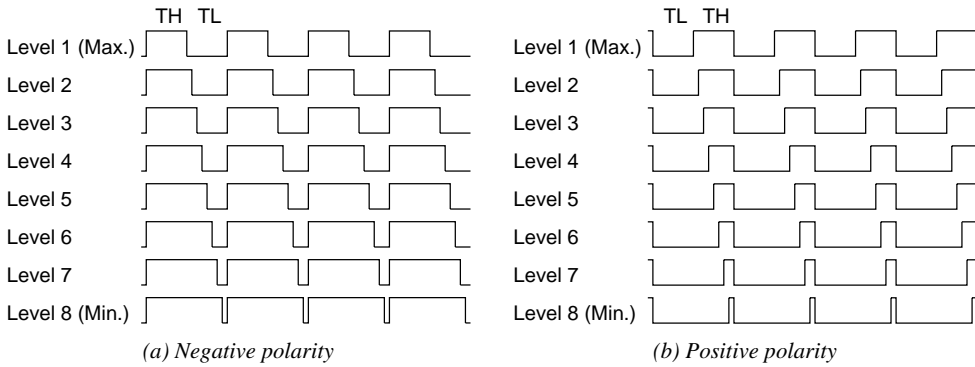


Fig. 4.12.4.1 Duty ratio of the buzzer signal waveform

Note: When a digital envelope has been added to the buzzer signal, the BDTY0–BDTY2 settings will be invalid due to the control of the duty ratio.

4.12.5 Digital envelope

A digital envelope for duty control can be added to the buzzer signal. The envelope can be controlled by staged changing of the same duty envelope as detailed in Table 4.12.4.2 in the preceding item from level 1 (maximum) to level 8 (minimum). The addition of an envelope to the buzzer signal can be done by writing "1" into ENON, but when "0" has been written it is not added. When a buzzer signal output is begun (writing "1" into BZE) after setting ENON, the duty ratio shifts to level 1 (maximum) and changes in stages to level 8. When attenuated down to level 8 (minimum), it is retained at that level. The duty ratio can be returned to maximum, by writing "1" into register ENRST during output of a envelope attached buzzer signal. The envelope attenuation time (time for changing of the duty ratio) can be selected by the register ENRTM. The time for a 1 stage level change is 62.5 msec (16 Hz), when "0" has been written into ENRTM and 125 msec (8 Hz), when to "1" has been written. However, there is also a max. 4 msec error from envelope ON, up to the first change.

Figure 4.12.5.1 shows the timing chart of the digital envelope.

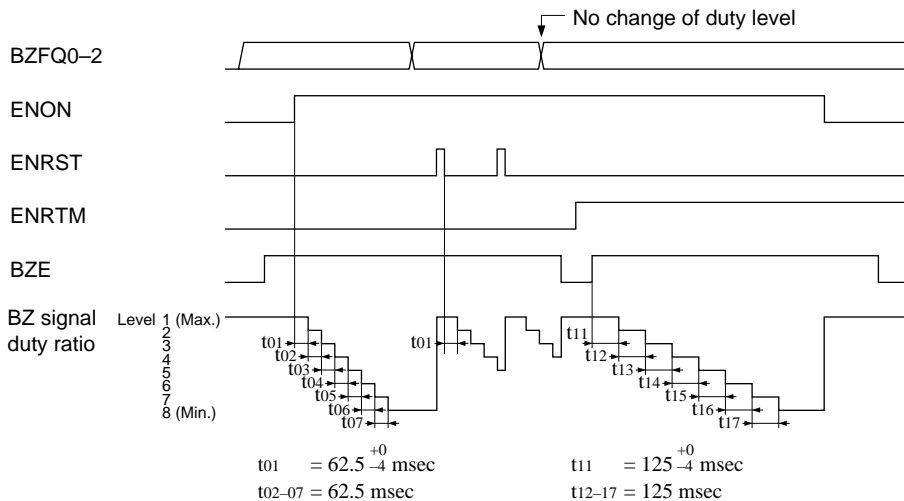


Fig. 4.12.5.1 Timing chart for digital envelope

4.12.6 One-shot output

The sound generator has a one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by SHTPW register for one-shot buzzer signal output time.

The output of the one-shot buzzer is controlled by writing "1" into the one-shot buzzer trigger BZSHT. When this trigger has been assigned, a buzzer signal in synchronization with the internal 256 Hz signal is output from the BZ terminal. Thereafter, when the set time has elapsed, a buzzer signal in synchronization with the 256 Hz signal goes off in the same manner as for the start of output.

The BZSHT also permits reading. When BZSHT is "1", the one-shot output circuit is in operation (during one-shot output) and when it is "0", it shows that the circuit is in the ready (outputtable) status.

In addition, it can also terminate one-shot output prior to the elapsing of the set time. This is done by writing a "1" into the one-shot buzzer stop BZSTP. In this case as well, the buzzer signal goes OFF in synchronization with the 256 Hz signal.

When "1" is written to BZSHT again during a one-shot output, a new one-shot output for 125 msec or 31.25 msec starts from that point (in synchronization with the 256 Hz signal).

The one-shot output cannot add an envelope for short durations. However, the sound level can be set by selecting the duty ratio, and the frequency can also be set.

One-shot output is invalid during normal buzzer output (during BZE = "1").

Figure 4.12.6.1 shows timing chart for one-shot output.

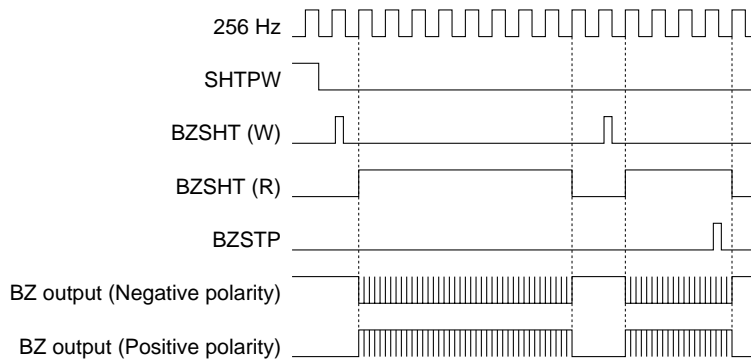


Fig. 4.12.6.1 Timing chart for one-shot output

4.12.7 I/O memory of sound generator

Table 4.12.7.1 shows the I/O addresses and the control bits for the sound generator.

Table 4.12.7.1 Control bits of sound generator

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	- *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W		SHTPW	0	Busy	Ready	1-shot buzzer status (reading)
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	- *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0] 0 1 2 3 Frequency (Hz) 4096.0 3276.8 2730.7 2340.6 [BZFQ2, 1, 0] 4 5 6 7 Frequency (Hz) 2048.0 1638.4 1365.3 1170.3
	R	R/W			BZFQ1	0			
					BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	- *2			
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
					BDTY1	0			
	R	R/W			BDTY0	0			

- *1 Initial value at initial reset
- *2 Not set in the circuit
- *3 Constantly "0" when being read

BZE: BZ output control register (FF6CH•D0)

Controls the buzzer (BZ) signal output.

- When "1" is written: BZ output ON
- When "0" is written: BZ output OFF
- Reading: Valid

When "1" is written to BZE, the BZ signal is output from the BZ terminal.

When "0" is written, the BZ terminal goes to a high (VDD) level.

At initial reset, this register is set to "0".

BZFQ0–BZFQ2: Buzzer frequency selection register (FF6EH•D0–D2)

Selects the buzzer signal frequency.

Table 4.12.7.2 Buzzer signal frequency setting

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Select the buzzer frequency from among the above 8 types that have divided the oscillation clock.

At initial reset, this register is set to "0".

BDTY0–BDTY2: Duty level selection register (FF6FH•D0–D2)

Selects the duty ratio of the buzzer signal as shown in Table 4.12.7.3.

Table 4.12.7.3 Duty ratio setting

Level	BDTY2	BDTY1	BDTY0	Duty ratio by buzzer frequency (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max.)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min.)	1	1	1	1/16	1/20	5/24	5/28

The sound level of this buzzer can be set by selecting this duty ratio.

However, when the envelope has been set to ON (ENON = "1"), this setting becomes invalid.

At initial reset, this register is set to "0".

ENRST: Envelope reset (FF6CH•D2)

Resets the envelope.

When "1" is written: Reset

When "0" is written: No operation

Reading: Always "0"

Writing "1" into ENRST resets envelope and the duty ratio becomes maximum. If an envelope has not been added (ENON = "0") and if no buzzer signal is being output, the reset becomes invalid. Writing "0" is also invalid.

This bit is dedicated for writing, and is always "0" for reading.

ENON: Envelope ON/OFF control register (FF6CH•D1)

Controls the addition of an envelope onto the buzzer signal.

When "1" is written: ON

When "0" is written: OFF

Reading: Valid

Writing "1" into the ENON causes an envelope to be added during buzzer signal output. When a "0" has been written, an envelope is not added.

At initial reset, this register is set to "0".

ENRTM: Envelope releasing time selection register (FF6CH•D3)

Selects the envelope releasing time that is added to the buzzer signal.

When "1" is written: 1.0 sec (125 msec \times 7 = 875 msec)

When "0" is written: 0.5 sec (62.5 msec \times 7 = 437.5 msec)

Reading: Valid

The releasing time of the digital envelope is determined by the time for converting the duty ratio.

When "1" has been written in ENRTM, it becomes 125 msec (8 Hz) units and when "0" has been written, it becomes 62.5 msec (16 Hz) units.

At initial reset, this register is set to "0".

SHTPW: One-shot buzzer pulse width setting register (FF6DH•D0)

Selects the output time of the one-shot buzzer.

When "1" is written: 125 msec

When "0" is written: 31.25 msec

Reading: Valid

Writing "1" into SHTPW causes the one-shot output time to be set at 125 msec, and writing "0" causes it to be set to 31.25 msec. It does not affect normal buzzer output.

At initial reset, this register is set to "0".

BZSHT: One-shot buzzer trigger/status (FF6DH•D1)

Controls the one-shot buzzer output.

• When writing

When "1" is written: Trigger

When "0" is written: No operation

Writing "1" into BZSHT causes the one-shot output circuit to operate and a buzzer signal to be output. This output is automatically turned OFF after the time set by SHTPW has elapsed. The one-shot output is only valid when the normal buzzer output is OFF (BZE = "0") and will be invalid when the normal buzzer output is ON (BZE = "1"). When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point (time extension).

• When reading

When "1" is read: BUSY

When "0" is read: READY

During reading BZSHT shows the operation status of the one-shot output circuit. During one-shot output, BZSHT becomes "1" and the output goes OFF, it shifts to "0".

At initial reset, this bit is set to "0".

BZSTP: One-shot buzzer stop (FF6DH•D2)

Stops the one-shot buzzer output.

When "1" is written: Stop

When "0" is written: No operation

Reading: Always "0"

Writing "1" into BZSTP permits the one-shot buzzer output to be turned OFF prior to the elapsing of the time set by SHTPW. Writing "0" is invalid and writing "1" is also invalid except during one-shot output. This bit is dedicated for writing, and is always "0" for reading.

4.12.8 Programming notes

- (1) Since it generates a BZ signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZE register.
- (2) The one-shot output is only valid when the normal buzzer output is OFF (BZE = "0") and will be invalid when the normal buzzer output is ON (BZE = "1").
- (3) The buzzer signal is generated by dividing the OSC1 oscillation clock. Since the frequencies and times that are described in this section are the values in the case of crystal oscillation (32.768 kHz, Typ.), they differ when CR oscillation (60 kHz, Typ.) is selected.

4.13 SVD (Supply Voltage Detection) Circuit

4.13.1 Configuration of SVD circuit

The E0C63466 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers. It is possible to check an external voltage drop, other than the supply voltage, by mask option.

Turning the SVD circuit ON/OFF and the SVD criteria voltage setting can be done with software.

Figure 4.13.1.1 shows the configuration of the SVD circuit.

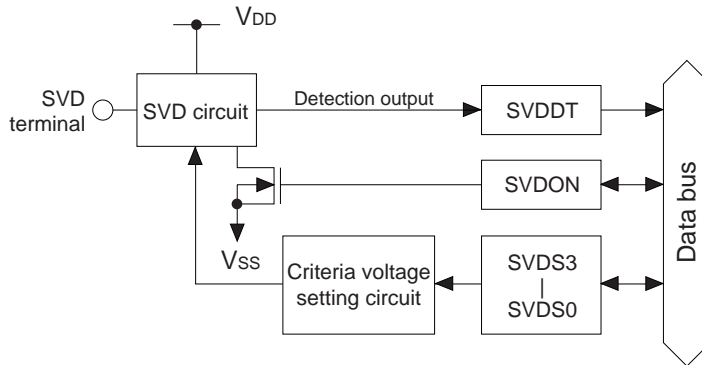


Fig. 4.13.1.1 Configuration of SVD circuit

4.13.2 Mask option

Besides the supply voltage (VDD terminal–VSS terminal) drop detection, the SVD circuit can detect the external voltage (SVD terminal–VSS terminal) input from the SVD terminal by comparing it with the detected voltage (1.05 V). This function can select whether or not to use with the mask option.

4.13.3 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (VDD terminal–VSS terminal) or the external voltage (SVD terminal–VSS terminal) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.

The criteria voltage can be set for the 16 types shown in Table 4.13.3.1 by the SVDS3–SVDS0 registers. When "0" is written to the SVDS3–SVDS0 register, the supply voltage detection voltage is set to 1.85 V. However, when "External voltage detection" is selected by mask option, the SVD circuit does not compare the supply voltage (VDD terminal–VSS terminal) but compares between the external voltage (SVD terminal–VSS terminal) input from the SVD terminal and 1.05 V.

Table 4.13.3.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
0	1	1	1	2.50
0	1	1	0	2.40
0	1	0	1	2.30
0	1	0	0	2.20
0	0	1	1	2.10
0	0	1	0	2.00
0	0	0	1	1.90
0	0	0	0	1.85/1.05

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	3.30
1	1	1	0	3.20
1	1	0	1	3.10
1	1	0	0	3.00
1	0	1	1	2.90
1	0	1	0	2.80
1	0	0	1	2.70
1	0	0	0	2.60

When the SVDON register is set to "1", source voltage or external voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF.

To obtain a stable detection result, the SVD circuit must be ON for at least 100 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

4.13.4 I/O memory of SVD circuit

Table 4.13.4.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.13.4.1 Control bits of SVD circuit

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting [SVDS3-0] 0 1 2 3 4 5 6 7 Voltage(V) 1.85/1.05 1.90 2.00 2.10 2.20 2.30 2.40 2.50 [SVDS3-0] 8 9 10 11 12 13 14 15 Voltage(V) 2.60 2.70 2.80 2.90 3.00 3.10 3.20 3.30
	R/W				SVDS2	0			
	R/W				SVDS1	0			
	R/W				SVDS0	0			
	R/W				SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	- *2			Unused
	R				0 *3	- *2			Unused
	R				SVDDT	0	Low	Normal	SVD evaluation data
	R				SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDS3–SVDS0: SVD criteria voltage setting register (FF04H)

Criteria voltage for SVD is set as shown in Table 4.13.3.1.

At initial reset, this register is set to "0".

SVDON: SVD control (ON/OFF) register (FF05H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON

When "0" is written: SVD circuit OFF

Reading: Valid

When the SVDON register is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least 100 µsec.

At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (VDD–VSS) ≥ Criteria voltage

When "1" is read: Supply voltage (VDD–VSS) < Criteria voltage

Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.

At initial reset, SVDDT is set to "0".

4.13.5 Programming notes

- (1) To obtain a stable detection result, the SVD circuit must be ON for at least 100 μ sec. So, to obtain the SVD detection result, follow the programming sequence below.
 1. Set SVDON to "1"
 2. Maintain for 100 μ sec minimum
 3. Set SVDON to "0"
 4. Read SVDDT
- (2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

4.14 Interrupt and HALT

<Interrupt types>

The E0C63466 provides the following interrupt functions.

External interrupt:	• Input interrupt	(2 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(2 systems)
	• Serial interface interrupt	(1 system)
	• Timer interrupt	(4 systems)
	• Stopwatch timer interrupt	(2 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).

When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.14.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT>

The E0C63466 has HALT functions that considerably reduce the current consumption when it is not necessary.

The CPU enters HALT status when the HALT instruction is executed.

In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.

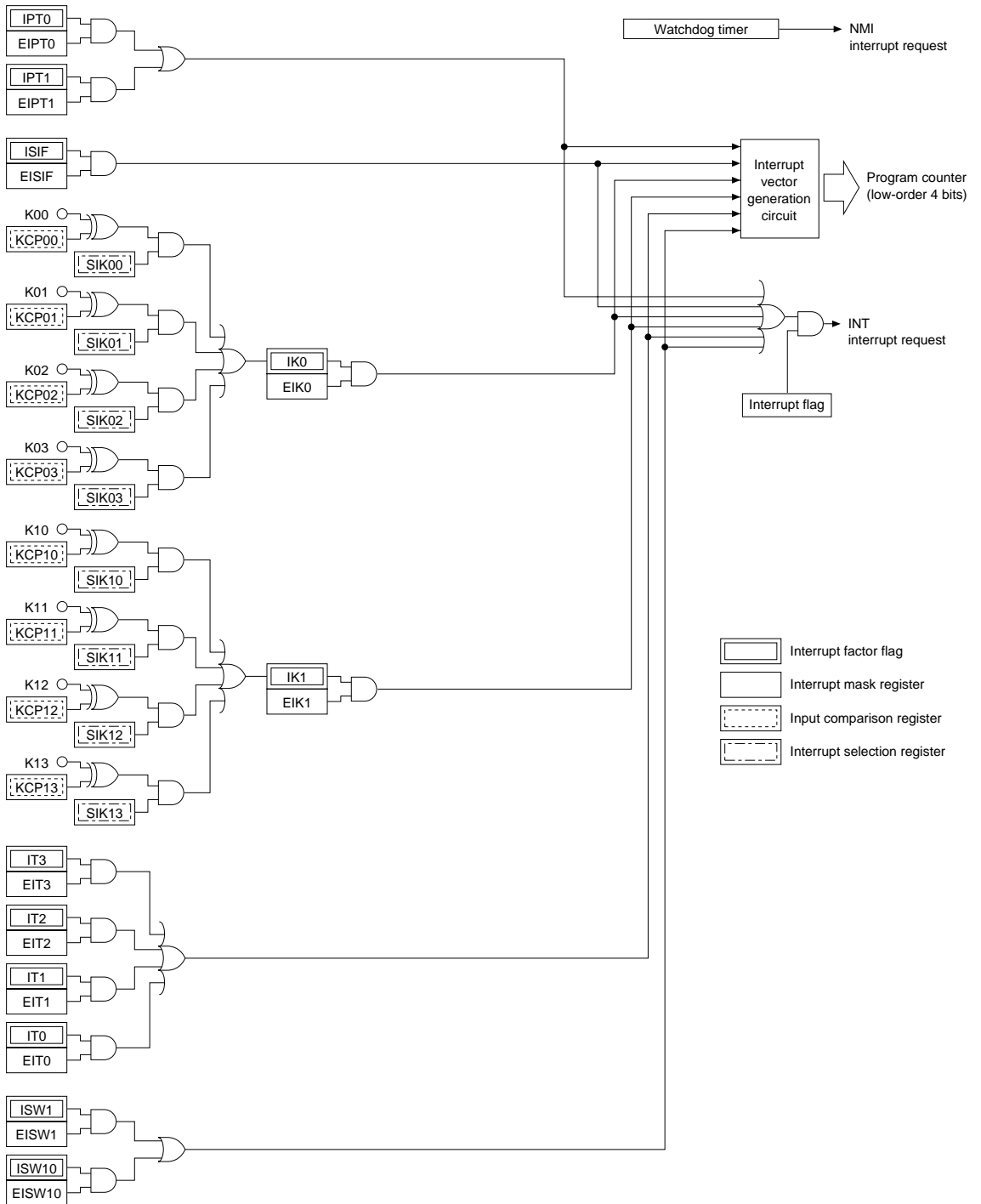


Fig. 4.14.1 Configuration of the interrupt circuit

4.14.1 Interrupt factor

Table 4.14.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.

The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.

At initial reset, the interrupt factor flags are reset to "0".

* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.14.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag
Programmable timer 1 (counter = 0)	IPT1 (FFF2H•D1)
Programmable timer 0 (counter = 0)	IPT0 (FFF2H•D0)
Serial interface (8-bit data input/output completion)	ISIF (FFF3H•D0)
K00–K03 input (falling edge or rising edge)	IK0 (FFF4H•D0)
K10–K13 input (falling edge or rising edge)	IK1 (FFF5H•D0)
Clock timer 1 Hz (falling edge)	IT3 (FFF6H•D3)
Clock timer 2 Hz (falling edge)	IT2 (FFF6H•D2)
Clock timer 8 Hz (falling edge)	IT1 (FFF6H•D1)
Clock timer 32 Hz (falling edge)	IT0 (FFF6H•D0)
Stopwatch timer (1 Hz)	ISW1 (FFF7H•D1)
Stopwatch timer (10 Hz)	ISW10 (FFF7H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.14.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.

The interrupt mask registers are read/write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.

At initial reset, the interrupt mask register is set to "0".

Table 4.14.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.14.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIPT1	(FFE2H•D1)	IPT1	(FFF2H•D1)
EIPT0	(FFE2H•D0)	IPT0	(FFF2H•D0)
EISIF	(FFE3H•D0)	ISIF	(FFF3H•D0)
EIK0	(FFE4H•D0)	IK0	(FFF4H•D0)
EIK1	(FFE5H•D0)	IK1	(FFF5H•D0)
EIT3	(FFE 6H•D3)	IT3	(FFF6H•D3)
EIT2	(FFE6H•D2)	IT2	(FFF6H•D2)
EIT1	(FFE6H•D1)	IT1	(FFF6H•D1)
EIT0	(FFE6H•D0)	IT0	(FFF6H•D0)
EISW1	(FFE7H•D1)	ISW1	(FFF7H•D1)
EISW10	(FFE7H•D0)	ISW10	(FFF7H•D0)

4.14.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

- 1 The content of the flag register is evacuated, then the I flag is reset.
- 2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).
- 3 The interrupt request causes the value of the interrupt vector (0100H–010EH) to be set in the program counter.
- 4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.14.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.14.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High ↑
0104H	Programmable timer	
0106H	Serial interface	
0108H	K00–K03 input	
010AH	K10–K13 input	
010CH	Clock timer	↓ Low
010EH	Stopwatch timer	

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.14.4 I/O memory of interrupt

Tables 4.14.4.1(a) and (b) show the I/O addresses and the control bits for controlling interrupts.

Table 4.14.4.1(a) Control bits of interrupt (1)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
	R/W				SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
	R/W				KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
	R/W				SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
	R/W				SIK10	0	Enable	Disable	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
	R/W				KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
	R/W				KCP10	1	↓	↑	
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
	R/W				EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE7H	0	0	EISW1	EISW10	0 *3	– *2			Unused
	R		R/W		0 *3	– *2			Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
R		R/W		EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)	

*1 Initial value at initial reset
 *2 Not set in the circuit
 *3 Constantly "0" when being read

Table 4.14.4.1(b) Control bits of interrupt (2)

Address	Register				Name	Init *1	1	0	Comment
	D3	D2	D1	D0					
FFF2H	0	0	IPT1	IPT0	0 *3	- *2	(R)	(R)	Unused
	R		R/W		0 *3	- *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
FFF3H	0	0	0	ISIF	0 *3	- *2	(R)	(R)	Unused
	R		R/W		0 *3	- *2	Yes	No	Unused
	R		R/W		0 *3	- *2	(W)	(W)	Unused
FFF4H	0	0	0	IK0	0 *3	- *2	(R)	(R)	Unused
	R		R/W		0 *3	- *2	Yes	No	Unused
	R		R/W		0 *3	- *2	(W)	(W)	Unused
FFF5H	0	0	0	IK1	0 *3	- *2	(R)	(R)	Unused
	R		R/W		0 *3	- *2	Yes	No	Unused
	R		R/W		0 *3	- *2	(W)	(W)	Unused
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
	R/W		R/W		IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W		R/W		IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
FFF7H	0	0	ISW1	ISW10	IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
	R		R/W		0 *3	- *2	(R)	(R)	Unused
	R		R/W		0 *3	- *2	Yes	No	Unused
R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)	
R		R/W		ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)	

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

EIPT1, EIPT0: Interrupt mask registers (FFE2H•D1, D0)**IPT1, IPT0: Interrupt factor flags (FFF2H•D1, D0)**

Refer to Section 4.10, "Programmable Timer".

EISIF: Interrupt mask register (FFE3H•D0)**ISIF: Interrupt factor flag (FFF3H•D0)**

Refer to Section 4.11, "Serial Interface".

KCP03–KCP00, KCP13–KCP10: Input comparison registers (FF22H, FF26H)**SIK03–SIK00, SIK13–SIK10: Interrupt selection registers (FF20H, FF24H)****EIK0, EIK1: Interrupt mask registers (FFE4H•D0, FFE5H•D0)****IK0, IK1: Interrupt factor flags (FFF4H•D0, FFF5H•D0)**

Refer to Section 4.4, "Input Ports".

EIT3–EIT0: Interrupt mask registers (FFE6H)**IT3–IT0: Interrupt factor flags (FFF6H)**

Refer to Section 4.8, "Clock Timer".

EISW1, EISW10: Interrupt mask registers (FFE7H•D1, D0)**ISW1, ISW10: Interrupt factor flags (FFF7H•D1, D0)**

Refer to Section 4.9, "Stopwatch Timer".

4.14.5 Programming notes

- (1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The E0C63466 contains control registers for each of the circuits so that current consumption can be reduced.

These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.

The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
Oscillation system voltage regulator	VDC
LCD system voltage circuit	LPWR
SVD circuit	SVDON

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in OFF status (OSCC = "0")

Oscillation system voltage regulator: Low speed side 1.3 V (VDC = "0")
However, it is fixed at 2.2 V when the CR oscillation circuit has been selected as the OSC1 oscillation circuit. Whether the VDC register value is "0" or "1" does not matter.

LCD system voltage circuit: OFF status (LPWR = "0")

SVD circuit: OFF status (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several μA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

- (1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the display memory area and the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to Section 4.7.5, "Display memory", for the display memory, and the I/O memory maps shown in Tables 4.1.1 (a)–(e) for the peripheral I/O area.
- (2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.
- (3) The E0C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the E0C63466 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Watchdog timer

- (1) When the watchdog timer is being used, the software must reset it within 3-second cycles.
- (2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

- (1) When switching the CPU system clock from OSC1 to OSC3, first set VD1. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set VD1 after switching to OSC1 and turning the OSC3 oscillation OFF. However, when the CR oscillation circuit has been selected as the OSC1 oscillation circuit, it is not necessary to set VD1.
- (2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.
- (3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.
- (4) When the CR oscillation circuit has been selected as the OSC1 oscillation circuit by mask option, it is not necessary to switch the operating voltage VD1 using the VDC register and the VD1 voltage is fixed at 2.2 V. The VD1 level does not change even if any data is written to the VDC register.

Input port

- (1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF

R: pull-up resistance 330 k Ω

- (2) The K13 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K13 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

Output port

- (1) When using the output port (R02, R03) as the special output port, fix the data register (R02, R03) at "1" and the high impedance control register (R02HIZ, R03HIZ) at "0" (data output).

Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R02 and R03 registers when the special output has been selected.

Be aware that the output terminal shifts into high impedance status when "1" is written to the high impedance control register (R02HIZ, R03HIZ).

- (2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.
- (3) When fosc3 is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

I/O port

- (1) When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.

Particular care needs to be taken of the key scan during key matrix configuration.

Make this waiting time the amount of time or more calculated by the following expression.

$$10 \times C \times R$$

C: terminal capacitance 5 pF + parasitic capacitance ? pF

R: pull-up resistance 330 k Ω

- (2) When special output (CL, FR) has been selected, a hazard may occur when the signal is turned ON or OFF.

LCD driver

- (1) When a program that access no memory mounted area (F078H–F0FFH, F178H–F1FFH, F201H, F203H, . . . , F277H) is made, the operation is not guaranteed.
- (2) Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

Clock timer

- (1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).
- (2) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

Stopwatch timer

- (1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 μ sec (1/4 cycle of 256 Hz).
- (2) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, this timer can not be used for the stopwatch function.

Programmable timer

- (1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec (when fOSC1 is 32.768 kHz) of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).
- (2) The programmable timer actually enters RUN/STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0/PTRUN1 register. Consequently, when "0" is written to the PTRUN0/PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0/PTRUN1 register maintains "1" for reading until the timer actually stops. Figure 5.2.1 shows the timing chart for the RUN/STOP control.

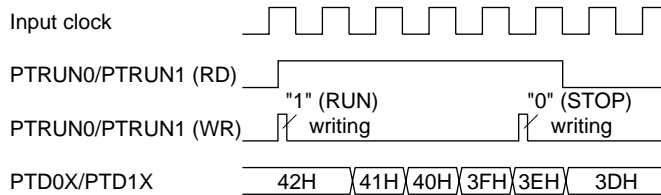


Fig. 5.2.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN/STOP status if a clock is not input after setting the RUN/STOP control register (PTRUN0).

- (3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
- (4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the OFF state.

Serial interface

- (1) Perform data writing/reading to the data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).
- (2) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) In addition, be sure to enable the serial interface with the ESIF register before the trigger. Supply trigger only once every time the serial interface is placed in the RUN state. Refrain from performing trigger input multiple times, as leads to malfunctioning. Moreover, when the synchronous clock \overline{SCLK} is external clock, start to input the external clock after the trigger.
- (3) Setting of the input/output permutation (MSB first/LSB first) with the SDP register should be done before setting data to SD0–SD7.
- (4) Be aware that the maximum clock frequency for the serial interface is limited to 1 MHz when OSC3 is used as the clock source of the programmable timer or in the slave mode.

Sound generator

- (1) Since it generates a BZ signal that is out of synchronization with the BZE register, hazards may at times be produced when the signal goes ON/OFF due to the setting of the BZE register.
- (2) The one-shot output is only valid when the normal buzzer output is OFF (BZE = "0") and will be invalid when the normal buzzer output is ON (BZE = "1").
- (3) The buzzer signal is generated by dividing the OSC1 oscillation clock. Since the frequencies and times that are described in this section are the values in the case of crystal oscillation (32.768 kHz, Typ.), they differ when CR oscillation (60 kHz, Typ.) is selected.

SVD circuit

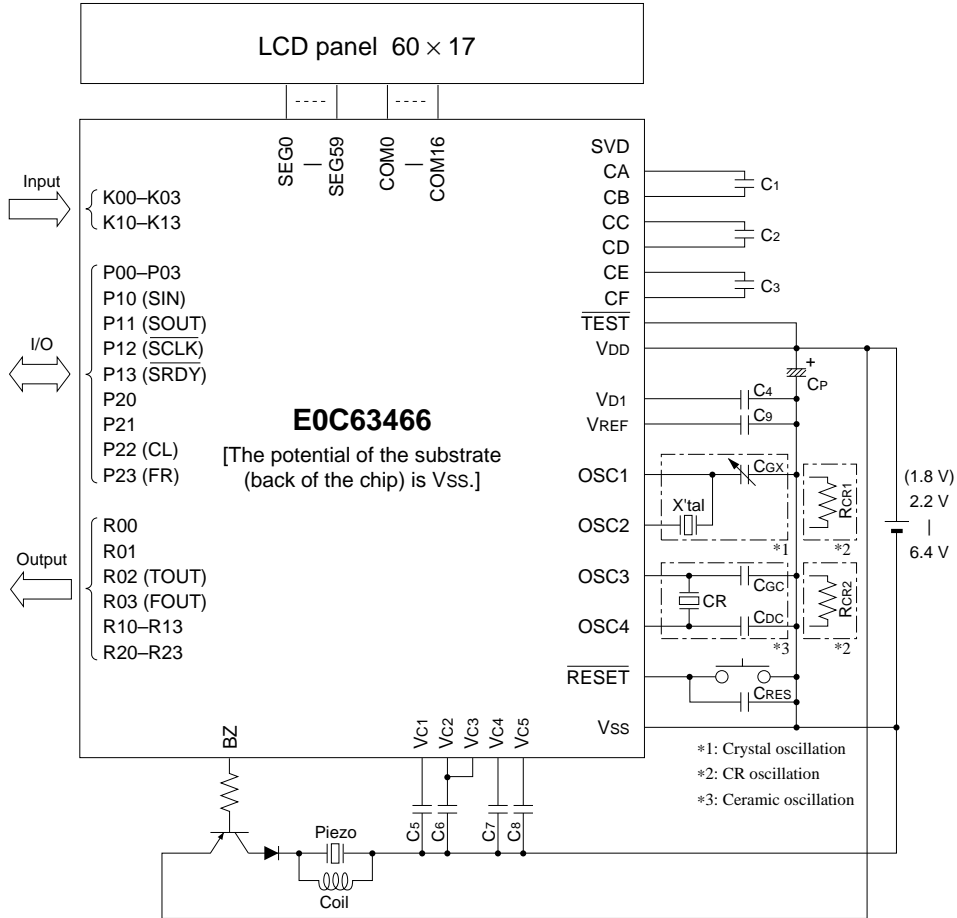
- (1) To obtain a stable detection result, the SVD circuit must be ON for at least 100 μ sec. So, to obtain the SVD detection result, follow the programming sequence below.
 1. Set SVDON to "1"
 2. Maintain for 100 μ sec minimum
 3. Set SVDON to "0"
 4. Read SVDDT
- (2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

Interrupt

- (1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".
- (2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
- (3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM

• When negative polarity is selected for buzzer output (mask option selection)



X'tal	Crystal oscillator	32.768 kHz, C1 (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
RCR1	Resistor for OSC1 CR oscillation	600 kΩ (60 kHz)
CR	Ceramic oscillator	4 MHz (3.0 V)
CGC	Gate capacitor	30 pF
CDC	Drain capacitor	30 pF
RCR2	Resistor for OSC3 CR oscillation	47 kΩ (1.8 MHz)
C1–C8	Capacitor	0.2 μF
C9	Capacitor	0.1 μF
CP	Capacitor	3.3 μF
CRES	RESET terminal capacitor	0.1 μF

Note: The above table is simply an example, and is not guaranteed to work.

- Note:
- In order to prevent unstable operation of the OSC3 oscillation circuit due to current leak between OSC3 and VDD, please keep enough distance between VDD and other signals on the board pattern.
 - In order to get a stable frequency for ceramic oscillation, please use maker's recommendatory value for CGC and CDC.
 - Precautions for Visible Radiation
Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.
 - (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.
 - (2) The inspection process of the product needs an environment that shields the IC from visible radiation.
 - (3) As well as the face of the IC, shield the back and side too.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V _{SS} =0V)			
Item	Symbol	Rated value	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage (1)	V _I	-0.5 to V _{DD} + 0.3	V
Input voltage (2)	V _{IOSC}	-0.5 to V _{D1} + 0.3	V
Permissible total output current *1	ΣI _{VDD}	10	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / time	T _{sol}	260°C, 10sec (lead section)	—
Permissible dissipation *2	P _D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package (QFP8-144pin, QFP17-144pin, QFP5-128pin).

7.2 Recommended Operating Conditions

(T _a =-20 to 70°C)							
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Supply voltage	V _{DD}	V _{SS} =0V	OSC3 oscillation OFF	1.8	3.0	6.4	V
			OSC1 CR oscillation	2.2	3.0	6.4	V
			OSC3 oscillation ON	2.2	3.0	6.4	V
Oscillation frequency	fosc1	Crystal oscillation	—	32.768	—	kHz	
		CR oscillation	40	60	80		
	fosc3	CR oscillation		1,800	2,250	kHz	
		Ceramic oscillation			4,100		
SVD terminal input voltage	SVD	V _{SS} =0V, SVD≤V _{DD}	0		6.4	V	

7.3 DC Characteristics

Unless otherwise specified:

$V_{DD}=3.0V$, $V_{SS}=0V$, $f_{osc1}=32.768kHz$, $T_a=25^{\circ}C$, $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	K00-03, K10-13 P00-03, P10-13, P20-23	$0.8 \cdot V_{DD}$		V_{DD}	V
High level input voltage (2)	V_{IH2}	\overline{RESET} , \overline{TEST}	$0.9 \cdot V_{DD}$		V_{DD}	V
Low level input voltage (1)	V_{IL1}	K00-03, K10-13 P00-03, P10-13, P20-23	0		$0.2 \cdot V_{DD}$	V
Low level input voltage (2)	V_{IL2}	\overline{RESET} , \overline{TEST}	0		$0.1 \cdot V_{DD}$	V
High level input current	I_{IH}	$V_{IH}=3.0V$ K00-03, K10-13 P00-03, P10-13, P20-23 \overline{RESET} , \overline{TEST}	0		0.5	μA
Low level input current (1)	I_{IL1}	$V_{IL1}=V_{SS}$ No Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 \overline{RESET} , \overline{TEST}	-0.5		0	μA
Low level input current (2)	I_{IL2}	$V_{IL2}=V_{SS}$ With Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 \overline{RESET} , \overline{TEST}	-12	-7	-5	μA
High level output current (1)	I_{OH1}	$V_{OH1}=0.9 \cdot V_{DD}$ R00-03, R10-13, R20-23 P00-03, P10-13, P20-23			-2	mA
High level output current (2)	I_{OH2}	$V_{OH2}=0.9 \cdot V_{DD}$ BZ			-2	mA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.1 \cdot V_{DD}$ R00-03, R10-13, R20-23 P00-03, P10-13, P20-23	3			mA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.1 \cdot V_{DD}$ BZ	3			mA
Common output current	I_{OH3}	$V_{OH3}=V_{C5}-0.05V$ COM0-16			-25	μA
	I_{OL3}	$V_{OL3}=V_{SS}+0.05V$	25			μA
Segment output current	I_{OH4}	$V_{OH4}=V_{C5}-0.05V$ SEG0-59			-10	μA
	I_{OL4}	$V_{OL4}=V_{SS}+0.05V$	10			μA

Unless otherwise specified:

$V_{DD}=5.0V$, $V_{SS}=0V$, $f_{osc1}=32.768kHz$, $T_a=25^{\circ}C$, $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	K00-03, K10-13 P00-03, P10-13, P20-23	$0.8 \cdot V_{DD}$		V_{DD}	V
High level input voltage (2)	V_{IH2}	\overline{RESET} , \overline{TEST}	$0.9 \cdot V_{DD}$		V_{DD}	V
Low level input voltage (1)	V_{IL1}	K00-03, K10-13 P00-03, P10-13, P20-23	0		$0.2 \cdot V_{DD}$	V
Low level input voltage (2)	V_{IL2}	\overline{RESET} , \overline{TEST}	0		$0.1 \cdot V_{DD}$	V
High level input current	I_{IH}	$V_{IH}=5.0V$ K00-03, K10-13 P00-03, P10-13, P20-23 \overline{RESET} , \overline{TEST}	0		0.5	μA
Low level input current (1)	I_{IL1}	$V_{IL1}=V_{SS}$ No Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 \overline{RESET} , \overline{TEST}	-0.5		0	μA
Low level input current (2)	I_{IL2}	$V_{IL2}=V_{SS}$ With Pull-up K00-03, K10-13 P00-03, P10-13, P20-23 \overline{RESET} , \overline{TEST}	-20	-12	-9	μA
High level output current (1)	I_{OH1}	$V_{OH1}=0.9 \cdot V_{DD}$ R00-03, R10-13, R20-23 P00-03, P10-13, P20-23			-5	mA
High level output current (2)	I_{OH2}	$V_{OH2}=0.9 \cdot V_{DD}$ BZ			-5	mA
Low level output current (1)	I_{OL1}	$V_{OL1}=0.1 \cdot V_{DD}$ R00-03, R10-13, R20-23 P00-03, P10-13, P20-23	7.5			mA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.1 \cdot V_{DD}$ BZ	7.5			mA
Common output current	I_{OH3}	$V_{OH3}=V_{C5}-0.05V$ COM0-16			-25	μA
	I_{OL3}	$V_{OL3}=V_{SS}+0.05V$	25			μA
Segment output current	I_{OH4}	$V_{OH4}=V_{C5}-0.05V$ SEG0-59			-10	μA
	I_{OL4}	$V_{OL4}=V_{SS}+0.05V$	10			μA

7.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:

$V_{DD}=3.0V$, $V_{SS}=0V$, $f_{OSC1}=32.768kHz$, $C_G=25pF$, $T_a=25^\circ C$, $V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5}$ are internal voltage, $C_1-C_8=0.2\mu F$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
LCD drive voltage (when VC1 standard is selected)	VC1	Connect 1 M Ω load resistor between VSS and VC1 (without panel load)	LC0-3="0"	Typ. $\times 0.88$	0.975	Typ. $\times 1.12$	V
			LC0-3="1"		0.990		
			LC0-3="2"		1.005		
			LC0-3="3"		1.020		
			LC0-3="4"		1.035		
			LC0-3="5"		1.050		
			LC0-3="6"		1.065		
			LC0-3="7"		1.080		
			LC0-3="8"		1.095		
			LC0-3="9"		1.110		
			LC0-3="10"		1.125		
			LC0-3="11"		1.140		
			LC0-3="12"		1.155		
			LC0-3="13"		1.170		
			LC0-3="14"		1.185		
LC0-3="15"	1.200						
	VC2	Connect 1 M Ω load resistor between VSS and VC2 (without panel load)	$2 \cdot V_{C1}$		$2 \cdot V_{C1}$ $\times 0.9$	V	
	VC4	Connect 1 M Ω load resistor between VSS and VC4 (without panel load)	$3 \cdot V_{C1}$		$3 \cdot V_{C1}$ $\times 0.9$	V	
	VC5	Connect 1 M Ω load resistor between VSS and VC5 (without panel load)	$4 \cdot V_{C1}$		$4 \cdot V_{C1}$ $\times 0.9$	V	
LCD drive voltage (when VC2 standard is selected)	VC1	Connect 1 M Ω load resistor between VSS and VC1 (without panel load)	$1/2 \cdot V_{C2}$ -0.1		$1/2 \cdot V_{C2}$ $\times 0.95$	V	
	VC2	Connect 1 M Ω load resistor between VSS and VC2 (without panel load)	LC0-3="0"	Typ. $\times 0.88$	1.95	Typ. $\times 1.12$	V
			LC0-3="1"		1.98		
			LC0-3="2"		2.01		
			LC0-3="3"		2.04		
			LC0-3="4"		2.07		
			LC0-3="5"		2.10		
			LC0-3="6"		2.13		
			LC0-3="7"		2.16		
			LC0-3="8"		2.19		
			LC0-3="9"		2.22		
			LC0-3="10"		2.25		
			LC0-3="11"		2.28		
			LC0-3="12"		2.31		
			LC0-3="13"		2.34		
LC0-3="14"			2.37				
LC0-3="15"	2.40						
	VC4	Connect 1 M Ω load resistor between VSS and VC4 (without panel load)	$3/2 \cdot V_{C2}$ $\times 0.95$		$3/2 \cdot V_{C2}$	V	
	VC5	Connect 1 M Ω load resistor between VSS and VC5 (without panel load)	$2 \cdot V_{C2}$ $\times 0.95$		$2 \cdot V_{C2}$	V	

Unless otherwise specified:

V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, R_{CR1}=600kΩ, R_{CR2}=47kΩ, T_a=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C₁-C₈=0.2μF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
SVD voltage	VSVD1	SVDS0-3="0" (internal)	Typ. ×0.93	1.85	Typ. ×1.07	V	
		SVDS0-3="1"		1.90			
		SVDS0-3="2"		2.00			
		SVDS0-3="3"		2.10			
		SVDS0-3="4"		2.20			
		SVDS0-3="5"		2.30			
		SVDS0-3="6"		2.40			
		SVDS0-3="7"		2.50			
		SVDS0-3="8"		2.60			
		SVDS0-3="9"		2.70			
		SVDS0-3="10"		2.80			
		SVDS0-3="11"		2.90			
		SVDS0-3="12"		3.00			
		SVDS0-3="13"		3.10			
		SVDS0-3="14"		3.20			
SVDS0-3="15"	3.30						
SVD voltage (external) *4	VSVD2	SVDS0-3="0" (external)	0.95	1.05	1.15	V	
SVD circuit response time	t _{SVD}				100	μS	
Current consumption	I _{OP}	During HALT (32 kHz crystal oscillation), LCD power OFF *1, *2, *3		1	2	μA	
		During HALT (32 kHz crystal oscillation), LCD power ON (V _{C1} standard) *1, *2, *3		6	12	μA	
		During HALT (32 kHz crystal oscillation), LCD power ON (V _{C2} standard) *1, *2, *3		4	8	μA	
		During HALT (60 kHz CR oscillation), LCD power OFF *1, *3		23	45	μA	
		During HALT (60 kHz CR oscillation), LCD power ON (V _{C1} standard) *1, *3		30	60	μA	
		During HALT (60 kHz CR oscillation), LCD power ON (V _{C2} standard) *1, *3		26	50	μA	
		During execution (32 kHz crystal oscillation), LCD power ON (V _{C1} standard) *1, *2, *3		10	19	μA	
		During execution (60 kHz CR oscillation), LCD power ON (V _{C1} standard) *1, *3		45	80	μA	
		During execution (2 MHz ceramic oscillation), LCD power ON (V _{C1} standard) *1		600	800	μA	
		During execution (4 MHz ceramic oscillation), LCD power ON (V _{C1} standard) *1		1,200	1,400	μA	
		During execution (1,800 kHz CR oscillation), LCD power ON (V _{C1} standard) *1		800	1,000	μA	
		SVD circuit current (during supply voltage detection) V _{DD} =1.85 to 6.4 V		1		7	μA
		SVD circuit current (during external voltage detection) V _{DD} =1.85 to 6.4 V		0.5		3	μA

*1 Without panel load. The SVD circuit is OFF.

*2 V_{DC} = "0"

*3 OSC = "0"

*4 Please input the voltage, which is within the range between V_{SS} and V_{DD}, into the SVD terminal.

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:

$V_{DD}=3.0V$, $V_{SS}=0V$, $f_{OSC1}=32.768kHz$, $C_G=25pF$, $C_D=$ built-in, $T_a=-20$ to $70^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	$t_{sta} \leq 3sec$ (V_{DD})	1.8			V
Oscillation stop voltage	Vstp	$t_{stp} \leq 10sec$ (V_{DD})	1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{DD}=2.2$ to $6.4V$			5	ppm
		with VDC switching			10	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	10	20		ppm
Harmonic oscillation start voltage	V_{hho}	$C_G=5pF$ (V_{DD})	6.4			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			$M\Omega$

OSC1 CR oscillation circuit

Unless otherwise specified:

$V_{DD}=3.0V$, $V_{SS}=0V$, $R_{CR1}=600k\Omega$, $T_a=-20$ to $70^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc1		-30	60kHz	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	$V_{DD}=2.2$ to $6.4V$			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 ceramic oscillation circuit

Unless otherwise specified:

$V_{DD}=3.0V$, $V_{SS}=0V$, Ceramic oscillator: 4MHz, $C_{GC}=C_{DC}=30pF$, $T_a=-20$ to $70^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	$V_{DD}=2.2$ to $6.4V$			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 CR oscillation circuit

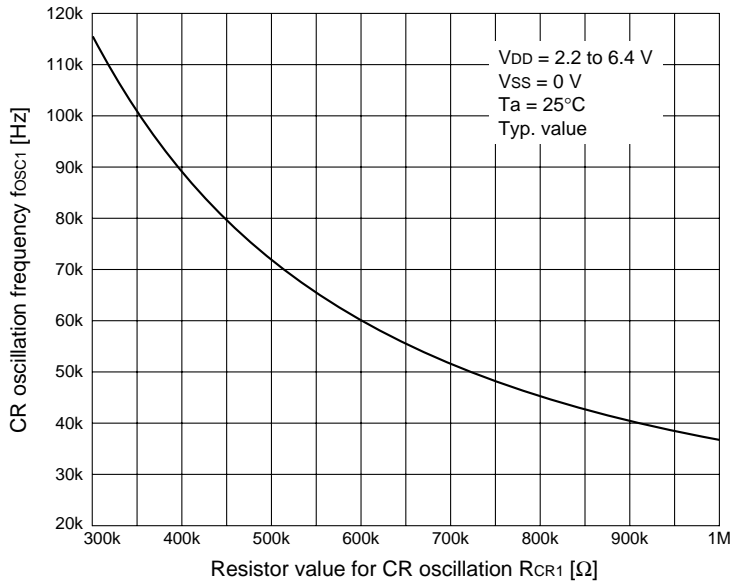
Unless otherwise specified:

$V_{DD}=3.0V$, $V_{SS}=0V$, $R_{CR2}=47k\Omega$, $T_a=-20$ to $70^{\circ}C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc3		-25	1,800kHz	25	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	$V_{DD}=2.2$ to $6.4V$			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

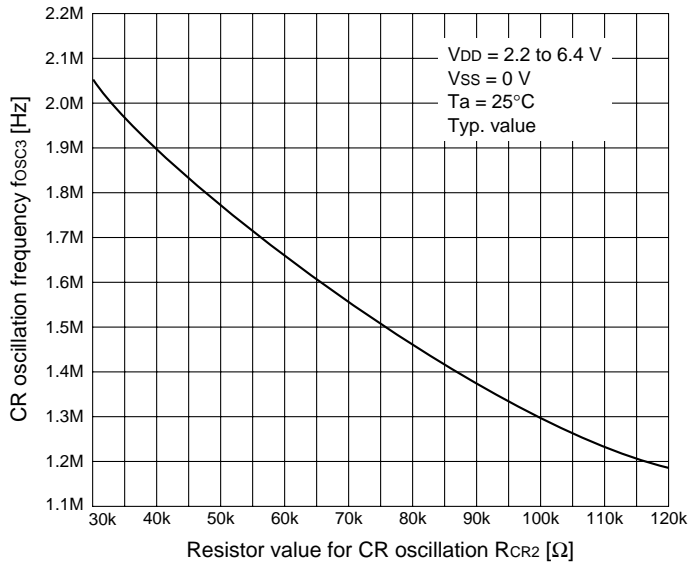
OSC1 CR oscillation frequency-resistance characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



OSC3 CR oscillation frequency-resistance characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.



7.6 Serial Interface AC Characteristics

Clock synchronous master mode

• During 32 kHz operation

Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	t _{smd}			5	μS
Receiving data input set-up time	t _{sms}	10			μS
Receiving data input hold time	t _{smh}	5			μS

• During 1 MHz operation

Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	t _{smd}			200	nS
Receiving data input set-up time	t _{sms}	400			nS
Receiving data input hold time	t _{smh}	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

Clock synchronous slave mode

• During 32 kHz operation

Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	t _{ssd}			10	μS
Receiving data input set-up time	t _{sss}	10			μS
Receiving data input hold time	t _{ssh}	5			μS

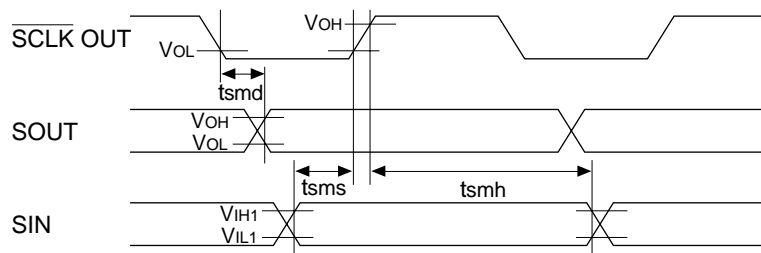
• During 1 MHz operation

Condition: $V_{DD}=3.0V$, $V_{SS}=0V$, $T_a=25^\circ C$, $V_{IH1}=0.8V_{DD}$, $V_{IL1}=0.2V_{DD}$, $V_{OH}=0.8V_{DD}$, $V_{OL}=0.2V_{DD}$

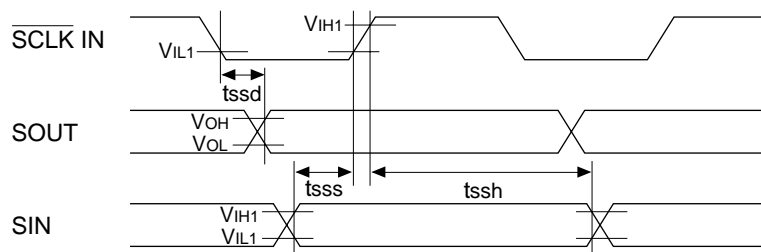
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	t _{ssd}			500	nS
Receiving data input set-up time	t _{sss}	400			nS
Receiving data input hold time	t _{ssh}	200			nS

Note that the maximum clock frequency is limited to 1 MHz.

<Master mode>

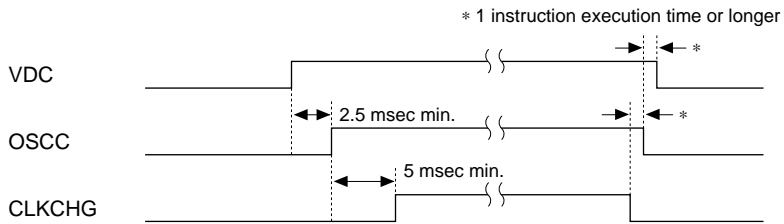


<Slave mode>



7.7 Timing Chart

System clock switching



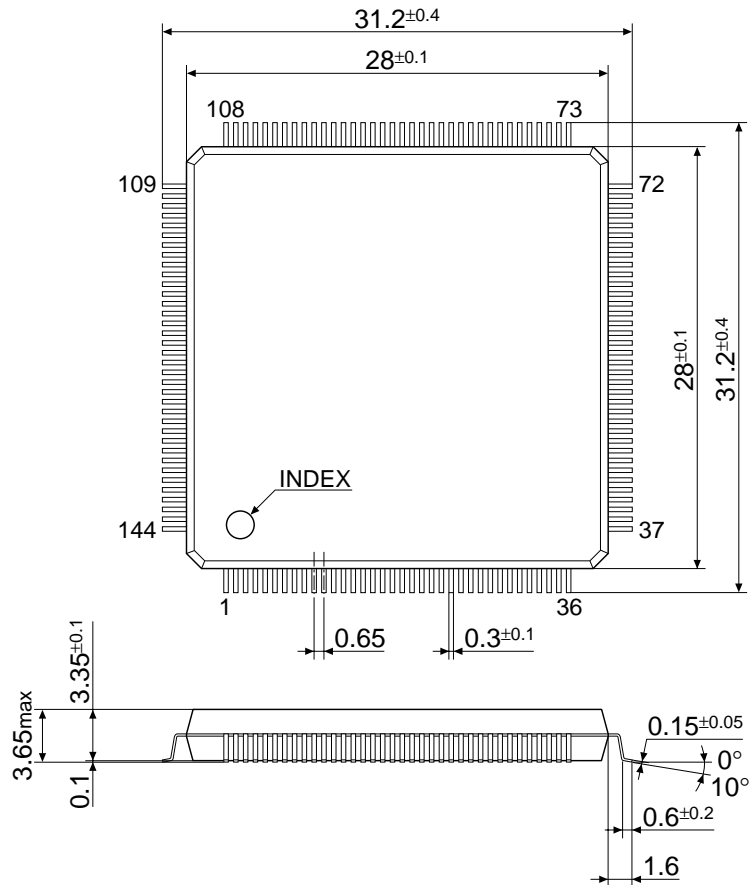
Note: When the OSC1 oscillation circuit has been selected as the CR oscillation circuit, it is not necessary to set the VDC register. Whether the VDC register value is "1" or "0" does not matter.

CHAPTER 8 PACKAGE

8.1 Plastic Package

QFP8-144pin

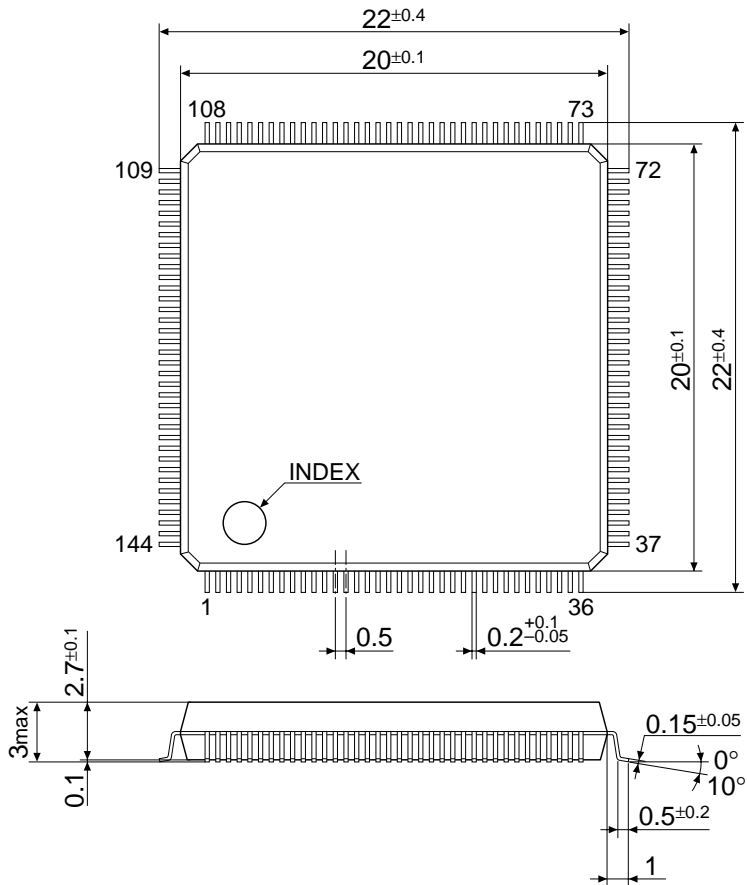
(Unit: mm)



The dimensions are subject to change without notice.

QFP17-144pin

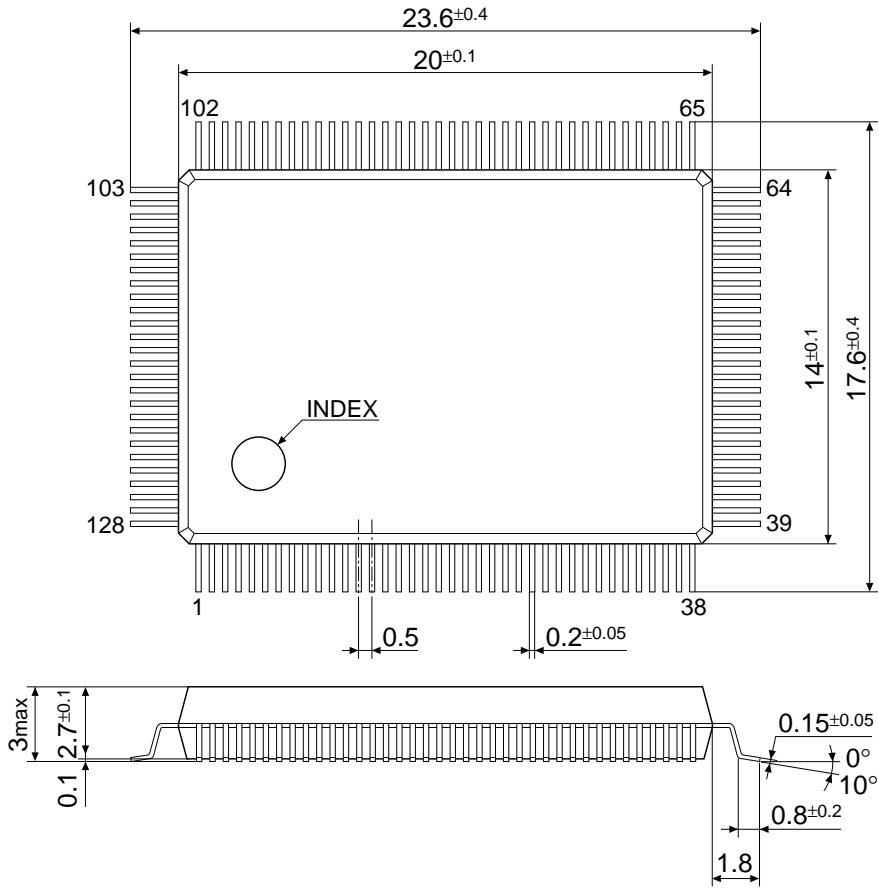
(Unit: mm)



The dimensions are subject to change without notice.

QFP5-128pin

(Unit: mm)

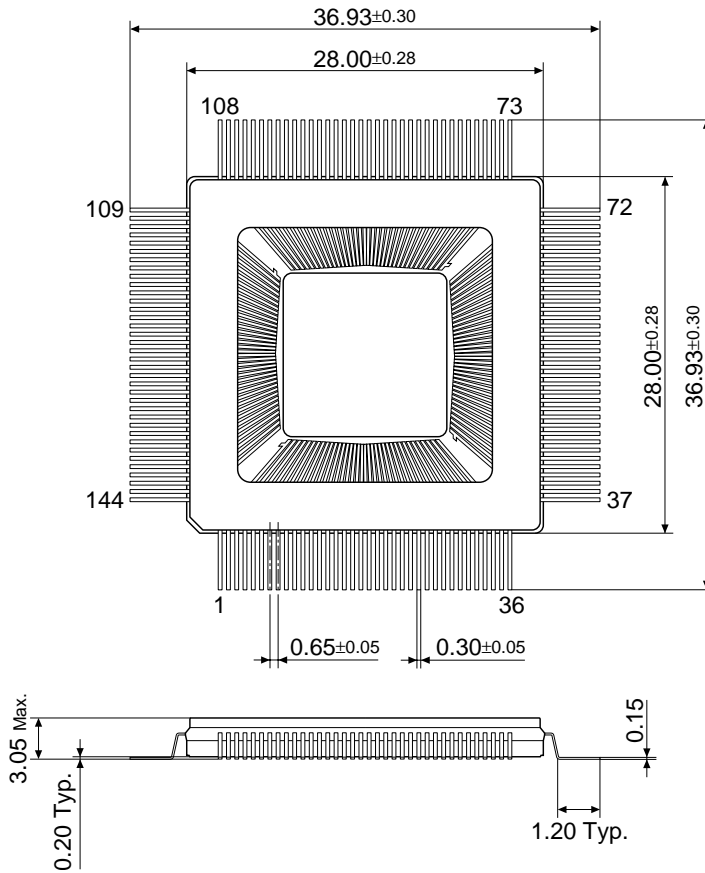


The dimensions are subject to change without notice.

8.2 Ceramic Package for Test Samples

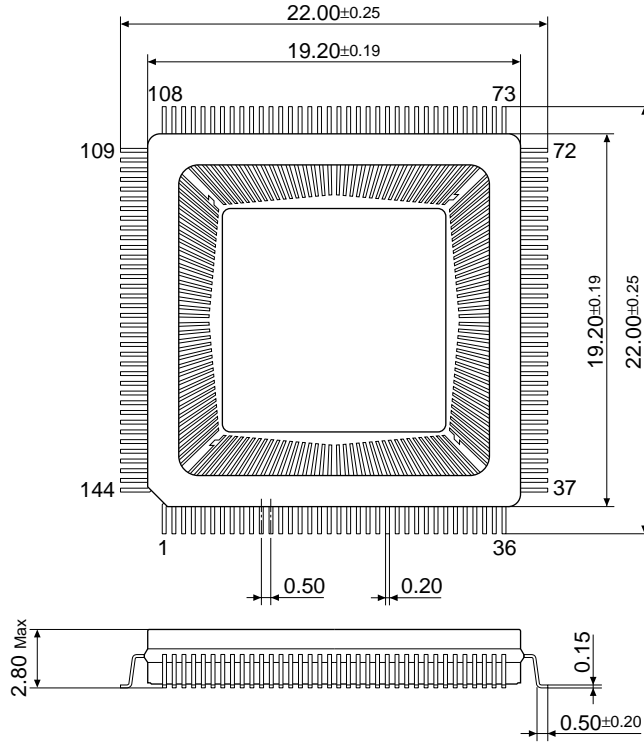
QFP8-144pin

(Unit: mm)



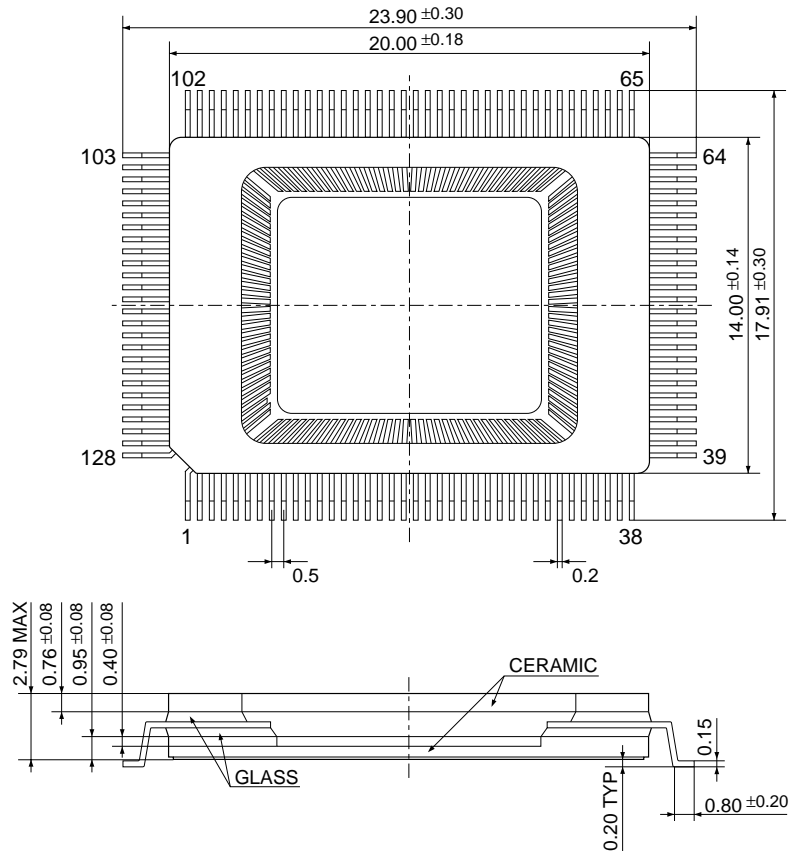
QFP17-144pin

(Unit: mm)



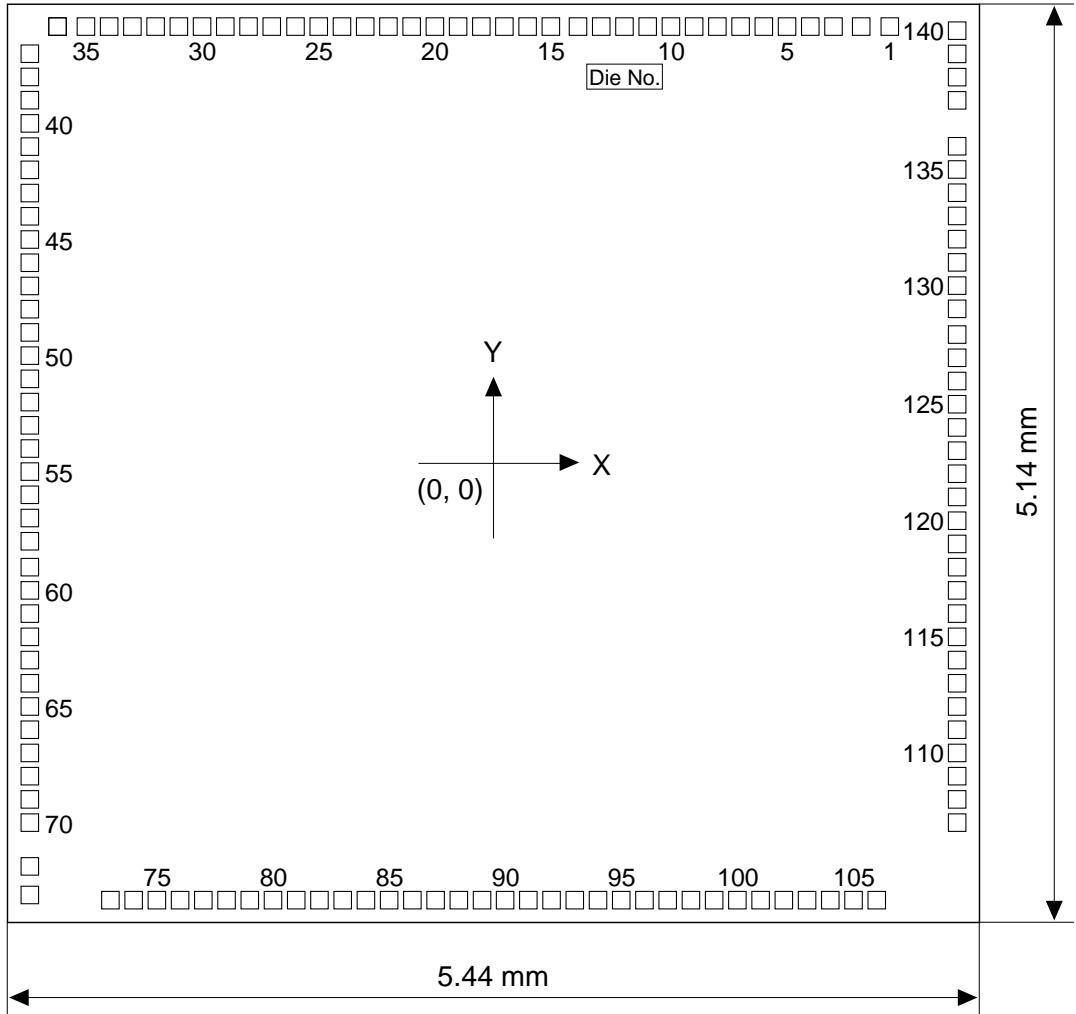
QFP5-128pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 μm
 Pad opening: 100 μm

9.2 Pad Coordinates

															Unit: μm		
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y		
1	N.C.	2218	2445	36	N.C.	-2440	2445	71	N.C.	-2595	-2256	106	SEG14	2145	-2445		
2	N.C.	2058	2445	37	N.C.	-2595	2293	72	N.C.	-2595	-2416	107	SEG13	2595	-2011		
3	R23	1903	2445	38	SVD	-2595	2163	73	SEG47	-2144	-2445	108	SEG12	2595	-1881		
4	R22	1773	2445	39	VC1	-2595	2033	74	SEG46	-2014	-2445	109	SEG11	2595	-1751		
5	R21	1643	2445	40	VC2	-2595	1903	75	SEG45	-1884	-2445	110	SEG10	2595	-1621		
6	R20	1513	2445	41	VC3	-2595	1773	76	SEG44	-1754	-2445	111	SEG9	2595	-1491		
7	R13	1383	2445	42	VC4	-2595	1643	77	SEG43	-1624	-2445	112	SEG8	2595	-1361		
8	R12	1253	2445	43	VC5	-2595	1513	78	SEG42	-1494	-2445	113	SEG7	2595	-1231		
9	R11	1123	2445	44	CF	-2595	1383	79	SEG41	-1364	-2445	114	SEG6	2595	-1101		
10	R10	993	2445	45	CE	-2595	1253	80	SEG40	-1234	-2445	115	SEG5	2595	-971		
11	R03	863	2445	46	CD	-2595	1123	81	SEG39	-1104	-2445	116	SEG4	2595	-841		
12	R02	733	2445	47	CC	-2595	993	82	SEG38	-974	-2445	117	SEG3	2595	-711		
13	R01	603	2445	48	CB	-2595	863	83	SEG37	-844	-2445	118	SEG2	2595	-581		
14	R00	473	2445	49	CA	-2595	733	84	SEG36	-714	-2445	119	SEG1	2595	-451		
15	P23	321	2445	50	COM8	-2595	603	85	SEG35	-584	-2445	120	SEG0	2595	-321		
16	P22	191	2445	51	COM9	-2595	473	86	SEG34	-454	-2445	121	COM7	2595	-188		
17	P21	61	2445	52	COM10	-2595	343	87	SEG33	-324	-2445	122	COM6	2595	-58		
18	P20	-68	2445	53	COM11	-2595	213	88	SEG32	-194	-2445	123	COM5	2595	71		
19	P13	-198	2445	54	COM12	-2595	83	89	SEG31	-64	-2445	124	COM4	2595	201		
20	P12	-328	2445	55	COM13	-2595	-46	90	SEG30	65	-2445	125	COM3	2595	331		
21	P11	-458	2445	56	COM14	-2595	-176	91	SEG29	195	-2445	126	COM2	2595	461		
22	P10	-588	2445	57	COM15	-2595	-306	92	SEG28	325	-2445	127	COM1	2595	591		
23	P03	-718	2445	58	COM16	-2595	-436	93	SEG27	455	-2445	128	COM0	2595	721		
24	P02	-848	2445	59	SEG59	-2595	-581	94	SEG26	585	-2445	129	BZ	2595	865		
25	P01	-978	2445	60	SEG58	-2595	-711	95	SEG25	715	-2445	130	Vss	2595	995		
26	P00	-1108	2445	61	SEG57	-2595	-841	96	SEG24	845	-2445	131	OSC1	2595	1125		
27	K13	-1241	2445	62	SEG56	-2595	-971	97	SEG23	975	-2445	132	OSC2	2595	1255		
28	K12	-1371	2445	63	SEG55	-2595	-1101	98	SEG22	1105	-2445	133	Vd1	2595	1385		
29	K11	-1501	2445	64	SEG54	-2595	-1231	99	SEG21	1235	-2445	134	OSC3	2595	1515		
30	K10	-1631	2445	65	SEG53	-2595	-1361	100	SEG20	1365	-2445	135	OSC4	2595	1645		
31	K03	-1761	2445	66	SEG52	-2595	-1491	101	SEG19	1495	-2445	136	VDD	2595	1775		
32	K02	-1891	2445	67	SEG51	-2595	-1621	102	SEG18	1625	-2445	137	RESET	2595	2032		
33	K01	-2021	2445	68	SEG50	-2595	-1751	103	SEG17	1755	-2445	138	TEST	2595	2162		
34	K00	-2151	2445	69	SEG49	-2595	-1881	104	SEG16	1885	-2445	139	VREF	2595	2292		
35	N.C.	-2281	2445	70	SEG48	-2595	-2011	105	SEG15	2015	-2445	140	N.C.	2595	2442		

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