MF947-02

EPSON

E0C63404 DEVELOPMENT HARDWARE TOOL

E0C63P404 TECHNICAL MANUAL

E0C63P404 Technical Hardware

SEIKO EPSON CORPORATION

PREFACE

This manual describes the hardware specification of the E0C63P404.
The E0C63P404 is a development tool for the E0C63404. The mask ROM in the E0C63404 has been changed to a Flash EEPROM. Almost all other circuits are compatible with the E0C63404, therefore this manual explains only the parts related to the PROM and other differences from the E0C63404. Furthermore, an exclusive PROM writer (UNIVERSAL ROM WRITER II) should be used for PROM programming.

Refer to the following manuals in addition to this manual.

For the functions and control of the peripheral circuit: "E0C63404 Technical Manual"
For the exclusive PROM writer and programming: "Universal ROM Writer II Hardware Manual"
"E0C63Pxxx Universal ROM Writer II User's Manual"
"E0C63P404 Adapter Socket Hardware Manual"

CONTENTS

CHAPTER 1 OUTLINE

The E0C63P404 is a 4-bit microcomputer, with a built-in Flash EEPROM (PROM), for evaluating the functions of the E0C63404.
The E0C63P404 has almost the same functions as the E0C63404. The mask ROM in the E0C63404 has been changed to a Flash EEPROM that allows the user to rewrite programs and data (character data, etc.) using the exclusive PROM writer. The E0C63P404 also supports On Board Programming (the data can be rewritten to the PROM if the IC is mounted on the board). The program can be rewritten up to 10 times under the development stage, it will increase the efficiency of device-level function evaluation.

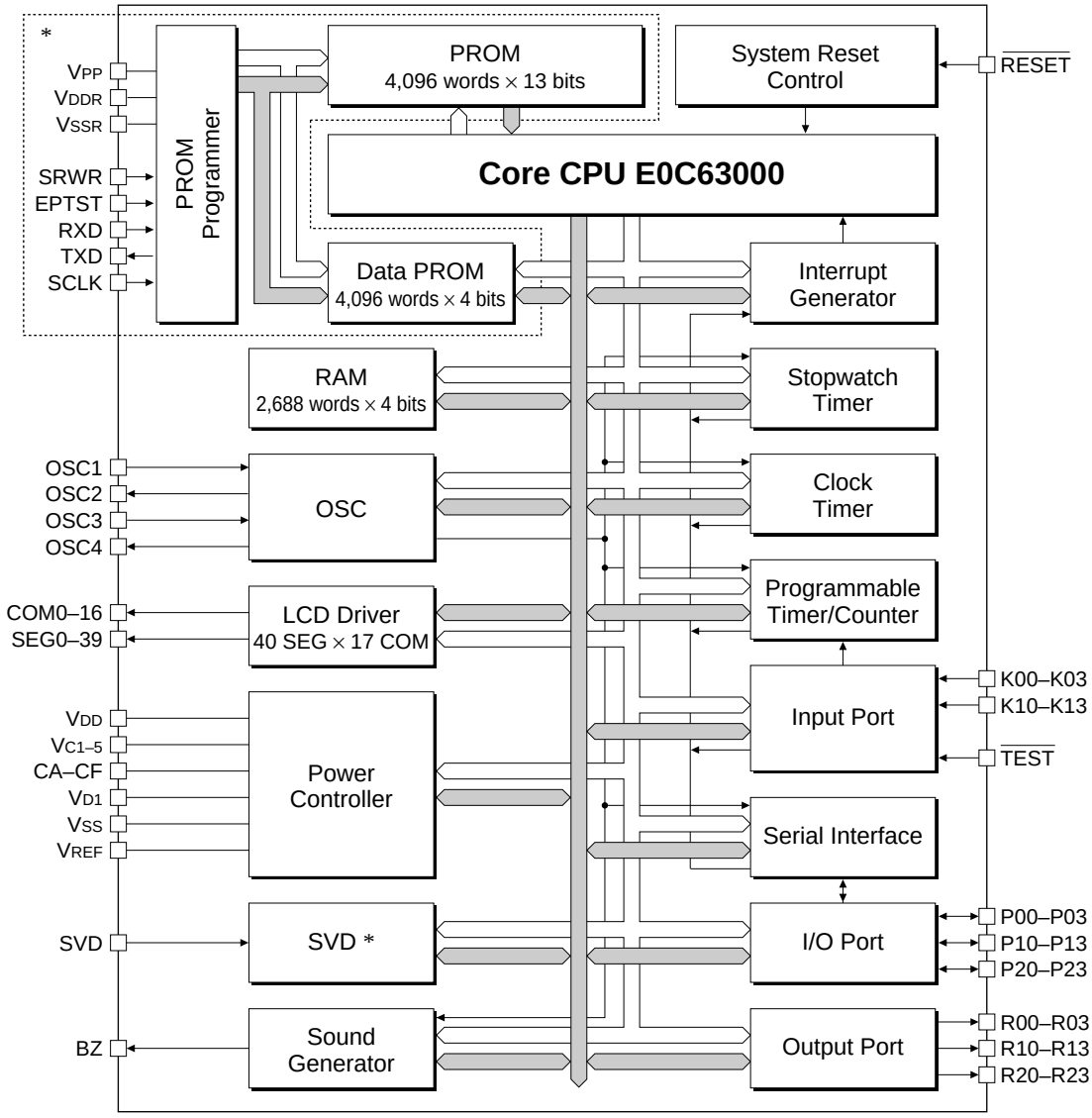
Note: • *Rewriting the PROM is done at the user's own risk.*
• *The E0C63P404 is a program development tool for evaluating the functions, therefore do not use it for mass production.*

1.1 Features

PROM configuration	Instruction PROM: 4,096 words × 13 bits [Flash EEPROM built-in] Data PROM: 2,048 words × 4 bits (= 8K bits) [Flash EEPROM built-in]
PROM method	Dual power: 12.5 V for writing/erase, 5 V for operating Rewriting: 10 times Max.
PROM programmer	Serial programming and parallel programming are available *3
OSC1 oscillation circuit	32.768 kHz (Typ.) crystal oscillation circuit *3
OSC3 oscillation circuit	1 MHz (Typ.) ceramic oscillation circuit *3
Instruction set	Basic instruction: 46 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec During operation at 1 MHz: 2 µsec 4 µsec 6 µsec
RAM capacity	Data memory: 2,688 words × 4 bits Display memory: 200 words × 4 bits
Input port	8 bits (Pull-up resistors may be supplemented *1)
Output port	12 bits (It is possible to switch the 2 bits to special output *2)
I/O port	12 bits (It is possible to switch the 2 bits to special output and the 4 bits to serial I/F input/output *2)
Serial interface	1 port (8-bit clock synchronous system)
LCD driver	40 segments × 8, 16 or 17 commons *2
Time base counter	2 systems (Clock timer, stopwatch timer)
Programmable timer	Built-in, 2 inputs × 8 bits, with event counter function
Watchdog timer	Built-in
Sound generator	With envelope and 1-shot output functions
Supply voltage detection (SVD) circuit	16values, programmable *3 (It is possible to switch 1 value to the external voltage detection *1)
External interrupt	Input port interrupt: 2 systems
Internal interrupt	Clock timer interrupt: 4 systems Stopwatch timer interrupt: 2 systems Programmable timer interrupt: 2 systems Serial interface interrupt: 1 system
Power supply voltage	4.5 V to 5.5 V *3
Package	QFP8-128pin (plastic) or chip

*1: Can be selected with mask option
*2: Can be selected with software
*3: Items that differ from the E0C63404

1.2 Block Diagram

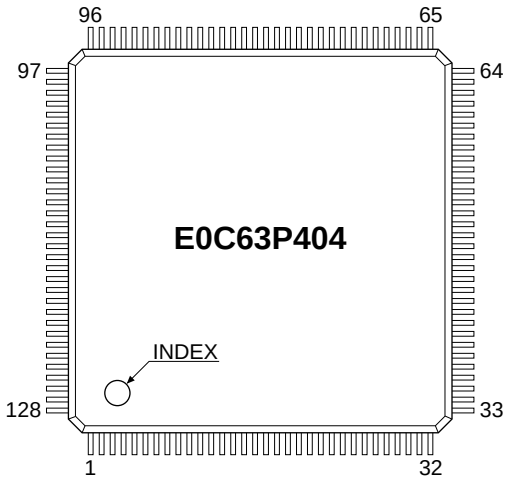


∗ The PROM block indicated with a dotted line and the SVD circuit differ from the E0C63404.

Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP8-128pin



No.	Name	No.	Name	No.	Name	No.	Name
1	EPTST *	33	R23	65	N.C.	97	SCLK *
2	SEG3	34	R22	66	SVD	98	TXD *
3	SEG2	35	R21	67	N.C.	99	SEG32
4	SEG1	36	R20	68	N.C.	100	SEG31
5	SEG0	37	R13	69	V_{C1}	101	SEG30
6	COM7	38	R12	70	V_{C2}	102	SEG29
7	COM6	39	R11	71	V_{C3}	103	SEG28
8	COM5	40	R10	72	V_{C4}	104	SEG27
9	COM4	41	R03	73	V_{C5}	105	SEG26
10	COM3	42	R02	74	CF	106	SEG25
11	COM2	43	R01	75	CE	107	SEG24
12	COM1	44	R00	76	CD	108	SEG23
13	COM0	45	P23	77	CC	109	SEG22
14	V_{DDR} *	46	P22	78	CB	110	SEG21
15	V_{SSR} *	47	P21	79	CA	111	SEG20
16	V_{PP} *	48	P20	80	COM8	112	SEG19
17	BZ	49	P13	81	COM9	113	SEG18
18	V_{SS}	50	P12	82	COM10	114	SEG17
19	OSC1	51	P11	83	COM11	115	SEG16
20	OSC2	52	P10	84	COM12	116	SEG15
21	V_{D1}	53	P03	85	COM13	117	SEG14
22	OSC3	54	P02	86	COM14	118	SEG13
23	OSC4	55	P01	87	COM15	119	SEG12
24	V_{DD}	56	P00	88	COM16	120	SEG11
25	N.C.	57	K13	89	SEG39	121	SEG10
26	N.C.	58	K12	90	SEG38	122	SEG9
27	N.C.	59	K11	91	SEG37	123	SEG8
28	$\overline{\text{RESET}}$	60	K10	92	SEG36	124	SEG7
29	$\overline{\text{TEST}}$	61	K03	93	SEG35	125	SEG6
30	V_{REF}	62	K02	94	SEG34	126	SEG5
31	N.C.	63	K01	95	SEG33	127	SEG4
32	N.C.	64	K00	96	RXD *	128	SRWR *

N.C. : No Connection
* : Terminals added in the E0C63P404.
They are N.C. terminals in the E0C63404.

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
V_{DD}	24	–	Power supply pin (+5 V)
V_{SS}	18	–	Power supply pin (0 V, GND)
V_{D1}	21	–	Oscillation/internal logic system regulated voltage output pin
V_{C1}–V_{C5}	69–73	–	LCD system power supply pin 1/4 bias generated internally, 1/5 bias supplied externally (selected by mask option)
V_{REF}	30	O	LCD system power supply testing pin
CA–CF	79–74	–	LCD system boosting/reducing capacitor connecting pin
OSC1	19	I	Crystal oscillation input pin
OSC2	20	O	Crystal oscillation output pin
OSC3	22	I	Ceramic oscillation input pin
OSC4	23	O	Ceramic oscillation output pin
K00–K03	64–61	I	Input port
K10–K13	60–57	I	Input port
P00–P03	56–53	I/O	I/O port
P10–P13	52–49	I/O	I/O port (switching to serial I/F input/output is possible by software)
P20	48	I/O	I/O port
P21	47	I/O	I/O port
P22	46	I/O	I/O port (switching to CL signal output is possible by software)
P23	45	I/O	I/O port (switching to FR signal output is possible by software)
R00	44	O	Output port
R01	43	O	Output port
R02	42	O	Output port (switching to TOUT signal output is possible by software)
R03	41	O	Output port (switching to FOUT signal output is possible by software)
R10–R13	40–37	O	Output port
R20–R23	36–33	O	Output port
COM0–COM16	13–6, 80–88	O	LCD common output pin (1/8, 1/16, 1/17 duty can be selected by software)
SEG0–SEG39	5–2, 127–99, 95–89	O	LCD segment output pin
BZ	17	O	Sound output pin
SVD	66	I	SVD external voltage input pin
$\overline{\text{RESET}}$	28	I	Initial reset input pin
$\overline{\text{TEST}}$	29	I	Testing input pin
SRWR *	128	I	PROM serial programming mode setting pin (fix at a Low level or open in normal mode)
EPTST *	1	I	PROM programming mode setting pin (fix at a Low level or open in normal mode)
RXD *	96	I	PROM serial programming data input pin (fix at a High level or open in normal mode)
TXD *	98	O	PROM serial programming data output pin (unused in normal mode)
SCLK *	97	I/O	PROM serial programming clock input/output pin (fix at a High level or open in normal mode)
V_{DDR} *	14	–	Power supply pin for PROM (+5 V)
V_{SSR} *	15	–	Power supply pin for PROM (0 V, GND)
V_{PP} *	16	–	PROM programming power supply (fix at +5 V in normal mode)

* Terminals added in the E0C63P404. (They are not used in the E0C63404.)

See Section 3.1, "Terminal Configuration", for the terminal functions during the programming mode.

CHAPTER 2 PROM PROGRAMMER AND OPERATING MODES

The biggest difference between the E0C63404 and the E0C63P404 is that the E0C63P404 contains Flash EEPROM as the instruction ROM and data ROM that allows the user to write data to it using the exclusive ROM writer (UNIVERSAL ROM WRITER II). The E0C63P404 also has a built-in PROM programmer that controls writing data to the PROM.
This chapter explains the PROM programmer and the operating modes that are added for the programming operation.

2.1 Configuration of PROM Programmer

Figure 2.1.1 shows the configuration of the PROM programmer.

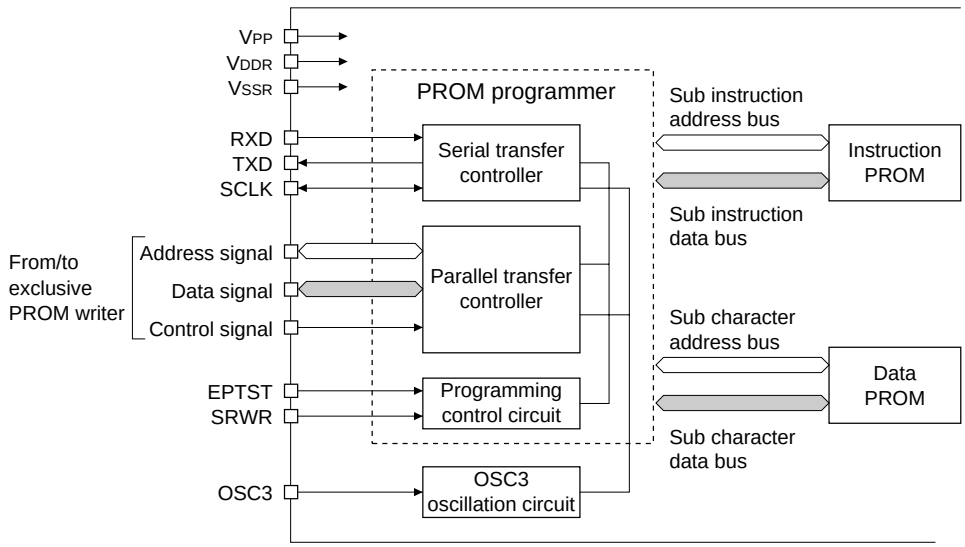


Fig. 2.1.1 Configuration of PROM programmer

The PROM programmer supports Serial Programming for writing data received in serial transfer and Parallel Programming that uses a parallel transfer. The programming method will be described later.

Terminals

The PROM programmer uses the following input/output terminals. The following sections will explain handling the terminals in each operating mode.

VDDR, VSSR: Power supply terminal for PROM

VPP: Power supply terminal for PROM programming

EPTST: PROM programming enable terminal (pull-down resistor built-in)

SRWR: PROM serial programming mode setting terminal (pull-down resistor built-in)

RXD: Serial data receive terminal (pull-up resistor built-in)

TXD: Serial data transmit terminal

SCLK: Serial clock input/output terminal (pull-up resistor built-in)

OSC3: OSC3 oscillation (1 MHz) input terminal

The parallel programming mode uses other terminals in addition to the terminals above. However, it is not necessary to switch the lines on the board, because the IC is programed by directly installing it to the exclusive PROM writer (UNIVERSAL ROM WRITER II).

2.2 Operating Modes

Three operating modes are available in the E0C63P404: one is for normal operation and the others are for programming.

1) Normal operation mode
2) PROM serial programming mode
3) PROM parallel programming mode

The operating mode is decided by the terminal settings at power on or initial reset.
Table 2.2.1 shows the terminals used for setting the mode.

Table 2.2.1 Operating mode setting terminals

Operating mode	Terminal settings	
	EPTST	SRWR
Normal operation mode	Low or Open	Low or Open
Serial programming mode	High	High

* The PROM writer sets the terminals in the parallel programming mode.
See Section 2.2.2 for terminal settings in the serial programming mode.

2.2.1 Normal operation mode

In this mode, the E0C63000 core CPU and the peripheral circuits operate by the programmed PROM. The CPU can enter this mode after the PROM programming has finished.
The PROM bit data is set to "1" at shipment. Therefore, the IC will not work even if the normal operation mode is set before programming.

In the normal operation mode, set the terminals for the PROM programmer as below. The board must be designed so that the terminal settings cannot be changed.

VDDR, VSSR: Supply the PROM power (4.5 V to 5.5 V) between the terminals. The same power supply for VDD and VSS can be used by connecting these terminals to VDD and VSS, respectively.

VPP: Supply a voltage the same as VDDR. In order to prevent damage to the IC, do not supply 12.5 V of programming voltage in the normal operation mode.

EPTST, SRWR: Open or fix at a Low level.

RXD, SCLK: Open or fix at a High level.

2.2.2 PROM serial programming mode

The PROM serial programming mode should be set when writing data to the PROM using a serial transfer from the exclusive PROM writer (UNIVERSAL ROM WRITER II). This mode will be mainly used for the programming of chip products, because the programming can be done even when the IC has already been mounted on the board.
To create data to be written to the instruction PROM and data PROM, use the E0C63 assembler similar to the E0C63404.

The following explains the procedure of PROM serial programming.

PROM serial programming procedure

(1) Set the required terminals for serial programming as follows:

VDDR, VSSR: Connect to the PROM power supply (4.5 V to 5.5 V). The same power supply for VDD and VSS can be used by connecting these terminals to VDD and VSS, respectively.

VPP: Connect to VPP on the PROM writer. The voltage (5 V/12.5 V) can be switched using the PROM writer.

Note: Be sure to set VPP to 5 V at the IC power on or initial reset. Note that the IC may be damaged if 12.5 V has been supplied to the VPP terminal at power on or initial reset.

EPTST: Set the terminal so that it will be fixed to a High level. (A switch should be provided on the target board to change the EPTST terminal level between High and Low.)

SRWR: Set the terminal so that it will be fixed at a High level.

Note: The EPTST and SRWR terminals must be fixed at a High level in the programming mode and at a Low level or open in the normal operation mode. Changing the voltage level may damage the IC.

RXD, TXD, SCLK: Connect to the PROM writer.

OSC3: Programming requires a 1 MHz OSC3 clock. When a different frequency is used or the OSC3 oscillation circuit is not used, supply a 1 MHz clock from the PROM writer at programming.
The PROM writer generates a 1 MHz clock with 5 V amplitude, note, however, that the E0C63P404 enables 2.1 V for High level voltage supplied to the OSC3 terminal. Therefore, the clock from the PROM writer cannot be input directly to the IC. Input the clock after shifting its level to 2.1 V by dividing the voltage with resistors provided on the target board as shown in Figure 2.2.2.1.

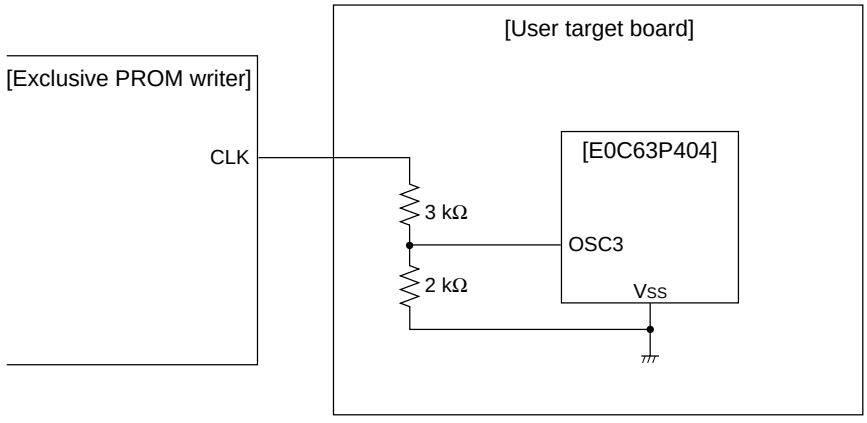
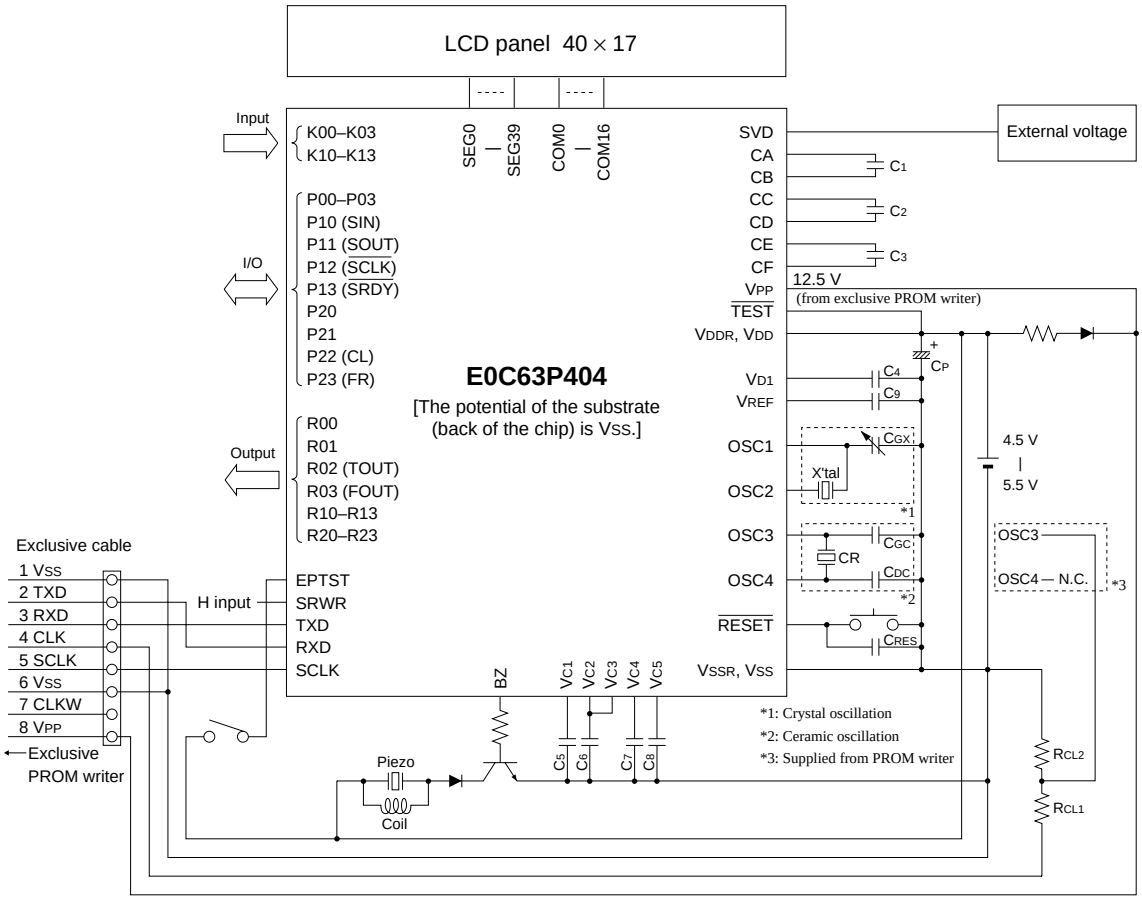


Fig. 2.2.2.1 How to supply a 1 MHz clock from the PROM writer to the OSC3 terminal

Figure 2.2.2.2 shows a sample connection diagram in the serial programming mode.



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	1 MHz (5.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
C1–C8	Capacitor	0.2 µF
C9	Capacitor	0.1 µF
CP	Capacitor	3.3 µF
CRES	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF
RCL1	Resistor	3 kΩ
RCL2	Resistor	2 kΩ

Note: This table is simply an example.

Fig. 2.2.2.2 Sample connection diagram in serial programming mode

Other terminals should be set as below.
Input port terminals (K): Fix at a High or Low level.
I/O port terminals (P): Fix at a High or Low level.
SVD terminal: Fix at a High level.
$\overline{\text{TEST}}$ terminal: Fix at a High level.

Supply a similar power voltage to the VDD and VSS terminals for the regular operation so that the OSC1 and OSC3 oscillation circuits operate normally.

(2) Turn the IC (user target board) power (+5 V) on.

(3) Turn the PROM writer on.

(4) Controls the $\overline{\text{RESET}}$ and EPTST terminals as shown in Figure 2.2.2.3.

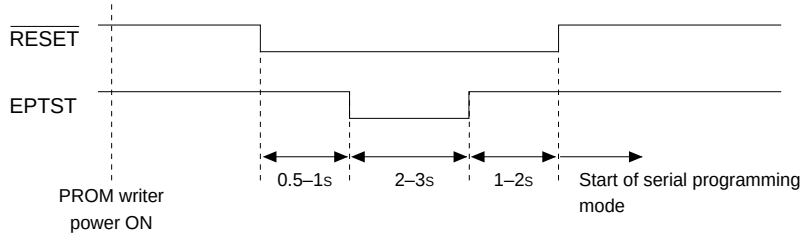


Fig. 2.2.2.3 Timing chart for entering serial programming mode

(5) Start up the romw63.exe in the personal computer, then load the 63p404.frm file. This allows serial programming to begin.

After setting this mode, data can be written to the exclusive PROM writer (UNIVERSAL ROM WRITER II). Refer to the "E0C63Pxxx Universal ROM Writer II User's Manual" for the connection and operation of the PROM writer.

2.2.3 PROM parallel programming mode

In the PROM parallel programming mode, the exclusive PROM writer (UNIVERSAL ROM WRITER II) transfers data in parallel to the IC installed on the PROM writer to write data to it. The terminal setting is done by the PROM writer. Thus there is no precaution on mode setting or board design.
Refer to the "E0C63Pxxx Universal ROM Writer II User's Manual" for the operation of the PROM writer.
To create data to be written to the instruction PROM and data PROM, use the E0C63 assembler the same as the E0C63404.

CHAPTER 3 DIFFERENCES FROM E0C63404

This chapter explains the differences on functions between the E0C63P404 and the E0C63404. The functions without description are the same in both models. Refer to the "E0C63404 Technical Manual" for the circuits and functions.

3.1 Terminal Configuration

The E0C63P404 has terminals for the PROM programmer in addition to the ones on the E0C63404. These terminals are assigned to the unused terminals of the E0C63404. The other terminals are the same configuration as the E0C63404.
Table 3.1.1 shows the terminal configuration and the terminal functions according to the operating mode.

Table 3.1.1 Terminal configuration

Pin name	Pin No.	Normal operation mode		Serial programming mode	
		I/O	Function	I/O	Function
V_{DD}	24	–	Power supply pin (+5 V)	–	Power supply pin (+5 V)
V_{SS}	18	–	Power supply pin (GND)	–	Power supply pin (GND)
V_{D1}	21	–	Internal regulated voltage output pin	–	Internal regulated voltage output pin
V_{C1}–V_{C4}	69–72	–	LCD system power supply pin	–	Unused
V_{C5}	73	–	LCD system power supply pin	–	Unused
V_{REF}	30	O	LCD system power supply testing pin	O	Unused
CA–CF	79–74	–	LCD system capacitor connecting pin	–	Unused
OSC1	19	I	Crystal oscillation input pin	I	Crystal oscillation input pin
OSC2	20	O	Crystal oscillation output pin	O	Crystal oscillation output pin
OSC3	22	I	Ceramic oscillation input pin	I	1 MHz oscillation input pin
OSC4	23	O	Ceramic oscillation output pin	O	1 MHz oscillation output pin
K00–03	64–61	I	Input port	I	Unused (High or Low)
K10	60	I	Input port	I	Unused (High or Low)
K11–13	59–57	I	Input port	I	Unused (High or Low)
P00–03	56–53	I/O	I/O port	I	Unused (High or Low)
P10–13	52–49	I/O	I/O port	I	Unused (High or Low)
P20–23	48–45	I/O	I/O port	I	Unused (High or Low)
R00–03	44–41	O	Output port	O	Unused
R10–13	40–37	O	Output port	O	Unused
R20–23	36–33	O	Output port	O	Unused
COM0–16	13–6, 80–88	O	LCD common output pin	O	Unused
SEG0–11	5–2, 127–120	O	LCD segment output pin	O	Unused
SEG12–15 (EXAD12–15)	119–116	O	LCD segment output pin	O	Unused
SEG16 ($\overline{ERD}$)	115	O	LCD segment output pin	O	Unused
SEG17 ($\overline{EWR}$)	114	O	LCD segment output pin	O	Unused
SEG18	113	O	LCD segment output pin	O	Unused
SEG19 (PCLK)	112	O	LCD segment output pin	O	Unused
SEG20–23 (EXD0–3)	111–108	O	LCD segment output pin	O	Unused
SEG24–SEG39	107–99, 95–89	O	LCD segment output pin	O	Unused
BZ	17	O	Sound output pin	O	Unused
SVD	66	I	SVD external voltage input pin	I	Unused (High)
$\overline{RESET}$	28	I	Initial reset input pin	I	Initial reset input pin
$\overline{TEST}$	29	I	Testing input pin (High or Open)	I	Unused (High)
SRWR *	128	I	Unused (Low or Open)	I	Serial programming setting (High)
EPTST *	1	I	Unused (Low or Open)	I	Programming mode setting (High)
RXD *	96	I	Unused (High or Open)	I	Serial data input pin
TXD *	98	O	Unused	O	Serial data output pin
SCLK *	97	I	Unused (High or Open)	I/O	Serial clock input/output pin
V_{DDR} *	14	–	Power supply pin for PROM (+5 V)	–	Power supply pin for PROM (+5 V)
V_{SSR} *	15	–	Power supply pin for PROM (GND)	–	Power supply pin for PROM (GND)
V_{PP} *	16	–	Power supply pin for PROM (+5 V)	–	PROM programming power supply (+5/12.5 V)

* They are N.C. (No Connection) terminals in the E0C63404.

In the parallel programming mode, all the terminals are set to the appropriate status by the exclusive PROM writer.

3.2 Mask Option

The E0C63P404 cannot specify the E0C63404 mask options individually.
The following option combination is provided for the E0C63P404:

Table 3.2.1 Combination of mask options

Mask option		Setting
OSC1 oscillation circuit		Crystal oscillation (32.768 kHz)
OSC3 oscillation circuit		Use <ceramic> or Not use
Multiple key entry reset combination		Not use
Multiple key entry reset time authorization		Not use
Input port pull up resistor	K00	With resistor
	K01	With resistor
	K02	With resistor
	K03	With resistor
	K10	With resistor
	K11	With resistor
	K12	With resistor
	K13	With resistor
Output port specification	R00	Complementary
	R01	Complementary
	R02	Complementary
	R03	Complementary
	R1x	Complementary
	R2x	Complementary
I/O port specification	P0x	Complementary
	P1x	Complementary
	P20	Complementary
	P21	Complementary
	P22	Complementary
	P23	Complementary
I/O port pull up resistor	P0x	With resistor
	P1x	With resistor
	P20	With resistor
	P21	With resistor
	P22	With resistor
	P23	With resistor
LCD drive power		Internal power supply
Serial interface polarity		Negative polarity
SVD circuit external voltage detection		Use
Sound generator buzzer output specification		Positive polarity

3.3 Power Supply

Supply voltage (V_{DD})

The operable voltage range is different.

E0C63404: 2.2 V to 6.4 V (Min. 1.8 V when the OSC3 oscillation circuit is not used.)
E0C63P404: 4.5 V to 5.5 V

Supply voltage for PROM (V_{DDR}, V_{SSR}, V_{PP})

Power supply terminals for PROM are added in the E0C63P404.

V_{DDR}: PROM power 4.5 V to 5.5 V (= V_{DD})
V_{SSR}: PROM ground 0 V (= V_{SS})
V_{PP}: PROM programming voltage in normal operation mode: V_{DDR}
in programming mode: 12.5 V
(The supplement of V_{PP} is controlled by the exclusive PROM writer in the programming mode.)

Operating voltage for oscillation circuit and internal circuits (V_{D1})

The V_{D1} voltage value is the same as the E0C63404.
During single clock operation: V_{D1} = 1.2 V
During twin clock operation: V_{D1} = 2.1 V

Since the E0C63P404 cannot use CR oscillation for the OSC1 oscillation circuit, the V_{D1} voltage is not fixed at 2.1 V. When using the E0C63P404 as a development tool for the E0C63404 (OSC1: CR oscillation circuit), be aware that even though it is unnecessary in the E0C63404, the E0C63P404 requires that the V_{D1} voltage be switched.

LCD drive voltage (V_{C1}–V_{C5})

The V_{C1}–V_{C5} voltage values are the same as the E0C63404.

Table 3.3.1 LCD drive voltage

LCD drive voltage	VCCHG = 0	VCCHG = 1
V_{C1} (0.975–1.2 V)	V_{C1} (standard)	$1/2 \times V_{C2}$
V_{C2} (1.950–2.4 V)	$2 \times V_{C1}$	V_{C2} (standard)
V_{C4} (2.925–3.6 V)	$3 \times V_{C1}$	$3/2 \times V_{C2}$
V_{C5} (3.900–4.8 V)	$4 \times V_{C1}$	$2 \times V_{C2}$

The E0C63P404 can select either V_{C1} standard (VCCHG = "0") or V_{C2} standard (VCCHG = "1") for generating the LCD drive voltage. V_{C2} standard is better for display quality and saving power. However, it is necessary to fix at V_{C1} standard when using the E0C63P404 as a development tool for the E0C63404 as the operating voltage will be 2.6 V or lower.

3.4 Initial Reset

Initial reset can be executed externally by setting the reset terminal to a Low level (VSS). After that the initial reset is released by setting the reset terminal to a High level (VDD) and the CPU starts operation. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 2 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 250 msec (when fOSC1 = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to High level. Be sure to maintain a reset input of 0.1 msec or more.
However, when turning the power on, the reset terminal should be set at a Low level as in the timing shown in Figure 3.4.1.

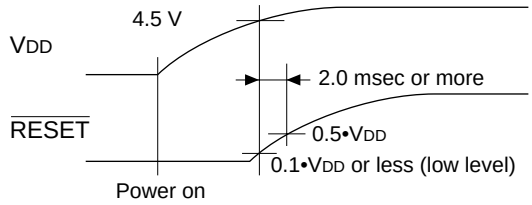


Fig. 3.4.1 Initial reset at power-on

The E0C63P404 uses initial reset as a trigger for setting either the normal operation mode or the programming mode. Therefore, design the reset input circuit so that the IC will be reset for sure. Initial resetting during operation is the same as the E0C63404.
When resetting the IC in the normal operation mode, make sure to fix the EPTST and SRWR terminals at a Low level. Moreover, the VPP terminal for PROM programming power supply must be fixed at 5 V during initial reset even when setting the programming mode. Do not reset the IC when 12.5 V is being supplied to the VPP terminal.

3.5 ROM

3.5.1 Instruction ROM

The E0C63P404 has employed a PROM for the instruction ROM. The memory capacity is the same as the E0C63404 at 4,096 × 13 bits.
The PROM can be rewritten up to 10 times. Rewriting data is done at the user's own risk.

3.5.2 Data ROM

The E0C63P404 has employed a PROM for the data ROM. The PROM has a capacity of 2,048 × 4 bits and is assigned to 8000H to 87FFH.
The PROM can be rewritten up to 10 times. Rewriting data is done at the user's own risk.

3.6 Oscillation Circuit

The E0C63P404 cannot use CR oscillation for the OSC1 and OSC3 oscillation circuits.
Therefore, the VD1 voltage is not fixed at 2.1 V. When using the E0C63P404 as a development tool for the E0C63404 (OSC1: CR oscillation circuit), be aware that even though it is unnecessary in the E0C63404, the E0C63P404 requires that the VD1 voltage be switched. Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure there is enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

3.7 SVD Circuit

The E0C63P404 has a 4-bit criteria voltage setting register (SVDS) the same as the E0C63404. The criteria voltage can be selected from among 16 types of voltage levels for internal voltage detection and one (1.05 V) for external voltage detection. However, the voltage levels of the E0C63P404 differ from the E0C63404 as shown in Tables 3.7.1 and 3.7.2. Be aware that the criteria voltage values of the E0C63P404 are provided as voltage ranges. The settings overlap each other, but the relation between the setting value and the criteria voltage is as follows:

SVD0–3 = 0 < 1 < 2 < ..... < 15

Table 3.7.1 SVD criteria voltage settings in E0C63404/63P404 (Internal voltage detection)

SVDS3	SVDS2	SVDS1	SVDS0	E0C63P404	E0C63404
0	0	0	0	1.55–2.15	1.85
0	0	0	1	1.60–2.20	1.90
0	0	1	0	1.70–2.30	2.00
0	0	1	1	1.80–2.40	2.10
0	1	0	0	1.90–2.50	2.20
0	1	0	1	2.00–2.60	2.30
0	1	1	0	2.10–2.70	2.40
0	1	1	1	2.20–2.80	2.50
1	0	0	0	2.30–2.90	2.60
1	0	0	1	2.40–3.00	2.70
1	0	1	0	2.50–3.10	2.80
1	0	1	1	2.60–3.20	2.90
1	1	0	0	2.70–3.30	3.00
1	1	0	1	2.80–3.40	3.10
1	1	1	0	2.90–3.50	3.20
1	1	1	1	3.00–3.60	3.30

Unit: V

Table 3.7.2 SVD criteria voltage setting in E0C63404/63P404 (External voltage detection)

SVDS3	SVDS2	SVDS1	SVDS0	E0C63P404	E0C63404
0	0	0	0	0.95–1.15	1.05

Unit: V

Table 3.7.3 I/O memory of E0C63P404 SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting (see Tables 3.7.1 and 3.7.2)
					SVDS2	0			
					SVDS1	0			
	R/W				SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set on the circuit

*3 Always "0" when being read

CHAPTER 4 SUMMARY OF NOTES

4.1 Notes Related to the PROM

(1) The PROM bit data is set to "1" at shipment. Therefore, It must be programmed before operating the IC in the normal operation mode.

(2) The PROM data can be rewritten up to 10 times for both the instruction and data PROMs.

(3) The circuit board should be designed so that the terminals can switch the input signals that differ between the PROM serial programming mode and the normal operation mode.

(4) The terminals for the PROM programmer should be set correctly according to the operating mode and fixed so that they cannot be changed during operation.
Especially the EPTST and SRWR terminals must be fixed at a High level in the programming mode, while they must be fixed at a Low level or must be opened in the normal operation mode. Changing the voltage level may damage the IC.

(5) Be sure to set V_{PP} to 5 V at the IC power on or initial reset regardless of the operating mode to be set. Note that the IC may be damaged if 12.5 V has been supplied to the V_{PP} terminal at power on or initial reset. To prevent damage of the IC, do not supply 12.5 V of programming voltage in the normal operation mode.

(6) Rewriting the PROM is done at on the user's own risk.

4.2 Notes on Differences form the E0C63404

Be aware of the following notes when using the E0C63P404 as a development tool for the E0C63404.

Power supply

(1) The E0C63P404 is operable with a supply voltage within the range of 4.5 V to 5.5 V. Be aware that the electrical characteristics differ from the E0C63404 due to the supply voltage used.

(2) The E0C63P404 operates normally even if either V_{C1} standard (VCCHG = "0") or V_{C2} standard (VCCHG = "1") is selected for generating the LCD drive voltage. However, it is necessary to fix at V_{C1} standard when developing an E0C63404 with an operating voltage of 2.6 V or lower voltage.

Initial reset

Note that the reset time differs from the E0C63404 due to the supply voltage used.

Oscillation circuit

The E0C63P404 cannot use CR oscillation for the OSC1 and OSC3 oscillation circuits.
Therefore, the V_{D1} voltage is not fixed at 2.1 V. When using the E0C63P404 as a development tool for the E0C63404 (OSC1: CR oscillation circuit), be aware that even though it is unnecessary in the E0C63404, the E0C63P404 requires that the V_{D1} voltage be switched. Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure there is enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

SVD circuit

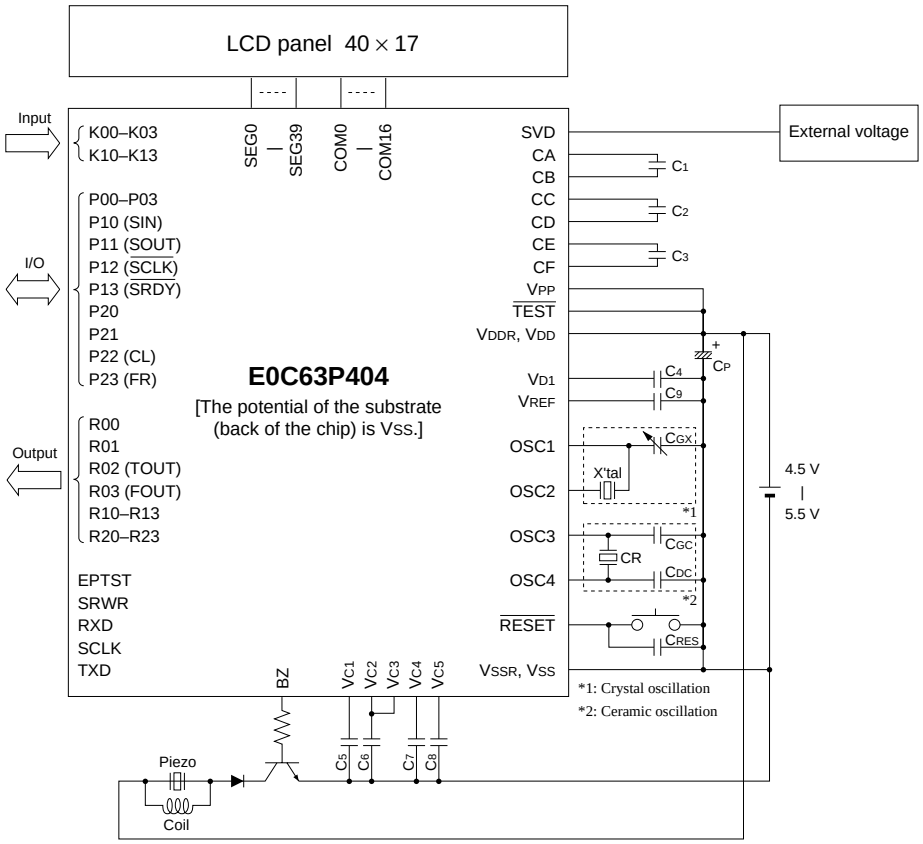
Note that the number of criteria voltage settings and the voltage values differ from the E0C63404.

CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

The connection diagrams shown below are reference sample circuits for when mask option settings are as follows:

OSC1: Crystal oscillation, OSC3: Ceramic oscillation, LCD power: Internal power, SVD external voltage detection: Used, BZ output: Positive polarity

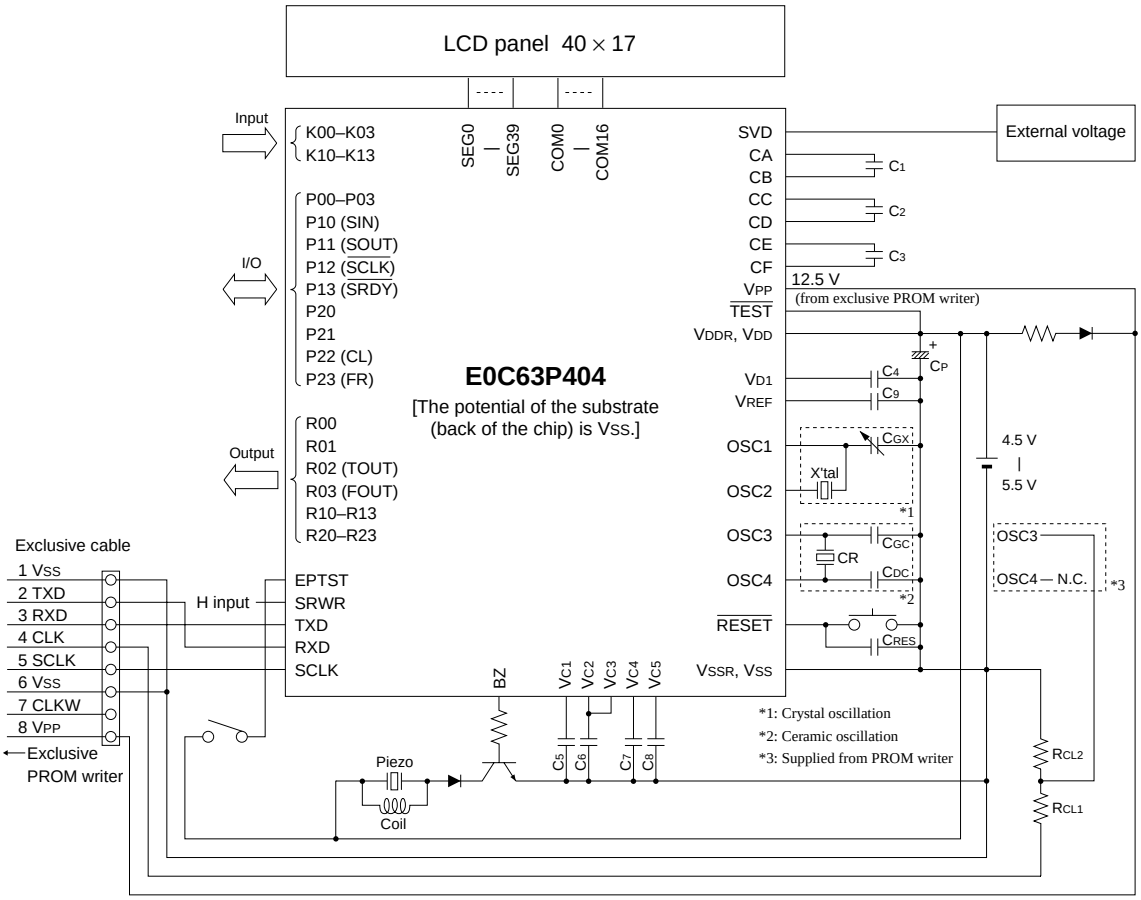
• *During normal operation*



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	1 MHz (5.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
C1–C8	Capacitor	0.2 µF
C9	Capacitor	0.1 µF
CP	Capacitor	3.3 µF
CRES	RESET terminal capacitor	0.1 µF

Note: This table is simply an example.

• *During PROM serial programming*



X'tal	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
CR	Ceramic oscillator	1 MHz (5.0 V)
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
C1–C8	Capacitor	0.2 µF
C9	Capacitor	0.1 µF
CP	Capacitor	3.3 µF
CRES	$\overline{\text{RESET}}$ terminal capacitor	0.1 µF
RCL1	Resistor	3 kΩ
RCL2	Resistor	2 kΩ

Note: This table is simply an example.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
PROM supply voltage (1)	V_{DDR}	-0.5 to 7.0	V
PROM supply voltage (2)	V_{PP}	-0.5 to 13.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{DD} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature	Topr	20 to 30	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package (QFP8-128pin).

6.2 Recommended Operating Conditions

(Ta=20 to 30°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	4.5	5.0	5.5	V
PROM supply voltage	V_{DDR}	V_{SSR}=0V	4.5	5.0	5.5	V
	V_{PP}	Normal operation mode	4.5	5.0	5.5	V
		Programming mode		12.5		V
Oscillation frequency	f_{OSC1}			32.768		kHz
	f_{OSC3}	Duty 50±5%, VDC="1", V_{DD}=5.0V		1,000		kHz
SVD terminal input voltage	V_{SVD}		0		5.5	V

6.3 DC Characteristics

Unless otherwise specified:

V_{DD}=V_{DDR}=5.0V, V_{SS}=V_{SSR}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03, K10–13 P00–03, P10–13, P20–23 RXD, SCLK, EPTST, SRWR	0.8·V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9·V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–03, K10–13 P00–03, P10–13, P20–23 RXD, SCLK, EPTST, SRWR	0		0.2·V_{DD}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1·V_{DD}	V
High level input current (1)	I_{IH1}	V_{IH1}=V_{DD} No Pull-down	K00–03, K10–13, P00–03 P10–13, P20–23, RXD, SCLK $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=V_{DD} With Pull-down	EPTST, SRWR	10	15	25	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No Pull-up	K00–03, K10–13, P00–03 P10–13, P20–23, EPTST, SRWR	-0.5		0	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With Pull-up	K00–03, K10–13, P00–03 P10–13, P20–23, RXD, SCLK $\overline{RESET}$, $\overline{TEST}$	-25	-15	-10	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, TXD, SCLK			-2.4	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9·V_{DD}	BZ			-2.4	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1·V_{DD}	R00–03, R10–13, R20–23, P00–03 P10–13, P20–23, TXD, SCLK	9.4			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1·V_{DD}	BZ	9.4			mA
Common output current	I_{OH3}	V_{OH3}=V_{C5}-0.05V	COM0–16			-30	µA
	I_{OL3}	V_{OL3}=V_{SS}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=V_{C5}-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{SS}+0.05V		10			µA

6.4 Analog Circuit Characteristics and Power Current Consumption

Unless otherwise specified:
V_{DD}=V_{DDR}=5.0V, V_{SS}=V_{SSR}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"		0.975		V
			LC0–3="1"		0.990		
			LC0–3="2"		1.005		
			LC0–3="3"		1.020		
			LC0–3="4"		1.035		
			LC0–3="5"		1.050		
			LC0–3="6"		1.065		
			LC0–3="7"		1.080		
			LC0–3="8"		1.095		
			LC0–3="9"		1.110		
			LC0–3="10"		1.125		
			LC0–3="11"		1.140		
			LC0–3="12"		1.155		
			LC0–3="13"		1.170		
			LC0–3="14"		1.185		
			LC0–3="15"		1.200		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)			2·V_{C1}		V
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)			3·V_{C1}		V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)			4·V_{C1}		V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)			1/2·V_{C2}		V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)	LC0–3="0"		1.95		V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"		2.16		
			LC0–3="8"		2.19		
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)			3/2·V_{C2}		V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)			2·V_{C2}		V

Unless otherwise specified:
V_{DD}=V_{DDR}=5.0V, V_{SS}=V_{SSR}=0V, f_{OSC1}=32.768kHz, C_G=25pF, Ta=25°C, V_{D1}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.2µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD1}	SVDS0–3="0" (internal)		1.55		2.15	V
		SVDS0–3="1"		1.60		2.20	
		SVDS0–3="2"		1.70		2.30	
		SVDS0–3="3"		1.80		2.40	
		SVDS0–3="4"		1.90		2.50	
		SVDS0–3="5"		2.00		2.60	
		SVDS0–3="6"		2.10		2.70	
		SVDS0–3="7"		2.20		2.80	
		SVDS0–3="8"		2.30		2.90	
		SVDS0–3="9"		2.40		3.00	
		SVDS0–3="10"		2.50		3.10	
		SVDS0–3="11"		2.60		3.20	
		SVDS0–3="12"		2.70		3.30	
		SVDS0–3="13"		2.80		3.40	
		SVDS0–3="14"		2.90		3.50	
		SVDS0–3="15"		3.00		3.60	
SVD voltage (external) *4	V_{SVD2}	SVDS0–3="0" (external)		0.95	1.05	1.15	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During HALT (32 kHz crystal oscillation)	LCD power OFF *1, *2, *3		1.0		µA
			LCD power ON (V_{C1} standard) *1, *2, *3		5.5		µA
			LCD power ON (V_{C2} standard) *1, *2, *3		4.0		µA
		During execution (32 kHz crystal oscillation)	LCD power ON (V_{C1} standard) *1, *2, *3		5.5		mA
		During execution (1 MHz ceramic oscillation)	LCD power ON (V_{C1} standard) *1		6.0		mA
		SVD circuit current (during supply voltage detection)			10.0		µA
		SVD circuit current (during external voltage detection)			3.0		µA
		During serial programming	Control from exclusive Flash writer		2.5		mA

*1 Without panel load. The SVD circuit is OFF.
*2 VDC = "0"
*3 OSCC = "0"
*4 Do not input a voltage out of the V_{DD}–V_{SS} range to the SVD terminal.

6.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified:
V_{DD}=V_{DDR}=5.0V, V_{SS}=V_{SSR}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})		4.5			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})		4.5			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)			14		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=4.5 to 5.5V	with VDC switching			5	ppm
			without VDC switching			10	ppm
Frequency/IC deviation	∂f/∂IC	C_G=5 to 25pF		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5pF (V_{DD})		20	25		ppm
Harmonic oscillation start voltage	V_{hho}	Between OSC1 and V_{SS}		5.5			V
Permitted leak resistance	R_{leak}			200			MΩ

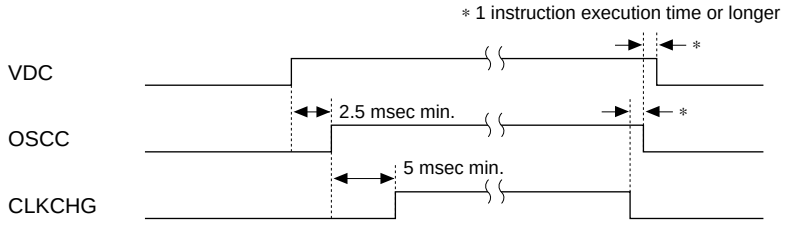
OSC3 ceramic oscillation circuit

Unless otherwise specified:
V_{DD}=V_{DDR}=5.0V, V_{SS}=V_{SSR}=0V, Ceramic oscillator: 1MHz, C_{GC}=C_{DC}=100pF, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	4.5			V
Oscillation start time	tsta	V_{DD}=4.5 to 5.5V			5	mS
Oscillation stop voltage	Vstp	(V_{DD})	4.5			V

6.6 Timing Chart

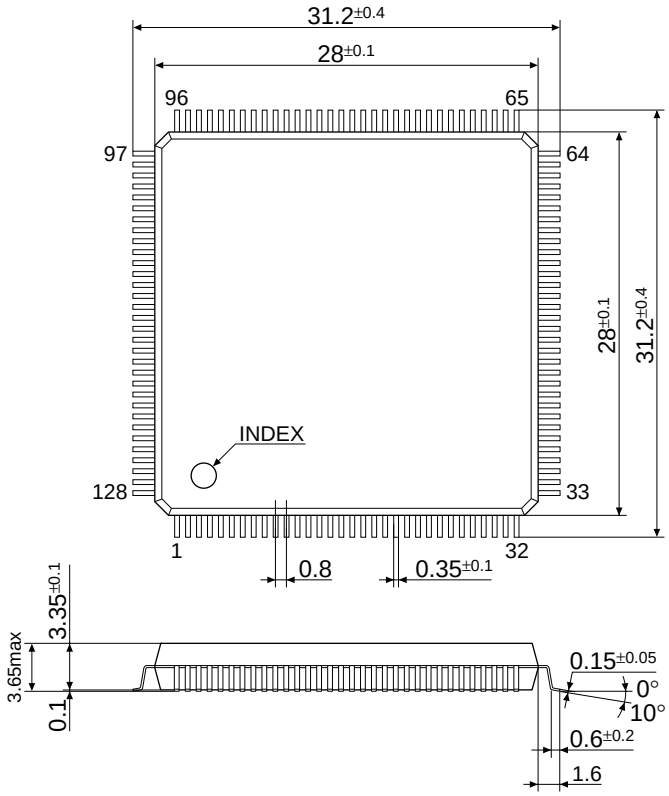
System clock switching



CHAPTER 7 PACKAGE

QFP8-128pin plastic package

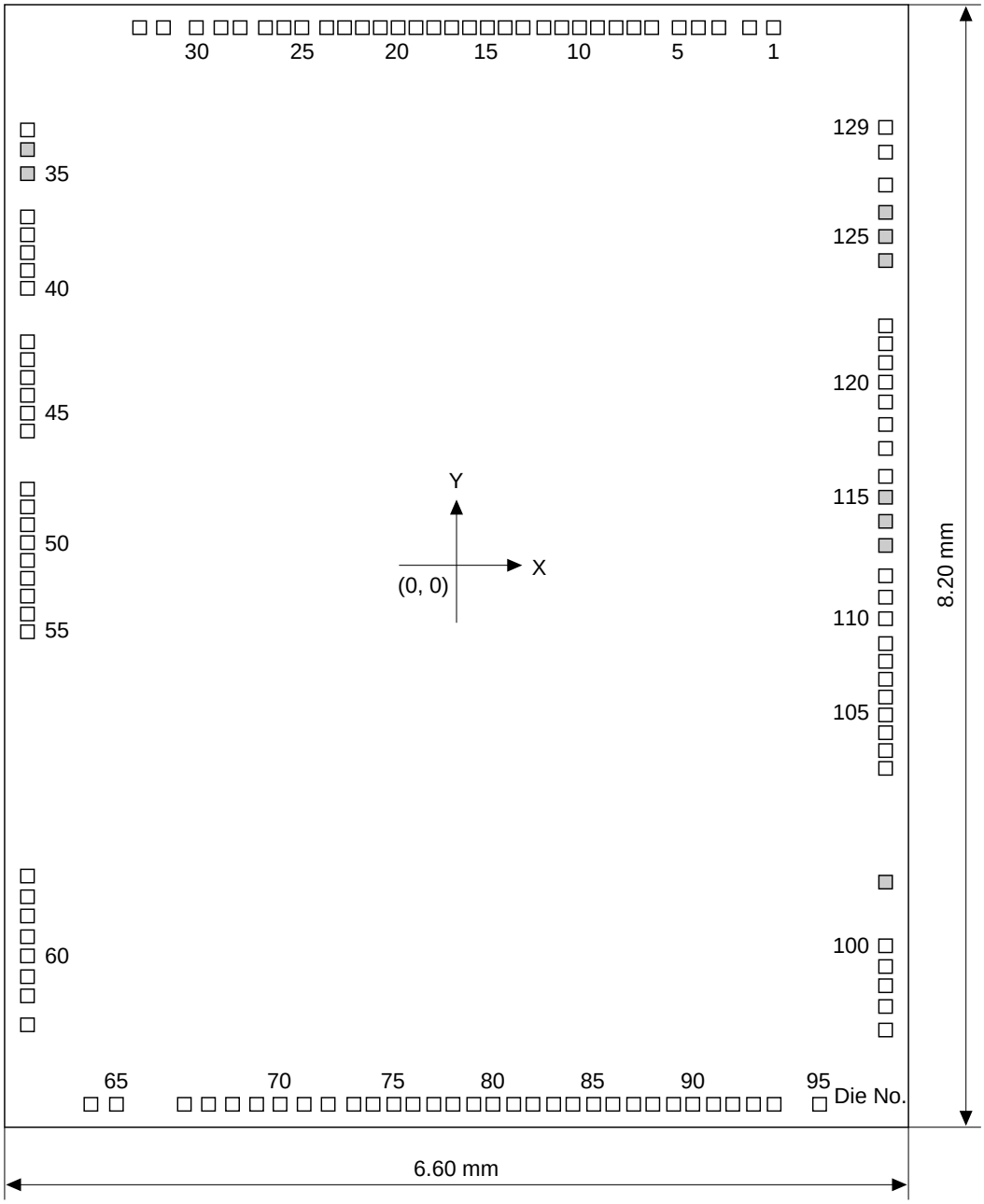
(Unit: mm)



The dimensions are subject to change without notice.

CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 98 µm

8.2 Pad Coordinates

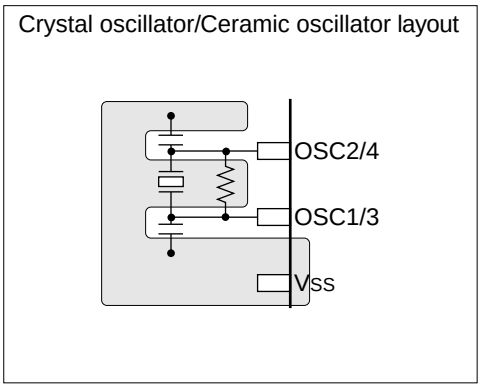
Unit: μm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	R23	2314.975	3932.500	44	CC	-3133.000	1246.375	87	SEG11	1293.175	-3932.500
2	R22	2140.125	3932.500	45	CB	-3133.000	1116.050	88	SEG10	1433.575	-3932.500
3	R21	1915.225	3932.500	46	CA	-3133.000	985.725	89	SEG9	1585.025	-3932.500
4	R20	1766.050	3932.500	47	COM8	-3133.000	561.925	90	SEG8	1725.425	-3932.500
5	R13	1625.650	3932.500	48	COM9	-3133.000	431.275	91	SEG7	1876.875	-3932.500
6	R12	1425.450	3932.500	49	COM10	-3133.000	301.275	92	SEG6	2017.275	-3932.500
7	R11	1295.450	3932.500	50	COM11	-3133.000	170.625	93	SEG5	2168.725	-3932.500
8	R10	1164.800	3932.500	51	COM12	-3133.000	40.625	94	SEG4	2319.200	-3932.500
9	R03	1028.950	3932.500	52	COM13	-3133.000	-90.025	95	SRWR	2651.025	-3932.500
10	R02	898.300	3932.500	53	COM14	-3133.000	-220.025	96	EPTST	3133.000	-3389.750
11	R01	768.300	3932.500	54	COM15	-3133.000	-350.675	97	SEG3	3133.000	-3217.825
12	R00	637.650	3932.500	55	COM16	-3133.000	-480.675	98	SEG2	3133.000	-3066.375
13	P23	485.875	3932.500	56	SEG39	-3133.000	-2264.925	99	SEG1	3133.000	-2925.975
14	P22	355.225	3932.500	57	SEG38	-3133.000	-2416.375	100	SEG0	3133.000	-2774.525
15	P21	225.225	3932.500	58	SEG37	-3133.000	-2556.775	101	N.C.	3133.000	-2309.450
16	P20	94.575	3932.500	59	SEG36	-3133.000	-2708.225	102	COM7	3133.000	-1478.425
17	P13	-35.425	3932.500	60	SEG35	-3133.000	-2848.625	103	COM6	3133.000	-1348.425
18	P12	-166.075	3932.500	61	SEG34	-3133.000	-3000.075	104	COM5	3133.000	-1218.100
19	P11	-296.075	3932.500	62	SEG33	-3133.000	-3140.475	105	COM4	3133.000	-1088.100
20	P10	-426.725	3932.500	63	RXD	-3133.000	-3351.725	106	COM3	3133.000	-957.450
21	P03	-556.725	3932.500	64	SCLK	-2669.875	-3932.500	107	COM2	3133.000	-827.450
22	P02	-687.375	3932.500	65	TXD	-2483.325	-3932.500	108	COM1	3133.000	-696.800
23	P01	-817.375	3932.500	66	SEG32	-1987.375	-3932.500	109	COM0	3133.000	-566.800
24	P00	-948.025	3932.500	67	SEG31	-1811.225	-3932.500	110	V_{DDR}	3133.000	-385.125
25	K13	-1129.375	3932.500	68	SEG30	-1635.725	-3932.500	111	V_{SSR}	3133.000	-227.825
26	K12	-1260.025	3932.500	69	SEG29	-1459.575	-3932.500	112	V_{PP}	3133.000	-72.150
27	K11	-1395.225	3932.500	70	SEG28	-1288.950	-3932.500	113	N.C.	3133.000	149.825
28	K10	-1580.150	3932.500	71	SEG27	-1112.800	-3932.500	114	N.C.	3133.000	325.975
29	K03	-1720.225	3932.500	72	SEG26	-937.300	-3932.500	115	N.C.	3133.000	502.125
30	K02	-1899.950	3932.500	73	SEG25	-749.775	-3932.500	116	BZ	3133.000	654.225
31	K01	-2140.125	3932.500	74	SEG24	-609.375	-3932.500	117	V_{SS}	3133.000	858.650
32	K00	-2314.000	3932.500	75	SEG23	-457.925	-3932.500	118	OSC1	3133.000	1033.500
33	SVD	-3133.000	3185.000	76	SEG22	-317.525	-3932.500	119	OSC2	3133.000	1197.950
34	N.C.	-3133.000	3041.675	77	SEG21	-166.075	-3932.500	120	V_{D1}	3133.000	1342.575
35	N.C.	-3133.000	2865.525	78	SEG20	-25.675	-3932.500	121	OSC3	3133.000	1485.250
36	V_{C1}	-3133.000	2549.950	79	SEG19	125.775	-3932.500	122	OSC4	3133.000	1623.375
37	V_{C2}	-3133.000	2419.300	80	SEG18	266.175	-3932.500	123	V_{DD}	3133.000	1753.700
38	V_{C3}	-3133.000	2288.975	81	SEG17	417.625	-3932.500	124	N.C.	3133.000	2230.800
39	V_{C4}	-3133.000	2158.650	82	SEG16	558.025	-3932.500	125	N.C.	3133.000	2406.950
40	V_{C5}	-3133.000	2028.325	83	SEG15	709.475	-3932.500	126	N.C.	3133.000	2583.100
41	CF	-3133.000	1637.675	84	SEG14	849.875	-3932.500	127	$\overline{RESET}$	3133.000	2782.325
42	CE	-3133.000	1507.350	85	SEG13	1001.325	-3932.500	128	$\overline{TEST}$	3133.000	3022.825
43	CD	-3133.000	1376.700	86	SEG12	1141.725	-3932.500	129	V_{REF}	3133.000	3203.850

N.C. : No Connection

CHAPTER 9 IMPLEMENT OF NOTES

- When using the crystal oscillation circuit and ceramic oscillation circuit, make a board pattern with noise measure as shown below.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 and VDD, please keep enough distance between VDD and other signals on the board pattern.

- Precautions for Visible Radiation
  Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 10 I/O MAP

E0C63P404 I/O MAP (1/5)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF00H	CLKCHG	OSCC	0	VDC	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W		R	R/W	0 *3	– *2			Unused
					VDC	0	2.1 V	1.2 V	CPU operating voltage switch (1.2 V: OSC1, 2.1 V: OSC3)
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting (see Tables 3.7.1 and 3.7.2)
					SVDS2	0			
	R/W				SVDS1	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	0	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT output enable
					0 *3	– *2			Unused
	R/W	R	R/W		FOFQ1	0			FOUT frequency selection [FOFQ1, 0] 0 1 2 3 / Frequency fOSC1/64 fOSC1/8 fOSC1 fOSC3
					FOFQ0	0			
FF07H	0	0	WDEN	WDRST	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF20H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
	R/W				SIK01	0	Enable	Disable	
					SIK00	0	Enable	Disable	
FF21H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF22H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
	R/W				KCP01	1	↓	↑	
					KCP00	1	↓	↑	
FF24H	SIK13	SIK12	SIK11	SIK10	SIK13	0	Enable	Disable	K10–K13 interrupt selection register
					SIK12	0	Enable	Disable	
	R/W				SIK11	0	Enable	Disable	
					SIK10	0	Enable	Disable	
FF25H	K13	K12	K11	K10	K13	– *2	High	Low	K10–K13 input port data
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	
FF26H	KCP13	KCP12	KCP11	KCP10	KCP13	1	↓	↑	K10–K13 input comparison register
					KCP12	1	↓	↑	
	R/W				KCP11	1	↓	↑	
					KCP10	1	↓	↑	
FF30H	R03HIZ	R02HIZ	R01HIZ	R00HIZ	R03HIZ	0	High-Z	Output	R03 output high impedance control (FOUTE=0) / FOUT output high impedance control (FOUTE=1)
					R02HIZ	0	High-Z	Output	R02 output high impedance control (PTOUT=0) / TOUT output high impedance control (PTOUT=1)
	R/W				R01HIZ	0	High-Z	Output	R01 output high impedance control
					R00HIZ	0	High-Z	Output	R00 output high impedance control
FF31H	R03	R02	R01	R00	R03	1	High	Low	R03 output port data (FOUTE=0) Fix at "1" when FOUT is used
					R02	1	High	Low	R02 output port data (PTOUT=0) Fix at "1" when TOUT is used
	R/W				R01	1	High	Low	R01 output port data
					R00	1	High	Low	R00 output port data

*1 Initial value at initial reset

*2 Not set on the circuit

*3 Always "0" when being read

E0C63P404 I/O MAP (2/5)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF32H	0	0	0	R1HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R1HIZ	0	High-Z	Output	R1 output high impedance control
FF33H	R13	R12	R11	R10	R13	1	High	Low	R10–R13 output port data
					R12	1	High	Low	
	R/W				R11	1	High	Low	
					R10	1	High	Low	
FF34H	0	0	0	R2HIZ	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					R2HIZ	0	High-Z	Output	R2 output high impedance control
FF35H	R23	R22	R21	R20	R23	1	High	Low	R20–R23 output port data
					R22	1	High	Low	
	R/W				R21	1	High	Low	
					R20	1	High	Low	
FF40H	IOC03	IOC02	IOC01	IOC00	IOC03	0	Output	Input	P00–P03 I/O control register
					IOC02	0	Output	Input	
	R/W				IOC01	0	Output	Input	
					IOC00	0	Output	Input	
FF41H	PUL03	PUL02	PUL01	PUL00	PUL03	1	On	Off	P00–P03 pull-up control register
					PUL02	1	On	Off	
	R/W				PUL01	1	On	Off	
					PUL00	1	On	Off	
FF42H	P03	P02	P01	P00	P03	– *2	High	Low	P00–P03 I/O port data
					P02	– *2	High	Low	
	R/W				P01	– *2	High	Low	
					P00	– *2	High	Low	
FF44H	IOC13	IOC12	IOC11	IOC10	IOC13	0	Output	Input	P13 I/O control register functions as a general-purpose register when SIF (slave) is selected
					IOC12	0	Output	Input	P12 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
	R/W				IOC11	0	Output	Input	P11 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
					IOC10	0	Output	Input	P10 I/O control register (EISF=0) functions as a general-purpose register when SIF is selected
FF45H	PUL13	PUL12	PUL11	PUL10	PUL13	1	On	Off	P13 pull-up control register functions as a general-purpose register when SIF (slave) is selected
					PUL12	1	On	Off	P12 pull-up control register (EISF=0) functions as a general-purpose register when SIF (master) is selected $\overline{SCLK}$ (I) pull-up control register when SIF (slave) is selected
	R/W				PUL11	1	On	Off	P11 pull-up control register (EISF=0) functions as a general-purpose register when SIF is selected
					PUL10	1	On	Off	P10 pull-up control register (EISF=0) SIN pull-up control register when SIF is selected
FF46H	P13	P12	P11	P10	P13	– *2	High	Low	P13 I/O port data functions as a general-purpose register when SIF (slave) is selected
					P12	– *2	High	Low	P12 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
	R/W				P11	– *2	High	Low	P11 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected
					P10	– *2	High	Low	P10 I/O port data (EISF=0) functions as a general-purpose register when SIF is selected

E0C63P404 I/O MAP (3/5)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register (EXLCDC=0) functions as a general-purpose register when FR output is selected
					IOC22	0	Output	Input	P22 I/O control register (EXLCDC=0) functions as a general-purpose register when CL output is selected
	R/W				IOC21	0	Output	Input	P21 I/O control register
					IOC20	0	Output	Input	P20 I/O control register
FF49H	PUL23	PUL22	PUL21	PUL20	PUL23	1	On	Off	P23 pull-up control register (EXLCDC=0) functions as a general-purpose register when FR output is selected
					PUL22	1	On	Off	P22 pull-up control register (EXLCDC=0) functions as a general-purpose register when CL output is selected
	R/W				PUL21	1	On	Off	P21 pull-up control register
					PUL20	1	On	Off	P20 pull-up control register
FF4AH	P23	P22	P21	P20	P23	– *2	High	Low	P23 I/O port data (EXLCDC=0) functions as a general-purpose register when FR output is selected
					P22	– *2	High	Low	P22 I/O port data (EXLCDC=0) functions as a general-purpose register when CL output is selected
	R/W				P21	– *2	High	Low	P21 I/O port data
					P20	– *2	High	Low	P20 I/O port data
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0			LCD drive duty switch [LDUTY1, 0]: 0 = Duty 1/17; 1 = 1/16; 2, 3 = 1/8
					LDUTY0	0			
	R/W				VCCHG	0	V_{C2}	V_{C1}	LCD regulated voltage switch
					LPWR	0	On	Off	LCD power On/Off
FF61H	EXLCDC	ALOFF	ALON	LPAGE	EXLCDC	0	Enable	Disable	Expanded LCD driver signal control
					ALOFF	1	All Off	Normal	LCD all OFF control
					ALON	0	All On	Normal	LCD all ON control
	R/W				LPAGE	0	F100-F14F	F000-F04F	Display memory area selection (when 1/8 duty is selected) functions as a general-purpose register when 1/16, 1/17 duty is selected
FF62H	LC3	LC2	LC1	LC0	LC3	– *2			LCD contrast adjustment [LC3–0]: 0 – 15 Contrast: Light – Dark
					LC2	– *2			
	R/W				LC1	– *2			
					LC0	– *2			
FF6CH	ENRTM	ENRST	ENON	BZE	ENRTM	0	1 sec	0.5 sec	Envelope releasing time
					ENRST*3	Reset	Reset	Invalid	Envelope reset (writing)
	R/W	W	R/W		ENON	0	On	Off	Envelope On/Off
					BZE	0	Enable	Disable	Buzzer output enable
FF6DH	0	BZSTP	BZSHT	SHTPW	0 *3	– *2			Unused
					BZSTP*3	0	Stop	Invalid	1-shot buzzer stop (writing)
					BZSHT	0	Trigger	Invalid	1-shot buzzer trigger (writing)
	R	W	R/W				Busy	Ready	1-shot buzzer status (reading)
					SHTPW	0	125 msec	31.25 msec	1-shot buzzer pulse width setting
FF6EH	0	BZFQ2	BZFQ1	BZFQ0	0 *3	– *2			Unused
					BZFQ2	0			Buzzer frequency selection [BZFQ2, 1, 0]: 0 = Frequency (Hz) 4096.0; 1 = 3276.8; 2 = 2730.7; 3 = 2340.6 [BZFQ2, 1, 0]: 4 = Frequency (Hz) 2048.0; 5 = 1638.4; 6 = 1365.3; 7 = 1170.3
					BZFQ1	0			
	R	R/W			BZFQ0	0			
FF6FH	0	BDTY2	BDTY1	BDTY0	0 *3	– *2			Unused
					BDTY2	0			Buzzer signal duty ratio selection (refer to main manual)
					BDTY1	0			
	R	R/W			BDTY0	0			
FF70H	0	0	SCTRG	ESIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
					SCTRG	0	Trigger	Invalid	Serial I/F clock trigger (writing)
	R		R/W				Run	Stop	Serial I/F clock status (reading)
					ESIF	0	SIF	I/O	Serial I/F enable (P1 port function selection)
FF71H	SDP	SCPS	SCS1	SCS0	SDP	0	MSB first	LSB first	Serial I/F data input/output permutation
					SCPS	0	↓	↓	Serial I/F clock phase selection –Negative polarity (mask option) –Positive polarity (mask option)
	R/W				SCS1	0			Serial I/F clock mode selection [SCS1, 0]: 0 = Clock Slave; 1 = PT [SCS1, 0]: 2 = Clock OSC1/2; 3 = OSC1
					SCS0	0			

E0C63P404 I/O MAP (4/5)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF72H	SD3	SD2	SD1	SD0	SD3	– *2	High	Low	MSB
					SD2	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					SD1	– *2	High	Low	
	R/W				SD0	– *2	High	Low	LSB
FF73H	SD7	SD6	SD5	SD4	SD7	– *2	High	Low	MSB
					SD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					SD5	– *2	High	Low	
	R/W				SD4	– *2	High	Low	LSB
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
					TM1	0			Clock timer data (64 Hz)
	R				TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
					TM5	0			Clock timer data (4 Hz)
	R				TM4	0			Clock timer data (8 Hz)
FF7CH	0	0	SWRST	SWRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data
					SWD2	0			BCD (1/100 sec)
					SWD1	0			
	R				SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data
					SWD6	0			BCD (1/10 sec)
					SWD5	0			
	R				SWD4	0			
FFC0H	0	EVCNT	FCSEL	PLPOL	0 *3	– *2			Unused
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
					FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
	R	R/W			PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
	R/W				CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
					RLD01	0			
	R/W				RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
					RLD05	0			
	R/W				RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
					RLD11	0			
	R/W				RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
					RLD15	0			
	R/W				RLD14	0			LSB

E0C63P404 I/O MAP (5/5)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
	R				PTD01	0			
					PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
	R				PTD05	0			
					PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
	R				PTD11	0			
					PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
	R				PTD15	0			
					PTD14	0			LSB
FFE2H	0	0	EIPT1	EIPT0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	0	0	0	EISIF	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EISIF	0	Enable	Mask	Interrupt mask register (Serial I/F)
FFE4H	0	0	0	EIK0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK0	0	Enable	Mask	Interrupt mask register (K00–K03)
FFE5H	0	0	0	EIK1	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	0 *3	– *2			Unused
					EIK1	0	Enable	Mask	Interrupt mask register (K10–K13)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE7H	0	0	EISW1	EISW10	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	0	0	ISIF	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					ISIF	0	Reset	Invalid	Interrupt factor flag (Serial I/F)
FFF4H	0	0	0	IK0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK0	0	Reset	Invalid	Interrupt factor flag (K00–K03)
FFF5H	0	0	0	IK1	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R			R/W	0 *3	– *2	(W)	(W)	Unused
					IK1	0	Reset	Invalid	Interrupt factor flag (K10–K13)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

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