EPSON

E0C88862

8-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Large Capacity ROM (60K bytes)
- Low Current Consumption
- Wide-range Operating Voltage (1.8V to 5.5V)
- High Speed Operation in Low Voltage (0.48µsec/3.0V)

■ DESCRIPTION

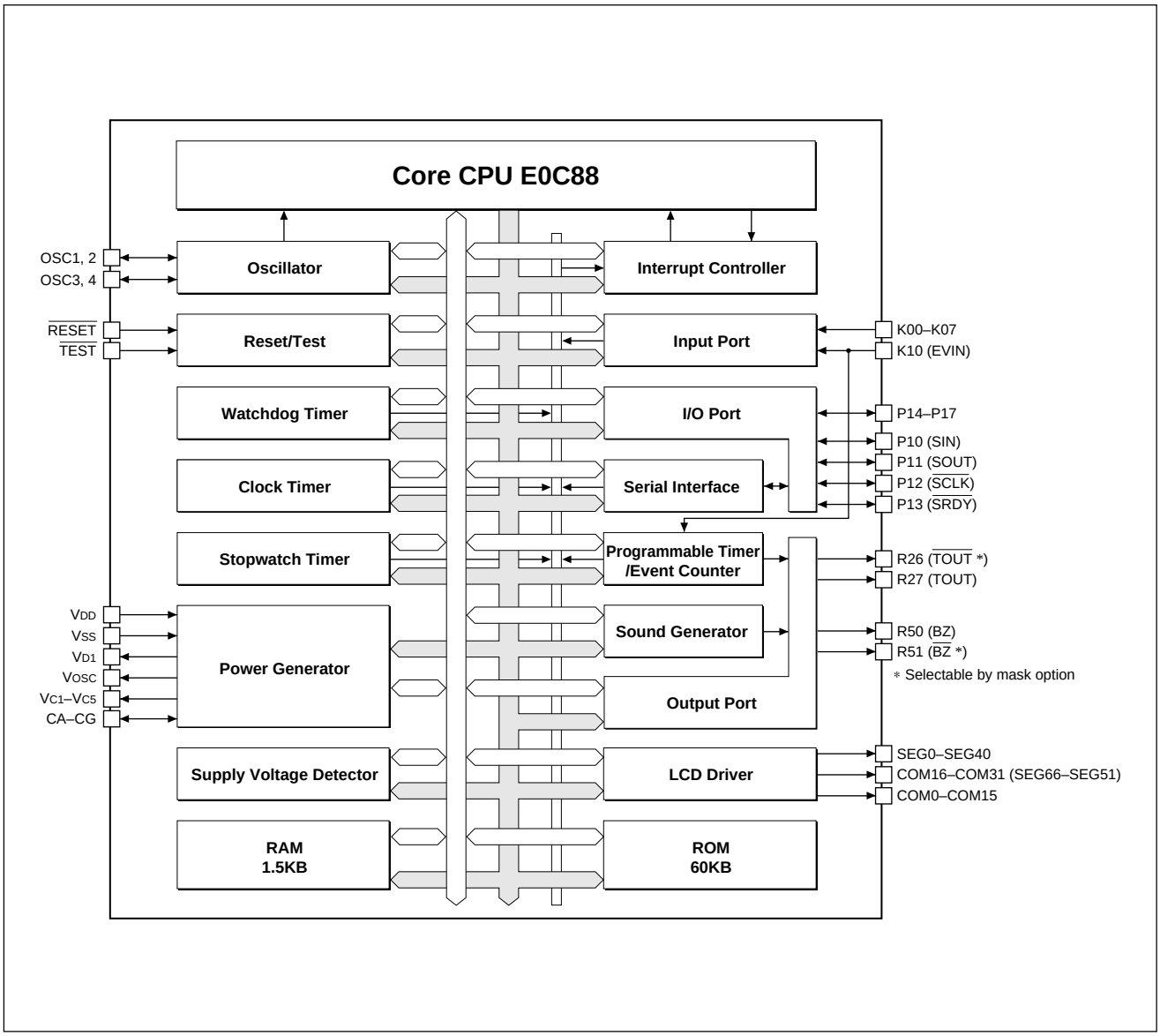
The E0C88862 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU, ROM, RAM, I/O, serial interface, dot-matrix LCD driver, timer and event counter. The E0C88862 fully operable over a wide range of voltages, and can perform high speed operations even at low voltage and low current consumption, it is suitable for portable systems that need to be driven with a battery.

■ FEATURES

- CMOS LSI 8-bit parallel processing
- Twin clock ..... OSC1 : 32.768kHz (Typ.)
  OSC3 : 8.2MHz (Max.)
- Instruction execution time ..... 0.244µsec (Min.)
- Multiplication and division instructions included
- ROM capacity 60K-byte
- RAM capacity ..... 1.5K-byte (RAM)
  2,736 (Display RAM)
- I/O port ..... Input only : 9 bits (EVIN is available by software)
  Output only : 4 bits (BZ, $\overline{BZ}$, TOUT and $\overline{TOUT}$ are available by software)
  Bidirectional I/O : 8 bits ($\overline{SRDY}$, $\overline{SCLK}$, SIN and SOUT are available by software)
- Serial interface ..... 1 channel (Clock synchronous or Asynchronous can be selected by software)
- Power supply circuit to drive liquid crystals .. Built-in (booster type, 5 potentials/4 potentials)
- LCD driver ..... Dot-matrix type (5 × 8 or 5 × 5)
  51 segments × 32 commons
  57 segments × 16 commons
  57 segments × 8 commons
- Timer ..... 8-bit programmable timer/event counter : 2 channels
  (16-bit 1 channel timer is available)
  Clock timer (8 bits) : 1 channel
  Stopwatch timer (8 bits) : 1 channel
- Sound generator ..... Envelope function, equipped with volume control
- Watchdog timer ..... Built-in
- Supply voltage detection (SVD) circuit .... 16 levels can be detected
- Interrupt ..... External : Input interrupt 2 systems (3 types)
  Internal : Timer interrupt 3 systems (9 types)
  : Serial I/F interrupt 1 system (3 types)

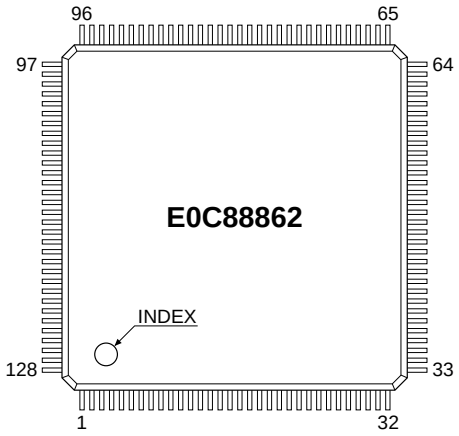
- Supply voltage ..... Normal mode : 2.4V to 5.5V (Max. 4.2MHz)
  Low power mode : 1.8V to 3.5V (Max. 80kHz)
  High speed mode : 3.5V to 5.5V (Max. 8.2MHz)
- Current consumption ..... SLEEP mode 0.3µA (Normal mode)
  HALT mode 1.5µA (32.768kHz/Normal mode)
  RUN mode 9µA (32.768kHz/Normal mode)
  1.1mA (4MHz/Normal mode)
- Package ..... QFP8-128pin (plastic), QFP15-128pin (plastic)

■ BLOCK DIAGRAM

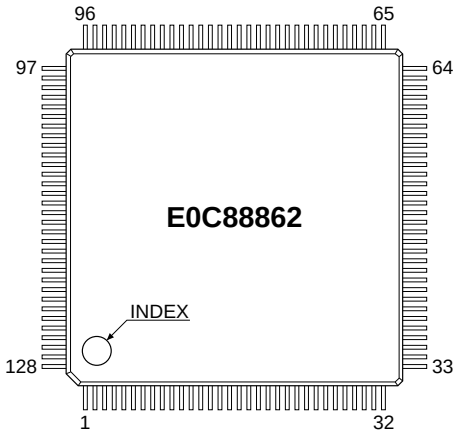


■ PIN CONFIGURATION

QFP8-128pin



QFP15-128pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	33	N.C.	65	N.C.	97	N.C.
2	N.C.	34	COM15	66	V_{OSC}	98	N.C.
3	N.C.	35	COM14	67	V_{D1}	99	N.C.
4	SEG28	36	COM13	68	V_{DD}	100	N.C.
5	SEG29	37	COM12	69	V_{SS}	101	SEG0
6	SEG30	38	COM11	70	OSC1	102	SEG1
7	SEG31	39	COM10	71	OSC2	103	SEG2
8	SEG32	40	COM9	72	$\overline{TEST}$	104	SEG3
9	SEG33	41	COM8	73	$\overline{RESET}$	105	SEG4
10	SEG34	42	COM7	74	K10/EVIN	106	SEG5
11	SEG35	43	COM6	75	K07	107	SEG6
12	SEG36	44	COM5	76	K06	108	SEG7
13	SEG37	45	COM4	77	K05	109	SEG8
14	SEG38	46	COM3	78	K04	110	SEG9
15	SEG39	47	COM2	79	K03	111	SEG10
16	SEG40	48	COM1	80	K02	112	SEG11
17	COM31/SEG51	49	COM0	81	K01	113	SEG12
18	COM30/SEG52	50	CG	82	K00	114	SEG13
19	COM29/SEG53	51	CF	83	P17	115	SEG14
20	COM28/SEG54	52	CE	84	P16	116	SEG15
21	COM27/SEG55	53	CD	85	P15	117	SEG16
22	COM26/SEG56	54	CC	86	P14	118	SEG17
23	COM25/SEG57	55	CB	87	P13/$\overline{SRDY}$	119	SEG18
24	COM24/SEG58	56	CA	88	P12/$\overline{SCLK}$	120	SEG19
25	COM23/SEG59	57	V_{C5}	89	P11/SOUT	121	SEG20
26	COM22/SEG60	58	V_{C4}	90	P10/SIN	122	SEG21
27	COM21/SEG61	59	V_{C3}	91	R26/$\overline{TOUT}$	123	SEG22
28	COM20/SEG62	60	V_{C2}	92	R27/TOUT	124	SEG23
29	COM19/SEG63	61	V_{C1}	93	R50/BZ	125	SEG24
30	COM18/SEG64	62	OSC3	94	R51/$\overline{BZ}$	126	SEG25
31	COM17/SEG65	63	OSC4	95	N.C.	127	SEG26
32	COM16/SEG66	64	N.C.	96	N.C.	128	SEG27

N.C.: No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	68	–	Power supply (+) terminal
V_{SS}	69	–	Power supply (GND) terminal
V_{D1}	67	–	Regulated voltage for internal circuit
V_{OSC}	66	–	Regulated voltage for OSC1 oscillation circuit
V_{C1}–V_{C5}	61–57	O	LCD drive voltage output terminals
CA–CG	56–50	–	Booster capacitor connection terminals for LCD
OSC1	70	I	OSC1 oscillation input terminal (select crystal oscillation/CR oscillation/external clock input with mask option)
OSC2	71	O	OSC1 oscillation output terminal
OSC3	62	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation/external clock input with mask option)
OSC4	63	O	OSC3 oscillation output terminal
K00–K07	82–75	I	Input terminals (K00–K07)
K10/EVIN	74	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
R26/$\overline{\text{TOUT}}$	91	O	Output terminal (R26) or programmable timer underflow signal inverted output terminal ($\overline{\text{TOUT}}$) (selectable by mask option)
R27/TOUT	92	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R50/BZ	93	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{\text{BZ}}$	94	O	Output terminal (R51) or buzzer inverted output terminal ($\overline{\text{BZ}}$) (selectable by mask option)
P10/SIN	90	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	89	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	88	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	87	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14–P17	86–83	I/O	I/O terminals (P14–P17)
COM0–COM15	49–34	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	32–17	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 or 1/8 duty is selected)
SEG0–SEG40	101–128, 4–16	O	LCD segment output terminals
$\overline{\text{RESET}}$	73	I	Initial reset input terminal
$\overline{\text{TEST}}$ *1	72	I	Test input terminal

*1 $\overline{\text{TEST}}$ is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V_{DD}.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Condition	Value	Unit	Note
Power voltage	V_{DD}		-0.3 ~ +7.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 ~ +7.0	V	
Input voltage	V_I		-0.3 ~ V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 ~ V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	2
Operating temperature	Topr		-40 ~ +85	°C	
Storage temperature	Tstg		-65 ~ +150	°C	
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–	

Note) 1 Case that to Nch open drain output by the mask option is included.
2 In case of plastic package.

● Recommended Operating Conditions

(V_{SS}=0V, Ta=-40 to 85°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V_{DD}		1.8		3.5	V	
Operating power voltage (High speed mode)	V_{DD}		3.5		5.5	V	
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		4.2	MHz	1
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 3.5V	30.000	32.768	80.000	kHz	1
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		8.2	MHz	1
Liquid crystal power voltage	V_{C5}	$V_{C5} \geq V_{C4} \geq V_{C3} \geq V_{C2} \geq V_{C1} \geq V_{SS}$			6.0	V	2
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	3
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	3
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	3, 4
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	3
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	3
Capacitor between CA and CB	C_7			0.1		µF	3
Capacitor between CA and CC	C_8			0.1		µF	3
Capacitor between CD and CE	C_9			0.1		µF	3, 4
Capacitor between CF and CG	C_{10}			0.1		µF	3

Note) 1 When an external clock is input from the OSC1 terminal by the mask option, leave the OSC2 terminal open, and when an external clock is input from the OSC3 terminal, leave the OSC4 terminal open.
2 When external power supply is selected by the mask option.
3 When LCD drive power is not used, the capacitor is not necessary. In this case, leave the V_{C1} to V_{C5} and CA to CG terminals open.
4 When a 1/4-bias LCD drive power supply is used, the capacitors C_4 and C_9 are not necessary.

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx	0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Kxx, Pxx	0		0.2V_{DD}	V	
High level input voltage (2) (Normal mode)	V_{IH2}	OSC1	1.6		V_{DD}	V	1
High level input voltage (2) (Low power mode)	V_{IH2}	OSC1	1.0		V_{DD}	V	1
High level input voltage (2) (High speed mode)	V_{IH2}	OSC1	2.4		V_{DD}	V	1
Low level input voltage (2) (Normal mode)	V_{IL2}	OSC1	0		0.6	V	1
Low level input voltage (2) (Low power mode)	V_{IL2}	OSC1	0		0.3	V	1
Low level input voltage (2) (High speed mode)	V_{IL2}	OSC1	0		0.9	V	1
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$	100	300	500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx, V_{IN} = 0V, f = 1MHz, Ta = 25°C		7	15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1V	5			µA	

Note) 1 When external clock is selected by mask option.
2 When pull-up resistor is added by mask option.

● SVD Circuit

(Unless otherwise specified: V_{DD}=1.8~5.5V, V_{SS}=0V, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.82	Typ×1.08	V	1
		Level 2 → Level 1		2.00		V	1
		Level 3 → Level 2		2.18		V	1
		Level 4 → Level 3		2.36		V	2
		Level 5 → Level 4		2.54		V	2
		Level 6 → Level 5		2.72		V	2
		Level 7 → Level 6		2.90		V	3
		Level 8 → Level 7		3.08		V	3
		Level 9 → Level 8		3.26		V	3
		Level 10 → Level 9	Typ×0.88	3.45	Typ×1.12	V	4
		Level 11 → Level 10		3.65		V	4
		Level 12 → Level 11		3.85		V	4
		Level 13 → Level 12		4.05		V	4
		Level 14 → Level 13		4.25		V	4
		Level 15 → Level 14		4.50		V	4

$V_{SVD\ (Level\ 0)} < V_{SVD\ (Level\ 1)} < V_{SVD\ (Level\ 2)} < V_{SVD\ (Level\ 3)} < V_{SVD\ (Level\ 4)} < V_{SVD\ (Level\ 5)} < V_{SVD\ (Level\ 6)} < V_{SVD\ (Level\ 7)}$
$< V_{SVD\ (Level\ 8)} < V_{SVD\ (Level\ 9)} < V_{SVD\ (Level\ 10)} < V_{SVD\ (Level\ 11)} < V_{SVD\ (Level\ 12)} < V_{SVD\ (Level\ 13)} < V_{SVD\ (Level\ 14)} < V_{SVD\ (Level\ 15)}$

Note) 1 Low power operating mode only
2 Low power operating mode or Normal operating mode only
3 Normal operating mode only
4 Normal operating mode or High speed operating mode only

● Current Consumption

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=25°C, OSC1=32.768kHz crystal oscillation, C_G=25pF, OSC3=Crystal/ceramic oscillation, Non heavy load protection mode, C_1 to C_{10}=0.1µF, No panel load)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status *1		0.3	1	µA	
	I_{DD2}	In HALT status *2		1.5	4	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		9	15	µA	
	I_{DD4}	CPU is in operating (4MHz) *4		1.1	1.5	mA	
Power current (Low power mode)	I_{DD1}	In SLEEP status *1		0.2	1	µA	
	I_{DD2}	In HALT status *2		1	3	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		5	8	µA	
Power current (High speed mode)	I_{DD1}	In SLEEP status *1		1	3	µA	
	I_{DD2}	In HALT status *2		2	6	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		13	22	µA	
	I_{DD4}	CPU is in operating (8MHz) *5		3.7	4.9	mA	
LCD drive circuit current	I_{LCDN}			2.5	5	µA	1
	I_{LCDH}	In heavy load protection mode		23	30	µA	2
SVD circuit current	I_{SVDN}	V_{DD} = 3.0V		30	60	µA	3
OSC1 CR oscillation current	I_{CR1}	R_{CR1} = 800kΩ		3	20	µA	4

*1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
*2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
*3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768 kHz, Clock timer: Operating, Others: Stop status
*4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 4 MHz, Clock timer: Operating, Others: Stop status
*5 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 8 MHz, Clock timer: Operating, Others: Stop status

Note) 1 The LCD drive circuit current varies according to the display patterns.
2 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).
3 The value in ***x*** V can be found by the following expression: I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 20) - 30 (Typ. value), I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 30) - 30 (Max. value)
4 When OSC1 CR oscillation circuit is selected by the mask option.

● LCD Driver

The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number). Therefore, these should be evaluated by connecting to the actual panel to be used.

TYPE A

(Unless otherwise specified: V_{DD}=V_{C2} (LCX=FH)+0.1 to 5.5V, V_{SS}=0V, Ta=25°C, C_1 to C_{10}=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C2}	When 1MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)			0.412V_{C5}		V	
	V_{C5} TYPE A	When 1MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		3.61		V	1
			LCX = 1H		3.76		V	
			LCX = 2H		3.88		V	
			LCX = 3H		4.00		V	
			LCX = 4H		4.12		V	
			LCX = 5H		4.27		V	
			LCX = 6H	Typ×0.94	4.39	Typ×1.06	V	
			LCX = 7H		4.51		V	
			LCX = 8H		4.63		V	
			LCX = 9H		4.75		V	
			LCX = AH		4.90		V	
			LCX = BH		5.02		V	
			LCX = CH		5.14		V	
			LCX = DH		5.26		V	
			LCX = EH		5.38		V	
			LCX = FH		5.53		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

TYPE B

(Unless otherwise specified: V_{DD}=V_{C2} (LCX=FH)+0.1 to 5.5V, V_{SS}=0V, Ta=25°C, C_1 to C_{10}=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C2}	When 1MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)			0.412V_{C5}		V	
	V_{C5} TYPE B	When 1MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		4.20		V	1
			LCX = 1H		4.34		V	
			LCX = 2H		4.49		V	
			LCX = 3H		4.63		V	
			LCX = 4H		4.78		V	
			LCX = 5H		4.92		V	
			LCX = 6H	Typ×0.94	5.07	Typ×1.06	V	
			LCX = 7H		5.21		V	
			LCX = 8H		5.36		V	
			LCX = 9H		5.50		V	
			LCX = AH		5.65		V	
			LCX = BH		5.80		V	
			LCX = CH		5.94		V	
			LCX = DH		6.09		V	
			LCX = EH		6.23		V	
			LCX = FH		6.38		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

TYPE C

(Unless otherwise specified: V_{DD}=V_{C2} (LCX=FH)+0.1 to 5.5V, V_{SS}=0V, Ta=25°C, C_1 to C_3/C_5 to C_8/C_{10}=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C2}	When 1MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)			0.505V_{C5}		V	
	V_{C5} TYPE C	When 1MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		3.43		V	1
			LCX = 1H		3.54		V	
			LCX = 2H		3.66		V	
			LCX = 3H		3.78		V	
			LCX = 4H		3.90		V	
			LCX = 5H		4.02		V	
			LCX = 6H	Typ×0.94	4.14	Typ×1.06	V	
			LCX = 7H		4.26		V	
			LCX = 8H		4.38		V	
			LCX = 9H		4.49		V	
			LCX = AH		4.61		V	
			LCX = BH		4.73		V	
			LCX = CH		4.85		V	
			LCX = DH		4.97		V	
			LCX = EH		5.09		V	
			LCX = FH		5.21		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

TYPE D

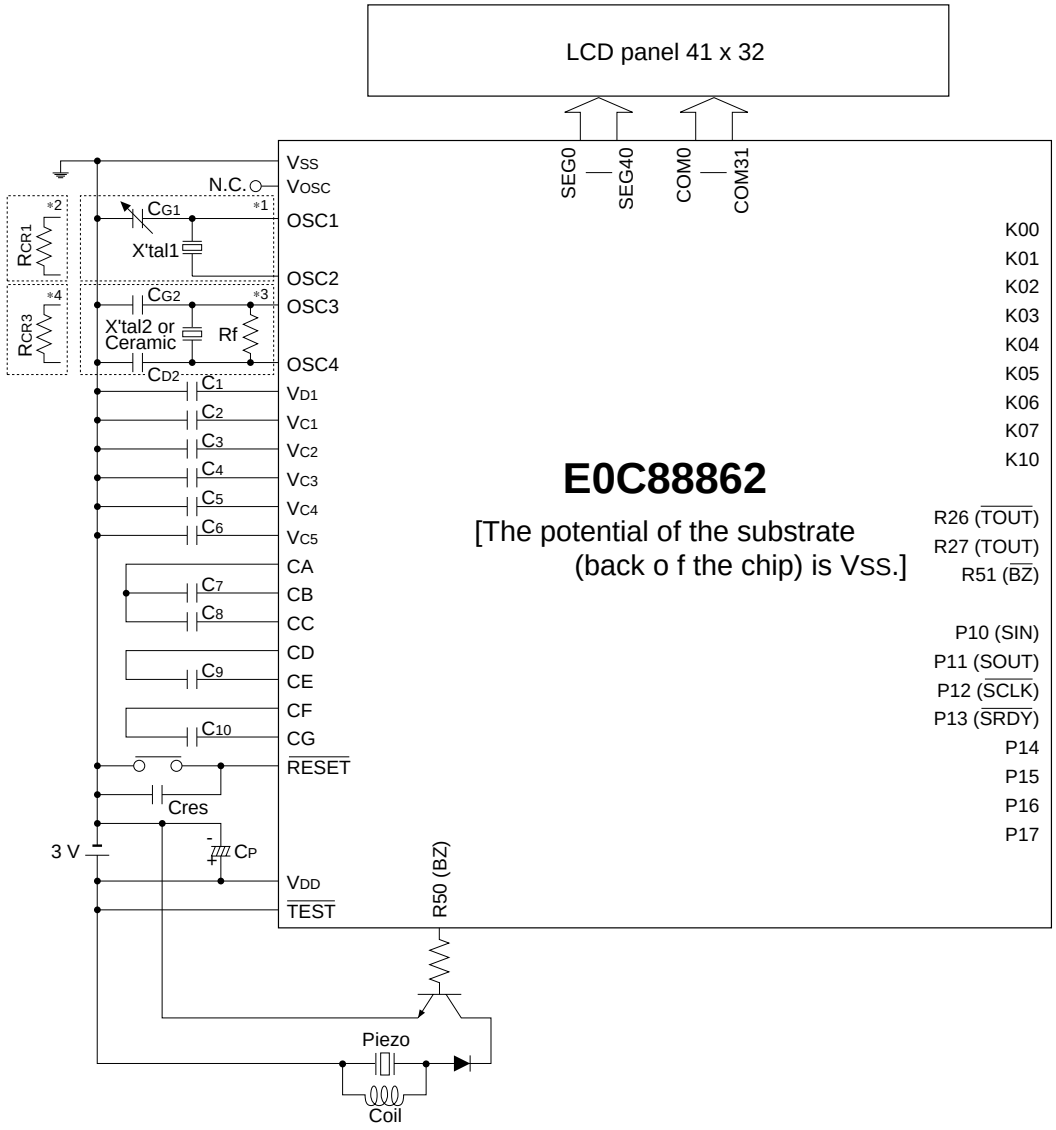
(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C, C_1 to C_3/C_5 to C_8/C_{10}=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	When 1MΩ load resistor is connected between V_{SS} and V_{C1} (no panel load)			0.260V_{C5}		V	
	V_{C5} TYPE D	When 1MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		3.80		V	1
			LCX = 1H		3.88		V	
			LCX = 2H		3.96		V	
			LCX = 3H		4.03		V	
			LCX = 4H		4.15		V	
			LCX = 5H		4.22		V	
			LCX = 6H	Typ×0.94	4.30	Typ×1.06	V	
			LCX = 7H		4.38		V	
			LCX = 8H		4.45		V	
			LCX = 9H		4.53		V	
			LCX = AH		4.65		V	
			LCX = BH		4.72		V	
			LCX = CH		4.80		V	
			LCX = DH		4.88		V	
			LCX = EH		4.95		V	
			LCX = FH		5.07		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

■ BASIC EXTERNAL CONNECTION DIAGRAM

● **When piezoelectric buzzer is driven with single terminal and LCD panel is driven with 1/5 bias power supply**



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, Cl (Max.)=35 kΩ
C_{G1}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for CR oscillation	800 kΩ
X'tal2	Crystal oscillator	4.9152 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal osciilation)
		30 pF (Ceramic osciilation)
C_{D2}	Drain capacitor	15 pF (Crystal osciilation)
		30 pF (Ceramic osciilation)

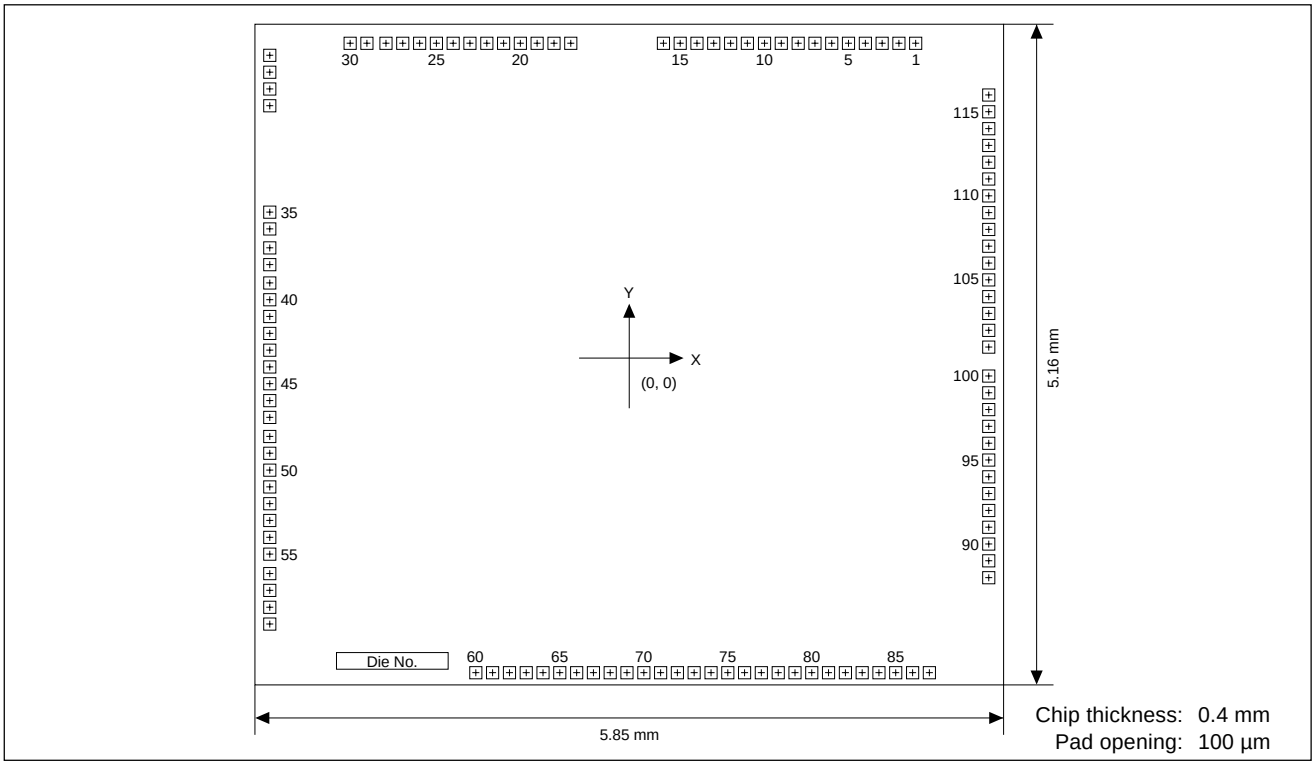
Symbol	Name	Recommended value
R_{CR3}	Resistor for CR oscillation	20 kΩ
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_{10}	Booster/reducer capacitors	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{\text{RESET}}$ terminal	0.47 µF

∗ The connection diagram shown above is an example of when mask option settings are as follows:
LCD power source: Internal power supply (1/5 bias), $\overline{\text{RESET}}$ terminal: With pull-up resistor,
R51 specification: General-purpose output port

∗1 OSC1 = Crystal oscillation, ∗2 OSC1 = CR oscillation, ∗3 OSC3 = Crystal/Ceramic oscillation, ∗4 OSC3 = CR oscillation

Note: The above table is simply an example, and is not guaranteed to work.

■ DIAGRAM OF PAD LAYOUT

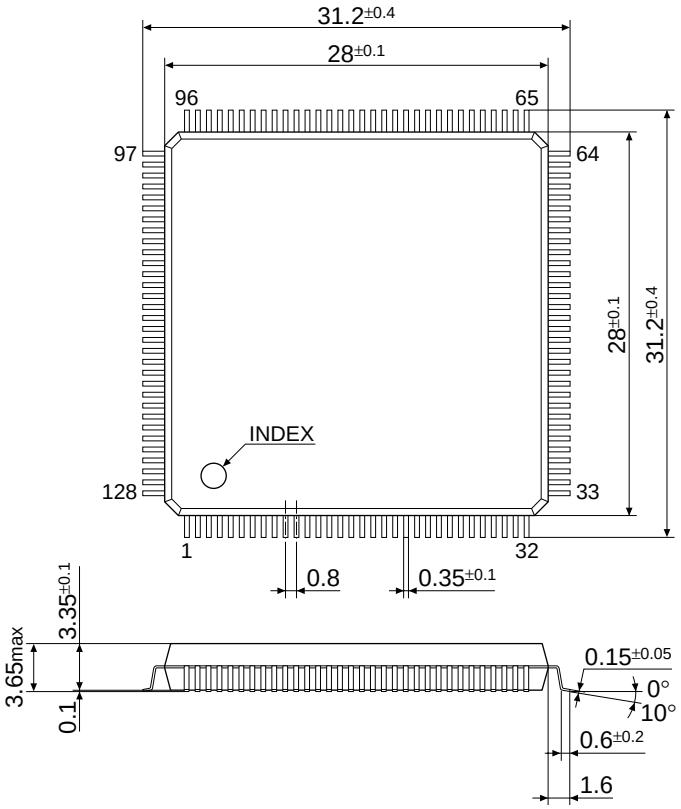


■ PAD COORDINATES

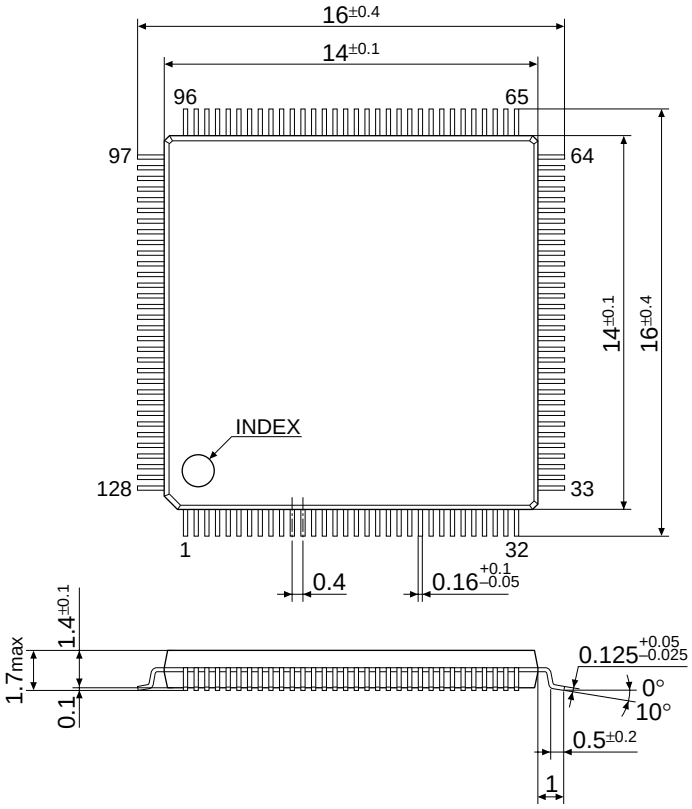
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	COM15	2238	2458	31	V_{OSC}	-2809	2364	60	SEG0	-1199	-2458	88	SEG28	2809	-1716
2	COM14	2107	2458	32	V_{D1}	-2809	2232	61	SEG1	-1068	-2458	89	SEG29	2809	-1584
3	COM13	1976	2458	33	V_{DD}	-2809	2101	62	SEG2	-936	-2458	90	SEG30	2809	-1453
4	COM12	1845	2458	34	V_{SS}	-2809	1970	63	SEG3	-805	-2458	91	SEG31	2809	-1322
5	COM11	1713	2458	35	OSC1	-2809	1139	64	SEG4	-674	-2458	92	SEG32	2809	-1191
6	COM10	1582	2458	36	OSC2	-2809	1008	65	SEG5	-543	-2458	93	SEG33	2809	-1059
7	COM9	1451	2458	37	$\overline{TEST}$	-2809	860	66	SEG6	-411	-2458	94	SEG34	2809	-928
8	COM8	1320	2458	38	$\overline{RESET}$	-2809	729	67	SEG7	-280	-2458	95	SEG35	2809	-797
9	COM7	1188	2458	39	K10/EVIN	-2809	586	68	SEG8	-149	-2458	96	SEG36	2809	-666
10	COM6	1057	2458	40	K07	-2809	455	69	SEG9	-18	-2458	97	SEG37	2809	-534
11	COM5	923	2458	41	K06	-2809	324	70	SEG10	114	-2458	98	SEG38	2809	-403
12	COM4	792	2458	42	K05	-2809	192	71	SEG11	245	-2458	99	SEG39	2809	-272
13	COM3	660	2458	43	K04	-2809	61	72	SEG12	376	-2458	100	SEG40	2809	-141
14	COM2	529	2458	44	K03	-2809	-70	73	SEG13	507	-2458	101	COM31/SEG51	2809	85
15	COM1	398	2458	45	K02	-2809	-201	74	SEG14	639	-2458	102	COM30/SEG52	2809	216
16	COM0	267	2458	46	K01	-2809	-333	75	SEG15	770	-2458	103	COM29/SEG53	2809	348
17	CG	-457	2458	47	K00	-2809	-464	76	SEG16	901	-2458	104	COM28/SEG54	2809	479
18	CF	-588	2458	48	P17	-2809	-613	77	SEG17	1032	-2458	105	COM27/SEG55	2809	610
19	CE	-720	2458	49	P16	-2809	-744	78	SEG18	1164	-2458	106	COM26/SEG56	2809	741
20	CD	-851	2458	50	P15	-2809	-876	79	SEG19	1295	-2458	107	COM25/SEG57	2809	873
21	CC	-982	2458	51	P14	-2809	-1007	80	SEG20	1426	-2458	108	COM24/SEG58	2809	1004
22	CB	-1113	2458	52	P13/$\overline{SRDY}$	-2809	-1138	81	SEG21	1557	-2458	109	COM23/SEG59	2809	1135
23	CA	-1245	2458	53	P12/$\overline{SCLK}$	-2809	-1269	82	SEG22	1689	-2458	110	COM22/SEG60	2809	1266
24	V_{C5}	-1376	2458	54	P11/SOUT	-2809	-1401	83	SEG23	1820	-2458	111	COM21/SEG61	2809	1398
25	V_{C4}	-1507	2458	55	P10/SIN	-2809	-1532	84	SEG24	1951	-2458	112	COM20/SEG62	2809	1529
26	V_{C3}	-1638	2458	56	R26/$\overline{TOUT}$	-2809	-1684	85	SEG25	2082	-2458	113	COM19/SEG63	2809	1660
27	V_{C2}	-1770	2458	57	R27/TOUT	-2809	-1815	86	SEG26	2214	-2458	114	COM18/SEG64	2809	1791
28	V_{C1}	-1901	2458	58	R50/BZ	-2809	-1947	87	SEG27	2345	-2458	115	COM17/SEG65	2809	1923
29	OSC3	-2050	2458	59	R51/$\overline{BZ}$	-2809	-2078	–				116	COM16/SEG66	2809	2054
30	OSC4	-2181	2458	–				–				–			

■ PACKAGE DIMENSIONS

Plastic QFP8-128pin

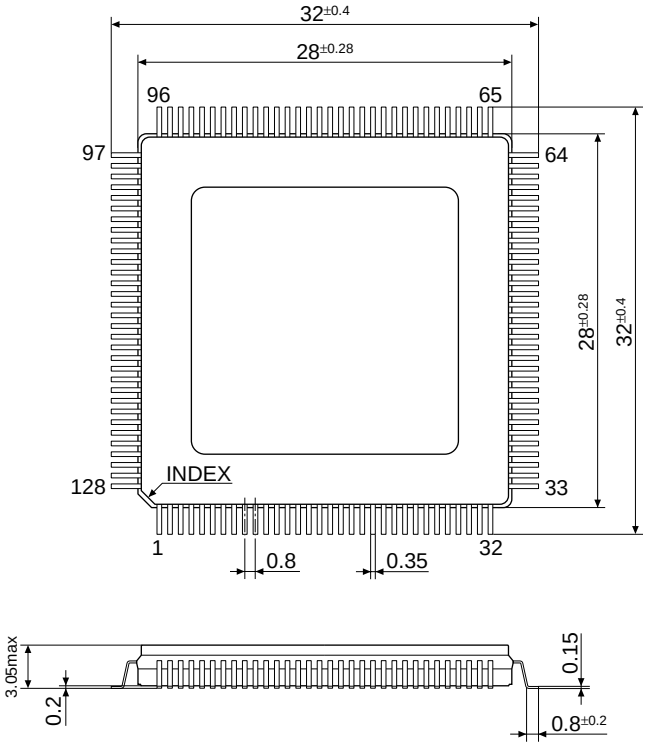


Plastic QFP15-128pin



Unit: mm

Ceramic QFP8-128pin



Unit: mm

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