MF1056-01

EPSON

E0C88348 DEVELOPMENT HARDWARE TOOL

E0C88P348 TECHNICAL MANUAL

E0C88P348 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

PREFACE

This manual describes the hardware specification of the E0C88P348.
The E0C88P348 is a development tool for the E0C88348. The mask ROM in the E0C88348 has been changed to a Flash EEPROM. Almost all other circuits are compatible with the E0C88348, therefore this manual explains only the parts related to the PROM and other differences from the E0C88348. Furthermore, an exclusive PROM writer (UNIVERSAL ROM WRITER II) should be used for PROM programming.

Refer to the following manuals in addition to this manual.

For the functions and control of the peripheral circuit:	"E0C88348 Technical Manual"
For the exclusive PROM writer and programming:	"Universal ROM Writer II Hardware Manual"
	"E0C88PxxxUniversal ROM Writer II User's Manual"
	"E0C88P348 Adapter Socket Hardware Manual"

CONTENTS

CHAPTER 1 OUTLINE

The E0C88P348 is a 8-bit microcomputer, with a built-in Flash EEPROM (PROM), for evaluating the functions of the E0C88348.
The E0C88P348 has almost the same functions as the E0C88348. The mask ROM in the E0C88348 has been changed to a Flash EEPROM that allows the user to rewrite programs using the exclusive PROM writer. The E0C88P348 also supports On Board Programming (the data can be rewritten to the PROM if the IC is mounted on the board). The program can be rewritten up to 10 times under the development stage, it will increase the efficiency of device-level function evaluation.

Note: • Refer to Chapter 4, "Summary of Notes", before rewriting the PROM.

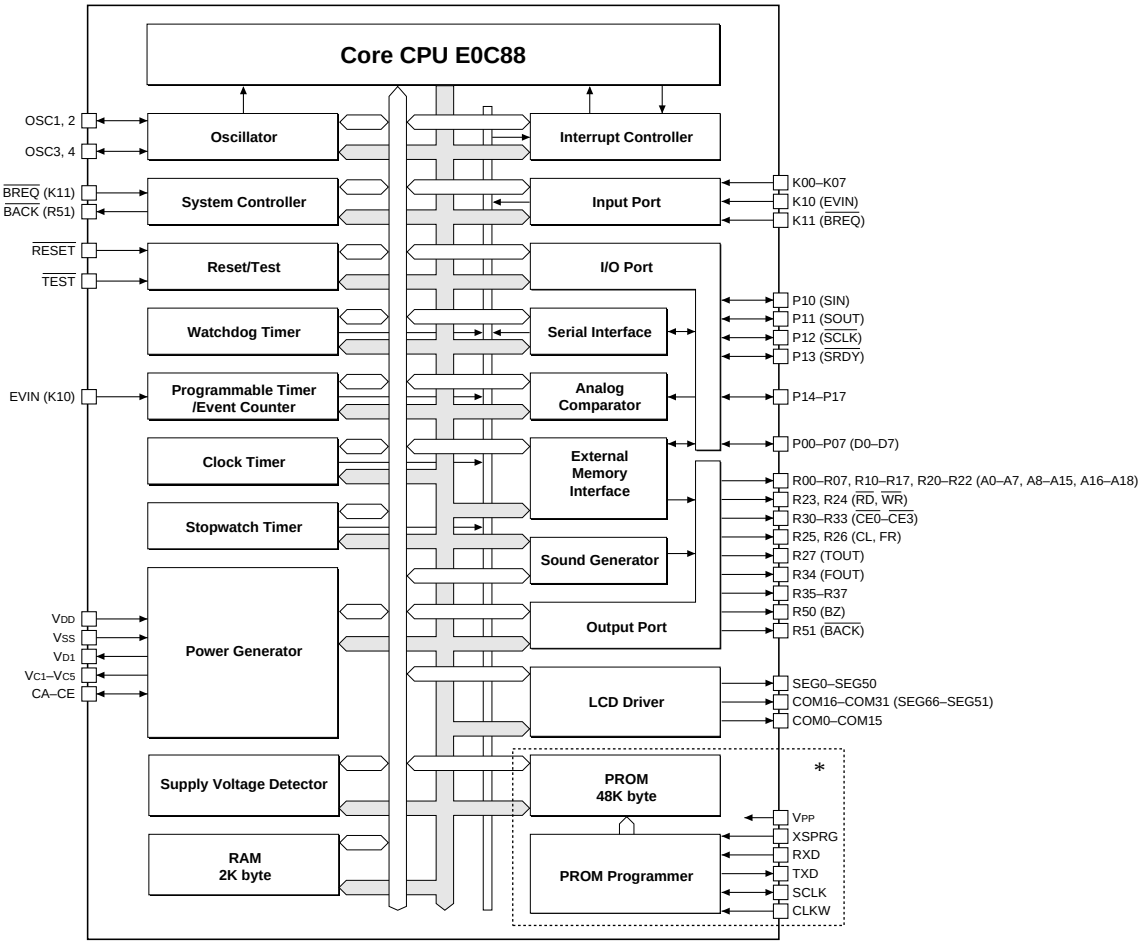
• The E0C88P348 is a program development tool for evaluating the functions, therefore do not use it for mass production.

1.1 Features

Core CPU	E0C88 (MODEL3) CMOS 8-bit core CPU
OSC1 oscillation circuit	32.768 kHz (Typ.) crystal oscillation circuit ∗
OSC3 oscillation circuit	6 MHz (Max.) crystal/ceramic oscillation circuit ∗
Instruction set	608 types (usable for multiplication and division instructions)
Instruction execution time	0.33 µsec/6 MHz (for 2-clock instructions) ∗
PROM (Flash EEPROM) ∗	48K bytes Dual power: V_{DD} = 5 V, V_{PP} = 12.5 V for writing/erase
PROM programmer	Serial programming and parallel programming are available ∗
RAM	2K bytes
Bus line	Address bus: 19 bits (shared with output ports) Data bus: 8 bits (shared with I/O ports) $\overline{CE}$ signal: 4 bits (shared with output ports) $\overline{WR}$ signal: 1 bit (shared with output port) $\overline{RD}$ signal: 1 bit (shared with output port)
Input port	10 bits (pull-up resistors built-in) ∗
Output port	9 bits (usable for buzzer, LCD control, FOUT, TOUT and $\overline{BACK}$ signal outputs)
I/O port	8 bits (usable for serial I/O)
Serial interface	1 ch. (8-bit clock synchronous or asynchronous system)
Timer	Programmable timer (8-bit): 2 ch. (usable as a 1-ch. 16-bit timer) Clock timer (8-bit): 1 ch. Stopwatch timer (8-bit): 1 ch.
LCD driver	51 segments × 32 commons, 67 segments × 16 or 8 commons LCD power supply circuit built-in (boostor type, 5 potentials)
Sound generator	Envelope and volume control functions built-in
Watchdog timer	Built-in
Supply voltage detection (SVD) circuit	8 values, programmable ∗
External interrupt	Input port interrupt: 2 systems (3 types)
Internal interrupt	Timer interrupt: 3 systems (9 types) Serial interface interrupt: 1 system (3 types)
Power supply voltage	3.3 V to 5.5 V ∗
Package	QFP8-160pin (plastic) or chip

∗: Items that differ from the E0C88348

1.2 Block Diagram

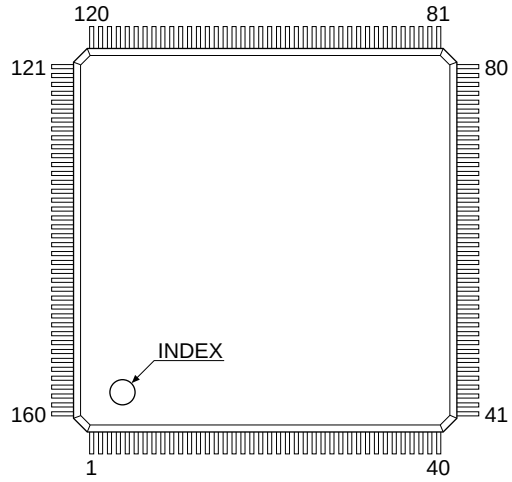


∗ The PROM block indicated with a dotted line differ from the E0C88348.

Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP8-160pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG18	41	COM24/SEG58	81	OSC1	121	R11/A9
2	SEG19	42	COM23/SEG59	82	OSC2	122	R12/A10
3	SEG20	43	COM22/SEG60	83	$\overline{\text{TEST}}$	123	R13/A11
4	SEG21	44	COM21/SEG61	84	$\overline{\text{RESET}}$	124	R14/A12
5	SEG22	45	COM20/SEG62	85	V_{PP} *	125	R15/A13
6	SEG23	46	COM19/SEG63	86	K11/$\overline{\text{BREQ}}$	126	R16/A14
7	SEG24	47	COM18/SEG64	87	K10/EVIN	127	R17/A15
8	SEG25	48	COM17/SEG65	88	K07	128	R20/A16
9	SEG26	49	COM16/SEG66	89	K06	129	R21/A17
10	SEG27	50	COM15	90	K05	130	R22/A18
11	SEG28	51	COM14	91	K04	131	R23/$\overline{\text{RD}}$
12	SEG29	52	COM13	92	K03	132	R24/$\overline{\text{WR}}$
13	SEG30	53	COM12	93	K02	133	R25/CL
14	SEG31	54	COM11	94	K01	134	R26/FR
15	SEG32	55	COM10	95	K00	135	R27/TOUT
16	SEG33	56	COM9	96	P17	136	R30/$\overline{\text{CE0}}$
17	SEG34	57	COM8	97	P16	137	R31/$\overline{\text{CE1}}$
18	SEG35	58	COM7	98	P15	138	R32/$\overline{\text{CE2}}$
19	SEG36	59	COM6	99	P14	139	R33/$\overline{\text{CE3}}$
20	SEG37	60	COM5	100	P13/$\overline{\text{SRDY}}$	140	R34/FOUT
21	SEG38	61	COM4	101	P12/$\overline{\text{SCLK}}$	141	R50/BZ
22	SEG39	62	COM3	102	P11/SOUT	142	R51/$\overline{\text{BACK}}$
23	SEG40	63	COM2	103	P10/SIN	143	SEG0
24	SEG41	64	COM1	104	P07/D7	144	SEG1
25	SEG42	65	COM0	105	P06/D6	145	SEG2
26	SEG43	66	CE	106	P05/D5	146	SEG3
27	SEG44	67	CD	107	P04/D4	147	SEG4
28	SEG45	68	CC	108	P03/D3	148	SEG5
29	SEG46	69	CB	109	P02/D2	149	SEG6
30	SEG47	70	CA	110	P01/D1	150	SEG7
31	SEG48	71	V_{C5}	111	P00/D0	151	SEG8
32	SEG49	72	V_{C4}	112	R00/A0	152	SEG9
33	SEG50	73	V_{C3}	113	R01/A1	153	SEG10
34	COM31/SEG51	74	V_{C2}	114	R02/A2	154	SEG11
35	COM30/SEG52	75	V_{C1}	115	R03/A3	155	SEG12
36	COM29/SEG53	76	OSC3	116	R04/A4	156	SEG13
37	COM28/SEG54	77	OSC4	117	R05/A5	157	SEG14
38	COM27/SEG55	78	V_{D1}	118	R06/A6	158	SEG15
39	COM26/SEG56	79	V_{DD}	119	R07/A7	159	SEG16
40	COM25/SEG57	80	V_{SS}	120	R10/A8	160	SEG17

∗ : Terminal changed in the E0C88P348.

Fig. 1.3.1 Pin layout diagram (QFP8-160pin)

1.4 Pin Description

Table 1.4.1 Pin description (QFP8-160pin)

Pin name	Pin No.	In/out	Function
V_{DD}	79	–	Power supply (+) terminal
V_{SS}	80	–	Power supply (GND) terminal
V_{D1}	78	–	Regulated voltage output terminal for oscillators
V_{C1}–V_{C5}	75–71	O	LCD drive voltage output terminals
CA–CE	70–66	–	Booster capacitor connection terminals for LCD
OSC1	81	I	OSC1 oscillation input terminal (crystal oscillation)
OSC2	82	O	OSC1 oscillation output terminal
OSC3	76	I	OSC3 oscillation input terminal (crystaloscillation/ceramic oscillation)
OSC4	77	O	OSC3 oscillation output terminal
K00–K07	95–88	I	Input terminals (K00–K07)
K10/EVIN	87	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
K11/$\overline{BREQ}$	86	I	Input terminal (K11) or bus request signal input terminal ($\overline{BREQ}$)
R00–R07/A0–A7	112–119	O	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	120–127	O	Output terminals (R10–R17) or address bus (A8–A15)
R20–R22/A16–A18	128–130	O	Output terminals (R20–R22) or address bus (A16–A18)
R23/$\overline{RD}$	131	O	Output terminal (R23) or read signal output terminal ($\overline{RD}$)
R24/$\overline{WR}$	132	O	Output terminal (R24) or write signal output terminal ($\overline{WR}$)
R25/CL	133	O	Output terminal (R25) or LCD synchronous signal output terminal (CL)
R26/FR	134	O	Output terminal (R26) or LCD frame signal output terminal (FR)
R27/TOUT	135	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R30–R33/$\overline{CE0}$–$\overline{CE3}$	136–139	O	Output terminals (R30–R33) or chip enable output terminals ($\overline{CE0}$–$\overline{CE3}$)
R34/FOUT	140	O	Output terminal (R34) or clock output terminal (FOUT)
R35–R37 *2	(only for chip)	O	Output terminals (R35–R37)
R50/BZ	141	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{BACK}$	142	O	Output terminal (R51) or bus acknowledge signal output terminal ($\overline{BACK}$)
P00–P07/D0–D7	111–104	I/O	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN	103	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	102	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{SCLK}$	101	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{SCLK}$)
P13/$\overline{SRDY}$	100	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{SRDY}$)
P14 *5	99	I/O	I/O terminal (P14)
P15 *5	98	I/O	I/O terminal (P15)
P16 *5	97	I/O	I/O terminal (P16)
P17 *5	96	I/O	I/O terminal (P17)
COM0–COM15	65–50	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	49–34	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 or 1/8 duty is selected)
SEG0–SEG50	143–160, 1–33	O	LCD segment output terminals
$\overline{RESET}$	84	I	Initial reset input terminal
$\overline{TEST}$ *1	83	I	Test input terminal
V_{PP} *3	85	–	PROM programming power supply (fix at +5 V in normal/high-speed mode)
XSPRG *2 *4	(only for chip)	I	PROM serial programming mode setting (fix at High in normal/high-speed mode)
RXD *2 *4	(only for chip)	I	PROM serial programming data input (fix at High in normal/high-speed mode)
TXD *2 *4	(only for chip)	O	PROM serial programming data output (unused in normal/high-speed mode)
SCLK *2 *4	(only for chip)	I/O	PROM serial programming clock I/O (fix at High in normal/high-speed mode)
CLKW *2 *4	(only for chip)	I	PROM serial programming source clock input (fix at High in normal/high-speed mode)

*1: $\overline{TEST}$ is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V_{DD}.
*2: These terminals can be used only when the E0C88P348 is shipped with a chip form.
*3: This terminal is changed in the E0C88P348.
*4: These terminals are added in the E0C88P348.
*5: Functions are limited in the E0C88P348.

See Section 3.1, "Terminal Configuration", for the terminal functions during the programming mode.

CHAPTER 2 PROM PROGRAMMER AND OPERATING MODES

The biggest difference between the E0C88348 and the E0C88P348 is that the E0C88P348 contains Flash EEPROM as the ROM that allows the user to write data to it using the exclusive ROM writer (UNIVERSAL ROM WRITER II). The E0C88P348 also has a built-in PROM programmer that controls writing data to the PROM.
This chapter explains the PROM programmer and the operating modes that are added for the programming operation.

2.1 Configuration of PROM Programmer

Figure 2.1.1 shows the configuration of the PROM programmer.

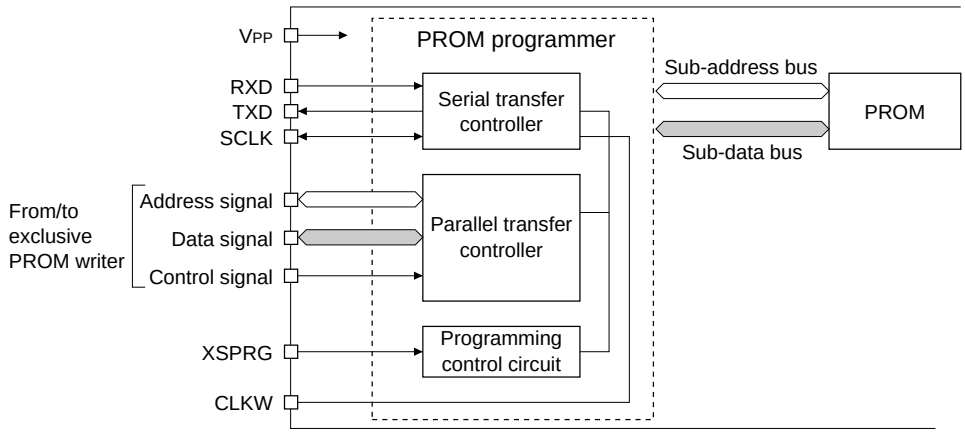


Fig. 2.1.1 Configuration of PROM programmer

The PROM programmer supports Serial Programming for writing data received in serial transfer and Parallel Programming that uses a parallel transfer. The programming method will be described later.

Terminals

The PROM programmer uses the following input/output terminals. The following sections will explain handling the terminals in each operating mode.

VPP: Power supply terminal for PROM programming

XSPRG: PROM serial programming mode setting terminal

RXD: Serial data receive terminal

TXD: Serial data transmit terminal

SCLK: Serial clock input/output terminal

CLKW: Serial programming source clock (3.072 MHz) input terminal

The parallel programming mode uses other terminals in addition to the terminals above. However, it is not necessary to switch the lines on the board, because the IC is programed by directly installing it to the exclusive PROM writer (UNIVERSAL ROM WRITER II).

2.2 Operating Modes

Three operating modes are available in the E0C88P348: one is for normal operation and the others are for programming.

1) Normal operation mode (Normal mode/High-speed mode)
2) PROM serial programming mode
3) PROM parallel programming mode

The operating mode is decided by the XSPRG terminal setting at power on or initial reset.

2.2.1 Normal operation mode

In this mode, the E0C88 core CPU and the peripheral circuits operate by the programmed PROM. The CPU can enter this mode after the PROM programming has finished.
The PROM bit data is set to "1" at shipment. Therefore, the IC will not work even if the normal operation mode is set before programming.

In the normal operation mode, set the terminals for the PROM programmer as below. The board must be designed so that the terminal settings cannot be changed.

VPP: Supply a voltage the same as VDD. In order to prevent damage to the IC, do not supply 12.5 V of programming voltage in the normal operation mode.

XSPRG: Fix at a High level.

RXD, SCLK, CLKW: Open or fix at a High level.

TXD: Open.

2.2.2 PROM serial programming mode

The PROM serial programming mode should be set when writing data to the PROM using a serial transfer from the exclusive PROM writer (UNIVERSAL ROM WRITER II). This mode will be used for the programming of chip products, because the programming can be done even when the IC has already been mounted on the board.
To create data to be written to the PROM, use the E0C88 assembler similar to the E0C88348.
The following explains the procedure of PROM serial programming.

PROM serial programming procedure

(1) Set the required terminals for serial programming as follows:

VPP: Connect to VPP on the PROM writer. The voltage (5 V/12.5 V) can be switched using the PROM writer.

Note: Be sure to set VPP to 5 V at the IC power on or initial reset. Note that the IC may be damaged if 12.5 V has been supplied to the VPP terminal at power on or initial reset.

XSPRG: Set the terminal so that it will be fixed to a Low level. (A switch should be provided on the target board to change the XSPRG terminal level between High and Low.)

Note: The XSPRG terminal must be fixed at a Low level in the programming mode and at a High level in the normal operation mode. Changing the voltage level may damage the IC.

RXD, TXD, SCLK: Connect to the PROM writer.

CLKW: Connect to the PROM writer. A 3.072 MHz clock will be supplied from the PROM writer at programming.

Other terminals should be set as below.
Input port terminals (K): Fix at a High or Low level.
I/O port terminals (P): Fix at a High or Low level.
$\overline{\text{TEST}}$ terminal: Fix at a High level.

(2) Turn the IC (user target board) power (+5 V) on.
A power voltage must be supplied to the VDD and VSS terminals same as the regular operation so that the OSC1 oscillation circuits operate normally.

(3) Turn the PROM writer on.

(4) Controls the $\overline{\text{RESET}}$ and XSPRG terminals as shown in Figure 2.2.2.1.

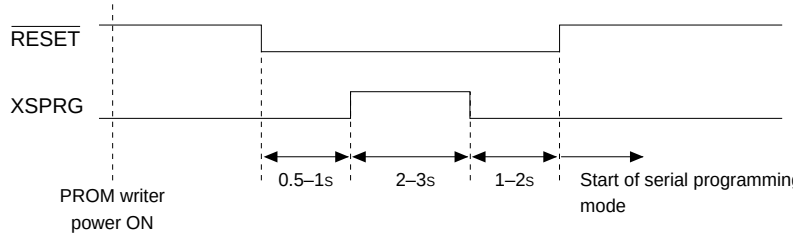


Fig. 2.2.2.1 Timing chart for entering serial programming mode

(5) Start up the romw88.exe in the personal computer, then load the 88p348.frm file. This allows serial programming to begin.

After setting this mode, data can be written to the exclusive PROM writer (UNIVERSAL ROM WRITER II). Refer to the "E0C88Pxxx Universal ROM Writer II User's Manual" for the connection and operation of the PROM writer.

2.2.3 PROM parallel programming mode

In the PROM parallel programming mode, the exclusive PROM writer (UNIVERSAL ROM WRITER II) transfers data in parallel to the IC installed on the PROM writer to write data to it. The terminal setting is done by the PROM writer. Thus there is no precaution on mode setting or board design.
Refer to the "E0C88Pxxx Universal ROM Writer II User's Manual" for the operation of the PROM writer.
To create data to be written to the PROM, use the E0C88 assembler the same as the E0C88348.

Note: The QFP8-160pin package supports the parallel programing mode only.

CHAPTER 3 DIFFERENCES FROM E0C88348

This chapter explains the differences on functions between the E0C88P348 and the E0C88348. The functions without description are the same in both models. Refer to the "E0C88348 Technical Manual" for the circuits and functions.

3.1 Terminal Configuration

The E0C88P348 has terminals for the PROM programmer in addition to the ones on the E0C88348. The other terminals are the same configuration as the E0C88348 (except for the VPP terminal).
Table 3.1.1 shows the pad configuration and the terminal functions according to the operating mode.

Table 3.1.1 Terminal configuration

Pin name	Pad No.	Normal operation mode		Serial programming mode	
		I/O	Function	I/O	Function
VDD	42	–	Power (+5V)	–	Power (+5V)
VSS	43	–	Power (GND)	–	Power (GND)
VD1	41	–	Regulated voltage output	–	Regulated voltage output
VC1–VC5	38–34	O	LCD drive voltage	O	Unused
CA–CE	33–29	–	Capacitor for LCD voltage	–	Unused
OSC1	44	I	OSC1 oscillation input	I	OSC1 oscillation input
OSC2	45	O	OSC1 oscillation output	O	OSC1 oscillation output
OSC3	39	I	OSC3 oscillation input	I	Unused
OSC4	40	O	OSC3 oscillation output	O	Unused
K00–K07	58–51	I	Input port	I	Unused (High or Low)
K10/EVIN	50	I	Input port or EVIN input	I	Unused (High or Low)
K11/$\overline{\text{BREQ}}$	49	I	Input port or $\overline{\text{BREQ}}$ input	I	Unused (High or Low)
R00–R07/A0–A7	75–82	O	Output port or address bus	O	Unused
R10–R17/A8–A15	83–90	O	Output port or address bus	O	Unused
R20–R22/A16–A18	91–93	O	Output port or address bus	O	Unused
R23/$\overline{\text{RD}}$	94	O	Output port or $\overline{\text{RD}}$ output	O	Unused
R24/$\overline{\text{WR}}$	95	O	Output port or $\overline{\text{WR}}$ output	O	Unused
R25/CL	96	O	Output port or CL output	O	Unused
R26/FR	97	O	Output port or FR output	O	Unused
R27/TOUT	98	O	Output port or TOUT output	O	Unused
R30–R33/$\overline{\text{CE0}}$–$\overline{\text{CE3}}$	99–102	O	Output port or $\overline{\text{CE}}$ output	O	Unused
R34/FOUT	103	O	Output port or FOUT output	O	Unused
R35–R37	104–106	O	Output port	O	Unused
R50/BZ	107	O	Output port or BZ output	O	Unused
R51/$\overline{\text{BACK}}$	108	O	Output port or $\overline{\text{BACK}}$ output	O	Unused
P00–P07/D0–D7	74–67	I/O	I/O port or data bus	I	Unused (High or Low)
P10/SIN	66	I/O	I/O port or SIN input	I	Unused (High or Low)
P11/SOUT	65	I/O	I/O port or SOUT output	I	Unused (High or Low)
P12/$\overline{\text{SCLK}}$	64	I/O	I/O port or $\overline{\text{SCLK}}$ terminal	I	Unused (High or Low)
P13/$\overline{\text{SRDY}}$	63	I/O	I/O port or $\overline{\text{SRDY}}$ output	I	Unused (High or Low)
P14 *1	62	I/O	I/O port	I	Unused (High or Low)
P15 *1	61	I/O	I/O port	I	Unused (High or Low)
P16 *1	60	I/O	I/O port	I	Unused (High or Low)
P17 *1	59	I/O	I/O port	I	Unused (High or Low)
COM0–COM15	28–24, 20–10	O	LCD COM output	O	Unused
COM16–COM31 /SEG66–SEG51	9–1, 169–163	O	LCD COM output or LCD SEG output	O	Unused
SEG0–SEG50	109–146, 150–162	O	LCD SEG output	O	Unused
$\overline{\text{RESET}}$	47	I	Initial reset	I	Initial reset
$\overline{\text{TEST}}$	46	I	Test port (High)	I	Unused (High)
VPP *2	48	–	PROM power (+5 V)	–	PROM program power (+5/12.5 V)
XSPRG *2	147	I	Unused (High)	I	PROM serial programming mode setting
RXD *2	21	I	Unused (High)	I	PROM serial programming data input
TXD *2	23	O	Unused	O	PROM serial programming data output
SCLK *2	22	I	Unused (High)	I/O	PROM serial programming clock I/O
CLKW *2	148	I	Unused (High)	I	PROM serial programming source clock input

*1: The functions of these terminals are limited in the E0C88P348. *2: These terminals differ from the E0C88348.

In the parallel programming mode, all the terminals are set to the appropriate status by the exclusive PROM writer.

3.2 Mask Option

The E0C88P348 cannot specify the E0C88348 mask options individually.
The following option combination is provided for the E0C88P348:

Table 3.2.1 Combination of mask options

Mask option		Setting
OSC1 oscillation circuit		Crystal oscillation (32.768 kHz)
OSC3 oscillation circuit		Crystal/ceramic oscillation
Multiple key entry reset combination		Not use
SVD reset		Not use
Input port pull up resistor	K00	With resistor
	K01	With resistor
	K02	With resistor
	K03	With resistor
	K04	With resistor
	K05	With resistor
	K06	With resistor
	K07	With resistor
	K10	With resistor
	K11	With resistor
	$\overline{\text{RESET}}$	With resistor
I/O port pull up resistor	P00	With resistor
	P01	With resistor
	P02	With resistor
	P03	With resistor
	P04	With resistor
	P05	With resistor
	P06	With resistor
	P07	With resistor
	P10	With resistor
	P11	With resistor
	P12	With resistor
	P13	With resistor
	P14	With resistor
	P15	With resistor
	P16	With resistor
	P17	With resistor
Output port specification	R00	Complementary
	R01	Complementary
	R02	Complementary
	R03	Complementary
	R04	Complementary
	R05	Complementary
	R06	Complementary
	R07	Complementary
	R10	Complementary
	R11	Complementary
	R12	Complementary
	R13	Complementary
	R14	Complementary
	R15	Complementary
	R16	Complementary
	R17	Complementary
LCD drive duty		1/32 & 1/16 duty
LCD power supply		Internal TYPE B (5.5 V)

3.3 Power Supply

Supply voltage (V_{DD})

The operable voltage range is different.

E0C88348:	Normal mode	2.4 V to 5.5 V
	Low-power mode	1.8 V to 3.5 V
	High-speed mode	3.5 V to 5.5 V
E0C88P348:	Normal mode	3.3 V to 5.5 V
	High-speed mode	4.5 V to 5.5 V

The E0C88P348 operation is guaranteed within the above voltage range. The operating mode should be set in the normal mode or the high-speed mode.

Supply voltage for PROM (V_{PP})

The power supply terminal for PROM is added in the E0C88P348.

V_{PP}:	PROM programming voltage	in normal operation mode:	V_{DD}
		in programming mode:	12.5 V

Power supply for oscillation circuit (V_{D1})

The V_{D1} voltage value can only be set to 2.2 V (normal mode) or 3.3 V (high-speed mode) in the E0C88P348 because the operating voltage range is limited.

Note: In the E0C88348, the internal circuits operate with the oscillation system regulated voltage (V_{D1}). On the other hand, the E0C88P348 internal circuits operate with the supply voltage (V_{DD}). Therefore, the operating frequency range of the E0C88P348 differs from that of the E0C88348. Refer to Chapter 6, "Electrical Characteristics", for details.

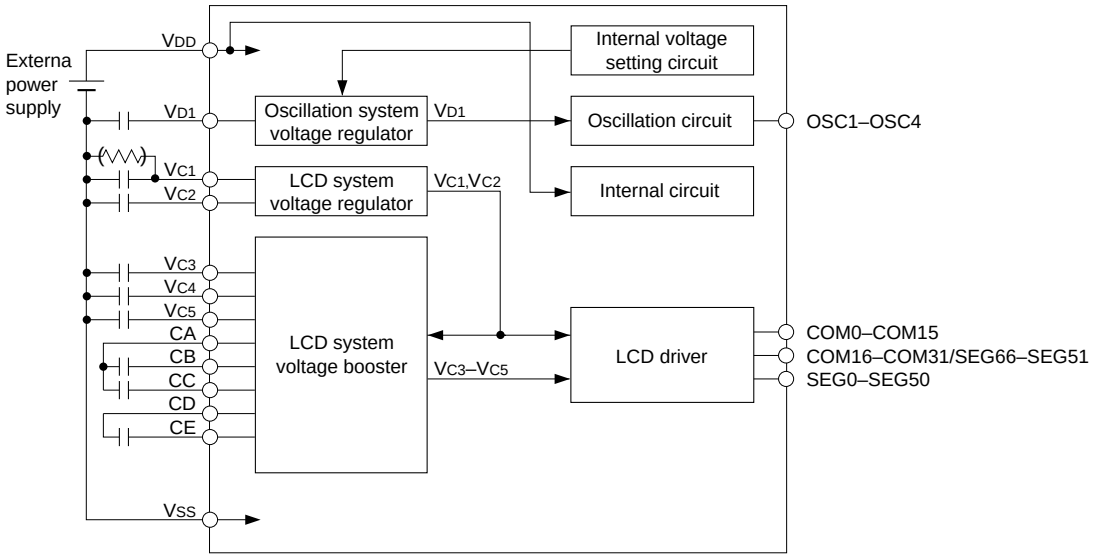


Fig. 3.3.1 Configuration of power supply circuit

LCD drive voltage (V_{C1}–V_{C5})

The range of the LCD drive voltage is different from that of the E0C88348.

Table 3.3.1 Range of LCD drive voltage

LCD drive voltage	Condition		E0C88348		E0C88P348	
			Min.	Max.	Min.	Max.
V_{C1}	∗1		0.18V_{C5}	0.22V_{C5}	0.18V_{C5}	0.22V_{C5}
V_{C2}	∗2		0.39V_{C5}	0.48V_{C5}	0.38V_{C5}	0.46V_{C5}
V_{C3}	∗3		0.59V_{C5}	0.63V_{C5}	0.58V_{C5}	0.63V_{C5}
V_{C4}	∗4		0.80V_{C5}	0.84V_{C5}	0.77V_{C5}	0.89V_{C5}
V_{C5} TYPE A (4.5 V)	∗5	LCX = 0H	Typ. × 0.94	Typ. × 1.06	Not set	Not set
		LCX = 1H				
		LCX = 2H				
		LCX = 3H				
		LCX = 4H				
		LCX = 5H				
		LCX = 6H				
		LCX = 7H				
		LCX = 8H				
		LCX = 9H				
		LCX = AH				
		LCX = BH				
		LCX = CH				
		LCX = DH				
		LCX = EH				
		LCX = FH				
V_{C5} TYPE B (5.5 V)	∗5	LCX = 0H	Typ. × 0.94	Typ. × 1.06	Typ. × 0.90	Typ. × 1.10
		LCX = 1H				
		LCX = 2H				
		LCX = 3H				
		LCX = 4H				
		LCX = 5H				
		LCX = 6H				
		LCX = 7H				
		LCX = 8H				
		LCX = 9H				
		LCX = AH				
		LCX = BH				
		LCX = CH				
		LCX = DH				
		LCX = EH				
		LCX = FH				

∗1: when a 1 MΩ load resistor is connected between V_{SS} and V_{C1} (Unit: V)
∗2: when a 1 MΩ load resistor is connected between V_{SS} and V_{C2}
∗3: when a 1 MΩ load resistor is connected between V_{SS} and V_{C3}
∗4: when a 1 MΩ load resistor is connected between V_{SS} and V_{C4}
∗5: when a 1 MΩ load resistor is connected between V_{SS} and V_{C5}

For details on the LCD drive voltage, refer to Section 6.4, "Analog Circuit Characteristics", in this manual and Section 7.4 in the "E0C88348 Technical Manual".

3.4 Initial Reset

When turning the E0C88P348 power on, the $\overline{\text{RESET}}$ terminal must be maintained at a Low level until the supply voltage goes to 3.3 V or more.

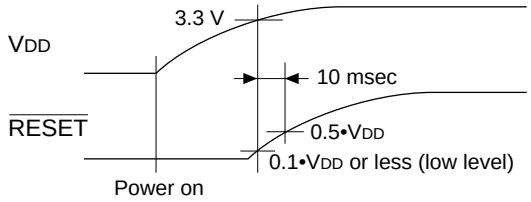


Fig. 3.4.1 Initial reset at power-on

The E0C88P348 uses initial reset as a trigger for setting either the normal operation mode or the programming mode. Therefore, design the reset input circuit so that the IC will be reset for sure. Initial resetting during operation is the same as the E0C88348.
When resetting the IC in the normal operation mode, make sure to fix the XSPRG terminal at a High level. Moreover, the VPP terminal for PROM programming power supply must be fixed at 5 V during initial reset even when setting the programming mode. Do not reset the IC when 12.5 V is being supplied to the VPP terminal.

3.5 ROM

The E0C88P348 has employed a PROM for the internal ROM. The memory capacity is the same as the E0C88348 at 48K bytes.
The PROM can be rewritten up to10 times. Rewriting data is done at the user's own risk.

3.6 Oscillation Circuit

In the E0C88P348, a crystal oscillator can only be used for the OSC1 oscillation circuit and a crystal or ceramic oscillator for the OSC3 oscillation circuit.
Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure there is enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

3.7 SVD Circuit

The E0C88P348 has a built-in SVD circuit similar to the E0C88348, but each detection level is different from the E0C88348. Furthermore, the range of detection levels is limited because the operating voltage range is different.

Table 3.7.1 SVD detection level of E0C88348/88P348

Detection level	E0C88348			E0C88P348		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Level 1 → Level 0	Typ. × 0.92	1.82	Typ. × 1.08	Not set		
Level 2 → Level 1		2.00		Not set		
Level 3 → Level 2		2.18		Not set		
Level 4 → Level 3		2.36		Not set		
Level 5 → Level 4		2.54		Not set		
Level 6 → Level 5		2.72		Not set		
Level 7 → Level 6		2.90		Not set		
Level 8 → Level 7		3.08		Not set		
Level 9 → Level 8		3.26		Typ. × 0.80	3.26	Typ. × 1.20
Level 10 → Level 9	Typ. × 0.88	3.45	Typ. × 1.12		3.45	
Level 11 → Level 10		3.65			3.65	
Level 12 → Level 11		3.85			3.85	
Level 13 → Level 12		4.05			4.05	
Level 14 → Level 13		4.25			4.25	
Level 15 → Level 14		4.50			4.50	

(Unit: V)

The mask option for reseting when low voltage is detected (available in the E0C88348) is not provided in the E0C88P348. Therefore, the function cannot be used with the E0C88P348.

CHAPTER 4 SUMMARY OF NOTES

4.1 Notes Related to the PROM

(1) The PROM bit data is set to "1" at shipment. Therefore, It must be programmed before operating the IC in the normal operation mode.

(2) The PROM data can be rewritten up to10 times.

(3) The circuit board should be designed so that the terminals can switch the input signals that differ between the PROM serial programming mode and the normal operation mode.

(4) The terminals for the PROM programmer should be set correctly according to the operating mode and fixed so that they cannot be changed during operation. Especially the XSPRG terminal must be fixed at a Low level in the programming mode, while they must be fixed at a High level in the normal operation mode. Changing the voltage level may damage the IC.

(5) Be sure to set VPP to 5 V at the IC power on or initial reset regardless of the operating mode to be set. Note that the IC may be damaged if 12.5 V has been supplied to the VPP terminal at power on or initial reset. To prevent damage of the IC, do not supply 12.5 V of programming voltage in the normal operation mode.

(6) If the operation of the E0C88P348 is unstable even though the writing and verification of the PROM data was completed normally, write and verify the PROM data without erasing the PROM.

(7) Rewriting the PROM is done at on the user's own risk.

4.2 Notes on Differences form the E0C88348

Be aware of the following notes when using the E0C88P348 as a development tool for the E0C88348.

Power supply

The E0C88P348 is operable with a supply voltage within the range of 3.3 V to 5.5 V. Be aware that as the supply voltage is different from the E0C88348 the electrical characteristics differ.

Initial reset

Note that the power-on reset time differs from the E0C88348 because the supply voltage is different. For the electrical characteristics, refer to "Power-on reset" in Section 6.6.
Furthermore, the reset functions using the input port (K00–K03) simultaneous low input or SVD circuit cannot be used because the mask option is fixed at "Not used".

Oscillation circuit

In the E0C88P348, a crystal oscillator can only be used for the OSC1 oscillation circuit and a crystal or ceramic oscillator for the OSC3 oscillation circuit.
Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure there is enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

LCD controller

The LCD drive voltage range of the E0C88P348 is different from that of the E0C88348. Check the electrical characteristic differences by referring to this manual and the "E0C88348 Technical Manual" before designing the LCD unit. Moreover, note that because mask options are not available, the LCD drive duty and LCD power specification of the E0C88P348 are fixed at 1/32 or 1/16 duty and the internal power supply is TYPE B (5.5 V).

SVD circuit

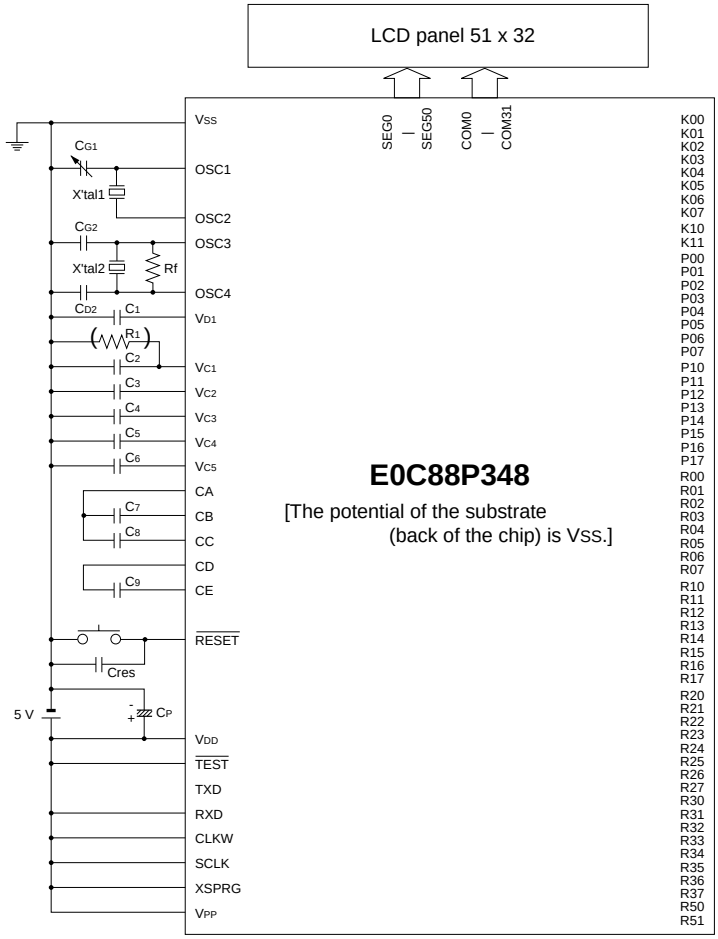
The SVD detection levels of the E0C88P348 are different from those of the E0C88348 because the operating voltage is different. When using the SVD function, check the available detection level.

Mask option

In the E0C88P348, the specifications selected by the E0C88348 mask options are fixed and cannot be selected. Therefore, some optional functions cannot be used in the E0C88P348. Check whether the functions are enabled or not in this manual and the "E0C88348 Technical Manual".

CHAPTER 5 BASIC EXTERNAL WIRING DIAGRAM

• During normal operation:



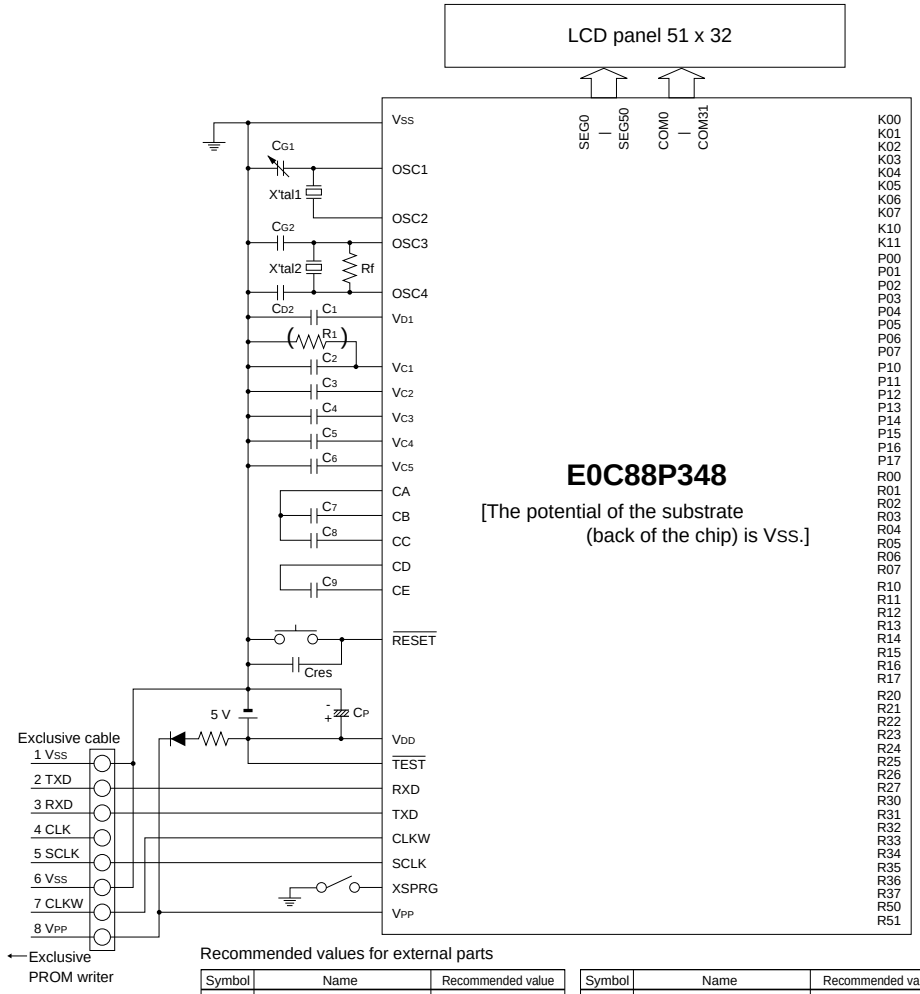
Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI (Max.) = 35 kΩ
X'tal2	Crystal oscillator	4.9152 MHz
Rf	Feedback resistor	1 MΩ
C_{G1}	Trimmer capacitor	5–25 pF
C_{G2}	Gate capacitor	15 pF
C_{D2}	Drain capacitor	15 pF
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF

Symbol	Name	Recommended value
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_9	Booster capacitors	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF
R_1	Load resistor between V_{SS} and V_{C1}	100 kΩ (It is needed when driving an LCD panel that constitutes a heavy load.)

Note: The above table is simply an example.

• ***During PROM serial programming:***



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI (Max.) = 35 kΩ
X'tal2	Crystal oscillator	4.9152 MHz
Rf	Feedback resistor	1 MΩ
C_{G1}	Trimmer capacitor	5–25 pF
C_{G2}	Gate capacitor	15 pF
C_{D2}	Drain capacitor	15 pF
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF

Symbol	Name	Recommended value
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_9	Booster capacitors	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{\text{RESET}}$ terminal	0.47 µF
R_1	Load resistor between V_{SS} and V_{C1}	100 kΩ (It is needed when driving an LCD panel that constitutes a heavy load.)

Note: The above table is simply an example.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

Note: The electrical characteristics of the E0C88P348 are different from those of the E0C88348. The following characteristics should be used as reference values when using the E0C88P348 as a development tool. ("" indicates that the characteristic value is different from the E0C88348.)*

6.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +6.4*	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +6.4*	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	1
Operating temperature	Topr		20 to 30*	°C	
Storage temperature	Tstg		-65 to +150	°C	2

Note) 1 In case of plastic package.
2 This rated value cannot insure the PROM data holding function.

6.2 Recommended Operating Conditions

(V_{SS} = 0 V, Ta = 20 to 30°C *)

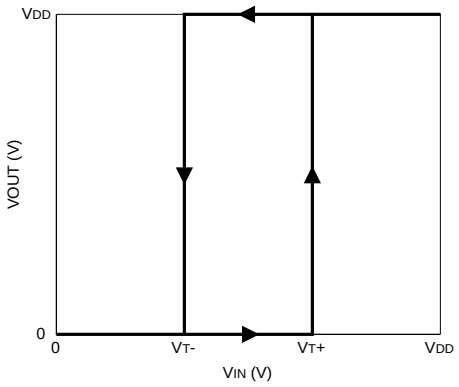
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		3.3*		5.5	V	
Operating power voltage (High-speed mode)	V_{DD}		4.5*		5.5	V	
PROM power voltage*	V_{PP}	Normal operation mode		V_{DD}*		V	
		Programming mode	12.2*	12.5*	12.8*	V	
Operating frequency	f_{OSC1}	V_{DD} = 3.3 to 5.5 V	30.000	32.768	50.000	kHz	
(Normal mode)	f_{OSC3}		0.03		4.2*	MHz	
Operating frequency	f_{OSC1}	V_{DD} = 4.5 to 5.5 V	30.000	32.768	50.000	kHz	
(High-speed mode)	f_{OSC3}		0.03		6.0*	MHz	
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	3
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	3
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	3
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	3
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	3
Capacitor between CA and CB	C_7			0.1		µF	3
Capacitor between CA and CC	C_8			0.1		µF	3
Capacitor between CD and CE	C_9			0.1		µF	3
Resistor between V_{C1} and V_{SS}	R_1			100		kΩ	4

Note) 3 No capacitor is required when the LCD power supply is not used. In this case, do not connect anything to the V_{C1}–V_{C5} and CA–CE terminals.
4 It is necessary when the panel load is large and for 1/32 duty driving.
The resistance value should be decided by connecting it to the actual panel to be used.

6.3 DC Characteristics

Unless otherwise specified: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage	V_{IH}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW	0.8V_{DD}		V_{DD}	V	
Low level input voltage	V_{IL}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW	0		0.2V_{DD}	V	
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.4V_{DD}*		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, TXD, V_{OH} = 0.9 V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, TXD, V_{OL} = 0.1 V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW, $\overline{RESET}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx, TXD	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW, $\overline{RESET}$	100		650*	kΩ	
Input terminal capacitance	C_{IN}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW, V_{IN} = 0 V, f = 1 MHz, Ta = 25°C			25*	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1 V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1 V	5			µA	



6.4 Analog Circuit Characteristics

■ LCD drive circuit

The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number). Therefore, these should be evaluated by connecting to the actual panel to be used. Moreover, if the display is uneven with a large panel load, connect a resistor (R_1) between the V_{SS} and V_{C1} terminal. (It is necessary in 1/32 duty driving.)

Unless otherwise specified: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C, $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_8 = C_9$ = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	#1		0.18V_{C5}		0.22V_{C5}	V	
	V_{C2}	#2		0.38V_{C5}*		0.46V_{C5}*	V	
	V_{C3}	#3		0.58V_{C5}*		0.63V_{C5}*	V	
	V_{C4}	#4		0.77V_{C5}*		0.89V_{C5}*	V	
	V_{C5} (5.5V)	#5	LCX = 0H	Typ×0.90*	4.73	Typ×1.10*	V	
			LCX = 1H		4.83		V	
			LCX = 2H		4.92		V	
			LCX = 3H		5.02		V	
			LCX = 4H		5.11		V	
			LCX = 5H		5.21		V	
			LCX = 6H		5.30		V	
			LCX = 7H		5.40		V	
			LCX = 8H		5.50		V	
			LCX = 9H		5.60		V	
			LCX = AH		5.70		V	
			LCX = BH		5.81		V	
			LCX = CH		5.93		V	
			LCX = DH		6.05		V	
			LCX = EH		6.17		V	
			LCX = FH		6.29		V	

#1 Connects 1 MΩ load resistor between V_{SS} and V_{C1}. (without panel load)

#2 Connects 1 MΩ load resistor between V_{SS} and V_{C2}. (without panel load)

#3 Connects 1 MΩ load resistor between V_{SS} and V_{C3}. (without panel load)

#4 Connects 1 MΩ load resistor between V_{SS} and V_{C4}. (without panel load)

#5 Connects 1 MΩ load resistor between V_{SS} and V_{C5}. (without panel load)

■ SVD circuit

Unless otherwise specified: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 9 → Level 8	Typ×0.80*	3.26	Typ×1.20*	V	5
		Level 10 → Level 9		3.45		V	5
		Level 11 → Level 10		3.65		V	5
		Level 12 → Level 11		3.85		V	5
		Level 13 → Level 12		4.05		V	5
		Level 14 → Level 13		4.25		V	5
		Level 15 → Level 14		4.50		V	6

$V_{SVD\ (Level\ 8)} < V_{SVD\ (Level\ 9)} < V_{SVD\ (Level\ 10)} < V_{SVD\ (Level\ 11)} < V_{SVD\ (Level\ 12)} < V_{SVD\ (Level\ 13)} < V_{SVD\ (Level\ 14)} < V_{SVD\ (Level\ 15)}$

Note) Levels 0 to 7 are not available in the E0C88P348.

5 Corresponds with normal operation mode.

6 Corresponds with normal and high-speed operating modes.

6.5 Power Current Consumption

Unless otherwise specified: V_{DD} = within the range of each operating mode, V_{SS} = 0 V, Ta = 25°C, OSC1 = 32.768 kHz crystal oscillation, C_G = 25pF, OSC3 = external clock input, Non heavy load protection mode, $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_8 = C_9$ = 0.1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status #1			1	µA	
	I_{DD2}	In HALT status #2			7*	µA	
	I_{DD3}	CPU is in operating #3 (V_{DD} = 5.5 V, 32.768 kHz)			12*	mA	
	I_{DD4}	CPU is in operating #4 (V_{DD} = 5.5 V, 1 MHz)			15*	mA	
	I_{DD5}	CPU is in operating #3 (V_{DD} = 3.3 V, 32.768 kHz)			4*	mA	
	I_{DD6}	CPU is in operating #4 (V_{DD} = 3.3 V, 1 MHz)			6*	mA	
	I_{HVL}	In heavy load protection mode			12*	mA	7
Power current (High speed mode)	I_{DD1}	In SLEEP status #1			2*	µA	
	I_{DD2}	In HALT status #2			11*	µA	
	I_{DD3}	CPU is in operating #3 (V_{DD} = 5.5 V, 32.768 kHz)			12*	mA	
	I_{DD4}	CPU is in operating #4 (V_{DD} = 5.5 V, 1 MHz)			15*	mA	
	I_{DD5}	CPU is in operating #3 (V_{DD} = 4.5 V, 32.768 kHz)			8*	mA	
	I_{DD6}	CPU is in operating #4 (V_{DD} = 4.5 V, 1 MHz)			10*	mA	
	I_{HVL}	In heavy load protection mode			12*	mA	7
LCD drive circuit current	I_{LCDN}	V_{DD} = 5.5 V			20*	µA	
	I_{LCDH}	In heavy load protection mode			40*	µA	7
SVD circuit current	I_{SVDN}	V_{DD} = 5.5 V			180*	µA	8
	I_{SVDH}	In heavy load protection mode			240*	µA	7

#1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
#2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
#3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768 kHz, Clock timer: Operating, Others: Stop status
#4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 1 MHz, Clock timer: Operating, Others: Stop status

Note) 7 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).

8 The value when V_{DD} = ***x*** V can be found by the following expression: I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 60*) - 150* (Max. value)

6.6 AC Characteristics

■ External memory access

• Read cycle (Normal operating mode)

Condition: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	tc+tl-100+n·tc/2			nS	9
Address hold time in read cycle	trah	th-80			nS	
Read signal pulse width	trp	tc-50*+n·tc/2			nS	9
Data input set-up time in read cycle	trds	300			nS	
Data input hold time in read cycle	trdh	0			nS	

Note) 9 Substitute the number of states for wait insertion in n.

• Read cycle (High speed operating mode)

Condition: V_{DD} = 4.5* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 2.4 V, V_{IL2} = 0.9 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in read cycle	tras	tc+tl-50+n·tc/2			nS	9
Address hold time in read cycle	trah	th-40			nS	
Read signal pulse width	trp	tc-25*+n·tc/2			nS	9
Data input set-up time in read cycle	trds	150			nS	
Data input hold time in read cycle	trdh	0			nS	

Note) 9 Substitute the number of states for wait insertion in n.

• Write cycle (Normal operating mode)

Condition: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	tc-180			nS	
Address hold time in write cycle	twah	th-80			nS	
Write signal pulse width	twp	tl-40+n·tc/2			nS	9
Data output set-up time in write cycle	twds	tc-180+n·tc/2			nS	9
Data output hold time in write cycle	twdh	th-80			nS	

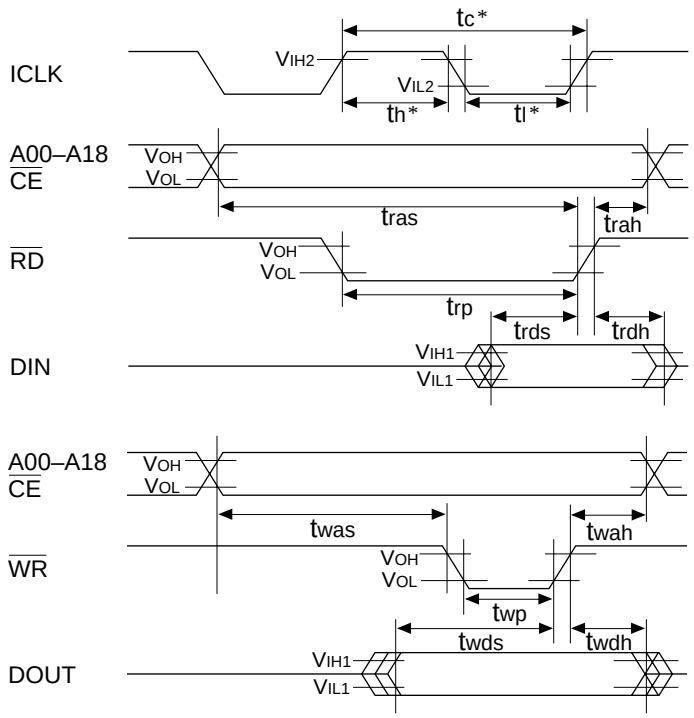
Note) 9 Substitute the number of states for wait insertion in n.

• Write cycle (High speed operating mode)

Condition: V_{DD} = 4.5* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{IH2} = 2.4 V, V_{IL2} = 0.9 V, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}, C_L = 100 pF (load capacitance)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Address set-up time in write cycle	twas	tc-90			nS	
Address hold time in write cycle	twah	th-40			nS	
Write signal pulse width	twp	tl-20+n·tc/2			nS	9
Data output set-up time in write cycle	twds	tc-90+n·tc/2			nS	9
Data output hold time in write cycle	twdh	th-40			nS	

Note) 9 Substitute the number of states for wait insertion in n.



* In the case of crystal oscillation and ceramic oscillation: th = 0.5tc ± 0.05tc, tl = tc - th (1/tc: oscillation frequency)

■ Serial interface

• Clock synchronous master mode (Normal operating mode)

Condition: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			200	nS	
Receiving data input set-up time	tsms	500			nS	
Receiving data input hold time	tsmh	200			nS	

• Clock synchronous master mode (High speed operating mode)

Condition: V_{DD} = 4.5* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			100	nS	
Receiving data input set-up time	tsms	250			nS	
Receiving data input hold time	tsmh	100			nS	

• Clock synchronous slave mode (Normal operating mode)

Condition: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			500	nS	
Receiving data input set-up time	tsss	200			nS	
Receiving data input hold time	tssh	200			nS	

• Clock synchronous slave mode (High speed operating mode)

Condition: V_{DD} = 4.5* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			250	nS	
Receiving data input set-up time	tsss	100			nS	
Receiving data input hold time	tssh	100			nS	

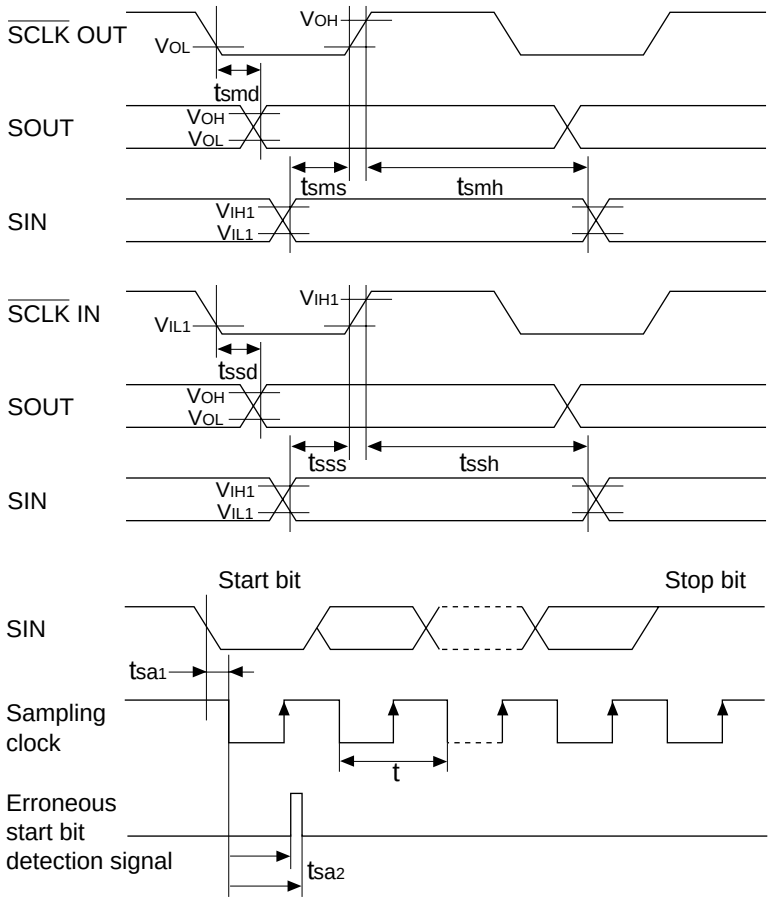
- **Asynchronous system (All operating mode)**

Condition: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	S	10
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	S	11

Note) 10 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

11 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)



■ Input clock

• $\overline{\text{SCLK}}$, EVIN input clock (Normal operating mode)

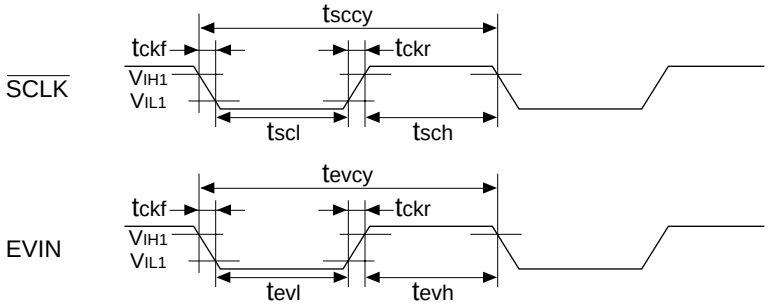
Condition: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLK}}$ input clock time	Cycle time	tsccy	4			µS	
	"H" pulse width	tsch	2			µS	
	"L" pulse width	tscl	2			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	4			µS	
	"H" pulse width	tevh	2			µS	
	"L" pulse width	tevl	2			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	

• $\overline{\text{SCLK}}$, EVIN input clock (High speed operating mode)

Condition: V_{DD} = 4.5* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

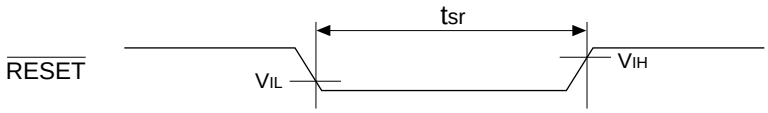
Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{\text{SCLK}}$ input clock time	Cycle time	tsccy	2			µS	
	"H" pulse width	tsch	1			µS	
	"L" pulse width	tscl	1			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	2			µS	
	"H" pulse width	tevh	1			µS	
	"L" pulse width	tevl	1			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	



• $\overline{\text{RESET}}$ input pulse (All operating mode)

Condition: V_{DD} = 3.3* to 5.5 V, V_{SS} = 0 V, Ta = 25°C*, V_{IH} = 0.5V_{DD}, V_{IL} = 0.1V_{DD}

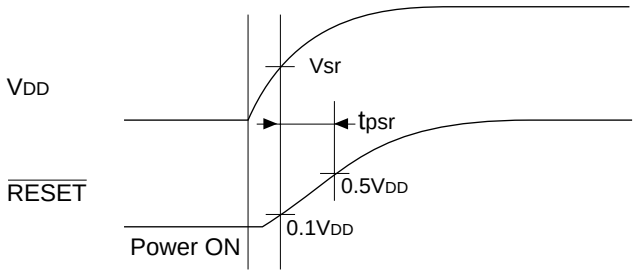
Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µS	

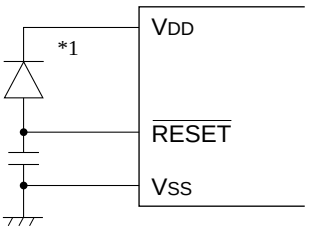


■ Power ON reset

Condition: VSS = 0 V, Ta = 25°C*

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	3.3			V	
$\overline{\text{RESET}}$ input time	tpsr	10			mS	





*1 Because the potential of the $\overline{\text{RESET}}$ terminal not reached VDD level or higher.

■ Operating mode switching

Condition: VDD = 3.3* to 5.5 V, VSS = 0 V, Ta = 25°C*

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Stabilization time	tvdc	5			mS	12

Note) 12 Stabilization time is the time from switching on the operating mode until operating mode is stabilized. For example, when turning the OSC3 oscillation circuit on, stabilization time is needed after the operating mode is switched on.

6.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator or cryctal oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

■ OSC1 (Crystal)

Unless otherwise specified: V_{DD} = within the range of each operating mode, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = C2-TYPE#1, C_{G1} = 25 pF, C_{D1} = Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	S	
External gate capacitance	C_{G1}	Including board capacitance	5		25	pF	
Built-in drain capacitance	C_{D1}	In case of the chip		13*		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-10		10	ppm	
Frequency/power voltage deviation	∂f/∂V_{DD}				2*	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 5 to 25 pF	15*			ppm	
Frequency/operating mode devistion	∂f/∂MD	V_{DD} = constant			20	ppm	

#1 C2-TYPE Made by Seiko Epson corporation

■ OSC3 (Crystal)

Unless otherwise specified: V_{DD} = within the range of each operating mode, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = CA-301 4MHz / CA-301 8MHz#1, R_F = 1 MΩ, C_{G2} = C_{D2} = 15 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz crystal oscillator			20	mS	13
Oscillation start time (High speed mode)	tsta	8.0 MHz crystal oscillator			20	mS	13

#1 CA-301 4MHz / CA-301 8MHz Made by Seiko Epson corporation
Note) 13 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G2} and C_{D2}.

■ OSC3 (Ceramic)

Unless otherwise specified: V_{DD} = within the range of each operating mode, V_{SS} = 0 V, Ta = 25°C,
Ceramic oscillator = CSA4.00MG/CSA8.00MTZ#1, R_F = 1 MΩ, C_{G2} = C_{D2} = 30 pF

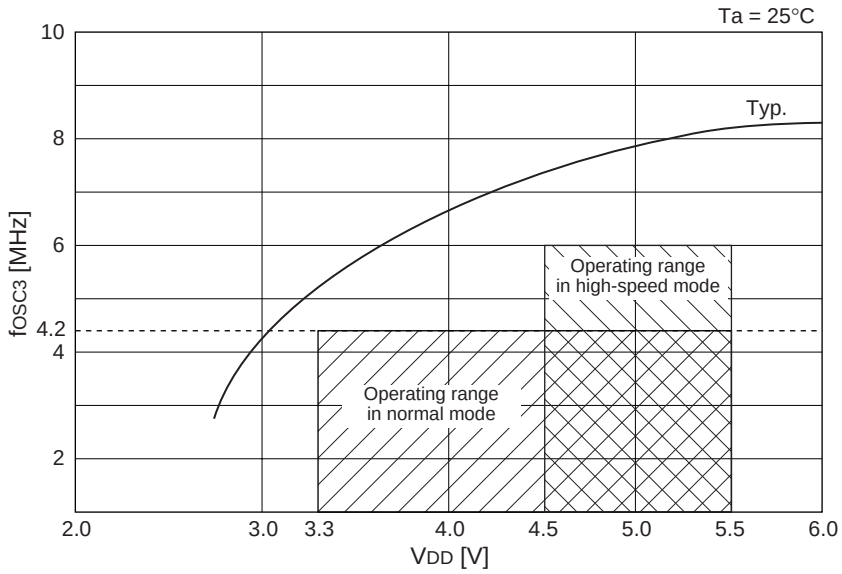
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz ceramic oscillator			5	mS	
Oscillation start time (High speed mode)	tsta	8.0 MHz ceramic oscillator			5	mS	

#1 CSA4.00MG/CSA8.00MTZ Made by Murata Mfg. Co.

6.8 Characteristics Curves (reference value)

■ Operating range

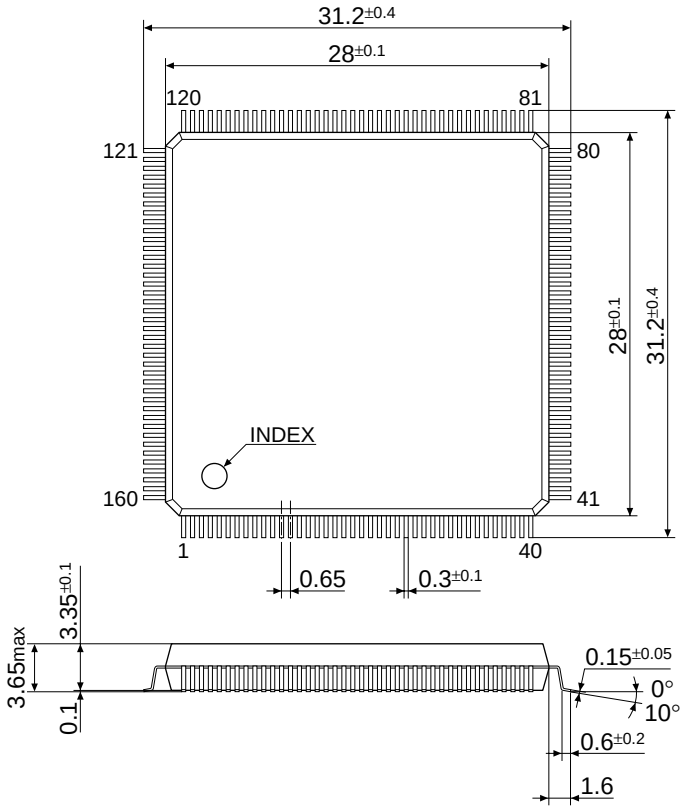
Operating conditions should be determined within the operating range shown in the figure below.



CHAPTER 7 PACKAGE

QFP8-160pin

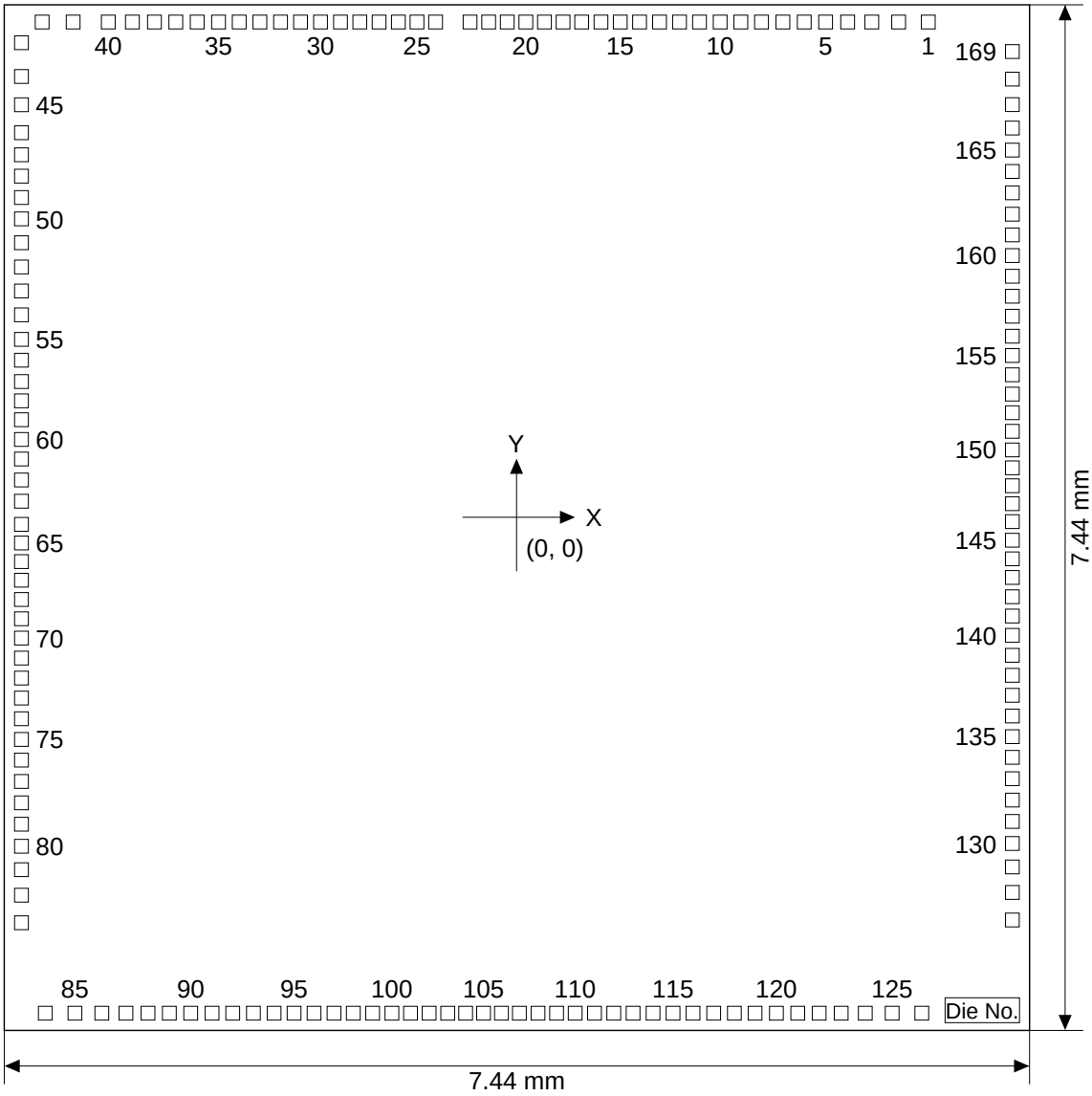
(Unit: mm)



The dimensions are subject to change without notice.

CHAPTER 8 PAD LAYOUT

8.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

8.2 Pad Coordinates

(Unit: mm)

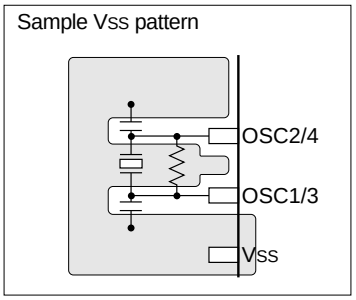
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	COM24/SEG58	2.985	3.595	44	OSC1	-3.595	3.200	87	R14/A12	-2.837	-3.595	130	SEG21	3.595	-2.364
2	COM23/SEG59	2.770	3.595	45	OSC2	-3.595	2.995	88	R15/A13	-2.677	-3.595	131	SEG22	3.595	-2.204
3	COM22/SEG60	2.575	3.595	46	$\overline{\text{TEST}}$	-3.595	2.792	89	R16/A14	-2.522	-3.595	132	SEG23	3.595	-2.049
4	COM21/SEG61	2.400	3.595	47	$\overline{\text{RESET}}$	-3.595	2.632	90	R17/A15	-2.367	-3.595	133	SEG24	3.595	-1.894
5	COM20/SEG62	2.240	3.595	48	V_{PP}	-3.595	2.477	91	R20/A16	-2.212	-3.595	134	SEG25	3.595	-1.739
6	COM19/SEG63	2.085	3.595	49	K11/$\overline{\text{BREQ}}$	-3.595	2.322	92	R21/A17	-2.062	-3.595	135	SEG26	3.595	-1.589
7	COM18/SEG64	1.930	3.595	50	K10/EVIN	-3.595	2.167	93	R22/A18	-1.912	-3.595	136	SEG27	3.595	-1.439
8	COM17/SEG65	1.775	3.595	51	K07	-3.595	1.994	94	R23/$\overline{\text{RD}}$	-1.762	-3.595	137	SEG28	3.595	-1.289
9	COM16/SEG66	1.625	3.595	52	K06	-3.595	1.818	95	R24/$\overline{\text{WR}}$	-1.617	-3.595	138	SEG29	3.595	-1.144
10	COM15	1.475	3.595	53	K05	-3.595	1.644	96	R25/CL	-1.472	-3.595	139	SEG30	3.595	-0.999
11	COM14	1.325	3.595	54	K04	-3.595	1.471	97	R26/FR	-1.327	-3.595	140	SEG31	3.595	-0.854
12	COM13	1.180	3.595	55	K03	-3.595	1.293	98	R27/TOUT	-1.187	-3.595	141	SEG32	3.595	-0.714
13	COM12	1.035	3.595	56	K02	-3.595	1.142	99	R30/$\overline{\text{CE0}}$	-1.047	-3.595	142	SEG33	3.595	-0.574
14	COM11	0.890	3.595	57	K01	-3.595	0.987	100	R31/$\overline{\text{CE1}}$	-0.907	-3.595	143	SEG34	3.595	-0.434
15	COM10	0.750	3.595	58	K00	-3.595	0.847	101	R32/$\overline{\text{CE2}}$	-0.772	-3.595	144	SEG35	3.595	-0.299
16	COM9	0.610	3.595	59	P17	-3.595	0.710	102	R33/$\overline{\text{CE3}}$	-0.637	-3.595	145	SEG36	3.595	-0.164
17	COM8	0.470	3.595	60	P16	-3.595	0.567	103	R34/FOUT	-0.502	-3.595	146	SEG37	3.595	-0.029
18	COM7	0.335	3.595	61	P15	-3.595	0.425	104	R35	-0.372	-3.595	147	XSPRG	3.595	0.101
19	COM6	0.200	3.595	62	P14	-3.595	0.273	105	R36	-0.242	-3.595	148	CLKW	3.595	0.231
20	COM5	0.065	3.595	63	P13/$\overline{\text{SRDY}}$	-3.595	0.119	106	R37	-0.112	-3.595	149	N.C.	3.595	0.361
21	RXD	-0.070	3.595	64	P12/$\overline{\text{SCLK}}$	-3.595	-0.049	107	R50/BZ	0.018	-3.595	150	SEG38	3.595	0.491
22	SCLK	-0.205	3.595	65	P11/SOUT	-3.595	-0.184	108	R51/$\overline{\text{BACK}}$	0.153	-3.595	151	SEG39	3.595	0.626
23	TXD	-0.340	3.595	66	P10/SIN	-3.595	-0.319	109	SEG0	0.288	-3.595	152	SEG40	3.595	0.761
24	COM4	-0.590	3.595	67	P07/D7	-3.595	-0.454	110	SEG1	0.423	-3.595	153	SEG41	3.595	0.896
25	COM3	-0.725	3.595	68	P06/D6	-3.595	-0.594	111	SEG2	0.563	-3.595	154	SEG42	3.595	1.036
26	COM2	-0.860	3.595	69	P05/D5	-3.595	-0.734	112	SEG3	0.703	-3.595	155	SEG43	3.595	1.176
27	COM1	-1.000	3.595	70	P04/D4	-3.595	-0.874	113	SEG4	0.843	-3.595	156	SEG44	3.595	1.316
28	COM0	-1.140	3.595	71	P03/D3	-3.595	-1.019	114	SEG5	0.988	-3.595	157	SEG45	3.595	1.461
29	CE	-1.280	3.595	72	P02/D2	-3.595	-1.164	115	SEG6	1.133	-3.595	158	SEG46	3.595	1.606
30	CD	-1.425	3.595	73	P01/D1	-3.595	-1.309	116	SEG7	1.278	-3.595	159	SEG47	3.595	1.751
31	CC	-1.570	3.595	74	P00/D0	-3.595	-1.459	117	SEG8	1.428	-3.595	160	SEG48	3.595	1.901
32	CB	-1.715	3.595	75	R00/A0	-3.595	-1.609	118	SEG9	1.578	-3.595	161	SEG49	3.595	2.051
33	CA	-1.865	3.595	76	R01/A1	-3.595	-1.759	119	SEG10	1.728	-3.595	162	SEG50	3.595	2.201
34	V_{C5}	-2.015	3.595	77	R02/A2	-3.595	-1.914	120	SEG11	1.883	-3.595	163	COM31/SEG51	3.595	2.356
35	V_{C4}	-2.165	3.595	78	R03/A3	-3.595	-2.069	121	SEG12	2.038	-3.595	164	COM30/SEG52	3.595	2.511
36	V_{C3}	-2.320	3.595	79	R04/A4	-3.595	-2.224	122	SEG13	2.193	-3.595	165	COM29/SEG53	3.595	2.666
37	V_{C2}	-2.475	3.595	80	R05/A5	-3.595	-2.384	123	SEG14	2.353	-3.595	166	COM28/SEG54	3.595	2.826
38	V_{C1}	-2.630	3.595	81	R06/A6	-3.595	-2.554	124	SEG15	2.528	-3.595	167	COM27/SEG55	3.595	2.996
39	OSC3	-2.790	3.595	82	R07/A7	-3.595	-2.739	125	SEG16	2.723	-3.595	168	COM26/SEG56	3.595	3.181
40	OSC4	-2.965	3.595	83	R10/A8	-3.595	-2.939	126	SEG17	2.938	-3.595	169	COM25/SEG57	3.595	3.381
41	V_{D1}	-3.220	3.595	84	R11/A9	-3.422	-3.595	127	SEG18	3.595	-2.919	–			
42	V_{DD}	-3.445	3.595	85	R12/A10	-3.207	-3.595	128	SEG19	3.595	-2.719	–			
43	V_{SS}	-3.595	3.445	86	R13/A11	-3.012	-3.595	129	SEG20	3.595	-2.534	–			

N.C. : No connection

CHAPTER 9 PRECAUTIONS ON MOUNTING

<Oscillation circuit>

- When using the crystal or ceramic oscillation circuit, make a board pattern that is protected against noise as shown in the figure below.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1/OSC3 and VDD, please keep enough distance between OSC1/OSC3 and VDD or other signals on the board pattern.

<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

EPSON International Sales Operations

AMERICA

S-MOS SYSTEMS, INC.
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200 Fax: +1-408-922-0238
Telex: 176079 SMOS SNJUD

S-MOS SYSTEMS, INC.
EASTERN AREA SALES AND TECHNOLOGY CENTER
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-617-246-3600 Fax: +1-617-246-5443

S-MOS SYSTEMS, INC.
SOUTH EASTERN AREA SALES AND TECHNOLOGY CENTER
4300 Six Forks Road, Suite 430
Raleigh, NC 27609, U.S.A.
Phone: +1-919-781-7667 Fax: +1-919-781-6778

S-MOS SYSTEMS, INC.
CENTRAL AREA SALES AND TECHNOLOGY CENTER
1450 E.American Lane, Suite 1550
Schaumburg, IL 60173, U.S.A.
Phone: +1-847-517-7667 Fax: +1-847-517-7601

EUROPE

- HEADQUARTERS -

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15
80992 Muenchen, GERMANY
Phone: +49-(0)89-14005-0 Fax: +49-(0)89-14005-110

- GERMANY -

EPSON EUROPE ELECTRONICS GmbH
SALES OFFICE
Breidenbachstrasse 46
D-51373 Leverkusen, GERMANY
Phone: +49-(0)214-83070-0 Fax: +49-(0)214-83070-10

- UNITED KINGDOM -

EPSON EUROPE ELECTRONICS GmbH
UK BRANCH OFFICE
G6 Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700 Fax: +44-(0)1344-381701

- FRANCE -

EPSON EUROPE ELECTRONICS GmbH
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350 Fax: +33-(0)1-64862355

ASIA

- HONG KONG, CHINA -

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone: +852-2585-4600 Fax: +852-2827-4346
Telex: 65542 EPSCO HX

- CHINA -

SHANGHAI EPSON ELECTRONICS CO., LTD.
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552 Fax: 21-6485-0775

- TAIWAN, R.O.C. -

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei, TAIWAN, R.O.C.
Phone: 02-2717-7360 Fax: 02-2712-9164
Telex: 24444 EPSONTB

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN, R.O.C.
Phone: 03-573-9900 Fax: 03-573-9169

- SINGAPORE -

EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911 Fax: +65-334-2716

- KOREA -

SEIKO EPSON CORPORATION
KOREA OFFICE
10F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone: 02-784-6027 Fax: 02-767-3677

- JAPAN -

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I
(Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

In pursuit of **“Saving” Technology**, Epson electronic devices.
Our lineup of semiconductors, liquid crystal displays and quartz devices
assists in creating the products of our customers’ dreams.
Epson IS energy savings.

EPSON

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

■ Electronic devices information on the Epson WWW server

http://www.epson.co.jp

Issue MAR. 1998, Printed in Japan Ⓜ A