CF010-05

EPSON

ASIC

Gate Array / Standard Cell / Embedded Array

October / 1999

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

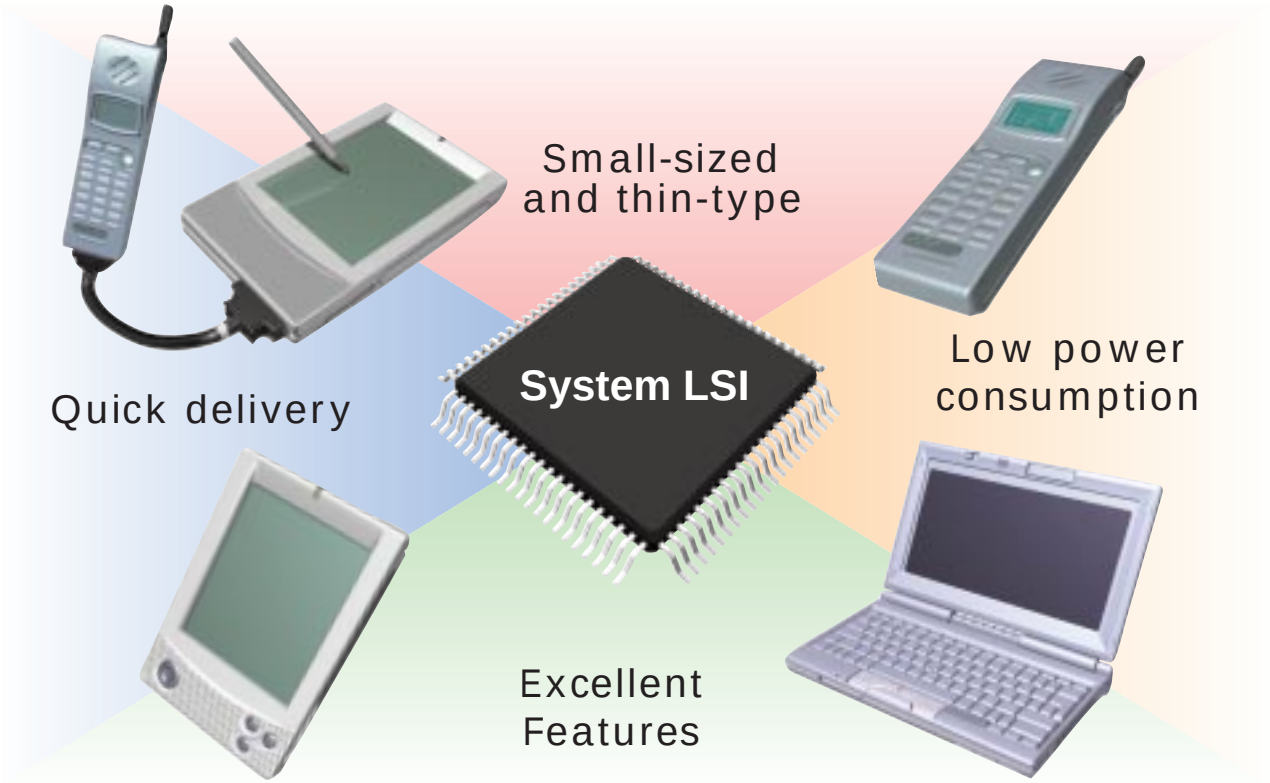
In pursuit of **“Saving” Technology**, Epson electronic devices.
Our lineup of semiconductors, liquid crystal displays and quartz devices assists in creating the products of our customers' dreams.
Epson IS energy savings.

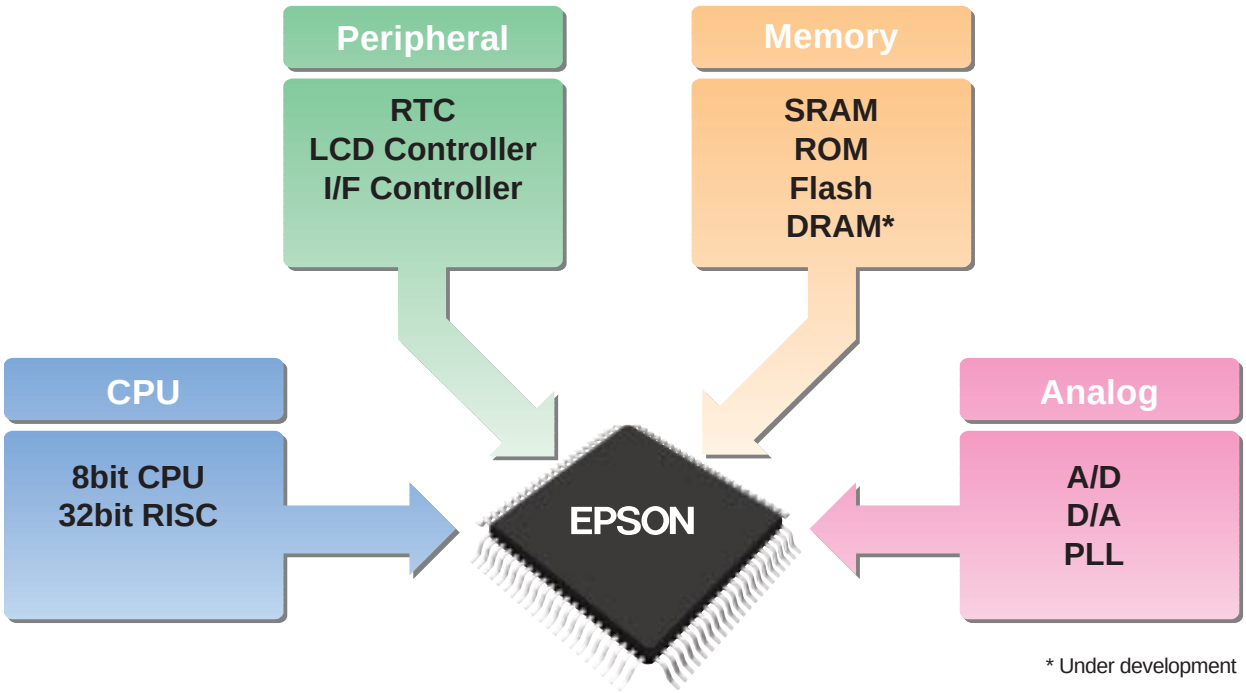
Contents

Energy Saving EPSON

SEIKO EPSON's System LSI Solutions

For coming 21st century, the system solutions will be provided by EPSON to achieve the system on-chip using ASIC technologies.
Design environment for System LSI will be also provided to meet a variety of customer needs. See enclosed slide for a suggested picture.





* Under development

EPSON ASIC Road Map

Gate Array

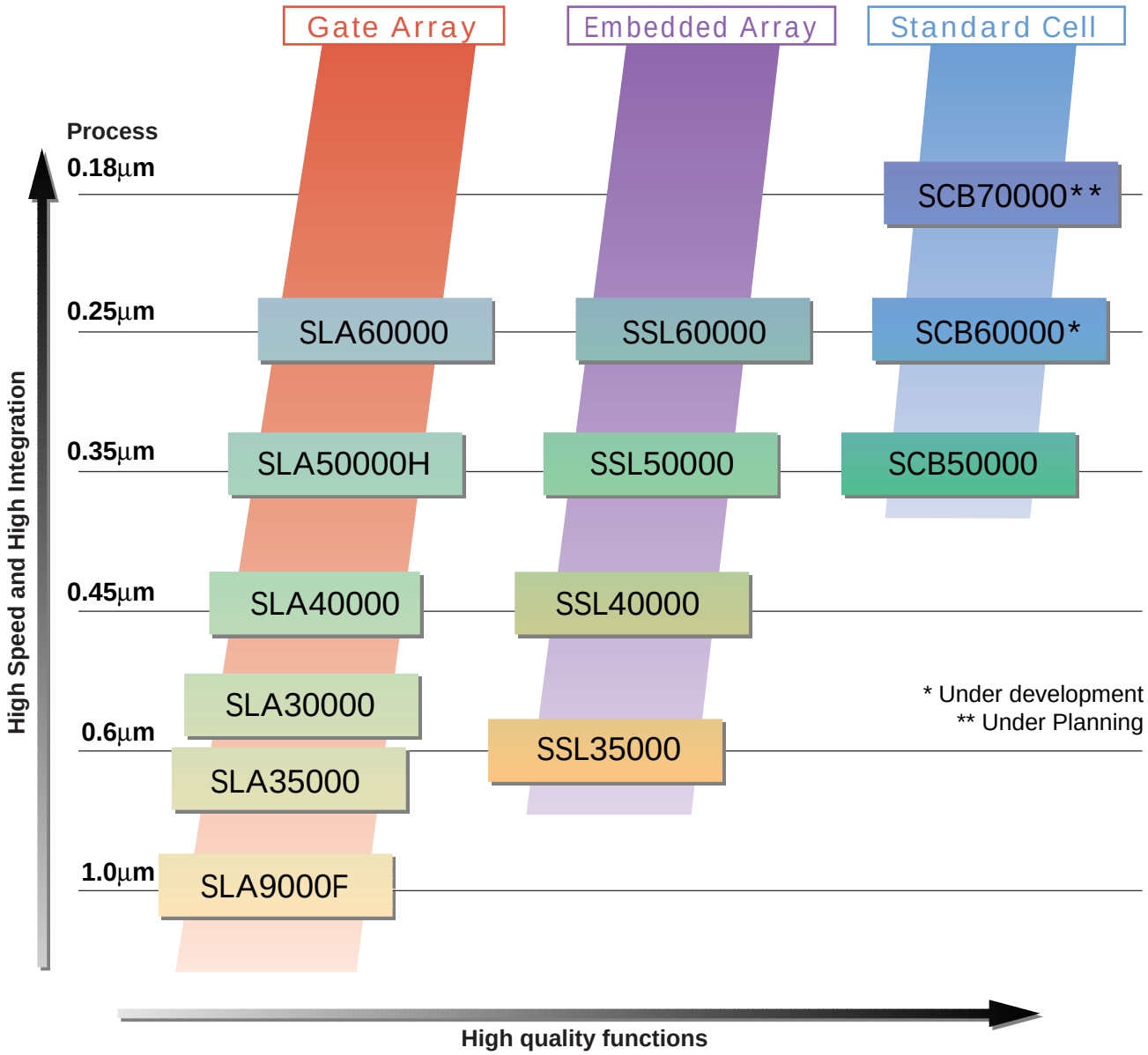
Quick delivery and low cost when developing a VLSI circuit.

Embedded Array

Can be designed by special features utilizing both Gate Array and Standard Cell.

Standard Cell

Can design an LSI with high integration and quality functions.



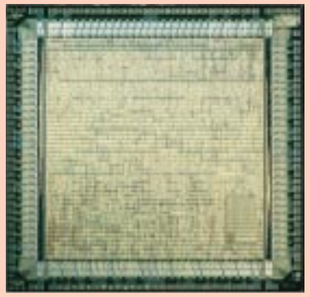
ASIC Products Line Up

EPSON supplies ASIC products - gate arrays, embedded arrays and standard cells. EPSON can produce the best system solution using the following products.

EPSON ASIC

Gate Array

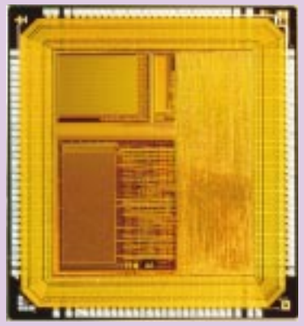
SLA60000	0.25µm	Low voltage, high speed and super-high integration CMOS Gate Array
SLA50000H	0.35µm	Correspond to 5V interfaces, high speed and integration CMOS Gate Array
SLA40000	0.45µm	Correspond to 5V interfaces, high speed and integration CMOS Gate Array
SLA35000	0.6µm	3V or 5V single, high-integration and low power CMOS Gate Array
SLA30000	0.6µm	3V and 5V, high speed CMOS Gate Array
SLA9000F	1.0µm	3V or 5V Single, CMOS Gate Array for Small Gate Counts



Gate array means a developing LSI method using ASIC technology composed of LSIs manufactured by a simple interconnecting process based on base bulk allocated transistors (basic cells) by a ruled array (row). Therefore, if the gate array method for developing LSIs is adopted, the development period can be shortened compared to a custom LSI. Furthermore, as many base bulks are provided, a wide gate band can be covered.

Embedded Array

SSL60000	0.25µm	Low voltage, high speed and high integration
SSL50000	0.35µm	High functions (many analog cells), low power consumption
SSL40000	0.45µm	Low power consumption
SSL35000	0.6µm	Many analog cells, possible to 5V single

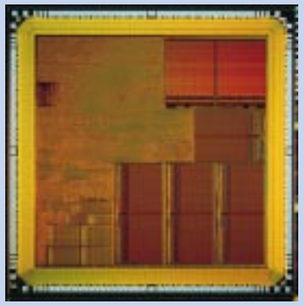


An embedded array is a semi-custom LSI using the new ASIC technology. It is composed of macro-standard cells, hard macro-cells for functional blocks for special usage like an ASSP, and so on. It is composed of the user's circuits by using the Sea of Gate system. This system has the same functions as the standard cell development, but it has the same development term as the gate array method, because it uses the sea of gate system for the logic part. It has the advantage that, even though a product design may need to be changed or modified, it can eliminate some risks because it is easier to change the circuit design.

Standard Cell

SCB60000*	0.25µm	Low voltage, super-high integration and high speed
SCB50000	0.35µm	Low voltage, high integration and high speed

* Under development



A standard cell is a semi-custom IC composed of the optimum designed internal logic cells, ROM, RAM, CPU and analog circuit on one chip. Compared to gate array, the standard cell can be designed more freely, and with higher functions and integration. Therefore, as the optimum system LSI can be produced, it is a very useful for product miniaturization, low power consumption.

Gate Array

The line-up of EPSON's CMOS Gate Array is shown in the following tables. The Gate Arrays have the characteristics of high speed, super-high integration and low power consumption.

Low voltage, high speed and integration CMOS Gate Array

SLA60000 Series

Series Name		SLA60000 Series									
Features		• Super-high density (adopting 0.25µm silicon gate CMOS with 3-, 4- and 5-metal layers) • High-speed operation (operation delay of internal gate = 107ps at 2.5V, 2-input power NAND standard) • Internal gate = 2.0 to 2.5V, I/O buffer = 3.3V, 2.5V and 2.0V (built-in level shifter) • Raw gate = 2.5M gate • RAM, ROM and various function cells available									
Master		SLA6009	SLA6017	SLA6028	SLA6040	SLA6059	SLA6083	SLA6123	SLA6158	SLA6190	SLA6251
Total BCs (Raw Gates)		99,200	171,720	284,394	400,290	595,362	831,572	1,234,820	1,587,754	1,902,960	2,519,604
Usable BCs	3-layer Metal	79,376	137,376	199,076	280,203	416,753	540,522	802,633	1,032,040	1,141,776	1,511,762
	4-layter Metal	89,298	154,548	241,735	340,247	506,058	665,258	987,856	1,270,203	1,427,220	1,889,703
Number of PADs (In Case of Micro Pitch)	80µm	(104)	(132)	(168)	(200)	(240)	284	344	388	424	488
	70µm	112	148	188	224	272	(320)	(388)	(440)	(480)	(552)
Propagation Delay	Internal Gates	t_{pd}=107ps (standard at 2.5V)									
	Input Buffers	t_{pd}=270ps (standard at 2.5V and F/O=2)									
	Output Buffers	t_{pd}=1600ps (standard at 2.5V and C_L=15pF)									
I/O Level		CMOS, LVTTL, PCI3.3V, LVDS*									
Input Mode		Normal, Pull-up/Pull-down, Schmitt, Level shifter, Fail-safe*, Gated*									
Output Mode		Normal, Open drain, 3-state, Bi-directional, Level shifter, Fail-safe*, Gated*									

* Under development

Correspond to 5V interfaces, high speed and integration CMOS Gate Array

SLA50000H Series

Series Name		SLA50000H Series										
Features		• Super-high density (adopting 0.35µm silicon gate CMOS with 2-, 3- and 4-metal layers) • High-speed operation (operation delay of internal gate = 0.140ns at 3.3V, 2-input power NAND standard) • Internal gate = 3.3V, 2.5V and 2.0V, I/O buffer = 5.0V, 3.3V and 2.0V (built-in level shifter) • Low power consumption (0.70µW/MHz/BC when internal cell = 3.3V) • Output drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24 mA when PCI = 5.0V, I_{OL} = 0.1, 1, 2, 6, 12mA when PCI = 3.3V, I_{OL} = 0.05, 0.3, 0.6, 2, 4, 8mA when 2.0V) • RAM, PLL*, IrDA* and various function cells available • Low noise output cell, PCI I/F, PECL I/F, USB I/F, Fail-Safe output, JTAG										
Master / Features	2-layer Metal	SLA5028H	SLA5075H	SLA5099H	SLA5125H	SLA5177H	SLA5250H	SLA5335H	SLA5442H	SLA5506H	SLA5668H	SLA5815H
	3-layer Metal	SLA502TH	SLA507TH	SLA509TH	SLA512TH	SLA517TH	SLA525TH	SLA533TH	SLA544TH	SLA550TH	SLA566TH	SLA581TH
	4-layer Metal	SLA502QH	SLA507QH	SLA509QH	SLA512QH	SLA517QH	SLA525QH	SLA533QH	SLA544QH	SLA550QH	SLA566QH	SLA581QH
Total BCs (Raw Gates)		28,710	75,774	99,198	125,772	177,062	250,160	335,858	442,112	506,688	668,552	815,468
Usable BCs	2-layer Metal	14,355	35,613	46,623	56,597	79,677	112,572	144,418	176,844	202,675	267,420	326,187
	3-layer Metal	25,264	64,407	84,318	100,617	132,796	187,620	251,893	309,478	354,681	467,986	570,827
	4-layer Metal	27,274	71,985	94,238	119,483	168,208	237,652	319,065	397,900	456,019	601,696	733,921
Number of PADs (In Case of Micro Pitch)		88 104	144 168	168 192	188 216	224	264	308	352	376	432	480
Propagatin Delay	Internal Gates	t_{pd} = 0.14ns (standard at 3.3V), 0.21ns (standard at 2.0V)										
	Input Buffers	t_{pd} = 0.38ns (standard at 5.0V) level shifter, t_{pd} = 0.4ns (standard at 3.3V), t_{pd} = 1.3ns (standard at 2.0V)										
	Output Buffers	t_{pd} = 2.12ns (standard at 5.0V) level shifter, t_{pd} = 2.02ns (standard at 3.3V), t_{pd} = 3.9ns (standard at 2.0V) C_L=15pF										
I/O Level		CMOS, LVTTL, PCI, PECL, USB										
Input Mode		LVTTL, CMOS, Pull-up/Pull-down, Schmitt, Fail-safe*, Gated*										
Output Mode		Normal, Open drain, 3-state, Bi-directional, Fail-safe*, Gated*										

* Under development

The number of gates depend on the circuit, so use the values in this table only as an estimate.

Correspond to 5V interfaces, high speed and integration CMOS Gate Array

SLA40000 Series

Series Name		SLA40000 Series							
Features		• Super-high density (adopting 0.45µm silicon gate CMOS with 2- and 3-metal layers) • High-speed operation (operation delay of internal gate = 0.160ns at 3.3V, 2-input power NAND standard) • Internal gate = 3.3V, 3.0V and 2.5V (2.0V single), I/O buffer = 5.0, 3.3 and 3.0V (2.0V single) (built-in level shifter) • Low power consumption (0.80µW/MHz/BC when internal cell = 3.0V) • Output drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24 mA when PCI = 5.0V, I_{OL} = 0.1, 1, 2, 6, 12mA when PCI = 3.3V, I_{OL} = 0.05, 0.3, 0.6, 2, 4mA when 2.0V) • RAM, PLL, IrDA, and various function cells available • Low noise output cell, PCI I/F, USB I/F, LVDS, JTAG							
Master / Features	2-layer Metal	SLA4028	SLA4046	SLA4078	SLA4115	SLA4162	SLA4239	SLA4318	SLA4411
	3-layer Metal	SLA402T	SLA404T	SLA407T	SLA411T	SLA416T	SLA423T	SLA431T	SLA441T
Total BCs (Raw Gates)		28,260	46,864	78,600	115,388	162,864	239,468	318,308	411,257
Usable BCs	2-layer Metal	14,130	22,026	35,370	51,924	70,031	95,787	127,323	164,502
	3-layer Metal	24,868	39,834	62,880	86,541	122,148	167,627	222,815	287,879
Number of PADs (In Case of Micro Pitch)		116 128	144 164	184 212	216 256	256 304	308 368	352 424	400 480
Propagatin Delay	Internal Gates	t_{pd} = 0.16ns (standard at 3.3V)							
	Input Buffers	t_{pd} = 0.4ns (standard at 5.0V) level shifter, t_{pd} = 0.42ns (standard at 3.3V)							
	Output Buffers	t_{pd} = 1.99ns (standard at 5.0V) level shifter, t_{pd} = 1.89ns (standard at 3.3V) C_L = 50pF							
I/O Level		CMOS, TTL, PCI, USB, LVDS*							
Input Mode		LVTTL, TTL, CMOS, Pull-up/Pull-down, Schmitt							
Output Mode		Normal, Open drain, 3-state, Bi-directional							

3V or 5V single, high-integration and low power CMOS Gate Array

SLA35000 Series

Series Name		SLA35000 Series			
Features		• Super-high density (adopting 0.6µm silicon gate CMOS with 3-metal layer) • High-speed operation (operation delay of internal gate = 0.4ns at 3.3V, 2-input power NAND standard) • Selectable supply voltage: 5.0V, 3.3V, and 3.0V • Low power consumption (0.77µW/MHz/BC when internal cell = 3.0V) • Output drivability (I_{OL} = 1, 4, 8, 12 mA when 5.0V, I_{OL} = 0.5, 2, 4, 6mA when 3.3V) • On-chip RAM available			
Master		SLA3504	SLA3506	SLA3509	SLA3516
Total BCs (Raw Gates)		41,417	64,320	95,760	161,841
Usable BCs		26,921	38,592	52,668	80,920
Number of PADs		110	130	162	210
Propagatin Delay	Internal Gates	t_{pd} = 0.3ns (standard at 5.0V), t_{pd} = 0.4ns (standard at 3.3V)			
	Input Buffers	t_{pd} = 0.48ns (standard at 5.0V), t_{pd} = 0.63ns (standard at 3.3V)			
	Output Buffers	t_{pd} = 2.08ns (standard at 5.0V), t_{pd} = 2.86ns (standard at 3.3V) C_L = 50pF			
I/O Level		CMOS, TTL			
Input Mode		TTL, CMOS, Pull-up/Pull-down			
Output Mode		Normal, 3-state, Bi-directional			

The number of gates depend on the circuit, so use the values in this table only as an estimate.

Gate Array

3V and 5V, high speed CMOS Gate Array

SLA30000 Series

Series Name		SLA30000 Series							
Features		• Super-high density (adopting 0.6µm silicon gate CMOS with 2 and 3-metal layers) • High-speed operation (operation delay of internal gate = 0.25ns at 5.0V, 2-input power NAND standard) • Selectable supply voltage: 5.0V, 3.3V, 3.0V and built-in dual-power supplies level shift circuit • Output drivability (I_{OL} = 0.1, 1, 4, 8, 12, 24 mA when PCI = 5.0V, I_{OL} = 0.05, 0.5, 4, 6, 12 mA when PCI = 3.3V) • On-chip RAM available • I/O cells supporting the PCI Revision 2.0 and low noise output cells available							
Master / Features	2-layer Metal	SLA3018	SLA3030	SLA3042	SLA3055	SLA3075	SLA3109	SLA3125	SLA3216
	3-layer Metal	SLA301T	SLA303T	SLA304T	SLA305T	SLA307T	SLA310T	SLA312T	SLA321T
Total BCs (Raw Gates)	Dual Power Supply	18,544	30,846	42,262	55,341	75,450	109,080	125,836	216,216
	Single Power Supply	23,572	37,232	49,680	63,784	85,251	120,802	138,400	232,582
Usable BCs (Dual Power Supply)	2-layer Metal	9,272	15,423	19,863	26,010	33,952	49,086	54,109	86,486
	3-layer Metal	16,318	26,219	35,077	44,272	58,851	81,810	94,377	151,351
Usable BCs (Single Power Supply)	2-layer Metal	11,786	18,616	23,349	29,978	38,362	54,360	59,512	93,032
	3-layer Metal	20,743	31,647	41,234	51,027	66,495	90,601	103,800	162,807
Number of PADs		128	160	184	208	240	256	304	376
Propagatin Delay	Internal Gates	t_{pd} = 0.25ns (standard at 5.0V), t_{pd} = 0.33ns (standard at 3.3V)							
	Input Buffers	t_{pd} = 0.48ns (standard at 5.0V), t_{pd} = 0.63ns (standard at 3.3V)							
	Output Buffers	t_{pd} = 2.08ns (standard at 5.0V), t_{pd} = 2.86ns (standard at 3.3V) C_L = 50pF							
I/O Level		CMOS, TTL, PCI							
Input Mode		TTL, CMOS, Pull-up/Pull-down, schmitt, 3.0/3.3/5.0V Level interface (Level shifter)							
Output Mode		Normal, open drain, 3-state, Bi-directional, 3.0/3.3/5.0V Level interface (Level shifter)							

3V or 5V single, CMOS Gate Array for Small Gate Counts

SLA9000F Series

Series Name		SLA9000F Series							
Features		• Adopting 1.0µm silicon gate CMOS with 2-metal layer process • High-speed operation (operation delay of internal gate = 0.3ns at 5.0V, 2-input Power NAND standard) • Simplified level shifter cells available • Output drivability (I_{OL} = 0.1, 2, 6, 12, 24 mA when 5.0V, I_{OL} = 0.1, 2, 4, 8, 12mA when 3.3V) • On-chip RAM available • Low noise output cells available							
Master		SLA902F	SLA904F	SLA907F	SLA909F	SLA913F	SLA919F	SLA927F	SLA944F
Total BCs (Raw Gates)		2,784	4,392	7,872	9,540	13,144	19,350	27,234	44,070
Usable BCs		1,809	2,854	4,723	5,724	7,229	10,642	13,617	22,035
Number of PADs		80	100	128	144	160	184	208	256
Propagation Delay	Internal Gates	t_{pd} = 0.3ns (standard at 5.0V), t_{pd} = 0.43ns (standard at 3.3V)							
	Input Buffers	t_{pd} = 0.91ns (standard at 5.0V), t_{pd} = 1.08ns (standard at 3.3V)							
	Output Buffers	t_{pd} = 3.5ns (standard at 5.0V), t_{pd} = 4.2ns (standard at 3.3V) C_L = 50pF							
I/O Level		TTL, CMOS							
Input Mode		TTL, CMOS, Pull-up/Pull-down, Schmitt, 3.0/3.3/5.0V Level interface							
Output Mode		Normal, Open drain, 3-state, Bi-directional, 3.0/3.3/5.0V Level interface							

The number of gates depend on the circuit, so use the values in this table only as an estimate.

Standard Cell

A standard cell is a semi-custom IC composed of the optimum designed internal logic cells, ROM, RAM, CPU and analog circuit on one chip. Compared to gate array, the standard cell can be designed more freely, and with higher functions and integration. Therefore, as the optimum system LSI can be produced, it is a very useful for product miniaturization, low power consumption.

SCB60000 Series*

Series Name	SCB60000 Series
Features	• Super-high Iintegration (Adopting 0.25 µm silicon gate CMOS with 3-, 4- and 5-metal layers) • High speed operation (Operation delay of internal gate 109ps at 2.5V, 2 input NAND standard) • Power voltage (Internal: 2.0V, 2.5V, I/O : 2.0V, 2.5V, 3.3V) • Low power consumption (Internal Cells: 0.07µm/MHz/BC at 2.0V) • Output drivability (I_{OL} = 0.1, 1, 3, 6, 12, 24mA at 2.5V and 3.3V, I_{OL} = 0.05, 0.3, 1, 2, 4, 8mA at 2.0V)
Macro Cells	• RAM Maximum size: 2Mbits, ROM Maximum size: 4Mbits • Planning of A/D, D/A many functional cells line up
Package	・Planning to corresponding to QFP, BGA and CSP

* Under development

Comparing wigh 0.35µm process products

	Gate Array	Embedded Array	Standard Cell
Integration Rate (%)	100	73	40
Power consumption (µW/MHz/FF)	7.65	4.51	2.22

■ When comparing these products with the SLA50000H series produced at EPSON, the integration rate is two fifths that of the SLA 50000H series and the power consumption is one third.

SCB50000 Series

Series Name	SCB50000 Series
Features	• Super-high Iintegration (Adopting 0.35 µm silicon gate CMOS with 2-, 3- and 4-metal layers) • High speed operation (Propagation delay 0.14ns at 3.3V, 2 input NAND standard) • Power voltage selectable : Single voltage (2.0V, 2.5V, 3.3V) Dual voltage (I/O: 5.0V / Internal: 3.3V, I/O 3.3V / Internal 2.5V, I/O 3.3V / Internal 2.0V) • Low power consumption (Internal Cells: 0.25µm/MHz/BC at 2.5V) • Output drivability (I_{OL} = 0.1, 1, 3, 8, 24mA at 5.0V, I_{OL} = 0.1, 1, 2, 6, 12mA at 3.3V I_{OL} = 0.05, 0.3, 0.6, 2, 4mA at 2.0V)
Macro Cells	• RAM Maximum size: 1Mbits, ROM Maximum size: 2Mbits • 8 bit A/D, 10 bit D/A*, PLL and various functional cells available • Mount 32 bits RISC CPU , ARM7TDMI
Package	• Line up QFP48pins to 304 pins, BGA and CSP
Test Design	• Using STPG for scan setting and auto-generating the test patterns of highly detecting faults

* Under development

Embedded Array

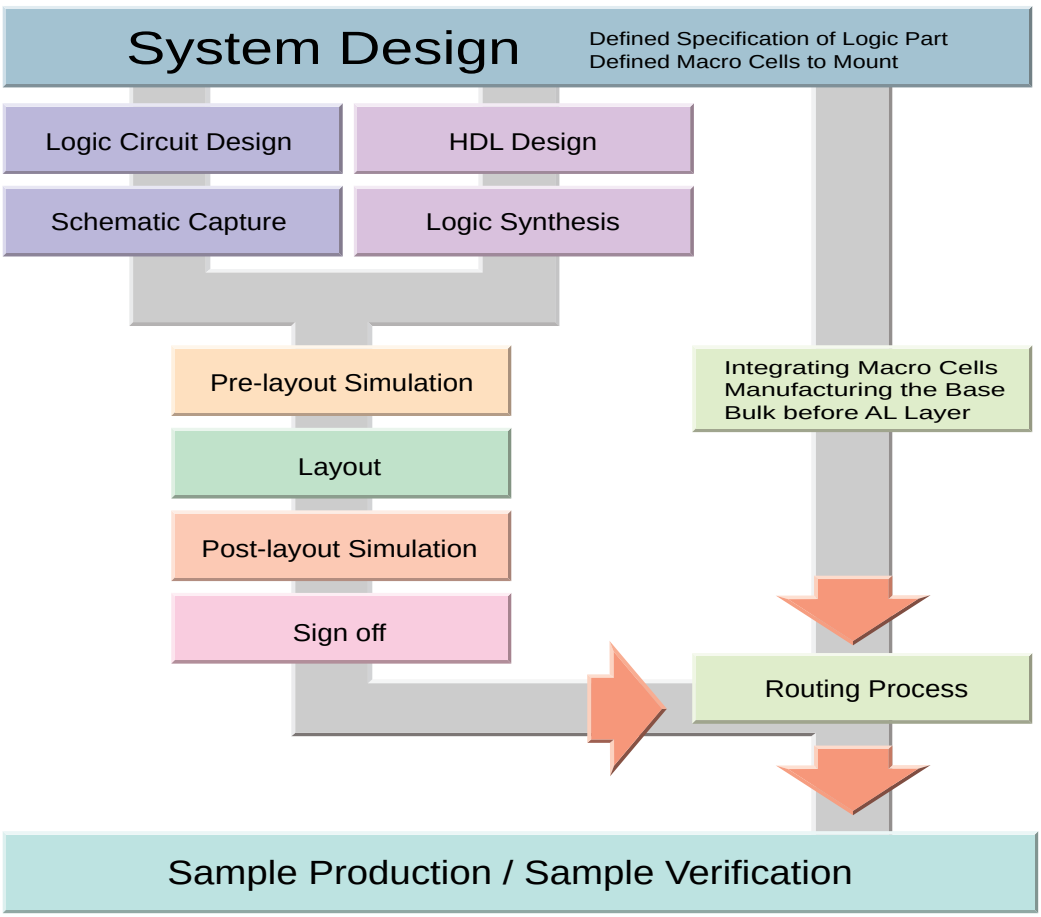
This product combines the gate array methodology with hard macros and standard cell. The idea is to fix the specifications of the hard macros before the finalisation of the design, for example : to fix the memory capacity, the type of 32 bits RISC processor, the specifications of one ADC, etc. Moreover the maximum number of gates is already fix (but no programmed) in order to reserve area in the die also for the user logic part. Then, meanwhile the design is finished, the bulk specified is started to be fabricated, processing all the mask steps, except the metal layers. Once the designer has finished with all the design steps, the prototype production starts with the advantage that only the metal layers should be processed like in the case of a pure Gate Array. This product has two main advantages from the development point of view :

- The turn around times for prototype production is the same as for the case of Gate Array.
- The costs of re-design for the user logic part are the same than the case of Gate Array.

These two advantages offer a big flexibility on the ASIC product allowing also make re-definition of the product with very low costs of development.

Embedded Array Design

The embedded array is designed as follows:
First, the number of gates and hard macro cell are decided. Then, the base bulk are manufactured. Here, the base bulk has hard macro cells and sea of gates, and is manufactured before the Al layer process. Furthermore, serial processing like normal gate arrays from the circuit design of the logic part to post-simulation is performed. Then, after the sign off (completing the post-simulation), the Al layer process is started and the sample product is delivered within the same TAT as the gate array.
If the logic part circuit or the ROM data need required to be changed, it only requires the same development cost and TAT as the gate array.

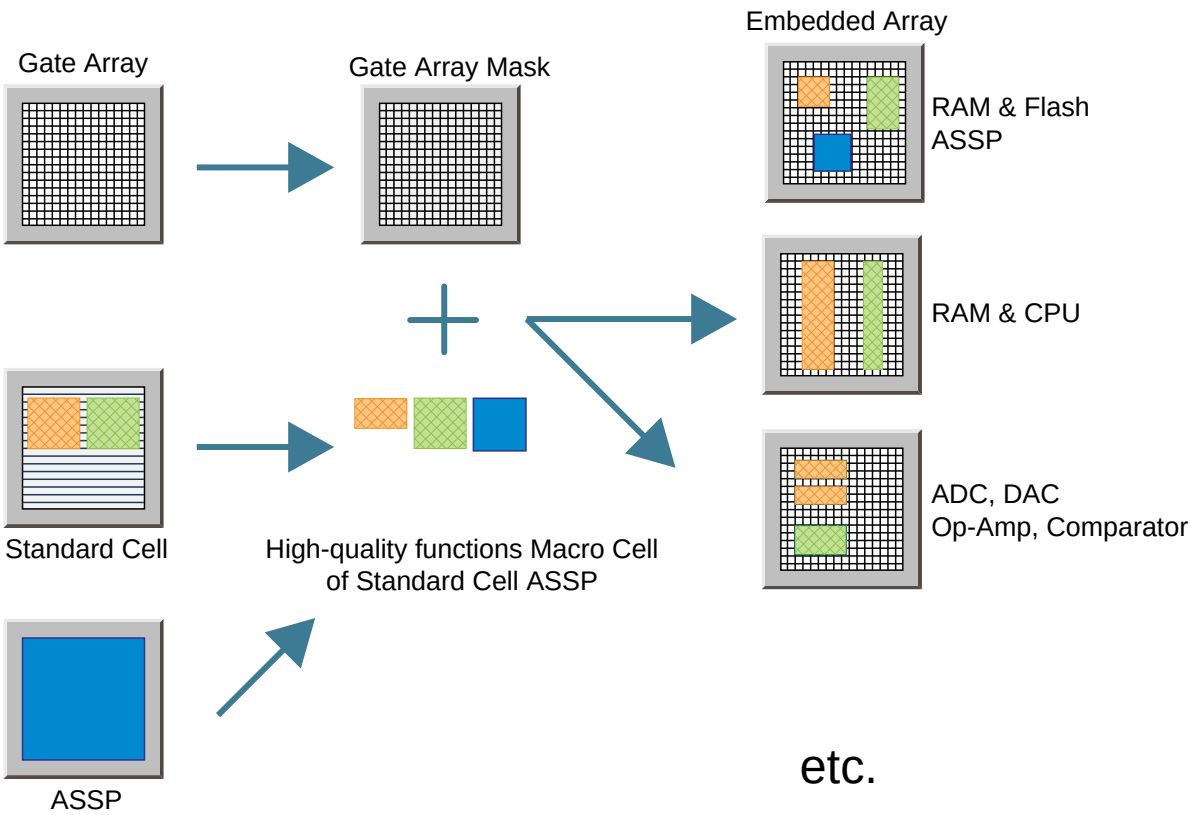


Embedded Array Procut Line-up

Series Name	SSL35000 Series	SSL40000 Series	SSL50000 Series	SSL60000 Series
Process	0.6µm, 3/4LM	0.45µm, 3/4LM	0.35µm, 3/4/5LM	0.25µm, 3/4/5LM
Total BCs (Row Gates)	to 500K	to 700K	to 1.4M	to 2.5M
Integration Rate	5K BC/mm^2	8K BC/mm^2	15K BC/mm^2	27K BC/mm^2
Propagation Delay (Internal Cell)	330ps / 2NAND, 3.3V	160ps / 2NAND, 3.3V	140ps / 2NAND, 3.3V	107ps / 2NAND, 2.5V
Power Consumption	0.77µW/MHz/BC, 3.0V	0.56µm/MHz/BC, 3.3V	0.39µW/MHz/BC, 3.3V	0.17µW/MHz/BC, 2.5V
Core Power Voltage	2.7 to 5.5V	2.7 to 3.6V	1.8 to 3.6V	1.8 to 2.7V
I/O Power Voltage	2.7 to 5.5V		1.8 to 5.5V	1.8 to 3.6V
Macro Cell	We supply many type of macro cells. Please refer to the macro cell line-up.			

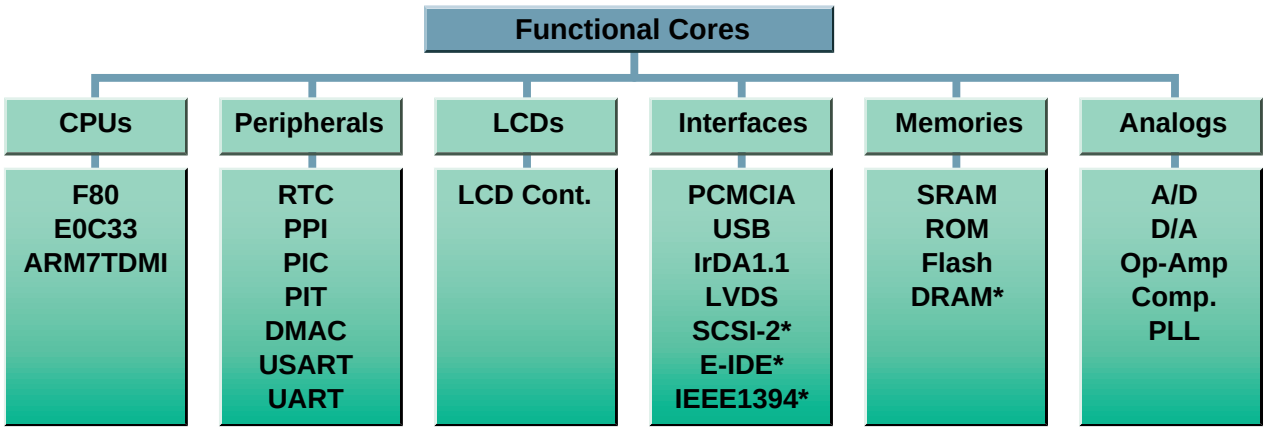
EPSON can supply many types of macro cells that are developed quickly, minimizing the cost and with large scale and high quality functions. A system on chip, for example, integrating analog cells, memory cells, all types of interface macro cells, CPU cores, and peripheral functional cells, can be easily developed. Many types of EPSON original ASSP macro cells can also be supplied.

Imaging Figure of the Embedded Array



Macro Cell

IP Tree



* Under development

8-bit CPU

EPSON's F80 is characterized by low power consumption. It has built-in sleep circuit to reduce power consumption at HALT mode.

Model	Bus Width	Process Cycle	Sleep Function at HALT
F80R	Internal 8bit	4CLK/1M Cycle	Yes
F80E	Internal 16bit	2CLK/1M Cycle	Yes

32-bit RISC CPU

Model	Processing Speed	Power Consumption / External Bus Width	Applications
E0C33000	50MIPS/50MHz/3.3V	180mW(general product)/50MHz/8,16bit	Printer, Scanner, PDA, Voice dictionary, DSC
ARM7TDMI	30MIPS/40MHz/3.3V	50mW(CPU core)/40MHz/8,16,32bit	Porable telephone, PHS, DSC

*Under development

Memory

Memory	V_{DD} (V)	Memory Size (Max)	Frequency (max)
Syncronous 1port RAM	1.8 to 3.6	1 Mbit	90 MHz
Syncronous 2port RAM	1.8 to 3.6	256 Kbit	90 MHz
Syncronous ROM	1.8 to 3.6	2 Mbit	76 MHz
FIFO	1.8 to 3.6	256 Kbit	76 MHz
Flash	2.7 to 3.6	4 Mbit	20 MHz
DRAM*(SDRAM)	3.0 to 3.6	16 Mbit	60 MHz

*Under development

Peripheral

Peripheral		Function	Features
DMAC	(F37)	DMAC 8-bit high speed data transmission	Possible to transmit DMA in the memory area
RTC	(F42)	Clock functions	Built-in time (second, minute, and hour) counter and calendar (day, week, month, and year) counter
USART	(F51)	Synchronous / asynchronous data communication	Character length: 5 to 8 bits, baud rate: x1, x16, x64
PIT	(F54)	Programmable general timer	Possible to assign freely 6 kinds of counter modes
PPI	(F55)	I / O Port functions	Possible to select a function for I / O port (24 bits) by programming
PIC	(F59)	Interrupt control	Possible to control a maximum of 64 levels by using the cascade connection
UART	(F65)	Asynchronous data communication with FIFO	Transmitting and receiving data derated the interrupt answering process, built-in independent 16B FIFO

■ We supply other lined up macro cells. Please contact EPSON Sales Division for details.

LCD Controller

Models	Features	Applicable Panels
F351 (SED 1351)	2 and 4 gray scale display, VRAM capacity: 64KB	Monochrome 4 gray scale, 640 x 400 STN panel
F352 (SED 1352)	2 to 16 gray scale display VRAM capacity : 128KB	Monochrome 16 gray scale, 640 x 240 (at 16 gray scale)
F354 (SED 1354)*	Applicable to monochrome, color (STN and TFT) and CRT, the display LCDC to operate on WinCE recognized by Microsoft corporation	STN (4K colors), TFT (64K colors), Maximum resolution 800 x 600
F375 (SED 1375)*	Applicable to monochrome and color (STN and TFT), low power consumption by built-in SRAM	STN, TFT (256 colors)

*Under development

Interface

Models	Features
LVDS	Clock frequency: 30 to 83MHz at 3.3V, 30 to 70MHz at 2.5V, prepared for an evaluation sample.
USB (ver1.0)	Data transmission speed: support full speed 12Mbit/sec, prepared for an evaluation kit.
IrDA (ver1.1)	Data transmission speed: support to FIR (4Mbps) and SIR (2.4 to 115.5Kbps) and prepared for an evaluation kit.
PCMCIA	Support to ATA-HDD interface, corresponding to 3.3V and 5.0V powers.
IEEE1394*	Transmission rate: support to 100, 200 and 400 MHz, applicable to PC peripheral (SBP-2).

*Under development

PLL

Model	Target Frequency (Hz)		Power Voltage (V)	Power Voltage (V)	At Starting Oscillation	Available Series
Phase Adjustment	25M to 50M		2.7 to 3.6	± 700	40 (µsec)	SLA 40000
	50M to 80M		2.7 to 3.6	± 700	12.5 (µsec)	SLA 40000
Model	**Input Frequency (Hz)**	**Output Frequency (Hz)**	**Power Voltage (V)**	**Jitter (PS)**	**Stable Time**	**Available Series**
Multiply	40M	80M	3.0 to 3.6	± 500	15 µsec	SLA 40000
	30M to 50M	60M to 100M	2.7 to 3.6	± 400	1 msec	SLA 40000
	32K to 150M*	10M to 150M	2.7 to 3.6	± 500	10 msec	SLA 50000H
	32K*	20M to 135M	3.0 to 3.6	± 200	100 msec	SSL 50000
	5M to 40M*	20M to 135M	3.0 to 3.6	± 150	100 µsec	SSL 50000

*Under development

A / D

Resolution (bit)	Precision (LSB)	Power Voltage (V)	Input Voltage (V)	Sampling Frequency (Hz)
8	± 2	2.7 to 3.3	0.74 to 0.9	310K (max)
8*	± 1	3.3	0 to 3.0	30M (typ)
9	± 1	2.85 to 3.00	0 to 3.0	2.0M (max)
10	± 2	2.7 to 3.3	1.8 to 2.2	2.0M (typ)

* Under development

D / A

Resolution (bit)	Precision (LSB)	Power Voltage (V)	Output Voltage (V)	Settling Time
8	± 1	2.7 to 3.3	0.2 to 2.7(V)	50 (µsec)
9	± 1	2.7 to 3.3	0.2 to 2.7(V)	50 (µsec)
10	± 2	4.75 to 5.25	2.94 to 3.06 (mA)	100 (nsec)
10*	± 2	2.7 to 3.3	10 to 30 (mA)	7.4 (nsec)

* Under development

Macro Cell

Macro Cell LIne UP

IP Macro Cell Line Up

	Standard Cells		Embedded Arrays			
Technology	SCB60000*	SCB50000	SSL60000*	SSL50000	SSL40000	SSL35000
Design rule	0.25µmCMOS	0.35µmCMOS	0.25µmCMOS	0.35µmCMOS	0.45µmCMOS	0.60µmCMOS
Layer	3/4/5	3/4	3/4/5	3/4	3	3
CPU Core						
8bit-ALU, 1Inst/4Clock [F80R]	○	●	○	●	●	●
16bit-ALU, 1Inst/2Clock [F80E]	○	●	○	●	●	●
32bit RISC Processor [E0C33000]	–	–	○	●	–	–
32bit RISC Processor [ARM7TDMI]	○	●	○	●	–	–
Peripheral Macro						
USART (8251) [F51]	○	●	○	●	–	●
PIT (8254) [F54]	○	●	○	●	●	●
PPI (8255) [F55]	○	●	○	●	●	●
PIC (8259) [F59]	○	●	○	●	●	●
DMAC (8237) [F37]	○	–	○	–	●	–
UART (16550) [F65]	○	●	○	●	●	●
RTC (SMC5242) [F42]	○	●	○	●	●	●
Graphics Controller						
LCD Controller (SED1351) [F35]	○	○	○	○	○	○
LCD Controller (SED1352) [F352]	○	○	○	●	○	●
LCD Controller (SED1354) [F354]	○	○	○	○	–	–
Interface Controller						
USB Function Controller [USBFC]	○	●	○	●	●	–
IrDA Controller (Ver. 1.1) [FICC]	○	●	○	●	●	–
Low Voltage Differential Signals [LVDS]	○	◎	○	◎	●	–
PCMCIA Controller (SPC8282)	○	–	○	○	–	–
I2C BUS Controller	○	–	○	○	–	–
IEEE1394 Controller	○	◎	○	◎	–	–
Special I/O Macro						
PCI Buffer	○	●	○	●	●	●
USB Buffer (Driver/Receiver for Full-Speed)	○	●	○	●	●	–
LVDS Buffer	○	◎	○	◎	●	–
Fail-Safe I/O	○	●	○	●	–	–
Gated I/O	○	●	○	●	–	–
Memory Macros						
Asynchronous 1Port SRAM	○	●	○	●	●	●
Asynchronous 2Port SRAM	○	●	○	●	●	●
Synchronous 1Port SRAM	○	●	○	●	●	●
Synchronous 2Port SRAM	○	●	○	●	–	●
Synchronous Dual Port SRAM	○	●	○	●	–	–
Asynchronous FIFO	○	●	○	●	–	●
Synchronous FIFO	○	●	○	●	–	●
Synchronous Mask ROM	○	●	○	●	●	●
Flash Memory	○	●	○	●	–	●
Synchronous DRAM	○	◎	○	◎	–	–
Analog Macros						
AD Converter	○	◎	○	●	–	●
DA Converter	○	◎	○	●	–	●
OP-Amp	○	○	○	○	–	○
Analog-Switch	○	○	○	○	–	○
Comparator	○	○	○	○	–	○
PLL						
Degital PLL	–	–	–	–	●	●
Analog PLL	○	◎	○	◎	–	–
Others						
Multiplier	○	○	○	●	–	–
SCAN Cell	○	●	○	●	●	–
JTAG	○	○	○	●	●	○

● : Available products
◎ : Under development
○ : Under planning

IP Macro Cell Line Up

	Gate Arrays					
Technology	SLA60000	SLA50000H	SLA40000	SLA35000	SLA30000	SLA9000F
Design rule	0.25µmCMOS	0.35µmCMOS	0.45µmCMOS	0.6µmCMOS	0.6µmCMOS	1.0µmCMOS
Layer	3/4/5	2/3/4	2/3	3	2/3	2
CPU Core						
8bit-ALU, 1Inst/4Clock [F80R]	○	●	●	●	●	●
16bit-ALU, 1Inst/2Clock [F80E]	○	●	●	●	●	–
32bit RISC Processor [E0C33000]	–	–	–	–	–	–
32bit RISC Processor [ARM7TDMI]	–	–	–	–	–	–
Peripheral Macro						
USART (8251) [F51]	○	●	●	●	●	●
PIT (8254) [F54]	○	●	●	●	●	–
PPI (8255) [F55]	○	●	●	●	●	●
PIC (8259) [F59]	○	●	●	●	●	–
DMAC (8237) [F37]	○	●	●	–	●	–
UART (16550) [F65]	○	●	●	●	●	●
RTC (SMC5242) [F42]	○	●	●	●	●	●
Graphics Controller						
LCD Controller (SED1351) [F35]	○	●	●	○	●	●
LCD Controller (SED1352) [F352]	○	●	●	●	●	–
LCD Controller (SED1354) [F354]	○	○	–	–	–	–
Interface Controller						
USB Function Controller [USBFC]	○	◎	●	–	–	–
IrDA Controller (Ver. 1.1) [FICC]	○	●	●	–	○	–
Low Voltage Differential Signals [LVDS]	○	–	●	–	–	–
PCMCIA Controller (SPC8282)	○	○	●	–	–	–
I2C BUS Controller	○	○	–	–	–	–
IEEE1394 Controller	–	–	–	–	–	–
Special I/O Macro						
PCI Buffer	○	●	●	–	●	–
USB Buffer (Driver/Receiver for Full-Speed)	○	●	●	–	–	–
LVDS Buffer	○	–	●	–	–	–
Fail-Safe I/O	○	●	–	–	–	–
Gated I/O	○	●	–	–	–	–
Memory Macros						
Asynchronous 1Port SRAM	○	●	●	●	●	●
Asynchronous 2Port SRAM	○	●	●	●	●	●
Synchronous 1Port SRAM	–	–	–	–	–	–
Synchronous 2Port SRAM	–	–	–	–	–	–
Synchronous Dual Port SRAM	–	–	–	–	–	–
Asynchronous FIFO	–	–	●	–	–	–
Synchronous FIFO	–	–	–	–	–	–
Synchronous Mask ROM	○	○	○	○	○	○
Flash Memory	–	–	–	–	–	–
Synchronous DRAM	–	–	–	–	–	–
Analog Macros						
AD Converter	–	–	–	–	–	–
DA Converter	–	–	–	–	–	–
OP-Amp	–	–	–	–	–	–
Analog-Switch	–	–	–	–	–	–
Comparator	–	–	–	–	–	–
PLL						
Degital PLL	–	◎	●	●	–	–
Analog PLL	○	○	–	–	–	–
Others						
Multiplier	○	●	–	–	–	–
SCAN Cell	●	●	●	–	●	●
JTAG	○	●	●	○	●	●

● : Available products
◎ : Under development
○ : Under planning

Macro Cell

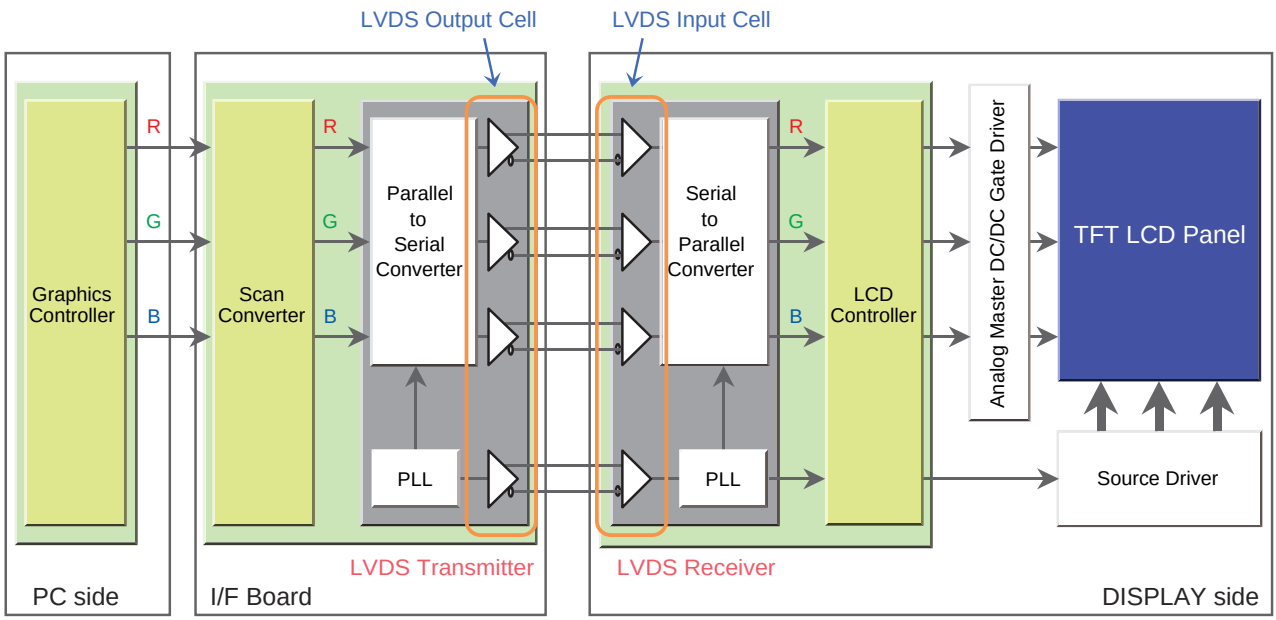
EPSON Unique ①

LVDS receiver/Transmitter

LVDS (Low Voltage Differential Signaling) is a method in which a low amplitude differential signal is transmitted at high speed. A feature of the LVDS is its strong countermeasure to noise, because data are transmitted or received by low amplitude signals. It is therefore widely used on LCD panel peripherals and in other fields. EPSON supplies the LVDS for an ASIC solution.

Example of LVDS Macro Cell Usage

Ultra-low Power Consumption



Features

1. Application products: 0.35µm CMOS embedded array (SSL50000 series)
2. Ultra-low power consumption 50mW/65MHz at 2.5V
3. Wide clock frequency band: 30MHz to 83MHz at 3.3V, 30MHz to 70MHz at 2.5V
4. Wide power source band: 3.3V±0.3V, 2.5V±0.25V
5. Applicable to SVGA, XGA, SXGA, UXGA
6. Built-in external parts (low pass filter)
7. Supports for various special functional cells (variable output buffer, seven-phase clock output functions and so on)

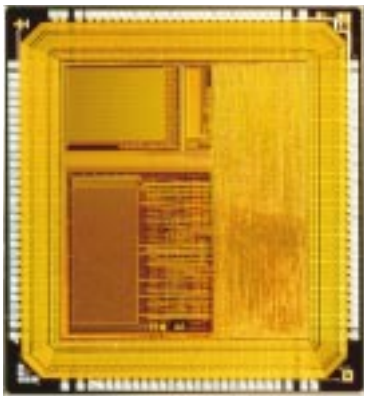
❍ The LVDS (built-in a receiver) ASIC has already been used at SLA40000 gate arrays many times and has satisfied many customers. Please contact EPSON Sales Division for details.

EPSON Unique ②

Embedded flash

The embedded flash is a memory macro designed for our ASIC. It is composed of optional sizes, as shown in the following table. If it is mixed with the CPU and other macro cells, a custom flash microcomputer (user's desired) can be created. Furthermore, as the high voltage generating circuit is built in the internal macro cell, the system can be configured to run on a 3.3 V single power source.

Example of Embedded Array Product Built-in Flash Memory



Embedded flash functions Table

		SSL50000 Series	SSL60000 Series*
Technology		0.35µm CMOS	0.25µm CMOS
Operation Voltage		2.7 to 3.6V	2.3 to 2.7V
Erase / Program Interface		White Pulse Input, (Command I/F)	White Pulse Input, Command I/F
Memory Size		64K to 2M bit, (256K to 4M bit)	64K to 4M bit
I/O		8, 16 bit	8, 16 bit
Sector Size		1K byte/Sector, (4K byte/sector)	1K, 4K byte/Sector
Chip Erase Time	**Typ.**	100 ms	100 ms
Sector Erase Time	**Typ.**	20 ms	20 ms
Byte Erase Time	**Typ.**	15 µs	15 µs
Read Access Time	**Max.**	50 ns	50 ns
Operating Current	**Max.**	15 mA	10 mA
Standby Current	**Max.**	10 µA	10 µA
Endurance Time	**Min.**	10,000 cycle	
Data Retention	**Min.**	10 years	
Temperature Range		0 to 70 °C	

* Under development

Macro Cell

EPSON Unique ③

32-bit RISC CPU: Product outline of E0C33

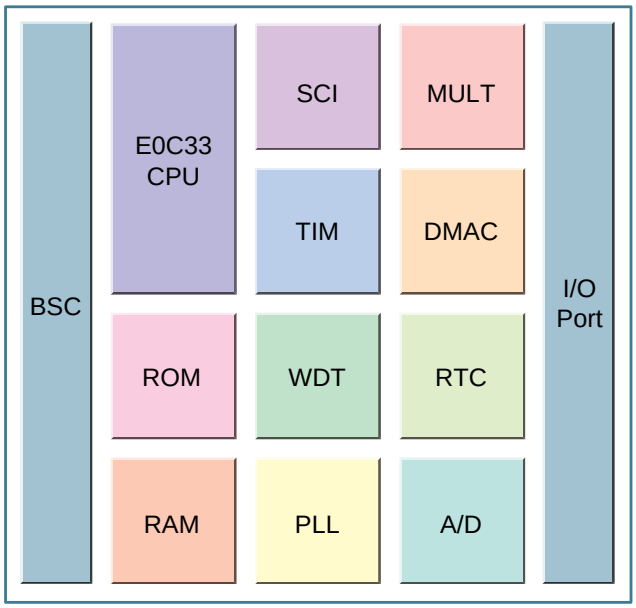
1. Features
   - High-speed operation, low power consumption
     50MHz (50MIPS) at 3.3V, 180mW (typ.) / 50MHz
   - A wealth of peripheral functions
     High-speed sum of products operator, Real time clock
     High-speed DMA, Each timer, Serial interface, Analog and so on.

2. Application
   - PC peripheral equipment (Printer, Scanner)
   - Voice dictionary, Voice memorandum, Amusement instrument and so on.
   - PDA, Portable telephone, PHS, DSC

3. Middleware
   - Sound compressing and expanding manufacture (VOX33)
   - JPEG Image compressing and expanding (JPEG33)*
   - Voice recognition (VRE33)*
   - Handwritten character recognition (HRE33)*

* Under development

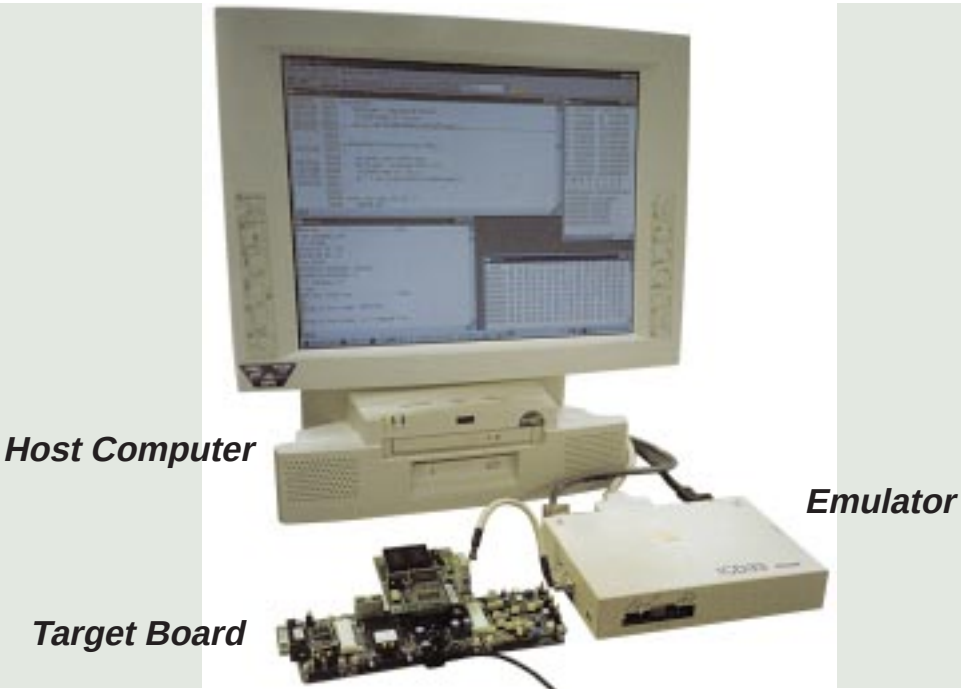
E0C33 Block Diagram



✵ As peripheral macro cells corresponding to a customer's request can be selected, and the most suitable system for the customer can be developed.

Software development circumstance of ASIC built-in microcomputer

When the software of an ASIC built-in a microcomputer is developed, the software debug condition can be constructed by the emulator for a standard microcomputer and each board. Therefore, even though there is no accomplishment product, the software can be developed, and the total development period can be shortened.

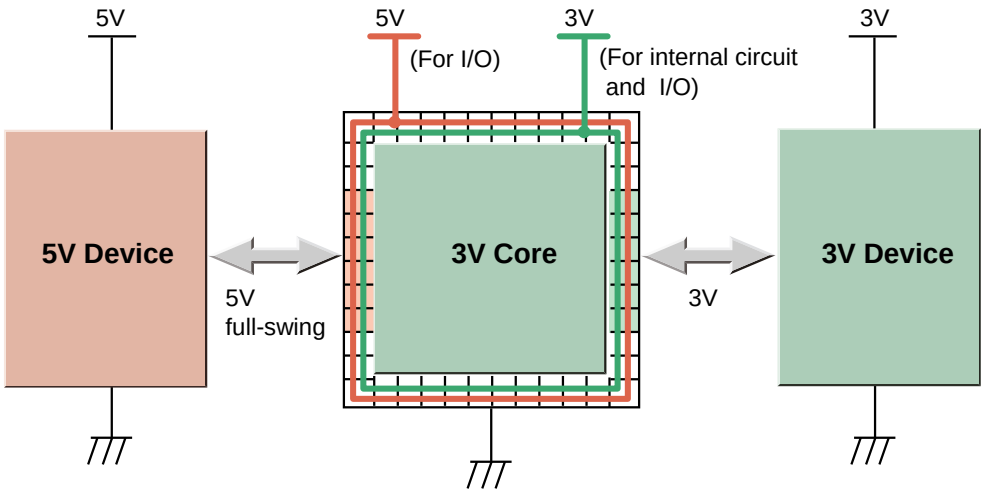


A low system voltage is needed to develop the low power consumption of the circuit. However, as all circuit components cannot be operated at low voltage, the circuit has multiple power systems. In fact, two power and pin systems (for example, 5V and 3V) are built into most portable equipment used around the world.

For Dual Power Supply System (5V and 3V)

Level Shifter

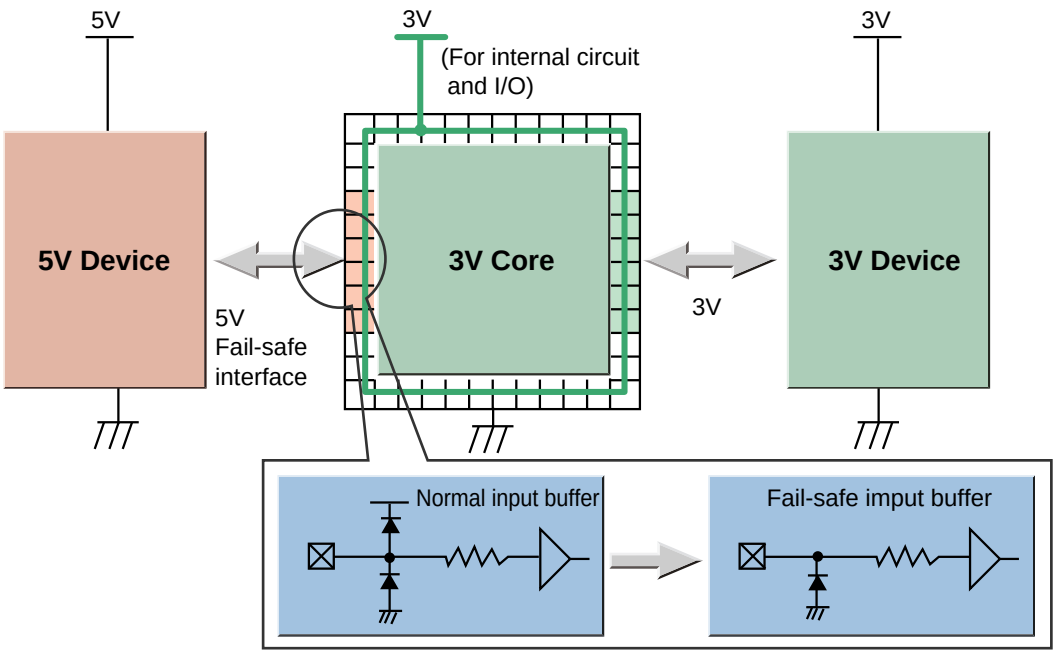
As ASIC products are mostly used to connect with other ICs, they need dual level signals of 5V and 3V. Therefore, SLA50000H, SLA40000 and SLA30000 series can interface with 5V or 3V signals of each I / O buffer, which is supplied dual voltages (5V and 3V). The dual voltages are most suitable for high speed signal processing and the required high driving current.



For Single Power Supply System (3V)

Fail-safe I / O Buffer

Even though dual power voltage cannot be supplied to ICs because of system restrictions, IC operated at 3V can interface with ICs operated at 5V by using input buffer which have to cut the forward direction diode to VDD and correspond to fail-safe for output.



Package

Electronic products are being developed with more and more high-quality functions, of smaller size, and of lighter weight. As a result, packaging technology is becoming increasingly important because ASIC products must be assembled very densely and be capable of high integration and high speed.
EPSON's ASIC products are designed in a variety of packages to meet customer needs, for example, many pins to few pins, smaller size, thin type, and so on.

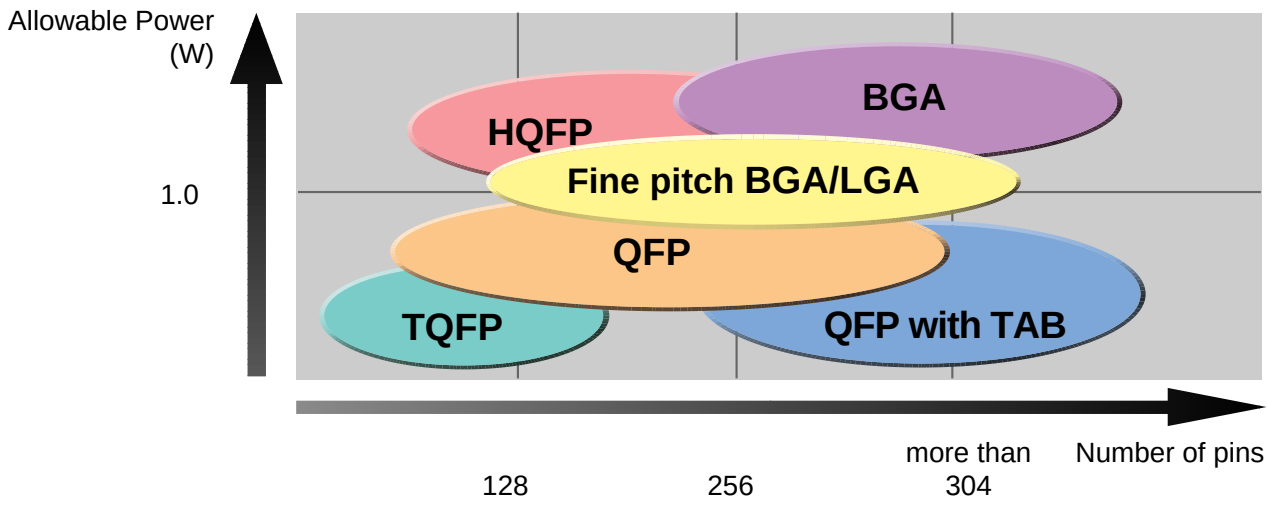
Number of Package Line-ups

User Needs	Package Line-up
Number of pins	Number of Package • QFP with TAB • QFP 10-304Pin • BGA 225 to 600*Pin
Small size/ Thin type	Smaller Package • Fine pitch BGA/LGA • QFP12-48Pin (from 7×7×1.4mm) Thin Type Package • TQFP (thickness=1.0mm)
Low Thermal Resistance	Low Thermal Resistance Package • HQFP, H2QFP, H3QFP • Copper lead flame for High Radiation

* Under development

Package Line up Covered to Allowable Power Source and Number of Pins

EPSON's ASIC products designed for the maximum power and the number of pins for each package type.



Many types of ASIC packages are available, for example, small and thin types, a few to many pins, and so on. We also supply packages required by customers, for example, low thermal resistance packages and BGAs as follows:

QFP, TQFP

Number of pins	Body Size (mm)	Type	Lead Pitch (mm)
44	10×10×1.45	QFP4	0.8
	10×10×1.4	QFP13	0.8
	14×14×2.7	QFP6	1.0
46	14×20×2.7	QFP5	1.0
48	7×7×1.4	QFP12	0.5
	7×7×1.0	TQFP12	0.5
	14×14×2.15	QFP27	0.8
	14×20×2.7	QFP5	0.8
52	14×14×2.7	QFP6	1.0
60	14×14×2.7	QFP6	0.8
	14×20×2.7	QFP5	1.0
64	10×10×1.4	QFP13	0.5
	10×10×1.0	TQFP13	0.5
	14×14×1.4	QFP15	0.8
	14×14×2.7	QFP6	0.8
	14×20×2.7	QFP5	1.0
80	12×12×1.4	QFP14	0.5
	12×12×1.0	TQFP14	0.5
	14×20×2.7	QFP5	0.8
100	12×12×1.0	TQFP14	0.4
	14×14×1.0	TQFP15	0.5
	14×14×1.4	QFP15	0.5
	14×20×2.7	QFP5	0.65
120	14×14×1.4	QFP15	0.4
	28×28×3.35	QFP8	0.8

Number of pins	Body Size (mm)	Type	Lead Pitch (mm)
128	14×14×1.0	TQFP15	0.4
	14×14×1.4	QFP15	0.4
	14×20×2.7	QFP5	0.5
	14×20×1.4	QFP26	0.5
	28×28×3.35	QFP8	0.8
144	16×16×1.0	TQFP24	0.4
	20×20×1.4	QFP20	0.5
	20×20×2.7	QFP17	0.5
	28×28×3.35	QFP8	0.65
160	20×20×2.7	QFP17	0.4
	28×28×1.4	QFP22	0.65
	28×28×3.35	QFP8	0.65
176	24×24×1.4	QFP21	0.5
	24×24×2.7	QFP18	0.5
184	20×20×1.4	QFP20	0.4
	20×20×2.7	QFP17	0.4
	32×32×3.4	QFP23	0.65
208	28×28×1.4	QFP22	0.5
	28×28×3.35	QFP8	0.5
216	24×24×1.4	QFP21	0.4
240	32×32×3.4	QFP23	0.5
256	28×28×1.4	QFP22	0.4
	28×28×3.35	QFP8	0.4
304	40×40×3.8	QFP10	0.5

HQFP

Number of pins	Body Size (mm)	Type	Lead Pitch (mm)
48	7×7×1.4	H3QFP12	0.5
64	10×10×1.4	H3QFP13	0.5
80	12×12×1.4	H3QFP14	0.5
100	14×20×2.7	H2QFP5	0.65
	14×14×1.4	HQFP15	0.5
128	14×14×1.4	H3QFP15	0.4
	14×20×2.7	HQFP5	0.5
	14×20×2.7	H2QFP5	0.5
	28×28×3.35	HQFP8	0.8

Number of pins	Body Size (mm)	Type	Lead Pitch (mm)
144	20×20×1.4	HQFP20	0.5
	28×28×3.5	HQFP8	0.65
160	28×28×3.35	HQFP8	0.65
	28×28×3.35	H2QFP8	0.65
208	28×28×3.35	HQFP8	0.5
	28×28×3.35	H2QFP8	0.5
240	32×32×3.4	H2QFP23	0.5
304	40×40×3.8	QFP10	0.5

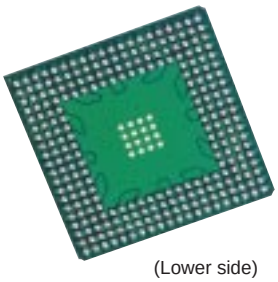
■ We also produce other packages - DIP, PLCC, SOP that are not listed here. Please contact EPSON Sales Division for detail.

BGA (Ball Grid Array)

Plastic BGA (PBGA)

Ball pitch 1.27mm

(Upper side)



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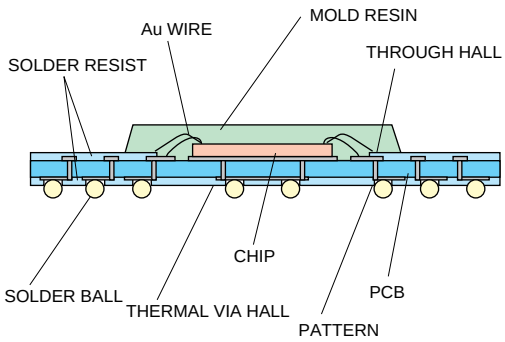
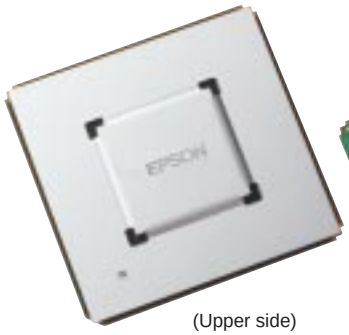


Low Thermal Resistance BGA (T-BGA)

Ball pitch 1.27mm



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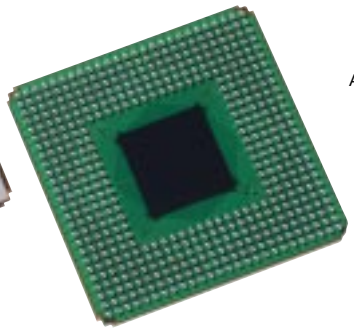

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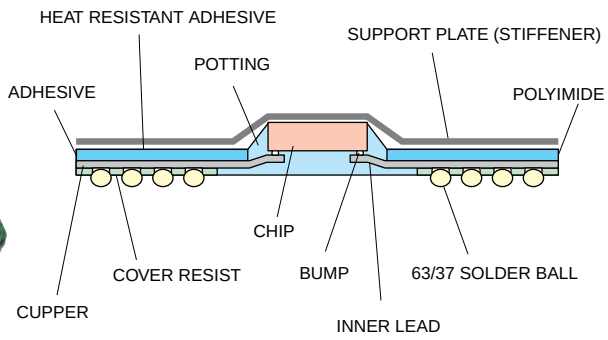
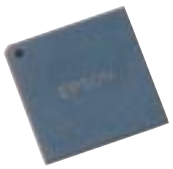


BGA

Type	Body Size (mm)	Pitch (mm)	Type	Body Size (mm)	Pitch (mm)
PBGA225	27×27×2.13	1.27	**T-BGA352**	35×35×2.13	1.27
PBGA256	27×27×2.13	1.27	**T-BGA420**	35×35×2.13	1.27
PBGA388	35×35×2.13	1.27	**T-BGA480**	35×35×2.13	1.27

Small type BGA (PFBGA)

Ball pitch 0.8mm



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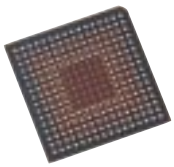

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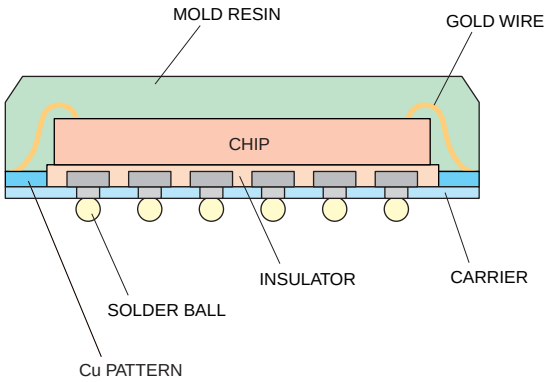
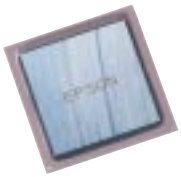


LGA (Land Grid Array)

CFLGA

Land pitch 0.8mm



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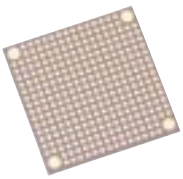

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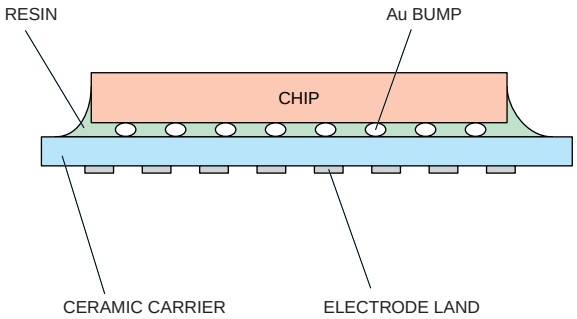


BGA

Type	Body Size (mm)	Pitch (mm)
PFBGA81	8×8×1.2	0.8
PFBGA121	10×10×1.2	0.8
PFBGA180	12×12×1.2	0.8
PFBGA220	14×14×1.2	0.8
PFBGA280	16×16×1.2	0.8

LGA

Type	Body Size (mm)	Pitch (mm)
CFLGA64	7×7×1.0	0.8
CFLGA104	9×9×1.0	0.8
CFLGA152	11×11×1.0	0.8
CFLGA239	13×13×1.0	0.8
CFLGA307	15×15×1.0	0.8
CFLGA424	17×17×1.0	0.8

■ When using BGAs or LGAs, PKG investigation will be necessary.

Package

The LSI chip heats up according to the power consumption within the LSI. The temperature of the LSI chip when it is mounted in a package can be calculated from the ambient temperature Ta, the thermal resistance ($\theta_{j\text{-}a}$) of the package, and the power consumption P_D.

The chip temperature (Tj) = Ta + ($P_D \times \theta_{j\text{-}a}$) (°C)

In normal use, the chip temperature (Tj) should be less than about 125°C.
The thermal resistances will change substantially depending on the mounting of the packages on the circuit board and depending on whether or not there is forced air cooling.

Thermal Resistance of Various Packages (Without Air Circulation)

Lead Frame Resin : 42ALLOY

ALLOY42

Package Type	Number of pins	0m/sec	1m/sec	2m/sec	3m/sec
		θj-a	θj-a	θj-a	θj-a
QFP4	44	160(°C/W)	–	–	–
QFP5	100	110	75	60	55
QFP5	128	110	75	60	55
QFP6	44	110	75	60	55
QFP6	60	105	70	55	50
QFP8	128	45	–	–	–
QFP8	144	45	40	35	30
QFP8	208	45	40	35	30
QFP12	48	235	–	–	–
QFP13	64	170	–	–	–
QFP14	80	120	–	–	–
QFP15	100	115	–	–	–
QFP17	144	70	50	45	35
QFP18	176	65	45	35	30
QFP20	144	85	60	45	40
TQFP14	80	100	70	50	40
TQFP14	100	100	–	–	–
TQFP15	100	110	–	–	–

Lead Frame Resin : Cu

Cu-L/F

Package Type	Number of pins	0m/sec	1m/sec	2m/sec	3m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	80	85(°C/W)	55	45	40
QFP5	100	80	55	35	30
QFP5	128	80	55	35	30
QFP8	120	45	–	–	–
QFP8	160	45	32	25	23
QFP8	256	50	–	–	–
QFP10	304	35	20	16	–
TAB-Q10	304	35	40	–	–
QFP12	48	175	120	90	80
QFP13	64	130	80	55	50
QFP14	80	110	–	–	–
QFP15	100	90	–	–	–
QFP20	184	65	–	–	–
QFP21	178	55	–	–	–
QFP21	216	55	–	–	–
QFP22	208	45	35	25	23
QFP22	256	45	35	25	23
QFP23	184	40	–	–	–
QFP23	240	40	–	–	–
TQFP12	48	165	–	–	–
TQFP13	64	140	–	–	–
TQFP15	128	105	–	–	–
TQFP24	144	80	–	–	–
HQFP5	128	60	–	–	–
HQFP8	160	32	19	12	10
HQFP15	128	87	45	30	–
H2QFP23	240	30	–	–	–
H3QFP15	128	85	–	–	–

PBGA

Package Type	Number of pins	0m/sec	1m/sec	2m/sec	3m/sec
		θj-a	θj-a	θj-a	θj-a
PBGA	225	72(°C/W)	46	37	–
PBGA	256	53	33	25	–
PBGA	358	45	–	–	–

■ We also produce other packages. Please contact EPSON Sales Division for detail.

User Interface

EPSON supports the following four Interfaces for customers.

1. HDL Interface

The Verilog-HDL or VHDL source file after function simulation and test pattern are brought to EPSON. Then EPSON will execute all design process from logic synthesis at our site.

2. Netlist Interface

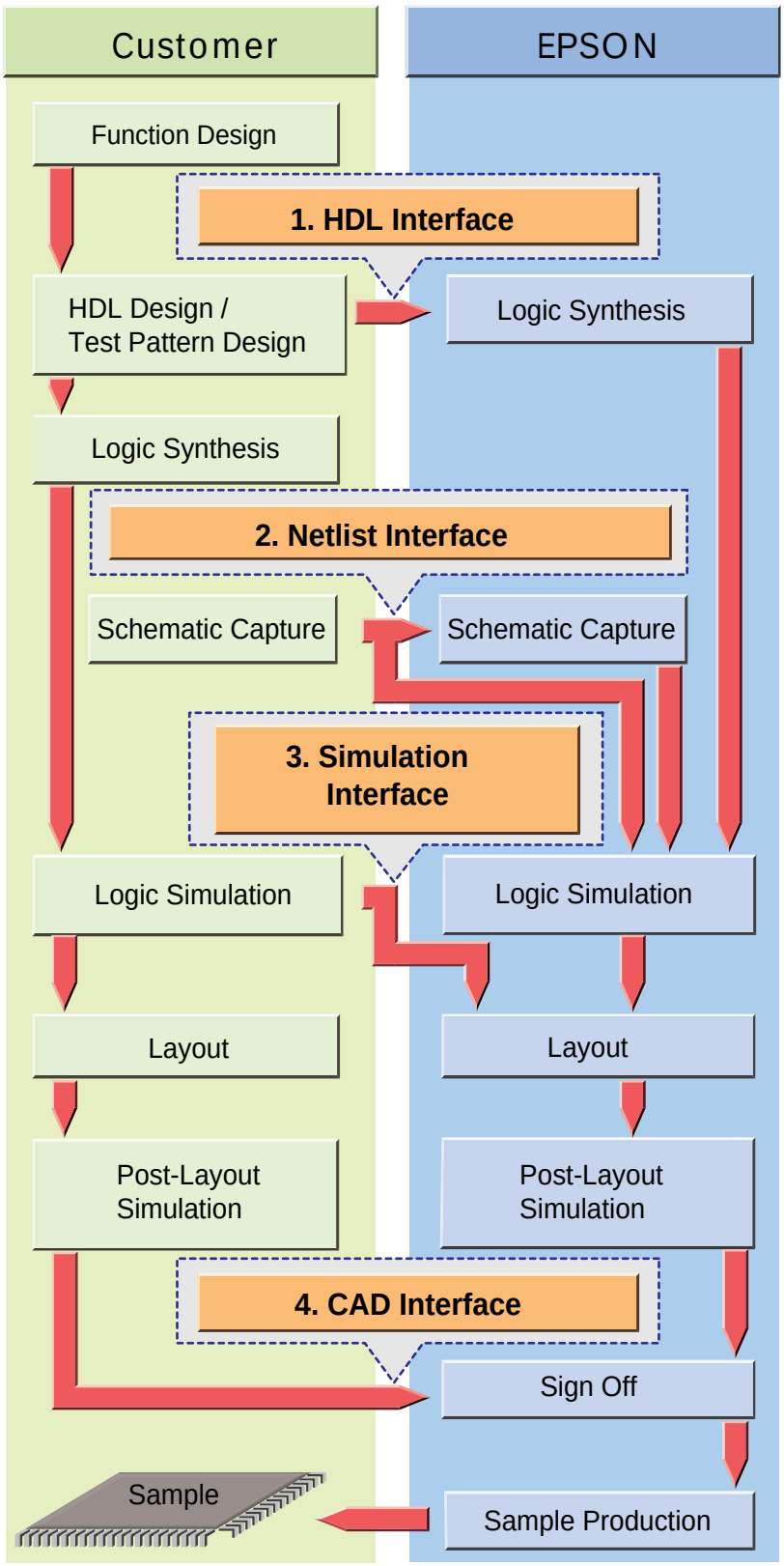
The Verilog-VHDL or VHDL gate level netlist after logic sythesis and test pattern are brought to EPSON. EPSON will execute all design process from logic simulation at our site. The optional schematic and test pattern are also brought to EPSON. EPSON will execute all design process from schematic capture at our site.

3. Simulation Interface

The Verilog-HDL gate level netlist after gate level simulation and test pattern are brought to EPSON. EPSON will execute all process from layout at our site.

4. CAD Interface

The Verilog-HDL gate level netlist after layout and post-layout simulation and test pattern are brought to EPSON. EPSON will execute all process from sample production at our site.



Development Support

As the ASIC devices become faster and larger, many kinds of ASIC development tools are required. EPSON supports various ASIC development tools, for example, HDL design is needed for the top-down design method.

■ HDL Design

The interrface of top-down design using Verilog-XL/Vss/Design Compiler is strongly supported by EPSON.

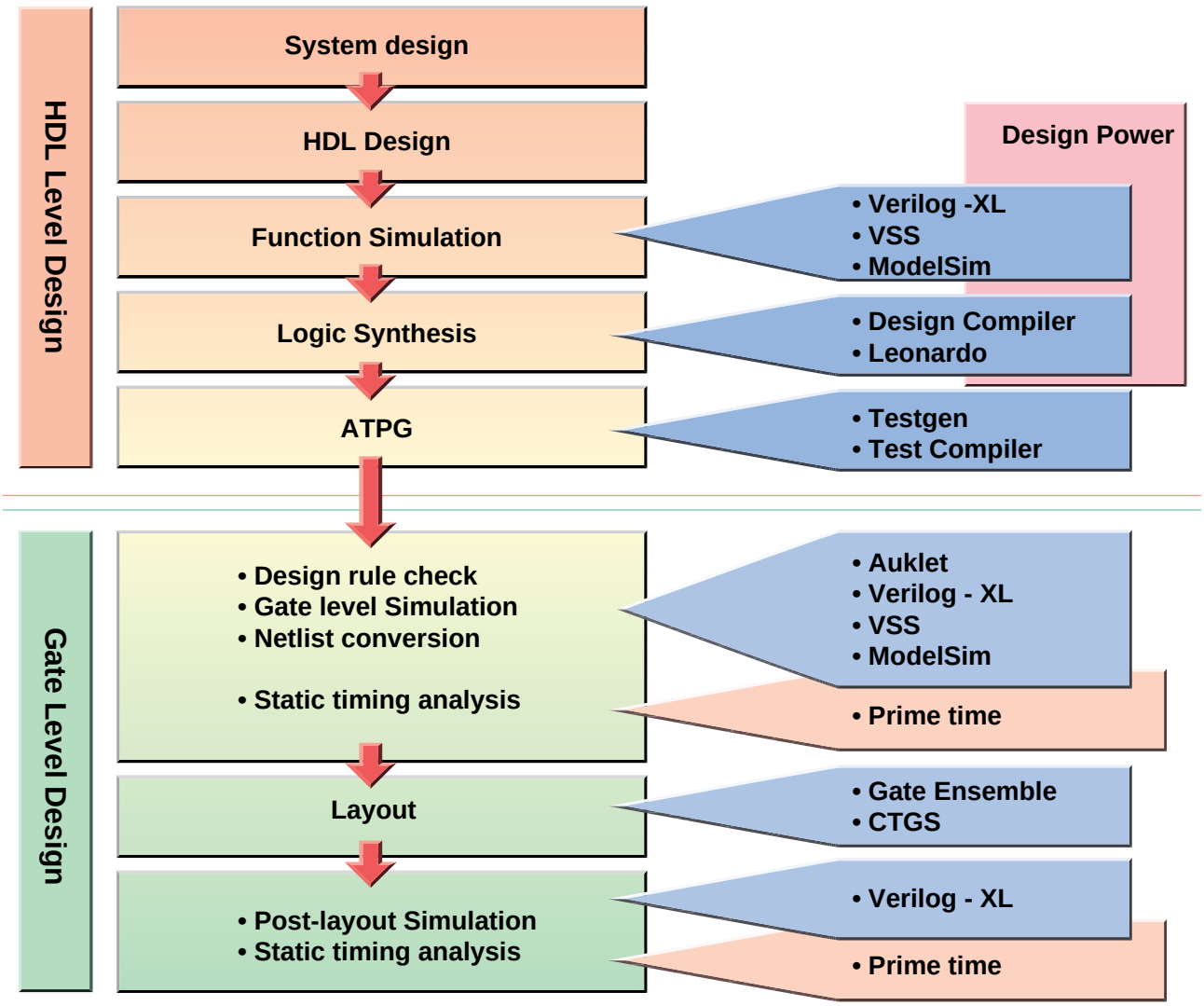
■ High Accuracy Circuit Design

High accuracy circuit design is supported by using the non-linear model simulation, well-balanced clock tree generation.

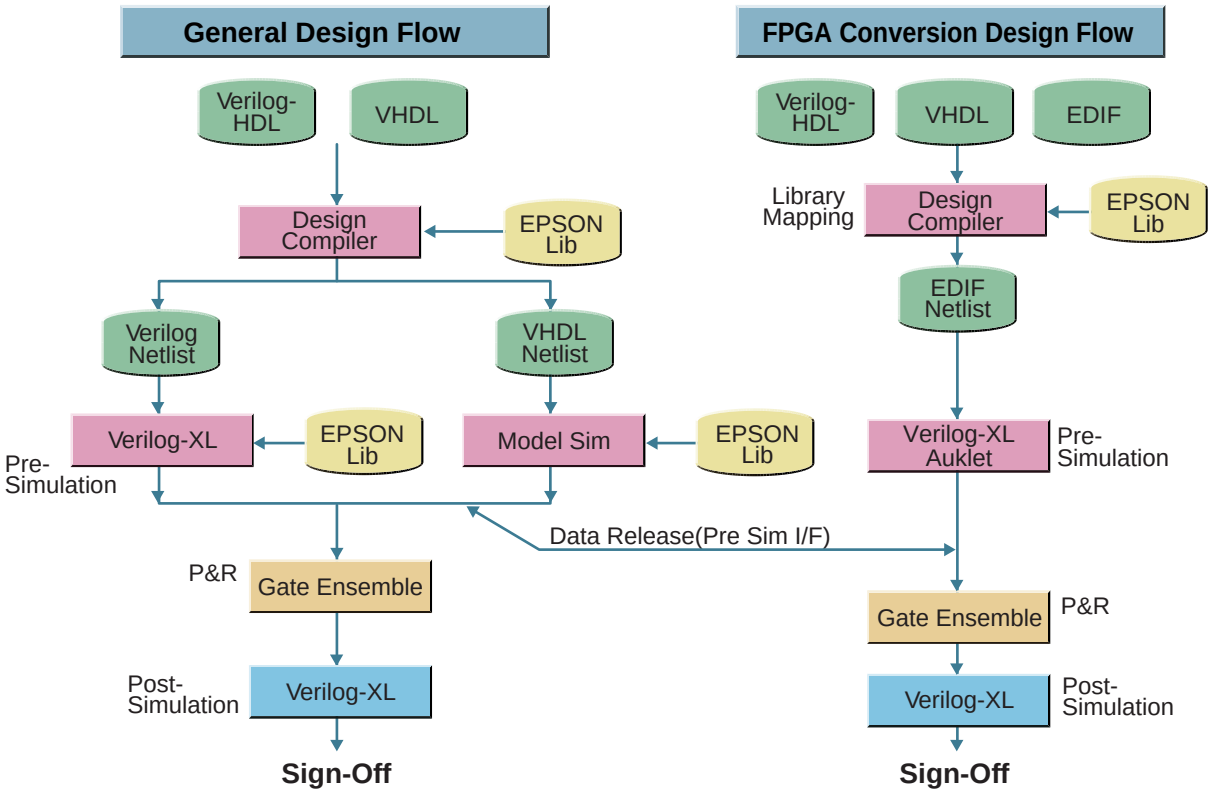
■ ATPG

High quality testing generation, before chip manufacture is necessary because the defective fraction in the market must be minimized. The test pattern and simplified test circuit design for high detection of the fraction detective is supported.

Development Flow and Top-down Design Tool



HDL Design Flow



EPSON's ASIC Development Support System-Auklet

< Main Functions >

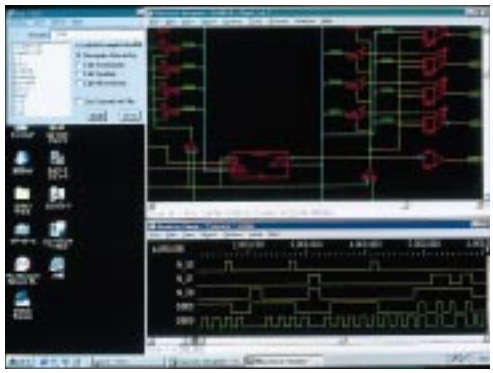
- Schematic capture by ECS
- Gate level simulation, waveform analysis and unswitched gates by using Verilog-XL (Cadence Design Systems Inc.) or Polaris (by AVANT! Corp.)

< Features >

- A total development support system with excellent GUI can be used on the following Windows system:
  Windows 95,98&NT/X-Window/Open Window.
- An error is high-lighted in the diagram when checking the electrical connection and included Fan-in / Fan-out between the on-line ERC and schematic.
- Waveform can display the resulting waveforms by simulation. The waveforms can be observed by communicating with the schematic by probing the I / O signals, internal nodes and so on.
- Supporting to create the test pattern by inputting waveforms

Loan "Auklet"

- If a customer has a problem that is not ready for a development tool or can not be developed by using the conventional design flow, EPSON supports the development of EPSON's ASIC products by using the development tool "Auklet". "Auklet" can be loaned without any charge.



The displayed logic simulation used by "Auklet"

Design For Testability

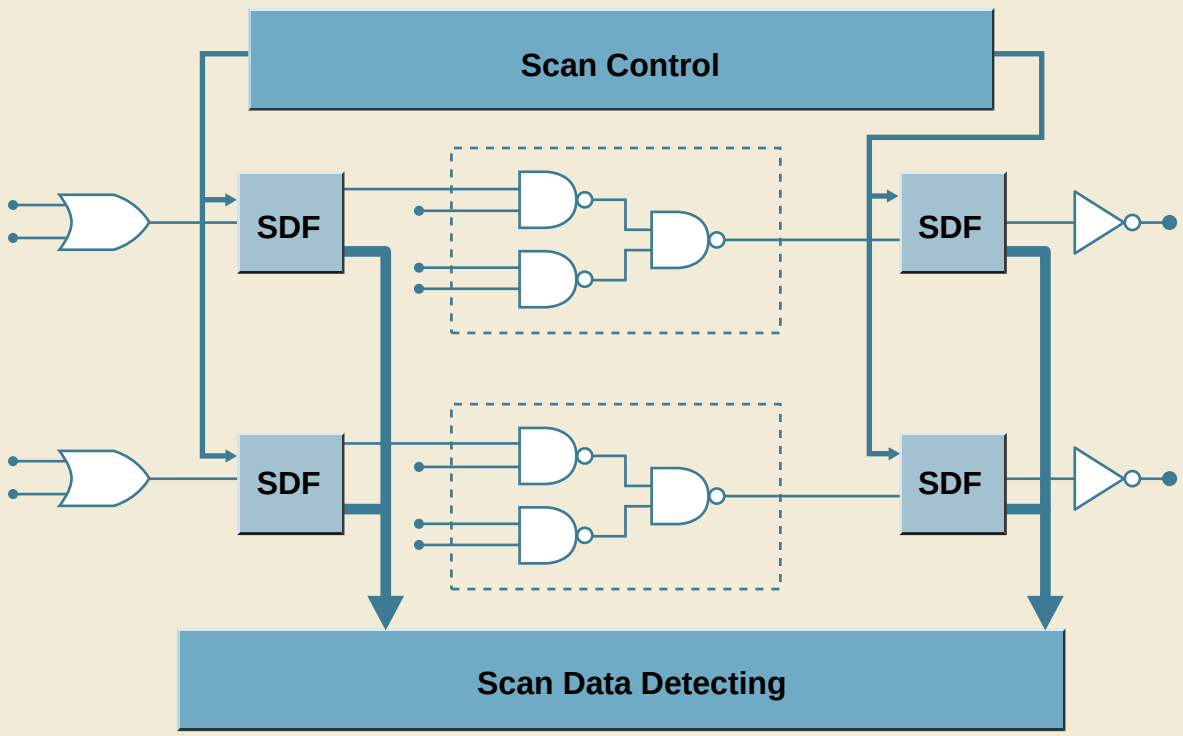
ASIC development needs to make it easier to inspect functions and test LSIs because a circuit is composed with large-scale integration, high -speed and complicated functions.
EPSON supports many methods for eliminating complicated testing.

Scanning Design

Scanning design is very powerful as a method for simplifying test design.
ATPG (Automatic Test Pattern Generator) can also be used and the test pattern for detecting high rates of faults can be created automatically.

< Features >

- Shortening the period of test pattern design and cutting down the production process
- Detecting faulty circuits and automatic creating test patterns
- Highly rate of fault detection (more than 95 percent in fact)



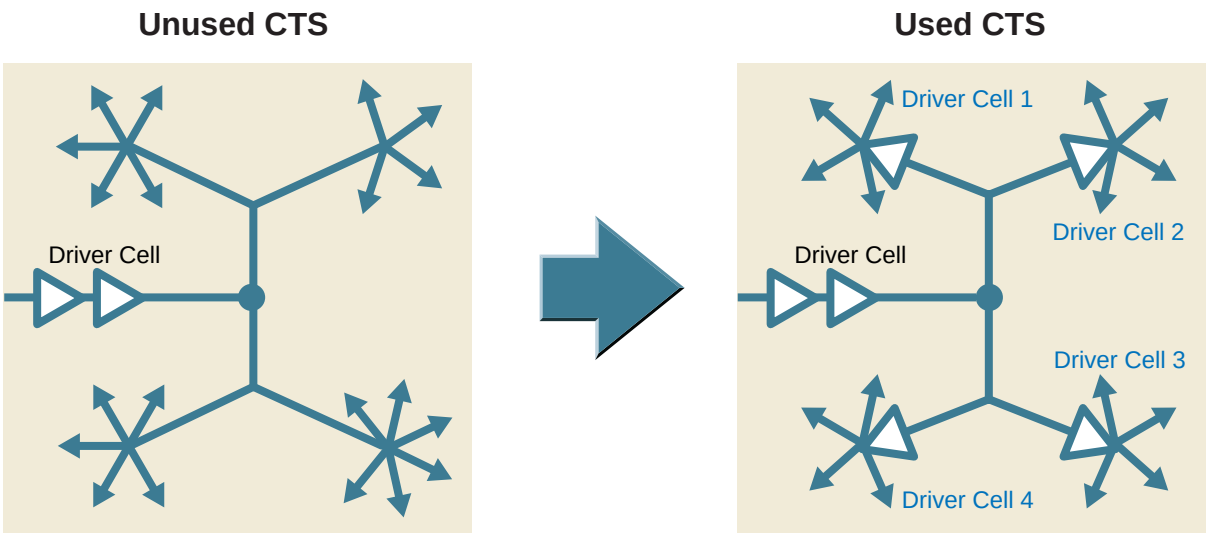
SDF : Flip-flop for scanning

: Combination circuit

: Scan data

CTS (Clock tree Synthesis)

Too many fan-outs and clock skew caused by wiring propagation delay is minimized and the clock tree is generated automatically when placing and routing.



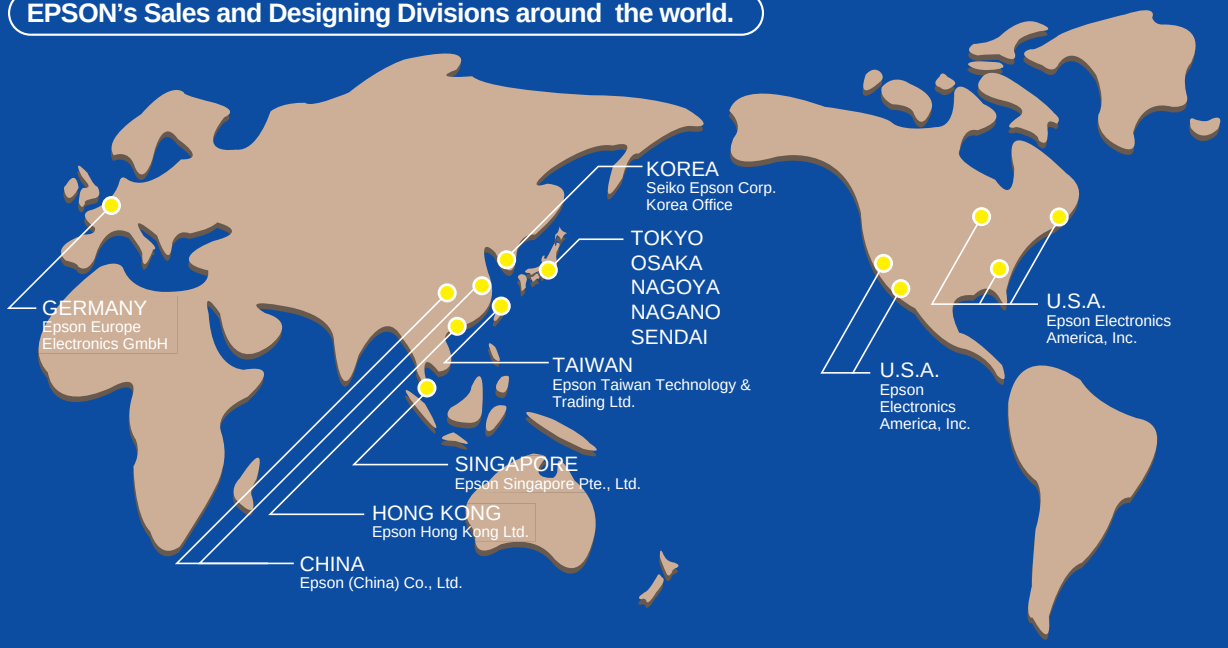
■ ***Otherwise, EPSON can support the test design like a JTAG.***

ASIC
Gate Array / Standard Cell / Embedded Array
October / 1999

In Partnership with Our Customers and with the Newest CMOS Technology, High Technology Products of the Next Generation can be Produced around the World.

The newest technologies are developed one after another in the new generation of high technology. Now, there are great changes from industry structures to life styles around the world. The key point in these changes depends on semiconductor development. EPSON is always meeting challenges to develop the newest semiconductor technology by forecasting the next generation and determining rapidly advancing and complex industrial needs. Our CMOS technology leads to the world in development of total power and the high quality products. We have the sprit to meet the challenge to develop a chip of higher density and with more advanced functions.
Thus, with EPSON's CMOS technology and ability to communicate with customers in Japan and around the World, our products can be always produced using the most excellent advanced technology.

EPSON's Sales and Designing Divisions around the world.



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