# Development of Gate Arrays/Embedded Arrays/Standard Cells

Semi-custom Gate Arrays and Standard Cells are developed by SEIKO EPSON in cooperation with the customer. The system is designed by the customer using design materials provided by SEIKO EPSON. The manufacturer will provide the 'Know How' and the 'Tools' required for making them into LSIs.
The logic and the test data are the means of exchanging information between the customer and SEIKO EPSON. As long as the LSIs are tested with SEIKO EPSON's tester and are delivered by SEIKO EPSON, the logic drawings will be necessary at all interface levels.
The customer's task is to carry out logic simulation right up to circuit approval. The rest will be performed by SEIKO EPSON.

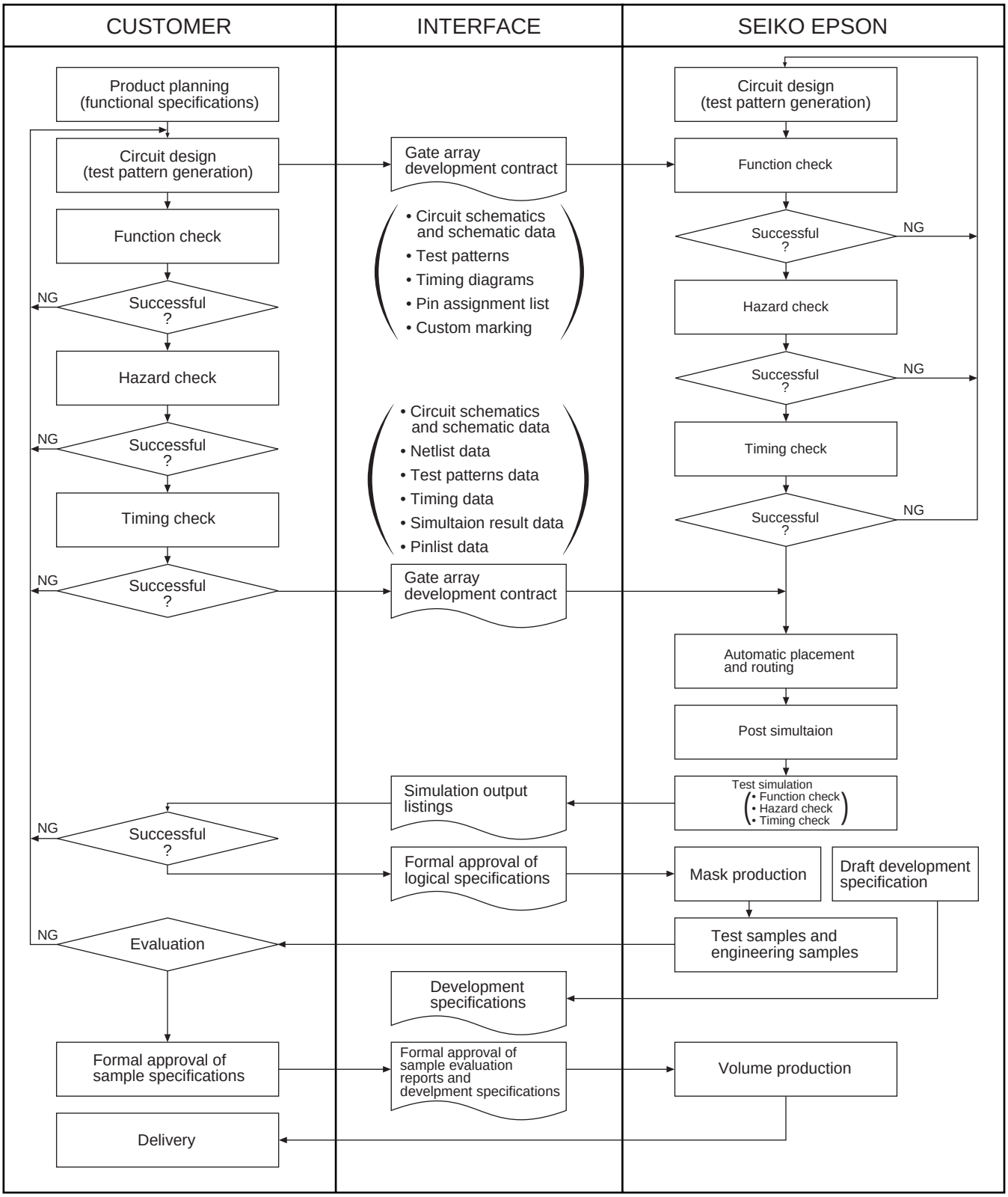
## 1 Interface Material

(1) Materials provided by SEIKO EPSON
- Design Manual
- Cell Library
- Time Chart Sheet (When Cartridge Tape (CT) is used, an CT will be provided for reference.)
- Timing Definition Sheet
- Assignment Sheet for package pin arrangement
- Assignment Sheet for package marking

(2) Materials provided by the customer
- Logic drawing on SEIKO EPSON's format
- Test Data
  : Time Chart
  : Pattern data by CT or Floppy disk
- Timing Definition
- Assignment for package pin arrangement
- Logo for package marking

## 2 Development Flow (Gate Arrays/Standard Cells)

LSI development for the SLA and SSC family can be carried out using the customer's logic circuit drawing and simulation data. The powerful DA support tool then checks this data before the LSI is presented to the customer.


CUSTOMER
INTERFACE
SEIKO EPSON
Product planning (functional specifications)
Circuit design (test pattern generation)
Function check
NG
Successful ?
Hazard check
NG
Successful ?
Timing check
NG
Successful ?
Gate array development contract
• Circuit schematics and schematic data
• Test patterns
• Timing diagrams
• Pin assignment list
• Custom marking
• Circuit schematics and schematic data
• Netlist data
• Test patterns data
• Timing data
• Simultaion result data
• Pinlist data
Gate array development contract
Simulation output listings
NG
Successful ?
Formal approval of logical specifications
NG
Evaluation
Development specifications
Formal approval of sample specifications
Formal approval of sample evaluation reports and develpment specifications
Delivery
Circuit design (test pattern generation)
Function check
NG
Successful ?
Hazard check
NG
Successful ?
Timing check
NG
Successful ?
Automatic placement and routing
Post simultaion
Test simulation
• Function check
• Hazard check
• Timing check
Mask production
Draft development specification
Test samples and engineering samples
Volume production

## 3 Embedded Arrays

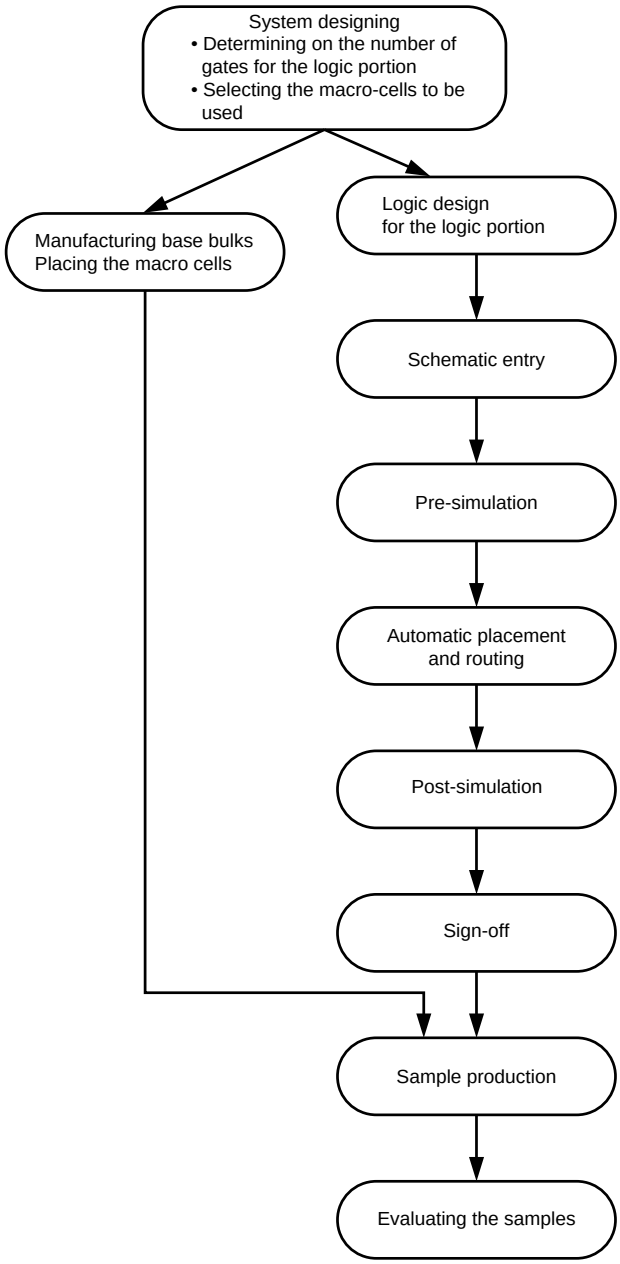
An embedded array is an ASIC under a new method featuring consolidation of “Sea of gates” of a gate array and hard-macro cells for specific applications. With this product, the concept of system-on-chip has been realized by use of hard-macro cells with high functions and quicker delivery leadtime has become available when modifying the circuit, thanks to adoption of the “Sea of Gates” for the logic portion.

● Designing the embedded arrays

When designing embedded arrays, execute system design first and determine the number of gates for the logic section and select the macro-cell to be used before starting manufacture of base bulks. The base bulks, necessary hard-macro cells and the Sea of Gates for the logic portion are manufactured up to just before the routing process. In parallel with this manufacturing processes, processes from the circuit designing of the logic portion through post-simulation fix should be executed, similar to the cases of ordinary gate arrays, to go into sample production process after sign-off.

After the sign-off, samples can be shipped with the same delivery leadtime as that of the gate arrays. Also, when making logic circuit modifications or ROM data changes, NRE charge and developing leadtime can be reduced to a level similar to that of the gate arrays.

Development flow




● Embedded Array Products mounted Macro Cell

| Function of each macrocell | |
|---|---|
| • 8-bit CPU Core | • Oscillator |
| • Peripheral | • ADC |
| • RAM(8KByte) | • DAC |
| • ROM(40KByte) | • Op-AMP |
| • FIFO | • Comparator |
| • RAMDAC(10bit×3ch) | • $I^2$CBUS |
| • Ethernet Transceiver | • LVDS* |
| • LCD Controller | • USB I/F* |
| • Monochrome LCD Interface | • IrDA V1.1* |
| • RTC | • PCMCIA* |
| • PLL | • Multiplier* |

* Under development

● Embedded Array Products

| Series Name | Process Technology | Propagation Delay | Power Voltage |
|---|---|---|---|
| SSL50000Series* | 0.35µm (CMOS 2-, 3- and 4-layers) | 0.140ns (3.3V) | Internal cell 3.3V, 2.0V<br>Part of I/O cells 5.0V, 3.3V, 2.0V<br>(Built-in a level shifter) |
| SSL40000Series | 0.45µm (CMOS 2- and 3-layers) | 0.160ns (3.3V) | Internal cell 3.3V, 3.0V (2.0V single)<br>Part of I/O cells 5.0V, 3.3V, 3.0V (2.0V single)<br>(Built-in a level shifter) |
| SSL35000Series | 0.6µm (CMOS 2- and 3-layers) | 0.25ns (5.0V)<br>0.33ns (3.3V) | 5.0V, 3.3V, 3.0V<br>(Built-in a level shifter) |

* Under development

## 4 ASIC Development on Auklet

SEIKO EPSON's Logic Array Design Systems brings engineering workstation level ASIC development to affordable personal computer systems or workstations. It gives you the necessary tools for all stages, from schematic capture through logic verification and pre-simulation.

Auklet Ver.1.3™ Development environment

| ITEMS | Auklet / PC | Auklet & Auklet-Core / UK |
|---|---|---|
| Host | IBMPC-AT, or close compatible*1 | SPARC Series |
| CPU | Pentium or more | SPARC |
| Operating Systems | MS-DOS Ver.6.0 or later | SUN OS 4.1.3 or 4.1.4, Solaris 2.5 |
| Window System | MS-Windows95,<br>MS-Windows NT 3.5 or 4.0 | X-Window (X11R5) + Motif<br>Open Window Ver.2 or ver.3 |
| Main Memory*2 | 32MB or more | 32MB or more |
| Hard Disk*2 | 220 MB or more | 220MB or more |
| Swap Space*2 | 64MB or more | 64MB or more |
| Mouse | In accordance with MS-Windows 95,<br>In accordance with MS-Windows NT | In accordance with X-Window<br>/Open Window |
| Printer | In accordance with MS-Windows 95,<br>In accordance with MS-Windows NT | Equivalent to Postscript |
| Plotter | In accordance with MS-Windows 95,<br>In accordance with MS-Windows NT | Nothing |

*1 : As certain personal computers are recommended, call our IC Sales Division for details.

*2 : This is the minimum memory size needed to drive Auklet or LADSnet. Therefore, it needs at least this memory size on more to drive Auklet or LADSnet complertely.

## 5 ASIC Development on CAE Vendor Tool

SEIKO EPSON provides the libraries and utility programs that transform your existing engineering workstations into powerful ASIC development platforms.
Having the tools to run simulations on your own hardware gives you greater control over crucial early design stages. Keeping the work in-house also means better quality control and greatly reduced turnaround time.

## 6 Supported Systems

● ASIC Development tool support library

Available as of November, 1997

| ASIC Design Tools | | Libraries available | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Vendor | Tool | SLA 50000 | SLA 50000H | SLA 40000 | SLA 35000 | SLA 30000 | SLA 9000F | SLA 100X | SSC 2500 | SSC 2000 |
| Seiko Epson | LADSnet | — | — | — | — | — | — | ✓ | ✓ | ✓ |
| | Auklet | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| Cadence | CTGen | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | Verilog-XL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| Viewlogic | TestGen | ✓ | ✓ | ✓ | | ✓ | ✓ | | | |
| | MOTIVE | ✓ | ✓ | ✓ | | ✓ | ✓ | | | |
| Synopsys | Design Compiler | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| | Design Power | ✓ | ✓ | ✓ | | ✓ | ✓ | | | |
| | VSS | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| Exemplar | Leonardo | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | |
| Model Tech. | V-System | ✓ | ✓ | ✓ | | ✓ | ✓ | | | |

✓ : Supported, — : Not Supported