Embedded Arrays

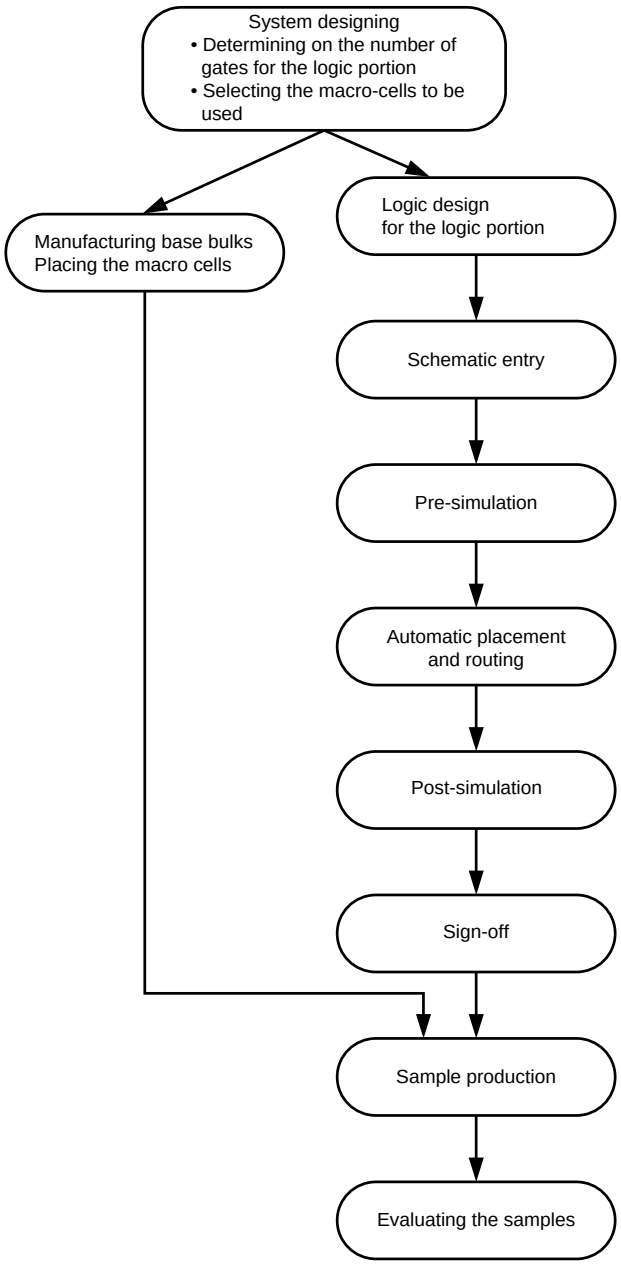
An embedded array is an ASIC under a new method featuring consolidation of "Sea of gates" of a gate array and hard-macro cells for specific applications. With this product, the concept of system-on-chip has been realised by use of hard-macro cells with high functions and quicker delivery lead time has become available when modifying the circuit, thanks to adoption of the "Sea of Gates" for the logic portion.

● Designing the embedded arrays

When designing embedded arrays, execute system design first and determine the number of gates for the logic section and select the macro-cell to be used before starting manufacture of base bulks. The base bulks, necessary hard-macro cells and the Sea of Gates for the logic portion are manufactured up to just before the routing process. In parallel with this manufacturing processes, processes from the circuit designing of the logic portion through post-simulation fix should be executed, similar to the cases of ordinary gate arrays, to go into sample production process after sign-off.

After the sign-off, samples can be shipped with the same delivery lead time as that of the gate arrays. Also, when making logic circuit modifications or ROM data changes, NRE charge and developing lead time can be reduced to a level similar to that of the gate arrays.

Development flow



● Embedded Array Products mounted Macro Cell

Function of each macro cell	
• 32-bit CPU Core	• Oscillator
• 8-bit CPU Core	• ADC
• Peripheral	• DAC
• RAM(1 M bits)	• Op-AMP
• ROM(2 M bits)	• Comparator
• FIFO	• LVDS
• RAMDAC(10-bit x 3 ch)	• USB
• Ethernet Transceiver	• IrDA V1.1
• LCD Controller	• PCMCIA
• Monochrome LCD Interface	• Multiplier
• RTC	• PLL

● Embedded Array Products

Series Name	Process Technology	Propagation Delay	Power Voltage
SSL60000Series*	0.25 m (CMOS 3/4/5 layers)	0.107ns (2.5V)	Internal cell 2.0V, 2.5V Part of I/O cells 2.0V, 2.5V, 3.3V (Built-in level shifter)
SSL50000Series	0.35 m (CMOS 2-, 3- and 4-layers)	0.140ns (3.3V)	Internal cell 3.3V, 2.0V Part of I/O cells 5.0V, 3.3V, 2.0V (Built-in a level shifter)
SSL40000Series	0.45 m (CMOS 2- and 3-layers)	0.160ns (3.3V)	Internal cell 3.3V, 3.0V (2.0V single) Part of I/O cells 5.0V, 3.3V, 3.0V (2.0V single) (Built-in a level shifter)
SSL35000Series	0.6 m (CMOS 2- and 3-layers)	0.25ns (5.0V) 0.33ns (3.3V)	5.0V, 3.3V, 3.0V (Built-in a level shifter)

* Under development