

## Standard Cells

The standard cells are semi-custom ICs that incorporates a well-designed internal logic cell and ROM/RAM, CPU peripheral circuits or analog circuits into a single chip. Compared to the gate arrays, they boast higher design flexibility, functionality and integration capabilities, providing system LSI chips optimized to the customer needs. These features greatly help electronic device manufacturers design products with a compact body, lower power consumption, and a lower price.

	Gate array	Embedded array	Standard cell
	SLA50000H Series	SSL50000 Series	SCB50000 Series
Integration (%)	100	73	40
Power consumption ( $\mu$ W/MHz/FF)	7.65	4.51	2.22

The standard cells offer 2/5 the degree of integration and 1/3 the power consumption of our SLA5000H series gate arrays.

### SCB60000 series

Series	SCB60000 series*
Features	<ul style="list-style-type: none"> <li>High integrated (Use of 0.25<math>\mu</math>m silicon-gate with 3/4/5-layer wiring process)</li> <li>High-speed operation (Internal gate delay: 107ps/2.5V, 2-input NAND, typical load)</li> <li>Selective supply voltage For a single power supply (2.5V, 2.0V) For dual power supplies (3.3V I/O / 2.5V Internal, 3.3V I/O / 2.0V Internal)</li> <li>Low power consumption (2.5V/MHz/gate, Internal cell at 2.5V)</li> <li>Driving power (I<sub>OL</sub>=0.1, 1, 3, 6, 12, 24mA/at 3.3V, I<sub>OL</sub>=0.1, 1, 3, 6, 9, 18mA/2.5V internal, I<sub>OL</sub>=0.05, 0.3, 1, 2, 3, 6mA/at 2.0V)</li> </ul>
Macro cell	Same as the embedded-array-mountable macrocells.
Package lineup	QFP48-304 pins, PBGA, TBGA, PFBGA, CFLGA

\*: Under development

### SCB50000 series

Series	SCB50000 series
Features	<ul style="list-style-type: none"> <li>High integrated (Use of 0.35<math>\mu</math>m silicon-gate with 2/3/4-layer wiring process)</li> <li>High-speed operation (Internal gate delay: 0.14ns/3.3V, 2-input power NAND, typical load)</li> <li>Selective supply voltage For a single power supply (2.0V, 2.5V, 3.3V) For dual power supplies (5.0V I/O / 3.3V Internal, 3.3V I/O / 2.5V Internal, 3.3V I/O / 2.0V Internal)</li> <li>Low power consumption (0.25<math>\mu</math>m/MHz/gate, Internal cell at 3.3V)</li> <li>Driving power (I<sub>OL</sub>=0.1, 1, 3, 8, 12, 24mA/at 5.0V, I<sub>OL</sub>=0.1, 1, 2, 6, 12mA/at 3.3V, I<sub>OL</sub>=0.05, 0.3, 0.6, 2, 4mA/at 2.0V)</li> </ul>
Macro cell	Same as the embedded-array-mountable macrocells.
Package lineup	QFP48-304 pins, PBGA, TBGA, PFBGA, CFLGA

Usable gates: Differ depending on the circuit and the listing is for your reference.