EPSON

SSC2000 Series

Standard Cell

Wide Voltage Operation Products

- Built-in Analog Circuit
- Internal Two Power Supplies (Level Shifter)
- Wide Operating Voltage: 0.9 V to 6.0 V
- Up to 11,000 gates

■ DESCRIPTION

The SSC2000 series is a CMOS standard cell with low-threshold manufacturing process providing low voltage operation.
Low voltage analog cells and internal two power supplies are available for this series.
The availability of low voltage analog cells along with digital circuit and the internal level shifter provides two power supplies mixed mode applications suitable for Lap-top PCs, Handy Terminals, pagers and hand held computer systems.

■ FEATURES

- Analog Circuit

OP AMP	4
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Analog Switch	22
Resistor	
Capacitance	

- Internal Two Power Supplies
  The SSC2000 series can be chosen with different two power supplies from 0.9 V to 6.0 V.
- Low voltage oscillator starting with mimium 0.9 V.
- I/O level: CMOS, TTL
- This series provides 20 models to I/O combinations of die sizes from 250 to 11000 gates.

■ PRODUCT LINEUP

Master / Features		SSC 2010	SSC 2020	SSC 2030	SSC 2040	SSC 2050	SSC 2060	SSC 2070	SSC 2080	SSC 2090	SSC 2100	SSC 2110	SSC 2120	SSC 2130	SSC 2140	SSC 2150	SSC 2160	SSC 2170	SSC 2180	SSC 2190	SSC 2200
Usable BCs		250	350	450	800	900	1,100	1,400	1,700	2,000	2,400	3,200	3,600	4,000	4,600	6,200	7,600	8,600	9,500	10,500	11,000
Number of PADs		40	44	48	60	64	72	80	84	92	100	112	120	124	132	148	160	172	180	188	192
Propagation Delay	Internal Gates	tpd = 8.5ns (standard at 1.5V), tpd = 3.0ns (standard at 3.0V)																			
	Input Buffers	tpd = 12.0ns (standard at 1.5V), tpd = 4.0ns (standard at 3.0V)																			
	Output Buffers	tpd = 40.0ns (standard at 1.5V), tpd = 14.0ns (standard at 3.0V) CL = 15pF																			
Propagation Delay Coefficient		The coefficient value is calculated by multiplying the coefficient value of Max. or Min. for Typ. value for VDD = 1.5V described in the SSC2000 series MSI CELL Library by lowest value or highest value of using voltage. For more information about the coefficient value, contact our sales office for technical support.																			
I/O Level		TTL, CMOS																			
Input Mode		TTL, CMOS, Pull-up/Pull-down, Schmitt, Dual power level interface (Level shifter)																			
Output Mode		Normal, Open drain, 3-state, Bi-directional, Dual power level interface (Level shifter)																			

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD1, 2}$	–0.3 to 7.0	V
Input voltage	V_I	–0.3 to $V_{DD1, 2}$ + 0.3	V
Output voltage	V_O	–0.3 to $V_{DD1, 2}$ + 0.3	V
Storage temperature	T_{stg}	–65 to 150	°C

■ RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD1}	1.5 V	1.35	1.5	1.65	V
	V_{DD2}	3 V (V_{DD1} = 1.5 V)	2.70	3.00	3.30	V
	V_{DD1}	3 V	2.70	3.00	3.30	V
	V_{DD2}	5 V (V_{DD1} = 3.0 V)	4.50	5.00	5.50	V
Allowable supply voltage	$V_{DD1, 2}$		0.90	—	6.00	V
Operating temperature	T_{opr}		0	—	70	°C

■ ELECTRICAL CHARACTERISTICS

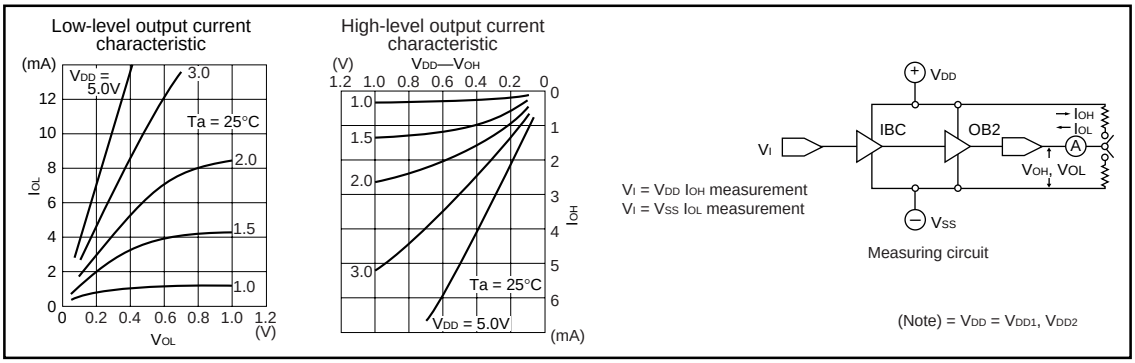
(Ta = 0 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Standby supply current	I_{DDS1}	Static state, V_{DD1} = 1.5 V	—	—	500	nA
	I_{DDS1}	Static state, V_{DD1} = 3.0 V	—	—	1.0	µA
	I_{DDS2}	Static state, V_{DD2} = 3.0 V per level shifter	—	—	90	nA
	I_{DDS2}	Static state, V_{DD2} = 5.0 V per level shifter	—	—	100	nA
High-level output voltage	V_{OH}	V_{DD1} = 1.5 V, I_{OH} = –0.17 mA	1.3	—	—	V
	V_{OH}	$V_{DD1, 2}$ = 3.0 V, I_{OH} = –0.64 mA	2.7	—	—	V
	V_{OH}	V_{DD2} = 5.0 V, I_{OH} = –1.2 mA	4.6	—	—	V
Low-level output voltage	V_{OL}	V_{DD1} = 1.5 V, I_{OL} = 0.58 mA	—	—	0.2	V
	V_{OL}	$V_{DD1, 2}$ = 3.0 V, I_{OL} = 2.2 mA	—	—	0.3	V
	V_{OL}	V_{DD2} = 5.0 V, I_{OL} = 4.0 mA	—	—	0.4	V
High-level input voltage	V_{IH1}	(TTL) V_{DD2} = 5.0 V	1.8	—	—	V
	V_{IH2}	(CMOS) V_{DD1} = 1.5 V	1.25	—	—	V
		(CMOS) $V_{DD1, 2}$ = 3.0 V	2.4	—	—	V
		(CMOS) V_{DD2} = 5.0 V	3.5	—	—	V
Low-level input voltage	V_{IL1}	(TTL) V_{DD2} = 5.0 V	—	—	0.6	V
	V_{IL2}	(CMOS) V_{DD1} = 1.5 V	—	—	0.25	V
		(CMOS) $V_{DD1, 2}$ = 3.0 V	—	—	0.6	V
		(CMOS) V_{DD2} = 5.0 V	—	—	1.5	V
Input leakage current	I_{LI}		–200	—	200	nA

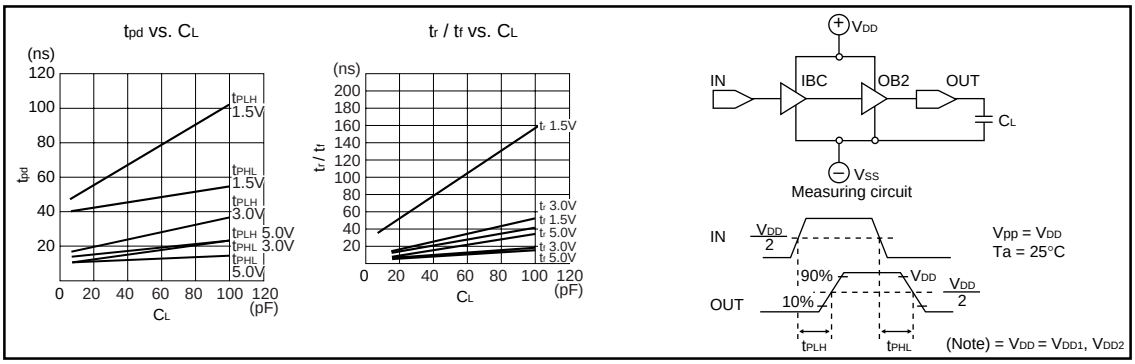
Note) I_{DD2} flows from V_{DD2} to the I/O cell using level shifter.
V_{DD1}: Voltage applied to MSI inside the chip and I/O cell.
V_{DD2}: Another voltage applied to MSI inside the chip and I/O cell.
$V_{DD2} \geq V_{DD1}$ should be satisfied

■ CHARACTERISTICS CURVES

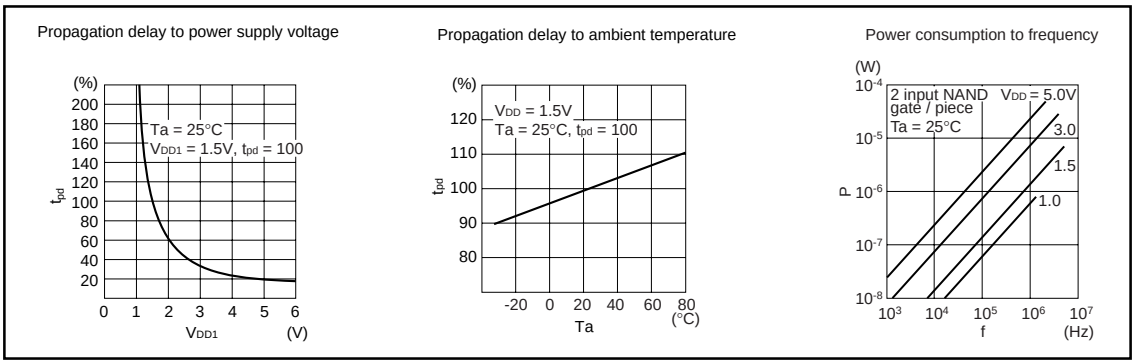
● Output current characteristic



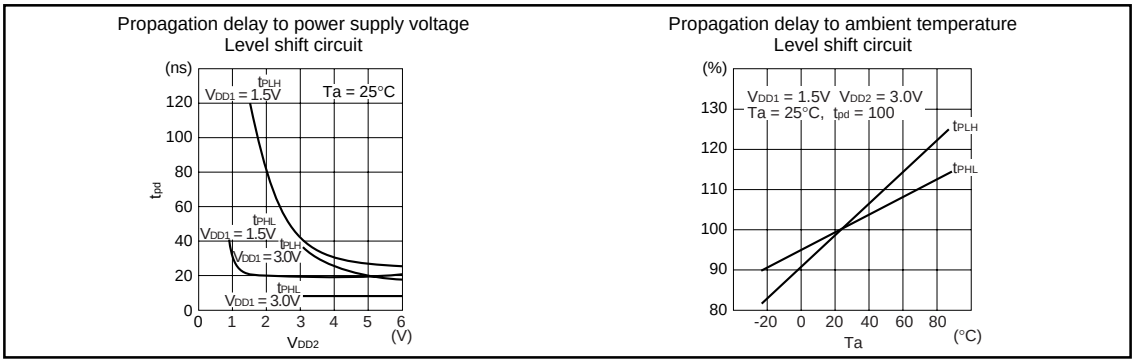
● tpd vs. CL characteristic and tr / tf vs. CL characteristic



● Propagation delay characteristic and power consumption characteristic



● Level shift circuit propagation delay characteristic



■ ANALOG CELL CHARACTERISTICS

● OP AMP

Single Power Supply 2.5 V to 6.0 V
Low Voltage Operation 2.5 V (Min.)
Stand-by Mode

(V_{DD} = 5.0V Ta = 0 to 70°C)

Characteristic	Symbol	OP1			OP2			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Offset Voltage	V_{OS}			10			10	mV
Input Common-mode Voltage Range	V_{CM}	0.9		4.5	1.2		4.4	V
Voltage Gain	AV	70	90		60	80		dB
Common-mode Rejection Ratio	CMRR	70	80		70	80		dB
Power Supply Rejection Ratio	PSRR	60	80		60	80		dB
Supply Current	I_S	10	30	65	35	100	210	µA
Output Short-sircuit Current	I_{OS}	5	15		20	60		µA
Slew Rate	SR	0.07	0.15		0.15	0.35		V/µs
Gain Bandwidth Product	GBW	80	200		130	300		kHz

(V_{DD} = 5.0V Ta = 0 to 70°C)

Characteristic	Symbol	OP3			OP4			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Offset Voltage	V_{OS}			10			10	mV
Input Common-mode Voltage Range	V_{CM}	1.2		4.4	1.4		4.2	V
Voltage Gain	AV	60	80		50	60		dB
Common-mode Rejection Ratio	CMRR	70	80		60	70		dB
Power Supply Rejection Ratio	PSRR	60	80		50	70		dB
Supply Current	I_S	70	200	400	180	470	980	µA
Output Short-sircuit Current	I_{OS}	50	150		150	430	800	µA
Slew Rate	SR	0.7	1.5		0.9	2.0		V/µs
Gain Bandwidth Product	GBW	270	550		220	440		kHz

Operation Voltage Range OP1 – OP3 V_{DD} = 2.5 to 6.0 V
OP4 V_{DD} = 4.0 to 6.0 V

● Comparator

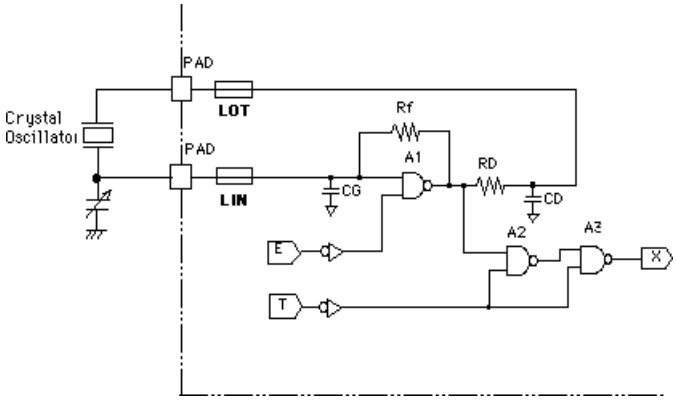
CMOS Output
Stand-by Mode

(V_{DD} = 5.0V 0 °C Ta = 0 to 70°C)

Characteristic	Symbol	CM1			CM2			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Offset Voltage	V_{OS}			10			10	mV
Response Time	td	0.34	1.34	2.30	0.10	0.41	0.70	µS
Input Common-mode Voltage Range	V_{IC}	0.8		4.8	0.9		4.7	V
Supply Current	I_{CC}	470	810	1250	530	1030	1560	µA

● **Crystal Oscillator**

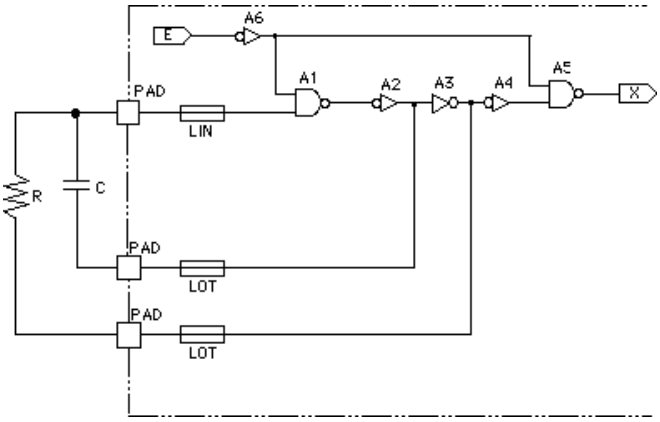
Oscillation Frequency several 10 kHz to several 10 MHz
Stand-by Mode
Oscillator cell is almost upper compatible of SLA100X series



● **CR Oscillator**

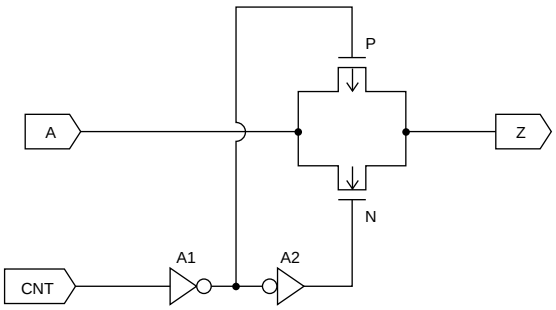
Oscillation Frequency f = 1/(KCR)

f : Oscillation Frequency (Hz) ,
K : Constant (Reference: 1.4 to 2.2)
R : Resistor (Ω) ,
C : Capacitance (F)

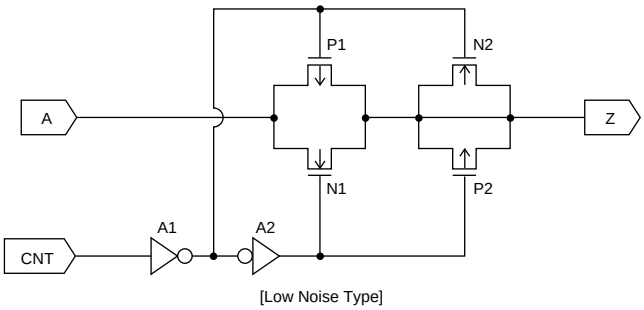


● **Analog Switch**

Two types of analog switches provided each for the I/O cell and internal cells.
The low noise type reduces the switching noise.



P : P channel MOS transistor
N : N channel MOS transistor
A1, A2 : Inverter



[Low Noise Type]

P1, P2 : P channel MOS transistor
N1, N2 : N channel MOS transistor
A1, A2 : Inverter

● **Resistor**

Resistance : 10 k Ω step

Cell	Symbol	Allowance of Step Resistance (kΩ)		
		Min.	Typ.	Max.
RP❊	Rp	7	10	20

● **Capacitor**

Capacitance : 1 pF step

Cell	Symbol	Allowance of Step Capacitance (pF)		
		Min.	Typ.	Max.
C❊	C	0.7	1.0	1.3

● **TEG sample**

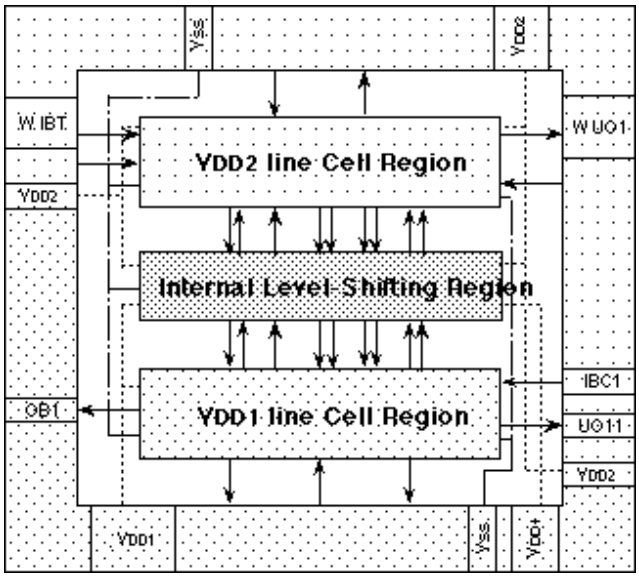
SSC2000 series provides the TEG samples to evaluate the analog characteristics on the target board. And the TEG samples for all analog cells are available except for a resistor and capacitor. The kinds of TEG samples are as follows:

Series	Package	Cell
SSC2140F10	QFP8 - 128 pin	Analog Switch (I/O Cell)
SSC2140F20	QFP8 - 128 pin	OP AMP Comparator Analog Switch (Internal Cell)
SSC2140F30	QFP8 - 128 pin	Crystal Oscillator Circuit CR Oscillator Circuit

● **Internal Two Power Supplies (Level Shifter)**

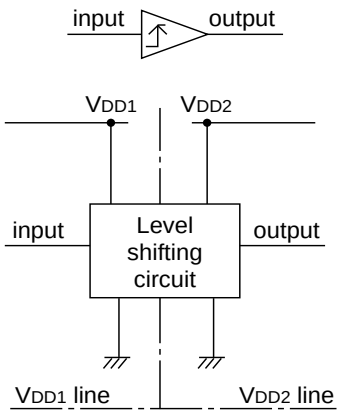
SSC2000 series provides the level shifter on the internal cells. There are two types of the internal two power supplies MSI cells, the MSI cells on the V_{DD1} line and the MSI cells on the V_{DD2} line. The two power supplies can operate in a wide voltage range from 0.9 V to 6.0 V. The following specification must be satisfied.

$$V_{DD2} \geq V_{DD1}$$

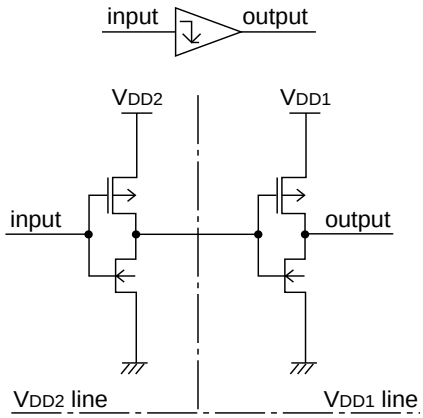


● **Directions for Level Shifter**

Low (Middle) Voltage Range
-> High Voltage Range



High Voltage Range
-> Low Voltage Range



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