EPSON

SSC2500 Series

Wide Voltage Standard Cell

- Wide Voltage Operation (V_{DD} = 0.9 to 5.5 V)
- Ultra-low Power Consumption
- Two Different Power Supplies are Usable
- Usable Gates from 300 to 16,000 Gates

■ DESCRIPTION

SSC2500 series are 1.6μm CMOS standard cell using low threshold production process.
Use of level shifters in its internal cell region provides cell regions working on two different power supplies within an IC, thus making them effectively applicable to equipment in which multiple power supplies are used in combination or to systems requiring battery backup. The low power type miniature cells newly added to the line-up can provide ultra-low power consumption LSI's. Moreover, they can be installed into small packages.

■ FEATURES

- CMOS standard cell using 1.6µm low voltage process.
- Applicable to wide operation voltage range of 0.9 to 5.5V.
- Low power type miniature cells allow ultra-low power consumption applications.
- Usable two power supplies by using level shifters.
  Most suitable for equipment using multiple power supplies in combination or systems requiring battery backup.
- Built-in oscillation circuit, resistors and capacitors providing low voltage oscillation at 0.9V.
- 18 of usable gate choices ranging from 300 to 16,000 gates.
- Built-in analog circuit (Under development).

■ PRODUCT LINEUP

Master / Features		SSC 2510	SSC 2520	SSC 2530	SSC 2540	SSC 2550	SSC 2560	SSC 2570	SSC 2580	SSC 2590	SSC 2600	SSC 2610	SSC 2620	SSC 2630	SSC 2640	SSC 2650	SSC 2660	SSC 2670	SSC 2680
Usable BCs		300	400	500	700	800	1,300	2,200	3,300	3,800	4,800	6,000	7,500	8,000	9,000	10,000	13,000	14,000	16,000
Number of PADs		44	48	52	60	64	80	100	120	128	144	160	176	184	196	208	232	240	256
Propagation Delay	Internal Gates	tpd = 7.5ns (standard at 1.5V), tpd = 2.5ns (standard at 3.0V)																	
	Input Buffers	tpd = 12.0ns (standard at 1.5V), tpd = 4.0ns (standard at 3.0V)																	
	Output Buffers	tpd = 40.0ns (standard at 1.5V), tpd = 14.0ns (standard at 3.0V) CL = 15pF																	
Maximum of Operating Frequancy		10MHz (3.0V), 1MHz (1.5V)																	
Propagation Delay Coefficient		The coefficient value is calculated by multiplying the coefficient value of Max. or Min. for Typ. value for VDD = 1.5V described in the SSC2500 series MSI CELL Library by lowest value or highest value of using voltage. For more information about the coefficient value, contact our sales office for technical support.																	
I/O Level		TTL, CMOS																	
Input Mode		TTL, CMOS, Pull-up/Pull-down, Schmitt, Dual power level interface (Level shifter)																	
Output Mode		Normal, Open drain, 3-state, Bi-directional, Dual power level interface (Level shifter)																	

■ ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{DD} (V_{DD1}, V_{DD2})	–0.3 to 7.0	V
Input voltage	V_I	–0.3 to V_{DD}+0.5	V
Output voltage	V_O	–0.3 to V_{DD}+0.5	V
Output current/pin	I_{OUT}	±25	mA
Storage temperature	Tstg	–65 to 150	°C

■ RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD} (V_{DD1}, V_{DD2})	1.2	1.5	1.8	V
		2.7	3.0	3.3	
		4.5	5.0	5.5	
Operating voltage	V_{DD} (V_{DD1}, V_{DD2})	0.9	—	5.5	V
Working temperature	Topr	0 –20	25 25	70 85	°C

■ ELECTRICAL CHARACTERISTICS

● **V_{DD} = 5.0V ±10%** (V_{SS} = 0 V, Ta = –20 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Standby supply current	I_{DDS}	Static state *1	—	—	6	μA
Input leak current	I_{LI}		–1	—	1	μA
3-state leak current	I_{OZ}		–1	—	1	μA
High level output voltage	V_{OH}	I_{OH} = –1, –2 mA	V_{DD}–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 1, 2, 4, 8, 12 mA	—	—	0.4	V
High level input voltage	V_{IH}	TTL level, V_{DD} = Max.	2.0	—	—	V
Low level input voltage	V_{IL}	TTL level, V_{DD} = Min.	—	—	0.8	V
High level input voltage	V_{T+}	TTL Schmitt, V_{DD} = 5.0 V	1.2	—	2.0	V
Low level input voltage	$V_{T–}$	TTL Schmitt, V_{DD} = 5.0 V	0.5	—	1.2	V
Hysteresis voltage	V_{HI}	TTL Schmitt, V_{DD} = 5.0 V	0.4	—	—	V
High level input voltage	V_{IH}	CMOS level, V_{DD} = Max.	3.5	—	—	V
Low level input voltage	V_{IL}	CMOS level, V_{DD} = Min.	—	—	1.5	V
High level input voltage	V_{T1+}	CMOS Schmitt 1, V_{DD} = 5.0 V	2.2	—	3.5	V
Low level input voltage	$V_{T1–}$	CMOS Schmitt 1, V_{DD} = 5.0 V	1.0	—	2.2	V
Hysteresis voltage	V_{HI1}	CMOS Schmitt 1, V_{DD} = 5.0 V	0.75	—	—	V
High level input voltage	V_{T2+}	CMOS Schmitt 2, V_{DD} = 5.0 V	2.7	—	3.65	V
Low level input voltage	$V_{T2–}$	CMOS Schmitt 2, V_{DD} = 5.0 V	0.65	—	1.6	V
Hysteresis voltage	V_{HI2}	CMOS Schmitt 2, V_{DD} = 5.0 V	1.35	—	—	V
Pull-up resistance	R_{PU}	V_I/V_O = 0 V	30 60 120 240	50 100 200 400	100 200 400 800	kΩ
Pull-down resistance	R_{PD}	V_I/V_O = V_{DD}	30 60 120 240	50 100 200 400	100 200 400 800	kΩ

*1: Under 4,000 gate equivalent and when the low power type cell is not used. (V_{DD} = V_{DD1}, V_{DD2}, V_{DD2}≥V_{DD1})

● **V_{DD} = 3.0V ±10%** (V_{SS} = 0 V, Ta = –20 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Static power consumption	I_{DDS}	Static state *1	—	—	5	μA
Input leak current	I_{LI}		–1	—	1	μA
High level output voltage	V_{OH}	I_{OH} = –0.45, –0.9 mA	V_{DD}–0.3	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.425, 0.85, 1.7, 3.4, 5.1 mA	—	—	0.3	V
High level input voltage	V_{IH}	CMOS level, V_{DD} = Max.	2.2	—	—	V
Low level input voltage	V_{IL}	CMOS level, V_{DD} = Min.	—	—	0.85	V
High level input voltage	V_{T1+}	CMOS Schmitt 1, V_{DD} = 3.0 V	1.2	—	2.15	V
Low level input voltage	V_{T1-}	CMOS Schmitt 1, V_{DD} = 3.0 V	0.65	—	1.6	V
Hysteresis voltage	V_{HI1}	CMOS Schmitt 1, V_{DD} = 3.0 V	0.3	—	—	V
High level input voltage	V_{T2+}	CMOS Schmitt 2, V_{DD} = 3.0 V	1.35	—	2.25	V
Low level input voltage	V_{T2-}	CMOS Schmitt 2, V_{DD} = 3.0 V	0.45	—	1.2	V
Hysteresis voltage	V_{HI2}	CMOS Schmitt 2, V_{DD} = 3.0 V	0.55	—	—	V
Pull-up resistance	R_{PU}	V_I/V_O = 0 V	50 100 200 400	100 200 400 800	200 400 800 1600	kΩ
Pull-down resistance	R_{PD}	V_I/V_O = V_{DD}	50 100 200 400	100 200 400 800	200 400 800 1600	kΩ

*1:Under 4,000 gate equivalent and when the low power type cell is not used. (V_{DD} = V_{DD1}, V_{DD2}, V_{DD2}≥V_{DD1})

● **V_{DD} = 1.5V ±0.3V** (V_{SS} = 0 V, Ta = –20 to 85°C)

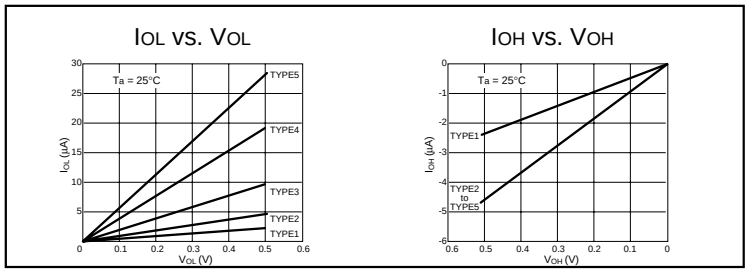
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Standby supply power	I_{DDS}	Static state *1	—	—	4	μA
Input leak current	I_{LI}		–1	—	1	μA
High level output voltage	V_{OH}	I_{OH} = –0.077, 0.154 mA	V_{DD}–0.2	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.07, 0.14, 0.28, 0.56, 0.84 mA	—	—	0.2	V
High level input voltage	V_{IH}	CMOS level, V_{DD} = Max.	1.3	—	—	V
Low level input voltage	V_{IL}	CMOS level, V_{DD} = Min.	—	—	0.25	V
High level input voltage	V_{T1+}	CMOS Schmitt 1, V_{DD} = 1.5 V	0.45	—	1.1	V
Low level input voltage	V_{T1-}	CMOS Schmitt 1, V_{DD} = 1.5 V	0.3	—	1.0	V
Hysteresis voltage	V_{HI1}	CMOS Schmitt 1, V_{DD} = 1.5 V	0	—	—	V
High level input voltage	V_{T2+}	CMOS Schmitt 2, V_{DD} = 1.5 V	0.45	—	1.1	V
Low level input voltage	V_{T2-}	CMOS Schmitt 2, V_{DD} = 1.5 V	0.25	—	0.9	V
Hysteresis voltage	V_{HI2}	CMOS Schmitt 2, V_{DD} = 1.5 V	0.05	—	—	V
Pull-up resistance	R_{PU}	V_I/V_O = 0 V	115 230 460 920	300 600 1200 2400	1150 2300 4600 9200	kΩ
Pull-down resistance	R_{PD}	V_I/V_O = V_{DD}	115 230 460 920	300 600 1200 2400	1150 2300 4600 9200	kΩ

*1:Under 4,000 gate equivalent and when the low power type cell is not used. (V_{DD} = V_{DD1}, V_{DD2}, V_{DD2}≥V_{DD1})

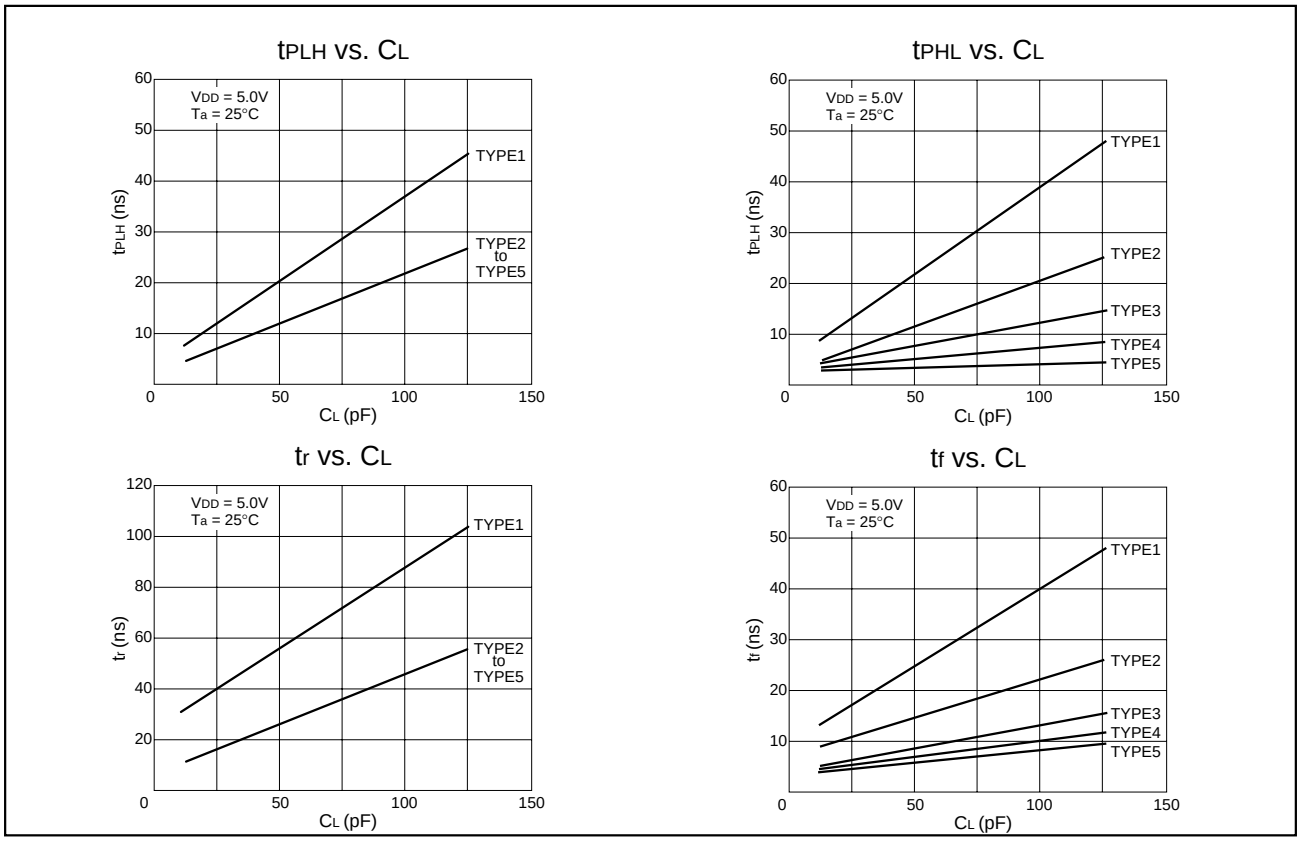
■ CHARACTERISTICS CURVES (V_{DD} = 5.0 V)

● Output Current Characteristics (V_{DD} = 5.0 V)

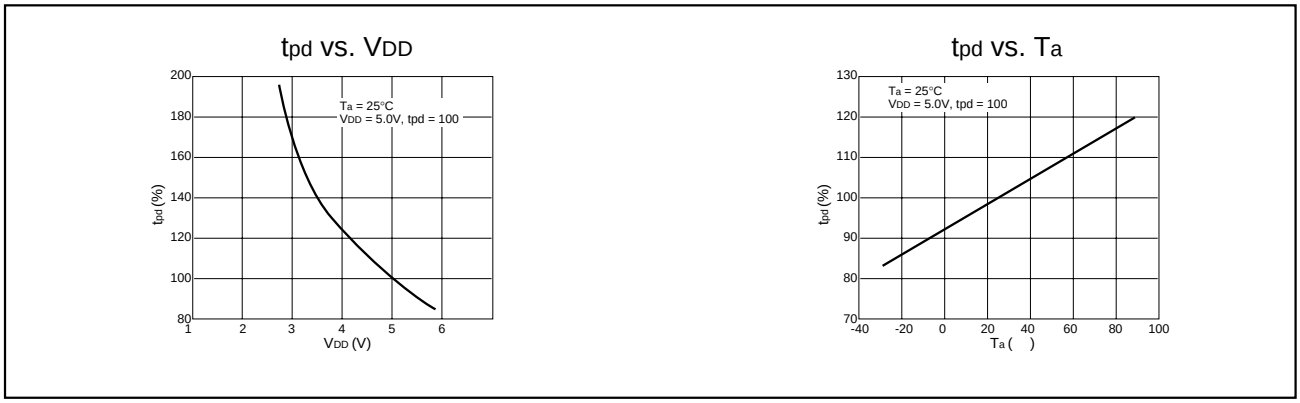
Type number	Output Current	
	I_{OH}(mA)	I_{OL}(mA)
Type 1	–1	1
Type 2	–2	2
Type 3	–2	4
Type 4	–2	8
Type 5	–2	12



● Output Buffer Characteristics (V_{DD} = 5.0 V)



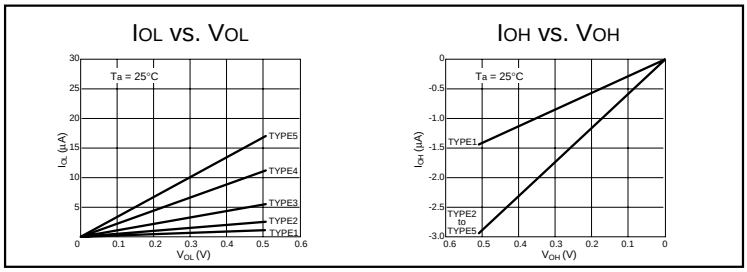
● Delay Characteristics (V_{DD} = 5.0 V)



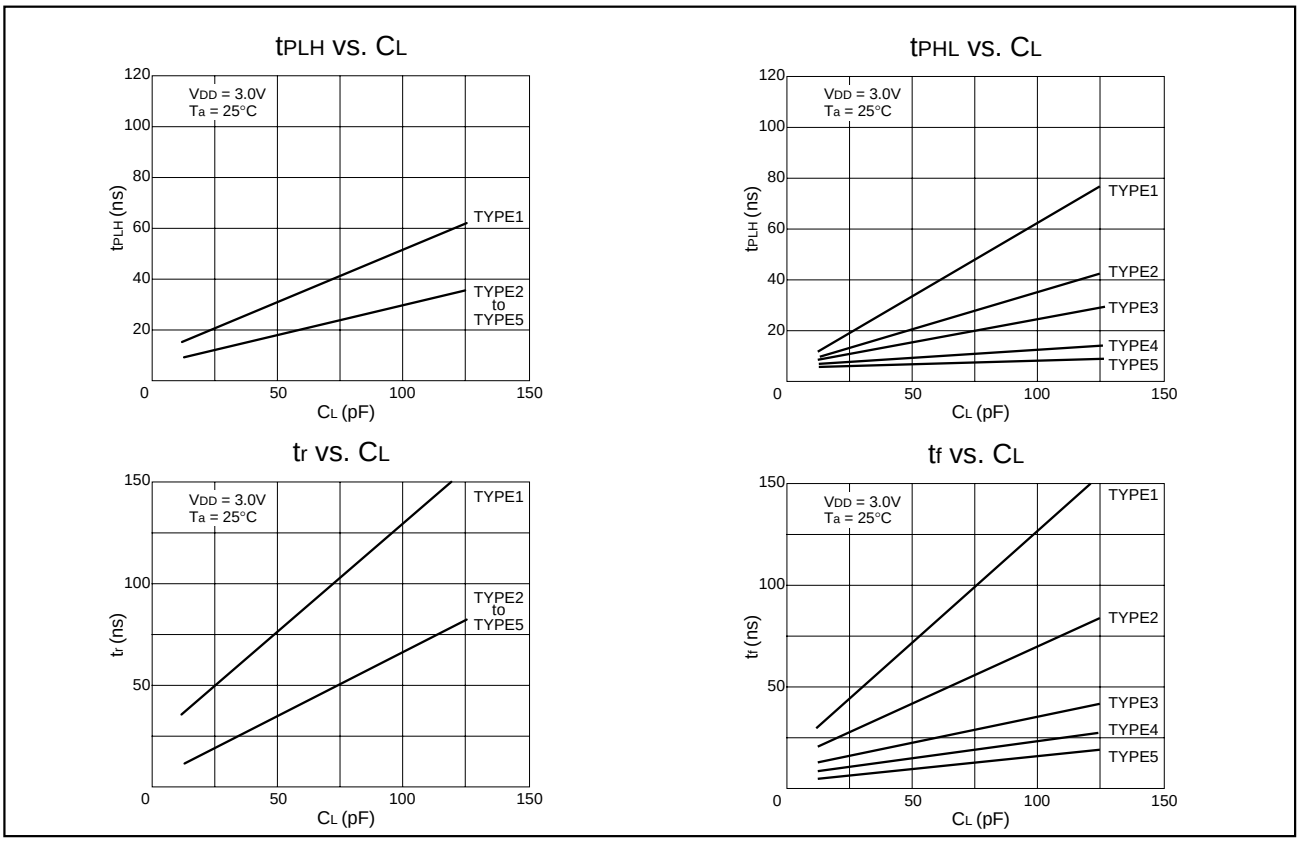
■ CHARACTERISTICS CURVES (V_{DD} = 3.0 V)

● Output Current Characteristics (V_{DD} = 3.0 V)

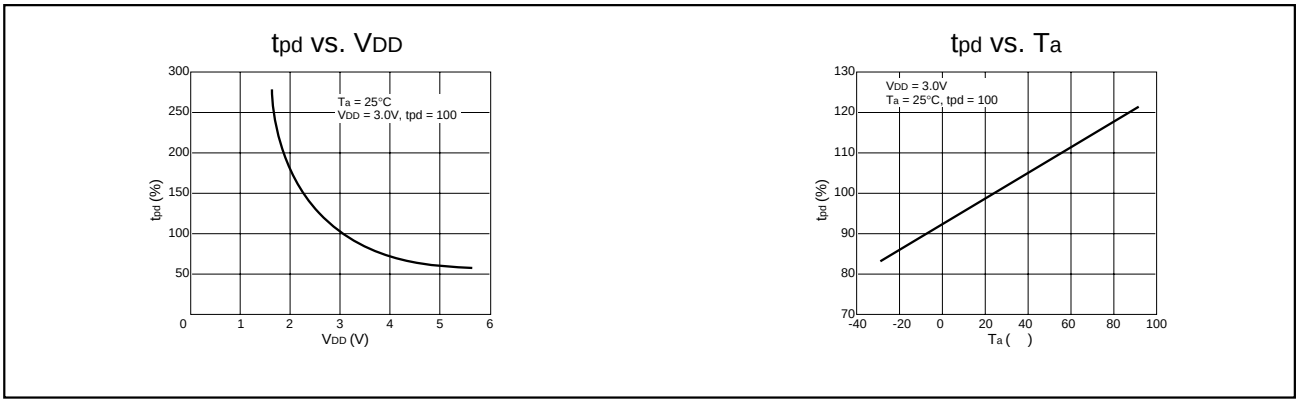
Type number	Output Current	
	I_{OH}(mA)	I_{OL}(mA)
Type 1	–450	425
Type 2	–900	850
Type 3	–900	1700
Type 4	–900	3400
Type 5	–900	5100



● Output Buffer Characteristics (V_{DD} = 3.0 V)



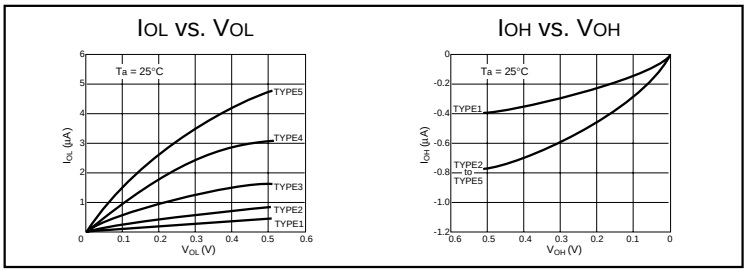
● Delay Characteristics (V_{DD} = 3.0 V)



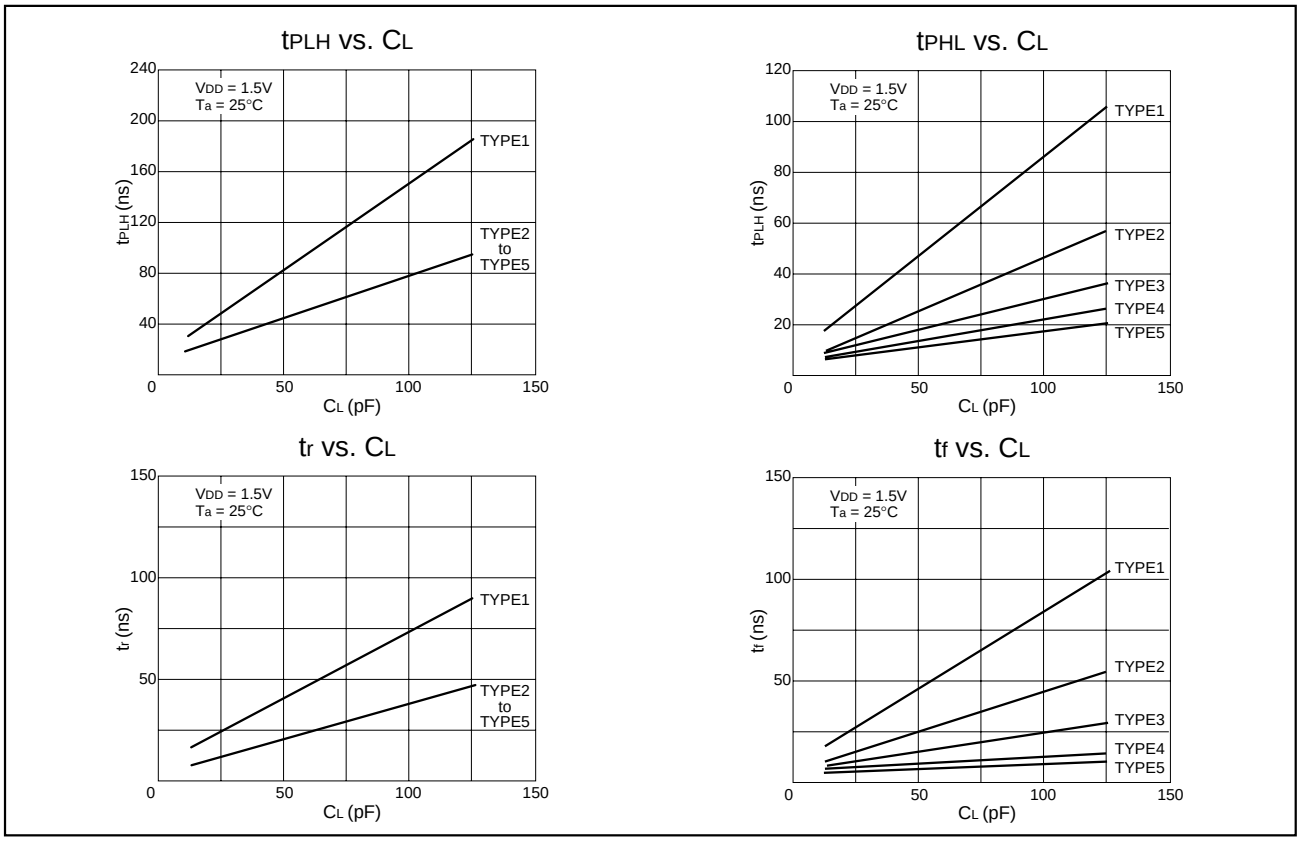
■ CHARACTERISTICS CURVES (V_{DD} = 1.5 V)

● Output Current Characteristics (V_{DD} = 1.5 V)

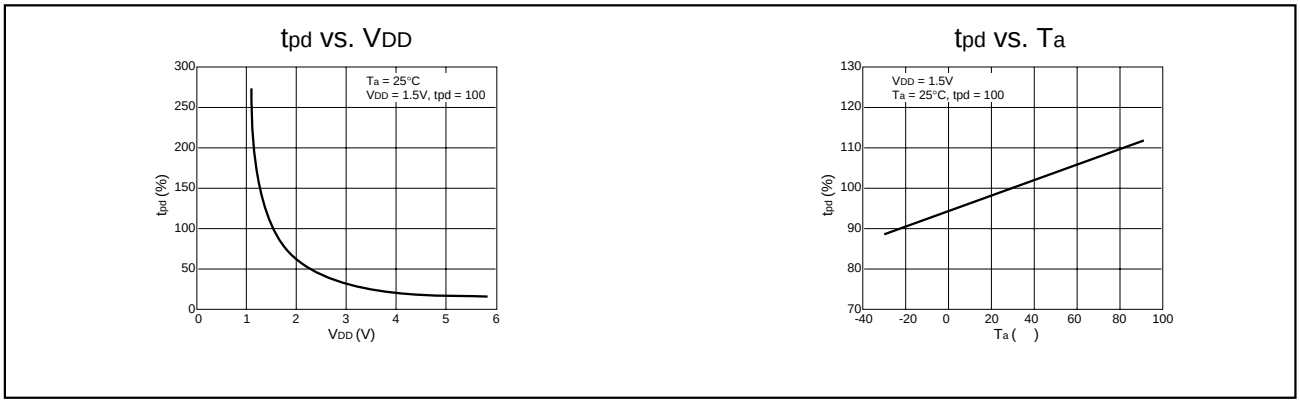
Type number	Output Current	
	I_{OH}(mA)	I_{OL}(mA)
Type 1	–77	70
Type 2	–154	140
Type 3	–154	280
Type 4	–154	560
Type 5	–154	840



● Output Buffer Characteristics (V_{DD} = 1.5 V)



● Delay Characteristics (V_{DD} = 1.5 V)

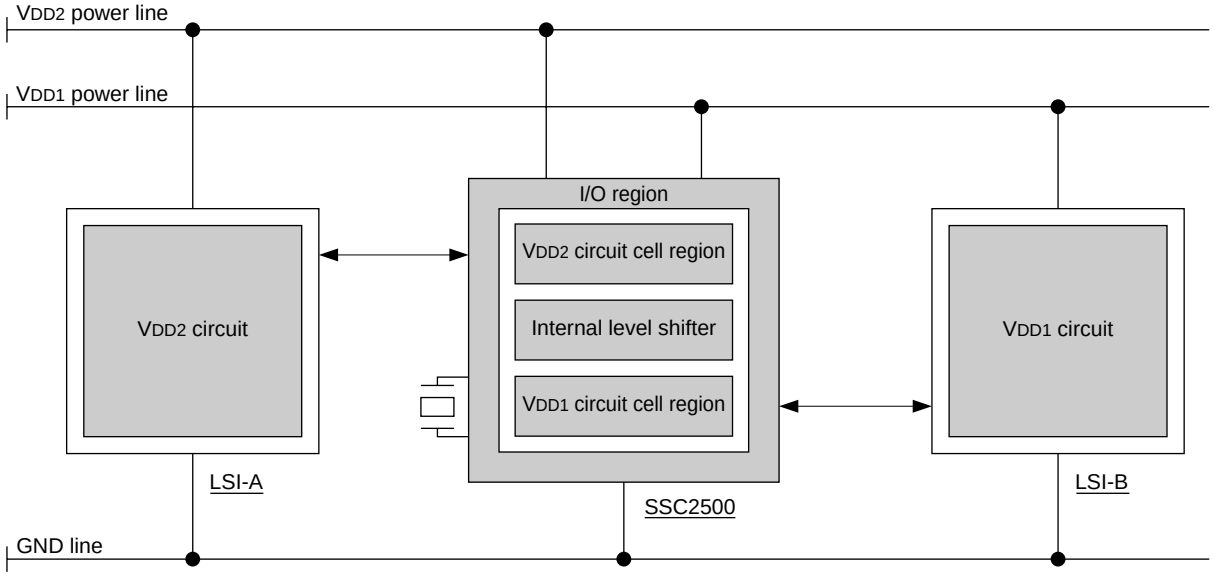


■ Two power supplies are usable:

For SSC2500 Series, level shifters can be built into the internal cell region by which cell regions workable on two different power supplies can be provided within an IC. For this purpose, two types of internal cells namely, V_{DD1} circuit cell and V_{DD2} circuit cell, are being prepared. Meanwhile, the relation of the voltage of these two power supplies must be:

$V_{DD2} \geq V_{DD1}$

This feature of being applicable to two different power supplies brought about by the level shifter facilitates equipment designs combining multiple power supplies or system designs requiring battery backup.



SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816 Fax: +81-(0)42-587-5624

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

Electric Device Information of EPSON WWW server

http://www.epson.co.jp

ENERGY SAVING EPSON