SCI7500F0A

Contents

OVERVIEW

Description

The SCI7500F0A is a four-line simultaneous selection method MLS (Multi Line Selection) drive power supply IC for driving liquid crystal displays. Using its CMOS charge pump-type high-efficiency voltage converter circuit, the chip is able to generate all the bias voltages required for the four-line MLS drive based on a single 3.0 V power supply input.
When a system is structured from column (segment) drivers such as the SED1580, row (common) drivers such as the SED1751, and this IC, this structure is able to produce a module with extremely low power consumption when compared to a conventional drive method.
Moreover, even greater power conservation is possible when combined with an LCD controller that can pause data transmission (a controller such as the SED1360).

Features

- Power Supply Voltage: 2.4 V to 3.6 V single-input power supply
- Low Consumption Current: 340 μA (in 6 × step-up mode, TYP)
- Standby Current: 5 μA (MAX)
- High Voltage Conversion Efficiency: 88% (6 × step-up mode, TYP)
- Generates all bias voltages required for 4-line MLS driving.
  An external contrast adjustment function can also be attached.
- Equipped with an internal charge pump-type DC/DC voltage converter circuit.
  Depending on the terminal settings, the chip can be switched between 5 × step-up (compatible with 1/200 duty) and 6 × step-up (compatible with 1/240 duty).
- Built-in electric charge discharging circuit for the liquid crystal drive current (VL).
- Internal “power off” function using an external signal (XSLP).
- Equipped internally with a liquid crystal drive polarity reverse signal generator circuit.
- The terminal settings can be used to set the range of time for the polarity reversal to 2H to 17H.
- Recommended panel size: VGA, 6.3" or less
- Product being shipped in QFP form ..... (QFP12-48 pin) SCI7500F0A
  Product being shipped in chip form SCI7500D0A
- This product not designed for resistance to radiation.

Block Diagram

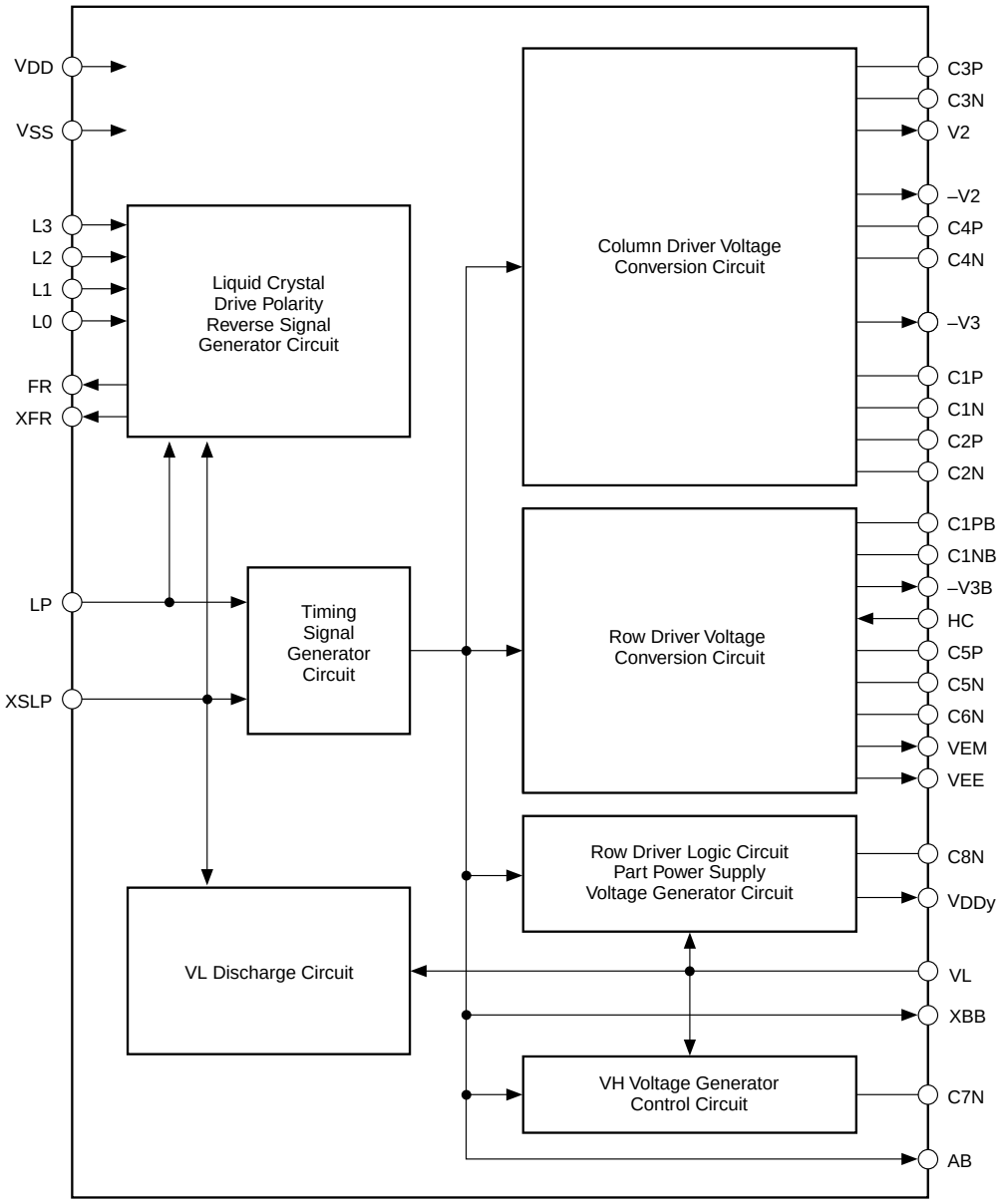


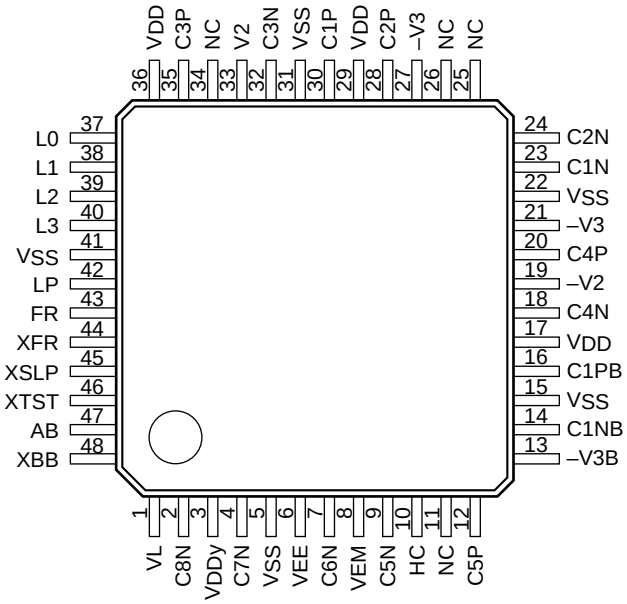
Figure 1: Block Diagram

Explanation of Block Diagram

- Liquid Crystal Drive Polarity Reverse Signal Generator Circuit
  This circuit generates the reverse polarity signal FR from the 1H period pulse signal LP. Pins L0 to L3 can be used to set the polarity reversal interval to 2H to 17H. Moreover, so that it will be possible to drive the top and bottom screens in a 2-screen drive panel in opposite phases, this IC outputs two signals with opposite polarities of each other (FR, XFR).
- Timing Signal Generator Circuit
  This circuit generates the clock for the charge pump from the 1H period pulse signal LP. When the display off control signal XSLP is set to the V_{SS} level, the clock stops and the voltage converter operation stops.
- Column Driver Voltage Conversion Circuit
  This circuit generates the V_2, $-V_2$, and $-V_3$ voltage levels required for column driving.
- Row Driver Voltage Conversion Circuit
  This generates the voltage (V_{EE}) required for generating the power supply voltages (V_H, V_L) required for the row drivers. Using V_{DD} as the reference, this generates either a $5\times$ or $6\times$ voltage level in the negative direction relative to the input power supply voltage. A terminal can be used to switch between the step-up modes. The contrast adjustment function is performed through the use of an external emitter follower circuit to adjust V_{EE} to generate VL.
- Row Driver Logic Circuit Part Power Supply Voltage Generator Circuit
  This generates the power supply voltage (V_{DDy}) required by the row driver logic circuit part. This generates a voltage that is higher than the voltage level V_L by an amount equal to V_{DD}–V_{SS}.
- V_H Voltage Generator Control Circuit
  This is a circuit for generating the power supply voltage (V_H) required for the row driver. The V_H voltage can be generated by an external MOS transistor and this circuit.
- V_L Discharge Circuit
  At power off or display off, this circuit discharges the charge remaining on the row driver negative voltage level-side power supply voltage terminal (V_L).

TERMINAL FUNCTIONS

Terminal Layout Diagram



Terminal No.	Terminal Name	Terminal No.	Terminal Name	Terminal No.	Terminal Name	Terminal No.	Terminal Name
1	V_L	13	$-V_{3B}$	25	—	37	L0
2	C8N	14	C1NB	26	—	38	L1
3	V_{DDy}	15	V_{SS}	27	$-V_3$	39	L2
4	C7N	16	C1PB	28	C2P	40	L3
5	V_{SS}	17	V_{DD}	29	V_{DD}	41	V_{SS}
6	V_{EE}	18	C4N	30	C1P	42	LP
7	C6N	19	$-V_2$	31	V_{SS}	43	FR
8	VEM	20	C4P	32	C3N	44	XFR
9	C5N	21	$-V_3$	33	V_2	45	XSLP
10	HC	22	V_{SS}	34	—	46	XTST
11	—	23	C1N	35	C3P	47	AB
12	C5P	24	C2N	36	V_{DD}	48	XBB

Explanation of Terminals

Liquid Crystal Drive Polarity Reverse Signal Generator Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
L0 to L3	I	37 to 40	1 to 4	Polarity reverse time setting terminals. These are the input terminals for setting the polarity reverse time. The time can be set in the range of 2H to 17H.
FR	O	43	7	Polarity reverse forward phase signal terminal. This terminal outputs the signal that is generated by the polarity reverse signal generating circuit.
XFR	O	44	8	Polarity reverse signal reverse phase terminal. This outputs the signal that is in the reverse phase from the polarity reverse forward phase signal terminal.

Timing Signal Generator Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
LP	I	42	6	Display data latch pulse input terminal. This is the input terminal for generating the charge pump clock and the polarity reverse signal. It is necessary to input into this terminal a pulse signal with a period of 1H.
XSLP	I	45	9	The display off control signal terminal. Setting this terminal to the VSS level stops the clock and stops the operations of the voltage converter.

Column Driver Voltage Conversion Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
C3P	(O)	35	43	The positive-side connection terminal for the flying capacitor CP3 for generating the V_2 output voltage.
C3N	(O)	32	41	The negative-side connection terminal for the flying capacitor CP3 for generating the V_2 output voltage.
V_2	O	33	42	V_2 output voltage terminal.
C4P	(O)	20	31	The positive-side connection terminal for the flying capacitor CP4 for generating the $-V_2$ output voltage.
C4N	(O)	18	29	The negative-side connection terminal for the flying capacitor CP4 for generating the $-V_2$ output voltage.
$-V_2$	O	19	30	$-V_2$ output voltage terminal.
C1P	(O)	30	39	The positive-side connection terminal for the flying capacitor CP1 for generating the $-V_3$ output voltage.
C1N	(O)	23	34	The negative-side connection terminal for the flying capacitor CP1 for generating the $-V_3$ output voltage.
C2P	(O)	28	37	The positive-side connection terminal for the flying capacitor CP2 for generating the $-V_3$ output voltage.
C2N	(O)	24	35	The negative-side connection terminal for the flying capacitor CP2 for generating the $-V_3$ output voltage.
$-V_3$	O	21, 27	32, 36	$-V_3$ output voltage terminal.

Row Driver Voltage Conversion Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
C1PB	(O)	16	27	The positive-side connection terminal for the flying capacitor CP1B and CP8 for generating the $-V_{3B}$ output voltage.
C1NB	(O)	14	25	The negative-side connection terminal for the flying capacitor CP1B for generating the $-V_{3B}$ output voltage.
$-V_{3B}$	O	13	24	The negative V_{3B} output voltage terminal. This is an output terminal equipped as the middle voltage level for generating the V_{EE} output voltage.
HC	I	10	22	The step-up mode select terminal. When this terminal is tied V_{SS}, then the chip is put into 5 X step-up mode. However, when it is connected to –3B, the chip is set to 6 X step-up mode.
C5P	(O)	12	23	The positive-side connection terminal for the flying capacitor CP5 and CP6 for generating the V_{EM} output voltage.
C5N	(O)	9	21	The negative-side connection terminal for the flying capacitor CP5 for generating the V_{EM} output voltage.
VEM	O	8	20	The V_{EM} output voltage terminal. This is an output terminal equipped as the middle voltage level for generating the V_{EE} output voltage.
C6N	(O)	7	19	The negative-side connection terminal for the flying capacitor CP6 for generating the V_{EE} output voltage. (The positive-side of CP6 is C5P.)
V_{EE}	O	6	18	The V_{EE} output voltage terminal. By changing the HC terminal interconnection method, it is possible to switch between the 5-level step-up mode and the 6-level step-up mode.

Common Driver Logic Circuit Part Power Supply Voltage Generator Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
C8N	(O)	2	14	The negative-side connection terminal for the flying capacitor CP8 for generating the V_{DDy} output voltage. The positive connection terminal for CP8 is the same as C1PB.
V_{DDy}	O	3	15	The row driver logic circuit part power supply output terminal. This generates the power supply voltage required for the row driver logic circuit part. The output is higher than the V_L level in the positive direction by an amount equal to the difference between V_{DD} and V_{SS}.

VH Voltage Generator Control Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
AB	O	47	11	The V_H output voltage generator clock terminal A. This is the clock output terminal for the external N-channel MOS transistor control.
XBB	O	48	12	The V_H output voltage generator clock terminal B. This is the clock output terminal for the external P-channel MOS transistor control.
C7N	(O)	4	16	The negative-side connection terminal for the flying capacitor CP7 for generating the V_H output voltage. The positive-side connection terminal corresponds to the external transistor.

VL Discharge Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
VL	I	1	13	This is the row driver negative voltage level power supply voltage terminal. The V_L signal that is used to adjust the contrast is input to this terminal. This serves as the power supply for the V_H voltage generator control circuit. XSLP operates the discharge circuit at the VSS level.

The Test Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
XTST	I	46	10	This is a test terminal. Insure that this terminal is always tied to the V_{DD} level.

Power Supply Terminals <Note 1>

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
V_{DD}	I	17, 29, 36 *1	28, 38 44 *1	Input power supply terminals (positive).
V_{SS}	I	5, 15, 22, 31, 41 *1	5, 17, 26 33, 40 *1	Input power supply terminals (negative).

Note: *1 Please connect these power supply terminals externally.

EXPLANATIONS OF FUNCTIONS

Overview of Operation

The SCI7500F0A is a power supply IC for operating the 4-line simultaneous selection method MLS (Multi Line Selection) driver LCDs. Using its CMOS charge pump-type high-efficiency voltage converter circuit, this chip can produce all of the bias voltages necessary for a 4-line MLS driving based on a single 3.0 V power supply.

The voltage levels produced are as follows:

- The liquid crystal drive power supply voltages required for the column drivers ($V_3 = V_{DD}$, V_2, $V_C = V_{SS}$, $-V_2$, $-V_3$).
- The liquid crystal drive power supply voltages required for the row drivers (V_H, $V_C = V_{SS}$, V_L).
- The power supply voltages for the logic circuits of the row driver (V_{DDy}).

However, the row driver low voltage-side power supply voltage (V_L) requires an external bipolar transistor for adjusting the contrast. Moreover, external MOS transistors (2SK***, 2SJ***) are required for generating the row driver high-level power supply voltage (V_H).

Depending on a terminal setting, the chip can switch between 6 X step-up mode and 5 X step-up mode, with 1/240 duty and 1/200 duty, respectively. Consequently, it is possible to obtain the required voltages with maximum efficiency.

An example of a system structure diagram for the power supply interconnections is given below:

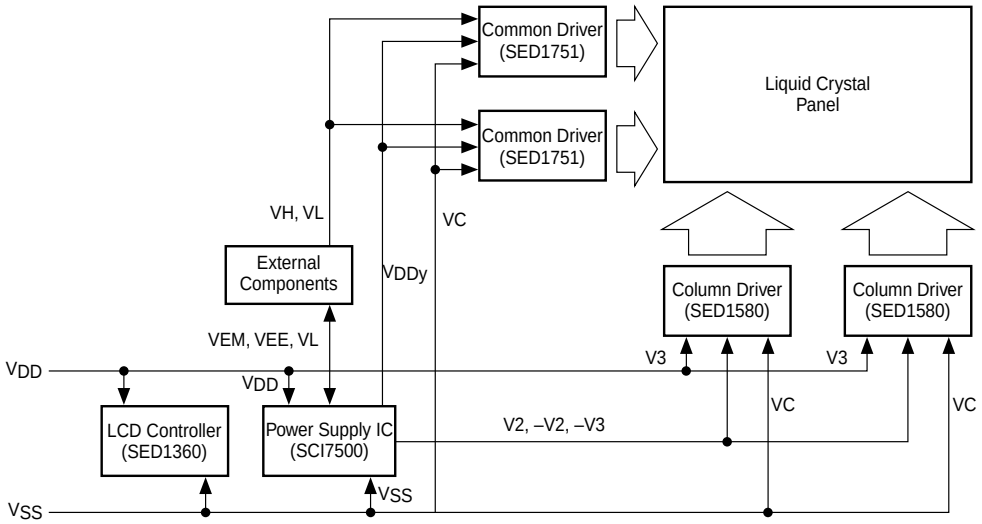


Figure 2: The System Configuration

The relationships between voltage levels in the system shown in Figure 2 are given in the table below.

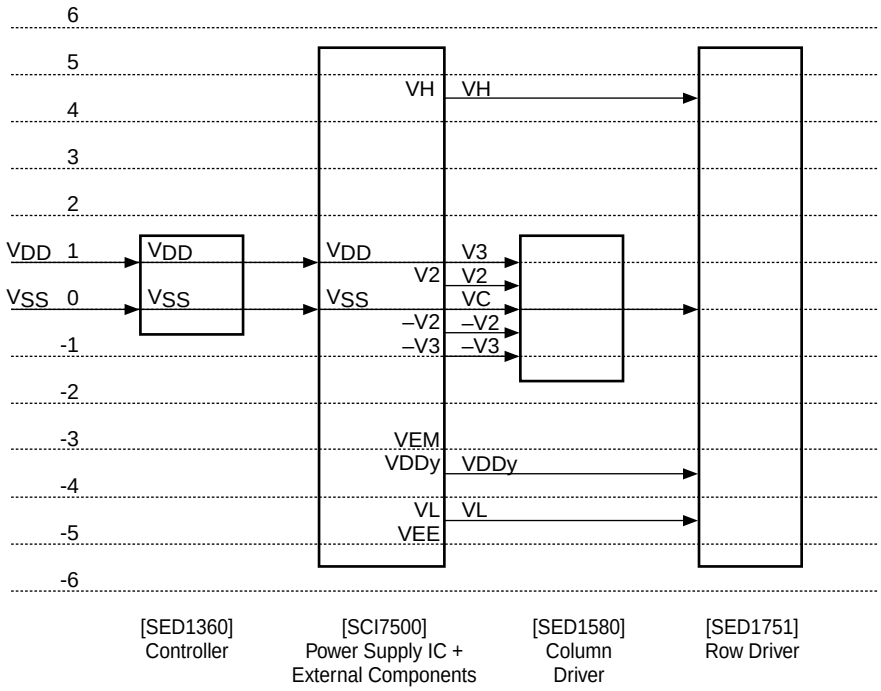


Figure 3: The Relationships Between Voltages Within the System (in 6 × step-up mode)

The logical formulas for each of the voltage levels is as given below:

When in 6 × step-up mode (when HC is connected to –V_{3B}).		**When in 5 × step-up mode (when HC is connected to V_{SS}).**	
Logical Formula	**Voltage level when V_{DD} = 3.0V and V_{SS} = 0V**	**Logical Formula**	**Voltage level when V_{DD} = 3.0V and V_{SS} = 0V**
$V_H = -V_L = 5 (V_{DD}-V_{SS})-\alpha$	15.0–α	$V_H = -V_L = 4 (V_{DD}-V_{SS})-\alpha$	12.0–α
$V_3 = V_{DD}-V_{SS}$	3.0	$V_3 = V_{DD}-V_{SS}$	3.0
$V_2 = 1/2 (V_{DD}-V_{SS})$	1.5	$V_2 = 1/2 (V_{DD}-V_{SS})$	1.5
$V_C = V_{SS}$	0	$V_C = V_{SS}$	0
$-V_2 = -1/2 (V_{DD}-V_{SS})$	–1.5	$-V_2 = -1/2 (V_{DD}-V_{SS})$	–1.5
$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0	$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0
$V_{EM} = -3 (V_{DD}-V_{SS})$	–9.0	$V_{EM} = -2 (V_{DD}-V_{SS})$	–6.0
$V_{DDy} = -4 (V_{DD}-V_{SS}) + \alpha$	–12.0 + α	$V_{DDy} = -3 (V_{DD}-V_{SS}) + \alpha$	–9.0 + α
$V_L = -5 (V_{DD}-V_{SS}) + \alpha$	–15.0 + α	$V_L = -4 (V_{DD}-V_{SS}) + \alpha$	–12.0 + α
$V_{EE} = -5 (V_{DD}-V_{SS})$	–15.0	$V_{EE} = -4 (V_{DD}-V_{SS})$	–12.0

Where α = variable ≥ 0 (contrast adjustment)

The Liquid Crystal Drive Polarity Reverse Signal Generator Circuit

This circuit produces the polarity reverse signal from the 1H period pulse signal LP. Terminals L0 to L3 can be used to set the polarity reversed period in the range of 2H to 17H. So that the upper and lower screens can be driven in mutually opposite phases when a 2-screen drive panel is used, this IC outputs two signals with mutually opposing polarities (i.e. with opposite phases) from the FR and the XFR terminals. The timing of the output transitions is synchronized with the falling edge of the LP signal.

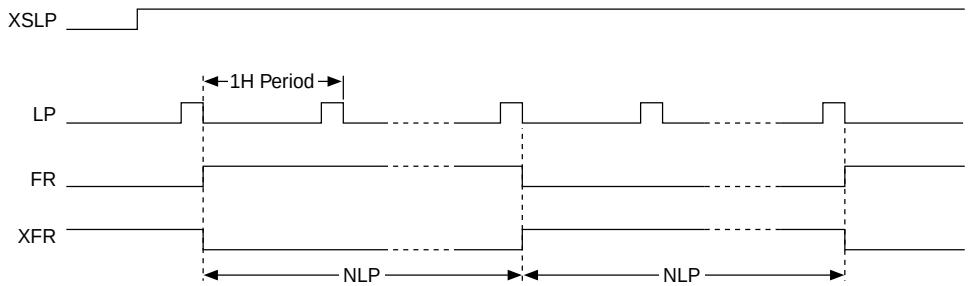


Figure 4: LP and FR Signal Timing Diagram

The relationship between the NLP during the polarity reversed interval and the settings of terminals L0 to L3 is as shown below:

Terminal Settings While Polarity is Reversed				Function		
L3	L2	L1	L0	Time	NLP	
0	0	0	0	17H	LP Signal	17th pulse
			1	2H	LP Signal	2nd pulse
		1	0	3H	LP Signal	3rd pulse
			1	4H	LP Signal	4th pulse
	1	0	0	5H	LP Signal	5th pulse
			1	6H	LP Signal	6th pulse
		1	0	7H	LP Signal	7th pulse
			1	8H	LP Signal	8th pulse
1	0	0	0	9H	LP Signal	9th pulse
			1	10H	LP Signal	10th pulse
		1	0	11H	LP Signal	11th pulse
			1	12H	LP Signal	12th pulse
	1	0	0	13H	LP Signal	13th pulse
			1	14H	LP Signal	14th pulse
		1	0	15H	LP Signal	15th pulse
			1	16H	LP Signal	16th pulse

The Timing Signal Generator Circuit

This generates the clock for the charge pump from the 1H period pulse signal LP. When the display off control signal XSLP is set to Vss, this clock stops and the IC voltage converter operation halts. The VH output voltage generator clocks AB and XBB are also produced by this circuit.

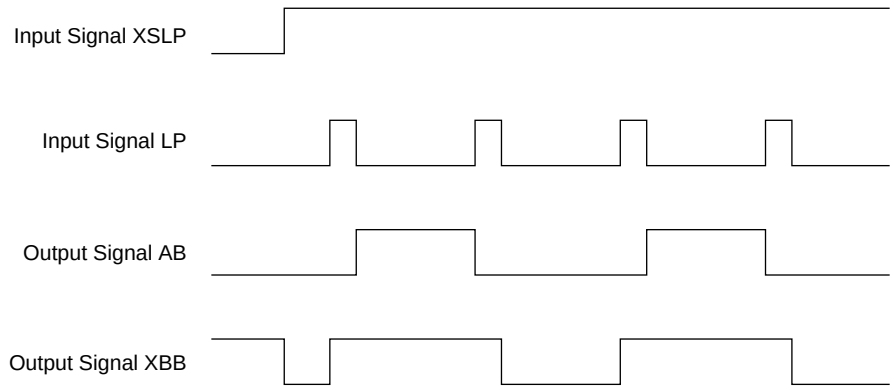


Figure 5: The AB and XBB Signal Output Timing

The Voltage Converter Circuit

The voltage converter circuit comprises a CMOS charge pump-type DC/DC converter. The relational diagram of the voltage converter circuits within this IC is as shown below. The numbers within parentheses in the diagram correspond to the number in "Figure 1: Block Diagram."

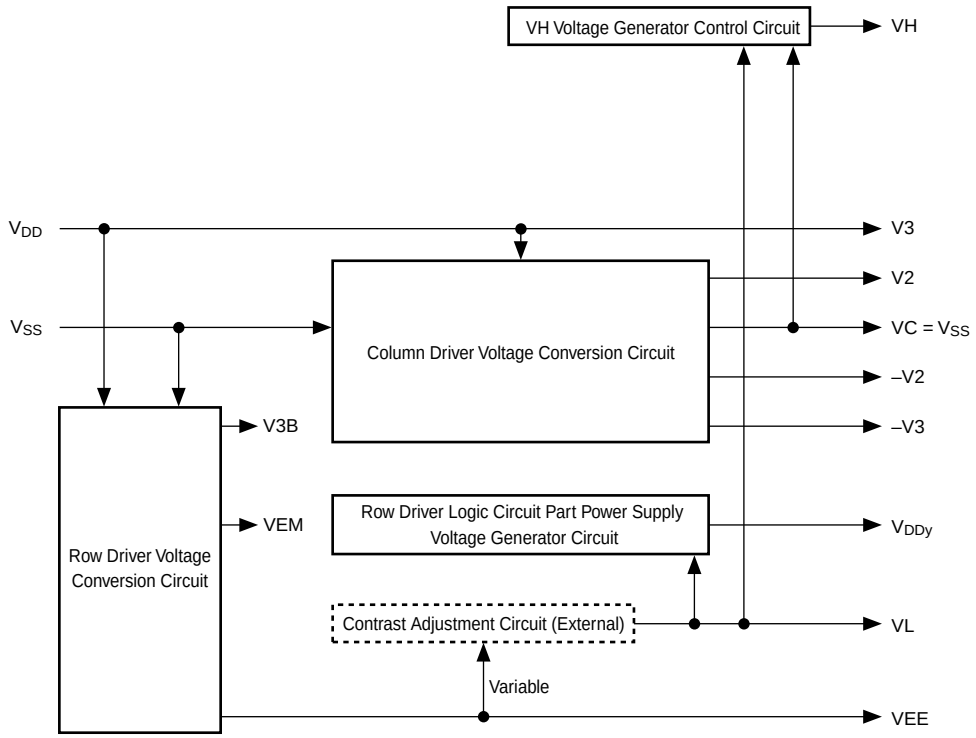


Figure 6: A Relational Diagram of the Voltage Converter Circuits

Logical Formulas for the Various Voltage Levels

When in 6 × step-up mode (when HC is connected to –V3B).		When in 5 × step-up mode (when HC is connected to VSS).	
Logical Formula	**Voltage level when VDD = 3.0V and VSS = 0V**	**Logical Formula**	**Voltage level when VDD = 3.0V and VSS = 0V**
$V_H = -V_L = 5\ (V_{DD}-V_{SS})-a$	15.0–α	$V_H = -V_L = 4\ (V_{DD}-V_{SS})-\alpha$	12.0–α
$V_3 = V_{DD}-V_{SS}$	3.0	$V_3 = V_{DD}-V_{SS}$	3.0
$V_2 = 1/2\ (V_{DD}-V_{SS})$	1.5	$V_2 = 1/2\ (V_{DD}-V_{SS})$	1.5
$V_C = V_{SS}$	0	$V_C = V_{SS}$	0
$-V_2 = -1/2\ (V_{DD}-V_{SS})$	–1.5	$-V_2 = -1/2\ (V_{DD}-V_{SS})$	–1.5
$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0	$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0
$V_{EM} = -3\ (V_{DD}-V_{SS})$	–9.0	$V_{EM} = -2\ (V_{DD}-V_{SS})$	–6.0
$V_{DDy} = -4\ (V_{DD}-V_{SS}) + \alpha$	–12.0+ α	$V_{DDy} = -3\ (V_{DD}-V_{SS}) + \alpha$	–9.0 + α
$V_L = -5\ (V_{DD}-V_{SS}) + \alpha$	–15.0+ α	$V_L = -4\ (V_{DD}-V_{SS}) + \alpha$	–12.0 + α
$V_{EE} = -5\ (V_{DD}-V_{SS})$	–15.0	$V_{EE} = -4\ (V_{DD}-V_{SS})$	–12.0

Where α = variable ≥ 0 (contrast adjustment)

The capacitors for the charge pump can be of two different types: the flying capacitors which transition between a charged state and a discharged state, and the storage capacitor that stores charge. The clock that controls the state changes in the flying capacitors is generated by the timing signal generator circuit from the display data latch pulse input terminal LP. The operating frequency f sw of the flying capacitor is calculated as follows:

$f_{SW} = 1/(2 \times t_{CLP})$
Where t CLP is the LP frequency.

The voltage logic that is biased by both ends of the flying capacitors and storage capacitors is as shown below: (Reference “10. Example of Connections (Reference)” regarding recommended capacitance values and connection methods for the capacitors.)

Flying Capacitors and Storage Capacitors

Capacitor Name		Voltage logic formula biased by both ends of the capacitors		Column side/ Row side
		6 × step-up mode	5 × step-up mode	
Flying Capacitor	CP1	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Column Side
	CP2	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	
	CP3	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CP4	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CP1B	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Row side
	CP5	$2\ (V_{DD}-V_{SS})$	$V_{DD}-V_{SS}$	
	CP6	$2\ (V_{DD}-V_{SS})$	$2\ (V_{DD}-V_{SS})$	
	CP7	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	
	CP8	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	
Storage Capacitor	CB1	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Column side
	CB3	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CB4	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CB1B	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Row side
	CB5	$2\ (V_{DD}-V_{SS})$	$V_{DD}-V_{SS}$	
	CB6	$2\ (V_{DD}-V_{SS})$	$2\ (V_{DD}-V_{SS})$	
	CB7	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	
	CB8	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	
	CVL	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	

Where α = variable ≥ 0 (contrast adjustment)

In the column driver voltage converter circuit either flying capacitor CP1 or CP2 can be omitted. When the panel is smaller than a 6.3 inch VGA panel, or if one wishes to sacrifice image quality to save cost, one may consider this omission; however, the output impedance will increase and will be outside of what is indicated in "Electrical Characteristics," and thus we recommend that you experimentally confirm the structure for each application.
Switching between the step-up modes in the row driver voltage converter circuits can be done by setting the HC terminal. When the HC terminal is connected to –V3B, then the system will be in 6 × step-up mode, but when the HC terminal is connected to the VSS terminal, then the system will be in 5 × step-up mode. Furthermore, by connecting the –V3 terminal to the –V3B terminal, it is possible to omit the flying capacitor CP1B and storage capacitor CP1B. However, when these capacitors are omitted, the output impedance will increase and will be outside of what is indicated in "Electrical Characteristics," and thus we recommend that you experimentally confirm the structure for each application.

The Contrast Adjustment Circuit

The row driver negative voltage-side power supply voltage VL can be adjusted and generated by an external emitter follower circuit using VEE. The contrast adjustment function is shown in the circuit connection example below:

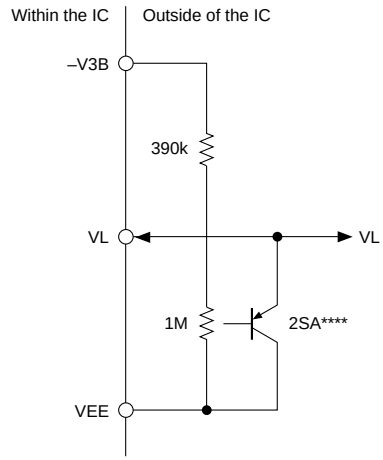


Figure 7: Contrast Adjustment Circuit

The VH Voltage Generator Control Circuit

The row driver positive voltage-side power supply voltage VH can be generated from this circuit and the VH output voltage generator clocks AB, XBB, and external components. This is shown in the circuit connection example below.

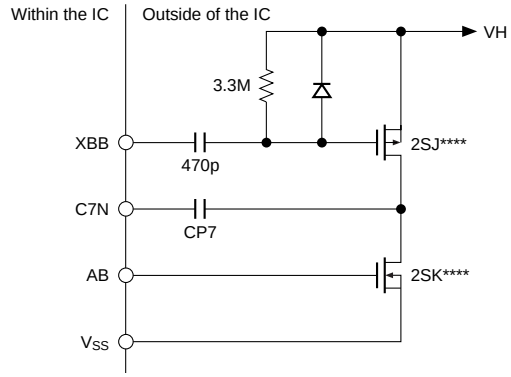


Figure 8: Example of Circuit Connections for Generating the VH Voltage

The VL Discharge Circuit

When XSLP is put to the VSS level, the VL discharge circuit within the IC is triggered, and residual charge at the row driver negative voltage-side power supply voltage terminal VL is discharged to the VSS level. The VL voltage adjusted for the contrast must be input to the VL terminal. (See "The Contrast Adjustment Circuit.")

The VH Discharge Circuit

When XSLP is put to the VSS level, the residual charge at the row driver positive voltage-side power supply terminal VH can be discharged to the VSS level through an external MOS transistor. An example circuit connection is shown below.

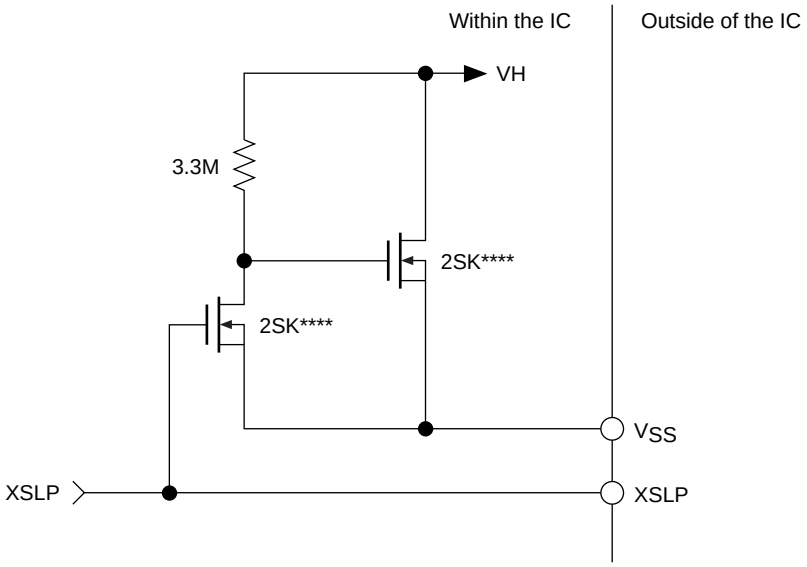


Figure 9: The VH Discharge Circuit

ELECTRICAL CHARACTERISTICS

The Absolute Maximum Ratings

V_{SS} = 0V

Item	Signal	Rated Value		Units	Notes
		Minimum	Maximum		
Input power supply voltage 1	V_{DD}	—	3.7	V	V_{DD} terminal
Input power supply voltage 2	V_L	V_{EE}-0.3	0.3	V	V_L terminal
Input terminal voltage	V_I	–0.3	V_{DD} + 3.0	V	The L3 to L0, LP, XSLP, and XTST terminals
Input current	I_{DD}	—	10	mA	V_{DD}, V_L
Output current 1	I_{V2}	—	6	mA	V_2 terminal
Output current 2	I-V_2	—	6	mA	-V_2 terminal
Output current 3	I-V_3	—	5	mA	-V_3 terminal
Output current 4	I V_{EE}	—	1	mA	V_{EE} terminal
Output current 5	I V_{DDy}	—	0.1	mA	V_{DDy} terminal
Allowable loss	Pd	—	100	mW	Ta ≤ 55 °C
Operating temperature	Topr	–30	85	°C	—
Storage temperature	Tstg	–55	150	°C	—
Soldering temperature and time	Tsol	—	260 × 10	°C × S	At the lead

Notes: *1 Do not apply a voltage from the outside to the output terminals nor to the capacitor connection terminals.

Notes: *2 Operating failures and/or permanent damage may occur if this chip is used under conditions exceeding the absolute maximum ratings listed above. Moreover, the reliability of this chip may be dramatically compromised even if the chip continues to function normally for a time.

DC Characteristics

When not otherwise specified: Ta = –30°C to +85°C, V_{SS} = 0V, 6 × step-up, $V_L = V_{EE} + 0.6V$, Standard connections <Note 1>, LP period = 69µs, LP width = 1µs.

Item	Symbol	Parameters		Standards Min	Standards Typ	Standards Max	Units	Notes
Input power supply voltage	V_{DD}	—		2.4	3.0	3.6	V	—
Input power supply voltage	V_L	—		V_{EE}+0.6	—	$–V_3$	V	—
High level input voltage	V_{IH}	Applicable terminals: LP, XSLP, L0 to L3, XTST V_{DD} = 2.4 to 3.6V		0.8V_{DD}	—	V_{DD}	V	—
Low level input voltage	V_{IL}			0	—	0.2V_{DD}	V	—
Input leakage current	I_{LIN}	$V_{SS} \le V_I \le V_{DD}$, V_{DD} = 2.4 to 3.6V		–0.5	—	0.5	µA	—
V_2 output voltage	V_2	I_O = 2mA (to V_{SS})	V_{DD} = 2.4V	1.148	—	1.2	V	—
			V_{DD} = 2.7V	1.298	—	1.35		
$–V_2$ output voltage	$–V_2$	I_O = 2mA (from V_{SS})	V_{DD} = 2.4V	–1.2	—	–1.120	V	2
			V_{DD} = 2.7V	–1.35	—	–1.272		
$–V_3$ output voltage	$–V_3$	I_O = 1mA (from V_{SS})	V_{DD} = 2.4V	–2.4	—	–2.340	V	2
			V_{DD} = 2.7V	–2.7	—	–2.644		
V_{EE} output voltage	V_{EE}	I_O = 0.4mA (from V_{SS})	V_{DD} = 2.4V	–12.0	—	–11.2	V	—
			V_{DD} = 2.7V	–13.5	—	–12.7		
V_{DDy} output voltage	V_{DDy}	I_O = 0.02mA (to V_L)	V_{DD} = 2.4V	V_L + 2.33	—	V_L + 2.40	V	—
			V_{DD} = 2.7V	V_L + 2.63	—	V_L + 2.70		
Output resistor 1	R_{ON1}	Applicable terminal: C7N I_{OH} = –0.2mA	V_{DD} = 2.4V	—	—	16	Ω	3
			V_{DD} = 2.7V	—	—	15		
Output resistor 1	R_{ON2}	Applicable terminal: C7N I_{OH} = 0.2mA	V_{DD} = 2.4V	—	—	21	Ω	3
			V_{DD} = 2.7V	—	—	20		
High level output voltage	V_{OH}	Applicable terminals: XBB, AB, FR, XFR V_{DD} = 2.4 to 3.6V	I_{OH} = –20µA	V_{DD}–0.1	—	V_{DD}	V	—
Low level output voltage	V_{OL}		I_{OL} = 20µA	0	—	0.1	V	—
Consumption	I_{OPR5}	5 × step-up, no load V_{DD} = 3.0V		—	250	330	µA	—
Current	I_{OPR6}	6 × step-up, no load V_{DD} = 3.0V		—	340	470	µA	—
Static current	I_Q	V_{DD} = 2.4 to 3.6V, XSLP = 0V		—	—	5	µA	—
Step-up power converter efficiency	Peff	6 × step-up, V_{DD} = 3.0V The load conditions were as follows: V_2: I_O = 2mA $–V_2$: I_O = 2mA $–V_3$: I_O = 1mA V_L: I_O = 0.4mA V_{DDy}: I_O = 0.02mA		—	88	—	%	—

Notes
1. For standard connections, see “Example of Connections (Reference).”
2. Measured in a state where negative charges were not applied to -V_2 and -V_3 simultaneously.
3. The measurement circuits and timing of the output resistance 1 R_{ON1}, and output resistance 2 R_{ON2} are as shown below.

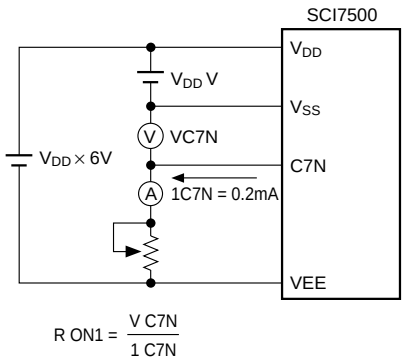


Figure 10: The RON1 Measurement Circuit Figure

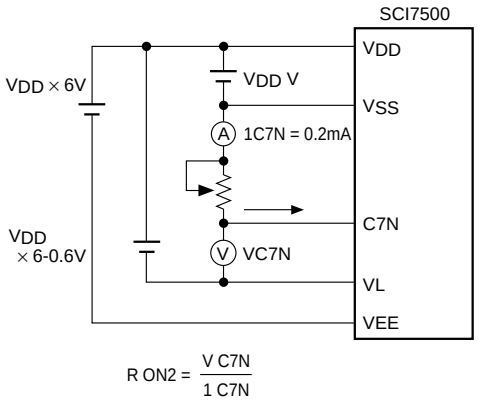


Figure 11: The RON2 Measurement Circuit

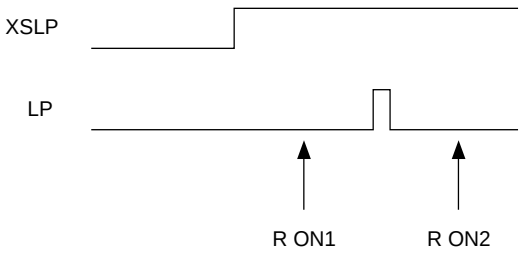


Figure 12: The Measurement Timing using RON1 and RON2

AC Characteristics

The AC test parameters:

- Input voltage level: V_{IH} = 0.8 V_{DD} V
  V_{IL} = 0.2 V_{DD} V
- Input signal rise time: Tr = max 10 ns
- Input signal fall time: Tf = max 10 ns
  V_{DD} = 2.4 to 3.6 V
  V_{SS} = 0 V
  Ta = –30 to 85 °C

Input Timing Characteristics

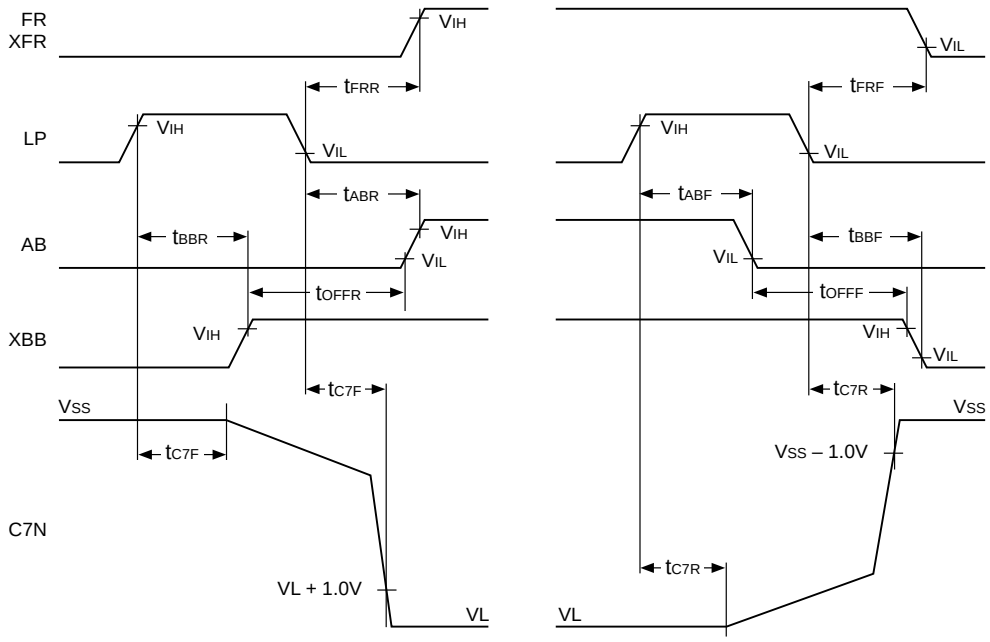
Item	Symbol	Ratings			Units	Notes
		Min	Typ	Max		
LP Period	t_{CLP}	50	65 to 90	125	µs	*1
LP Pulse Width	t_{WLP}	70	—	2000	ns	

Note *1 While the chip continues to function with LP pulse widths in excess of 2000 ns, the wider the LP pulse width, the higher the output impedance of the various output voltages. For this IC, although we are recommending inputting of LP signals through the LP pin as the basic clock, inputting of other signals through the LP pin will also provide the same characteristics as far as the signals being input can satisfy the above specifications.

(Reference) LP Period

Frame Frequency	Duty	LP Period
40	1/200	125 µs
60	1/200	83 µs
60	1/240	69 µs
80	1/240	52 µs

Output Timing Characteristics



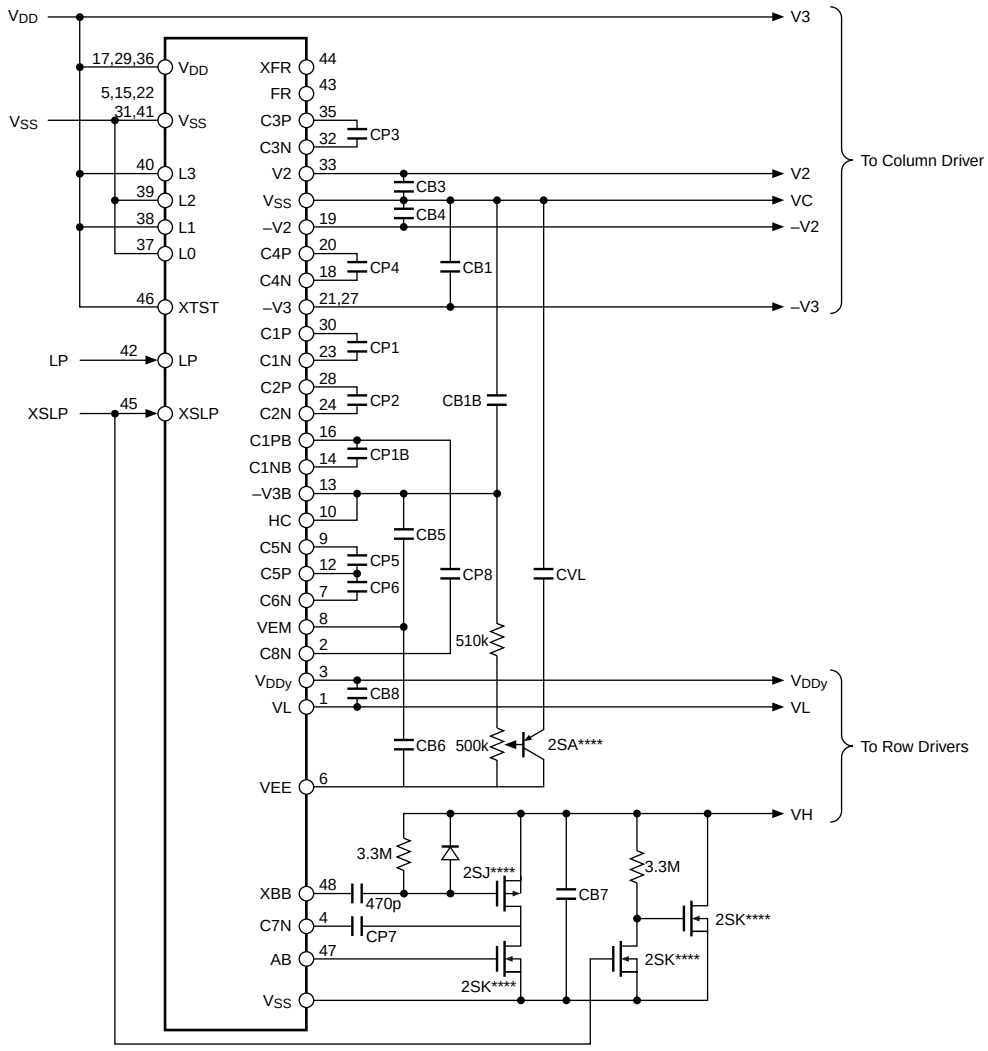
LP pulse width = 1µs, 6 X step-up voltage, VL = VEE + 0.6V, Standard Connections

Item	Signal	Applicable Terminals	Load Conditions	Rated Values		Units
				Min	Max	
FR signal rise delay time	t_{FRR}	FR, XFR	C_L = 50pF	330	3300	ns
FR signal fall delay time	t_{FRF}	FR, XFR		330	3300	ns
AB signal rise delay time	t_{ABR}	AB	*2	230	2000	ns
AB signal fall delay time	t_{ABF}	AB		180	1900	ns
XBB signal rise delay time	t_{BBR}	XBB		130	1100	ns
XBB signal fall delay time	t_{BBF}	XBB		280	3200	ns
Rising edge output phase differential time	t_{OFFR}	AB, XBB		1000	2400	ns
Falling edge output phase differential time	t_{OFFF}	AB, XBB		1000	2200	ns
C7N signal falling edge delay time	t_{C7F}	C7N	*3	270	2400	ns
C7N signal rising edge delay time	t_{C7R}	C7N		490	3800	ns

Note *2 When 2SJ185, 2SK1399 (manufactured by NEC) are used.
Note *3 With a load with standard connections.

EXAMPLE OF CONNECTIONS (REFERENCE)

Standard Connections for the 6 × step-up mode.

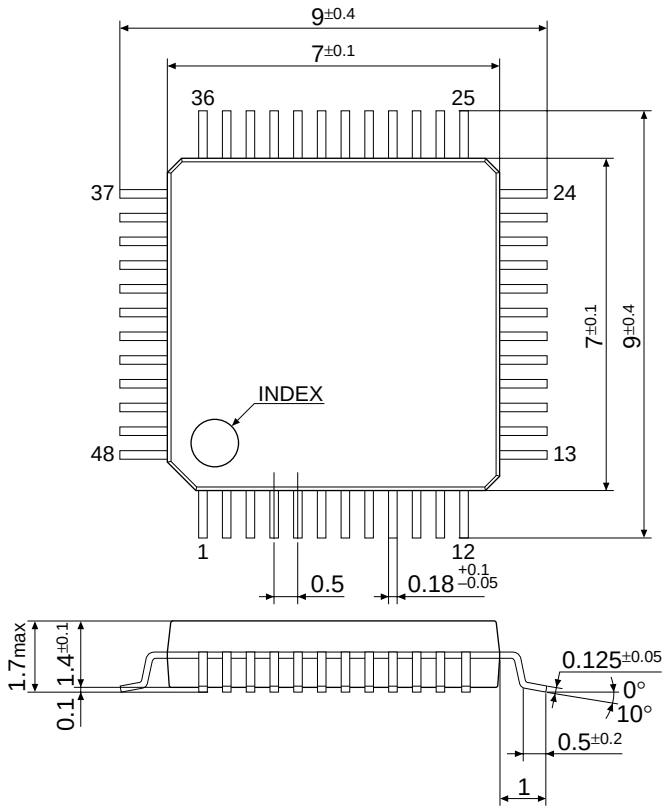


Capacitor Name	Capacitance Value (μF)	Capacitor Name	Capacitance Value (μF)
CP1	4.7	CB1	4.7
CP2	4.7	CB3	4.7
CP3	4.7	CB4	4.7
CP4	4.7	CB5	1.0
CP5	1.0	CB6	1.0
CP6	1.0	CB7	1.0
CP7	1.0	CB8	0.1
CP8	0.1	CB1B	4.7
CP1B	4.7	CVL	1.0

The capacitance values for the capacitors are the recommended value for a 6.3 inch VGA liquid crystal panel. The characteristics shown in “Electrical Characteristics” are the characteristics obtained when capacitors with the values shown above are used. Consequently, while one may consider reducing the capacitance values of these capacitors when a liquid crystal panel smaller than a 6.3-inch VGA screen is used, in such a case the output impedance would increase, and thus we recommend experimental verification for each product type, and that the capacitance values be set such that the liquid crystal drive voltages are stable.

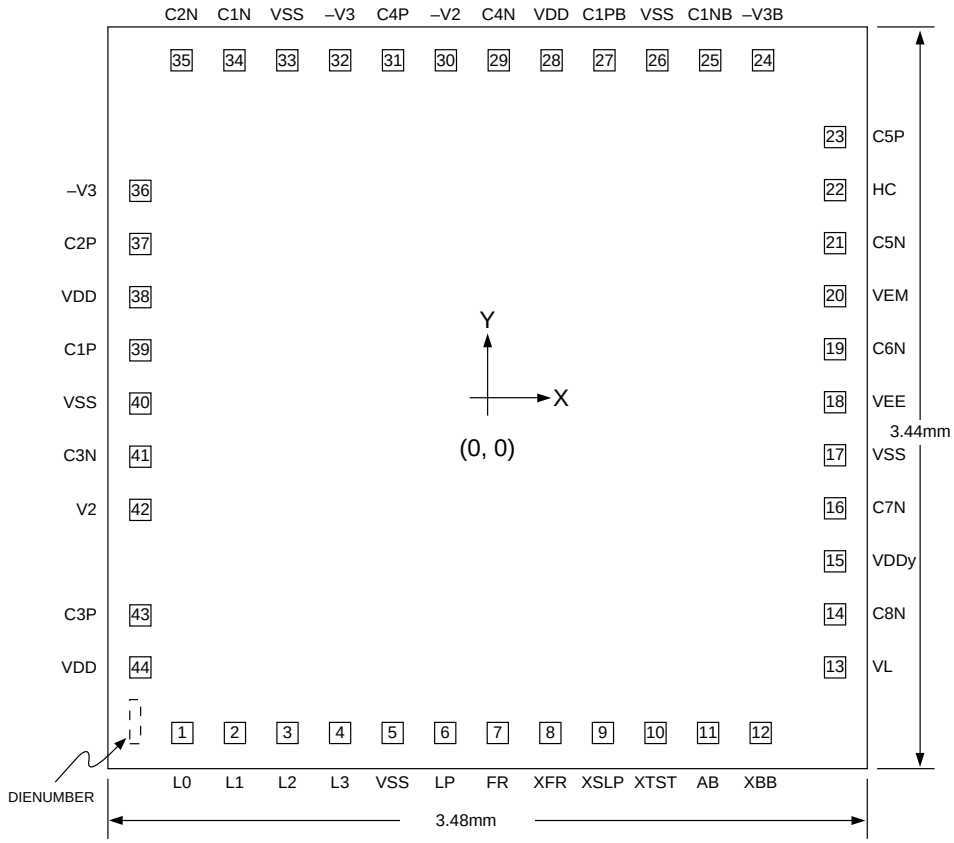
EXTERNAL DIMENSIONS (REFERENCE)

Note: These dimensions are subject to change without notice.



Plastic QFP12-48 pin

EXTERNAL SHAPE OF THE CHIP (SCI7500D0A)



PAD layout

Chip size:	3.48mm × 3.44mm
Chip thickness:	400μm ± 30μm
PAD hole size:	100μm × 100μm
Substrate potential:	V_{DD}
DIE number:	F7500D0A

COORDINATES OF RESPECTIVE PAD CENTERS

Unit: µm

PAD No.	PAD name	X	Y
1	L0	–1431.2	–1554.4
2	L1	–1191.2	
3	L2	–951.2	
4	L3	–711.2	
5	VSS	–471.2	
6	LP	–280.8	
7	FR	–40.8	
8	XFR	199.2	
9	XSLP	439.2	
10	XTST	679.2	
11	AB	919.2	
12	XBB	1159.2	
13	VL	1574.4	–1264.8
14	C8N		–1024.8
15	VDDy		–784.8
16	C7N		–544.8
17	VSS		–304.8
18	VEE		–64.8
19	C6N		175.2
20	VEM		415.2
21	C5N		655.2
22	HC		895.2

PAD No.	PAD name	X	Y
23	C5P	1574.4	1135.2
24	–V3B	1235.2	1554.4
25	C1NB	995.2	
26	VSS	755.2	
27	C1PB	475.2	
28	VDD	235.2	
29	C4N	–4.8	
30	–V2	–244.8	
31	C4P	–484.8	
32	–V3	–724.8	
33	VSS	–964.8	
34	C1N	–1204.8	
35	C2N	–1444.8	
36	–V3	–1574.4	935.2
37	C2P		655.2
38	VDD		415.2
39	C1P		175.2
40	VSS		–64.8
41	C3N		–304.8
42	V2		–544.8
43	C3P		–1024.8
44	VDD		–1264.8

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