SED1580

Contents

OVERVIEW

Description

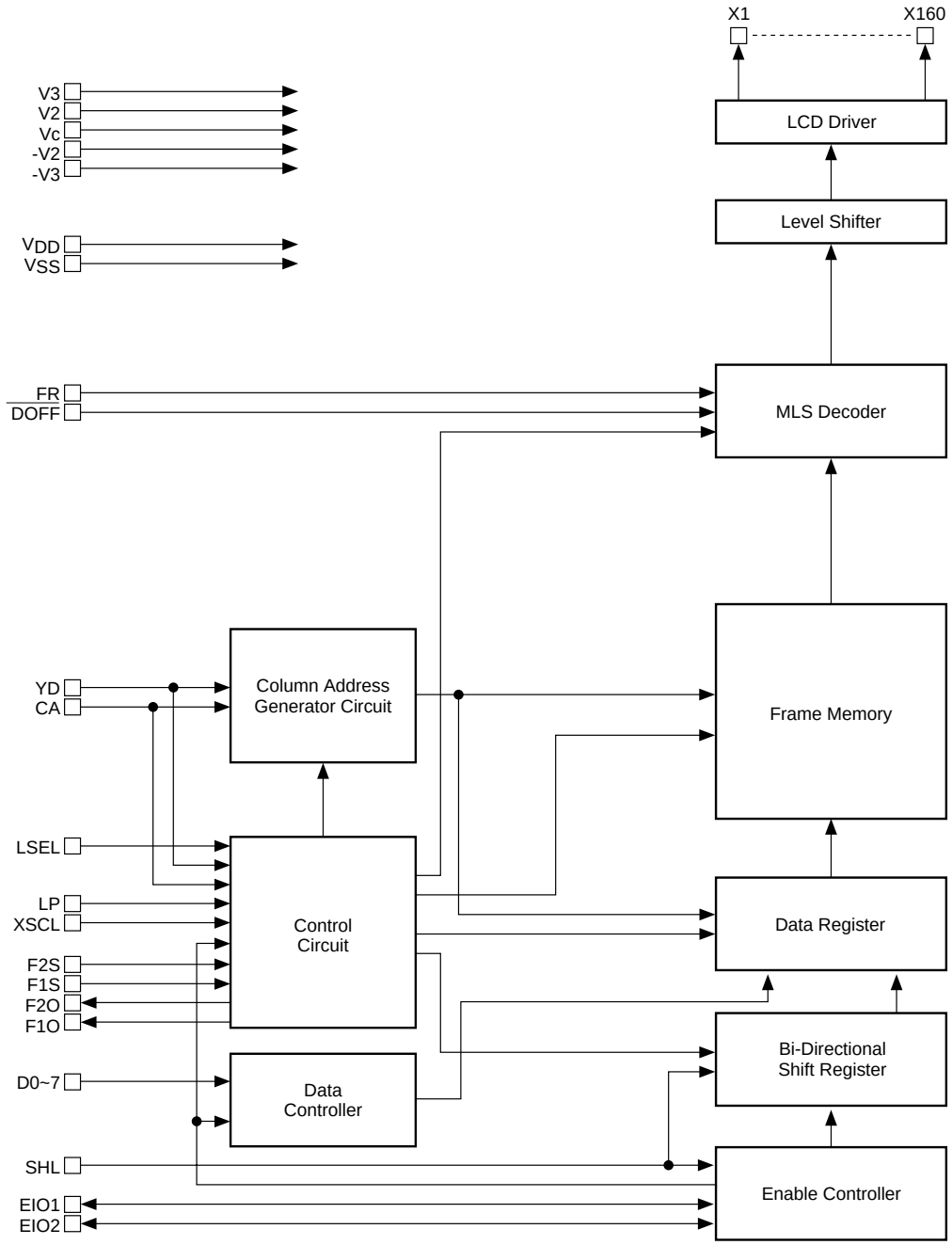
The SED1580 is a 160-output, 5-level segment (column) driver for MLS (Multi-Line Selection) driving, able to drive with both high contrast and high speed. It is used in conjunction with the SED1751. When paired with the SED1751 it can be connected to the SED1360 LCD controller.
Because the SED1580 stores display data in its internal display RAM and generates LC drive signals, display data transmission from the controller can be suspended except for when there are changes to the display, thereby enabling an ultra low power display system.
The SED1580 uses a slim package, facilitating the construction of thinner LCD panels, and the low-voltage operation of its logic power source makes it appropriate to a wide range of applications.

FEATURES

- Number of simultaneous line selects: 4 Lines
- Drive duty ratio (MAX) 1/240 duty
- LCD driver outputs 160 outputs
- Internal display RAM 160×240 bit
- Extremely low consumption current
- Power Source Voltages Logic System: 3.0 to 3.6V (Max)
  LCD System: 6.0 to 7.2V (Max)
- High speed, low power data transmission possible through the 4-bit/8-bit switchable bus enable chain method
- Non-biased display off function
- Output shift direction pin select supported
- Slim chip shape
- Shipment status:
  In CHIP form SED1580D0B
  In TCP form SED1580T0A
- This product is not designed for resistance to light or radiation

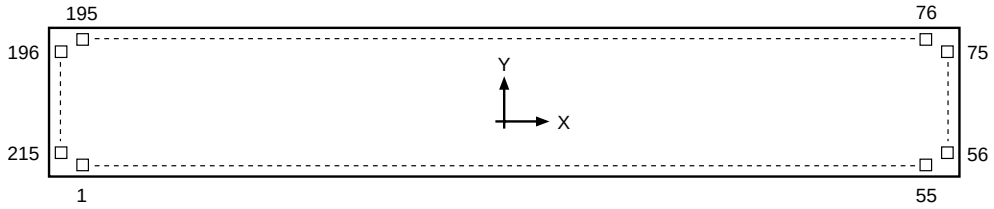
BLOCK DIAGRAM

Block Diagram



PIN CONFIGURATION

Pad Layout



Chip size 12.89 mm × 2.77 mm
Bump pitch: 103 microns (Min.)
Chip thickness: 625 microns ± 15 µm

Bump size (Unit: µm)

Pad number		
	X	Y
56 to 215	67	63
1, 7 to 16, 18 to 36, 38 to 49, 55	74	74
2 to 6, 17, 37, 50 to 54	110	74
22	110	75

Bump specifications (reference values)

Items	Specifications		
	MIN	TYP	MAX
Bump size specifications	–4 µm	Bump size	+4 µm
Bump height specifications	–5.5 µm	22.5 µm	+5.5 µm
Bump strength	30g		

Pin Coordinates

SED1580 Bump Center Coordinates

Units: µm

Pin	Name	X	Y
1	EIO2	–5378	–1240
2	$-V_3$	–5222	
3	$-V_2$	–5044	
4	VC	–4866	
5	V_2	–4688	
6	V_3	–4510	
7	NC	–4322	
8	NC	–4144	
9	NC	–3966	
10	NC	–3789	
11	NC	–3611	
12	F1O	–3449	
13	F2O	–2915	
14	NC	–2266	
15	SHL	–2086	
16	TEST	–1906	
17	V_{SS}	–1726	
18	BSEL	–1546	
19	LSEL	–1366	
20	FR	–1186	
21	YD	–1006	
22	NC	–826	
23	CA	–546	
24	LP	–466	
25	XSCL	–286	
26	D0	163	
27	D1	343	
28	D2	523	
29	D3	703	
30	D4	883	
31	D5	1063	
32	D6	1243	
33	D7	1423	
34	F2S	1603	
35	F1S	1783	
36	$\overline{DOFF}$	1963	
37	V_{DD}	2143	
38	NC	2387	
39	NC	2564	
40	NC	2742	
41	NC	2920	
42	NC	3098	
43	NC	3275	
44	NC	3453	
45	NC	3631	
46	NC	3809	
47	NC	3986	
48	NC	4164	
49	NC	4342	
50	V_3	4722	
51	V_2	4900	
52	V_C	5077	
53	$-V_2$	5255	
54	$-V_3$	5433	
55	EIO1	5629	
56	X1	6303	–1009
57	X2		–903
58	X3		–797
59	X4		–690
60	X5		–584
61	X6		–478
62	X7		–371
63	X8		–265
64	X9		–159
65	X10		–53
66	X11		53
67	X12		159
68	X13		265
69	X14		372
70	X15		478
71	X16		584
72	X17		690
73	X18		797
74	X19		903
75	X20		1009
76	X21	6098	1246
77	X22	5995	
78	X23	5893	
79	X24	5790	
80	X25	5688	
81	X26	5585	
82	X27	5483	
83	X28	5380	
84	X29	5278	
85	X30	5175	
86	X31	5073	
87	X32	4970	
88	X33	4868	
89	X34	4765	
90	X35	4663	
91	X36	4560	
92	X37	4458	
93	X38	4355	
94	X39	4253	
95	X40	4150	
96	X41	4048	
97	X42	3945	
98	X43	3843	
99	X44	3740	
100	X45	3637	
101	X46	3535	
102	X47	3432	
103	X48	3330	
104	X49	3227	
105	X50	3125	
106	X51	3022	
107	X52	2920	
108	X53	2817	
109	X54	2715	
110	X55	2612	
111	X56	2510	
112	X57	2407	
113	X58	2305	
114	X59	2202	
115	X60	2100	
116	X61	1997	
117	X62	1895	
118	X63	1792	
119	X64	1690	
120	X65	1587	
121	X66	1485	
122	X67	1382	
123	X68	1280	
124	X69	1177	
125	X70	1075	1246
126	X71	972	
127	X72	870	
128	X73	767	
129	X74	665	
130	X75	562	
131	X76	460	
132	X77	357	
133	X78	255	
134	X79	152	
135	X80	50	
136	X81	–52	
137	X82	–154	
138	X83	–257	
139	X84	–359	
140	X85	–462	
141	X86	–564	
142	X87	–567	
143	X88	–769	
144	X89	–872	
145	X90	–974	
146	X91	–1077	
147	X92	–1179	
148	X93	–1282	
149	X94	–1385	
150	X95	–1487	
151	X96	–1590	
152	X97	–1692	
153	X98	–1795	
154	X99	–1897	
155	X100	–2000	
156	X101	–2102	
157	X102	–2205	
158	X103	–2307	
159	X104	–2410	
160	X105	–2512	
161	X106	–2615	
162	X107	–2717	
163	X108	–2820	
164	X109	–2922	
165	X110	–3025	
166	X111	–3127	
167	X112	–3230	
168	X113	–3332	
169	X114	–3435	
170	X115	–3537	
171	X116	–3640	
172	X117	–3742	
173	X118	–3845	
174	X119	–3947	
175	X120	–4050	
176	X121	–4152	
177	X122	–4255	
178	X123	–4357	
179	X124	–4460	
180	X125	–4562	
181	X126	–4655	
182	X127	–4767	
183	X128	–4870	
184	X129	–4972	
185	X130	–5075	
186	X131	–5177	

Units: µm

Pin	Name	X	Y
187	X132	–5280	1246
188	X133	–5382	
189	X134	–5485	
190	X135	–5587	
191	X136	–5690	
192	X137	–5792	
193	X138	–5895	
194	X139	–5997	
195	X140	–6100	
196	X141	–6303	1009

Pin	Name	X	Y
197	X142	–6303	903
198	X143		797
199	X144		690
200	X145		584
201	X146		478
202	X147		372
203	X148		265
204	X149		159
205	X150		53
206	X151		–53

Pin	Name	X	Y
207	X152	–6303	–159
208	X153		–265
209	X154		–371
210	X155		–478
211	X156		–584
212	X157		–690
213	X158		–797
214	X159		–903
215	X160		–1009

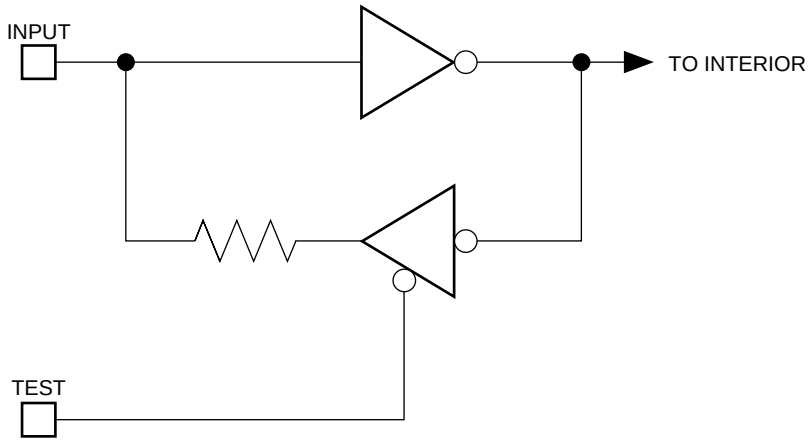
Pin Functions

Pin Functions Table

Pin Name	I/O	Function	# of Pins
X1 to X160	O	Segment (column) output to drive the LC. Output transition occurs on falling edge of LP.	160
BSEL	I	Display data input bit number select input. “L”: 4 bit input. “H”: 8 bit input.	1
LSEL	I	1/2 H operation select input. “L”: Normal operation. “H”: 1/2 H operation.	1
D0 to D7	I	Display data input. When 4 bit input is used, D0 to D3 is used, and D4 to D7 can be left NC.	8
XSCL	I	Display data shift clock input. Display data (D0 to D7) is read sequentially into the data register on the falling edge.	1
LP	I	Display data latch clock input * Accepts into the LCD driver the control signal from the LC driver selected by the MLS decoder, doing so at the falling edge, and outputs the LC driver output. * Writes the contents of the data registers to the frame memory 4 LP at a time for the specified column address. * Resets the enable control circuit. * When 1/2 operation is selected, inputs the LP with twice the normal frequency.	1
EIO1 EIO2	I/O	Enable I/O * Is set to input or output depending on the SHL input level. * When output, the LP input is reset (in an “H” state), and when the 160 bit of display data has been read in, the signal automatically falls to L. * When connected in cascade, is connected to the next stage EIO input.	1 1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th># of Pins</th></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and EIO terminal I/O control input.
<u>WHEN BSEL = “L” (i.e. 4-bit input):</u>
When the display data has been input to terminals (D3, D2, D1, D0) in the order (a, b, c, d) (e, f, g, h)... (w, x, y, z), the relationship between the data and the segment is as shown in the table below:
<table>
<tr><td rowspan="2">SHL</td><td colspan="20">Xn (Segment Output)</td><td colspan="2">EIO</td></tr>
<tr><td>160</td><td>159</td><td>158</td><td>157</td><td>156</td><td>155</td><td>154</td><td>153</td><td>...</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>...</td><td>s</td><td>t</td><td>u</td><td>v</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>...</td><td>h</td><td>g</td><td>f</td><td>e</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
<u>WHEN BSEL = “H” (i.e., 8-bit input):</u>
When the display data has been input to terminals (D7, D6, D5, D4, D3, D2, D1, D0) in the order (a, b, c, d, e, f, g, h) ... (s, t, u, v, w, x, y, z), the relationship between the data and the segment is as shown in the table below:
<table>
<tr><td rowspan="2">SHL</td><td colspan="20">Xn (Segment Output)</td><td colspan="2">EIO</td></tr>
<tr><td>160</td><td>159</td><td>158</td><td>157</td><td>156</td><td>155</td><td>154</td><td>153</td><td>...</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>...</td><td>s</td><td>t</td><td>u</td><td>v</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>...</td><td>h</td><td>g</td><td>f</td><td>e</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
</td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>Forced blank input.
When at “L” level, segment output is forced to Vc. The display RAM data is maintained.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input. With terminator (*1).</td><td>1</td></tr>
<tr><td>YD</td><td>I</td><td>Frame running start input
* Resets the column address for writing or reading.
* The number of running lines for writing (column address number) relating to frame memory is determined based on the number of LP pulses input during a single YD cycle.</td><td>1</td></tr>
<tr><td>CA</td><td>I</td><td>Field delimiter signal input. With terminator (*1).
This signal is input at the start of each new field, and is output by the SED1751.</td><td>1</td></tr>
<tr><td>F1S
F2S</td><td>I</td><td>Drive pattern cutover gap set input
(F2S, F1S) = (0,0), (0,1), (1,0), (1,1)
Cutover gap Field, 8H, 2H, 4H</td><td>1
1</td></tr>
<tr><td>F1O
F2O</td><td>O</td><td>Driver pattern select output for the Y driver. Connects to the common (row) driver.</td><td>1
1</td></tr>
<tr><td>TEST</td><td>I</td><td>Test input. Normally fixed at “L”.</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power</td><td>Power supply for logic.</td><td>1 each</td></tr>
<tr><td>V_3, V_2, V_C, $-V_2$, $-V_3$</td><td>Power</td><td>Power supply for LC driver. $V_3 > V_2 > V_C > -V_2 > -V_3$</td><td>5 each</td></tr>
</table>

Note: *1 Regarding the terminator


INPUT
TO INTERIOR
TEST

FUNCTIONS

The Functional Blocks

Enable Control

When the enable signal is in a disable state (EIO = "H"), the internal clock signal and data bus are fixed at "L", placing the chip in power save mode.
When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to "VSS".
The enable control circuit automatically senses when 160 bits worth of data have been received, and automatically sends the enable signal, thus eliminating the need for a control signal from the control LSI.

Bi-directional Shift Register

This sends the control signal for writing the display data D0 – D7 to the data register. The order in which the display data is latched into the data register by the SHL input is returned (SIC? Reversed?).

Data Register

This is a 160 dot register which controls writing to the display RAM. It has 4 lines. At each falling edge of the LP signal it accepts display data from one line, and writes to the frame memory after it has stored 4 lines of data.

Frame Memory

This is static RAM (with peripheral circuits) that stores LC display data. It has a capacity of 160 segments by 240 lines.

MLS Decoder

This outputs the drive control signals necessary for the 4 MLS driving. The control signal is set by field information provided by the four lines of display data, FR, DOFF, and the control circuit.

LCD Driver

The LCD driver outputs the LC drive voltage. The driver voltage is selected by the control signal from the 5 levels V3, V2, VC, –V2 and –V3, determined by the MLS decoder.

Column Address Generating Circuit

When writing to or reading from frame memory, this outputs the column address corresponding to the location of the RAM in frame memory.

Level Shifter

This is a level interface circuit used to convert signal levels when signals are propagated from low-voltage parts to high-voltage parts.

Data Control

This accepts display data input when enabled, and sends it to the data register.

Control Circuit

This determines the self refresh rate, enables the data register to write to the display RAM, controls the output of the column address generator, and performs field control on the MLS decoder.

The Self Refresh Function

Setting the Self Refresh Mode

"Self refresh mode" refers to a situation where the transmission of display data from the display controller to the SED1580 is suspended when the content of the display does not change, and where the SED1580 automatically senses this and enters a power down display mode.
To place the SED1580 in the self refresh mode maintain the shift clock XSCL at the "L" level during four horizontal display periods (4x the LP signal period) after the completion of the input of the display data of an n + 3 line.
When the XSCL is suspended, the power is reduced, so display data inputs D0 – D7 are suspended, as is transmission from the display controller, being set to "H" or "L". At this time the display controller must send LP, YD, or FR signals periodically to the SED1580 as it does when data is being sent. The SED1580 receives these signals, periodically reads display data from its internal RAM, and refreshes the display. The display off function is operational even when in the self refresh mode.

Getting Out of the Self Refresh Mode

In order to get out of the self refresh mode, the display controller inputs the shift clock XSCL to the SED1580 for four or more horizontal display periods with the timing of the data transmission from the falling edge of the LP signal at the time of an n + 3 line. With the falling edge of the LP signal after the fourth horizontal period after getting out of this mode, the display data transmitted during the four horizontal display intervals is written to frame memory.
When SED1580s are cascade connected, if the number of XSCL clocks input does not correspond to the cascade connections, then not all of the SED1580s will be released from self refresh mode.

Note: When the number of lines is 240:

n lines	1, 5, 9, ...233, 237 (1 + multiples of 4)
n + 1 lines	2, 6, 10,...234, 238 (2 + multiples of 4)
n + 2 lines	3, 7, 11,...235, 239 (3 + multiples of 4)
n + 3 lines	4, 8, 12,...236, 240 (Multiples of 4)

The Relationship Between Drive Output Voltages and Display Data

F20, F10, and the common drive voltage have the following relationships:

FR	**L**				**H**			
F1O **F2O**	**1** **1**	**0** **1**	**1** **0**	**0** **0**	**1** **1**	**0** **1**	**1** **0**	**0** **0**
n line	V1	V1	–V1	V1	–V1	–V1	V1	–V1
n + 1 line	–V1	V1	V1	V1	V1	–V1	–V1	–V1
n + 2 line	V1	–V1	V1	V1	–V1	V1	–V1	–V1
n + 3 line	V1	V1	V1	–V1	–V1	–V1	–V1	V1

Note: Voltage relationships: V1 > VC > –V1 (VC is the middle voltage level)

The transitions in (F2O, F1O) within each field when the drive pattern changes:

First field	In the order (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0)
Second field	In the order (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1)
Third field	In the order (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0)
Fourth field	In the order (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1)

This is determined by the values of the inputs (F2S, F1S) during the changeover interval. The relationship between F2S and F1S and the changeover interval is as follows:

When the changeover interval is selected for each field, the value stored in the field is the first value shown in the shown in the (F2O, F1O) change table above (the value on the left).

F2S	F1S	Changeover Interval
0	0	Field
0	1	8-line interval
1	0	2-line interval
1	1	4-line interval

The relationship between the display data, the LC AC signal FR, and the segment output voltage is as shown below. The output voltage changes in conjunction with the F20, F10 values that determine the common drive voltage.

Display data: 0= not lit, 1 = lit

When FR = "L"

Display Line	n line	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	n + 1 line	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2 line	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3 line	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	(F2O, F1O) = (1,1)	V_2	V_C	V_C	$-V_2$	V_3	V_2	V_2	V_C	V_C	$-V_2$	$-V_2$	$-V_3$	V_2	V_C	V_C	$-V_2$
	(F2O, F1O) = (1,0)	V_2	V_C	V_3	V_2	V_C	$-V_2$	V_2	V_C	V_C	$-V_2$	V_2	V_C	$-V_2$	$-V_3$	V_C	$-V_2$
	(F2O, F1O) = (0,1)	V_2	V_C	V_C	$-V_2$	V_C	$-V_2$	$-V_2$	$-V_3$	V_3	V_2	V_2	V_C	V_2	V_C	V_C	$-V_2$
	(F2O, F1O) = (0,0)	V_2	V_3	V_C	V_2	V_C	V_2	$-V_2$	V_C	V_C	V_2	$-V_2$	V_C	$-V_2$	V_C	$-V_3$	$-V_2$

When FR = "H"

Display Line	n line	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	n + 1 line	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2 line	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3 line	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	(F2O, F1O) = (1,1)	$-V_2$	V_C	V_C	V_2	$-V_3$	$-V_2$	$-V_2$	V_C	V_C	V_2	V_2	V_3	$-V_2$	V_C	V_C	V_2
	(F2O, F1O) = (1,0)	$-V_2$	V_C	$-V_3$	$-V_2$	V_C	V_2	$-V_2$	V_C	V_C	V_2	$-V_2$	V_C	V_2	V_3	V_C	V_2
	(F2O, F1O) = (0,1)	$-V_2$	V_C	V_C	V_2	V_C	V_2	V_2	V_3	$-V_3$	$-V_2$	$-V_2$	V_C	$-V_2$	V_C	V_C	V_2
	(F2O, F1O) = (0,0)	$-V_2$	$-V_3$	V_C	$-V_2$	V_C	$-V_2$	V_2	V_C	V_C	$-V_2$	V_2	V_C	V_2	V_C	V_3	V_2

When $\overline{DOFF}$ = "L", all drive outputs are tied to the V_C level.

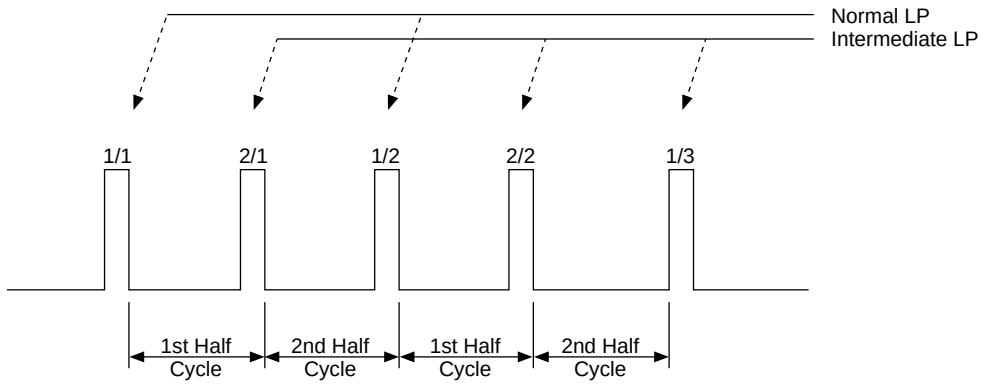
LC Drive Output Voltages During 1/2 H Operation

When LSEL is set to "H" and twice the normal frequency is applied to the LP input terminal, then the chip functions in 1/2 mode. Each time LP is input the field data changes, thus the output changes at the center point of the 1H interval. However, the input of display data to the D1580, writing of display data to the frame memory, and read in display data from the frame memory is the same as in the normal drive.
The Y driver output changes according to the field data output by the X driver with each LP input, causing a transition at the center point of the 1H interval; however, the transition of the drive line occurs each 1H, just as in the normal drive.
During 1/2 H operation, the changes of the F20, F10 in each field are as shown in the table below. In this table the statuses of the F20 and F10 are represented as given below:

(F2O, F1O) = (1,1)	(1)
(F2O, F1O) = (1,0)	(2)
(F2O, F1O) = (0,1)	(3)
(F2O, F1O) = (0,0)	(4)

	First Half Cycle	Second Half Cycle	First Half Cycle	Second Half Cycle	
Field #1	(4)	(1)	(1)	(4)	
Field #2	(1)	(4)	(4)	(1)	This pattern is
Field #3	(3)	(2)	(2)	(3)	repeated hereafter.
Field #4	(2)	(3)	(3)	(2)	

During 1/2H operation, the values of F2S and F1S are ignored.

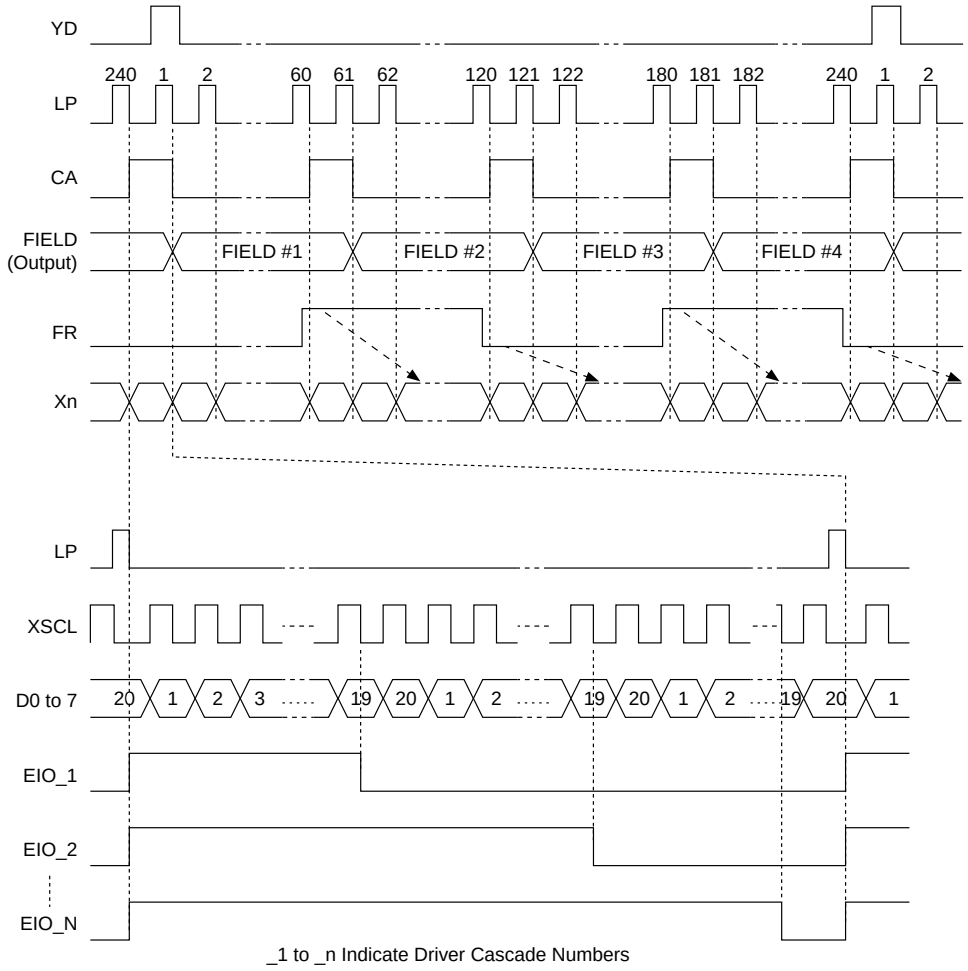


The segment output voltage during 1/2 H operation also follows the display data of 4.3 and the diagram showing the relationship between the LC AC signal FR and the segment output voltage. In the signal B/A that indicates the number of the LP, the “A” in the figure indicates LP during a normal drive, and “B” differentiates between the normal LP and the intermediate LP (where B = 1 is normal and B = 2 is intermediate).

Timing diagram (assuming 1/240 duty)

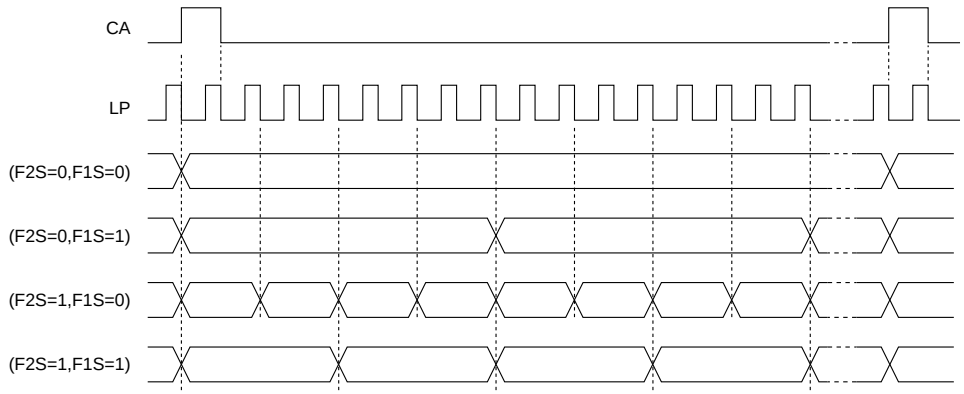
(This diagram provided only as a reference.)

Normal Drive Timing

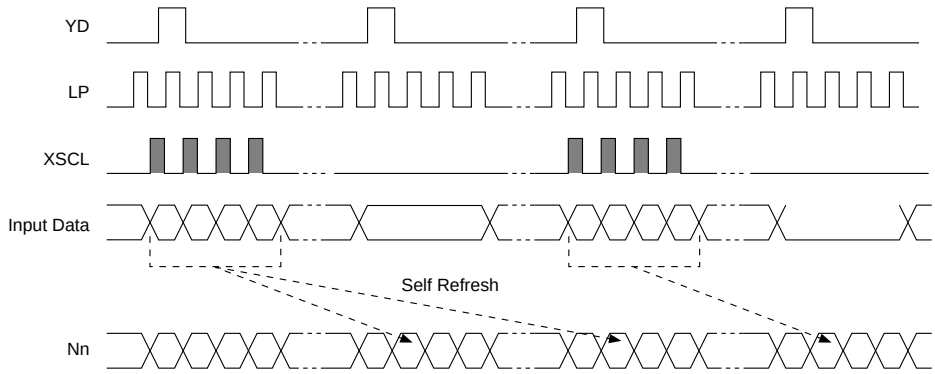


_1 to _n Indicate Driver Cascade Numbers

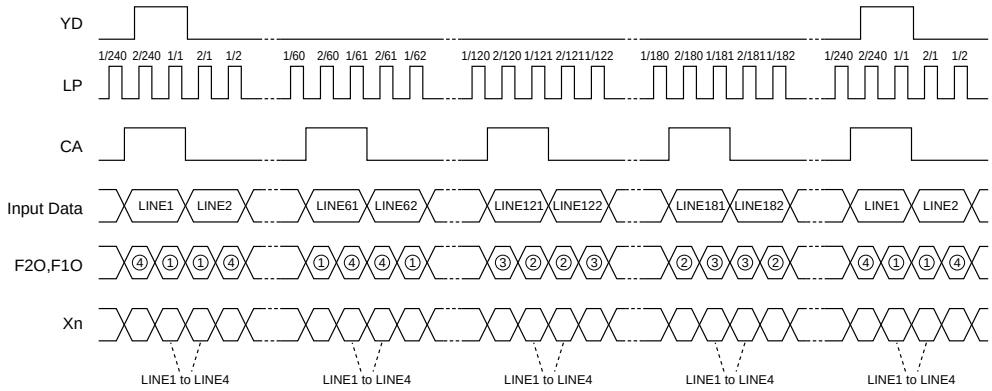
F2O, F1O Change Timing



Setting and Releasing Self Refresh



1/2 H Drive Timing



ELECTRICAL CHARACTERISTICS

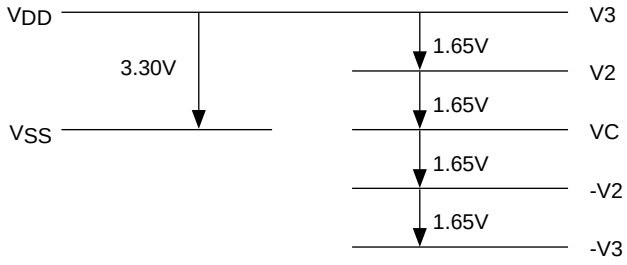
Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	$–V_3$	–8.0 to +0.3	V
Input voltage	V_I	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_O	V_{SS} –0.3 to V_{DD} +0.3	V
EIO output current	I_{O1}	20	mA
Operating temperature	Topr	–20 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

Note 1: The voltages are all relative to V_{DD} = 0V.

Note 2: Storage temperature 1 is the recommendation for the chip itself or for the chip and a plastic package, and storage temperature 2 is the recommendation for the chip mounted on TCP.

Note 3: Ensure that the relationship between V_3, V_2, V_C, $–V_2$ and $–V_3$ is always as follows:
$V_{DD} \geq V_3 > V_2 > V_C > –V_2 > –V_3$



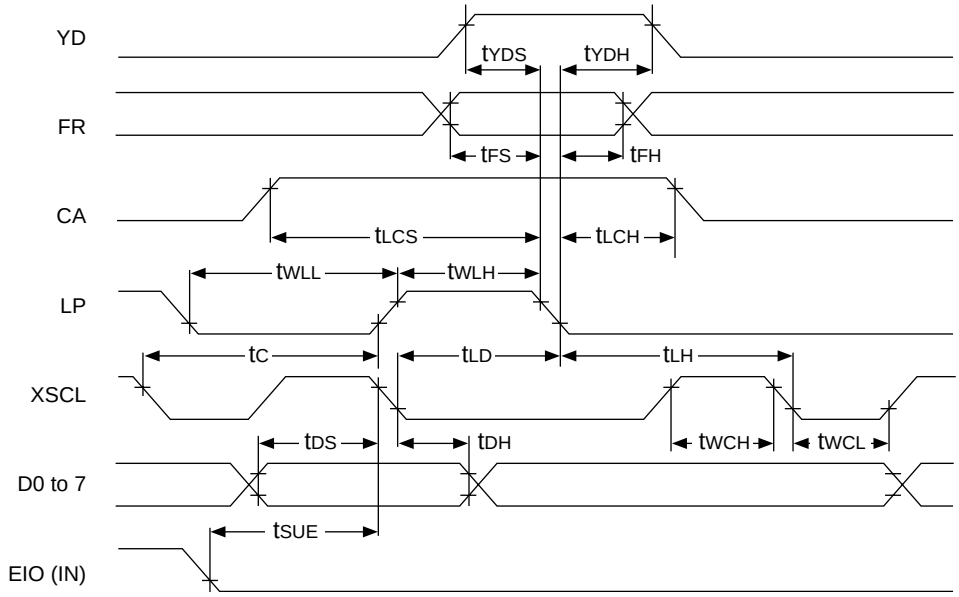
DC Characteristics

Unless otherwise specified, V_{DD} = V3 = 0V, V_{SS} = –3.3V ± 0.3V, Ta = –20 to 85°C

Parameter	Symbol	Conditions	Applicable terminals	Min	Typ	Max	Units
Power voltage (1)	V_{SS}		V_{SS}	–3.6	–3.3	–3.0	V
Power voltage (2)	$–V_3$	V_{SS} = –3.0V to –3.6V	$–V_3$	–7.2	–6.4	–6.0	V
Power voltage (3)	$–V_2$	V_{SS} = –3.0V to –3.6V	$–V_2$		$(–V_3)$* 3/4		V
Power voltage (4)	V_C	V_{SS} = –3.0V to –3.6V	V_C		$(–V_3)$* 2/4		V
Power voltage (5)	V_2	V_{SS} = –3.0V to –3.6V	V_2		$(–V_3)$* 1/4		V
High-level input voltage	V_{IH}	V_{SS} = –3.3V to –3.6V	EIO1, EIO2, SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0 to D7, F1S, F2S, $\overline{DOFF}$	0.2* V_{SS}			V
Low-level input voltage	V_{IL}					0.8* V_{SS}	V
High-level output voltage	V_{OH}	V_{SS} = –3.3V to –3.6V	I_{OH} = –0.6mA; EIO1, EIO2 F1O, F2O	V_{DD} – 0.4			V
Low-level output voltage	V_{OL}		I_{OL} = 0.6mA; EIO1, EIO2 F1O, F2O			V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0 to D7, F1S, F2S, $\overline{DOFF}$			5.0	µA
I/O leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$	EIO1, EIO2			5.0	µA
Static current (1)	Issq	V_{IN} = V_{DD} or V_{SS}	V_{SS}			10	µA
Static current (2)	$–I_{3T}$	$–V_3$ = –6.6V	$–V_3$			5	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5V, V_{SS} = –3.30V, V_3 = V_{DD} = 0V, V_2 = –1.65V, V_C = –3.30V, $–V_2$ = –4.95V, V_3 = 6.60V	X1 to X160		0.8	1.5	KΩ
Average operating consumption current (1) Data Transfer Mode	Isst	V_{SS} = –3.30V, V_3 = V_{DD} = 0V, V_2 = –1.65V, V_C = –3.30V, $–V_2$ = –4.95V, $–V_3$ = –6.60V, V_{IN} = V_{DD} or V_{SS}, f_{XSCL} = 480 kHz, f_{LP} = 12kHz, f_{FR} = 30Hz, Input Data: checker pattern, 8-bit, 320 × 200, no load	V_{SS}		70	100	µA
Average operating consumption current (1) Self Refresh Mode	Isss	XSCL = V_{SS} Other parameters are the same as for Isst			50	70	µA
Average operating consumption current (2)	$–I_{3T}$	Parameters are the same as for Isst	$–V_3$		10	20	µA
Input terminal capacitance	CI	Freq = 1 MHz, Ta = 25°C, Chip alone	SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0 to D7, F1S, F2S, $\overline{DOFF}$			8	pF
I/O terminal capacitance	CI/O		EIO1, EIO2			15	pF
Output terminal capacitance	CO		F1O, F2O			7	pF

AC Characteristics

Input Timing Characteristics

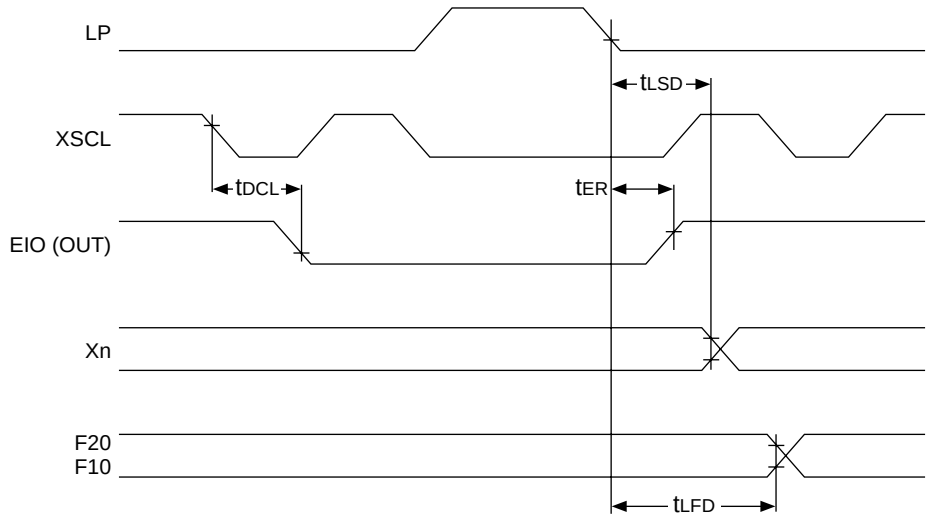


V_{SS} = –3.3 V ± 0.3 V, V_{IH} = 0.2 V_{SS}, V_{IL} = 0.8 V_{SS}

Parameter	Symbol	Conditions	Min	Max	Units
XSCL period	t_C		150		ns
XSCL high level pulse width	t_{WCH}		20		ns
XSCL low level pulse width	t_{WCL}		20		ns
Data setup time	t_{DS}		10		ns
Data hold time	t_{DH}		10		ns
Time between XSCL and LP fall	t_{LD}		10		ns
Time between LP and XSCL fall	t_{LH}		150		ns
LP high level pulse width	t_{WLH}		100		ns
LP low level pulse width	t_{WLL}		100		ns
FR setup time	t_{FS}		25		ns
FR hold time	t_{FH}		10		ns
EIO setup time	t_{SUE}		30		ns
YD setup time	t_{YDS}		50		ns
YD hold time	t_{YDH}		50		ns
CA setup time	t_{LCS}		10		µs
CA hold time	t_{LCH}		–200	200	ns
Input signal rise time and fall time	tr, tf			30	ns

Note: CA is only effective at the first LP in the field. Assuming 1/N duty, the “first LP” refers to 1 and 1+ (multiples of (N/4).
FR is accepted at the falling edge of LP, and its state is reflected into the output that changes at the falling edge the following 1H.

Output Timing Characteristics

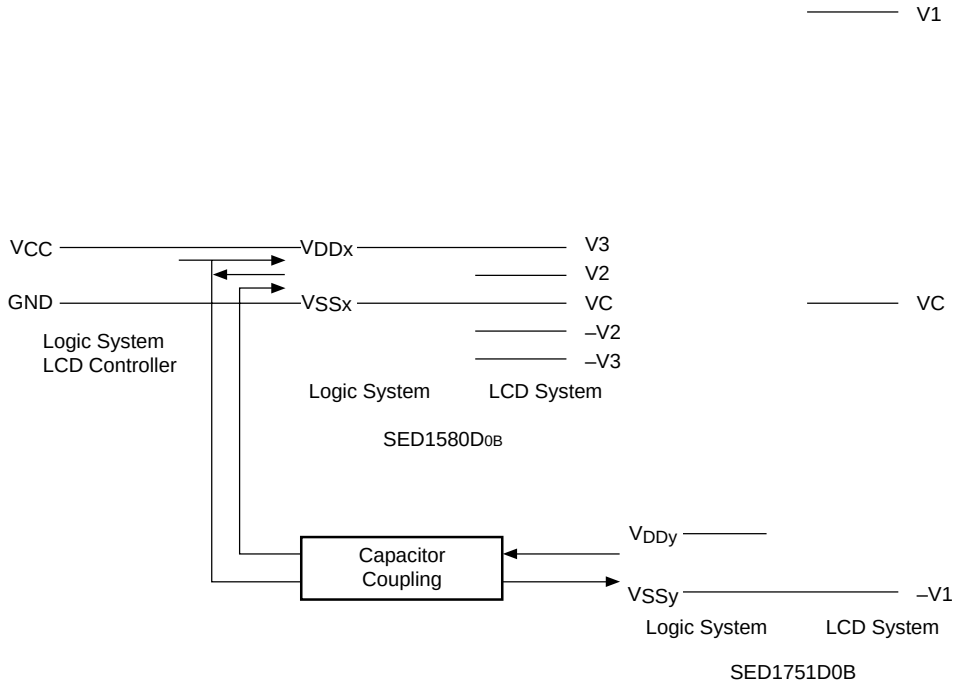


V_{SS} = –3.3V ± 0.3V, V_{IH} = 0.2 V_{SS}, V_{IL} = 0.8 V_{SS}, –V_3 = –6.6V ± 0.6V

Parameter	Symbol	Conditions	Min	Max	Units
EIO reset time	t_{ER}	C_L = 15 pF (EI0)		80	ns
EIO output delay time	t_{DCL}			90	ns
LP → Xn output delay time	t_{LSD}	CL = 100 pF		400	ns
LP → F2O, F1O output delay time	t_{LFD}			3000	ns

POWER SOURCE

The Relationship Between Voltage Levels



When the SED1580 and SED1751 are used to structure an extremely low-power module system, the power supplies for the SED1580 logic systems and LCD systems, and the power supplies for the LCD controller should have the voltage relationships shown in the figure above.
In this case, caution is required when sending signals to the logic system. Specifically, use caution with the following:

LCD Controller	→	SED1580	Direct connection
LCD Controller	→	SED1751	Requires a capacitor coupling
SED1580	→	SED1751	Requires a capacitor coupling
SED1751	→	SED1580	Requires a capacitor coupling

Cautions During Power Up and Power Down

This LSI requires special attention to be paid to the sequence in which the power supplies are turned on. Ensure that the power supply ON sequence is always one of the sequences below:

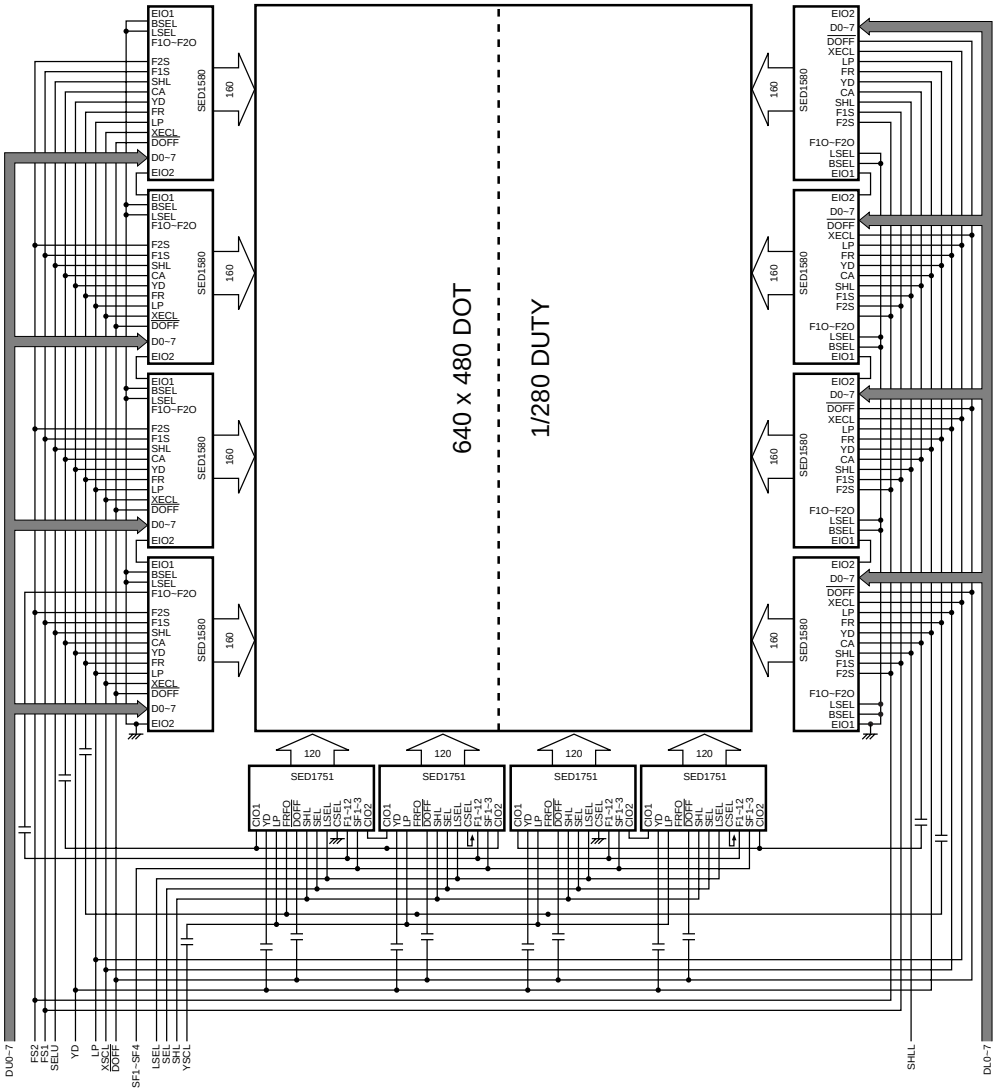
Logic system ON → First LP cycle → LCD system ON

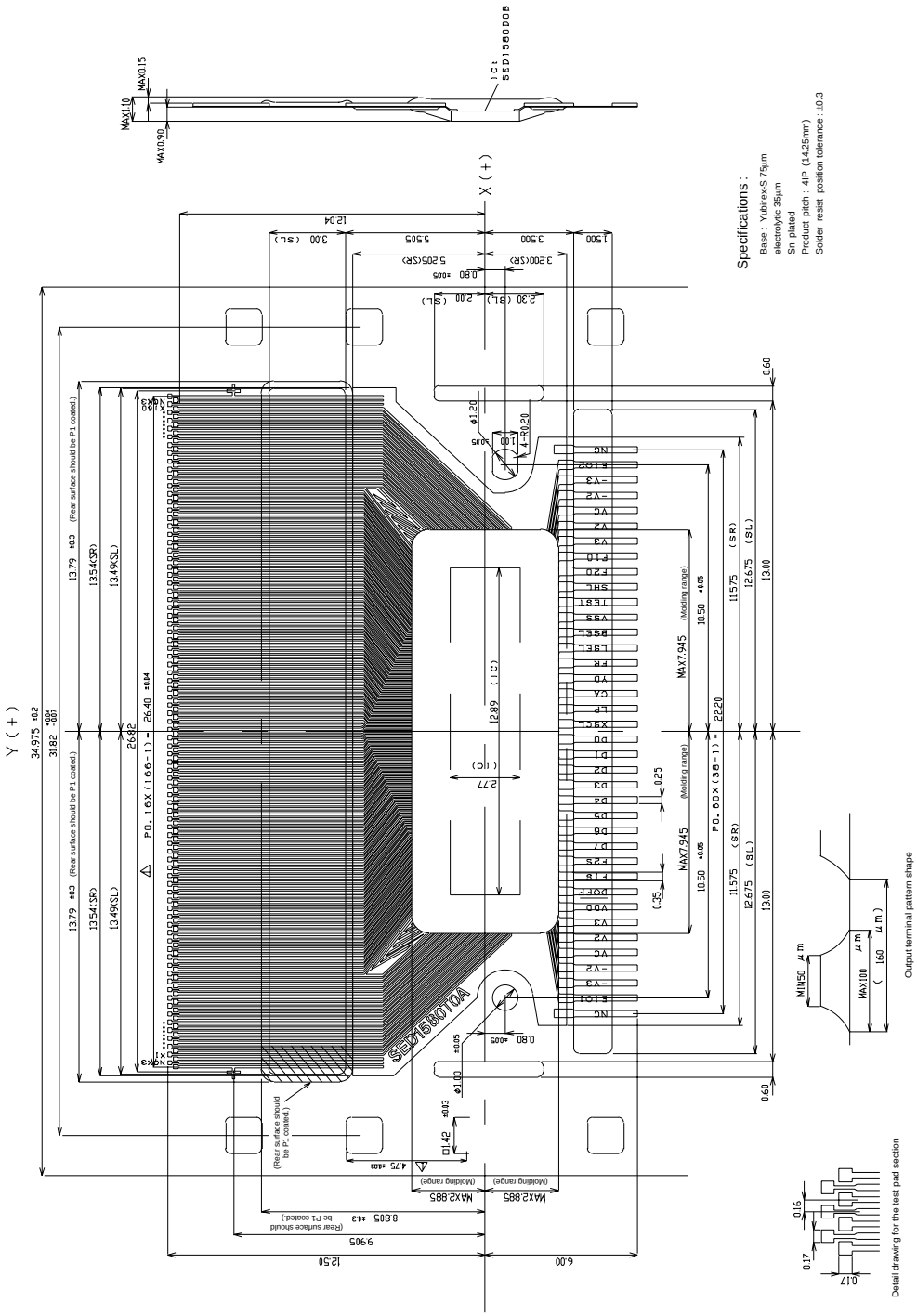
or

Logic system ON → $\overline{\text{DOFF}}$ = "L" → LCD system ON → First LP cycle (*2) → $\overline{\text{DOFF}}$ = "H"

After applying power to the SED1580, the 2 frame interval is not displayed correctly because the number of LP cycles input in the first frame is counted and used to determine an address in the frame memory. This requires the use of $\overline{\text{DOFF}}$. Consequently, display data should be transmitted at the point marked with (*2). For power down, use the LCD system OFF → Logic system OFF sequence, or power both down at the same time.

EXAMPLE OF EXTERNAL CONNECTIONS




Specifications :
Base : Yubirex-S 75µm
electrolytic 35µm
Sn plated
Product pitch : 4IP (14.25mm)
Solder resist position tolerance : ±0.3
X (+)
Y (+)
SED1580T0A
Output terminal pattern shape
Detail drawing for the test pad section

Notes

Regarding this development specification, take the followings into consideration.

1. The contents of this development specification may be revised without prior notice.
2. This development specification does not guarantee or grant the industrial property rights or any other rights.
   The application examples contained in this development manual are given in order to help customers understand the product. Note that we shall not take any responsibility regarding problems on circuits.
   Regarding the use of semiconductor elements, take the followings into consideration.

[Precautions on Handling Optical Parts]

Following the solar cell theory, the characteristics of a semiconductor element changes as it is exposed to the light. Therefore, if this IC is exposed to the light, malfunction may occur.

(1) Design and mount the IC so that it won't be exposed to the light when in use.
(2) Design and mount the IC so that it won't be exposed to the light in the inspection process.
(3) Be concerned about shading of all the surfaces (front, back and side) of the IC.