SED1220
LCD Controller/Drivers

Technical Manual

Contents

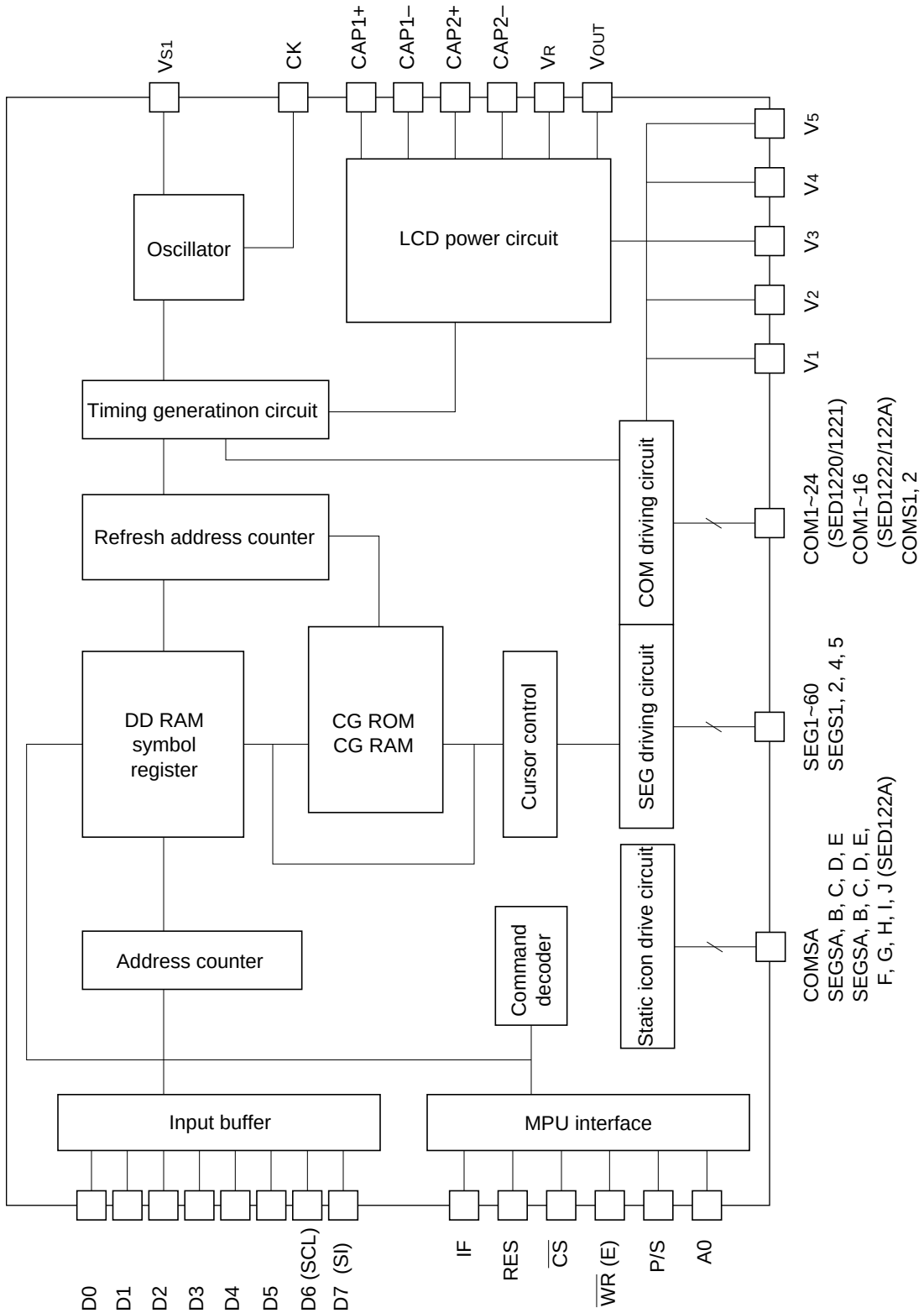
OVERVIEW

SED1220 is a dot matrix LCD controller/driver for character display. Using 4bits data, 8bits data or serial data being provided from the micro computer, it displays up to 36 characters, 4 user defined characters and up to 120 symbols.
Up to 256 types of built-in character generator ROMs are prepared. Each character font is consisted of 5 × 8 dots. It also contains the RAM for displaying 4 user defined characters each font consisting of 5 × 8 dots. It is symbol register allows character display with high degree of freedom. This handy equipment can be operated with minimum power consumption with its low power consumption design, standby and sleeping mode.

FEATURES

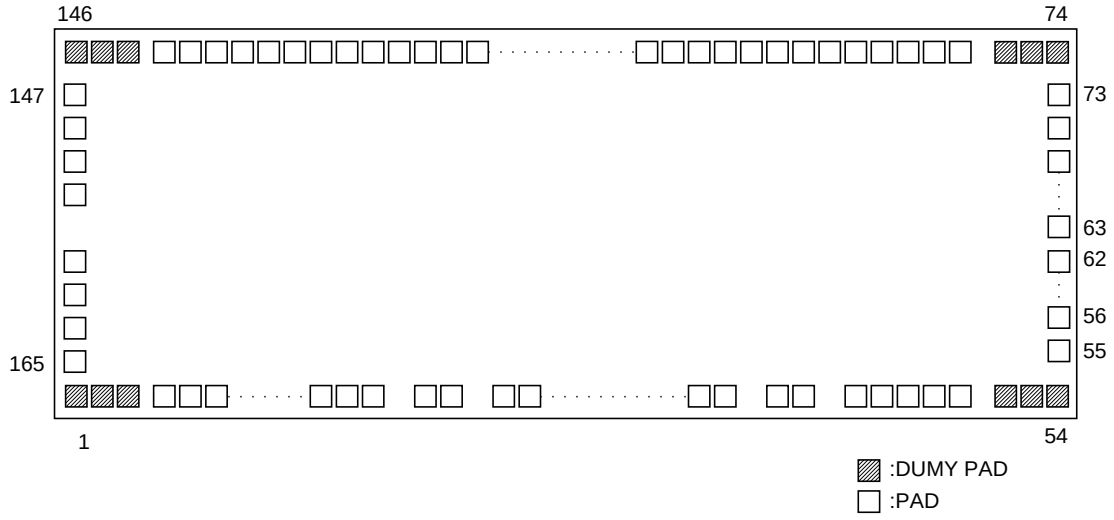
- Built-in data display RAM – 36 characters + 4 user defined characters + 120 symbols.
- CG ROM (For up to 256 characters), CG RAM (for 4 characters) and symbol register (for 120 symbols).
- No. of display digit and lines
  < In normal mode >
  ① (12 digits + 4 segments for signal) × 3 lines + 120 symbols + 5 static symbols (SED1220D**)
  ② (12 digits + 4 segments for signal) × 2 lines + 120 symbols + 5 static symbols (SED1221D**)
  ③ 12 digits × 2 lines + 120 symbols + 5 static symbols (SED1222D**)
  ④ (12 digits + 4 segments for signal) × 2 lines + 120 symbols + 10 static symbols (SED122AD**)
  < In standby mode >
  ① 5 static symbols
  ② 5 static symbols
  ③ 5 static symbols
  ④ 10 static symbols
- Built-in CR oscillation circuit (C and R contained)
- Accepts external clock input
- High-speed MPU interface
  Affords interface with both 68/80 system MPUs
  Affords interface through 4 bits and 8 bits
- Affords serial interface
- Character font consists of 5 × 8 dots
- Duty ratio ① 1/26 (SED1220D**)
  ② 1/18 (SED1221D**, SED1222D**)
- Simplified command setting
- Built-in power circuit for driving liquid crystal
  Power amplifier circuit, power regulation circuit and voltage followers × 4
- Built-in electronic volume function
- Low power consumption
  80 μA max. (In normal operation, including operating current of the power supply).
  20 μA max. (In standby mode for displaying static icon).
  5 μA max. (In sleeping mode when display is turned off).
- Power supply
  V_{DD} - V_{SS} –2.4 V ~ –3.6 V
  V_{DD} - V_5 –4.0 V ~ – 6.0 V
- Temperature range for wide range operation
  Ta = –30 ~ 85°C
- CMOS process
- Shipping style
  Chip (Al pad product) SED1222D*A
  Chip (Au bump product) SED122*D*B
  TCP SED122*T**
- This unit does not employ radiation protection design

BLOCK DIAGRAM



CHIP SPECIFICATION

SED1220D**/1221D**/122AD**



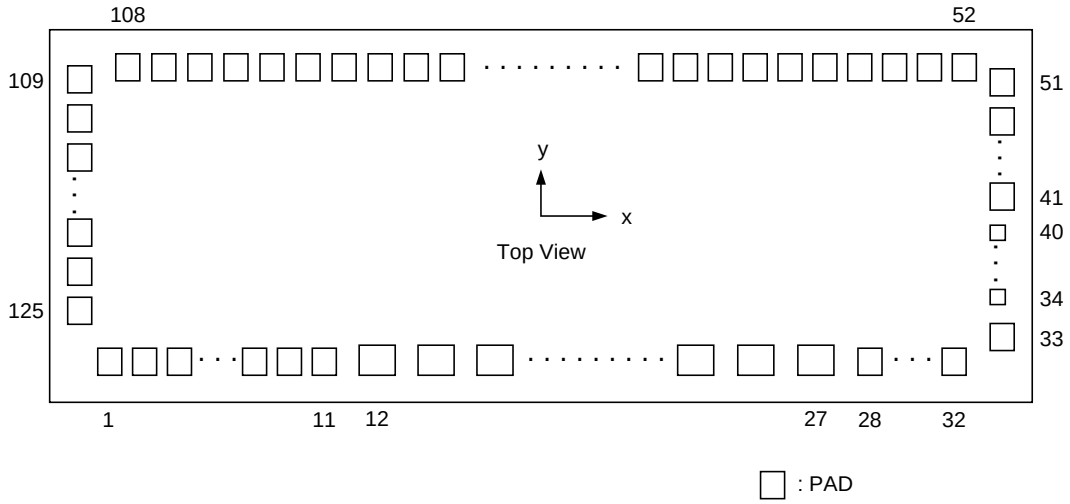
SED122∗D**
↑
Digits prepared for CGROM pattern changes

Chip size: 7.70 × 2.77 mm
Pad pitch: 100 µm (Minimum)
Chip thickness (for reference): 625 ± 25 µm (SED122∗D∗A)
(SED122∗D∗B)

1) A1 pad specifications
   Pad size on Y side: 75 µm × 135 µm
   Pad size on X side: 135 µm × 75 µm
2) Au bump specifications
   Bump size on Y side: 69 µm × 129 µm
   Bump size on X side: 129 µm × 69 µm
   Bump height (for reference) 22.5 µm ± 5.5 µm

<Fuse Pines>
1) Al pad. pad size 86 µm × 75 µm
2) Au bump
   Bump size 80 µm × 69 µm

SED1222D**



SED1222D**
↑
Digits prepared for CGROM pattern changes

Chip size:	7.70 × 2.77 mm
Pad pitch:	124 µm (Minimum)
Chip thickness (for reference):	625 ± 50 µm (SED1222D*A)

1) A1 pad specifications

Pad size on Y side:	90 µm × 96 µm
Pad size on X side:	96 µm × 90 µm (PAD. No. 1 ~ 11, 28 ~ 32, 52 ~ 108)
	175 µm ×135 µm (PAD. No. 12 ~ 27)

<Fuse Pines>

1) Al pad. pad size	86 µm × 75 µm

<SED1220D$_{**}$/1221D$_{**}$>

Unit: µm

PAD		COORDINATES		PAD		COORDINATES	
No.	Name	X	Y	No.	Name	X	Y
1	NC	–3700	–1204	55	V_{DD}	3670	–910
2	NC	–3600	↑	56	(FSA)	3603	–796
3	NC	–3500		57	(FSB)	↑	–696
4	A0	–3252		58	(FSC)		–596
5	$\overline{WR}$	–3132		59	(FS0)		–496
6	$\overline{CS}$	–3012		60	(FS1)		–396
7	D7	–2892		61	(FS2)	↓	–296
8	D6	–2772		62	(FS3)	3603	–196
9	D5	–2652		63	V_{DD}	3670	–82
10	D4	–2532		64	COMSA	↑	61
11	D3	–2412		65	COMS1		203
12	D2	–2292		66	COM1		303
13	D1	–2172		67	COM2		403
14	D0	–2052		68	COM3		503
15	V_{DD}	–1836		69	COM4		603
16	V_{DD}	–1736		70	COM5		703
17	V_{SS}	–1556		71	COM6		803
18	V_{SS}	–1456		72	COM7	↓	903
19	V_5	–1276		73	COM8	3670	1003
20	V_5	–1176		74	NC	3700	1204
21	V_4	–996		75	NC	3600	↑
22	V_4	–896		76	NC	3500	
23	V_3	–716		77	SEGS1	3319	
24	V_3	–616		78	SEGS2	3219	
25	V_2	–436		79	SEG1	3119	
26	V_2	–336		80	SEG2	3019	
27	V_1	–156		81	SEG3	2919	
28	V_1	–56		82	SEG4	2819	
29	V_0	124		83	SEG5	2719	
30	V_0	224		84	SEG6	2619	
31	V_R	404		85	SEG7	2519	
32	V_R	504		86	SEG8	2419	
33	V_{OUT}	684		87	SEG9	2319	
34	V_{OUT}	784		88	SEG10	2219	
35	CAP2–	964		89	SEG11	2119	
36	CAP2–	1064		90	SEG12	2019	
37	CAP2+	1244		91	SEG13	1919	
38	CAP2+	1344		92	SEG14	1819	
39	CAP1–	1524		93	SEG15	1719	
40	CAP1–	1624		94	SEG16	1619	
41	CAP1+	1804		95	SEG17	1519	
42	CAP1+	1904		96	SEG18	1419	
43	V_{SS}	2084		97	SEG19	1319	
44	V_{SS}	2184		98	SEG20	1219	
45	V_{DD}	2364		99	SEG21	1119	
46	V_{DD}	2464		100	SEG22	1019	
47	CK	2693		101	SEG23	919	
48	VS1	2821		102	SEG24	819	
49	P/S	2949		103	SEG25	719	
50	I/F	3077		104	SEG26	619	
51	RES	3205		105	SEG27	519	
52	NC	3500		106	SEG28	419	
53	NC	3600		107	SEG29	319	
54	NC	3700	–1204	108	SEG30	219	1204

(FS*) : Being fuse adjusting pins, maintain them on floating state.
CK pins : Should be V_{DD} when not being used.

PAD		COORDINATES	
No.	Name	X	Y
109	SEG31	119	1204
110	SEG32	19	
111	SEG33	–81	
112	SEG34	–181	
113	SEG35	–281	
114	SEG36	–381	
115	SEG37	–481	
116	SEG38	–581	
117	SEG39	–681	
118	SEG40	–781	
119	SEG41	–881	
120	SEG42	–981	
121	SEG43	–1081	
122	SEG44	–1181	
123	SEG45	–1281	
124	SEG46	–1381	
125	SEG47	–1481	
126	SEG48	–1581	
127	SEG49	–1681	
128	SEG50	–1781	
129	SEG51	–1881	
130	SEG52	–1981	
131	SEG53	–2081	
132	SEG54	–2181	
133	SEG55	–2281	
134	SEG56	–2381	
135	SEG57	–2481	
136	SEG58	–2581	
137	SEG59	–2681	
138	SEG60	–2781	
139	SEGS4	–2881	
140	SEGS5	–2981	
141	COM24	–3081	
142	COM23	–3181	
143	COM22	–3281	
144	NC	–3500	
145	NC	–3600	
146	NC	–3700	1204
147	COM21	–3670	1000
148	COM20		900
149	COM19		800
150	COM18		700
151	COM17		600
152	COM16		500
153	COM15		400
154	COM14		300
155	COM13		200
156	COM12		100
157	COM11		0
158	COM10		–100
159	COM9		–200
160	COMS2		–300
161	SEGSA		–433
162	SEGSB		–533
163	SEGSC		–633
164	SEGSD		–733
165	SEGSE	–3670	–833

<SED1222D**>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	$\overline{A0}$	–3312	–1228
2	$\overline{WR}$	–3180	↑
3	CS	–3048	
4	D7	–2916	
5	D6	–2784	
6	D5	–2652	
7	D4	–2520	
8	D3	–2388	
9	D2	–2256	
10	D1	–2124	↓
11	D0	–1992	–1228
12	V_{DD}	–1786	–1204
13	V_{SS}	–1506	↑
14	V_5	–1226	
15	V_4	–946	
16	V_3	–666	
17	V_2	–386	
18	V_1	–106	
19	V_0	174	
20	V_R	454	
21	V_{OUT}	734	
22	CAP2–	1014	
23	CAP2+	1294	
24	CAP1–	1574	
25	CAP1+	1854	
26	V_{SS}	2134	↓
27	V_{DD}	2414	–1204
28	$\overline{CK}$	2692	–1228
29	VS1	2836	↑
30	P/S	2980	
31	I/F	3124	↓
32	RES	3268	–1228
33	V_{DD}	3694	–919
34	(FSA)	3603	–796
35	(FSB)	↑	–696
36	(FSC)		–596
37	(FS0)		–496
38	(FS1)		–396
39	(FS2)	↓	–296
40	(FS3)	3603	–196
41	V_{DD}	3694	–73
42	COMSA	↑	63
43	COMS1		199
44	COM1		323
45	COM2		447
46	COM3		571
47	COM4		695
48	COM5		819
49	COM6		943
50	COM7	↓	1067
51	COM8	3694	1191
52	SEG1	3472	1228
53	SEG2	3348	1228
54	SEG3	3224	1228

PAD		COORDINATES	
No.	Name	X	Y
55	SEG4	3100	1228
56	SEG5	2976	↑
57	SEG6	2852	
58	SEG7	2728	
59	SEG8	2604	
60	SEG9	2480	
61	SEG10	2356	
62	SEG11	2232	
63	SEG12	2108	
64	SEG13	1984	
65	SEG14	1860	
66	SEG15	1736	
67	SEG16	1612	
68	SEG17	1488	
69	SEG18	1364	
70	SEG19	1240	
71	SEG20	1116	
72	SEG21	992	
73	SEG22	868	
74	SEG23	744	
75	SEG24	620	
76	SEG25	496	
77	SEG26	372	
78	SEG27	248	
79	SEG28	124	
80	SEG29	0	
81	SEG30	–124	
82	SEG31	–248	
83	SEG32	–372	
84	SEG33	–496	
85	SEG34	–620	
86	SEG35	–744	
87	SEG36	–868	
88	SEG37	–992	
89	SEG38	–1116	
90	SEG39	–1240	
91	SEG40	–1364	
92	SEG41	–1488	
93	SEG42	–1612	
94	SEG43	–1736	
95	SEG44	–1860	
96	SEG45	–1984	
97	SEG46	–2108	
98	SEG47	–2232	
99	SEG48	–2356	
100	SEG49	–2480	
101	SEG50	–2604	
102	SEG51	–2728	
103	SEG52	–2852	
104	SEG53	–2976	
105	SEG54	–3100	
106	SEG55	–3224	
107	SEG56	–3348	↓
108	SEG57	–3472	1228

(FS*) : Being fuse adjusting pins, maintain them on floating state.
CK pins : Should be V_{DD} when not being used.

PAD		COORDINATES	
No.	Name	X	Y
109	SEG58	–3694	1191
110	SEG59		1067
111	SEG60		943
112	COM16		819
113	COM15		695
114	COM14		571
115	COM13		447
116	COM12		323
117	COM11		119
118	COM10		75
119	COM9		–49
120	COMS2		–173
121	SEGSA		–335
122	SEGSB		–459
123	SEGSC		–583
124	SEGSD		–707
125	SEGSE	–3694	–831

<SED122AD**>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	NC	–3700	–1204
2	NC	–3600	↑
3	NC	–3500	
4	A0	–3252	
5	WR	–3132	
6	CS	–3012	
7	D7	–2892	
8	D6	–2772	
9	D5	–2652	
10	D4	–2532	
11	D3	–2412	
12	D2	–2292	
13	D1	–2172	
14	D0	–2052	
15	V_{DD}	–1836	
16	V_{DD}	–1736	
17	V_{SS}	–1556	
18	V_{SS}	–1456	
19	V_5	–1276	
20	V_5	–1176	
21	V_4	–996	
22	V_4	–896	
23	V_3	–716	
24	V_3	–616	
25	V_2	–436	
26	V_2	–336	
27	V_1	–156	
28	V_1	–56	
29	V_0	124	
30	V_0	224	
31	V_R	404	
32	V_R	504	
33	V_{OUT}	684	
34	V_{OUT}	784	
35	CAP2–	964	
36	CAP2–	1064	
37	CAP2+	1244	
38	CAP2+	1344	
39	CAP1–	1524	
40	CAP1–	1624	
41	CAP1+	1804	
42	CAP1+	1904	
43	V_{SS}	2084	
44	V_{SS}	2184	
45	V_{DD}	2364	
46	V_{DD}	2464	
47	CK	2693	
48	VS1	2821	
49	P/S	2949	
50	I/F	3077	
51	RES	3205	
52	NC	3500	
53	NC	3600	
54	NC	3700	–1204

PAD		COORDINATES	
No.	Name	X	Y
55	V_{DD}	3670	–910
56	(FSA)	3603	–796
57	(FSB)	↑	–696
58	(FSC)		–596
59	(FS0)		–496
60	(FS1)		–396
61	(FS2)		–296
62	(FS3)	3603	–196
63	V_{DD}	3670	–82
64	COMSA	↑	61
65	COMS1		203
66	COM1		303
67	COM2		403
68	COM3		503
69	COM4		603
70	COM5		703
71	COM6		803
72	COM7		903
73	COM8	3670	1003
74	NC	3700	1204
75	NC	3600	↑
76	NC	3500	
77	SEGS1	3319	
78	SEGS2	3219	
79	SEG1	3119	
80	SEG2	3019	
81	SEG3	2919	
82	SEG4	2819	
83	SEG5	2719	
84	SEG6	2619	
85	SEG7	2519	
86	SEG8	2419	
87	SEG9	2319	
88	SEG10	2219	
89	SEG11	2119	
90	SEG12	2019	
91	SEG13	1919	
92	SEG14	1819	
93	SEG15	1719	
94	SEG16	1619	
95	SEG17	1519	
96	SEG18	1419	
97	SEG19	1319	
98	SEG20	1219	
99	SEG21	1119	
100	SEG22	1019	
101	SEG23	919	
102	SEG24	819	
103	SEG25	719	
104	SEG26	619	
105	SEG27	519	
106	SEG28	419	
107	SEG29	319	
108	SEG30	219	1204

(FS*) : This is a fuse adjusting terminal. Set it to floating state.
CK pins : Set it to V_{DD} when not used.

PAD		COORDINATES	
No.	Name	X	Y
109	SEG31	119	1204
110	SEG32	19	
111	SEG33	–81	
112	SEG34	–181	
113	SEG35	–281	
114	SEG36	–381	
115	SEG37	–481	
116	SEG38	–581	
117	SEG39	–681	
118	SEG40	–781	
119	SEG41	–881	
120	SEG42	–981	
121	SEG43	–1081	
122	SEG44	–1181	
123	SEG45	–1281	
124	SEG46	–1381	
125	SEG47	–1481	
126	SEG48	–1581	
127	SEG49	–1681	
128	SEG50	–1781	
129	SEG51	–1881	
130	SEG52	–1981	
131	SEG53	–2081	
132	SEG54	–2181	
133	SEG55	–2281	
134	SEG56	–2381	
135	SEG57	–2481	
136	SEG58	–2581	
137	SEG59	–2681	
138	SEG60	–2781	
139	SEGS4	–2881	
140	SEGS5	–2981	
141	NC	–3081	
142	NC	–3181	
143	NC	–3281	
144	NC	–3500	
145	NC	–3600	
146	NC	–3700	1204
147	COM16	–3670	1000
148	COM15		900
149	COM14		800
150	COM13		700
151	COM12		600
152	COM11		500
153	COM10		400
154	COM9		300
155	COMS2		200
156	SEGSA		67
157	SEGSB		–33
158	SEGSC		–133
159	SEGSD		–233
160	SEGSE		–333
161	SEGSF		–433
162	SEGSG		–533
163	SEGSH		–633
164	SEGSI		–733
165	SEGSJ	–3670	–833

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
V_{DD}	Power supply	Connected to logic supply. Common with MPU power terminal V_{CC}.	1
V_{SS}	Power supply	0V power terminal connected to system ground.	1
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V1 to V4 by built-in power circuit: $V_1 = 1/5\ V_5$ (1/4 V_5) $V_2 = 2/5\ V_5$ (2/4 V_5) $V_3 = 3/5\ V_5$ (3/4 V_5) $V_4 = 4/5\ V_5$ (4/4 V_5) voltage ratings in ( ) are for optinal choices.	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit, and DC/DC source. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with V_{DD} pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Q'ty</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 ~ D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = “Low”, the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><th>P/S</th><th>RES</th><th>I/F</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3-D0</th><th>$\overline{CS}$</th><th>A0</th><th>$\overline{WR}$</th></tr>
<tr><td>“L”</td><td>—</td><td>—</td><td>SI</td><td>SCL</td><td>—</td><td>—</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>—</td></tr>
<tr><td>“H”</td><td>“H”</td><td>“H”</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>“H”</td><td>“L”</td><td>“H”</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
<tr><td>“H”</td><td>“L”</td><td>“L”</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
</table>
RES: Indicates the active potential.
OPEN: Though “OPEN” is available, fixing the potential is recommended for noise-withstnading characteristical reason.
—: Indicates that it can be set at either “H” or “L”, but fixing the potential is required.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ⌐↓. In case of an 80 series MPU, initialization can be performed by changing ⌊↑.
A reset operation is performed by edge sensing of the RES signal.
An interface type for the 68/80 series MPU is selected by input level after initialization.
“L” : 68 series MPU interface
“H” : 80 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the “Low” level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$

(E)</td><td>I</td><td><When connecting an 80 series MPU>
Active “Low”. This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
<When connecting a 68 series MPU>
Active “High”. This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/Command</th><th>Data</th><th>Serial Clock</th></tr>
<tr><td>“High”</td><td>$\overline{CS}$</td><td>A0</td><td>D0~D7</td><td>–</td></tr>
<tr><td>“Low”</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
“High”: 8-bit parallel input
“Low”: 4-bit parallel input
When P/S = “Low”, connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
<tr><td>CK</td><td>I</td><td>External input terminal
It must be fixed to “High” when the internal oscillation circuit is used.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

Dynamic drive terminal (SED1220D**/1221D**/122AD**)

Pin name	I/O	Description	Q'ty
COM1~ COM24	O	Common signal output pin (for characters)	24
COMS1, CMOS2	O	Common signal output pin (except for characters) CMOS1, CMOS2: Common output for symbol display	2
SEG1~ SEG60	O	Segment signal output pin (for characters)	60
SEGS1, 2 4, 5	O	Segment signal output pin (except for characters) SEGS1, SEGS2: Segment output for signal output	4

Dynamic drive terminal (SED1222D**)

Pin name	I/O	Description	Q'ty
COM1~ COM16	O	Common signal output pin (for characters)	16
COMS1, CMOS2	O	Common signal output pin (except for characters) CMOS1, CMOS2: Common output for symbol display	2
SEG1~ SEG60	O	Segment signal output pin (for characters)	60

Static drive terminal

Pin name	I/O	Description	Q'ty
COMSA	O	Common signal output pin (for icon)	1
SEGSA, B C, D, E F, G, H, I, J	O	Segment signal output pin (for icon) SEGSF, G, H, I, J (only SED122A)	5 to 10

Note: For the electrode of liquid crystal display panel to be connected to the static drive terminal, we recommend you to use a pattern in which it is separated from the electrode connected to the dynamic drive terminal. When this pattern is too close to the other electrode, both the liquid crystal display and electrode will be deteriorated.

FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the SED1220 Series, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting "High" or "Low" as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0~D7
"High"	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0~D7
"Low"	Serial Input	$\overline{CS}$	A0	H, L	SI	SCL	—

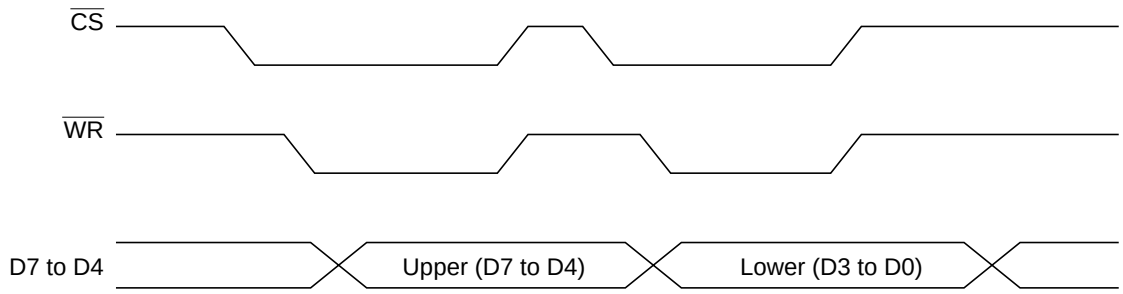
Parallel Input
In the SED1220 Series, when parallel input is selected (P/S = "High"), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either "High" or "Low" is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.
Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0~D7
↓ active	68 series	A0	E	$\overline{CS}$	D0~D7
↑ active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0~D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = "Low")

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = "Low").
When no chip is selected, the shift register and counter are reset to the initial status.
Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL).
At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.
The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = "High", it is regarded as display data. When A0 = "Low", it is regarded as a command.
The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.
Fig. 1 shows a timing chart of the serial interface.
Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length. We recommend the user to perform an operation check with a real machine.
We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

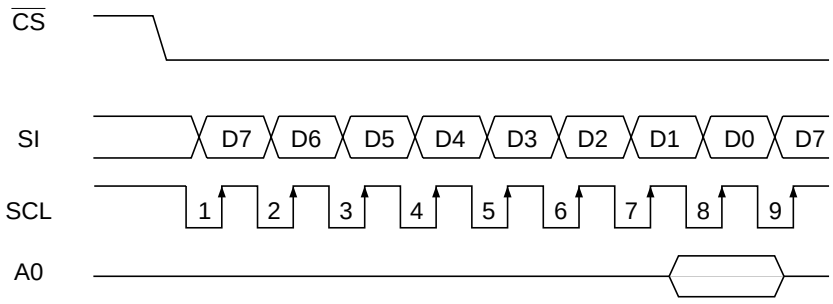


Fig. 1

Identification of data bus signals

The SED1220 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{WR}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{WR}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The SED1220 series has a chip select pin ($\overline{CS}$). Only when $\overline{CS}$ = "Low", MPU interfacing is enabled.
In any status other than Chip Select, D0 to D7 and A0, $\overline{WR}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{CS}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the SED1220 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

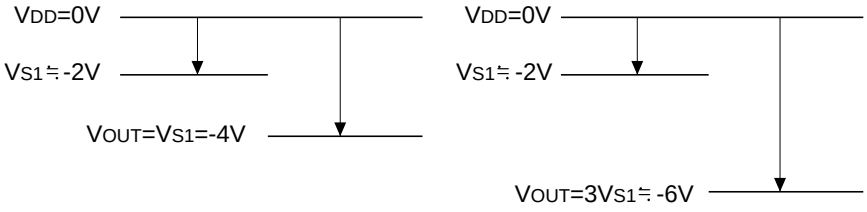
A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Amplifying circuit	Voltage regulating circuit	Voltage follower	External voltage input	Amplifying system pin
	○	○	○	—	Per specification
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V_5 pin and V_{OUT} pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and V_{OUT} pins open.

Voltage Tripler Circuit

If capacitors are connected between CAP+1 – CAP–1 and CAP2+,CAP2– and VSS VOUT, VDD– VSS potential is negatively tripled and generated at VOUT terminal. When the voltage is boosted double, open CAP2+ and connect CAP2– to VOUT terminal.
At this time, the oscillating circuit must be operating since the amplifying circuit utilize the signal from the oscillation output.



Potential relationship of amplified voltage

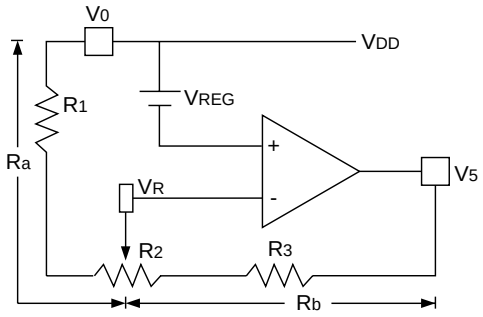
Voltage regulating circuit

Amplified voltage generated at VOUT outputs liquid crystal drive voltage V5 through the voltage regulation circuit.V5 voltage can be obtained from the expression ① below by adjusting the resistors Ra and Rb within the range of V5<VOUT.calculated by the following formula:

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{REG} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \text{①}$$

Where, VREG is the constant power supply within IC. VREG is maintained constantly at VREG ≒ 2.0V.
Voltage regulation of V5 output is done by connecting to a variable register between VR, VDD and V5. It is recommended to combine fixed registers R1 and R3 with variable resistor R2 for fine adjustment of V5 voltage.

[Sample setting on R1, R2 and R3]
- R1 + R2 + R3 = 1.2 M ohm (decided from the current value I05 passed between VDD – V5. Where, I05≤5 µA is supposed).
- Variable voltage range provided by R2 is from –4V to –6V (to be decided considering charecteristics of the liquid crystal).
- Since VREG = 2.0V, if the electronic volume register is set at (0, 0, 0, 0, 0), followings are derived from above conditions and expression ① :



R1 = 400KΩ
R2 = 200KΩ
R3 = 600KΩ

The voltage regulation circuit outputs VREG with the temperature gradient of approximately –0.04%/°C.
Since VR terminal has high input impedance, anti-noise measures must be considered including use of shortened wiring distance and shield wire.

● Voltage Regulation Circuit Using Electronic Volume Function

The electronic volume function allows to control the liquid crystal drive voltage V_5 with the commands and thus to adjust density of the liquid crystal display. Liquid crystal drive voltage V_5 can have one of 32 voltage values if 5-bit data is set to the electronic volume register.

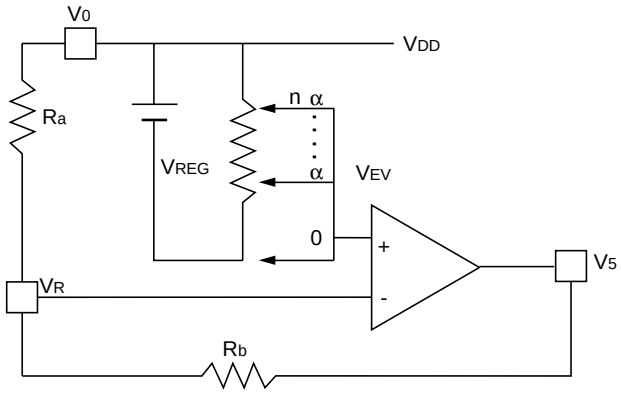
When using the electronic volume function, you need to turn the voltage regulation circuit on using the supply control command.

[Sample constants setting when electronic volume function is used]

$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{EV} \quad \cdots\cdots\cdots\cdots\cdots\cdots \textcircled{2}$$

Where $V_{EV} = V_{REG} - \alpha$

$\alpha = V_{REG} / 150$



No.	Electronic volume register	a	V_5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	(n-1)α	•
31	(1, 1, 1, 1, 1)	nα	Small

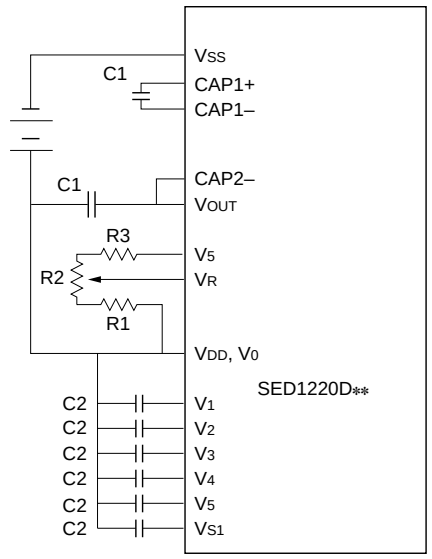
When the electronic volume function is not used, select (0, 0, 0, 0, 0) for the electronic volume register.

Liquid crystal voltage generating circuit

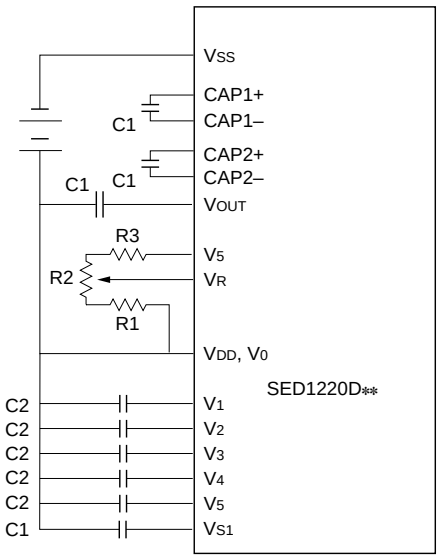
V_5 potential is resistive divided within IC to produce V_1, V_2, V_3 and V_4 potentials required for driving the liquid crystal. V_1, V_2, V_3 and V_4 potentials are then subject to impedance conversion and provided to the liquid crystal drive circuit.

The liquid crystal drive voltage is fixed to 1/5 (1/4) bias. The liquid crystal power terminals V_1 – V_5 must be externally connected with the voltage regulating capacitor C2.

When a built-in supply is used
When voltage is doubled



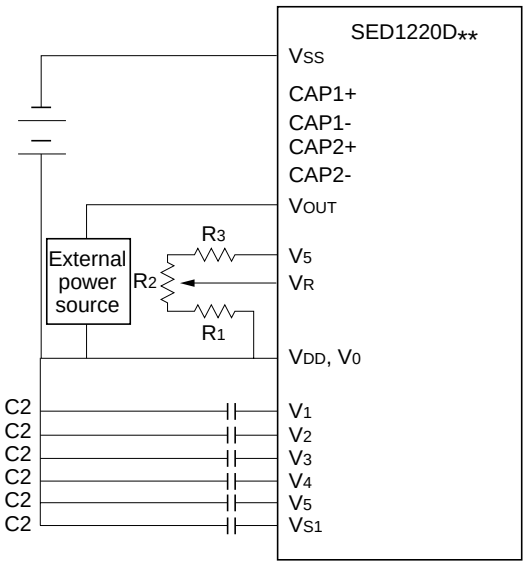
When voltage is tripled



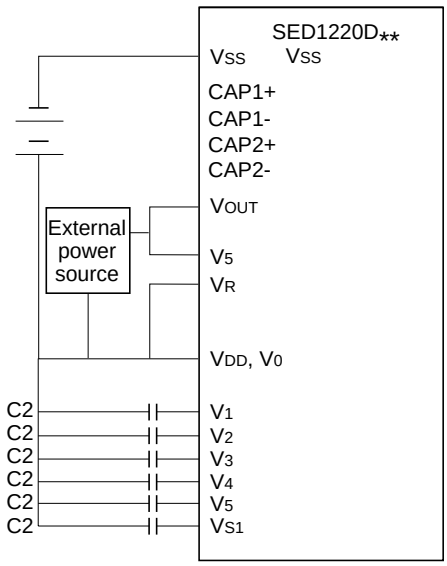
Reference setting values: C1: 0.1 - 4.7 µF
C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

Example 2: When using the built-in power source
(VC, VF, P) = (1, 1, 0)



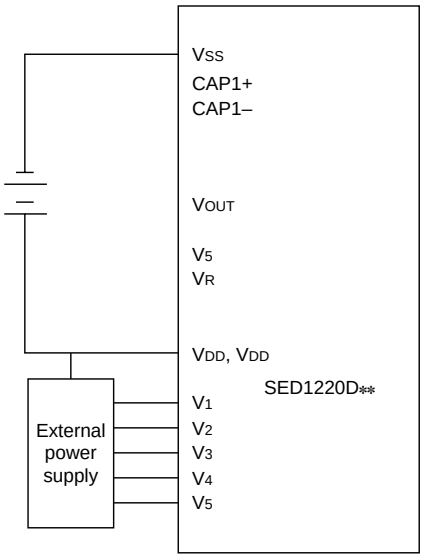
Example 3: When using the built-in power source
(VC, VF, P) = (0, 1, 0)



Reference setting values: C1: 0.47 - 4.7 µF
C2: 0.1 - 4.7 µF

We suggest you to determine the most appropriate capacitance values, fitting to the panel size, for respective capacitors C1 and C2 in consideration of the liquid crystal display and drive waveforms.

When a built-in supply is used



Low Power Consumption Mode

SED1220 is provided with standby mode and sleep mode for saving power consumption during standby period.

● Standby Mode

Switching between on and off of the standby mode is done using the power save command.
In the standby mode, only static icon is displayed.

1. Liquid crystal display output
   COM1 ~ COM24, COMS1, COMS2 : V_{DD} level
   SEG1 ~ SEG60, SEGS1, 2, 4, 5 : V_{DD} level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Can be turned on by static drives.
   Use the static icon RAM for controlling the static icon display done with SEGSA, B, C, D, E, COMSA.
2. DD RAM, CG RAM and symbol register
   Written information is saved as it is irrespective of on or off of the stand-by mode.
3. Operation mode is retained the same as it was prior to execution of the standby mode.
   The internal circuit for the dynamic display output is stopped.
4. Oscillating circuit
   The oscillation circuit for the static display must be remained on.

● Sleep Mode

To enter the sleep mode, turning off the power circuit and oscillation circuit using the commands, and then execute power save command. This mode helps to save power consumption by reducing current to almost resting current level.

1. Liquid crystal display output
   COM1 ~ COM24, COMS1, COMS2 : V_{DD} level
   SEG1 ~ SEG60, SEGS1, 2, 4, 5 : V_{DD} level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Clear all the data of the static icon registers to "0".
2. DD RAM, CG RAM and symbol register
   Written information is saved at it is irrespective of on or off the sleep mode.
3. Operation mode mode is retained the same at it was prior to execution of the sleep mode.
   All internal circuits are stopped.
4. Power circuit and oscillation circuit
   Turn off the built-in supply circuit and oscillation circuit using the power save command and supply control command.

Reset Circuit

Upon activation of the RES input, this LSI will be initialized.

● Initial State

1. Display on/off control
   C = 0 : Cursor off
   B = 0 : Blink off
   D = 0 : Display off
2. Power save
   O = 0 : Oscillation off
   PS = 0 : Power save off
3. Supply control
   VC = 0 : Voltage regulation circuit off
   VF = 0 : Voltage follower off
   P = 0 : Amplifying circuit off
4. System setting
   N2, N1 = 0 : 2 lines
   S = 0 : Left-hand shift
   CG = 0 : "CGRAM" blank
5. Electronic volume control
   Address : 28H
   Data : (0, 0, 0, 0, 0)
6. Static icon
   Address : 20H
   Data : (0, 0, 0, 0, 0)
   Address : 21H
   Data : (0, 0, 0, 0, 0)
   Address : 22H
   Data : (0, 0, 0, 0, 0)
   Address : 23H
   Data : (0, 0, 0, 0, 0)

As explained in the Section "MPU interface", the RES terminal connects to the reset terminal of the MPU and initialization is being effected together with the MPU.
However, when the bus, port, etc. of the MPU maintains high-impedance for a certain duration of time after resetting, make the resetting input to the SED1220 after the inputs to the SED1220 have become definite.
As the resetting signal, like explained in the Section "DC characteristics", active level pulses of minimum 10us or more should be used. Normal operation status can be obtained after 1us from the edge of the RES signal.
By making the RES terminal active, respective registers can be cleared and the aforesaid setting state can be obtained.
If initialization is not effected by the RES terminal when the supply voltage is applied, it may go into a state where cancellation is unworkable.
In case the built-in liquid crystal power circuit will not be used, it becomes necessary that the RES input be active when the external liquid crystal power is being applied.

COMMAND

Table 4 lists the commands. SED1220 identifies the data bus signal using different combinations of A0 and $\overline{WR}$ (E). High speed command interpretation and execution are possible since only the internal timing is used.

- **Command Overview**

Command type	Command name	A0	$\overline{WR}$
Display control instruction	Cusor Home	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
System set	System set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

Instruction execution duration of dependents on the internal process time of SED1220, therefore it is necessary to provide a duration larger than the system cycle time (t_{CYC}) between execution of two successive instruction.

- **Description of Commands**

(1) Cursor Home
This command presets the address counter to 30H and moves the cursor, when it is present, to the first digit of the first line.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

* : Don't Care

(2) Display ON/OFF Control
This command performs on or off of display and cursor setting.

Note: Symbols driven by COMSA and SEGSA – E must be controlled through the static icon RAM.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	*	D

D = 0 : Display off
1 : Display on

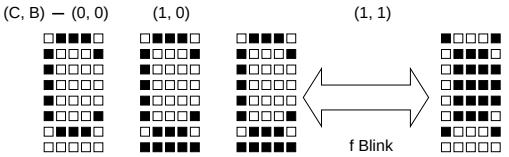
B = 0 : Cursor blink off
1 : Cursor blink on

Blink displays characters in black and white, alternately. The alternating display will be repeated with approx. 1 second interval.

C = 0 : Display of cursor
1 : Does not display

Following table shows relationship between B and C registers and the cursor.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Underbar cursor
1	1	Alternate display of display characters in black and white. The cursor position indicates the position of address



The cursor position indicates the position of address counter.

Therefore, whenever moving the cursor, change the address counter value using the RAM address set command or the auto increment done by writing the RAM data.

ISelective flashing symbol display is possible by selecting (C, B) = (1, 0) and thus locating the address counter to the position of the symbol register through selecting (since the symbol is corresponding to the character at each 5 dots).

(3) Power Save
This command is used to controlling the oscillation circuit and setting or resetting the sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

* : Don't Care

PS = 0 : Power save off (reset)
1 : Power save on (set)

O = 0 : Oscillating circuit off (stop of oscillation)
1 : Oscillating circuit on (oscilla tion)

(4) Supply Control
This command is used for controlling operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Amplifying circuit off
1 : Amplifying circuit on

Note: The oscillation circuit must be turned on for the amplitying circuit to be active.

VF = 0 : Voltage follower off
1 : Voltage follower on

VC = 0 : Voltage regulation circuit off
1 : Voltage regulation circuit on

(5) System Set
This command is used for selecting display line, common shift direction and use/non-use of CR RAM.
When power on or resetting is done, execute this command first.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	N1	N2	S	CG

∗ : Don't Care

N2, N1 = 0, 0 : 2lines
N2, N1 = 0, 1 : 3lines

S = 0 : COM left shift
= 1 : COM right shift

CG = 0 : Use CG RAM
1 : Does not use RAM

(6) RAM Address Set
This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DD RAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.
② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 H	CGRAM (00H)							–	CGRAM (01H)							–
1 0 H	CGRAM (02H)							–	CGRAM (03H)							–
2 0 H	SI							–	EV	Test						–
3 0 H	DDRAM line 1							For signals							Unused	
4 0 H	DDRAM line 2							"							"	
5 0 H	DDRAM line 3							"							"	
6 0 H	Symbol register							"							"	
7 0 H	Symbol register							"							"	

– :Unused
For signals :Output from SEGS1 to SEGS2, SEGS4, SEGS5
For symbol register :Output from COMS1 to COMS2.

SI :Static icon register
EV :Electronic volume register
Test :Test register (Do not use)

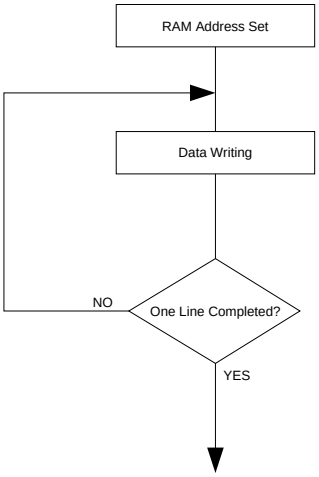
(7) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data the DD RAM, CG RAM or symbol register.
② This command automatically increases the address counter by +1, thus enabling continuous writing of data.

<Example of Data Writing>

Following figures illustrates an example of continuous writing of one line data to DD RAM.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 SED1220 Series Command List

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Display ON/OFF Control	0	0	0	0	1	1	C	B	*	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF), D = 1 (display ON) D = 0 (display OFF)
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(4) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(5) System Set	0	0	0	1	1	0	N2	N1	S	CG	Sets the use or non-use of CG RAM and shifting direction of display line (N1, N2) and COM CG = 1 (use of CG RAM), 0 = (Does not use CG RAM), M2, N1 = 0, 0 (2 lines) 0, 1 (3 lines). S = 0 (left shift), 1 (right shift).
(6) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(7) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(8) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(9) Test Mode	0	0	0	0	0	0	*	*	*	*	Command for IC chip test. Don't use this command.

CHARACTER GENERATOR

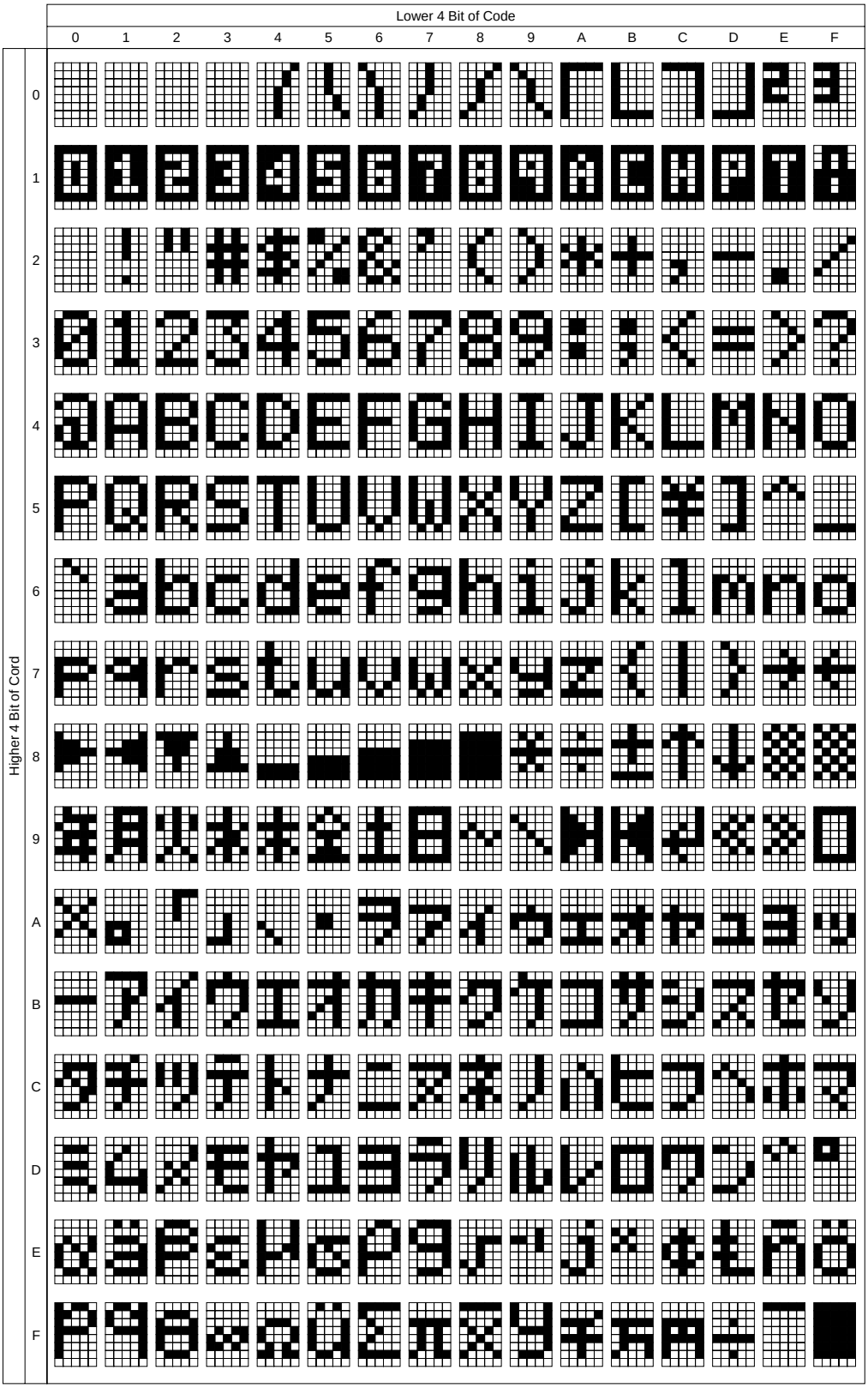
Character Generator ROM (CG ROM)

Character Generator ROM (CG ROM)
SED1220 cntains the character generator ROM (CG ROM) consisted of up to 256 types of characters.
Character size is 5×8 dots.
Tables 5 though 7 show the SED1220** character code.
Concerning the 4 characters from 00H through 03H, the system command selects on which of CG ROM and CG RAM they are to be used.
SED1220 CG ROM is mask ROM and compatible with customized ROM. Contact us for its use in your system.
Product name of modified CG ROM is defined as below:

(Example) S E D 1 2 2 0 D $\underset{\uparrow}{0}$B

Digit for CG ROM pattern change

SED1220DA*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED1220DB*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F

SED1220DG*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

Character Generator RAM (CG ROM)

CGRAM contained in SED1220 enables user programming of character patterns for display signals with higher degrees of freedom.

When using CGRAM, select it using the system command.

Capacity of CGRAM is 160 bits and accepts registration of any 4 5 × 8 dots patterns.

Following shows relationship between the CGRAM characters, CGRAM addresses and character code.

Character code	RAM address		CGRAM data (character pattern) D7 — D0								Character display SEG	Signal display SEGS 1 2 4 5
00H	00H~07H	0	*	*	*	0	1	1	1	1	■□□□□	■□ ■■
02H	10H~17H	1	*	*	*	1	0	0	0	0	□■■■■	□■ □□
		2	*	*	*	1	0	0	0	0	□■■■■	□■ □□
		3	*	*	*	0	1	1	1	1	■□□□□	■□ ■■
		4	*	*	*	0	0	0	0	1	■■■■□	□□ □■
		5	*	*	*	0	0	0	0	1	■■■■□	□□ □■
		6	*	*	*	1	1	1	1	0	□□□□□	□□ □□
		7	*	*	*	0	0	0	0	0	□□□□□	□□ □□
01H	08H~0FH	8	*	*	*	0	0	1	0	0	■■■■■	■■ ■■
03H	18H~1FH	9	*	*	*	0	0	1	0	0	■■■■■	■■ ■■
		A	*	*	*	0	1	1	1	0	□□■□□	□□ □□
		B	*	*	*	0	1	1	1	0	□□■□□	□□ □□
		C	*	*	*	0	1	1	1	0	□□■□□	□□ □□
		D	*	*	*	1	1	1	1	1	□■■■□	□■ ■□
		E	*	*	*	0	0	0	0	0	□■■■□	□■ ■□
		F	*	*	*	0	0	0	0	0	□■■■□	□■ ■□

Unused

Character data
1: Display
0: Non-display

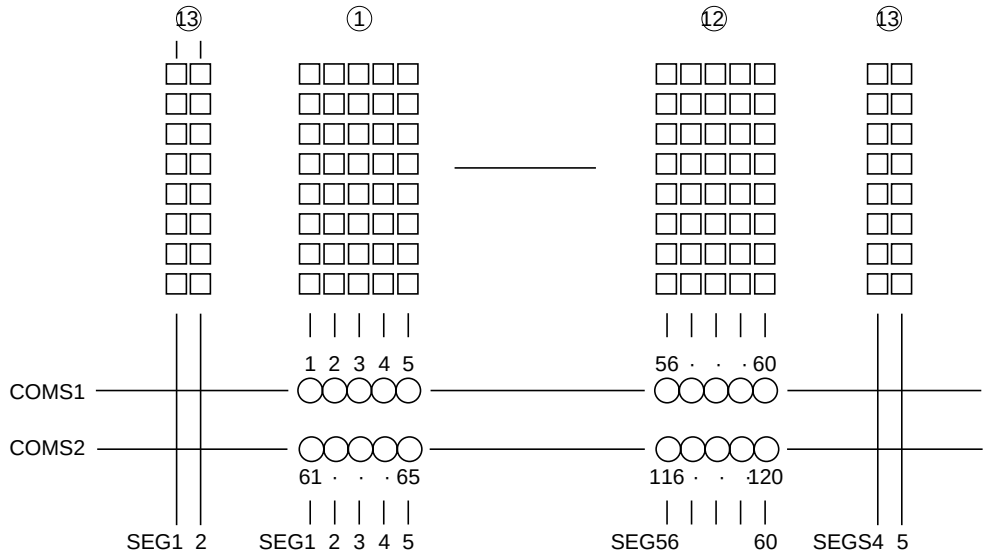
It is possible to set a 5 × 8 character size in this system. In this case, use the ∗7H/∗FH RAM. Note that the ∗7H/∗FH data is inverted when a under-bar cursor is used.

Symbol Register

SED1220 contains the symbol register which enable individual symbol setting for displaying on the screen.

Capacity of the symbol register is 120 bits and is capable of displaying up to 120 symbols.

Following shows relationship between the symbol register display patterns, RAM addresses and written data.



RAM address		Symbol Bits							
		D7							D0
60H~6BH	0	*	*	*	1	2	3	4	5
	1	*	*	*	6	7	8	9	10
	:	:							
	B	*	*	*	56	57	58	59	60
70H~7BH	0	*	*	*	61	62	63	64	65
	1	*	*	*	66	67	68	69	70
	:	:							
	B	*	*	*	116	117	118	119	120

Note: When the symbol is 1.5 times or more than the character, it is recommended to drive it using both COMS1 and COMS2.

Static Icon Ram

SED1220 contains the static icon RAM for displaying the static icons in addition to the dynamic icons.
Capacity of static icon RAM is 10 bits (SED1220/1221/1222) or 20 bit (SED122A) and is capable of displaying up to 5 icons (SED1220/1221/1222) or 10 icons (SED122A).
Following shows relationship between the static icons functions, static icon RAM addresses and written data.

< SEGSA, B, C, D, E >

Function	RAM address	Static icon data D7							D0	Display
Display On/Off	20H	*	*	*	0	0	1	1	1	S E G S A B C D E
Blink On/Off	21H	*	*	*	1	0	0	0	1	f BLINK

< SEGSF, G, H, I, J >

Function	RAM address	Static icon data D7							D0	Display
Display On/Off	22H	*	*	*	0	0	1	1	1	S E G S F G H I J
Blink On/Off	23H	*	*	*	1	0	0	0	1	f BLINK

*: Blank
1: Display or blink on
0: Display or blink off
f_{BLINK}: 1–2 Hz

Electronic Volume RAM (register)

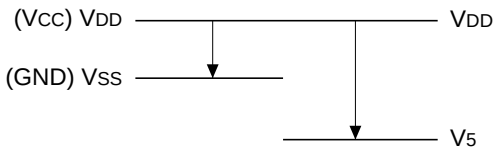
SED1220 contains the electronic volume function for controlling the liquid crystal drive voltage V5 and density of liquid crystal display. The electronic volume function enables to select one of 32 voltage status of the liquid crystal drive voltage V5 by writting 5-bit data to the electronic volume RAM.
Following shows relationship between RAM addresses set by the electronic volume and written data.

Function	RAM address	Electronic volume data D7							D0	Condition	V_{EV}
Electronic volume data	28H	*	*	*	0	0	0	0	0	0	V_{REG}–0
		*	*	*	0	0	0	0	1	1	V_{REG}–α
		*	*	*	0	0	0	0	0	2	V_{REG}–2α
							:			:	
		*	*	*	1	1	1	0	1	29	V_{REG}–29α
		*	*	*	1	1	1	1	0	30	V_{REG}–30α
		*	*	*	1	1	1	1	1	31	V_{REG}–31α
	29H	*	*	*	*	*					For testing

* : Blank
Note : Do not use the address “29H”. It is for testing
$\alpha = V_{REG}/150$

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0~+0.3	V
Power supply voltage (2)		V_5, V_{out}	–7.0~+0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5~+0.3	V
Input voltage		V_{IN}	V_{SS}–0.3~+0.3	V
Output voltage		V_O	V_{SS}–0.3~+0.3	V
Operating temperature		T_{opr}	–30~+85	°C
Storage temperature	TCP	T_{str}	–55~+100	°C
	Bare chip		–65~+125	



Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition	min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Operatable	V_{SS}		–3.6	–3.0	–2.4	V	V_{SS}
	Data retain voltage			–3.6		–2.0		*1
Power supply voltage (2)	Operatable	V_5		–7.0		–4.0	V	V_5 *2
	Operatable	V_1, V_2		0.6×V_5		V_{DD}	V	V_1, V_2
	Operatable	V_3, V_4		V_5		0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHC}		0.2×V_{SS}		V_{DD}	V	*3
Low-level input voltage		V_{ILC}		V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*3
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V		20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}			0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	Display state	V_5 = –6 V without load			80	µA	V_{DD} *5
		Standby state	Oscillation ON, Power OFF, V_{SS} = –3V without load			20	µA	V_{DD}
		Sleep state	Oscillation OFF, Power OFF, V_{SS} = –3.0V			5	µA	V_{DD}
		Access state	f_{cyc}=200KHz, V_{SS} = –3.0V			500	µA	V_{DD} *6
Input pin capacity		C_{IN}	Ta=25°C f=1MHz		5.0	8.0	pF	*3

Frame frequency	f_{FR}	Ta=25°C V_{SS}=–3.0V	70	100	130	Hz	*10
External clock frequency	f_{ck}	Display of 2 lines		23.4		KHz	*10 *11
	f_{ck}	Display of 3 lines		33.8		KHz	*10 *11

Reset time	t_R		1.0			µs	*7
Reset pulse width	t_{RW}		10			µs	*8
Reset start time	t_{RES}		50			ns	*8

Dynamic system

Built-in power supply	Input voltage	V_{S1}		–2.3	–2.1	–1.9	V	*9
	Amplified voltage output voltage	V_{OUT}	When voltage is tripled	–6.9	–6.3	–5.7	V	V_{OUT}
	Voltage follower operating voltage	V_5		–7.0		–4.0	V	
	Reference voltage	V_{REG}	Ta = 25°C	–2.06	–2.0	–1.94	V	

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

*2: When the voltage is Tripled, care must be paid to supply the voltage V_{SS} so that operating voltage of V_{OUT} and V_5 may not be exceeded.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

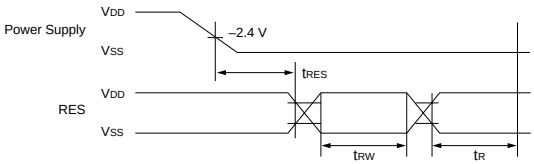
(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Character “  ” display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.

*6: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

*7: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED1220 usually enters the operating state after t_R.

*8: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.



All signal timings are based on 20% and 80% of V_{SS} signals.

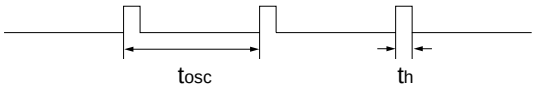
*9: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*10: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

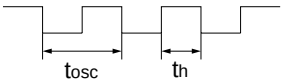
f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}

*11: When performing the operations using an external clock, not taking advantage of the built-in oscillation circuit, input the waveforms indicated below. Meanwhile, while using an external clock but when clock inputs are not being made, fix it to “H”. (Normal High)

<Incase the external clock = fosc>
- Duty = (t_h/tosc) × 100 = 20 ~ 30%
- fosc = 1/tosc

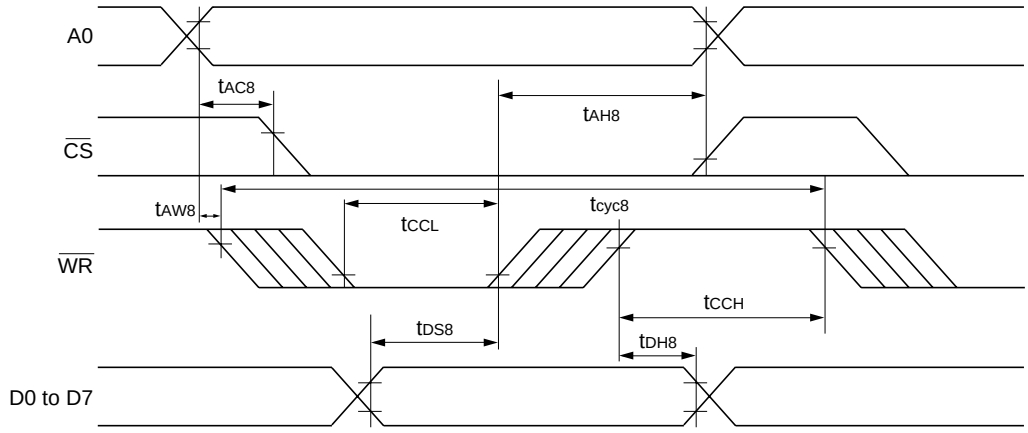


<Incase the external clock = 4 × fosc>
- Duty = (t_h/tosc) × 100 = 50%
- fosc = 1/tosc



TIMING CHARACTERISTICS

(1) MPU Bus Write Timing (80 series)



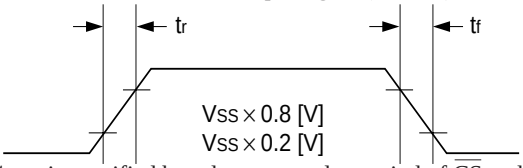
[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	Every timing is specified	30	–	ns
Address setup time		tAW8	on the basis of 20% and	60	–	ns
CS setup time		tAC8	80% of VSS.	0	–	ns
System cycle time	WR	tCYC8		650	–	ns
Write “L” pulse width (WR)		tCCL		150	–	ns
Write “H” pulse width (WR)		tCCH		450	–	ns
Data setup time	D0 ~ D7	tDS8		100	–	ns
Data hold time		tDH8		50	–	ns

[Ta = –30 to 85°C, VSS = –3.3 V to –2.7 V]

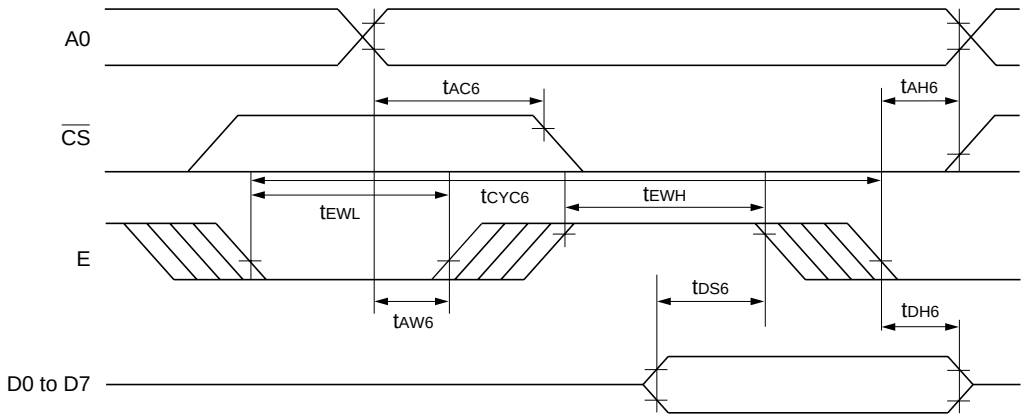
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	Every timing is specified	10	–	ns
Address setup time		tAW8	on the basis of 20% and	60	–	ns
CS setup time		tAC8	80% of VSS.	0	–	ns
System cycle time	WR	tCYC8		500	–	ns
Write “L” pulse width (WR)		tCCL		100	–	ns
Write “H” pulse width (WR)		tCCH		350	–	ns
Data setup time	D0 ~ D7	tDS8		100	–	ns
Data hold time		tDH8		20	–	ns

*1: For the rise and fall of an input signal (tr and tf), set a value not exceeding 25ns (excluding RES input).



*2: tCCL is specified based on an overlap period of CS and WR “L” levels.

(2) MPU Bus Write Timing (68 series)



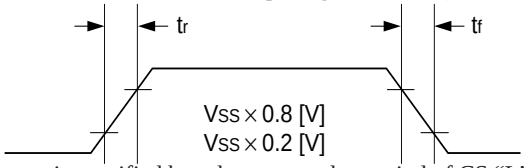
[Ta = –30 to 85°C, V_{SS} = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address setup time	A0, $\overline{CS}$	t_{AW6}	Every timing is specified	60	–	ns
Address hold time		t_{AH6}	on the basis of 20% and	30	–	ns
$\overline{CS}$ setup time		t_{AC6}	80% of V_{SS}.	0	–	ns
System cycle time	$\overline{WR}$	t_{CYC6}		650	–	ns
Enable “L” pulse width (WR)		t_{EWL}		150	–	ns
Enable “H” pulse width (WR)		t_{EWH}		450	–	ns
Data setup time	D0 ~ D7	t_{DS6}		100	–	ns
Data hold time		t_{DH6}		50	–	ns

[Ta = –30 to 85°C, V_{SS} = –3.3 V to –2.7 V]

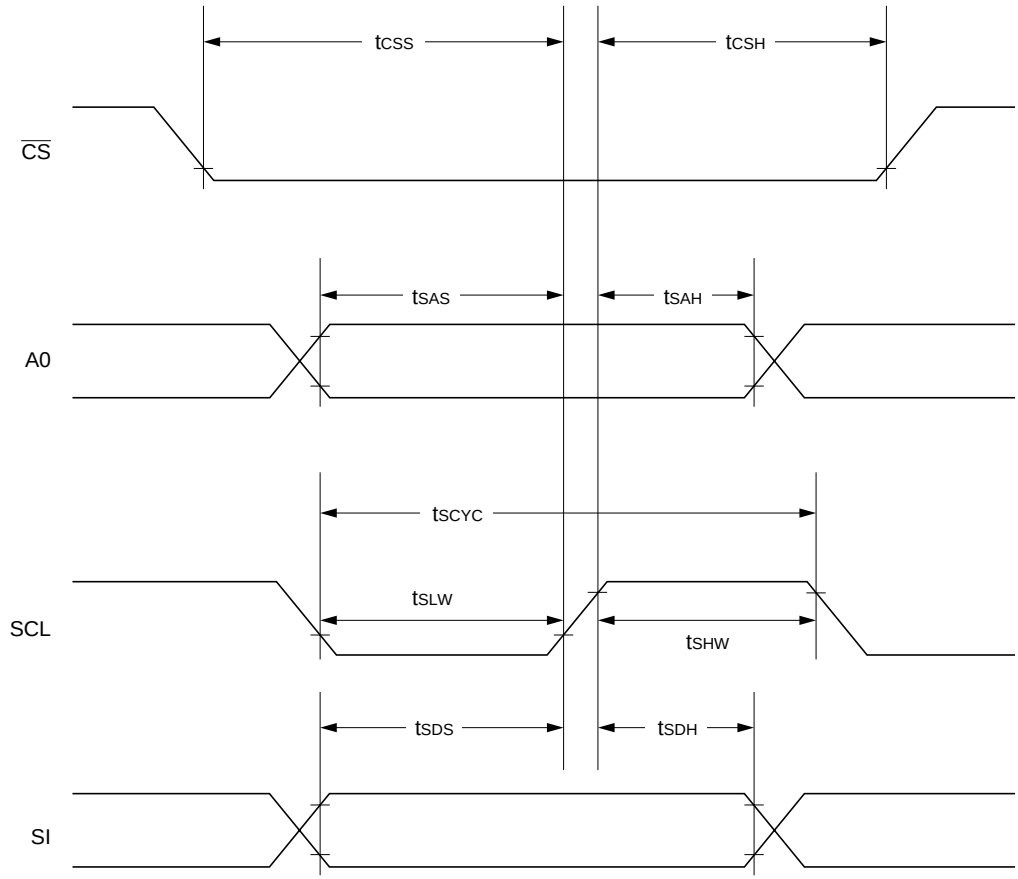
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address setup time	A0, $\overline{CS}$	t_{AW6}	Every timing is specified	60	–	ns
Address hold time		t_{AH6}	on the basis of 20% and	10	–	ns
$\overline{CS}$ setup time		t_{AC6}	80% of V_{SS}.	0	–	ns
System cycle time	$\overline{WR}$	t_{CYC6}		500	–	ns
Enable “L” pulse width (WR)		t_{EWL}		100	–	ns
Enable “H” pulse width (WR)		t_{EWH}		350	–	ns
Data setup time	D0 ~ D7	t_{DS6}		100	–	ns
Data hold time		t_{DH6}		20	–	ns

*1: For the rise and fall of an input signal (t_r and t_f), set a value not exceeding 25ns (excluding RES input).



*2: t_{EWH} is specified based on an overlap period of CS “L” and E “H” levels.

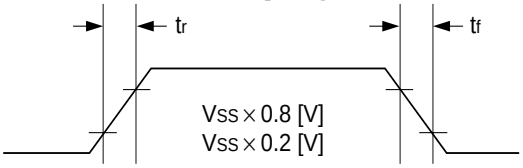
(3) Serial Interface



[Ta = –30 to 85°C, VSS = –3.6 V to –2.4 V]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	Every timing is specified	1000		ns
SCL “H” pulse width		tSHW	on the basis of 20% and	300		ns
SCL “L” pulse width		tSLW	80% of VSS.	300		ns
Address setup time	A0	tSAS		50		ns
Address hold time		tSAH		300		ns
Data setup time	SI	tSDS		50		ns
Data hold time		tSDH		50		ns
CS-SCL time	CS	tCSS		150		ns
		tCSH		700		ns

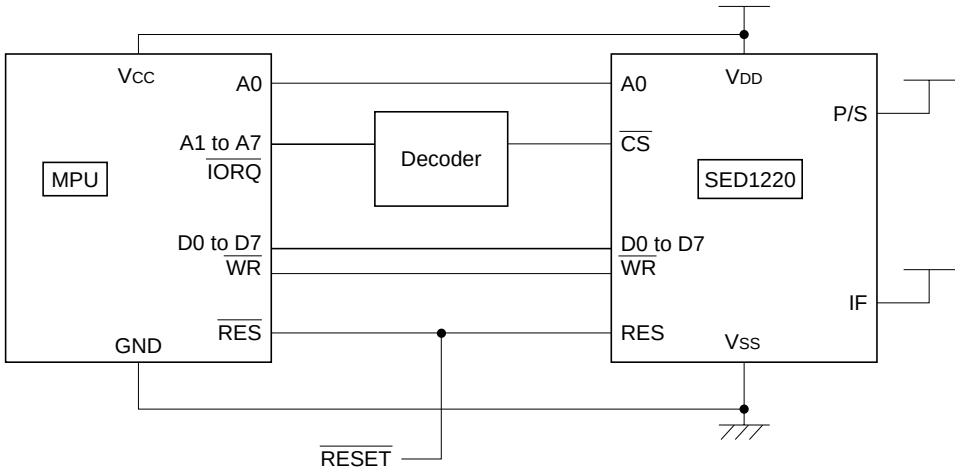
*1: For the rise and fall of an input signal (tr and tf), set a value not exceeding 25ns (excluding RES input).



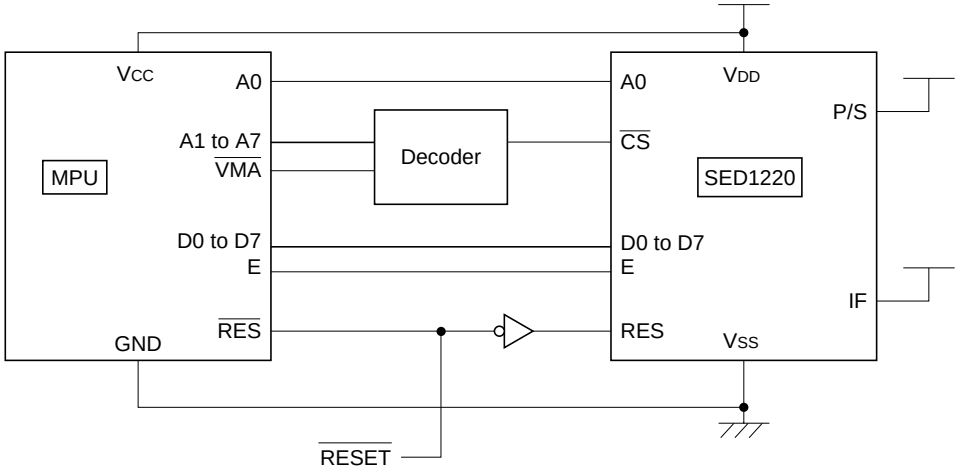
MPU INTERFACE (REFERENCE EXAMPLES)

The SED1220 Series can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the SED1220 Series can be operated by less signal lines.

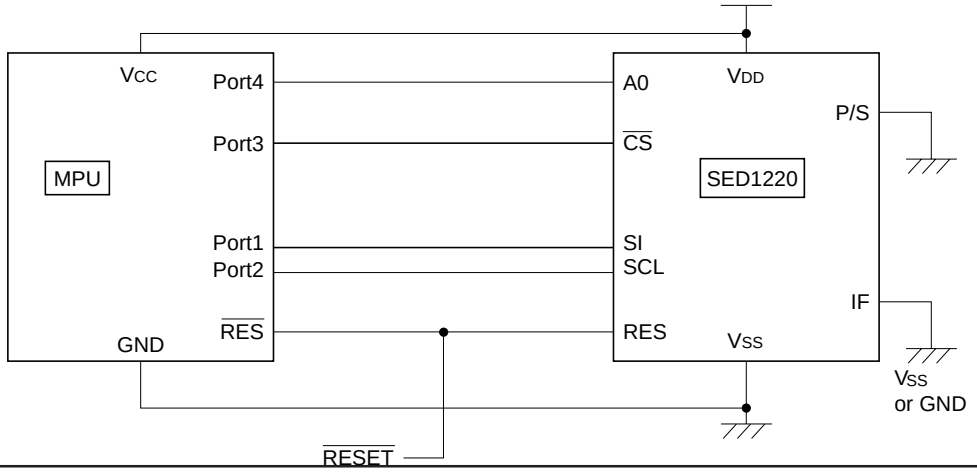
80 Series MPU



68 Series MPU

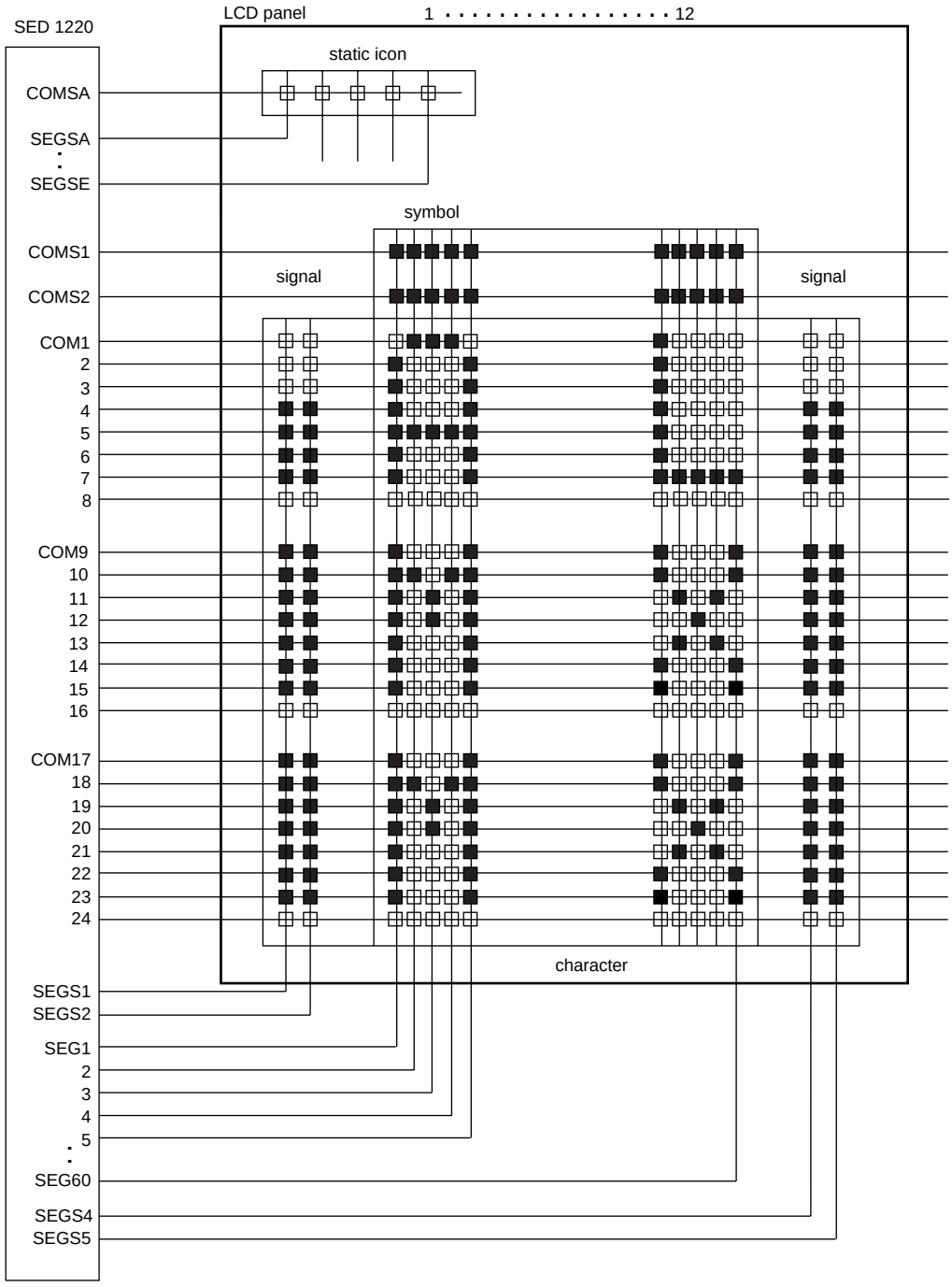


Serial Interface

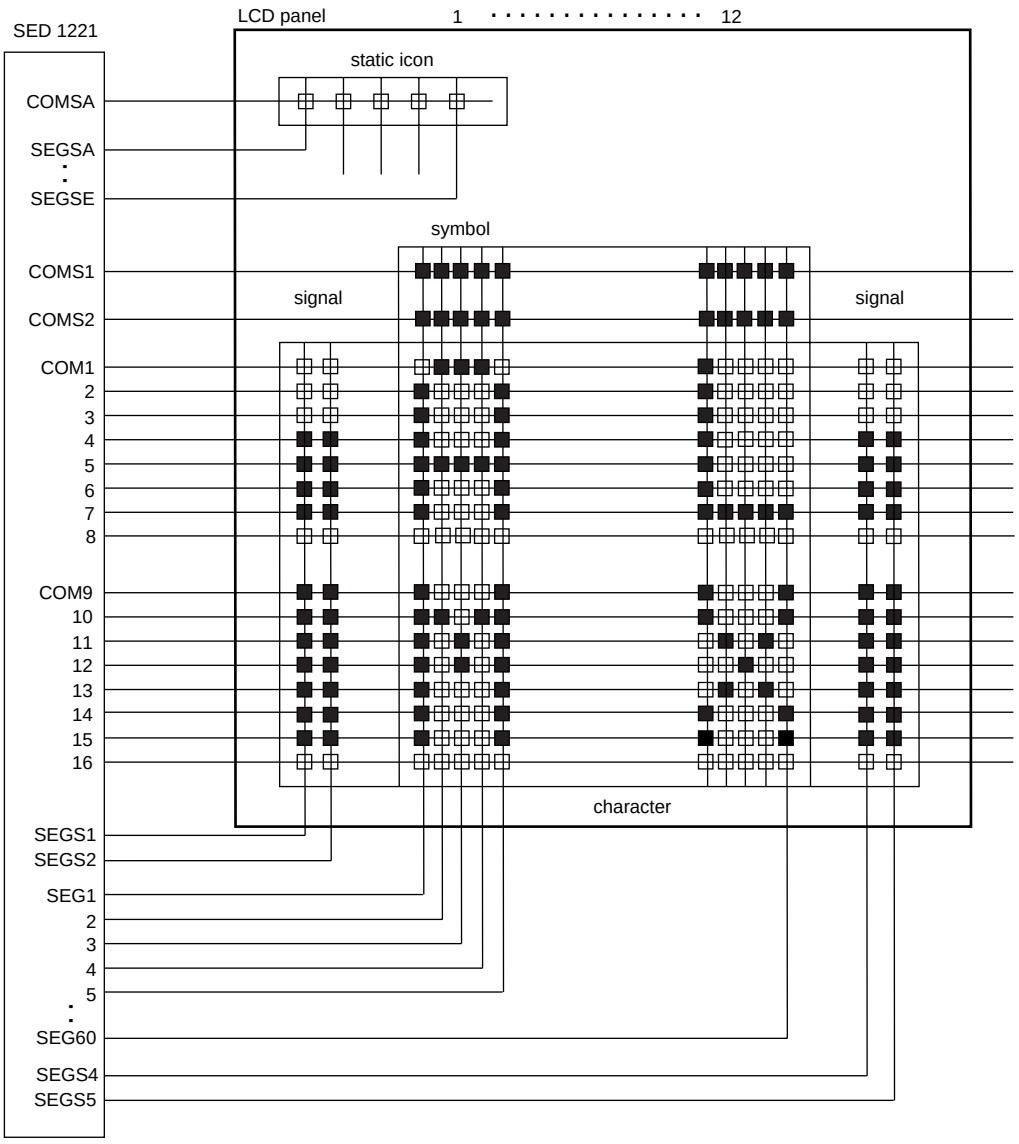


INTERFACE TO LCD CELLS (REFERENCE)

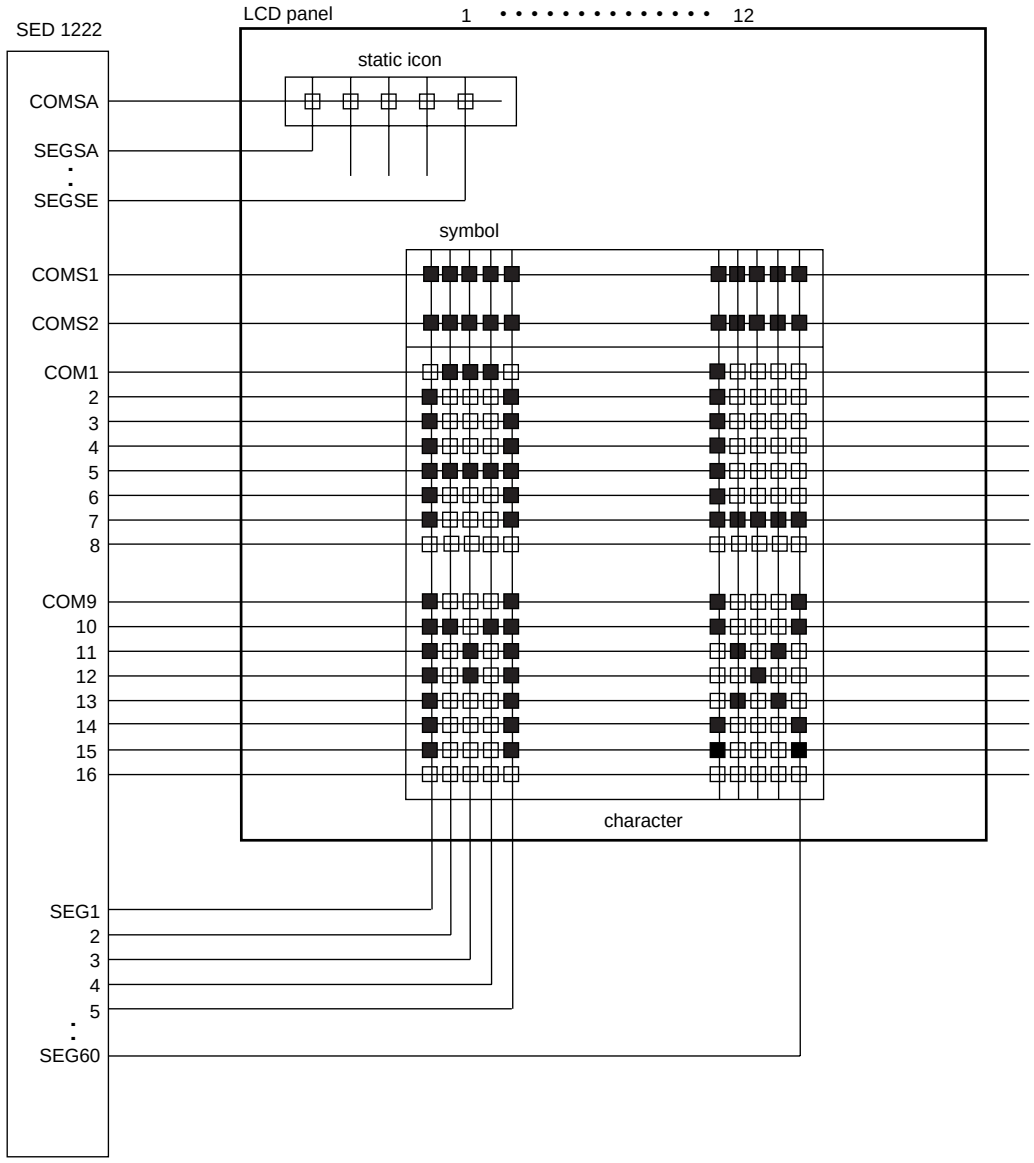
12 columns by 3 lines, 5 × 8-dot matrix segments and symbols



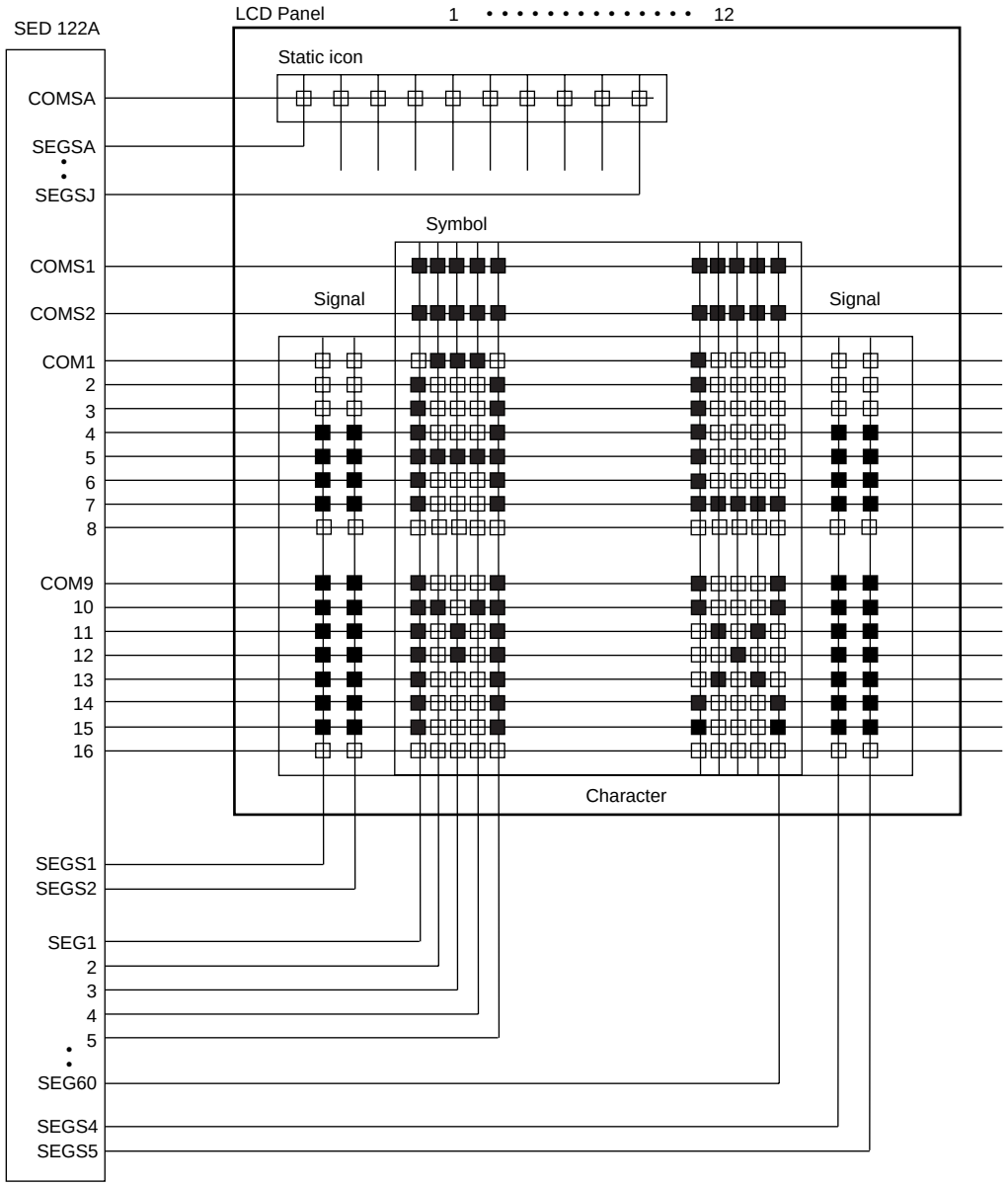
12 columns by 2 lines, 5 × 8-dot matrix segments and symbols



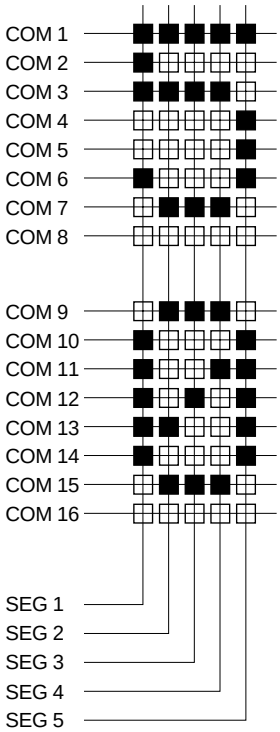
12 columns by 2 lines, 5 × 8-dot matrix segments and symbols

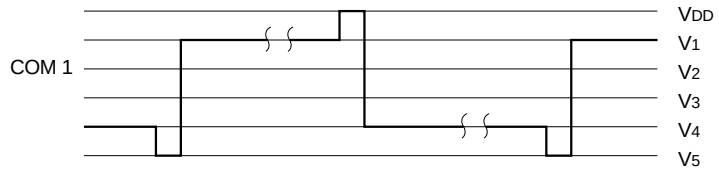


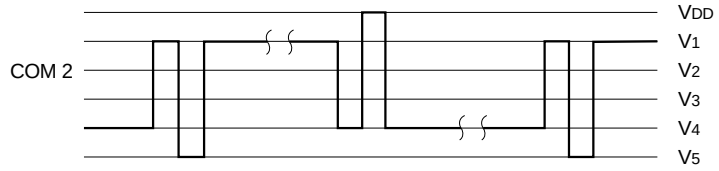
12 columns by 2 lines, 5 × 8-dot matrix segments and symbols

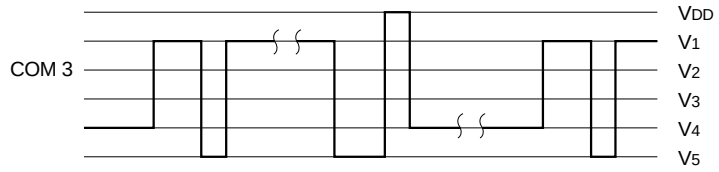


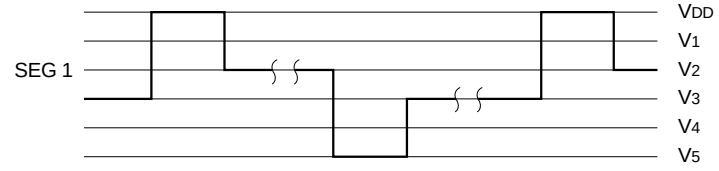
LIQUID CRYSTAL DRIVE WAVEFORMS (B WAVEFORMS)

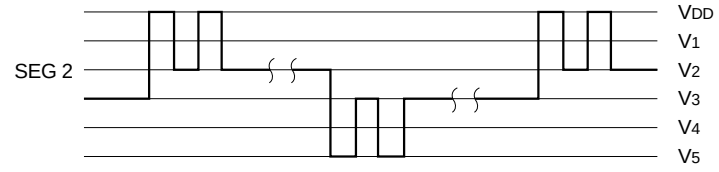


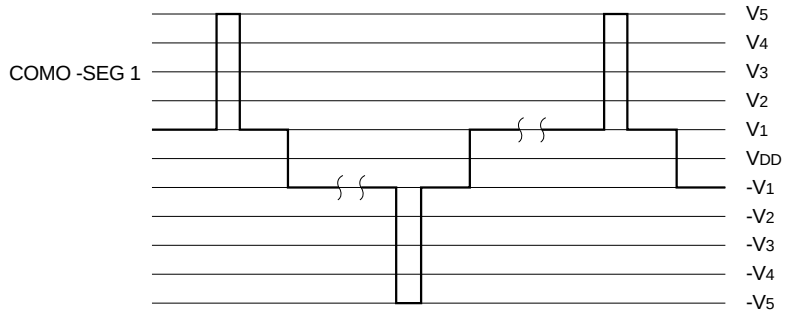


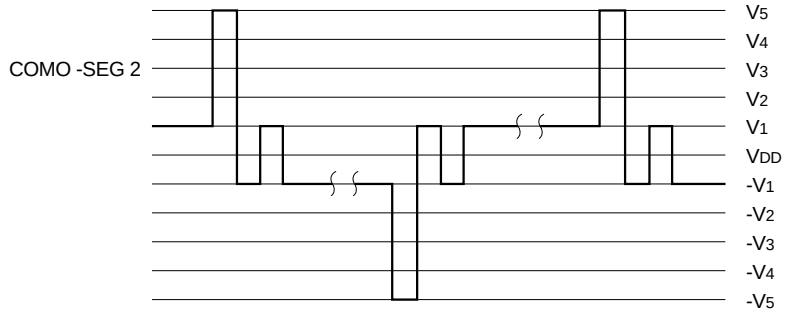






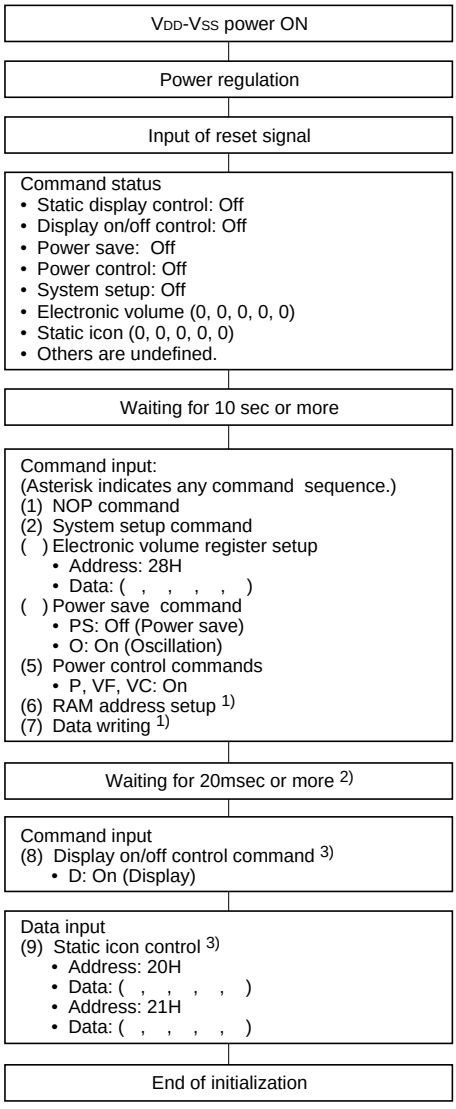




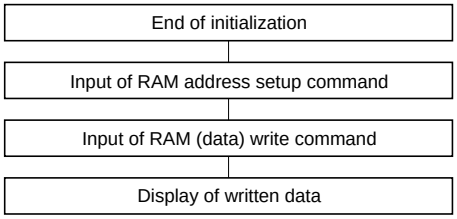


Instruction Setup Example (Reference Only)

(1) Initial setup



(2) Display mode

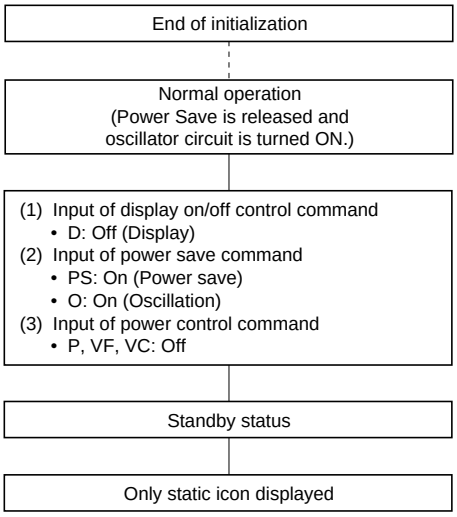


Notes 1) Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
• DDRAM: Write the 20H data (character code).
• CGRAM: Write the 00H data (null data).
• Symbol register: Write the 00H data (null data).
As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

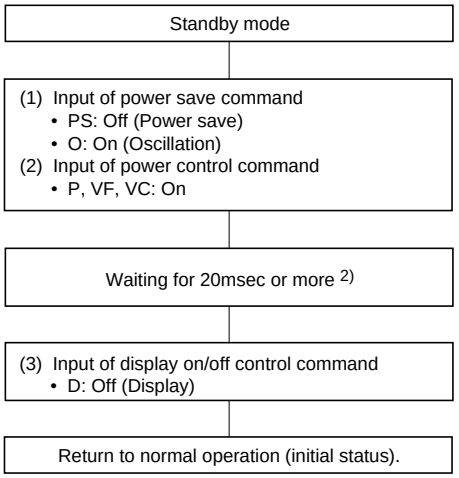
2) Since it is specified based on rise characteristics of the booster, power control and voltage follower circuits, time to be set differs depending on external capacity. Be sure to set it after the external capacity is confirmed.

3) A display of the dynamic drive series is turned on when the on command is input and the static icon is turned on using the static icon control command.
To turn both on at the same time when the display is turned on, execute display on/off command and static icon control within 1 frame period.

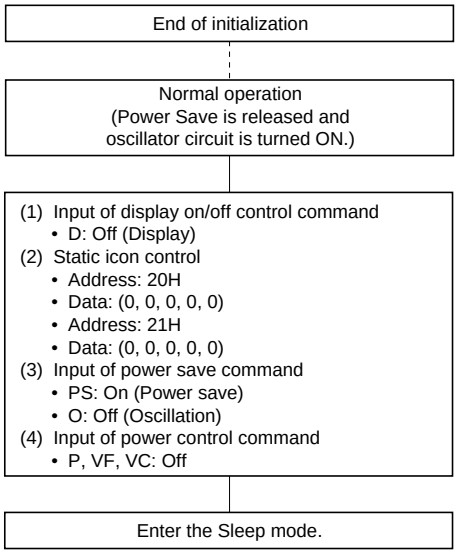
(3-1) Selecting the Standby mode



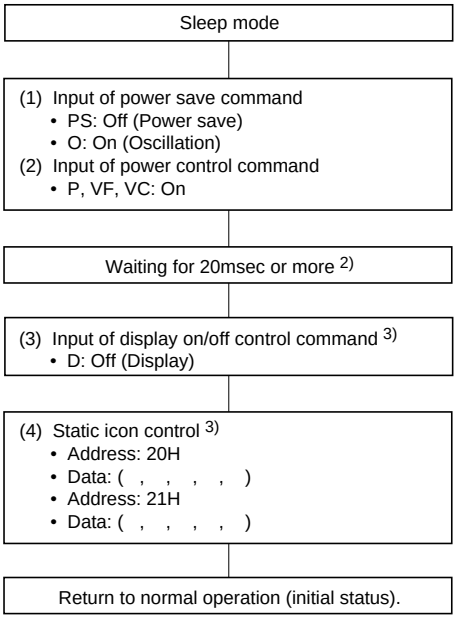
(3-2) Releasing the Standby mode



(4-1) Selecting the Sleep mode



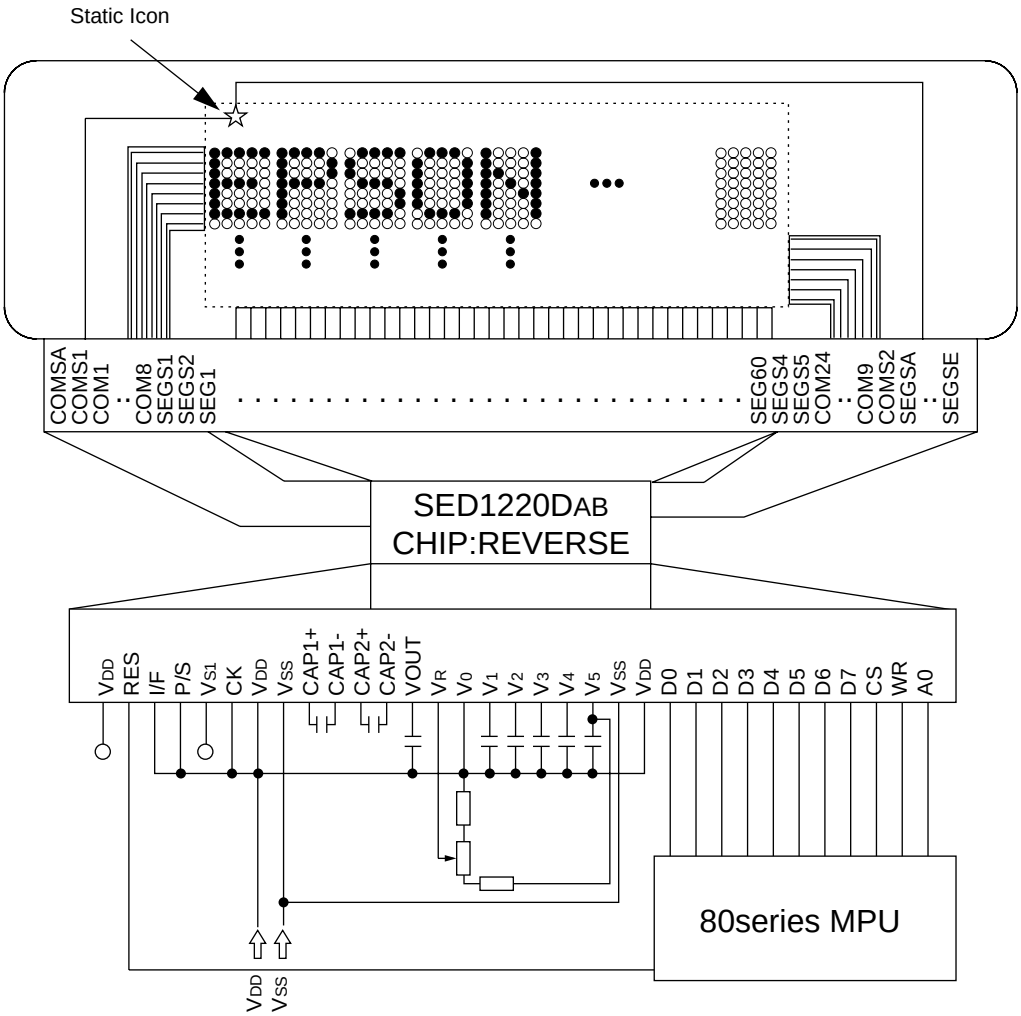
(4-2) Releasing the Sleep mode



Instruction Setup Example of SED1220 series

(1) Initial setup
(2) display ON “EPSON”
(3) Display ON the Icon
(4) Standby Mode sequence
(5) Releasing the Standby Mode sequence

<Diagram of SED1220Txx and LCD Panel>



(1) Initial setup

(1.1) V_{DD}–V_{SS} Power ON

(1.2) Power regulation

(1.3) Input of RESET signal

(1.4) Command Status

- Display ON/OFF :OFF
- Power save :OFF
- Power control :OFF
- System reset :OFF
- Electronic Volume :(0, 0, 0, 0, 0)
- Static display control :OFF
- Others are undefined.

(1.5) Waiting for 10μ sec or more

(1.6) Command Input: ((*) indicates any command sequence.)

(a) System Setup command: CGRAM→Not use, 3lines, COM Left shift

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1	0	0

(*) Electronic volume resister setup: Data→(0, 0, 0, 0, 0, 0)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0

(*) Power save command: PS→0, 0→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	0

(d) Power Control command: P, VF, VC→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	1	1

(e) (f) RAM address setup, Data writing

• RAM address setup: Set address is 30H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0

• Data writing: All data→20H (for 1 Line)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• RAM address setup: Set address is 40H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	0	0	0

• Data writing: All data→20H (for 2 line)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• RAM address setup: Set address is 50H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	0	0	0

• Data writing: All data →20H (for 3 Line)

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0

• End of Initialization

(2) Display ON “EPSON”

(2.1) RAM address setup command: 30H

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0

(2.2) Data writing command: Writing “EPSON”

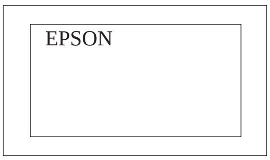
A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	1	0	0	0	1	0	1	E: 45H
1	0	0	1	0	1	0	0	0	0	P: 50H
1	0	0	1	0	1	0	0	1	1	S: 53H
1	0	0	1	0	0	1	1	1	1	O: 4FH
1	0	0	1	0	0	1	1	1	0	N: 4EH

(2.3) Waiting for 20ms or more

(2.4) Display ON/OFF control command: B, C→0, D→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1

Display ON 5×7 Dots “EPSON”



(3) Display ON The Icon: Valid in Standby mode only
(3.1) Display ON/OFF command: D→OFF

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	0

(3.2) Static display control command: 1 ~ 2Hz Blink

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1
1	0	0	0	0	1	0	0	0	0

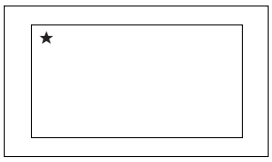
(3.3) Power save command: PS→ON, 0→ON

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	1

(3.4) Power control commands: P, VF, VC→OFF

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	0	0	0

Display ON the Icon



(4) Releasing the Standby Mode
(4.1) Power save command: PS→0, 0→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0/1	0/1	1	0

(4.2) Power control commands: P, VF, VC→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	1	1

(4.3) Waiting for 20ms or more

(4.4) Display ON/OFF command: D→1

A0	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	0	1

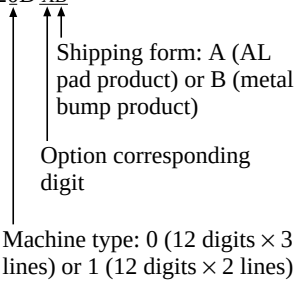
END of Releasing the Standby mode

Option List

SED1220 provides the optional functions as described in the following. Being adaptable to the customer's optional demand, contact the Business Department of our company when installed.

○ Our product name corresponding to a customer's option is defined as shown below:

(Example) SED1220D XB



1. Specification of Character Generator ROM (CGROM)
   SED1220 integrates a character generator ROM which can generate a maximum of 256 type characters. The size of these characters is composed of 5 × 7 (8) dots.
   Being a mask ROM, the SED1220 CGROM is adaptable to the character generator ROM exclusive for the customer, too.
   For our standard CGROMs, refer to the Character Fonts Table.
2. Specification of Liquid Crystal Driver Voltage Bias Value.
   SED1220 integrates a liquid crystal diver voltage generator circuit. Its 5-volt potential is divided into resistance inside of IC to generate 1-V, 2-V, 3-V or 4-V potential as required for the liquid crystal driver. Further, the 1-V, 2-V, 3-V or 4-Vpotential is converted into impedance by a voltage follower to be supplied to the liquid crystal driver circuit.
   Either 1/5 or 1/4 bias value can be selected as demanded by the customer.
   Our standard bias value is preset to 1/5.
3. Specification of Reference Voltage of Liquid Crystal Driver Voltage Regulation Circuit.
   SED1220 integrates a voltage regulation circuit using a booster voltage as its power supply to generate 5V for the liquid crystal driver via the voltage regulation circuit.
   The voltage regulation circuit integrates a reference voltage regulator V_{REG}.
   The customer can select a specification of using either the internal reference voltage or external V_{SS} reference voltage.
   Our standard specification is preset to the internal reference voltage.
4. Power Supply to Booster Circuit
   SED1220 integrates a booster circuit.
   The customer can select a specification of using either the regulator output V_{S1} or V_{SS} as the supply voltage to the booster circuit.
   Our standard specification is preset to the regulator output V_{S1}.
5. External Clock Specifications
   SED1220 integrates an external clock terminal and there are two clock specifications, f and 4×f oscillation.
   Either of them can be selected on your request.

	Internal oscillation	External clock f osc.	External clock 4×f osc.
Standard	○	○	×
Optional	○	×	○

   The standard external clock specification is set to f_{OSC}.

6. Reset Signal Input Polarity Specifications
   SED1220 inputs reset signal from the reset terminal using edge detection and I/F specification 80/68 series can be selected according to this signal level. RES input polarity can also be selected on your request.

RES input polarity	Type	
	Standard	Optional
↓	68 series	80 series
↑	80 series	68 series

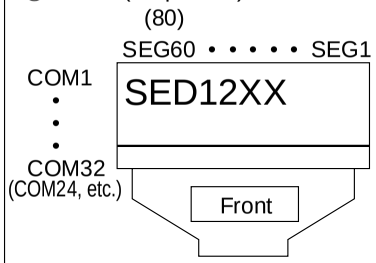
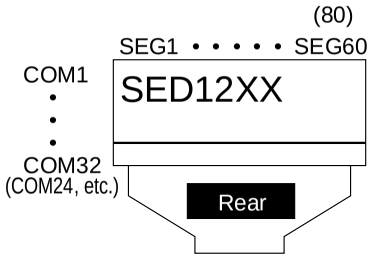
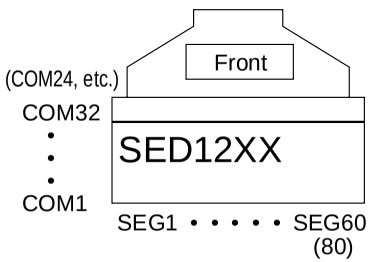
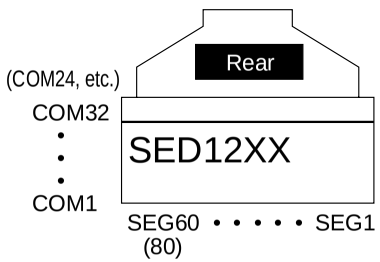
   ↓ is set to the 68 series and ↑ to the 80 series as the standard RES input polarities.

7. Pad Layout Specifications of COMS1 Symbol Terminal
   On SED1220, pad layout of COMS1 symbol terminal can be changed. COMS1 pad layout can be selected on your request.

	Standard	Optional
Pad No	Pad Name	Pad Name
65	COMS1	COM1
66	COM1	COM2
67	COM2	COM3
68	COM3	COM4
69	COM4	COM5
70	COM5	COM6
71	COM6	COM7
72	COM7	COM8
73	COM8	COMS1

SED1220/1225/1240 Example of System Setup Depending on Mount Direction

Reference

	① Case1 (Chip Front)	② Case2 (Chip Rear)	③ Case3 (Chip Front)	④ Case4 (Chip Rear)
				
SED1220	• Unable to correspond with commands. • Only able to correspond with custom fonts.	○ System set • S = 0	○ System set • S = 1	• Unable to correspond with commands. • Only able to correspond with custom fonts.
SED1225	○ System set • S1 = 0 • S2 = 1 (Horizontally-reversed)	○ System set • S1 = 0 • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 1 (Horizontally-reversed)
SED1240	○ System set • CS = 0 • SS = 1 (SEG-reversed) However, the input of DDRAM address of "SED12XX" from the first digit of the first line shall be 3FH and 3EH, in this order (as it is reversed in the unit of character).	○ System set • CS = 0 • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 1 (SEG-reversed) However, the input of DDRAM address of "SED12XX" from the first digit of the first line shall be 3FH and 3EH, in this order.