SED1225 Series
LCD Controller/Drivers

Technical Manual

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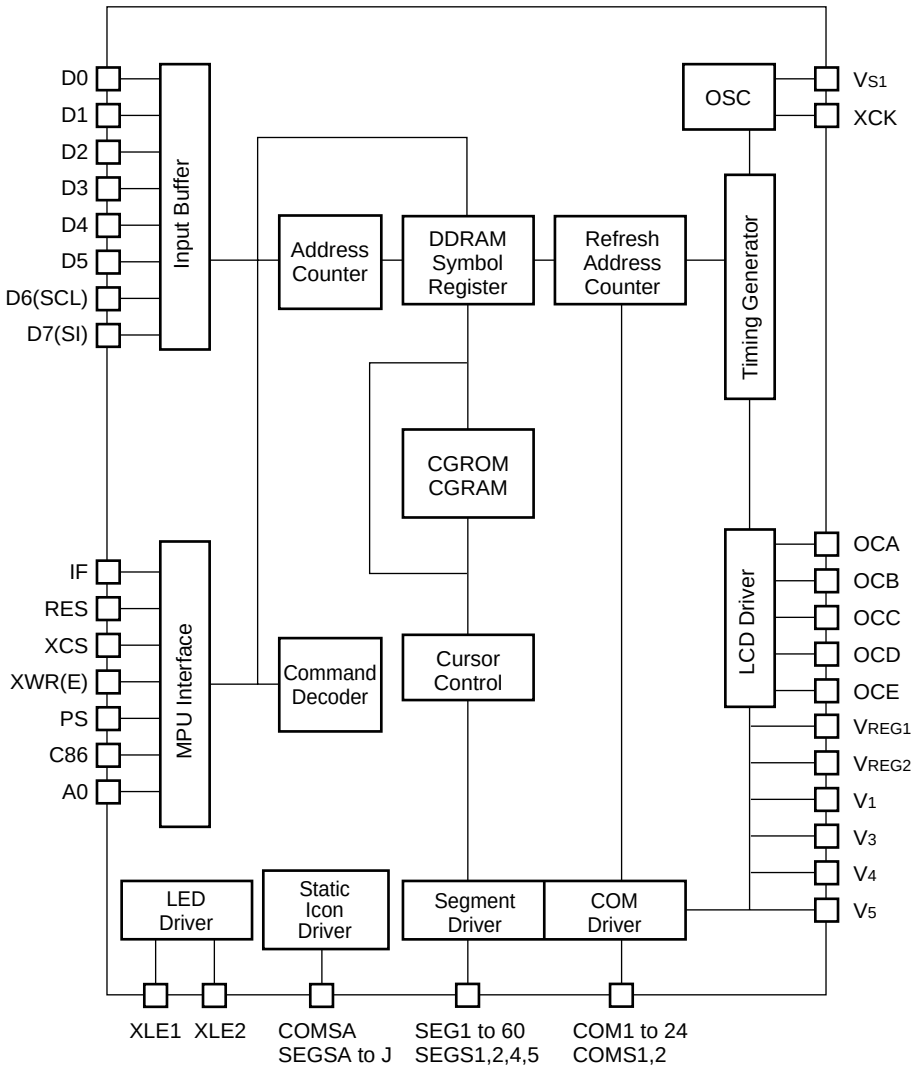
OUTLINE

The SED1225 dot-matrix LCD Controller Driver receives 4-bit, 8-bit, or serial data from the microprocessor and displays up to 36 characters, four user-defined characters, and up to 120 symbols.
Up to 256 types of built-in character generator ROMs are provided. Each character font has a 5×8-dot structure. Also, the user-defined character RAM contains four 5×8-dot characters. In addition, a symbolic register can be used for flexible symbol display. The Driver featuring the very low power consumption can drive a handy terminal unit in either Sleep or Standby mode with the minimum power consumption.

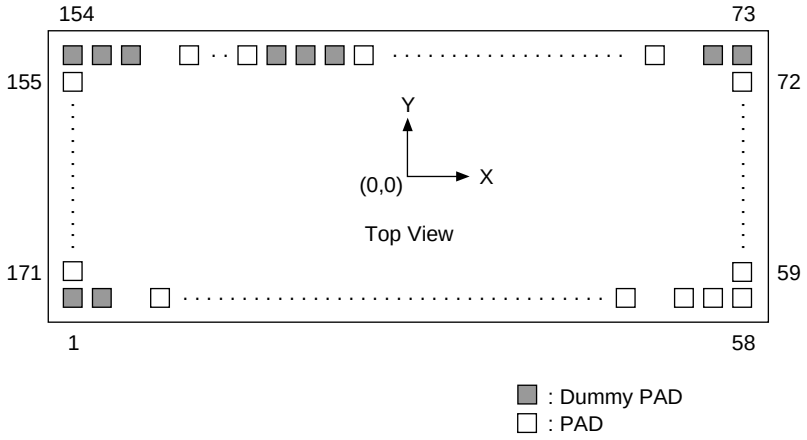
FEATURES

- Built-in display data RAM
  Can display up to 36 characters, 4 user-defined characters, and 120 symbols.
- Built-in CGROM (for 256-character display), CGRAM (for 4-character display), and symbol register (for 120 symbol display)
- No. of display columns by lines
  Normal mode: (12 columns plus 4 signal segments) × 3 line + 120 symbols + 10 static symbols
  Standby mode: 10 static symbols
- Built-in C&R oscillators
- Available external clock input
- High-speed MPU interfaces
  Interface to both 68- and 80-series MPUs
  Support of 4/8-bit interface
- Support of serial interface
- Character font: 5x8 dots
- Duty ratio: 1/18, 1/26
- Simple command setup
- Built-in LCD drive power circuit: Power amp and regulator
- Built-in electronic controls
- Very low power consumption
  30 µA (including the operating current of the built-in power supply during normal operation)
  10 µA (Static icon display during Standby operation
  5 µA (Display off during Sleep operation)
- Power supplies
  V_{DD} – Vss: –1.7 to –3.6 V
  V_{DD} – V_5: –3.0 to –6.0 V
- Wide operating temperature range: Ta=-30 to +85°C
- CMOS process
- Package design
  Chip (with gold bump): SED1225D✻B
  TCP: SED1225T✻✻
- This IC package is not designed to have a radiation or strong light resistance.

BLOCK DIAGRAM



PIN ASSIGNMENT



SED1225D**
↑
CGROM pattern version number

Chip size: 7.85 × 1.97 mm
Pad pitch: 90 µm (min)
Chip thickness (Reference): 625 µm

Au bump specifications
Bump size:
Pad Nos. 59 to 72, and 155 to 171: 78 µm × 59 µm
Pad Nos. 1 to 58, and 73 to 154: 59 µm × 78 µm
Bump height (Reference): 22.5 µm

Pad coordinates (1/2)

PAD		Coordinate	
No.	Name	X	Y
1	Dummy	-3768	-822
2	Dummy	-3678	-822
3	A0	-3349	-822
4	XWR(E)	-3200	-822
5	XCS	-3050	-822
6	D7(SI)	-2901	-822
7	D6(SCL)	-2751	-822
8	D5	-2602	-822
9	D4	-2452	-822
10	D3	-2303	-822
11	D2	-2153	-822
12	D1	-2004	-822
13	D0	-1854	-822
14	XLE1	-1705	-822
15	XLE1	-1615	-822
16	XLE2	-1466	-822
17	XLE2	-1376	-822
18	V_{DD}	-1286	-822
19	V_{DD}	-1197	-822
20	V_{SS}	-1107	-822
21	V_{SS}	-1017	-822
22	V_5	-868	-822
23	V_5	-778	-822
24	V_4	-629	-822
25	V_4	-539	-822
26	V_3	-389	-822
27	V_3	-300	-822
28	V_1	-150	-822
29	V_1	-60	-822
30	(V_{REG1})	89	-822
31	(V_{REG1})	179	-822
32	V_{REG2}	328	-822
33	V_{REG2}	418	-822
34	OCA	567	-822
35	OCA	657	-822
36	OCB	807	-822
37	OCB	896	-822
38	OCC	1046	-822
39	OCC	1136	-822
40	OCD	1285	-822
41	OCD	1375	-822
42	OCE	1524	-822
43	OCE	1614	-822

PAD		Coordinate	
No.	Name	X	Y
44	V_{SS}	1718	-822
45	V_{SS}	1808	-822
46	C86	1973	-822
47	PS	2122	-822
48	IF	2272	-822
49	RES	2421	-822
50	XCK	2571	-822
51	VS1	2720	-822
52	(FSA)	2893	-822
53	(FSB)	3065	-822
54	(FSC)	3237	-822
55	(FS3)	3409	-822
56	(V_{DD})	3589	-822
57	(V_{DD})	3678	-822
58	(V_{DD})	3768	-822
59	(FS2)	3758	-628
60	(FS1)	3758	-456
61	(FS0)	3758	-283
62	COMSA	3758	-179
63	COMS1	3758	-90
64	COM1	3758	0
65	COM2	3758	90
66	COM3	3758	179
67	COM4	3758	269
68	COM5	3758	359
69	COM6	3758	449
70	COM7	3758	538
71	COM8	3758	628
72	COMS1	3758	718
73	Dummy	3768	822
74	Dummy	3678	822
75	SEGS1	3409	822
76	SEGS2	3320	822
77	SEG1	3230	822
78	SEG2	3140	822
79	SEG3	3050	822
80	SEG4	2961	822
81	SEG5	2871	822
82	SEG6	2781	822
83	SEG7	2692	822
84	SEG8	2602	822
85	SEG9	2512	822
86	SEG10	2423	822

Note 1 : Set the pins V_{DD} of Nos. 56 to 58 and the pins V_{RBG1} of Nos. 30 and 31 to the floating state.

2 : Since the pins FS* of Nos. 52 to 55 and 59 to 61 are for fuse adjustment, set them to the floating state.

Pad coordinates (2/2)

PAD		Coordinate	
No.	Name	X	Y
87	SEG11	2333	822
88	SEG12	2243	822
89	SEG13	2153	822
90	SEG14	2064	822
91	SEG15	1974	822
92	SEG16	1884	822
93	SEG17	1795	822
94	SEG18	1705	822
95	SEG19	1615	822
96	SEG20	1526	822
97	SEG21	1436	822
98	SEG22	1346	822
99	SEG23	1256	822
100	SEG24	1167	822
101	SEG25	1077	822
102	SEG26	987	822
103	SEG27	898	822
104	SEG28	808	822
105	SEG29	718	822
106	SEG30	629	822
107	SEG31	539	822
108	SEG32	449	822
109	SEG33	359	822
110	SEG34	270	822
111	SEG35	180	822
112	SEG36	90	822
113	SEG37	1	822
114	SEG38	-89	822
115	SEG39	-179	822
116	SEG40	-268	822
117	SEG41	-358	822
118	SEG42	-448	822
119	SEG43	-538	822
120	SEG44	-627	822
121	SEG45	-717	822
122	SEG46	-807	822
123	SEG47	-896	822
124	SEG48	-986	822
125	SEG49	-1076	822
126	SEG50	-1165	822
127	SEG51	-1255	822
128	SEG52	-1345	822
129	SEG53	-1435	822

PAD		Coordinate	
No.	Name	X	Y
130	SEG54	-1524	822
131	SEG55	-1614	822
132	SEG56	-1704	822
133	SEG57	-1793	822
134	SEG58	-1883	822
135	SEG59	-1973	822
136	SEG60	-2062	822
137	SEGS4	-2152	822
138	SEGS5	-2242	822
139	Dummy	-2332	822
140	Dummy	-2422	822
141	Dummy	-2512	822
142	COM24	-2602	822
143	COM23	-2692	822
144	COM22	-2781	822
145	COM21	-2871	822
146	COM20	-2961	822
147	COM19	-3050	822
148	COM18	-3140	822
149	COM17	-3230	822
150	COM16	-3320	822
151	COM15	-3409	822
152	Dummy	-3589	822
153	Dummy	-3678	822
154	Dummy	-3768	822
155	COM14	-3758	718
156	COM13	-3758	628
157	COM12	-3758	538
158	COM11	-3758	449
159	COM10	-3758	359
160	COM9	-3758	269
161	COMS2	-3758	179
162	SEGSA	-3758	90
163	SEGSB	-3758	0
164	SEGSC	-3758	-90
165	SEGSD	-3758	-179
166	SEGSE	-3758	-269
167	SEGSF	-3758	-359
168	SEGSG	-3758	-449
169	SEGSH	-3758	-538
170	SEGSI	-3758	-628
171	SEGSJ	-3758	-718

PIN DESCRIPTION

Power Supply Pins

Pin Name	I/O	Description	No. of Pins
V_{DD}	Power supply	Connects to the logic power supply. This is common to the Vcc power pin of the MPU.	1
V_{SS}	Power supply	0V power pin connected to system ground (GND)	2
V_1, V_3 V_4, V_5	Power supply	Multi-level LCD drive power supplies. A capacitor is required for external stabilization.	4
V_{S1}	O	Output pin of oscillator (OSC) power voltage. Do not connect any external load to this pin.	1

Notes: Two V_{SS} pins are provided. As they are commonly connected inside the IC, an input into any V_{SS} can be used if power impedance is low. To have the enough noise resistance, however, the V_{SS} power input from each pin is recommended.

LCD Power Pins

Pin Name	I/O	Description	No. of Pins
V_{REG2}	O	Output pins of LCD voltage and amp source power supplies. A capacitor is required for stabilization.	1
OCA OCB OCC OCD OCE	O	A voltage capacitor pin. A capacitor is required for amplification.	5

LED Drive Terminal

Pin Name	I/O	Description	No. of Pins
XLE1 XLE2	O	An Nch open drain output terminal to drive the LED. Connects to the LED cathode.	2

System Bus Connector Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descrition</th><th>No. of Pins</th></tr>
<tr><td>D7(SI)
D6(SCL)
D5 to D0</td><td>I</td><td>An 8-bit input data bus to be connected to the standard 8- or 16-bit MPU data bus. Pins D7 and D6 function as the serial data and clock inputs respectively if PS is logical low.
<table>
<tr><th>PS</th><th>C86</th><th>IF</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3 to D0</th><th>XCS</th><th>A0</th><th>XWR</th></tr>
<tr><td>"L"</td><td>—</td><td>—</td><td>SI</td><td>SCL</td><td>OPEN</td><td>OPEN</td><td>OPEN</td><td>XCS</td><td>A0</td><td>—</td></tr>
<tr><td>"H"</td><td>"H"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>XCS</td><td>A0</td><td>E</td></tr>
<tr><td>"H"</td><td>"H"</td><td>"L"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>XCS</td><td>A0</td><td>E</td></tr>
<tr><td>"H"</td><td>"L"</td><td>"H"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>XCS</td><td>A0</td><td>XWR</td></tr>
<tr><td>"H"</td><td>"L"</td><td>"L"</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>XCS</td><td>A0</td><td>XWR</td></tr>
</table>
Open : May be open. However, the potential is recommended to fix to have better noise-resistance characteristics.
- : May be high or low. However, the potential must be fixed.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, the most significant bit of MPU address bus is connected to identify data or command.
0: Indicates D0 to D7 are command.
1: Indicates D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>Initializes when RES is set to low. The system is reset at RES signal level.</td><td>1</td></tr>
<tr><td>XCS</td><td>I</td><td>A Chip Select signal. The address bus signal is decoded and entered.
This is valid when low.</td><td>1</td></tr>
<tr><td>XWR</td><td>I</td><td>- When an 80-series MPU is connected
Active low.
The WR signal of 80-series MPU is connected. The data bus signal is fetched at the rising edge of XWR signal.
- When a 68-series MPU is connected
Active high.
Used as an Enable Clock input of 68-series MPU. The data bus signal is fetched at the falling edge of XWR signal.</td><td>1</td></tr>
<tr><td>PS</td><td>I</td><td>A switching pin between serial data input and parallel data input.
<table>
<tr><th>P/S</th><th>Chip select</th><th>Data/Command</th><th>Data</th><th>Serial Clock</th></tr>
<tr><td>"H"</td><td>XCS</td><td>A0</td><td>D0 to D7</td><td>—</td></tr>
<tr><td>"L"</td><td>XCS</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>An interface data length select pin during parallel data input.
- 8-bit parallel input if IF=high
- 4-bit parallel input if IF=low
This pin is connected to V_{DD} or V_{SS} if PS=low.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>An MPU interface switch pin.
- 68-series MPU interface if C86=high
- 80-series MPU interface if C86=low
This pin is connected to V_{DD} or V_{SS} if PS=low.</td><td>1</td></tr>
<tr><td>XCK</td><td>I</td><td>An external clock input pin.
It must be fixed to high to use the internal oscillator.
To use an external clock input, turn the internal oscillator OFF by issuing the command.</td><td>1</td></tr>
</table>

LCD Driver Signals

Dynamic drive pins

Pin Name	I/O	Description	No. of Pins
COM1 to COM24	O	Common signal output pins (for character display)	24
COMS1, COMS2	O	Common signal output pins (for non-character display) COMS1, COMS2: Common outputs for symbol display	3
SEG1 to SEG60	O	Segment signal output pins (for character display)	60
SEGS1, 2 4, 5	O	Segment signal output pins (for non-character display) SEGS1, 2, 4, 5: Segment outputs for signal output	4

Note: As the same COMS1 signal is output at two pins, one of them must be used.

Static drive pins

Pin Name	I/O	Description	No. of Pins
COMSA	O	Common signal output pin (for icon display)	1
SEGSA, B C, D, E, F G, H, I, J	O	Segment signal output pin (for icon display)	10

Notes: We recommend to separate LCD panel electrodes of static drive pins from those of dynamic drive pins. If these patterns are closely located, the LCD and its electrodes may be deteriorated.

FUNCTION DESCRIPTION

MPU Interfaces

Interface type selection

The SED1225 can transfer data via the 4- or 8-bit data bus or via the serial data input (SI). The parallel or serial data input can be selected by setting the PS pin to high or low (see Table 1).

Table 1

PS	Type	XCS	A0	XWR	SI	SCL	D0 to D7
H	Parallel input	XCS	A0	XWR	–	–	D0 to D7
L	Serial input	XCS	A0	H, L	SI	SCL	–

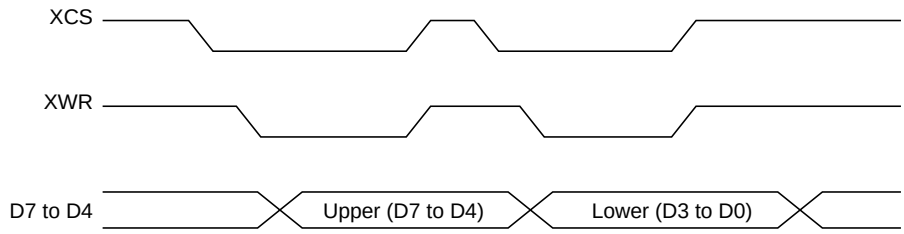
The SED1225 has the C86 pin for MPU selection. If the parallel input is selected (PS=high), if can be connected directly to the 80-series or 68-series MPU by setting the C86 pin to high or low (see Table 2). Also, the 8-bit or 4-bit data bus can be selected by the IF pin signal.

Table 2

C86 pin signal	Type	A0	XWR	XCS	D0 to D7
"L"	80 series	A0	XWR	XCS	D0 to D7
"H"	68 series	A0	E	XCS	D0 to D7

Interface to 4-bit MPU

If the 4-bit interface is selected (IF=low), the 8-bit command and data, and its address are transferred in two times.



Note: During continuous writing, the write time greater than the system cycle time (tcyc) must be set before the subsequent write operation.

Serial interface

The serial interface consists of an 8-bit shift register and a 3-bit counter. During chip select (XCS=low), an SI input and an SCL input can be accepted. During no chip select (XCS=high), the shift register and counter is initialized (reset).
Serial data of D7 to D0 are fetched in this order from the serial data input pin (SI) at the rising edge of serial clock. The data is converted into 8-bit parallel data at the rising edge of the eighth serial clock.
The serial data input (SI) is identified to have the display data or command by the A0 input. It is display data if A0=high, and it is command if A0=low.
The A0 input is fetched and identified at the rising edge of "8 × n-th" serial clock (SCL). Figure 1 shows a serial interface timing chart.
The SCL signals must be well protected from the far-end reflection and ambient noise due to increased line length. The operation checkout on the actual machine is recommended.
Also, we recommend to repeat periodical command writing and status refreshing to avoid a malfunction due to noise.

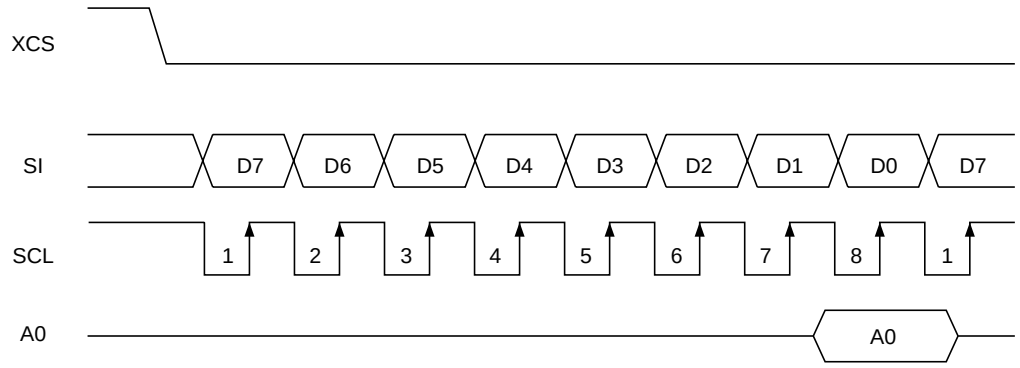


Figure 1

Data bus signal identification

The SED1225 identifies the data bus based on a combination of A0, AWR and E signals as defined on Table 3.

Table 3

Common	68 Series	80 Series	Function
A0	E	XWR	
1	1	0	Writes in the RAM and symbol register.
0	1	0	Writes (commands) in the internal register.

Chip Select

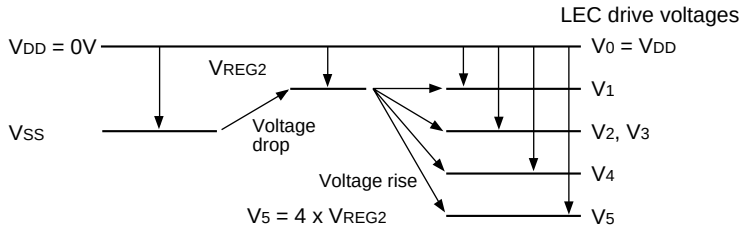
The SED1225 has an Chip Select pin (XCS) to allow an MPU interface input only if XCS=low.
During no chip select status, all of D0 to D7, A0, XWR, SI and SCL inputs are made invalid. If the serial input interface is selected, the shift register and counter are reset.
However, the Reset signal is entered independent from the XCS status.

Power Circuit

The built-in power circuit featuring the low power consumption generates the required LCD drive voltages. The power circuit consists of an amp and a voltage regulator.

Amp

When the capacitors are connected to the OCA, OCB, OCC, OCD, OCE, V_{REG2} pins, the LCD drive voltages are generated.
As the amp uses the signals from the oscillator, the oscillator or an external clock must be operating.
The following provides the potential relationship.



Voltage regulator

- Voltage regulator using the electronic control function
  Use the electronic control function and set the voltages appropriate to the LCD panel driving.
  When a 5-bit data is set in the electronic control register, one of 32-state voltages can be set for LCD driving. Before using the electronic control function, turn ON the power circuit by issuing the power control command.
  The following explains how to calculate the voltages using the electronic control function.

$V_5 = 4 \times V_{EV}$

Conditions:

$V_{EV} = V_{REG2} - X$

where,

$X = n\alpha$ (n=0, 1, ..., 31)

$\alpha = V_{REG2}/95$

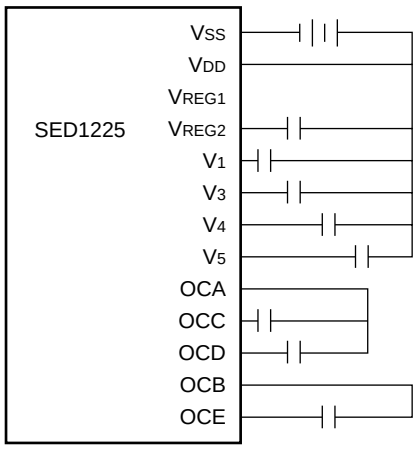
No.	Electronic control register	X	V_5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	n-1α	•
31	(1, 1, 1, 1, 1)	nα	Small

This is reference voltage for the liquid crystal drive power circuit. The V_{REGZ} has a temperature characteristics of about –0.05%/deg.

External unit connection examples

An external voltage regulation capacitor must be connected to the LCD power pin. The LCD drive voltages are fixed to 1/4 biasing.

1/4 bias example



Note: We recommend to display the capacitance appropriate to the LCD panel size and set up the capacitance by observing the drive signal waveforms.

Reference set value: (0.1~1.0 μF)

Power Save mode

The SED1225 supports the Standby and Sleep modes to save the power consumption during system idling.

- Standby mode
  The Standby mode is selected or released by the Power Save command. During Standby mode, only the static icon is displayed.
  1. LCD display outputs
     COM1 to COM16, COMS1, COMS2:
     V_{DD} level
     SEG1 to SEG60, SEGS1, 2, 4, 5:
     V_{DD} level
     SEGSA, B, C, D, E, F, G, H, I, J, COMSA:
     Can light by static drive
     Use the Static Icon RAM to display the static icon with SEGSA, B, C, D, E, F, G, H, I, J and COMSA.
  2. DDRAM, CGRAM and symbol register
     Their write contents do not change. The contents are kept regardless of Standby mode selection or release.
  3. The operation mode before selection of Standby mode is kept.
     The internal circuits for dynamic display are stopped.
  4. Oscillator
     The oscillator must be turned ON for static display.
- Sleep mode
  To select the Sleep mode, turn OFF the power circuit and oscillator by issuing the command, and clear all data of Static Icon register to zero. Then, issue the Power Save command. The system power consumption will be minimized to almost the stopped status.
  1. LCD display outputs
     COM1 to COM16, COMS1, COMS2:
     V_{DD} level
     SEG1 to SEG60, SEGS1, 2, 4, 5:
     V_{DD} level
     SEGSA, B, C, D, E, F, G, H, I, J, COMSA:
     Clear all data of Static Icon register to zero.
  2. DDRAM, CGRAM and symbol register
     Their write contents do not change. The contents are kept regardless of Standby mode selection or release.
  3. The operation mode before selection of Standby mode is kept.
     All internal circuits are stopped.
  4. Oscillator
     Turn OFF the built-in power supply and oscillator by issuing the Power Save and power control commands.

Reset Circuit

When the RES input is made active, this LSI is initialized.

- Initialization status
  - (1) Display ON/OFF control
    - C=0: Cursor off
    - B=0: Blink off
    - DC=0: Normal display
    - D=0: Display off
  - (2) Power save
    - O=0: Oscillating circuit off
    - PS=0: Power save off
  - (3) Power control
    - P=0: Power circuit off
  - (4) System set
    - N=0: 3 lines
    - S2, S1=0: Direction of normal display
    - CG=0: CGRAM unused
  - (5) Electronic control
    - Address: 28H
    - Data: (0,0,0,0,0)
  - (6) Static icon
    - Address: 20H to 23H
    - Data: (0,0,0,0,0)
  - (7) LED register
    - Address: 2AH
    - Data: (0,0,0,0,0)
  - (8) CG RAM, DD RAM and symbol register
    - Address: 00H to 1FH, 30H to 7CH
    - Data: Must be initialized by MPU after reset input because of being indefinite.

Connect the RES terminal to the MPU reset terminal as described in "6-1 MPU Interface", and execute initialization simultaneously with the MPU. However, if the MPU bus and port are put into high impedance for a certain time period by resetting, perform reset input to the SED1225 after the input to the SED1225 has been determined. When the RES terminal becomes "L", each register is cleared and the above setup is established. If initialization by the RES terminal is not performed when power voltage is applied, resetting may be disabled.

COMMAND

Table 4 lists the supported commands. The SED1225 identifies a data bus by a combination of A0, XWR and E signals. It features high-speed processing as the commands are analyzed and executed in the internal timing only.

- Command outline

Table 4

Command type	Command name	A0	XWR
Display control instruction	Cursor Home	0	0
	Display On/Off Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
System setup	System Setup	0	0
Address control instruction	Address Setup	0	0
Data input instruction	Data Write	1	0

As the execution time of each instruction depends on the internal processing time of the SED1225, an enough time greater than the system cycle time (tcyc) must be assigned for continuous instruction execution.

- Explanation of commands

(1) Cursor Home

The Cursor Home command presets the Address counter to 30H, and shifts the cursor to column 1 of line 1 if Cursor Display is ON.

A0	XWR	D7							D0
0	0	0	0	0	1	✻	✻	✻	✻

✻ : Don't Care

(2) Display On/Off Control

The Display On/Off Control command sets the LCD character and cursor display.

A0	XWR	D7							D0
0	0	0	0	1	1	C	B	DC	D

✻ : Don't Care

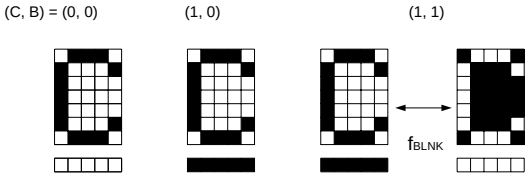
D=0: Turns the display off.
D=1: Turns the display on.
DC=0: Selects the standard size display.
DC=1: Selects the double-height vertical display.
B=0: Turns cursor blinking off.
B=1: Turns cursor blinking on.

During blinking, the cursor character is alternately displayed normally and reversely. The normal and reverse display is repeated approximately every one second.

C=0: Does not display the cursor.
C=1: Displays the cursor.

The following provides the relationship between the C and B registers and cursor display.

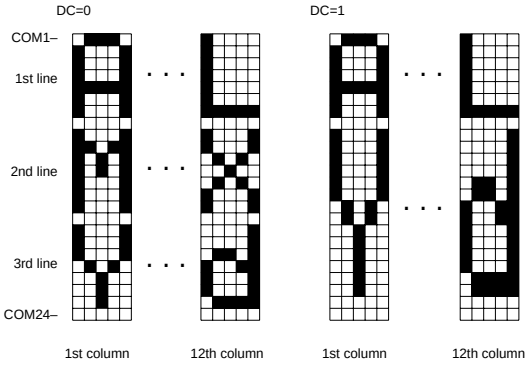
C	B	Cursor display
0	0	Not displayed
0	1	Not displayed
1	0	Underbar cursor
1	1	Alternate character display normally and reversely



The cursor display position is indicated by the address counter. Accordingly, to move the cursor, change the address counter value by automatic increment by writing the RAM address set command or RAM data.

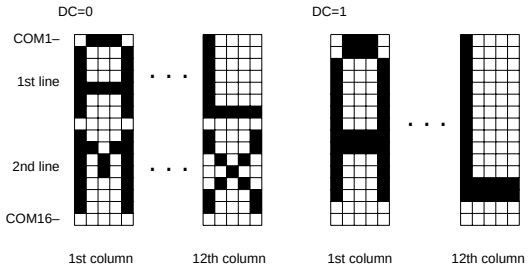
The following shows the relationship between the DC resistor and display:

(1) N=0 (1/26 duty)



The character on the 3rd line will be displayed in double size on the second and third lines by setting DC=1.

(2) N=1 (1/18 duty)



The character on the 1st line will be displayed in double size on the first and second lines by setting DC=1.

(3) Power Save

The Power Save command controls the oscillator and sets or releases the Sleep mode.

A0 XWR D7 — D0

0	0	0	1	0	0	✻	✻	O	PS

✻ : Don't Care

PS=0: Turns the Power Save on. (Release)
PS=1: Turns the Power Save off. (Select)
O=0: Turn the oscillator off. (Stop oscillation)
O=1: Turns the oscillator on. (Oscillation)

(4) Power Control

The Power Control command controls the built-in power circuit operations.

A0 XWR D7 — D0

0	0	0	1	0	1	0	0	0	P

✻ : Don't Care

P=0: Turns the power circuit off.
P=1: Turns the power circuit on.
Note: The oscillator must be operating to operate the voltage amp.

(5) System Reset

The System Reset command sets the display direction, the display line, and the use or no use of CGRAM. This command must first be executed after the power-on or reset.

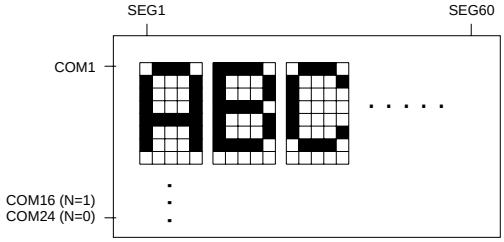
A0 XWR D7 — D0

0	0	0	1	1	0	N	S2	S1	CG

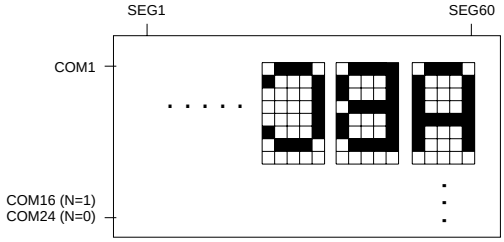
✻ : Don't Care

N=0: Displays 3 lines. (1/26 duty)
N=1: Displays 2 lines. (1/18 duty)
S2=0: Normal display
S2=1: Right and left reverse display
S1=0: Normal display
S1=1: Top and bottom reverse display
CG=0: Does not use the CGRAM.
CG=1: Uses the CGRAM.

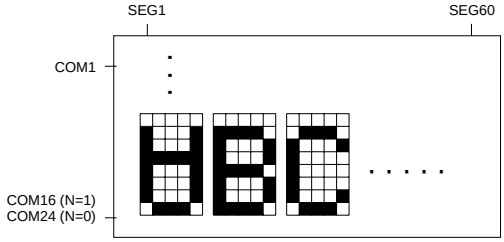
(1) Normal display



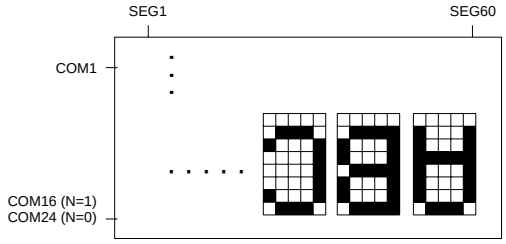
(2) Horizontal flipping



(3) Vertical flipping



(4) Horizontal vertical flipping



(6) RAM Address Setup

The RAM Address Setup command sets an address into the Address counter to write data into DDRAM, CGRAM and Symbol register.
When the cursor display is ON, the cursor is located at a position corresponding to the DDRAM address set by this command.

A0	XWR	D7					D0
0	0	1	ADDRESS				

✻ : Don't Care

① The 00H to 7FH address length can be set. To write data in the RAM, set the data write address by this command. When the subsequent data is written continuously, the address is automatically incremented.

RAM map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM (00H)								CGRAM (01H)							
10H	CGRAM (02H)								CGRAM (03H)							
20H	SI1				SI2			Unused	EV		TEST		LED	Unused		
30H	DDRAM line 1								For signals							Unused
40H	DDRAM line 2															Unused
50H	DDRAM line 3															Unused
60H	Symbol register															Unused
70H	Symbol register															Unused

SI : Static Icon register
EV : Electronic Control register
TEST : Test register
(Do not use in normal operations.)

LED : LED register
For signals : SEGS1, 2, 4, 5
Symbol register : COMS1, COMS2

(7) Data Write

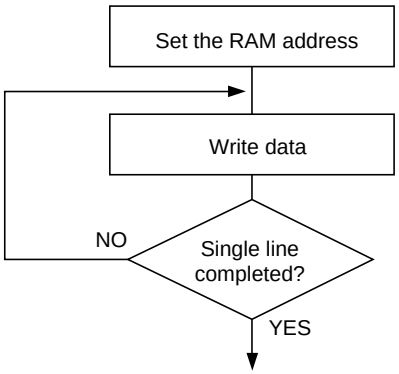
A0	XWR	D7					D0
1	0	DATA					

✻ : Don't Care

① This command writes data in the DDRAM, CGRAM or Symbol register.
② When this command is executed, the Address counter is incremented by 1 automatically. This allows continuous data writing.

Data write example:

The following gives an example to write a single line of data continuously.



Note: Assign an enough time greater than "tcyc" before executing the next instruction.

Table 4 SED1225 command list

Command	Code										Function
	A0	XWR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Shifts the cursor to its home position.
(2) Display On/Off Control	0	0	0	0	1	1	C	B	DC	D	Turns on or off the cursor, cursor blinking, double-size display, and data display. C=1: Cursor ON; C=0: Cursor OFF B=1: Blinking ON; B=0: Blinking OFF DC=1: Double-size display; DC=0: Normal display D=1: Display ON; D=0: Display OFF
(3) Power Save	0	0	0	1	0	0	*	*	0	PS	Turns on or off the Power Save mode and oscillator. PS=1: Power Save ON; PS=0: Power Save OFF O=1: OSC ON; O=0: OSC OFF
(4) Power Control	0	0	0	1	0	1	0	0	0	P	Turns on or off the built-in power circuit and voltage follower capacity, and sets the amp frequency. P=1: Power circuit ON; P=0: Power circuit OFF
(5) System Reset	0	0	0	1	1	0	N	S2	S1	CG	Sets the use or no use of CGRAM and the display direction. N=1: 3-line display; N=0: 2-line display CG=1: Use of CGRAM; CG=0: No use of CGRAM S2=0, S1=0: Normal display S2=0, S1=1: Top and bottom reverse display S2=1, S1=0: Right and left reverse display S2=1, S1=1: 180-degree rotation display
(6) RAM Address Setup	0	0	1	ADDRESS							Sets an address of DDRAM, CGRAM or Symbol register.
(7) RAM Write	1	0	DATA								Writes data in the DDRAM, CGRAM or Symbol register.
(8) NOP	0	0	0	0	0	0	0	0	0	0	This is a non-operation command.
(9) Test Mode	0	0	0	0	0	0	*	*	*	*	This is an IC chip test command. Do not use in normal operations.

BUILT-IN MEMORIES

Character Generator ROM (CGROM)

The SED1225 contains up to 126 types of CGROMs. Each character has a 5×8-dot structure.
Tables 5 to 8 defines the SED1225D** character codes. Four characters (00H to 03H) of character codes are used for the CGROM or CGRAM by the System Setup command.

The SED1225's CGROM is a mask ROM and it can be used as a custom CGROM. Consult to our sales agency for details.
The CGROM versions are identified as follows:
Example: SED1225D$_{0B}^{\uparrow}$
CGROM pattern ID

Table 5 SED1225DAB

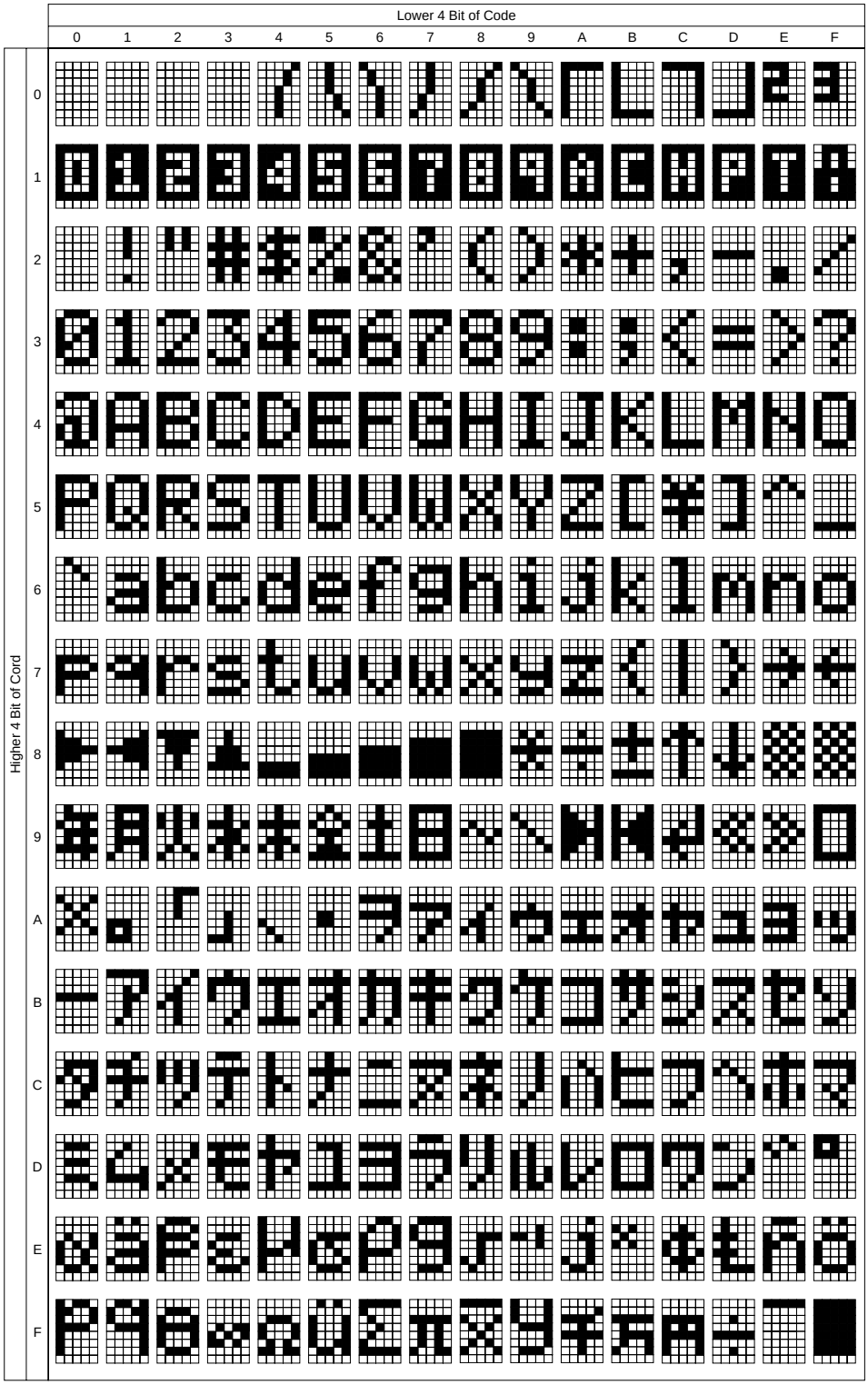
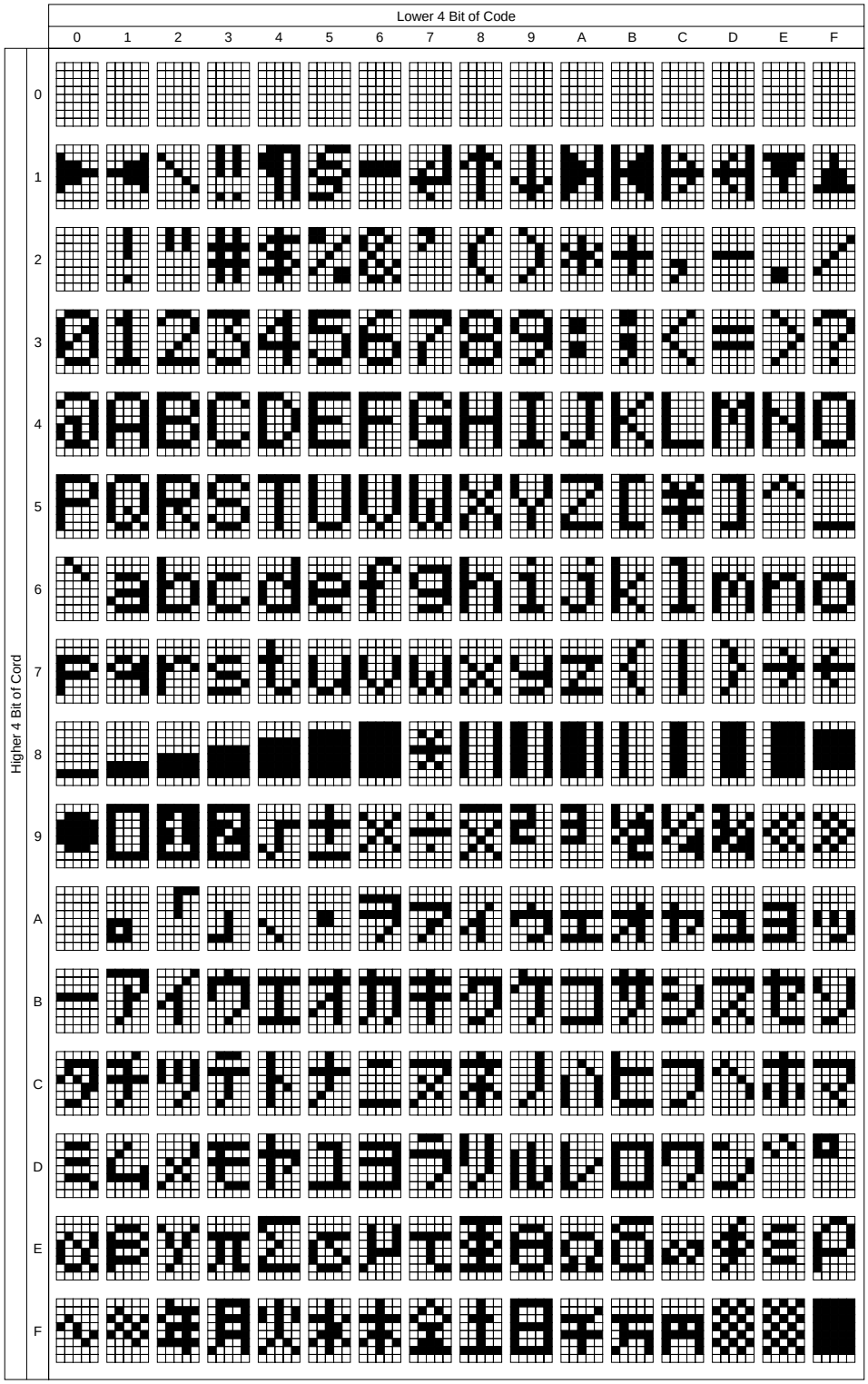


Table 6 SED1225DBB

Table 7 SED1225DGB



Character Generator RAM (CGRAM)

The SED1225 has a built-in CGRAM to program user-defined character patterns for highly flexible signal and character display.
Issue the System Setup command to use the CGRAM.
The CGRAM has the 160-bit storage capacity, and it can store up to four 5×8-dot character patterns.
The following provides the relationship between CGRAM character patterns and CGRAM addresses and character codes.

Character Code	RAM Address		CGRAM Data D7							D0	Character Display SEG	Signal Display SEGS 1 2	4 5
00H	00H to 07H	0	*	*	*	0	1	1	1	1	□■■■■	□■	■■
		1	*	*	*	1	0	0	0	0	■□□□□	■□	□□
		2	*	*	*	1	0	0	0	0	■□□□□	■□	□□
		3	*	*	*	0	1	1	1	1	□■■■■	□■	■■
		4	*	*	*	0	0	0	0	1	□□□□■	□□	□■
		5	*	*	*	0	0	0	0	1	□□□□■	□□	□■
		6	*	*	*	1	1	1	1	0	■■■■□	■■	■□
		7	*	*	*	0	0	0	0	0	□□□□□	□□	□□
01H	08H to 0FH	8	*	*	*	0	0	1	0	0	□□■□□	□□	□□
		9	*	*	*	0	0	1	0	0	□□■□□	□□	□□
		A	*	*	*	0	1	1	1	0	□■■■□	□■	■□
		B	*	*	*	0	1	1	1	0	□■■■□	□■	■□
		C	*	*	*	0	1	1	1	0	□■■■□	□■	■□
		D	*	*	*	1	1	1	1	1	■■■■■	■■	■■
		E	*	*	*	1	1	1	1	1	■■■■■	■■	■■
		F	*	*	*	0	0	0	0	0	□□□□□	□□	□□

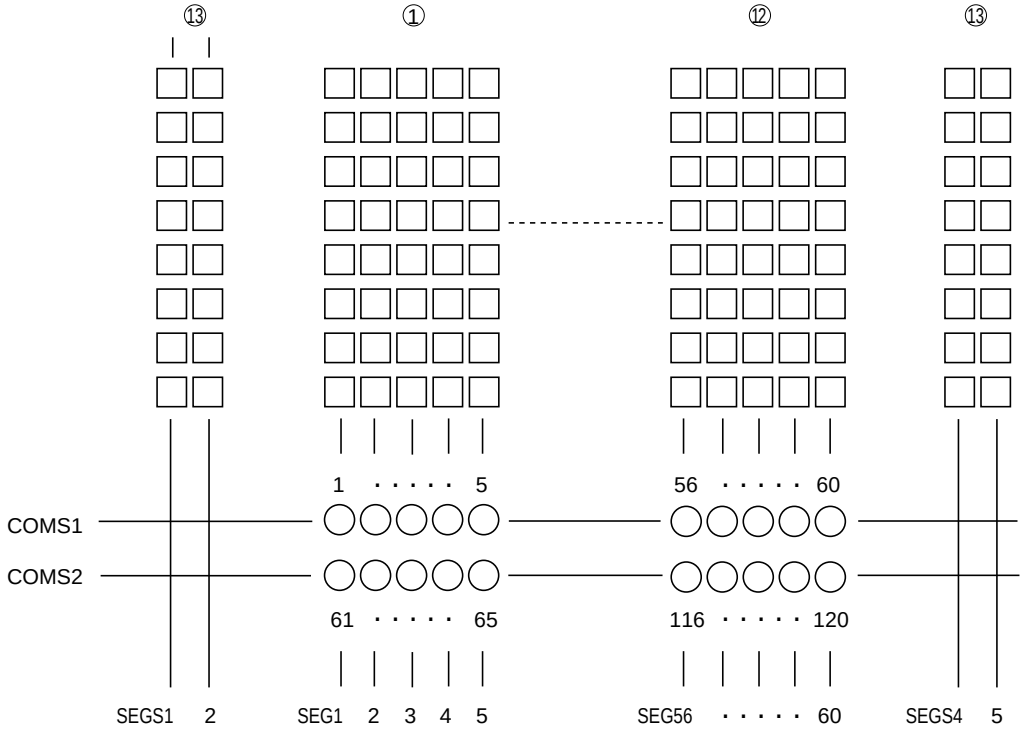
D7 to D5: Un used
D4 to D0: Character data (1 for display; 0 for no display)

The 5×8-dot character size can also be set. To do so, use the *7H and *FH RAM addresses. However, the *7H and *FH data is reversed if the underbar cursor is used.

Symbol Register

The SED1225 has a built-in Symbol register to allow separate symbol setup on the display panel.
The Symbol register has the 120-bit storage capacity, and it can display 120 symbols. Also, the SED1225 contains a Blink register for every 5-dot blinking.

The following provides the relationship between the Symbol register display patterns, RAM addresses and write data.



RAM Address		Corresponding symbol bits							
		D7	D6	D5	D4	D3	D2	D1	D0
60H to 6BH	0	*	*	BL1	1	2	3	4	5
	1	*	*	BL2	6	7	8	9	10
	:	:							
	B	*	*	BL12	56	57	58	59	60
70H to 7BH	0	*	*	BL13	61	62	63	64	65
	1	*	*	BL14	66	67	68	69	70
	:	:							
	B	*	*	BL24	116	117	118	119	120

BL1 to BL24: Blinking setup (0 for no blinking; 1 for blinking)

Note: If the symbol size is 1.5 times greater than other dots, we recommend to divide and drive the SEG* and COMS1 and COMS2 separately.

Static Icon RAM

The SED1225 has a built-in Static Icon RAM to display a static icon separately from the dynamic icon.
The Static Icon RAM has the 20-bit storage capacity, and it can display 10 icons. The following provides the relationship between the static icon functions and the static icon, RAM address and write data.

(SEGSA, B, C, D, E)

Function	RAM Address	Static Icon Data D7							D0	Display SEGSA B C D E
Display ON/OFF	20H	*	*	*	0	0	1	1	1	□□■■■
Blink ON/OFF	21H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

(SEGSF, G, H, I, J)

Function	RAM Address	Static Icon Data D7							D0	Display SEGSA B C D E
Display ON/OFF	22H	*	*	*	0	0	1	1	1	□□■■■
Blink ON/OFF	23H	*	*	*	1	0	0	0	1	□□■■■ ⇕ f BLINK ■□■■□

* : Unused
1 : Display or blinking
0 : No display or no blinking
f_{BLINK} : 1 to 2Hz

Electronic Control RAM (Register)

The SED1225 has the electronic control functions to control LCD drive voltages and to adjust the LCD display density. One of 32-state LCD voltages can be selected when the 5-bit data is written in the Electronic Control RAM.

The following provides the relationship between the RAM address and write data by electronic control setup.

Function	RAM Address	Electronic Control Data D7							D0	Status	VEV
Electronic Control	28H	*	*	*	0	0	0	0	0	0	VREG-0
		*	*	*	0	0	0	0	1	1	VREG-α
		*	*	*	0	0	0	1	0	2	VREG-2α
		. . . . .								. . . . .	. . . . .
		*	*	*	1	1	1	0	1	29	VREG-29α
		*	*	*	1	1	1	1	0	30	VREG-30α
		*	*	*	1	1	1	1	1	31	VREG-31α
	29H	*	*	*	*	*					For test

* : Unused

α : α=VREG/95 (1/4biased)

Note: Do not use address 29H as it can be used for IC chip test only.

LED RAM (Register)

The SED1225 has the LED drive functions to drive the LCD by controlling the XLE1 and XLE2 pins.

The following provides the relationship between the RAM address and write data by LED register setup.

Function	RAM Address	LED Register Data D7				D3	D2	D1	D0
LED ON/OFF Timer	2AH	✻	✻	✻	✻	TIM2	TIM1	LED2	LED1

✻ : Unused

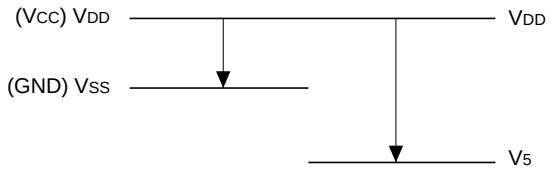
The following defines the XLE1 and XLE2 pin state depending on the TIM1, TIM2, LED1 and LED2 set values.

LED Register Set Value		Output Status (XLE1, XLE2)
TIM2 TIM1	LED2 LED1	
0	0	XLE = High impedance
0	1	XLE = Low
1	0	Keeps XLE low approximately 15 sec after input of Display ON command.
1	1	XLE = Low

Note: When this function is used, minimize power supply and power cable impedance to avoid IC misoperation due to large current.

MAXIMUM ABSOLUTE RATINGS

Item		Symbol	Rating	Unit
Power voltage (1)		V_{SS}	–0.6 to +0.3	V
Power voltage (2)		V_5	–7.0 to +0.3	V
Power voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		Topr	–30 to +85	°C
Storage temperature	TCP	Tstr	–55 to +100	°C
	Bare chip		–65 to +125	



Notes: 1. All voltages are referenced to V_{DD}=0 V.
2. The following voltage levels must always be satisfied:
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4$, and $V_{DD} \geq V_{SS} \geq V_5$
3. If the LSI is used beyond the maximum absolute rating, the LSI may be destroyed permanently. The LSI should meet the electric characteristics during normal operations. If not, the LSI may be malfunction or the LSI reliability may be lost.

DC CHARACTERISTICS

(V_{SS} = –3.6 to –1.7 V, Ta = –30 to +85°C unless otherwise noted.)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Pin
Power voltage (1)	Operable	V_{SS}	1/4 bias	–3.6	–3.0	–1.7	V	V_{SS}
			1/5 bias	–3.6	–3.0	–2.7		
	Data hold voltage			–3.6		–1.5		
Power voltage (2)	Operable	V_5		–6.0		–3.0	V	V_5
	Operable	V_1, V_2		0.5 × V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4		V_5		0.5 × V_5	V	V_3, V_4
"Hi" input voltage		V_{IHC}		0.2 × V_{SS}		V_{DD}	V	*2
"Lo" input voltage		V_{ILC}		V_{SS}		0.8 × V_{DD}	V	*2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0		1.0	µA	*2
LCD driver ON resistance		R_{ON} (LCD)	Ta=25°C, ΔV=0.1V, V_5=–5.0V		10	20	kΩ	COM, SEG *3
LED driver ON resistance		R_{ON} (LED)	V_{SS}=–3.0V, I_{OL}=10mA		100		Ω	XLE1, XLE2
Static current consumption		I_{DDQ}			0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	During display	V_5 = –5V; No loading V_{SS}=–1.8V		20	30	µA	V_{DD} *4
		During display	V_5 = –5V; No loading V_{SS}=–3.0V		30	45	µA	V_{DD} *4
		During standby	OSC On; PWR off No loading; V_{SS}=–3.0V		10	15	µA	V_{DD}
		During sleep	OSC Off; PWR off No loading; V_{SS}=–3.0V		0.1	5	µA	V_{DD}
		During access	fcyc=200KHz V_{SS}=–3.0V		150	300	µA	V_{DD} *5
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		8.0	10.0	pF	*3

Frame frequency	f_{FR}	Ta = 25°C, V_{SS} = –3.0V	70	100	130	Hz	*8
External clock frequency	f_{CK}			33.8		kHz	*8, *9

Reset time	t_R		1.0			µs	*6
Reset pulse width	t_{RW}		10			µs	*6
Reset start time	t_{RES}		50			ns	*7

Dynamic system:

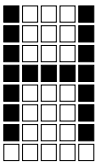
Built-in power supply	Amp output voltage	V_5	Ta = 25°C (during 1/4 bias)	4 × V_{REG2}			V	
	Reference voltage	V_{REG2}	Ta = 25°C (during 1/4 bias)	–1.55	–1.5	–1.45	V	

*1 Although the wide operating character range is guaranteed, a quick and excessive voltage variation may not be guaranteed during access by the MPU. The low-voltage data hold characteristics are valid during Sleep mode. No access by the MPU is allowed during this time.

*2 D0 to D5, D6 (SCL), D7 (SI), A0, RES, XCS, XWR (E), PS, IF, C86

*3 The resistance if a 0.1-volt voltage is supplied between the SEGn, SEGSn, COMn or COMSn output pin and each power pin (V_1, V_2, V_3 or V_4). It is defined within power voltage (2).
$R_{ON} = 0.1V/\Delta I$
where, ΔI is current that flows when the 0.1-volt voltage is supplied between the power supply and output.

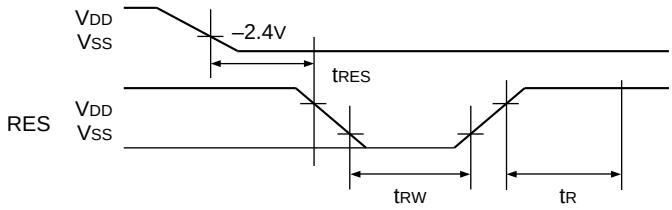
*4 Applied if not accessed by the MPU during character display and if the built-in power circuit and oscillator are operating.
Display character:



*5 Current consumption if always written in "fcyc". The current consumption during access is roughly proportional to the access frequency (fcyc).

*6 The "t_R" (reset time) indicates a time period from the rising edge of RES signal to the completion of internal circuit reset. Therefore, the SED1225 enters the normal operation status after "t_R".

*7 Defines the minimum pulse width of RES signal. A pulse width greater than "t_{RW}" must be entered for reset.



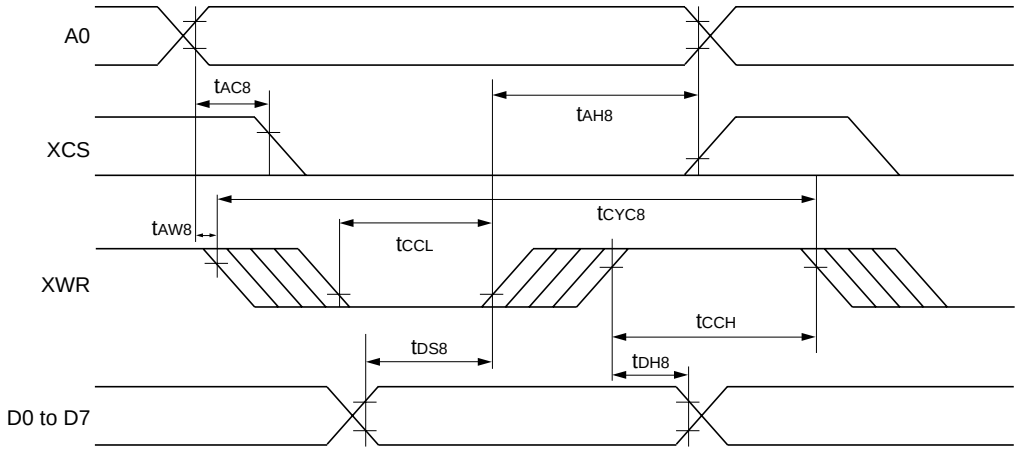
All signal timings are based on 20% and 80% of Vss.

*8 The following provides the relationship between the oscillator frequency (f_{OSC}) for built-in circuit driving and the frame frequency (f_{FR}).
$f_{OSC} = 13 \times 26 \times f_{FR}$ (3-line display)
$= 13 \times 18 \times f_{FR}$ (2-line display)
<Reference>
$f_{BLK} = (1/128) \times f_{FR}$

*9 Enter the waveforms in 40% to 60% duty to use an external clock instead of the built-in oscillator. If no external clock is entered, fix it to high. (Normal high)

SIGNAL TIMING CHARACTERISTICS

(1) MPU bus write timing (80 series)



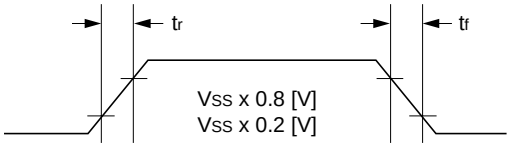
(Ta = –30 to +85°C, V_{SS} = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time XCS setup time	A0 XCS	t_{AW8} t_{AH8} t_{AC8}	All timing must be based on 20% and 80% of V_{SS}.	60 30 0	— — —	ns
System cycle time	XWR	t_{CYC8}		1850	—	ns
Write "Lo" pulse width (XWR)		t_{CCL}		150	—	ns
Write "Hi" pulse width (XWR)		t_{CCH}		1650	—	ns
Data setup time Data hold time	D0 to D7	t_{DS8} t_{DH8}		50 50	— —	ns

(Ta = –30 to +85°C, V_{SS} = –3.3V to –2.7V)

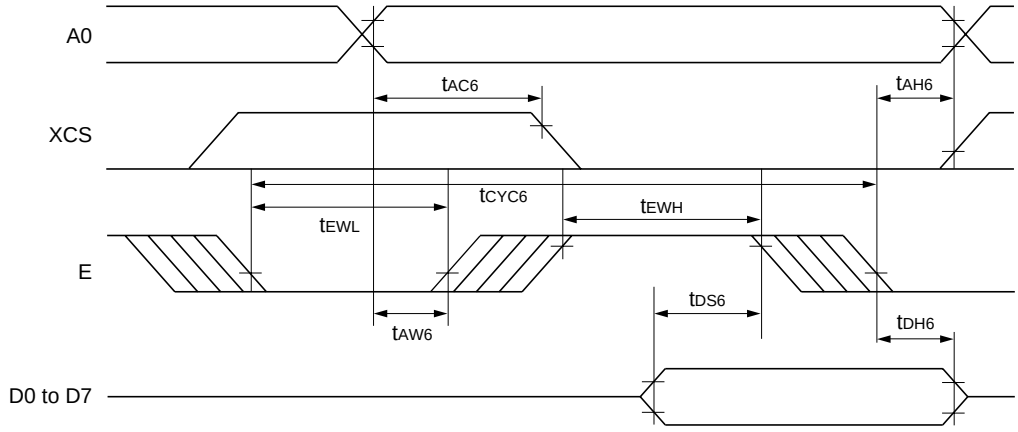
Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time Address hold time XCS setup time	A0 XCS	t_{AW8} t_{AH8} t_{AC8}	All timing must be based on 20% and 80% of V_{SS}.	60 30 0	— — —	ns
System cycle time	XWR	t_{CYC8}		1150	—	ns
Write "Lo" pulse width (XWR)		t_{CCL}		100	—	ns
Write "Hi" pulse width (XWR)		t_{CCH}		1000	—	ns
Data setup time Data hold time	D0 to D7	t_{DS8} t_{DH8}		20 20	— —	ns

*1 The input signal rise and fall times (tr, tf) are defined to be 25 nsec max (except for RES input).



*2 "t_{CCL}" is defined by the overlap time of XCS low level and XWR low level.

(2) MPU bus write timing (68 series)



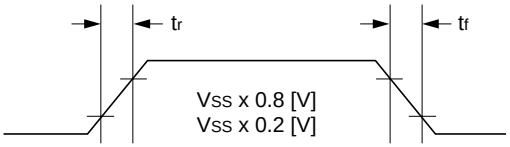
(Ta = –30 to +85°C, V_{SS} = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time	A0	t_{AW6}	All timing must be based on 20% and 80% of V_{SS}.	60	–	ns
Address hold time	XCS	t_{AH6}		50	–	
XCS setup time		t_{AC6}		0	–	
System cycle time	XWR	t_{CYC6}		1850	–	ns
Enable "Lo" pulse width (XWR)		t_{EWL}		1650	–	ns
Enable "Hi" pulse width (XWR)		t_{EWH}		150	–	ns
Data setup time	D0 to D7	t_{DS6}		20	–	ns
Data hold time		t_{DH6}		80	–	

(Ta = –30 to +85°C, V_{SS} = –3.3V to –2.7V)

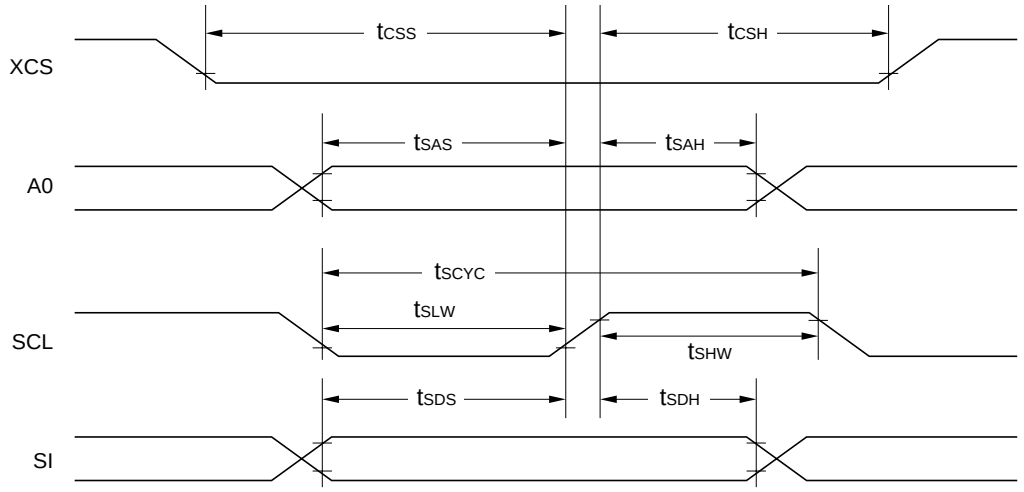
Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address setup time	A0	t_{AW6}	All timing must be based on 20% and 80% of V_{SS}.	60	–	ns
Address hold time	XCS	t_{AH6}		30	–	
XCS setup time		t_{AC6}		0	–	
System cycle time	XWR	t_{CYC6}		1150	–	ns
Enable "Lo" pulse width (XWR)		t_{EWL}		1000	–	ns
Enable "Hi" pulse width (XWR)		t_{EWH}		100	–	ns
Data setup time	D0 to D7	t_{DS6}		20	–	ns
Data hold time		t_{DH6}		50	–	

*1 The input signal rise and fall times (tr, tf) are defined to be 25 nsec max (except for RES input).



*2 "t_{EWH}" is defined by the overlap time of XCS low level and XWR low level.

(3) Serial interface



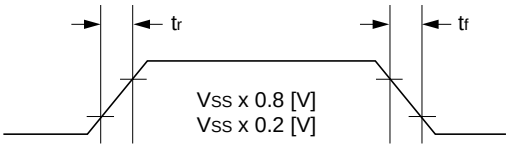
(Ta = –30 to +85°C, Vss = –3.6V to –1.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
System clock cycle SCL "Hi" pulse width SCL "Lo" pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}	All timing must be based on 20% and 80% of Vss.	3000 2850 150	— — —	ns
Address setup time Address hold time	A0	t_{SAS} t_{SAH}		50 800	— —	ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		50 50	— —	ns
CS-to-SCL time	XCS	t_{CSS} t_{CSH}		400 2500	— —	ns

(Ta = –30 to +85°C, Vss = –3.3V to –2.7V)

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
System clock cycle SCL "Hi" pulse width SCL "Lo" pulse width	SCL	t_{SCYC} t_{SHW} t_{SLW}	All timing must be based on 20% and 80% of Vss.	1400 1300 50	— — —	ns
Address setup time Address hold time	A0	t_{SAS} t_{SDH}		50 500	— —	ns
Data setup time Data hold time	SI	t_{SDS} t_{SDH}		30 30	— —	ns
CS-to-SCL time	XCS	t_{CSS} t_{CSH}		200 1500	— —	ns

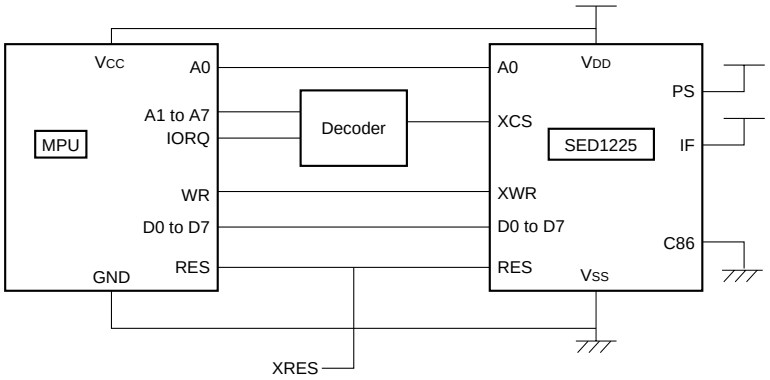
*1 The input signal rise and fall times (tr, tf) are defined to be 25 nsec max (except for RES input).



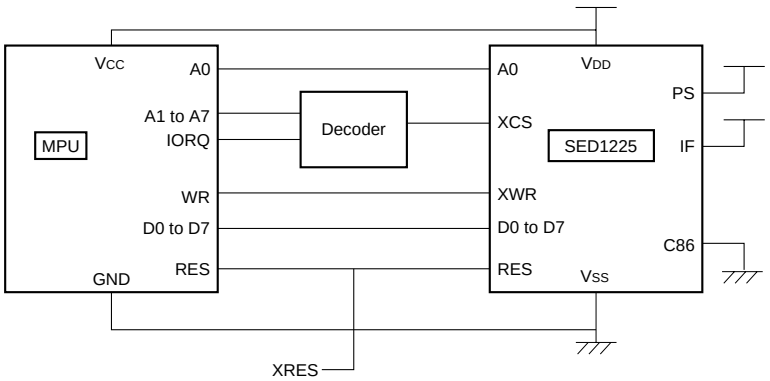
MPU INTERFACES (REFERENCE)

The SED1225 can be connected to the 80-series or 68-series MPU. Also, it can operate with a less number of signal lines via the serial interface.
If the MPU buses and ports are set to high impedance for a certain time due to RESET, the RESET signal must be entered in the SED1225 after the SED1225's inputs have been determined.

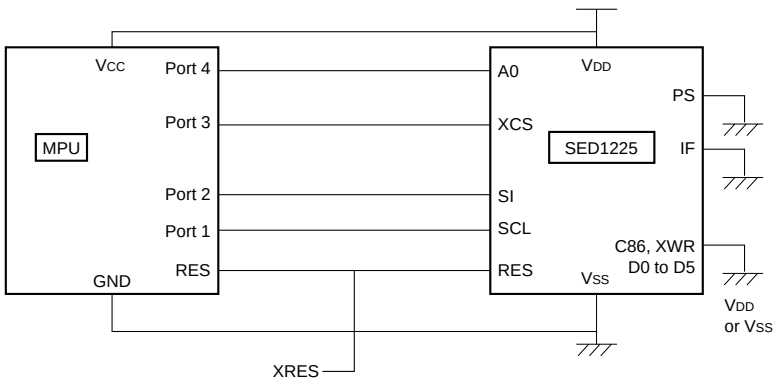
80-Series MPU



68-Series MPU

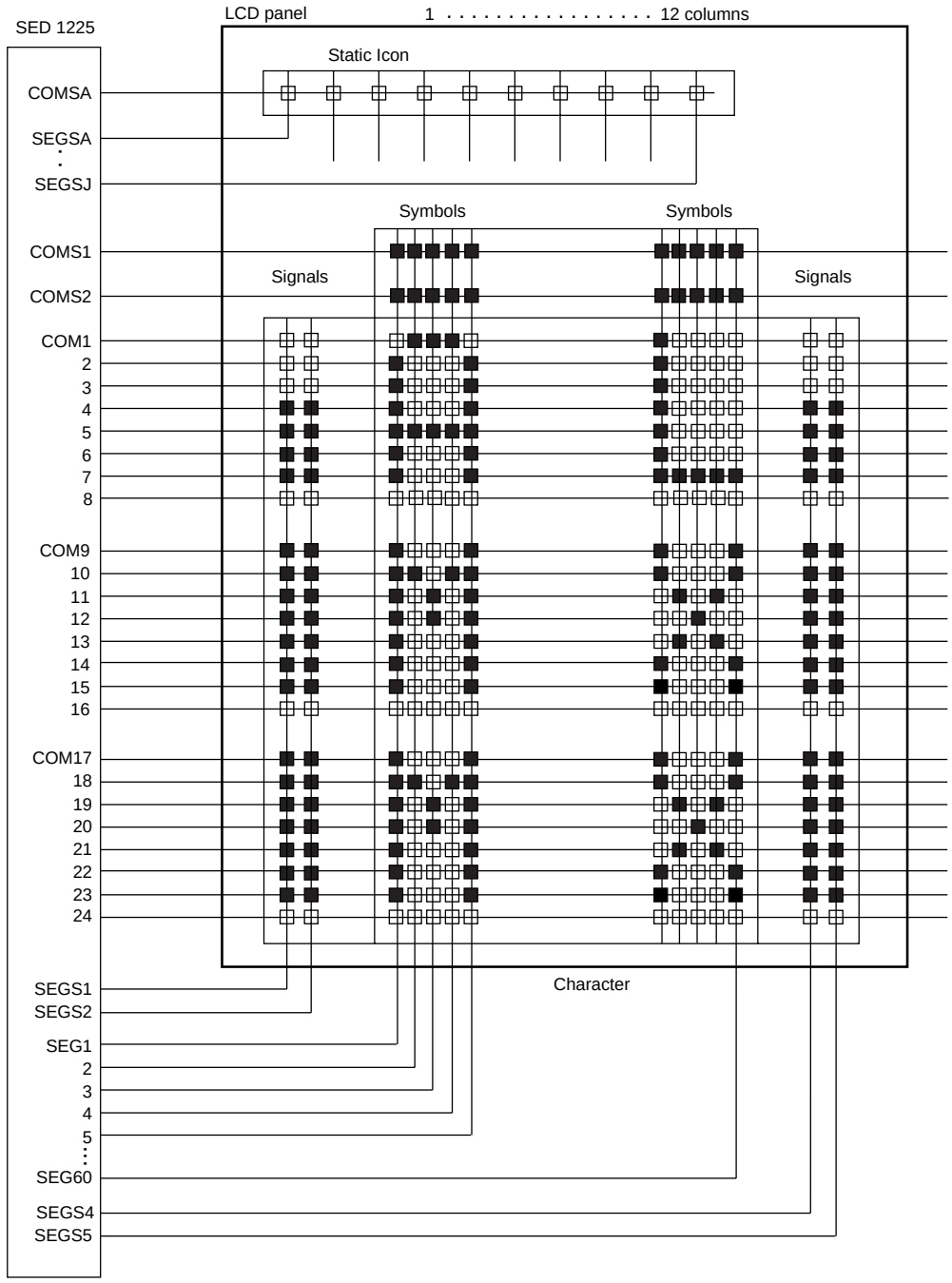


Serial Interface

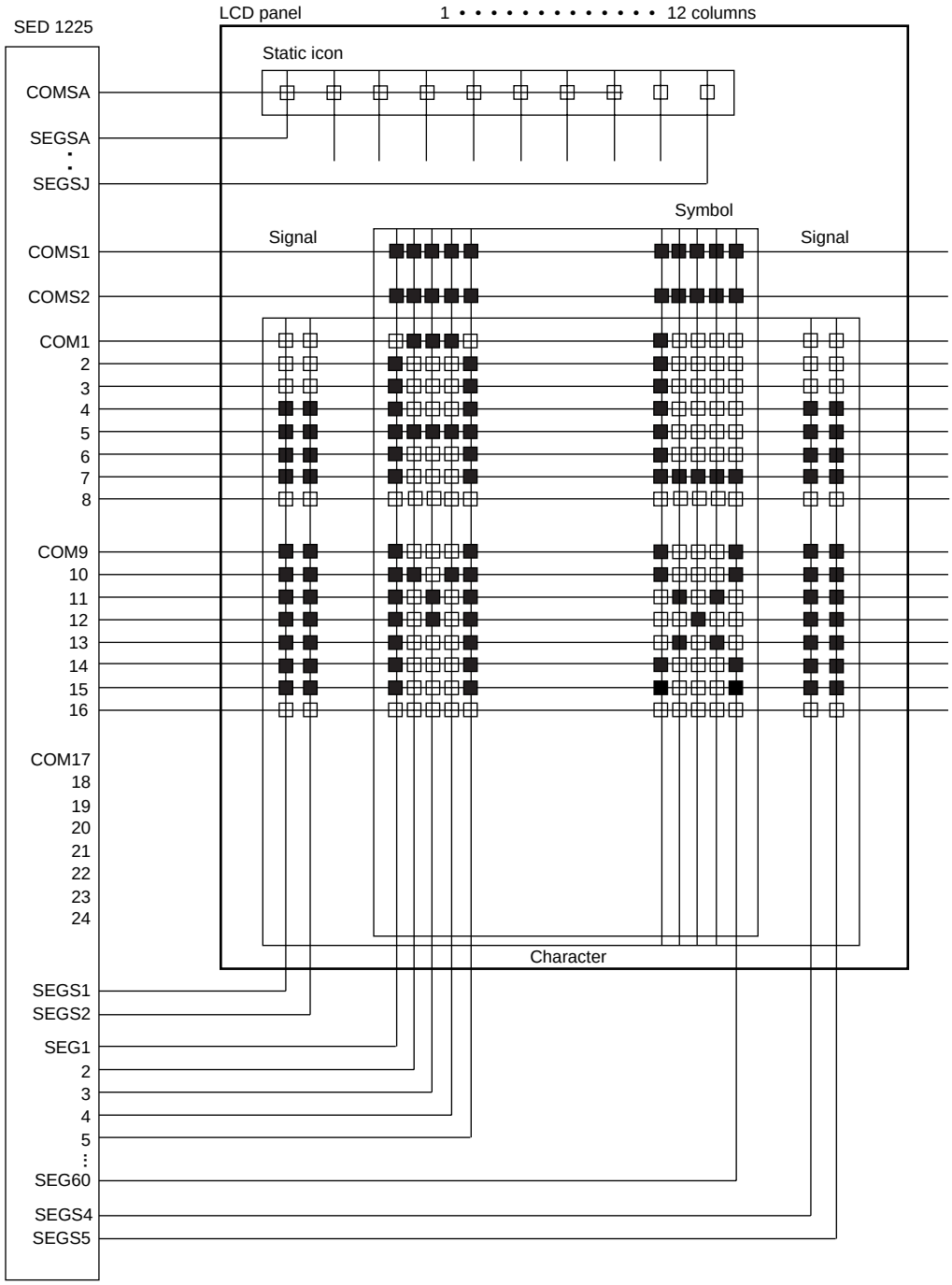


LCD CELL INTERFACE

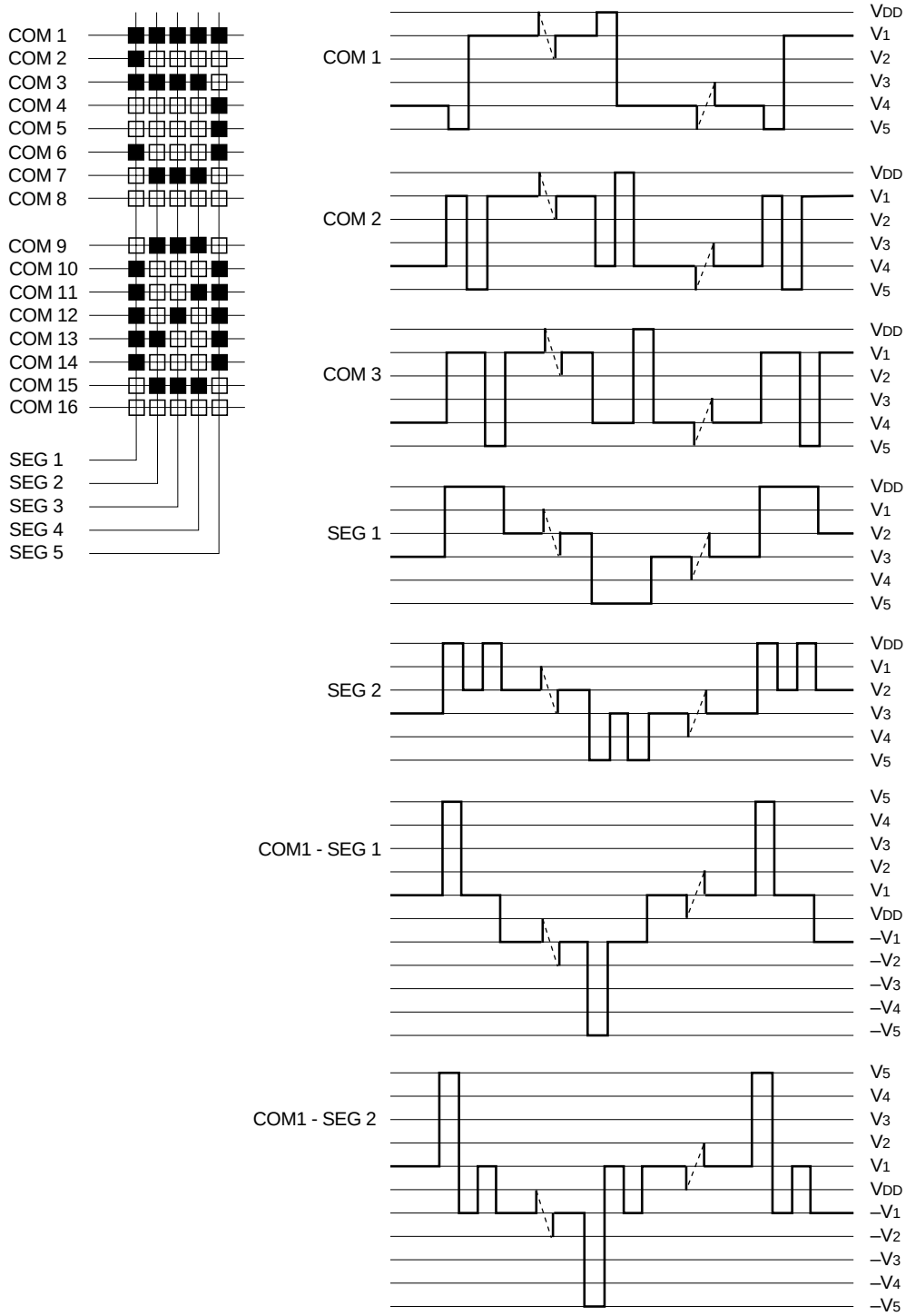
12 columns by 3 lines, 5×8 dots + Symbols



12 columns by 2 lines (N=1), 5×8 dots + Symbols

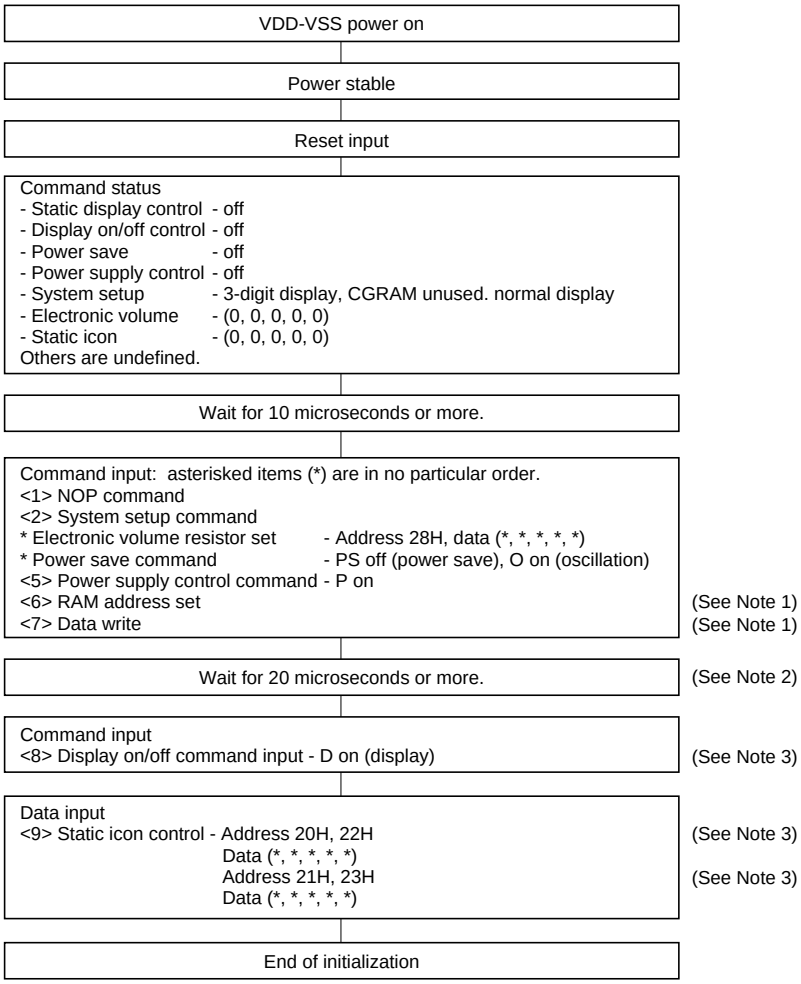


LCD DRIVE WAVEFORMS (B WAVEFORMS)

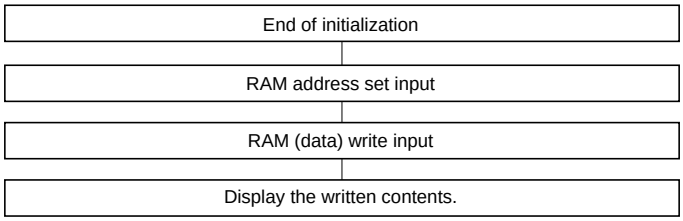


EXAMPLE OF INSTRUCTION SETUP (REFERENCE)

Initialization

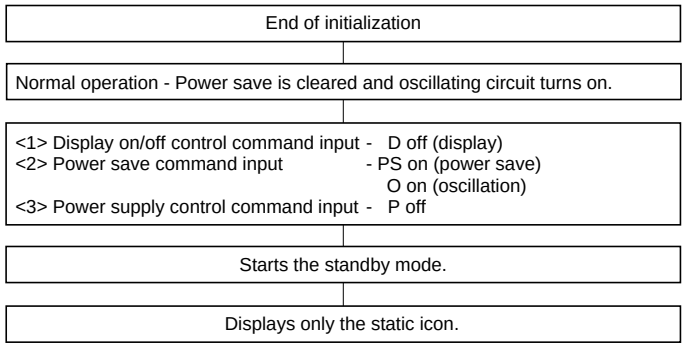


Display Mode

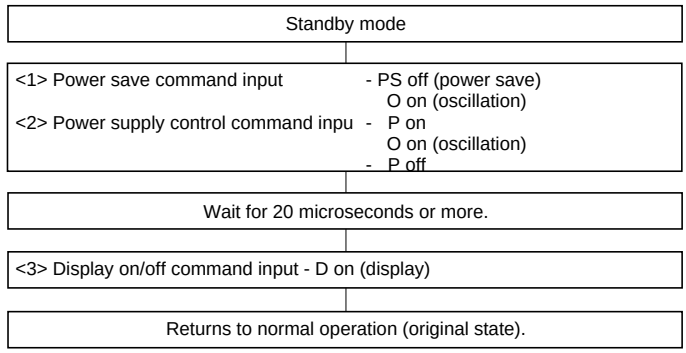


Standby Mode

(1) Setting the standby mode

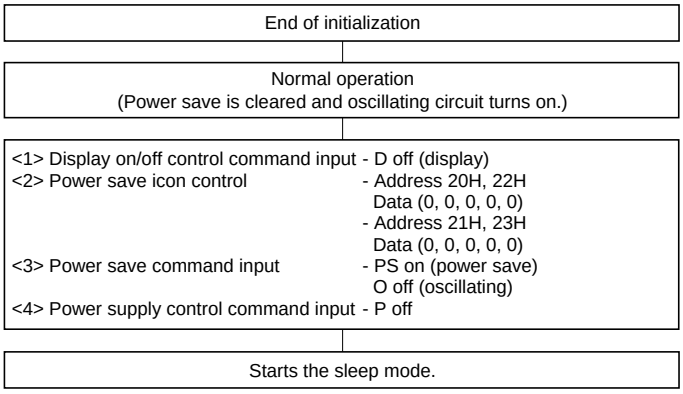


(2) Clearing the standby mode



Sleep Mode

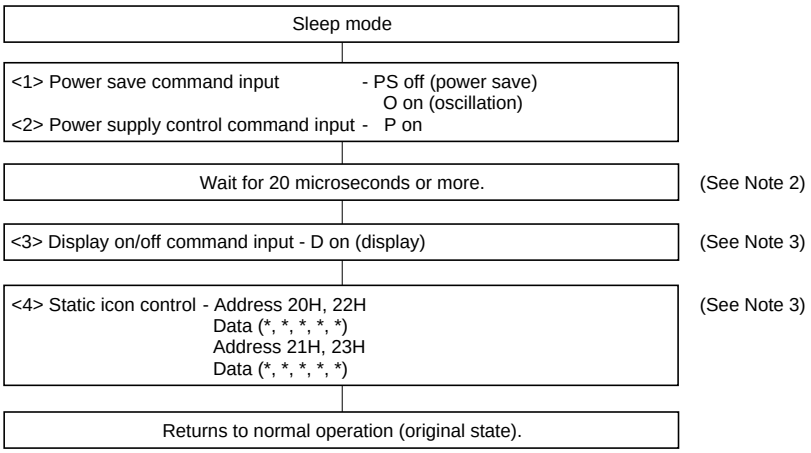
(1) Setting the Sleep mode.



(See Note 3)

(See Note 3)

(2) Clearing the sleep mode



(See Note 2)

(See Note 3)

(See Note 3)

Note 1. <6> and <7> of 15-1 indicate RAM initialization. Set the contents to be displayed in the beginning. For items not to be displayed (RAM Clear), use the following steps:
- DD RAM - write 20H (character code).
- CG RAM - write 00H (data '0').
- Symbol register - write 00H (data '0').

The RAM data is unspecified at the time of reset input (after power is turned on). If the data '0' is not written at this stage, unexpected display may occur to the unset position.

Note 2. Defined by the rising characteristics of the power circuit, time setting varies according to the external capacity. So be sure to make confirmation by external capacity, and set this time.

Note 3. The dynamic drive system display lamp is lit up by the display on/off command when it is on. The static icon lamp is lit by the static icon control command. So to light up the lamp simultaneously with start of display, execute the display on/off control command and static icon control within one frame.

OPTION LIST

The SED 1225 has the following options. Options are available exclusively for users. Please contact our Sales Department for information.

- The following shows how to define the name of the product compatible with options:

  Example: SED1225D*B
  ↑
  Option compatibility column

Specification of character generator ROM (CGROM)

The SED1225 incorporates a characters generator ROM consisting of up to 256 types of characters, with each character size featuring 5 × 7 (8) dots. The SED1225 CGROM is designed as a masked ROM, and is compatible with the CGROM for exclusive use of the user. For the standard CGROM, see the Character Font Table.

Specifications of external clock

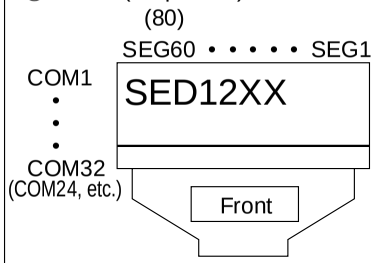
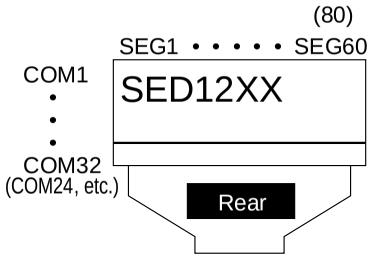
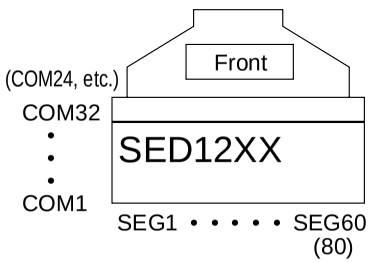
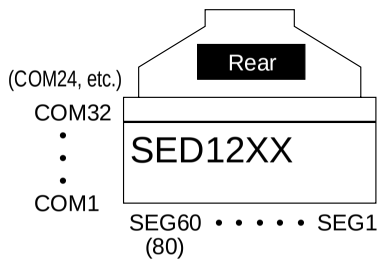
The SED1225 has an external clock terminal which is provided with two types of functions; f_{OSC} and $4 \times f_{OSC}$. Either f_{OSC} or $4 \times f_{OSC}$ can be selected according to the user's requirements.

	Built-in oscillation f_{OSC}	External clock f_{OSC}	External clock $4 \times f_{OSC}$
Standard	○	○	×
Optional	○	×	○

The standard external clock specifications are set on the f_{OSC}.

SED1220/1225/1240 Example of System Setup Depending on Mount Direction

Reference

	① Case1 (Chip Front)	② Case2 (Chip Rear)	③ Case3 (Chip Front)	④ Case4 (Chip Rear)
				
SED1220	• Unable to correspond with commands. • Only able to correspond with custom fonts.	○ System set • S = 0	○ System set • S = 1	• Unable to correspond with commands. • Only able to correspond with custom fonts.
SED1225	○ System set • S1 = 0 • S2 = 1 (Horizontally-reversed)	○ System set • S1 = 0 • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 1 (Horizontally-reversed)
SED1240	○ System set • CS = 0 • SS = 1 (SEG-reversed) However, the input of DDRAM address of "SED12XX" from the first digit of the first line shall be 3FH and 3EH, in this order (as it is reversed in the unit of character).	○ System set • CS = 0 • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 1 (SEG-reversed) However, the input of DDRAM address of "SED12XX" from the first digit of the first line shall be 3FH and 3EH, in this order.

CAUTIONS

The following points should be noted when this Development Specification is used:

1. This Development Specification is subject to modification for improvement without prior notice.
2. This Development Specification is not intended to guarantee enforcement of industrial property and other rights, or to grant license for the use of this product. Examples of applications mentioned in this Development Specification are given for effective understanding of the product. We are not responsible for any circuit problems which might occur due to use of these examples. The size of the values appearing in the characteristics table is represented by the size of the number line.
3. Part or whole of this Development Specification shall not be quoted, reproduced or used for other purposes without permission of our company.

For the use of the semi-conductor, take note of the following:

"Handling cautions for light"

According to the principle of the solar battery the semiconductor characteristics are changed when exposed to light. So misoperation may occur if this IC is exposed to light.

For the single IC unit, measures against light are not yet completely taken. The board and the product where this IC is mounted must be provided with the following measures:

(1) For designing and mounting, measures must be taken to provide the structure which ensures the light protecting properties of the IC during actual use.

(2) In the inspection process, environmental design must be made with consideration given to the light protecting properties of the IC.

(3) To ensure light protecting properties of the IC, consideration must be given to the surface, back and sides of the IC chip.