MF425-04

EPSON

SED1600 Series

LCD Drivers

Technical Manual

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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SED1600 Series
LCD Drivers

Technical Manual

SEIKO EPSON CORPORATION

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Segment drivers

Common drivers

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1. SELECTION GUIDE

SED1600 series

● Segment drivers

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Data bus	Package
SED1601D$_{AA}$	4.5 to 5.5	12 to 28	1/100 to 1/300	80	8-bit parallel	Al pad chip
SED1601F$_{AA}$						QFP5-100pin
SED1606D$_{0A}$	2.7 to 5.5	8 to 28			4-bit parallel	Al pad (for COB)
SED1606D$_{0B}$						Au bump chip
SED1606F$_{0A}$*						QFP5-100pin
SED1606D$_{1A}$						Al pad chip (DOFF type)
SED1606D$_{1B}$						Au bump chip (DOFF type)
SED1620D$_{0A}$	4.5 to 5.5	12 to 28	1/84 to 1/200	128		Al pad chip
SED1640D$_{0B}$	2.7 to 5.5	8 to 28	1/100 to 1/300	80		Au bump chip (slim chip)
SED1640T$_{0A}$*						Slim TCP*
SED1648D$_{0A}$						Al pad chip (zigzag positioning)

* : Under development

● Common drivers

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Package
SED1610F$_{AA}$	4.5 to 5.5	12 to 28	1/64 to 1/300	86	QFP5-100pin
SED1632D$_{0A}$					Al pad chip
SED1651D$_{0A}$	2.7 to 5.5	8 to 28		100	Al pad chip (zigzag positioning)
SED1670D$_{0A}$					Al pad chip (INH type)
SED1670D$_{1A}$					Al pad chip (DOFF type)
SED1670D$_{0B}$					Au bump chip (INH type)
SED1670D$_{1B}$					Au bump chip (DOFF type)
SED1670F$_{0A}$*					QFP5-128pin * Under study
SED1670F$_{1A}$*					QFP5-128pin * Under study
SED1672D$_{0A}$				68	Al pad chip (INH type)
SED1672D$_{1A}$					Al pad chip (DOFF type)
SED1672D$_{0B}$					Au bump chip (INH type)
SED1672D$_{1B}$					Au bump chip (DOFF type)
SED1672F$_{0A}$*					QFP5-100pin (INH type)
SED1672F$_{1A}$*					QFP5-100pin (DOFF type)

* : Under development

2. SED1601
Dot Matrix LCD Segment Driver

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OVERVIEW

The SED1601 is an 80 segment (column) dot-matrix LCD driver for use with very high capacity, high duty ratio displays It is intended to be used in conjunction with the SED1610F or SED1190F common (row) drivers.

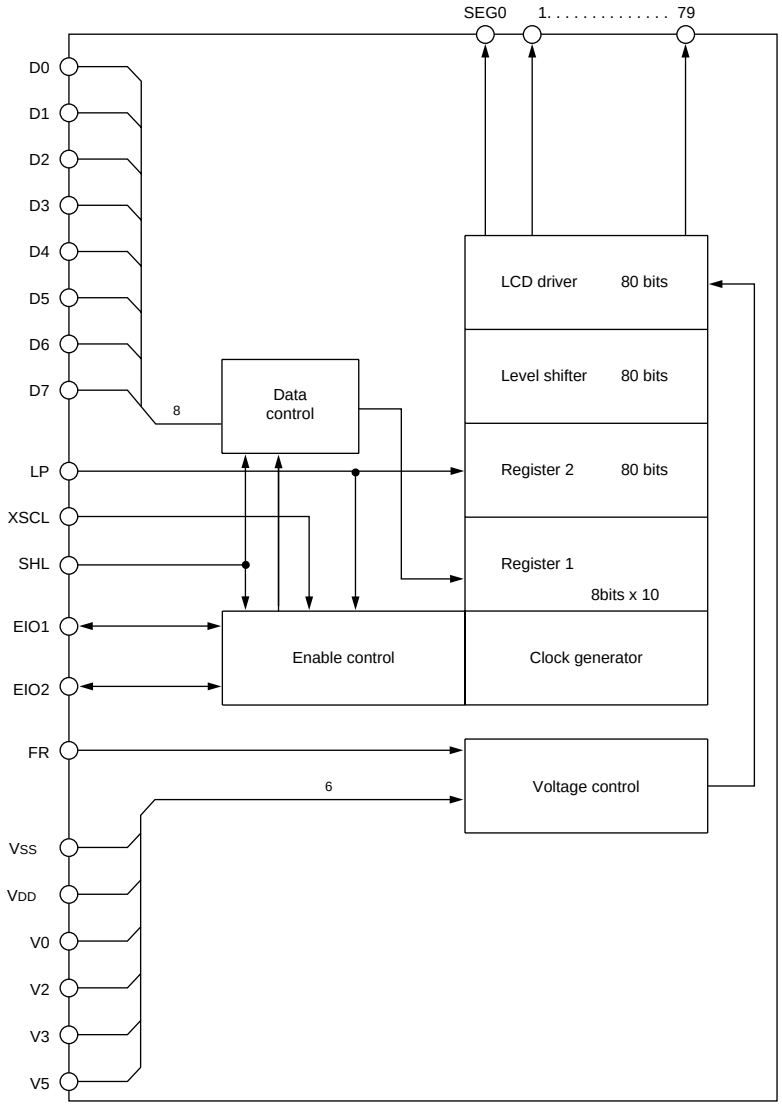
The SED1601 is designed to drive LCDs over a wide range of voltages. The bias voltages are isolated from V_{DD}, and are generated externally, giving a high degree of flexibility in circuit design and drive capability.

The SED1601 propagetes a daisy-chain enable signal automatically which simplifies the driver/ controller interface.

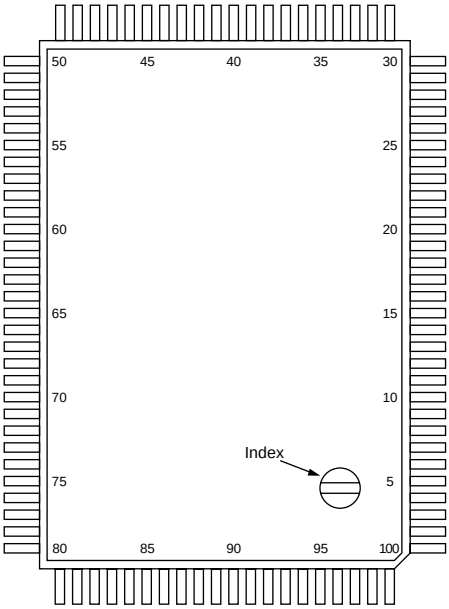
FEATURES

- 8-bit MPU bus
- 80 segment drivers
- Maximum Capacity Configuration: 640×200 pixels in combination with the SED1610F
- Wide range of LCD drive voltages: 12 to 28 V
- 4-bit bus and automatic daisy-chain enable support
- High frequency shift clock: 6 MHz maximum
- Selectable output shift direction
- Selectable drive bias
- Single 5V ±10% logic power supply
- Implemented in low power, Si-gate CMOS
- Packaging
  SED1601F$_{AA}$ (100-pin QFP, Plastic)
  SED1601D$_{AA}$ (Die form, Al pad)

BLOCK DIAGRAM



PACKAGE OUTLINE



PINOUT

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	SEG0	26	SEG25	51	SEG50	76	SEG75
2	SEG1	27	SEG26	52	SEG51	77	SEG76
3	SEG2	28	SEG27	53	SEG52	78	SEG77
4	SEG3	29	SEG28	54	SEG53	79	SEG78
5	SEG4	30	SEG29	55	SEG54	80	SEG79
6	SEG5	31	SEG30	56	SEG55	81	EIO2
7	SEG6	32	SEG31	57	SEG56	82	D0
8	SEG7	33	SEG32	58	SEG57	83	D1
9	SEG8	34	SEG33	59	SEG58	84	D2
10	SEG9	35	SEG34	60	SEG59	85	D3
11	SEG10	36	SEG35	61	SEG60	86	D4
12	SEG11	37	SEG36	62	SEG61	87	D5
13	SEG12	38	SEG37	63	SEG62	88	D6
14	SEG13	39	SEG38	64	SEG63	89	D7
15	SEG14	40	SEG39	65	SEG64	90	V_{DD}
16	SEG15	41	SEG40	66	SEG65	91	V_{SS}
17	SEG16	42	SEG41	67	SEG66	92	V0
18	SEG17	43	SEG42	68	SEG67	93	V2
19	SEG18	44	SEG43	69	SEG68	94	V3
20	SEG19	45	SEG44	70	SEG69	95	V5
21	SEG20	46	SEG45	71	SEG70	96	SHL
22	SEG21	47	SEG46	72	SEG71	97	XSCL
23	SEG22	48	SEG47	73	SEG72	98	LP
24	SEG23	49	SEG48	74	SEG73	99	FR
25	SEG24	50	SEG49	75	SEG74	100	EIO1

BLOCK DESCRIPTION

Data Control

This circuitry controls the transfer of data between input pins D0 to D3 and the internal register, register 1. The locations in which the data is stored in register 1 depend on the level on the SHL pin. See section 2 for details.

If the driver is disabled (see below) the data control circuitry holds the internal data bus low.

Enable Control

If the daisy-chain enable input selected by SHL (see section 2 for detailes) is high, the driver is enabled. If the enable input is low, the internal clock and data bus are held low.

The enable control circuitry detects when register 1 has received 20 nibbles (80-bits) of display data and propagates a daisy chain enable via its enable output, as selected by SHL. This allows straightforward cascading of SED1601 segment drivers for large capacity displays.

The enable input of the first driver in the chain is tied to V_{DD}. The enable outputs of all drivers are reset by LP.

Clock Generator

This circuitry generates 20 shift-clocks, one per 4-bit channel of register, locked to XSCL.

Register 1

This regiser receives 4-bit parallel data from the D0 to D3 inputs, stores it in an order determined by SHL, and transfers it to register 2 on the falling edge of LP.

Register 2

This 80-bit register feeds the display data on the level shift circuitry.

Level Shift, LCD Drivers and Voltage Control

The level shift circuitry converts the TTL level data to the levels required by LCD driver using voltages from the voltage control block and the frame signal, FR. Table 1 shows the relationship between display data, FR and segment drive voltage.

Table 1. Drive Voltage vs. Data, FR

Contents of Register 2	FR	SEG
H	H	V_0
	L	V_5
L	H	V_2
	L	V_3

PIN DESCRIPTION

SEG0 to SEG79 LCD segment driver outputs

D0 to D7 Display data input

XSCL Data is shifted into the driver on the falling edge of this input signal.

LP Data is shifted into the LCD drive circuitry on the falling edge of this input.

SHL Shift direction and enable input/output select input. If data is shifted into the driver as 20 nibbles (80 bits) in the order (a1, a2, a3, a4, a5, a6, a7, a8), (b1, b2, b3, b4, b5, b6, b7, b8) . . . , (j1, j2, j3, j4, j5, j6, j7, j8), then SHL selects the relationship between segment and data and the configuration of the enable input/output as below.

SHL	SEG													EIO	
	79	78	77	76	75	74	73	72	. . .	3	2	1	0	1	2
L	a1	a2	a3	a4	a5	a6	a7	a8	. . .	j5	j6	j7	j8	Output	Input
H	j8	j7	j6	j5	j4	j3	j2	j1	. . .	a4	a3	a2	a1	Input	Output

EIO1, EIO2 Enable I/O lines. The line selected as input by SHL receives the active high daisy-chain enable from the preceding driver. The line selected as output by SHL propagates as active high daisy-chain enable when register 1 is full. The enable output is reset byLP.

FR LCD AC drive signal input

V_{DD}, V_{SS} Logic power inputs

V0, V2, V3, V5 LCD drive power inputs

$V_{DD} \geq V0 \geq V2 \geq V3 \geq V5$

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_2, V_3	V_5–0.3 to V_{DD}+0.3	V
Input pin voltage (1)	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage (1)	V_O	V_{SS}–0.3 to V_{DD}+0.3	V
Output pin current (1)	I_O	20	mA
Output pin current (2)	I_{OSEG}	20	mA
Operating temperature	Topr	–20 to +75	°C
Storage temperature 1	Tstg 1	–65 to +150(SED1601F$_{AA}$) –55 to +150(SED1601D$_{AA}$)	°C
Soldering temperature and time at lead	Tsol	260, 10	°C, s
Power dissipation	P_D	300	mW

Notes:

1. All voltages are referred to V_{DD} = 0V.
2. The LCD drive voltages must satisfy the condition $V_{DD} \geq V0, V2, V3 \geq V5$.
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced during the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

ELECTRICAL CHARACTERISTICS

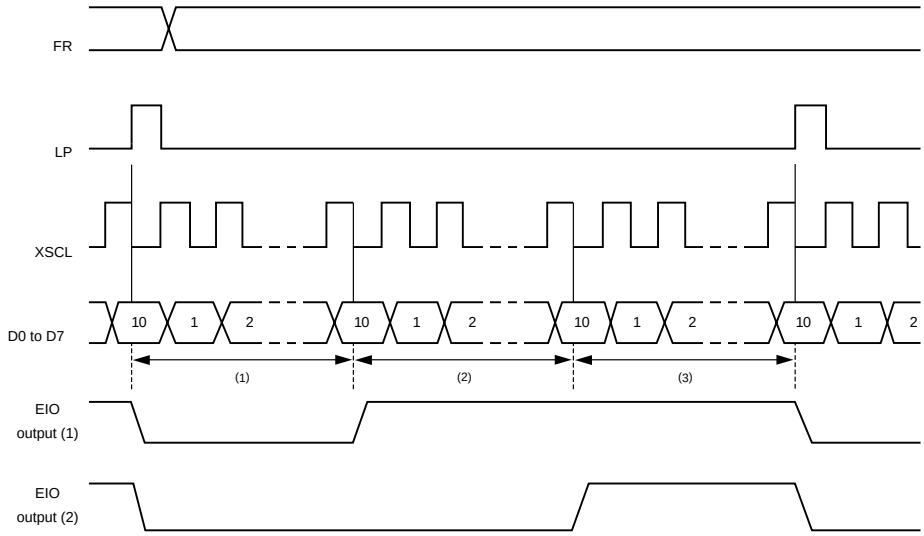
DC Characteristics

Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0V±10% and Ta = –20 to 75 °C

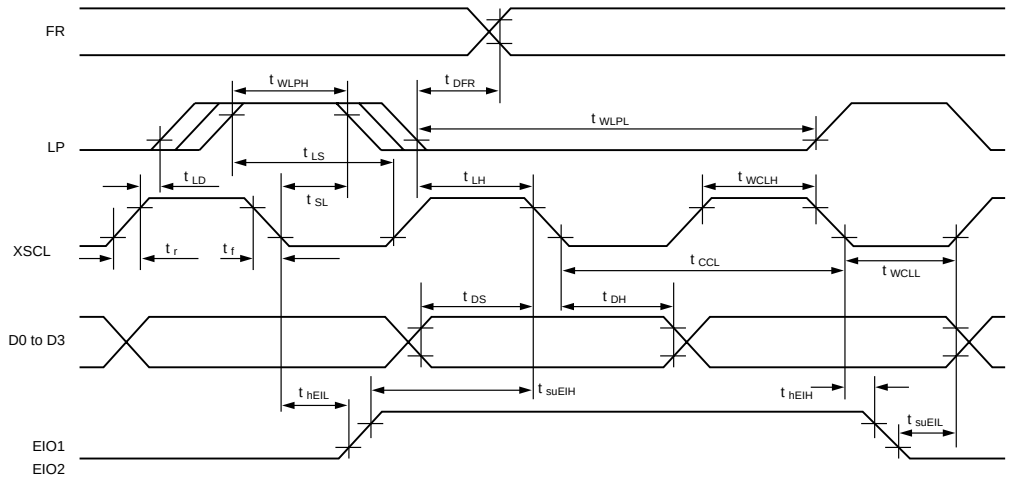
Parameter	Symbol	Condition	Rating			Unit	Pin
			Min.	Typ.	Max.		
Operating voltage (1)	—		–5.5	–5.0	–4.5	V	V_{SS}
Recommended operating voltage Min. operating voltage	—		–28.0	 –8.0	–12.0	V	V5
Operating voltage (2)	—		–2.5		0	V	V0
"H" input voltage	V_{IH}		0.2V_{SS}			V	EIO1, EIO2, XSCL, LP, D0 to D7, FR, SHL
"L" input voltage	V_{IL}				0.8V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH} = –0.6 mA	–0.4			V	EIO1, EIO2
"L" output voltage	V_{OL}	I_{OL} = 0.6 mA			V_{SS}+0.4	V	
Input leakage current	V_{LI}	$V_{SS} \le V_{IN} \le 0V$			2.0	µA	D0 to D7, XSCL, LP, SHL, FR
Input/output current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$			5.0	µA	EIO1, EIO2
Static current	I_{DDS}	V5 = –12.0 to –28.0V VIH = V_{DD}, VIL = V_{SS}			25	µA	V_{DD}
Output resistance	R_{SEG}	|ΔV_{ON}| = 0.5V, V5 = –20.0V		2.0		kΩ	SEG0 to SEG79
		V5 = –14.0V		2.5			
		V5 = –8.0V		4.0			
Current dissipation (1)	I_{SSO1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{XSCL} = 1.5MHz f_{LP} = 7.7kHz, Frame period = 16.67ms, Input data: Inverted bit by bit No-load		120	500	µA	V_{SS}
Current dissipation (2)	I_{SSO2}	V_{SS} = –5.0V, V2 = –4.0V, V3 = –16.0V, V5 = –20.0V All other conditions are same as I_{SS1}.		20	100	µA	V5
Input capacitance	C_I	Ta = 25 °C			8.0	pF	D0 to D7, XSCL, LP, FR, SHL
Input/output capacitance	$C_{I/O}$				15.0	pF	EIO1, EIO2

AC Characteristics

Input timing



Note: (1), (2) and (3) are cascaded drivers.



Ta = –20 to 75 deg. C, V_{SS} = –5.0V±10%

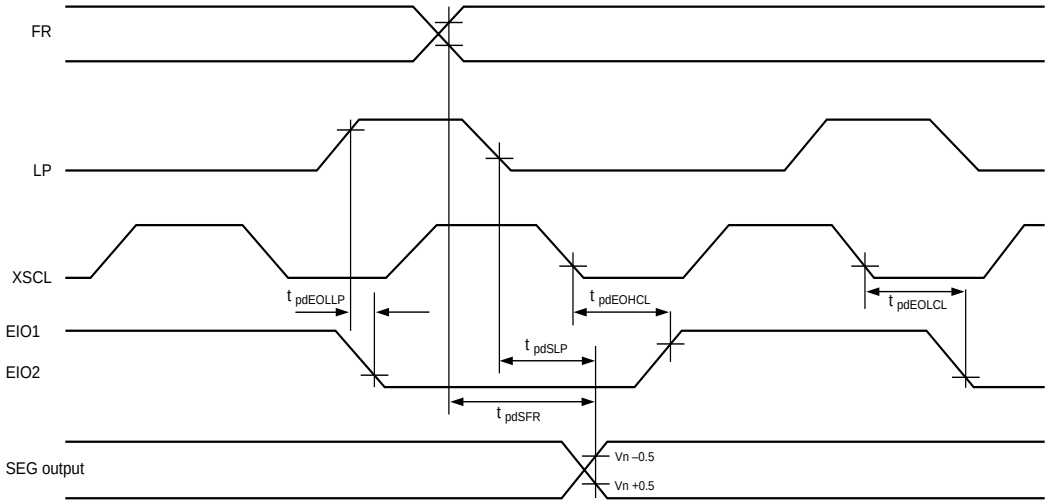
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
XSCL period	t_{CCL}	t_r, t_f ≤10 ns	166		ns
XSCL "H" pulse width	t_{WCLH}		70		ns
XSCL "L" pulse width	t_{WCLL}		70		ns
Data setup time	t_{DS}		60		ns
Data hold time	t_{DH}		40		ns
XSCL-rise to LP-rise time	t_{LD}		0		ns
XSCL-fall to LP-fall time	t_{SL}		70		ns
LP-rise to XSCL-rise time	t_{LS}		70		ns
LP-fall to XSCL-fall time	t_{LH}		70		ns
LP "H" pulse width	t_{WLPH}		70		ns
LP "L" pulse width	t_{WLPL}		230		ns
Allowable FR delay time	t_{DFR}		–500	500	ns
Enable "H" setup time	t_{SUEIH}		40		ns
Enable "H" hold time	t_{hEIH}		0		ns
Enable "L" setup time	t_{SUEIL}		0		ns
Enalbe "L" hold time	t_{hEIL}		0		ns
Input signal rise time	t_r			50 (NOTE)	ns
Input signal fall time	t_f			50 (NOTE)	ns

Note: These limits on signal transition times reduce the likelihood of noise during trnasitions causing a malfunction. This is especially important for the falling edge of XSCL.

t_r and t_f should satisfy the following relation ship

$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

Output Timing Characteristics



$V_{IH}=V_{OH}=0.2 \times V_{SS}$

$V_{IL}=V_{OL}=0.8 \times V_{SS}$

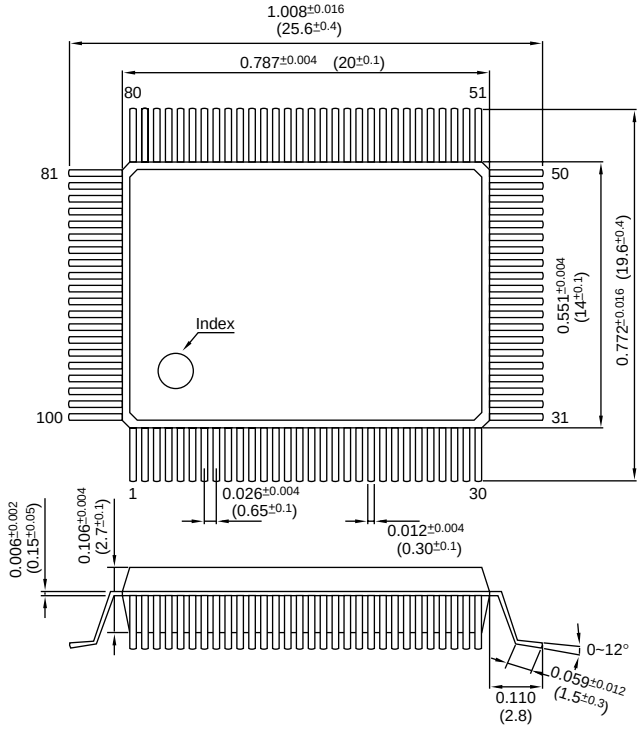
Ta = –20 to 75 °C, V_{SS} = –5.0V±10%

Parameter	Symbol	Condition		Rating		Unit
				Min.	Max.	
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L"	C_L = 15 pF		70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H"			70	ns
(XSCL-rise to enable) time	$t_{pdEOHCL}$				100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = –12.0 to –28.0V C_L = 100 pF			4.5	µs
(FR to SEG output) delay time	t_{pdSFR}				4.5	µs

Mechanical Specifications

SED1601F

Dimensions: inches(mm)



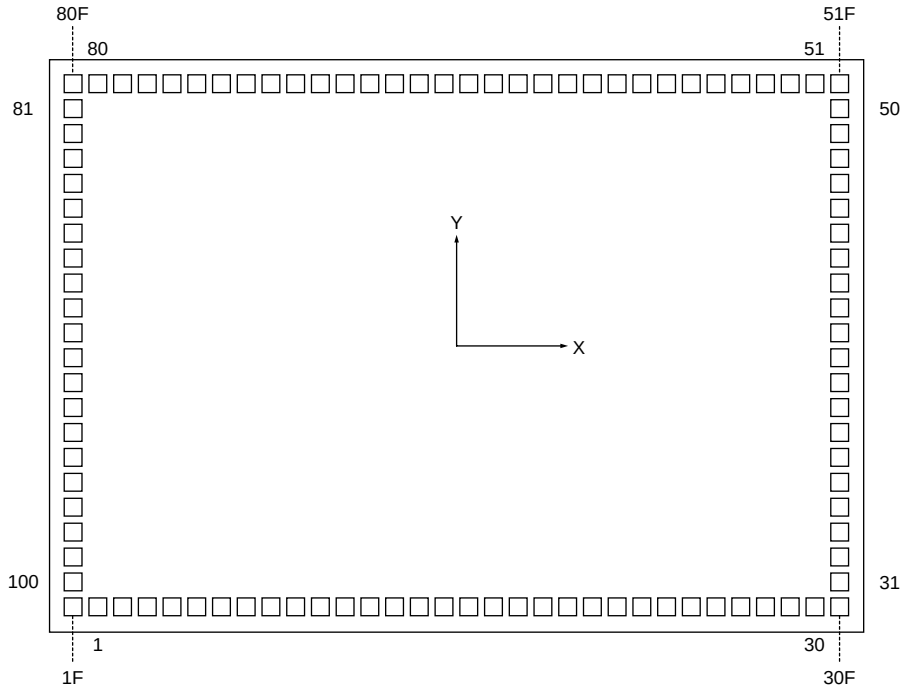
SED1601D

Chip size: 6.20 mm × 4.59 mm

Chip thickness: 0.44 mm ±0.025 mm

Pad size: 0.1 mm × 0.1 mm

Pad size: 0.18 mm (minimum)



Pad number	Pad name	X (µm)	Y (µm)
1	SEG0	–2700	–2120
2	SEG1	–2503	–2120
3	SEG2	–2306	–2120
4	SEG3	–2109	–2120
5	SEG4	–1912	–2120
6	SEG5	–1714	–2120
7	SEG6	–1534	–2120
8	SEG7	–1354	–2120
9	SEG8	–1174	–2120
10	SEG9	–994	–2120
11	SEG10	–813	–2120
12	SEG11	–633	–2120
13	SEG12	–453	–2120
14	SEG13	–273	–2120
15	SEG14	–93	–2120
16	SEG15	88	–2120
17	SEG16	268	–2120
18	SEG17	448	–2120
19	SEG18	628	–2120
20	SEG19	808	–2120
21	SEG20	989	–2120
22	SEG21	1169	–2120
23	SEG22	1349	–2120
24	SEG23	1529	–2120
25	SEG24	1709	–2120
26	SEG25	1907	–2120
27	SEG26	2104	–2120
28	SEG27	2301	–2120
29	SEG28	2498	–2120
30	SEG29	2695	–2120
31	SEG30	2925	–1895
32	SEG31	2925	–1669
33	SEG32	2925	–1443
34	SEG33	2925	–1217
35	SEG34	2925	–991

Pad number	Pad name	X (µm)	Y (µm)
36	SEG35	2925	–811
37	SEG36	2925	–631
38	SEG37	2925	–450
39	SEG38	2925	–270
40	SEG39	2925	–90
41	SEG40	2925	90
42	SEG41	2925	270
43	SEG42	2925	451
44	SEG43	2925	631
45	SEG44	2925	811
46	SEG45	2925	991
47	SEG46	2925	1217
48	SEG47	2925	1443
49	SEG48	2925	1669
50	SEG49	2925	1896
51	SEG50	2695	2120
52	SEG51	2498	2120
53	SEG52	2301	2120
54	SEG53	2104	2120
55	SEG54	1907	2120
56	SEG55	1709	2120
57	SEG56	1529	2120
58	SEG57	1349	2120
59	SEG58	1169	2120
60	SEG59	989	2120
61	SEG60	808	2120
62	SEG61	628	2120
63	SEG62	448	2120
64	SEG63	268	2120
65	SEG64	88	2120
66	SEG65	–93	2120
67	SEG66	–273	2120
68	SEG67	–453	2120
69	SEG68	–633	2120
70	SEG69	–813	2120

Pad number	Pad name	X (µm)	Y (µm)
71	SEG70	–994	2120
72	SEG71	–1174	2120
73	SEG72	–1354	2120
74	SEG73	–1534	2120
75	SEG74	–1714	2120
76	SEG75	–1912	2120
77	SEG76	–2109	2120
78	SEG77	–2306	2120
79	SEG78	-2503	2120
80	SEG79	-2700	2120
81	EIO2	–2925	1896
82	D0	–2925	1669
83	D1	–2925	1443
84	D2	–2925	1217
85	D3	–2925	991
86	D4	–2925	811
87	D5	–2925	631
88	D6	–2925	451
89	D7	–2925	270
90	V_{DD}	–2925	90
91	V_{SS}	–2925	90
92	V0	–2925	270
93	V2	–2925	450
94	V3	–2925	631
95	V5	–2925	811
96	SHL	–2925	991
97	XSCL	–2925	1217
98	LP	–2925	1443
99	FR	–2925	1669
100	EIO1	–2925	1895
1F	SEG0	–2925	–2120
30F	SEG29	2925	–2120
51F	SEG50	2925	2120
80F	SEG79	–2925	2120

APPLICATION NOTES

Generating LCD Drive Voltages

The LCD drive voltages need to be accurately and stably generated if a good quality display is to be achieved.

The easiest way to generate these voltages is to use a resistive divider network, however is should be noted that LCD panels present a significant capacitive load, resulting in high transient currents when the segment drive voltages are switched. It is good practice to put surge compensating capacitors in the divider network, but if the source resistance of the network is too high, distortion of the drive waveform will still resutlt. In this case the only solution is to reduce the divider network source resistance

Bacause low divider network source resistance increases the system current consumption, if you are disigning with low power operation in mind, it is recommended that a voltage follower op-amp be used to generate the LCD drive voltages. The driver is designed so that V0 is isolated from V_{DD}, allowing op-amps to be used. Note that V_{DD} –V0 should be less than 2.5V as a higher potential difference will degrade tha LCD drive capability of the SED1601. If a resistive divider network is used, V_{DD} and V0 should be tied together.

System Power-up

If LCD drive level voltages are connected to the driver **BEFORE** the logic circuits are powered up, large currents will flow in the device, **DAMAGING** the chip.

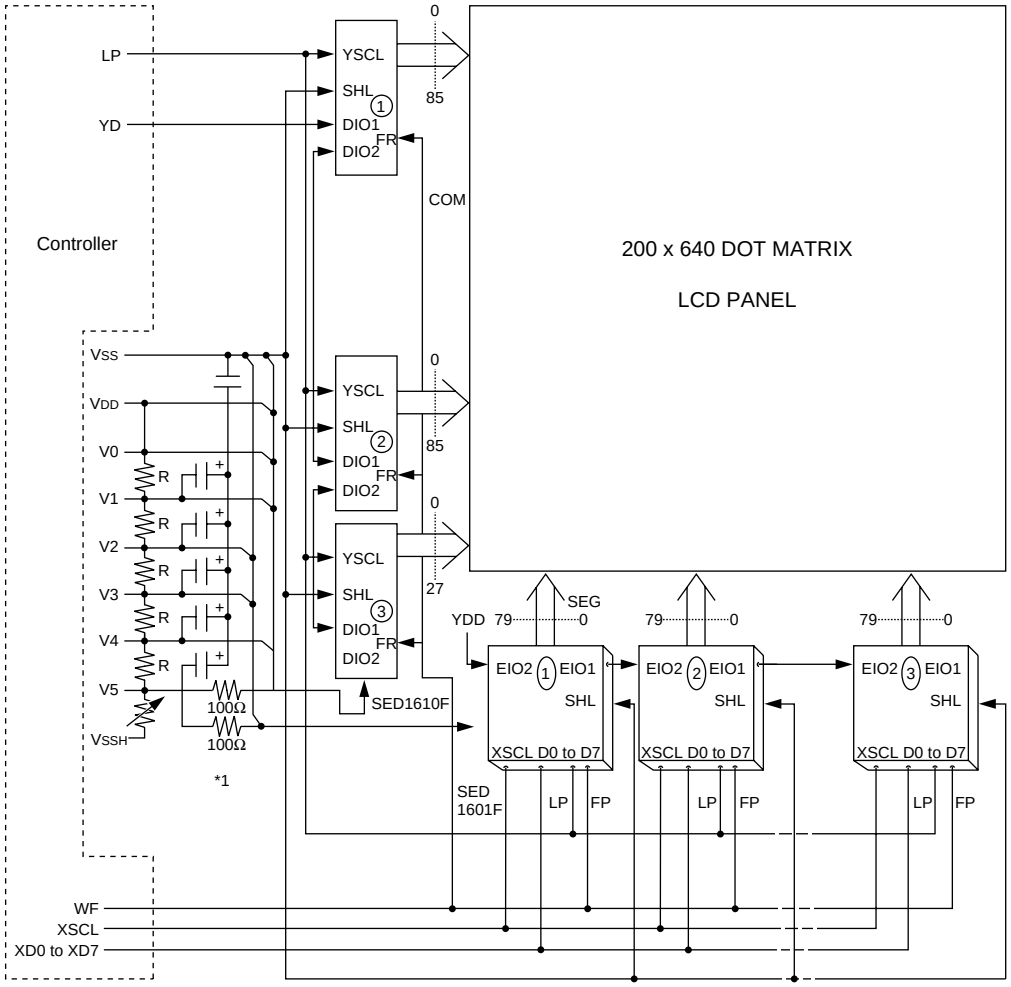
POWER ON: Logic power on before, or simultaneously with, LCD power on.

POWER OFF: LCD power off before, or simultaneously with, logic power off.

It is recommended that a current limiting resistor of about 100Ω is placed in series with V5.

Typical Application

200×640 Dot Matrix Display System



3. SED1606
Dot Matrix LCD Segment Driver

CONTENTS

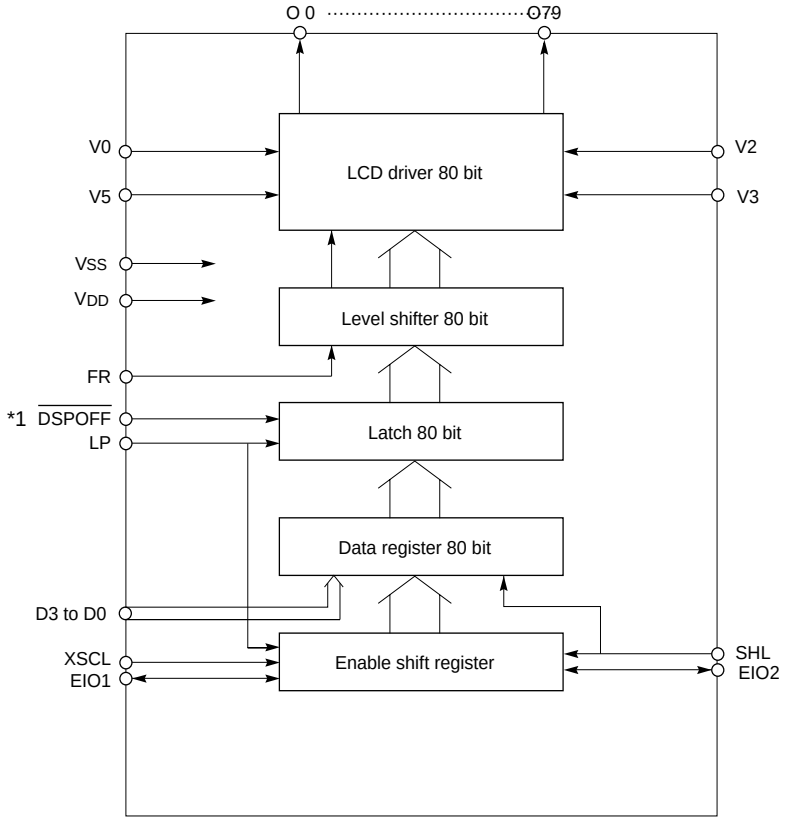
OVERVIEW

The SED1606 is an 80 output segment (column) driver which is suitable for driving a very high capacity dot-matrix LCD panels. It is intended to be used in conjunction with the SED1670/72 as a pair.
The SED1606 is featured in a high quality of picture in LCD display. It employs a high-speed enable chain system which is favorable to a low-power driving. Allowed to be operated with a low voltage in the logic system power supply, it can meet a wide range of applications.

FEATURES

- Number of LCD drive output segments: 80
- Low current consumption
- Low voltage operation: –2.7 V (Max.)
- Wide range of LCD drive voltages: –8 V to –28 V
- High-speed and low-power data transfer enabled by means of a 4-bit bus and chain enable support
  Shift clock frequency: 6.5 MHZ (at –2.7 V)
  10.0 MHZ (at –4.5 V)
- Selectable pin output shift direction
- Adjustable offset bias of LCD power to a V_{DD} level
- Logic system power supply : –2.7 V to –5.5 V
- Chip packaging
  SED1606D0A (AL-pad die form)
  SED1606D0B (Au bump die form)
  SED1606D1A (AL-pad die form)
  SED1606D1B (Au bump die form)
  PKG SED1606F0A (QFP5-100 pin)
- No radial rays countermeasure taken in designing

BLOCK DIAGRAM



1 Dummy terminal NC when SED1606D0 is used.
DSPOFF terminal when SED1606D1* is used

PIN DESCRIPTION

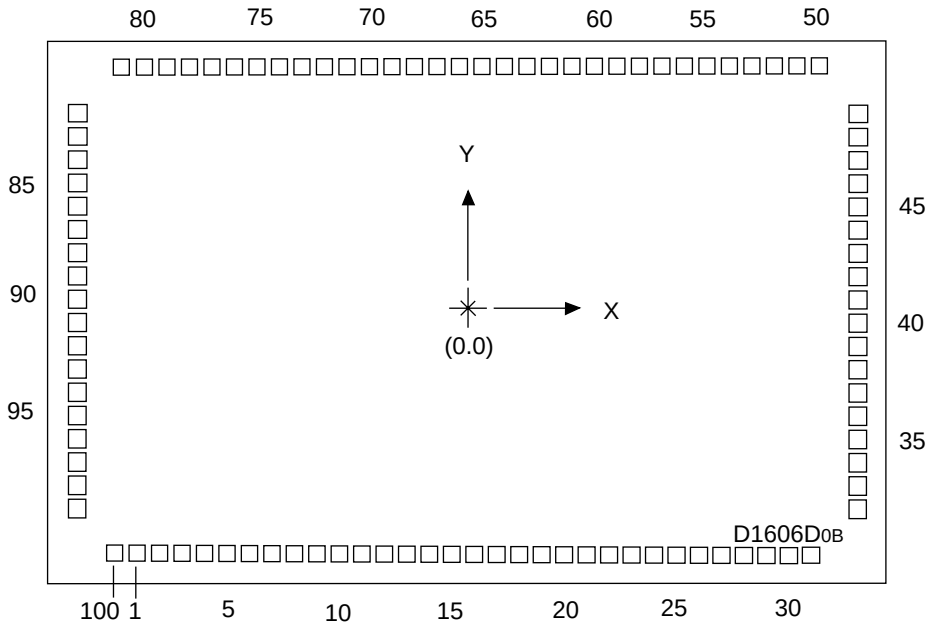
<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>O0 ~ O79</td><td>O</td><td>Segment (column) output for LCD driving
The output changes at the LP falling edge.</td><td>80</td></tr>
<tr><td>D0 ~ D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (Falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (Falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Enable input/output
To be set to input or output according to the SHL input level.
The output is reset by the LP input. Upon the end of fetching of 80-bit data, the system starts up automatically to “H”.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO pin I/O control input When data is input to (D3, D2 ... D0) pins sequentially in order of (a3, a2, a1, a0), (b3, b2, b1, b0) ... (t3, t2, t1, t0), the relationship between the data and segment output becomes as shown in the table below:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a3</td><td>b2</td><td>c1</td><td>. . .</td><td>t2</td><td>t1</td><td>t0</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>t0</td><td>t1</td><td>t2</td><td>. . .</td><td>a1</td><td>a2</td><td>a3</td><td>Input</td><td>Output</td></tr>
</table>
(Note) The relationship between the data and segment output is determined irrespective of the number of shift clock inputs.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output AC converted signal input</td><td>1</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>Force input of blank
V0 level is forcibly set by entering “L” level (available with SED1606D1∗ alone).</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V V_{SS}: –2.7 V to –5.5 V</td><td>2</td></tr>
<tr><td>V0, V2, V3, V5

*1</td><td>Power supply</td><td>LCD drive circuit power supply
V_{DD}: 0 V V_5: –8 V to –28 V
$V_{DD} \geq V_0 \geq V_2 \geq 6/9\ V_5$
$3/9\ V_5 \geq V_3 \geq V_5$
When used at a same potential, V_0 and V_{DD} are used by grounding them close to the IC chip.</td><td>4</td></tr>
</table>

*1 Be sure to connect V_0 to V_5 to their LCD power, respectively.

Total: 100
SED1606D0∗ (including four NC’4)
SED1606D1∗ (including four NC’3)

PAD LAYOUT AND COORDINATES



Chip size: ..... 5.59 mm × 3.50 mm
Pad pitch: ..... 0.153 mm (Min.)
Chip thickness: ..... 0.400 mm (AL-pad die form)
0.525 mm (Au-bump die form)

Au bump specifications [Reference values]

Bump size: 117μm × 109μm ± 20 um
Bump height: 17μm to 28μm (Details shall be stipulated in the delivery specification.)

AL-pad die form

Pad Opening 87×76μm

Unit (μm)

PAD		Actual dimensions	
NO.	NAME	X	Y
1	O0	–2227	–1578
2	O1	–2073	
3	O2	–1920	
4	O3	–1766	
5	O4	–1612	
6	O5	–1459	
7	O6	–1305	
8	O7	–1152	
9	O8	–998	
10	O9	–845	
11	O10	–691	
12	O10	–537	
13	O12	–384	
14	O13	–230	
15	O14	–76	
16	O15	77	
17	O16	231	
18	O17	384	
19	O18	538	
20	O19	692	
21	O20	845	
22	O21	999	
23	O22	1152	
24	O23	1306	
25	O24	1460	
26	O25	1613	
27	O26	1767	
28	O27	1921	
29	O28	2074	
30	O29	2228	
31	O30	2381	
32	O31	2622	–1346
33	O32		–1188
34	O33		–1029

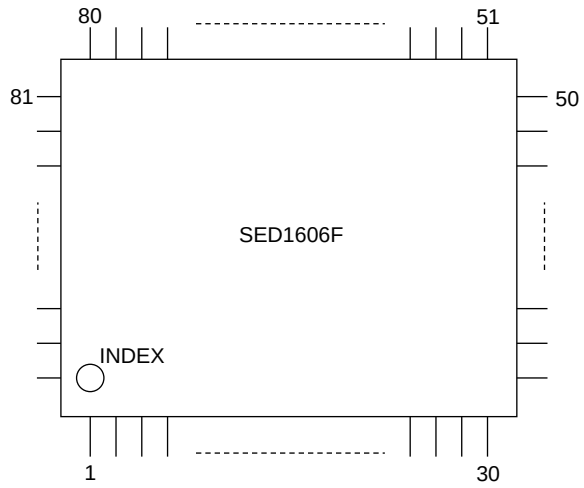
PAD		Actual dimensions	
NO.	NAME	X	Y
35	O34	2622	–871
36	O35		–713
37	O36		–554
38	O37		–396
39	O38		–238
40	O39		–79
41	O40		79
42	O41		238
43	O42		396
44	O43		554
45	O44		713
46	O45		871
47	O46		1029
48	O47		1188
49	O48		1346
50	O49	2381	1578
51	O50	2228	
52	O51	2074	
53	O52	1921	
54	O53	1767	
55	O51	1613	
56	O55	1460	
57	O56	1306	
58	O57	1152	
59	O58	999	
60	O59	845	
61	O60	692	
62	O61	538	
63	O62	384	
64	O63	231	
65	O64	77	
66	O65	–76	
67	O66	–230	
68	O67	–384	

PAD		Actual dimensions	
NO.	NAME	X	Y
69	O68	–537	1578
70	O69	–691	
71	O70	–846	
72	O71	–998	
73	O72	–1152	
74	O73	–1305	
75	O74	–1459	
76	O75	–1613	
77	O76	–1766	
78	O77	–1920	
79	O78	–2073	
80	O79	–2227	
81	EIO2	–2381	
82	D0	–2622	1346
83	D1		1192
84	D2		1039
85	D3		885
86	Dummy		732
87	Dummy		578
88	Dummy		424
89	*1		271
90	V_{DD}		106
91	V_{SS}		–58
92	V0		–224
93	V2		–389
94	V3		–553
95	V5		–718
96	SHL	–2611	–885
97	XSCL		–1039
98	LP		–1192
99	FR		–1346
100	EIO1	–2381	–1578

1: Pad No.89 is dummy when SED1606D0 is used.
It will be DSPOFF with SED1606D1*.

PIN LAYOUT

Package Type: QFP–5 100pin



PIN No.	NAME	PIN No.	NAME	PIN No.	NAME	PIN No.	NAME	PIN No.	NAME
1	O0	21	O20	41	O40	61	O60	81	EIO2
2	O1	22	O21	42	O41	62	O61	82	D0
3	O2	23	O22	43	O42	63	O62	83	D1
4	O3	24	O23	44	O43	64	O63	84	D2
5	O4	25	O24	45	O44	65	O64	85	D3
6	O5	26	O25	46	O45	66	O65	86	NC
7	O6	27	O26	47	O46	67	O66	87	NC
8	O7	28	O27	48	O47	68	O67	88	NC
9	O8	29	O28	49	O48	69	O68	89	*1
10	O9	30	O29	50	O49	70	O69	90	V_{DD}
11	O10	31	O30	51	O50	71	O70	91	V_{SS}
12	O11	32	O31	52	O51	72	O71	92	V0
13	O12	33	O32	53	O52	73	O72	93	V2
14	O13	34	O33	54	O53	74	O73	94	V3
15	O14	35	O34	55	O54	75	O74	95	V5
16	O15	36	O35	56	O55	76	O75	96	SHL
17	O16	37	O36	57	O56	77	O76	97	XSCL
18	O17	38	O37	58	O57	78	O77	98	LP
19	O18	39	O38	59	O58	79	O78	99	FR
20	O19	40	O39	60	O59	80	O79	100	EIO1

1: Pad No.89 is dummy when SED1606D0 is used.
It will be DSPOFF with SED1606D1*.

FUNCTIONAL DESCRIPTION

Enable shift register

This is a bidirectional shift register with which the shift direction is selected by SHL input. The output of this shift register is used to store the data bus signals to data register.
When the enable signal is in the disable status, the internal clock signal and data bus are fixed to "L" and the system is made into the power save mode.
When using two or more segment drivers, connect the EIO pin of each driver in a cascade arrangement and the EIO pin of the leading driver to "V_{DD}".
Since the enable controller circuit automatically detects that the data for 80 bits have been fetched thoroughly and then transfers the enable signal to the controller, it is not necessary to provide the control signal using the control LSI.

Data register

This is a register used to convert the data bus signal into serial or parallel signal through the enable shift register output. Consequently, the relationship between the serial display data and segment output is determined irrespective of the number of shift clock inputs.

Latch

This latch is used to fetch the content of data register at the LP falling edge trigger and to send its output to the level shifter.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver

This driver outputs the LCD drive voltage.
The relationship among the data bus signal, AC converted signal FR and segment output voltage is as shown in the table below:

(SED1606D0*)

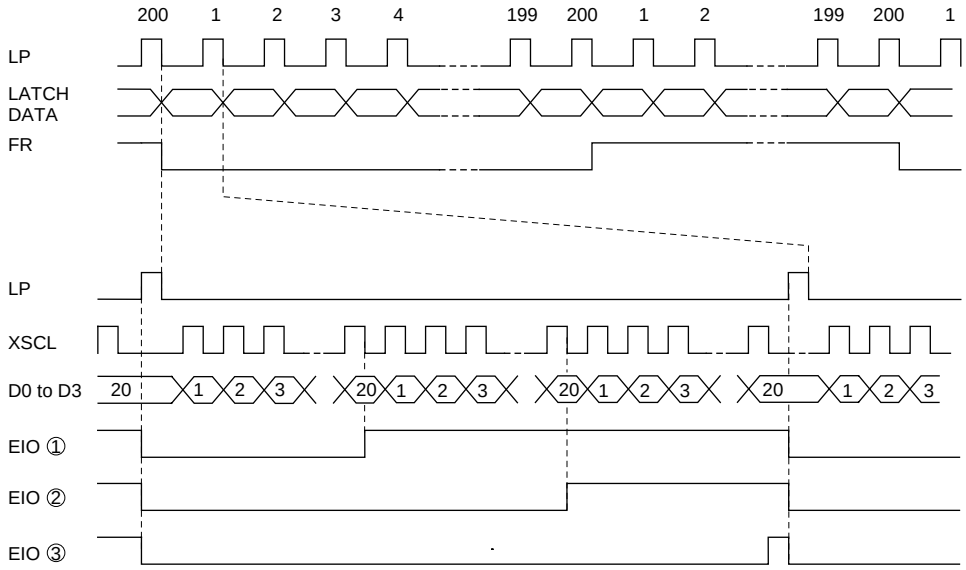
Data bus signal	FR	O output voltage
H	H	V_0
	L	V_5
L	H	V_2
	L	V_3

(SED1606D1*)

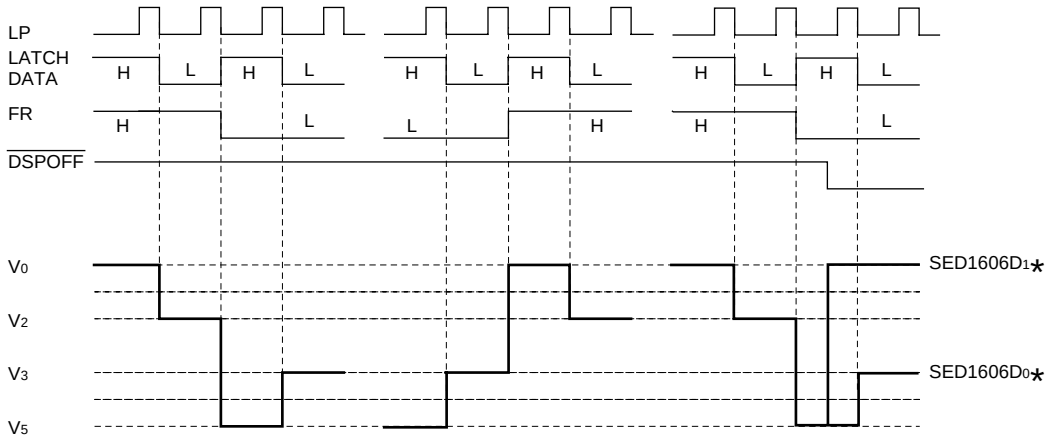
$\overline{DSPOFF}$	Data bus signal	FR	O output voltage
H	H	H	V_0
		L	V_5
H	L	H	V_2
		L	V_3
L	—	—	V_0

TIMING CHART

When the duty is 1/200 (Reference Example)



① to ③ stand for a cascaade No. of driver.



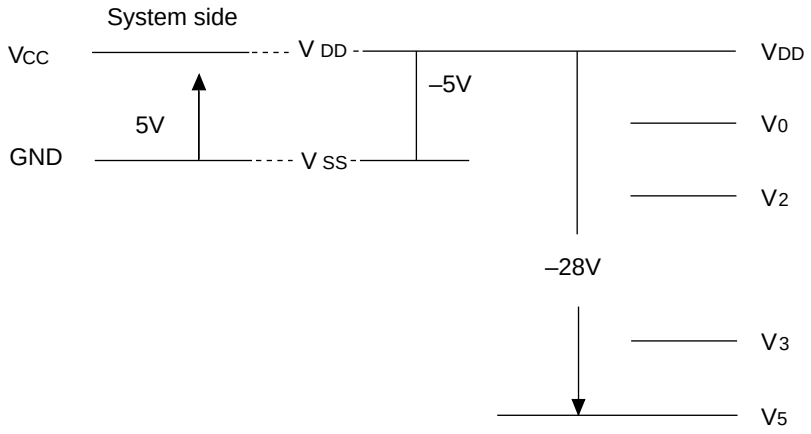
When SED1606D1* is used:
The driver output is forcibly switched to
V0 output upon switching of $\overline{\text{DSPOFF}}$

ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V_5	–30.0 to +0.3	V
Power voltage (3)	V_0, V_2, V_3	V_5–0.3 to V_{DD}+0.3	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage	V_O	V_{SS}–0.3 to V_{DD}+0.3	V
EIO output current	I_O	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg 1	–65 to +150	°C

Notes:
1. The storage temperature 1 stipulates the temperature by unit of a chip.
2. The voltage of V_0, V_2 and V_3 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$.



3. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.

ELECTRICAL CHARACTERISTICS

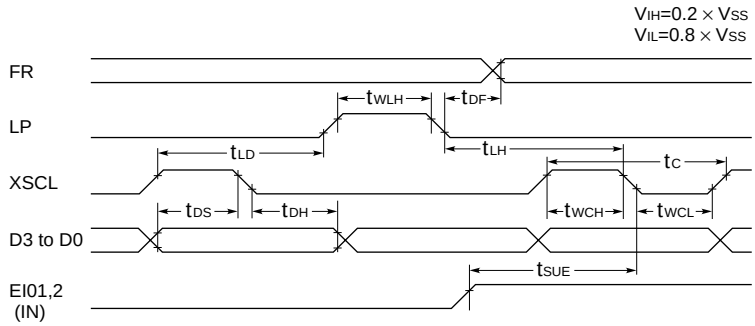
DC characteristics

Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V±10% and Ta = –40 to 85°C.

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–		–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	V_{SS}=–2.7 to –5.5V		–28.0	–	–12.0	V	V_5
Operation enable voltage	V_5	Function		–	–	–8.0	V	V_5
Supply voltage (2)	V_0	Recommended value		V_{DD}–2.5	–	V_{DD}	V	V_0
Supply voltage (3)	V_2	Recommended value		3/9V_5	–	–	V	V_2
Supply voltage (4)	V_3	Recommended value		V_5	–	6/9V_5	V	V_3
"H" input voltage	V_{IH}	V_{SS}=–2.7 to –5.5V		0.2V_{SS}	–	–	V	EIO1, EIO2, FR, D0 to D3, XSCL, SHL, LP
"L" input voltage	V_{IL}			–	–	0.8V_{SS}	V	
"H" output voltage	V_{OH}	V_{SS}=–2.7 to –5.5V	I_{OH}=–0.6mA	V_{DD}–0.4	–	–	V	EIO1, EIO2
"L" output voltage	V_{OL}		I_{OL}=0.6mA	–	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		–	–	2.0	µA	D0 to D3, LP, FR XSCL, SHL
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$		–	–	5.0	µA	EIO1, EIO2
Static current	I_{SS}	V5=–28.0 to –14.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}		–	–	25	µA	V_{SS}
Output resistance	R_{SEG}	ΔV_{ON}=0.5V V_5=–20.0V V_3=13/15·V_5 V_2=2/15·V_5 V_0=V_{DD} Ta=25°C		–	1.2	1.6	KΩ	O0 to O79
Average operating current consumption (1)	I_{SS}	V_{SS}=–5.0V, V_{IH}=V_{DD} V_{IL}=V_{SS}, f_{XSCL}=2.69MHz f_{LP}=16.8KHz, f_{FR}=70Hz Input data: Dice display at no load		–	0.10	0.2	mA	V_{SS}
		V_{SS}=–3.0V Other conditions are the same as V_{SS} = -5 V		–	0.07	0.15		
Average operating current consumption (2)	I_5	V_{SS}=–5.0V, V_0=0.0V, V_2=–9.3V V_3=–18.6V, V_5=–28.0V Other conditions are the same as in the item of I_{SS}.		–	0.05	0.08	mA	V_5
Input pin capacitance	C_I	Freq.=1MHz Ta=25°C By unit of a chip		–	–	8	pF	D0 to D3, LP, FR XSCL, SHL
Input/output pin capacitance	$C_{I/O}$			–	–	15	pF	EIO1, EIO2

AC CHARACTERISTICS

Input timing characteristics



VSS=–5.0V±0.5V, Ta=–40 to 85°C

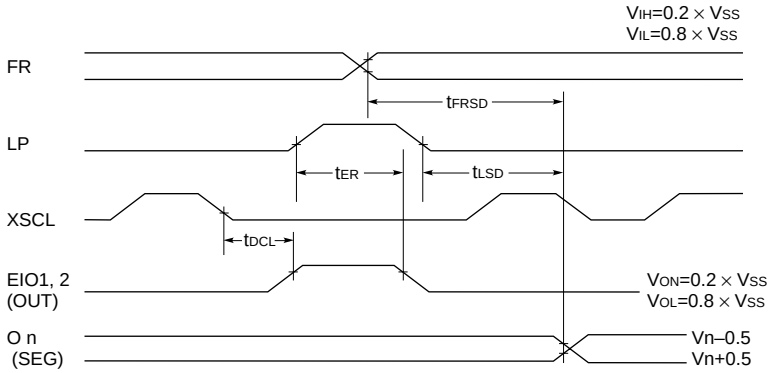
Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	t_C	–	100	–	ns
XSCL “H” pulsewidth	t_{WCH}	–	30	–	ns
XSCL “L” pulsewidth	t_{WCL}	–	30	–	ns
Data setup time	t_{DS}	–	20	–	ns
Data hold time	t_{DH}	–	10	–	ns
XSCL-rise to LP-rise time	t_{LD}	–	0	–	ns
LP-fall to XSCL-fall time	t_{LH}	–	40	–	ns
LP “H” pulsewidth	t_{WLH}	*3	40	–	ns
Allowable FR delay time	t_{DF}	–	–900	+900	ns
EIO setup time	t_{SUE}	–	35	–	ns

VSS=–4.5V to –2.7V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	t_C	VSS=–2.7V *1	153	–	ns
		VSS=–3.0V *2	133	–	
XSCL “H” pulsewidth	t_{WCH}	–	50	–	ns
XSCL “L” pulsewidth	t_{WCL}	–	50	–	ns
Data setup time	t_{DS}	–	30	–	ns
Data hold time	t_{DH}	–	15	–	ns
XSCL-rise to LP-rise time	t_{LD}	–	0	–	ns
LP-fall to XSCL-fall time	t_{LH}	VSS=–2.7V	75	–	ns
		VSS=–3.0V	65	–	
LP “H” pulsewidth	t_{WLH}	VSS=–2.7V *3	75	–	ns
		VSS=–3.0V *3	65	–	
Allowable FR delay time	t_{DF}	–	–900	+900	ns
EIO setup time	t_{SUE}	VSS=–2.7V	60	–	ns
		VSS=–3.0V	51	–	

*1 Equivalent to 6.5 MHz
*2 Equivalent to 7.5 MHz
*3 t_{WLH} stipulates the time when LP is “H” and XSCL is “L”.
*4 t_r and t_f of input signal are stipulated by unit of 20 ns.
*5 At a high-speed operation, t_r and t_f = {t_C – (t_{DCL} + t_{SUE})}/2

Output timing characteristics



V_{DD}=–5.0±0.5V, V_5=–12.0 to –28.0V

Parament	Symbol	Condition	Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)	–	90	ns
EIO output delay time	t_{DCL}		–	55	ns
LP to SEG output delay time	t_{LSD}	C_L=100pF (On)	–	200	ns
FR to SEG output delay time	t_{FRSD}		–	400	ns

V_{DD}=–4.5V to 2.7V, V_5=–12.0 to –28.0V

Parament	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)		–	150	ns
EIO output delay time	t_{DCL}		V_{SS}=–2.7V	–	88	ns
			V_{SS}=–3.0V	–	77	ns
LP to SEG output delay time	t_{LSD}	C_L=100pF (On)		–	400	ns
FR to SEG output delay time	t_{FRSD}			–	800	ns

*1 t_r and t_f of input signal are stipulated by unit of 20 ns.
*2 At a high-speed operation, t_r and t_f = {t_C – (t_{DCL} + t_{SUE})}/2

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is optimum to divide the resistance of potential between V_5 and V_{DD} to drive the LCD using the voltage follower with an operational amplifier. In taking into consideration of such a case using the operational amplifier, the maximum potential level V_0 for LCD driving has been made a separate pin from V_{DD}.
When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD}.

When no operational amplifier is used, connect V_0 and V_{DD} close to the IC chip.
When a series resistance exists in the power supply line of V_5 and V_{DD}, a voltage drop of V_5 and V_{DD} occurs at the LSI power supply pin, the relationship with the LCD's intermediate potential ($V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$) cannot be met, this causing the LSI to be broken down in some cases. When a protection resistor is inserted, it is necessary to stabilize the voltage by capacitance.

Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating or above V_{SS} = –2.6 V, and when the LCD driving signal is output before the applied voltage to the LCD driving system is stabilized, an overcurrent flows and LSI breaks down in some cases.

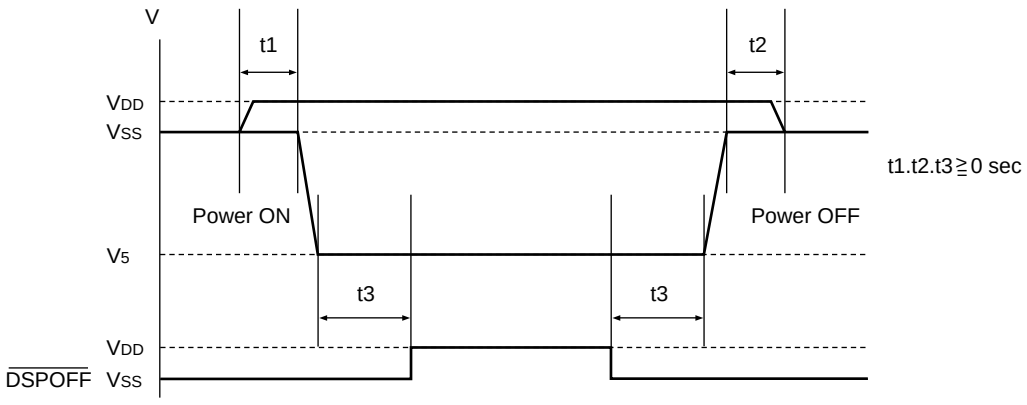
Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF .. LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

For a countermeasure to such overcurrent, it is effective to put a high-speed melting fuse or protection resistor in series with the LCD power unit.
It is then required to select the optimum value in the protection resistance according to the capacitance of LC cell.

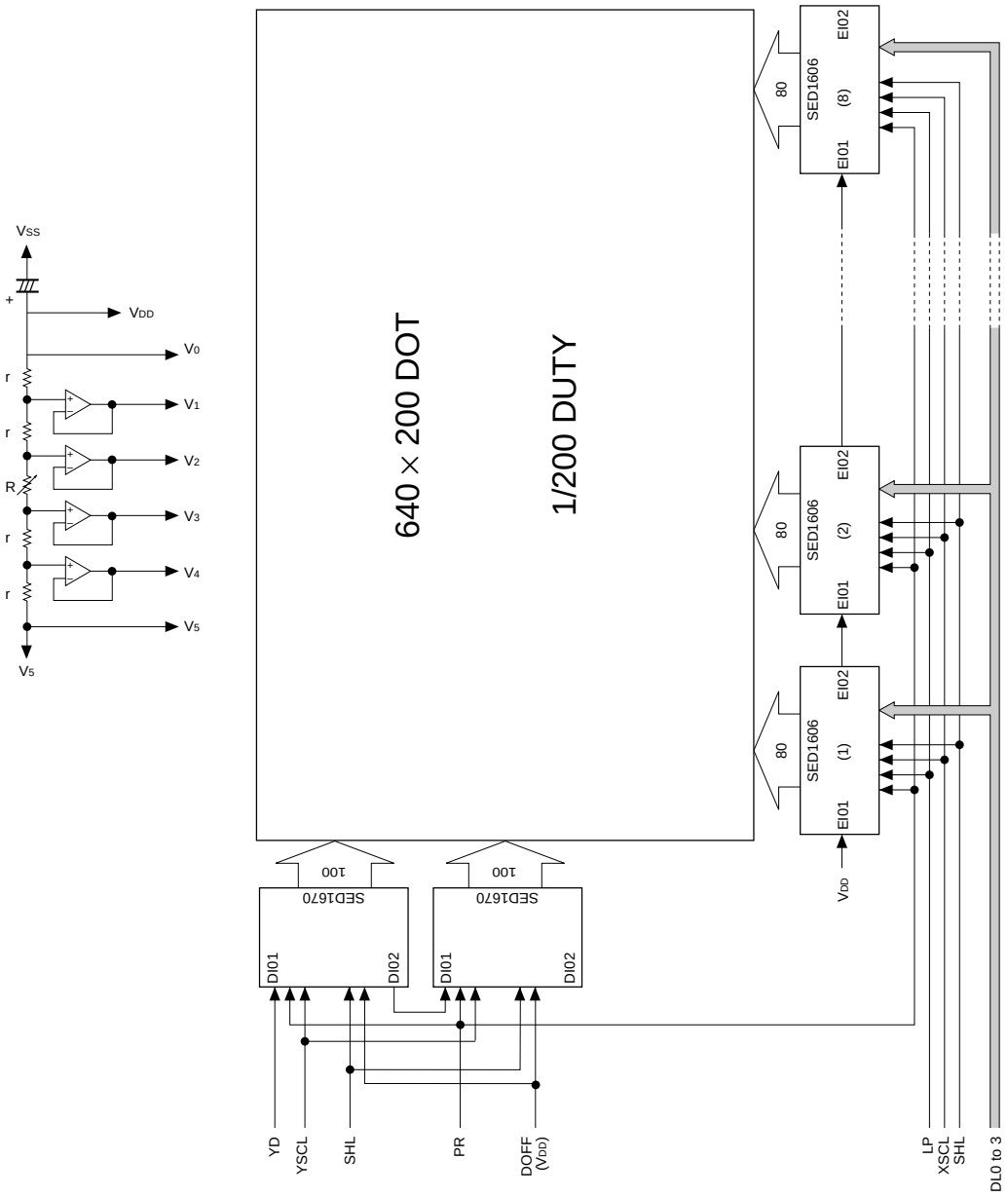
Until the LCD driver voltage stabilizes. It is recommended to set the LCD driver output potential to V0 using the display off function (DSPOFF).

Power ON/OFF sequence when SED1606D1∗ is used



TYPICAL CIRCUIT DIAGRAM

Configuration Drawing of Large Screen LCD



4. SED1620D0A
Dot Matrix LCD Segment Driver

CONTENTS

OVERVIEW

The SED1620D0A is a dot matrix LCD segment (column) driver for use with high capacity, high duty cycle LCD panels.

The SED1620D0A has 128 segment drive outputs and can operate at duty cycles up to1/300, when used in combination with the SED1631D0A common (row) driver.

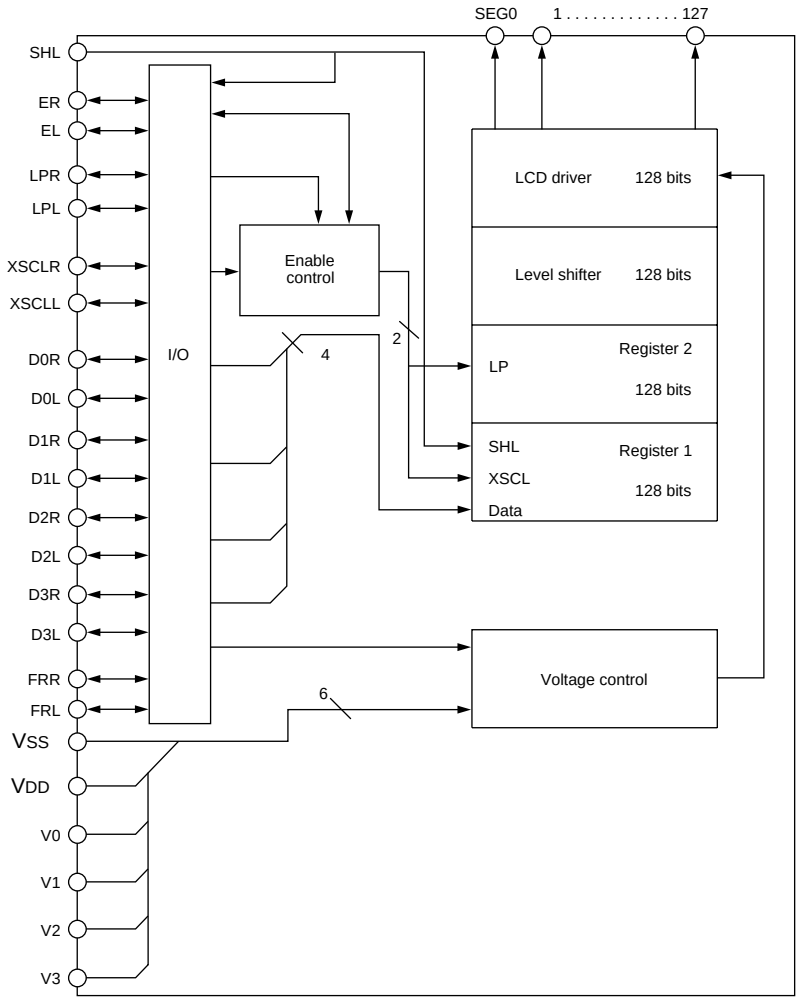
The driver is designed to work over a large range of LCD drive voltages and has its maximum drive voltage, V0 isolated from V_{DD} for flexibility of bias voltage generation.

The SED1620D0A does not require an enable clock to propagate a daisy chain driver enable leading to a simplified controller-driver interface.

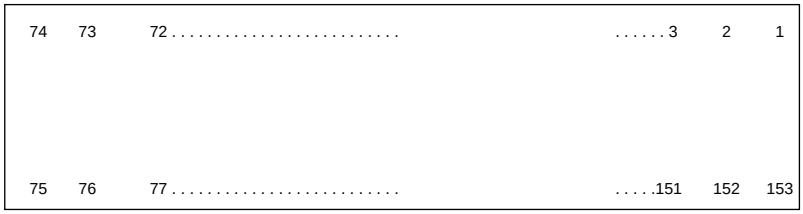
FEATURES

- 128 segment drive outputs
- Maximum configuration: 640×480 pixels when used with the SED1631D0A
- Wide range of LCD drive voltages: 12 to 28V
- 4-bit, 4 MHz a data bus
- Automatically propagates a daisy chain enable signal
- Selectable shift direction
- Flexible bias voltage generation
- Implemented in low power, Si-gate CMOS
- Single 5.0 V ±10 logic power supply
- Supplied in die form
- Pad layout suitable for single sided board assembly

BLOCK DIAGRAM



DIE OUTLINE



See page 4-13 for pad assignments.

BLOCK DESCRIPTION

Input/Output

The circuitry in this block configures the I/O lines as inputs or outputs as determined by the SHL input. See "PIN DESCRIPTION" and the table below.

Signal Name	SHL	
	H	L
xxR	O	I
xxL	I	O

Enable

The enable circuitry controls the state of the internal bus and clock as well as generating the daisy chain enable.

If the enable selected as the input by SHL is taken low the internal clock is held low and the SED1620D0A enters stand-by mode.

When the enable input is high and the enable circuitry detects that register 1 is full, it generates a daisy chain enable signal by outputting a high level signal from the enable output.

The enable input of the first driver in the chain must be tied to V_{DD}. The enable outputs of all drivers are reset by LP.

Register 1

Register 1 is a 32×4 bit, bi-directional shift register clocked by the input XSCL. The inputs and outputs of register 1, and its shift direction are selected by SCL.

Register 2

Register 2 is a 128 bit latch. Parallel data from register 1 is latched into register 2 on the falling edge of LP.

Level Shifter, voltage Controller and LCD Drivers

The level shifter generates the voltage levels required by the LCD driver circuitry from the data in register 2, using the voltages supplied by the voltage controller and the AC drive signal, FR. THe relationship between display data, FR and the segment drive voltages is shown below.

D0 • D3	FR	SEG
H	H	V0
	L	V5
L	H	V2
	L	V3

PIN DESCRIPTION

SEG0 to SEG127 LCD segment (column) drive outputs.

SHL I/O terminal configuration and register 1 shift direction select input.

SHL	D0R -D3R	D0L -D3L	XSCLR	XSCLL	LPR	LPL	ER	EL	FRR	FRL
H	O	I	O	I	O	I	O	I	O	I
L	I	O	I	O	I	O	I	O	I	O

SHL=H

SEG0-127	127	126	125	124	123	.....	4	3	2	1	0
Data	z	y	x	w	v	.....	e	d	c	b	a

SHL=L

SEG0-127	127	126	125	124	123	.....	4	3	2	1	0
Data	a	b	c	d	e	.....	v	w	x	y	z

D0x to D3x Display data input/output lines configured by SHL.

XSCLx Shift clock input/output lines configured by SHL.

LPx Display data latch pulse input/output lines configured by SHL.

Ex Enable input/output lines configured by SHL.

FRx LCD AC drive signal input/output lines configured by SHL.

V_{DD}, V_{SS} Logic power supply inputs.
V_{DD} = 0 V, V_{SS} = –5 V

V_0, V_2, V_3, V_5 LCD drive power supply inputs.
$V_{DD} \geq V_0 > V_2 > V_3 > V_5$
$-12 \geq V_5 \geq -28$ V

SPECIFICATIONS

Absolute Maximum Ratings

V_{DD} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to 0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_2, V_3	V_5–0.3 to 0.3	V
Input voltage	V_I	V_{SS}–0.3 to 0.3	V
Output voltage	V_O	V_{SS}–0.3 to 0.3	V
Output current	I_O	20	mA
Operating temperature	Topr	–20 to + 75	°C
Storing temperature 1	Tstg 1	–55 to +150	°C

Notes:

1. V_0, V_2 and V_3 must satisfy the condition
   $V_{DD} \geq V_0, V_2, V_3 \geq V_5$.
2. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.

Electrical Specifications

DC Characteristics

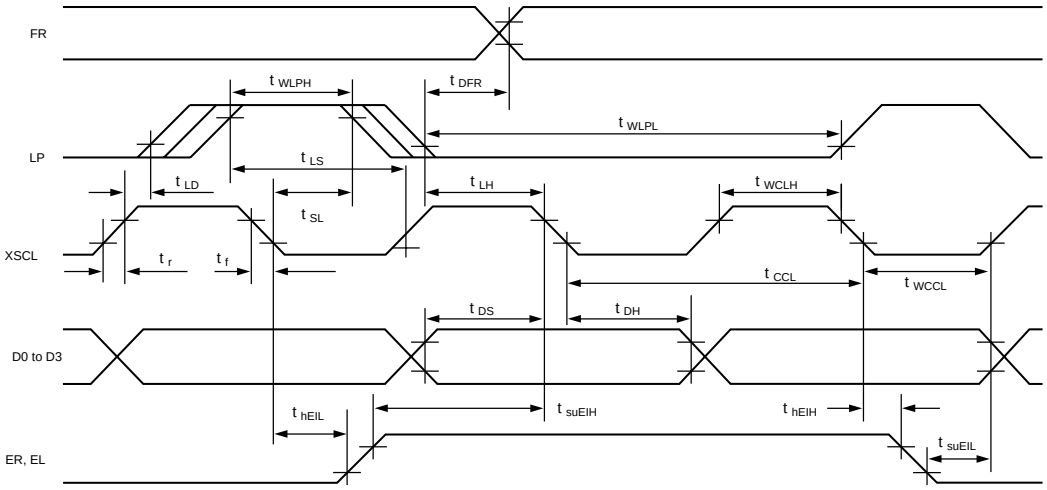
V_{DD} = V_0 = 0 V, V_{SS} = –5.0 V ± 10%, Ta = –20 to 75 °C

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
Operating voltage 1	V_{SS}	—		–5.5	–5.0	–4.5	V
Operating voltage 2	V_5	Recommended		–28.0	—	–12.0	V
		Operable		–28.0	—	–8.0	V
Operating voltage 3	V_0	—		–2.5	—	0	V
H input voltage	V_{IH}	All I/O terminals and SHL		0.2 V_{SS}	—	0	V
L input voltage	V_{IL}			—	—	0.8 V_{SS}	V
H output voltage	V_{OH}	ER, EL	I_{OH} = –0.6mA	–0.4	—	—	V
L output voltage	V_{OL}		I_{OL} = 0.6 mA	—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0$ V, SHL		—	—	2.0	µA
	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0$ V, all I/O terminals		—	—	5.0	µA
Segment output resistance	R_{SEG}	$\|\Delta V_{ON}\|$ = 0.5 V, V5 = –14.0 V		—	2.5	4.5	kΩ
Standby current (Current flows V_{DD})	I_{DDS}	V_5 = –12 to –28 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}		—	—	25	µA
Operating current 1 (Current flows V_{SS})	I_{SSO}	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{LP} = 7.7 kHz f_{XSCL} = 1.5 MHz, Frame period = 16.67 ms, Input-data inverted every bit, No load		—	180	400	µA
Operating current 2 (Current flows V_5)	I_{V5}	V_{SS} = –5.0 V, V_2 = –4.0 V V_3 = –16 V, V_5 = –20 V Other conditions are same as I_{SSO}		—	80	160	µA
Input capacitance	C_I	Ta = 25 °C	SHL	—	—	8.0	pF
	$C_{I/O}$		All I/O's	—	—	15.0	pF

Note: The device is guaranteed to function over this range however the output resistance of the segment driver is greater than that in the recommendeds voltage range. The ability to drive a selected panel under these conditions must be confirmed through test.

AC Characteristics

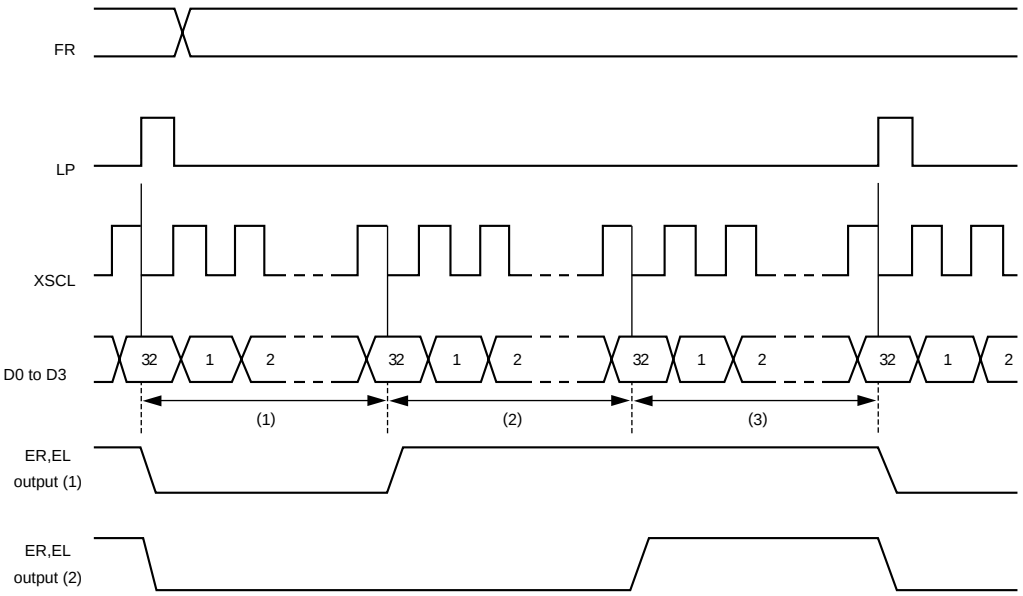
Input Timing



V_{IH}=0.2V_{SS}

V_{IL}=0.8V_{SS}

Typical Input Timing



Note: (1), (2) and (3) are cascaded drivers.

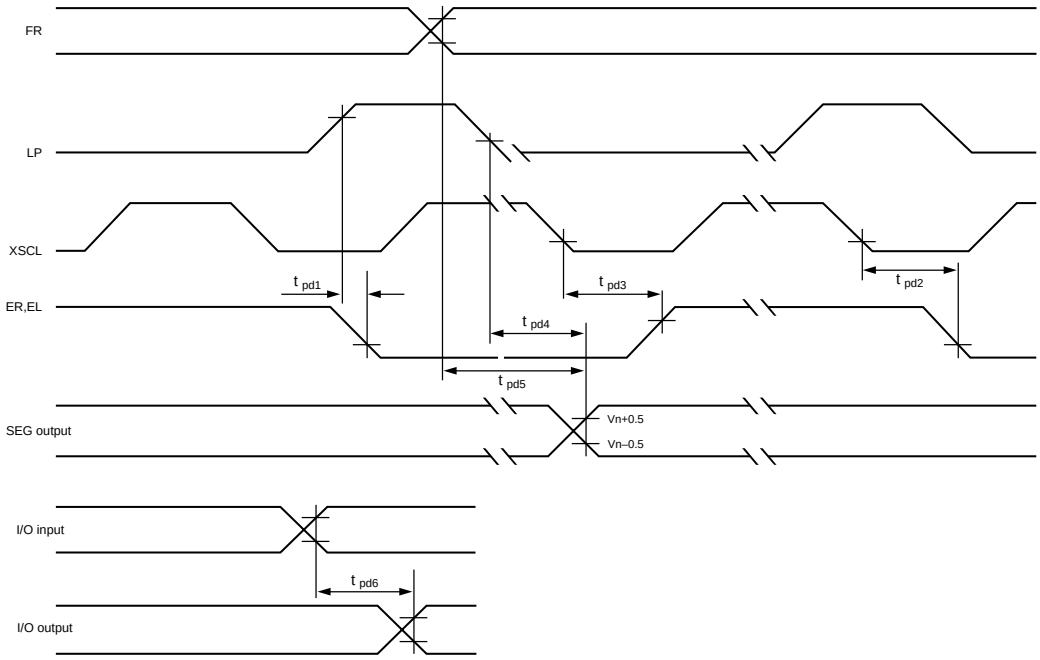
Ta = –20 to 75 °C, V_{SS} = –5.0 V ± 10%

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
XSCL period	t_{CCL}	t_r, $t_f \leq 25$ ns	250	—	—	ns
XSCL H pulsewidth	t_{WCLH}	—	100	—	—	ns
XSCL L pulsewidth	t_{WCLL}	—	100	—	—	ns
Data set up time	t_{DS}	—	80	—	—	ns
Data hold time	t_{DH}	—	60	—	—	ns
XSCL rise to LP rise time	t_{LD}	—	0	—	—	ns
XSCL fall to LP fall time	t_{SL}	—	100	—	—	ns
LP rise to XSCL rise time	t_{LS}	—	100	—	—	ns
LP fall to XSCL fall time	t_{LH}	—	100	—	—	ns
LP "H" pulse width	t_{WLPH}	—	100	—	—	ns
LP "L" pulse width	t_{WLPL}	—	260	—	—	ns
FR permissible delay time	t_{DFR}	—	–500	—	500	ns
Enable "H" set up time	t_{suEIH}	—	70	—	—	ns
Enable "H" hold time	t_{hEIH}	—	40	—	—	ns
Enable "L" set up time	t_{suEIL}	—	0	—	—	ns
Enable "L" hold time	t_{hEIL}	—	0	—	—	ns
Rise up time	t_r	—	—	—	150*	ns
Fall down time	t_f	—	—	—	150*	ns

* Note: The limits are set to reduce the chance of noise during signal transition causing incorrect operation.
For high speed operation

$$t_r, t_f < \frac{t_{CCL} - (t_{WCLH} + t_{WCLL})}{2}$$

Output Timing



$V_{OH}=V_{IH}=0.2V_{SS}$

$V_{OL}=V_{IL}=0.8V_{SS}$

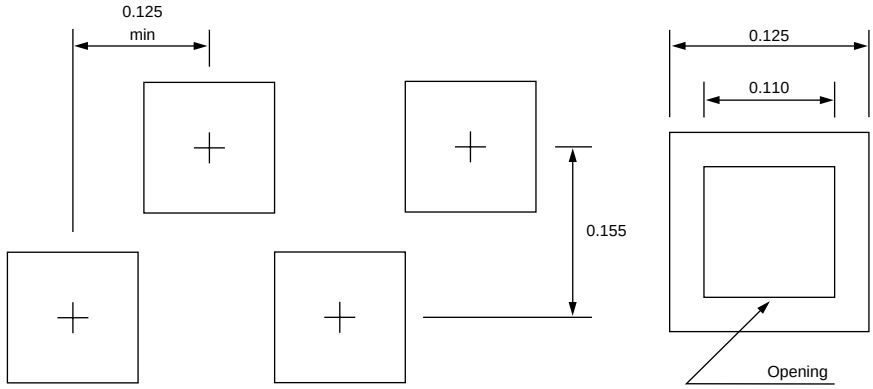
Ta = –20 to 75 °C, V_{SS} = –5.0 V ± 10%

Parameter	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
LP rise to disable time	t_{pd1}	C_L = 15 pF, XSCL = L	—	—	100	ns
XSCL fall to disable time	t_{pd2}	C_L = 15 pF, LP = H	—	—	100	ns
XSCL fall to enable time	t_{pd3}	C_L = 15 pF	—	—	100	ns
LP fall to SEG output time	t_{pd4}	V_5 = –12.0 to –28.0 V	—	—	4.5	ns
FR to SEG output delay time	t_{pd5}	C_L = 100 pf	—	—	4.5	ns
I/O to O/I delay time*	t_{pd6}	C_L = 15 pF	—	—	30	ns

* Note: Except for ER and EL.

Mechanical Specification

Pad Specification



Units: mm

Die Mark

D1620D0A (Aluminum pateern)

PAD ASSIGNMENT AND LOCATION

Unit (μm)

NO.	NAME	X	Y	NO.	NAME	X	Y	NO.	NAME	X	Y
1	NC	4893	1793	52	SEG 41	–2278	1793	103	SEG 92	–1523	–1793
2	V_{DD}	4138	1793	53	SEG 42	–2404	1638	104	SEG 93	–1397	–1638
3	EL	3886	1638	54	SEG 43	–2530	1793	105	SEG 94	–1272	–1793
4	D0L	3760	1793	55	SEG 44	–2655	1638	106	SEG 95	–1146	–1638
5	D1L	3635	1638	56	SEG 45	–2781	1793	107	SEG 96	–1020	–1793
6	D2L	3509	1793	57	SEG 46	–2907	1638	108	SEG 97	–894	–1638
7	D3L	3383	1638	58	SEG 47	–3033	1793	109	SEG 98	–768	–1793
8	FRL	3257	1793	59	SEG 48	–3159	1638	110	SEG 99	–643	–1638
9	LPL	3131	1638	60	SEG 49	–3284	1793	111	SEG 100	–517	–1793
10	XSCLL	3006	1793	61	SEG 50	–3410	1638	112	SEG 101	–391	–1638
11	SEG 0	2880	1638	62	SEG 51	–3536	1793	113	SEG 102	–265	–1793
12	SEG 1	2754	1793	63	SEG 52	–3662	1638	114	SEG 103	–136	–1638
13	SEG 2	2628	1638	64	SEG 53	–3788	1793	115	SEG 104	–14	–1793
14	SEG 3	2502	1793	65	SEG 54	–3913	1638	116	SEG 105	112	–1638
15	SEG 4	2377	1638	66	SEG 55	–4039	1793	117	SEG 106	238	–1793
16	SEG 5	2251	1793	67	SEG 56	–4165	1638	118	SEG 107	364	–1638
17	SEG 6	2125	1638	68	SEG 57	–4291	1793	119	SEG 108	490	–1793
18	SEG 7	1999	1793	69	SEG 58	–4417	1638	120	SEG 109	615	–1638
19	SEG 8	1873	1638	70	SEG 59	–4542	1793	121	SEG 110	741	–1793
20	SEG 9	1748	1793	71	SEG 60	–4668	1638	122	SEG 111	867	–1638
21	SEG 10	1622	1638	72	SEG 61	–4794	1793	123	SEG 112	993	–1793
22	SEG 11	1496	1793	73	SEG 62	–4920	1638	124	SEG 113	1119	–1638
23	SEG 12	1370	1638	74	SEG 63	–5046	1793	125	SEG 114	1244	–1793
24	SEG 13	1244	1793	75	SEG 64	–5046	–1793	126	SEG 115	1370	–1638
25	SEG 14	1119	1638	76	SEG 65	–4920	–1638	127	SEG 116	1496	–1793
26	SEG 15	993	1793	77	SEG 66	–4794	–1793	128	SEG 117	1622	–1638
27	SEG 16	867	1638	78	SEG 67	–4668	–1638	129	SEG 118	1748	–1793
28	SEG 17	741	1793	79	SEG 68	–4542	–1793	130	SEG 119	1873	–1638
29	SEG 18	615	1638	80	SEG 69	–4417	–1638	131	SEG 120	1999	–1793
30	SEG 19	490	1793	81	SEG 70	–4291	–1793	132	SEG 121	2125	–1638
31	SEG 20	364	1638	82	SEG 71	–4165	–1638	133	SEG 122	2251	–1793
32	SEG 21	238	1793	83	SEG 72	–4039	–1793	134	SEG 123	2377	–1638
33	SEG 22	112	1638	84	SEG 73	–3913	–1638	135	SEG 124	2502	–1793
34	SEG 23	–14	1793	85	SEG 74	–3788	–1793	136	SEG 125	2628	–1638
35	SEG 24	–139	1638	86	SEG 75	–3662	–1638	137	SEG 126	2754	–1793
36	SEG 25	–265	1793	87	SEG 76	–3536	–1793	138	SEG 127	2880	–1638
37	SEG 26	–391	1638	88	SEG 77	–3410	–1638	139	XSCLR	3006	–1793
38	SEG 27	–517	1793	89	SEG 78	–3284	–1793	140	LPR	3131	–1638
39	SEG 28	–643	1638	90	SEG 79	–3159	–1638	141	FPR	3257	–1793
40	SEG 29	–768	1793	91	SEG 80	–3033	–1793	142	D3R	3383	–1638
41	SEG 30	–894	1638	92	SEG 81	–2907	–1638	143	D2R	3509	–1793
42	SEG 31	–1020	1793	93	SEG 82	–2781	–1793	144	D1R	3635	–1638
43	SEG 32	–1146	1638	94	SEG 83	–2655	–1638	145	D0R	3760	–1793
44	SEG 33	–1272	1793	95	SEG 84	–2530	–1793	146	ER	3886	–1638
45	SEG 34	–1397	1638	96	SEG 85	–2404	–1638	147	V_{DD}	4138	–1793
46	SEG 35	–1523	1793	97	SEG 86	–2278	–1793	148	SHL	4264	–1638
47	SEG 36	–1649	1638	98	SEG 87	–2152	–1638	149	V_{SS}	4389	–1793
48	SEG 37	–1775	1793	99	SEG 88	–2026	–1793	150	V0	4515	–1638
49	SEG 38	–1901	1638	100	SEG 89	–1901	–1638	151	V2	4641	–1793
50	SEG 39	–2026	1793	101	SEG 90	–1775	–1793	152	V3	4767	–1638
51	SEG 40	–2152	1638	102	SEG 91	–1649	–1638	153	V5	4893	–1793

Note:

1. NC = Not Connected
2. 2 pads V_{DD} are supplied, and should be used to reduce the power souce impedance

APPLICATION NOTES

Generating LCD Drive Voltages

The LCD drive voltages need to be accurately and stably generated if a good quality display is to be achieved.

The easiest way to generate these voltages is to use a resistive divider network, however is should be notes that LCD panels present a significant capacitive load, resulting in high transient currents when the segment drive voltage are switched. It is good practice to put surge compensating capacitors in the divider network, but if the source resistance of the network is too high, distortion of the drive waveform will still result. In this case the only solution is to reduce the divider network source resistance.

Because low divider network source resistance increases the system current consumption, if you are designing with low power operation in mind, it is recommended that a voltage follower op-amp be used to generate the LCD drive voltages. The driver is designed so that V0 is isolated from V_{DD}, allowing op-amps to be used. Note that V_{DD} – V0 should be less than 2.5 V as a higher potential difference will degrade the LCD drive capability of the SED1620D0A. If a resistive divider network is used V_{DD} and V0 should be tied together.

System Power-up

If LCD drive level voltages are connected to the driver **BEFORE** the logic circuits are powered up, large currents will flow in the device, **DAMAGING** the chip.

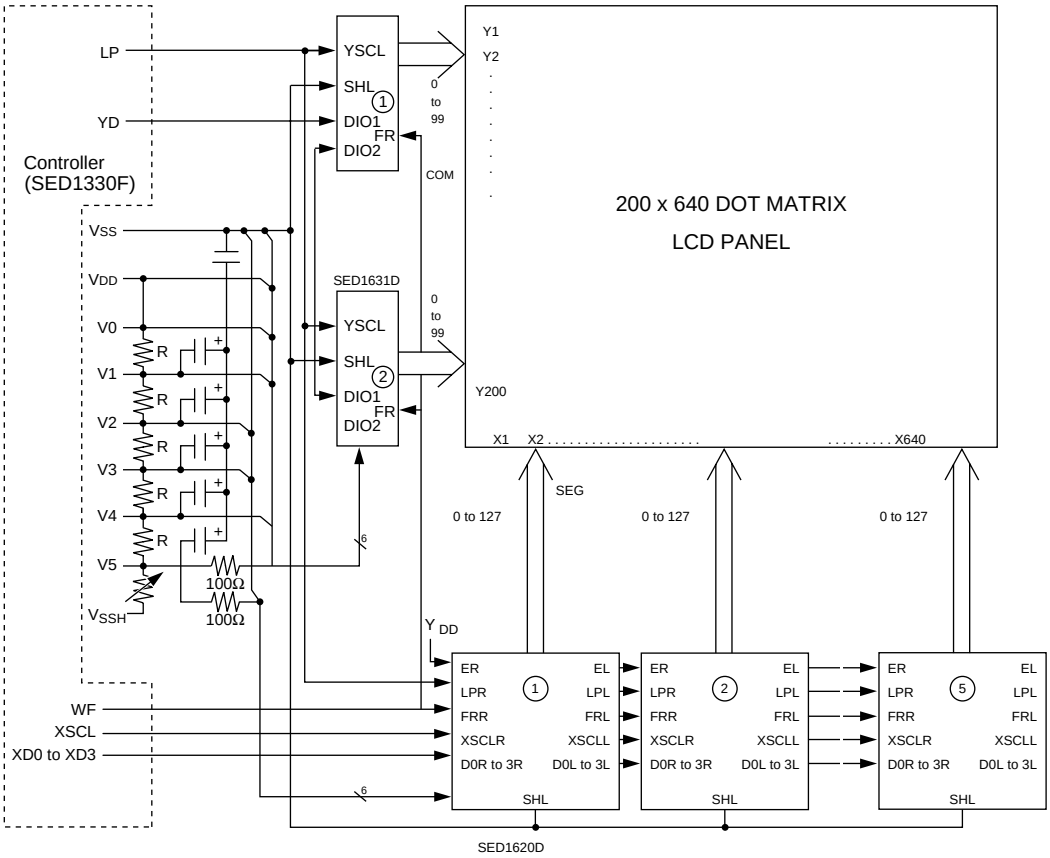
POWER ON: Logic power on before, or simulaneously with, LCD power on.

POWER OFF: LCD power off before, or simultaneously with, logic power off.

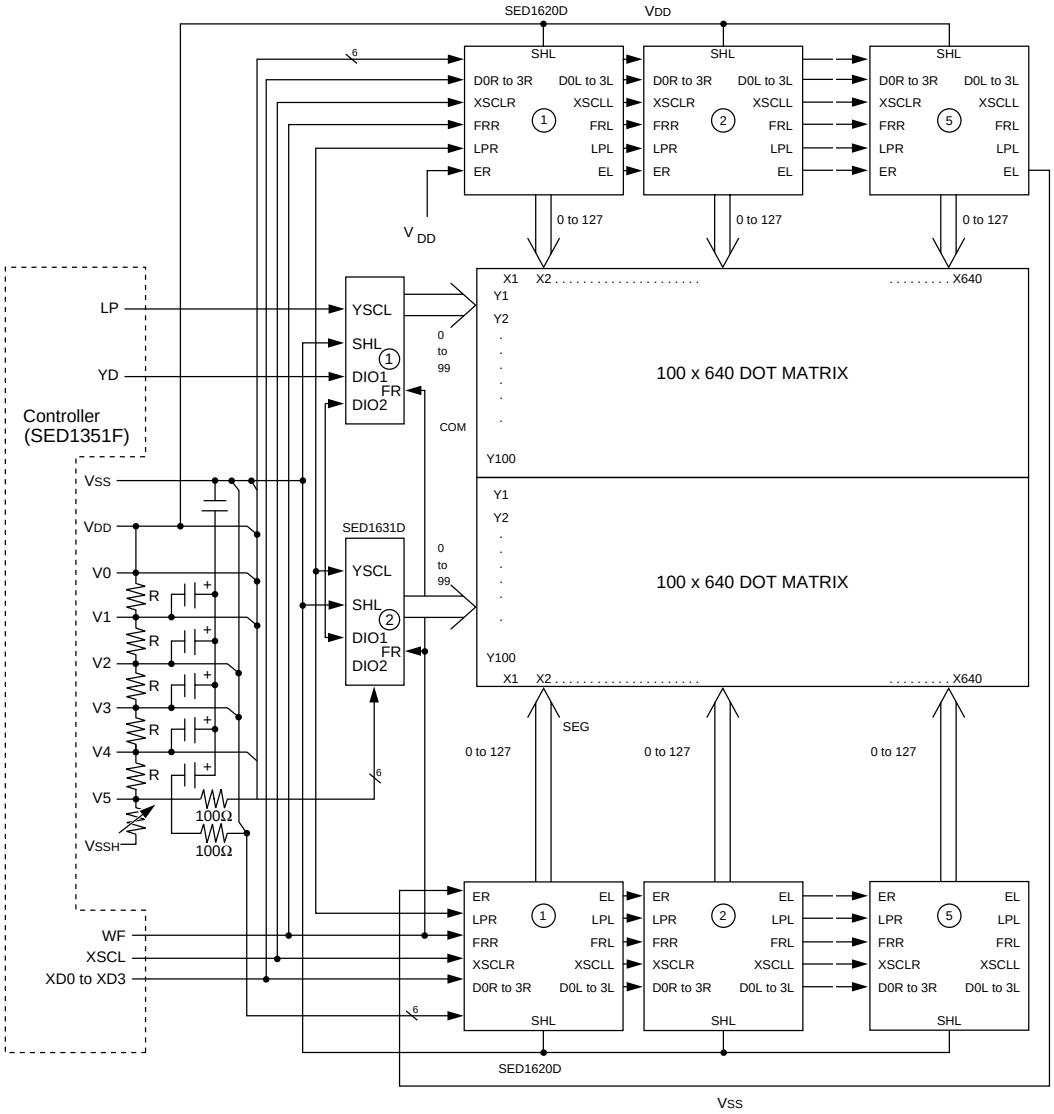
It is recommended that a current limiting resistor of about 100Ω is placed in series with V5. Also note the back of the die must be connected to V_{DD} or insulated.

Typical Application

200 x 640 Dot Matrix Display System



100 x 640 x 2 Dual Panel Drive



5. SED1640
LCD Driver

CONTENTS

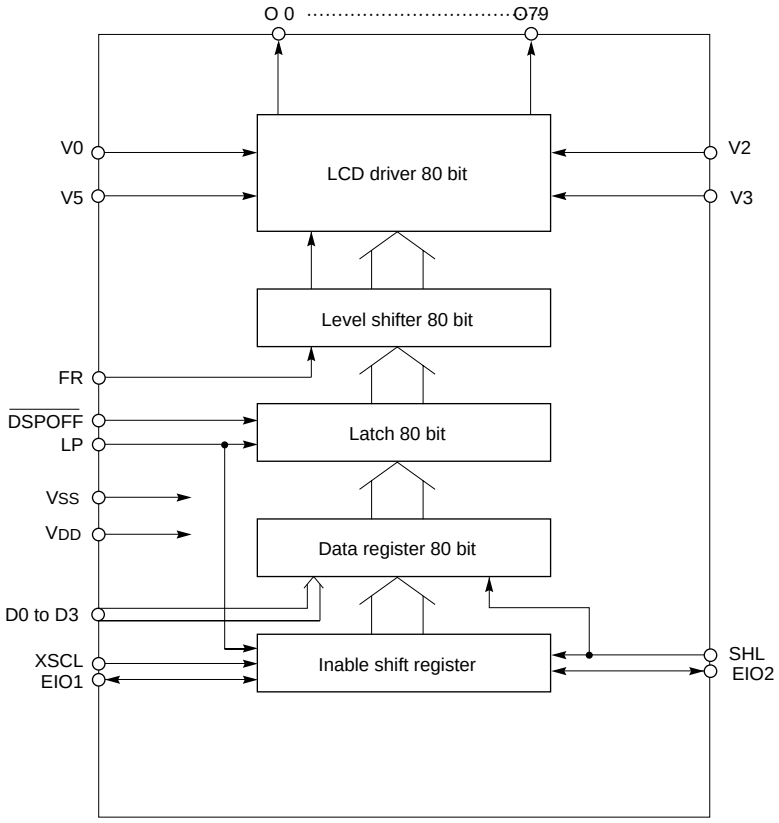
DESCRIPTION

The SED1640 is an 80 output segment (column) driver for use in combination with an SED1670/72.
It is provided with high-vision measure of the LCD display and adopts high speed inable chain system for low power operation and slim chip shape suitable for minimizing of the LCD panel. Also, low voltage operation of the logic power source suits a wide range of applications.

FEATURES

- LCD driver output number : 80
- Ultra-slim chip
- Low current consumption
- Low voltage operation : –2.7V max.
- Wide range of liquid crystal drive voltage : –8 to –28V
- High speed and low power data transfer is possible by adoption of the 4 bit bus inable chain system.
  Shift clock frequency
  6.5MHz (at –2.7V)
  7.5MHz (at –3.0V)
- Non-bias display off function
- Pin selection of the output shift direction is available.
- Offset bias regulation of the liquid crystal power is possible depending on the V_{DD} level.
- Logic system power source : –2.7V to –5.5V
- Product shapes
  Chip : SED1640D0B (Au bump article)
  Tab : SED1640T** (to be decided)

BLOCK DIAGRAM



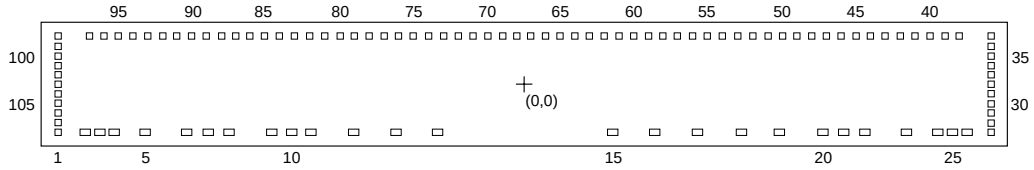
FUNCTIONS OF THE TERMINALS

<table>
<tr><th>Terminal names</th><th>I/O</th><th>Functions</th><th>Numbers of terminals</th></tr>
<tr><td>O0 ~ O79</td><td>O</td><td>LCD driving segment (column) output.
The output level varies by the trailing edge of the LP.</td><td>80</td></tr>
<tr><td>D0 ~ D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Inable input and output.
Set to input or output depending on the SHL input level.
The output is reset by the LP input and, after receiving 80 bit data, it automatically rises to “H”.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shifting direction choice and input/output controlling input to the EIO terminal.
When data are input to (D3, D2 ...D0) terminals in the order of (a,b,c,d,e,f,g,h).....(w,x,y,z), relations between data and segment outputs are as follows:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>. . .</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>. . .</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>OUtput</td></tr>
</table>
(Note) Relations between data and segment outputs are determined independent from the shift clock number.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Input of the alternating signal of the LCD drive output.</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power source</td><td>Power supply for the logics V_{DD} : 0V
V_{SS} : –2.7 ~ –5.5V</td><td>3</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power source</td><td>Power supply for the LCD driver circuit
V_{DD} : 0V V_5 : –8 ~ –28V
$V_{DD} \geqq V_0 \geqq V_2 \geqq 6/9\ V_5$
*1 $3/9\ V_5 \geqq V_3 \geqq V_5$</td><td>8</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>Forced blank input
At the “L” level, it forces the output to V0 level.
* When using this function, the unit may be used in common with SED1670∗/∗.</td><td>1</td></tr>
</table>

*1 Be sure to connect pairs of V0 - V5 to respective LCD power sources.

Total 107 (including NC5)

PAD LAYOUT



Chip size ..... 11.59mm x 1.40mm
Pad pitch ..... 105µm (Min.)
Chip thickness ..... 625µm ±25µm

Au bump specification (SED1640D0B) reference values

Bump size	A	160µm × 80µm ±4µm	(Pad No. 2 ~ 26)
Bump size	B	86µm × 91µm ±4µm	(Pad No. 1, 27, 37 and 98)
Bump size	C	86µm × 68µm ±4µm	(Pad No. 28 ~ 36 and 99 ~ 107)
Bump size	D	82µm × 74µm ±4µm	(Pad No. 38 ~ 97)
Bump height	A ~ D	22.5 ±5.5µm	(Pad No. 1 ~ 107)

PAD COORDINATES

PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates
2	V0	–5345	–541
3	V2	–5164	
4	V3	–4984	
5	V5	–4594	
6	V_{SS}	–4091	
7	Dummy	–3839	
8	SHL	–3587	
9	Dummy	–3065	
10	Dummy	–2828	
11	V_{DD}	–2590	
12	$\overline{DSPOFF}$	–2086	
13	FR	–1583	
14	LP	–1079	
15	XSCL	1079	
16	D0	1583	
17	D1	2086	
18	D2	2590	
19	Dummy	3065	
20	D3	3587	
21	Dummy	3839	
22	V_{SS}	4091	
23	V5	4594	
24	V3	4984	
25	V2	5164	
26	V0	5345	
27	EIO1	5644	–544
28	O0		–426
29	O1		–320
30	O2		–215
31	O3		–109
32	O4		–4
33	O5		102
34	O6		207
35	O7		313
36	O8		418
37	O9		546

PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates
38	O10	5269	553
39	O11	5090	
40	O12	4912	
41	O13	4733	
42	O14	4554	
43	O15	4376	
44	O16	4197	
45	O17	4019	
46	O18	3840	
47	O19	3661	
48	O20	3483	
49	O21	3304	
50	O22	3126	
51	O23	2947	
52	O24	2768	
53	O25	2590	
54	O26	2411	
55	O27	2233	
56	O28	2054	
57	O29	1875	
58	O30	1697	
59	O31	1518	
60	O32	1340	
61	O33	1161	
62	O34	982	
63	O35	804	
64	O36	625	
65	O37	447	
66	O38	268	
67	O39	89	
68	O40	–89	
69	O41	–268	
70	O42	–447	
71	O43	–625	
72	O44	–804	
73	O45	–982	

PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates
74	O46	–1161	553
75	O47	–1340	
76	O48	–1518	
77	O49	–1697	
78	O50	–1875	
79	O51	–2054	
80	O52	–2233	
81	O53	–2411	
82	O54	–2590	
83	O55	–2768	
84	O56	–2947	
85	O57	–3126	
86	O58	–3304	
87	O59	–3483	
88	O60	–3661	
89	O61	–3840	
90	O62	–4019	
91	O63	–4197	
92	O64	–4376	
93	O65	–4554	
94	O66	–4733	
95	O67	–4912	
96	O68	–5090	
97	O69	–5269	
98	O70	–5644	546
99	O71		418
100	O72		313
101	O73		207
102	O74		102
103	O75		–4
104	O76		–109
105	O77		–215
106	O78		–320
107	O79		–426
1	EIO2		–544

FUNCTIONS

Inable shift registor

The inable shift registor is a bidirectional shift registor wherewith the shift direction is determined by the SHL inputs and outputs of such shift registor are used to store data bus signals to the data registor. When inable signals are in the disable state, the internal clock signal and data bus are fixed to "L" to become the power save mode.
When using multiple units of the segment driver, EIO terminals of each driver should be connected by the cascade connection and the EIO terminals of the top end driver should be connected to "V_{DD}". (Refer to the example of the connection) Since the inable control circuit automatically detects when all the 80 bit data are taken in and automatically transfers the inable signal, control signals from a controlling LSI are not needed.

Data registor

This is a registor for serial and parallel conversion of data bus signals by means of the inable shift registor output. Consequently, the relations between the serial display data and segment outputs are determined independent from the shift clock input number.

Latch

It takes in the contents of the data registor by means of the trailing edge trigger of the LP to transmit the output to the level shifter.

Level shifter

This is a level interface circuit to convert the voltage level of signals from logic level to LCD driving level.

LCD driver

It outputs the LCD drive voltage.
Relations among data bus signals, alternating signals FR and the segment output voltage are given below.

$\overline{DSPOFF}$	Data bus signals	FR	O Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_0

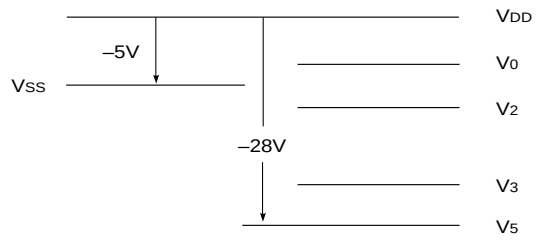
ABSOLUTE MAXIMUM RATING

Items	Symbols	Ratings	Unit
Power voltage (1)	V_{SS}	–7.0 ~ +0.3	V
Power voltage (2)	V_5	–30.0 ~ +0.3	V
Power voltage (3)	V_0, V_2, V_3	V_5–0.3 ~ V_{DD}+0.3	V
Input voltage	V_I	V_{SS}–0.3 ~ V_{DD}+0.3	V
Output voltage	V_O	V_{SS}–0.3 ~ V_{DD}+0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	Topr	–40 ~ +85	°C
Storing temperature 1	Tstg 1	–65 ~ +150	°C
Storing temperature 2	Tstg 2	–55 ~ +100	°C

Note 1) All the above voltage is based on V_{DD} = 0V.

Note 2) The storing temperature 1 specifies that of chips proper and the storing temperature 2 specifies that of TAB packages.

Note 3) Voltage of V_0, V_2 and V_3 should always be maintained under a condition of $V_{DD} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5$.



Note 4) When logic power becomes floating state or if V_{SS} = –2.6 or beyond while the LCD driver power source is being applied, the LSI may be permanently damaged and avoid such circumstances.
Pay extra attention to the power sequence at times of turning on and turning off the power supply.

ELECTRICAL CHARACTERISTICS

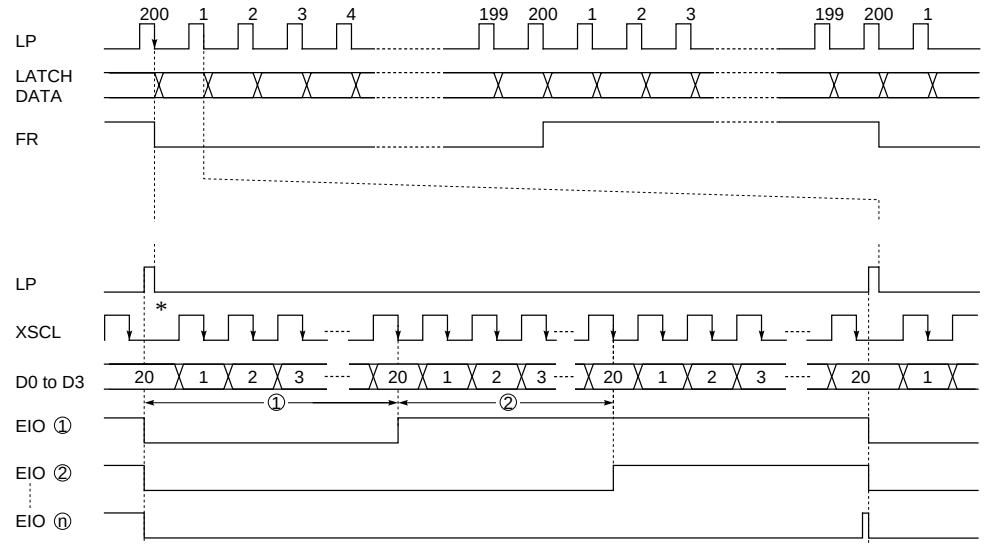
DC characteristics

Unless otherwise designated, V_{DD} = V0 = 0V, V_{SS} = –5.0V±10% and Ta = –40 to 85°C.

Items	Symbols	Conditions	Applicable terminals	Min.	Typ.	Max.	Unit
Power voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V_5	V_{SS}=–2.7 ~ –5.5V	V_5	–28.0		–12.0	V
Operatable voltage	V_5	Function	V_5			-8.0	V
Power voltage (2)	V_0	Recommended value	V_0	V_{DD}–2.5		V_{DD}	V
Power voltage (3)	V_2	Recommended value	V_2	3/9V_5			V
Power voltage (4)	V_3	Recommended value	V_3	V_5		6/9V_5	V
High level input voltage	V_{IH}	V_{SS}=–2.7 ~ –5.5V	EIO1, EIO2, FR, D0 ~ D3, XSCL, SHL, LP, $\overline{DSPOFF}$	0.2V_{SS}			V
Low level input voltage	V_{IL}					0.8V_{SS}	V
High level output	V_{OH}	V_{SS}=–2.7 ~ –5.5V, I_{OH}=–0.6mA	EIO1, EIO2	V_{DD}–0.4			V
Low level output voltage	V_{OL}	I_{OL}=0.6mA				V_{SS}+0.4	V
Input leak current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{DD}$	D0 ~ D3, LP, FR XSCL, SHL, $\overline{DSPOFF}$			2.0	µA
Input and output leak current	$I_{LI/O}$	$V_{SS} \leqq V_{IN} \leqq V_{DD}$	EIO1, EIO2			5.0	µA
Rest current	I_{SS}	V5=–28.0 ~ –14.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	V_{SS}			25	µA
Output resistance	R_{SEG}	ΔVON=0.5V V_5=–20.0V V_3=13/15•V5 V_2=2/15•V5 V_0=V_{DD}	O 0 ~ O 79		1.5	2.5	KΩ
Average operating current consumption (1)	I_{SS}	V_{SS}=–5.0V, V_{IH}=V_{DD} V_{IL}=V_{SS}, f_{XSCL}=2.69MHz f_{LP}=16.8KHz, f_{FR}=70Hz Input data: Diced display no-load	V_{SS}		0.10	0.2	mA
		V_{SS}=–3.0V Other conditions are the same as with V_{SS} =–5V			0.07	0.15	
Average operating current consumption (2)	I_5	V_{SS}=–5.0V, V_0=0.0V, V_2=–9.3V, V_3=–18.6V, V_5=–28.0V Other conditions are the same as with the item I_{SS}.	V5		0.02	0.05	mA
Input terminal capacity	C_I	Freq.=1MHz Ta=25°C Chips proper	D0 ~ D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$			8	pF
Input and output terminal capacity	$C_{I/O}$		EIO1, EIO2			15	pF

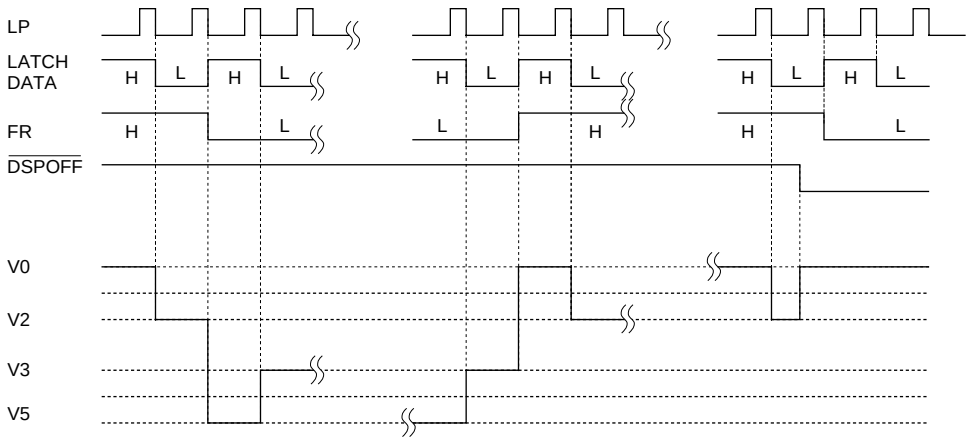
TIMING DIAGRAM

In case of 1/200 duty (an example)



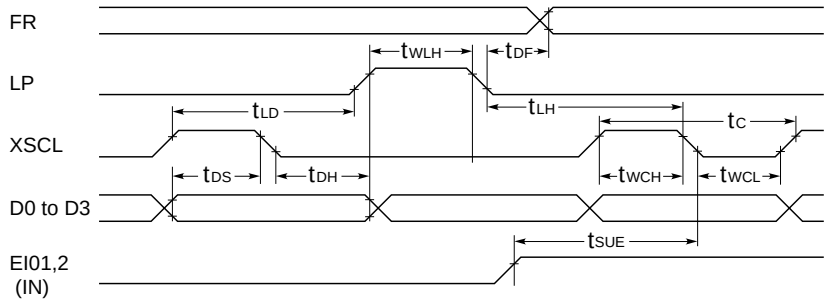
① ~ ⓝ indicate the cascade numbers of drivers.

* In case of high speed data transfer, it is necessary to secure a longer XSCL cycle in the timing of the LP pulse insertion in order to maintain the specified value of LP → XSCL (t_{LH}).



AC CHARACTERISTICS

Input timing characteristics



V_{SS}=–5.0V±0.5V, Ta=–40 ~ 85°C

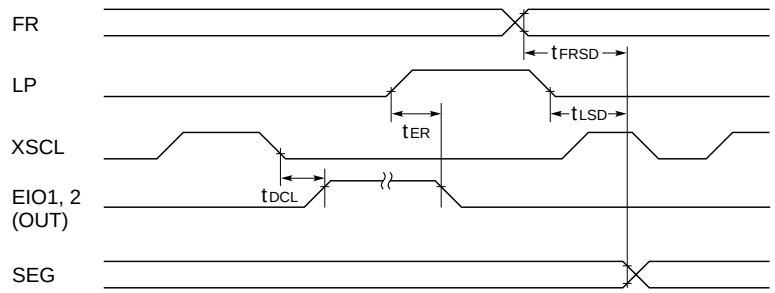
Items	Symbols	Conditions	Min.	Max.	Unit
XSCL cycle	t_C		100		ns
XSCL high level pulse duration	t_{WCH}		30		ns
XSCL low level pulse duration	t_{WCL}		30		ns
Data setup time	t_{DS}		30		ns
Data hold time	t_{DH}		20		ns
XSCL → LP rise time	t_{LD}		0		ns
LP → XSCL fall time	t_{LH}		40		ns
LP high level pulse duration	t_{WLH}	*3	40		ns
FR delay permissible time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}		35		ns

V_{SS}=–4.5V ~ 2.7V, Ta=–40 ~ 85°C

Items	Symbols	Conditions	Min.	Max.	Unit
XSCL cycle	t_C	V_{SS}=–2.7V *1	153		ns
		V_{SS}=–3.0V *2	133		
XSCL high level pulse duration	t_{WCH}		50		ns
XSCL low level pulse duration	t_{WCL}		50		ns
Data setup time	t_{DS}		50		ns
Data hold time	t_{DH}		30		ns
XSCL → LP rise time	t_{LD}		0		ns
LP → XSCL fall time	t_{LH}	V_{SS}=–2.7V	75		ns
		V_{SS}=–3.0V	65		
LP high level pulse duration	t_{WLH}	V_{SS}=–2.7V *3	75		ns
		V_{SS}=–3.0V *3	65		
FR delay permissible time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}	V_{SS}=–2.7V	50		ns
		V_{SS}=–3.0V	40		

*1 6.5MHz equivalence
*2 7.5MHz equivalence
*3 t_{WLH} specifies the time when LP is “H” and, at the same time, XSCL is “L”.

Output timing characteristics



V_{DD}=–5.0±0.5V, V5=–12.0 ~ –28.0V

Items	Symbols	Conditions	Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)		90	ns
EIO output delay time	t_{DCL}			55	ns
LP → SEG output delay time	t_{LSD}	C_L=100pF (0n)		200	ns
FR → SEG output delay time	t_{FRSD}			400	ns

V_{DD}=–4.5V ~ 2.7V, V5=–12.0 ~ –28.0V

Items	Symbols	Conditions		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)			150	ns
EIO output delay time	t_{DCL}		V_{SS}=–2.7V		95	ns
			V_{SS}=–3.0V		85	ns
LP → SEG output delay time	t_{LSD}	C_L=100pF (0n)			400	ns
FR → SEG output delay time	t_{FRSD}				800	ns

REGARDING THE LCD DRIVING POWER

Methods to obtain necessary voltage levels

In order to obtain necessary voltage levels for driving of the LCD, it should be the best to divide the potential between V5 V_{DD} resistively to drive by means of the voltage follower by the operation amplifier. In consideration of the case of using the operation amplifier, the maximum potential level V0 and V_{DD} should be separated to independent terminals.

Nevertheless, if V0 potential drops below the V_{DD} potential increasing the potential difference, the capacity of the LCD driver decreases and, therefore, it is suggested that the potential difference between V0 ~ V_{DD} be maintained within 0V ~ 2.5V. When the operation amplifier is not used, V0 and V_{DD} should be connected.

As shown in the example of the connection, when using the resistive divider, set the resistance as low as the power capacity of the system allows.

When a series resistance exist in the power line of V5 (V_{DD}), voltage drop of V5 (V_{DD}) at the LSI current end occurs by I5 at times of signal changes and it becomes unable to maintain the relations of the LCD with intermediate potentials ($V_{DD} \geqq V0 \geqq V2 \geqq V3 \geqq V5$) leading to breakage of the LSI. When installing protective resistors, it is necessary to stabilize the voltage by their capacity.

Cautions when turning the power on and off

Since the LCD drive system voltage with this LSI is comparatively high, when high voltage is applied to the LCD drive system leaving the logic power floating or leaving V_{SS} = –2.6V or over or if LCD drive signals are output before the applied voltage to the LCD drive system is stabilized, excess current may flow to break the LSI. It therefore is suggested to bring the potential of the LCD drive output to the V0 level until the LCD drive system voltage gets stabilized using the _____ display-off function ($\overline{DSPOFF}$).

When turning the power on or off, follow the sequence below.

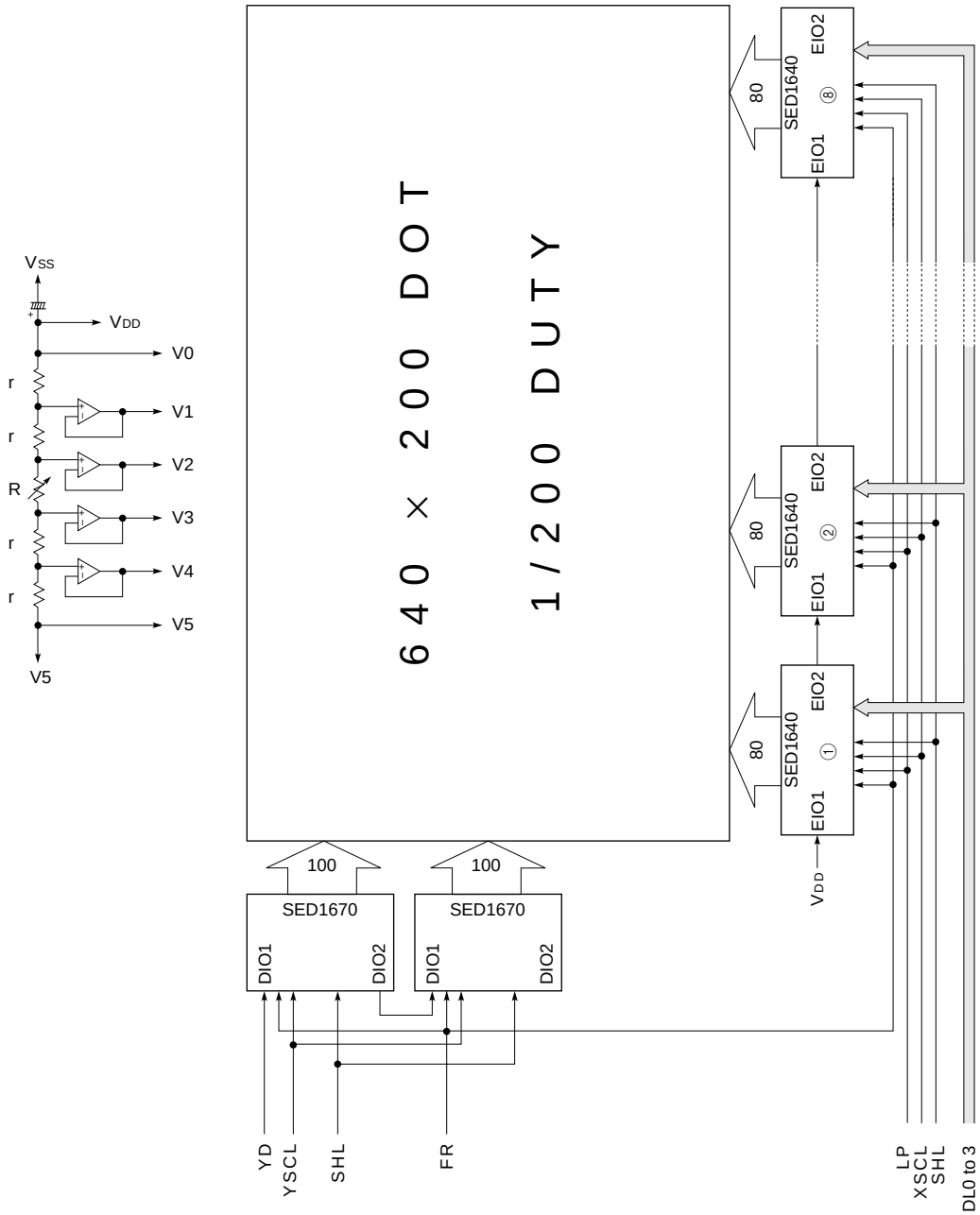
When turning on the power.....Logic systems ON → LCD drive system ON (or turn them on simultaneously).

When turning off the power.....LCD drive system OFF → Logic system OFF (or turn them off simultaneously).

Insert quick melting fuse in series to the LCD power source for prevention of an excess current flow. It is necessary to choose the optimum value for the protective resistance matching the capacity of the liquid crystal cells.

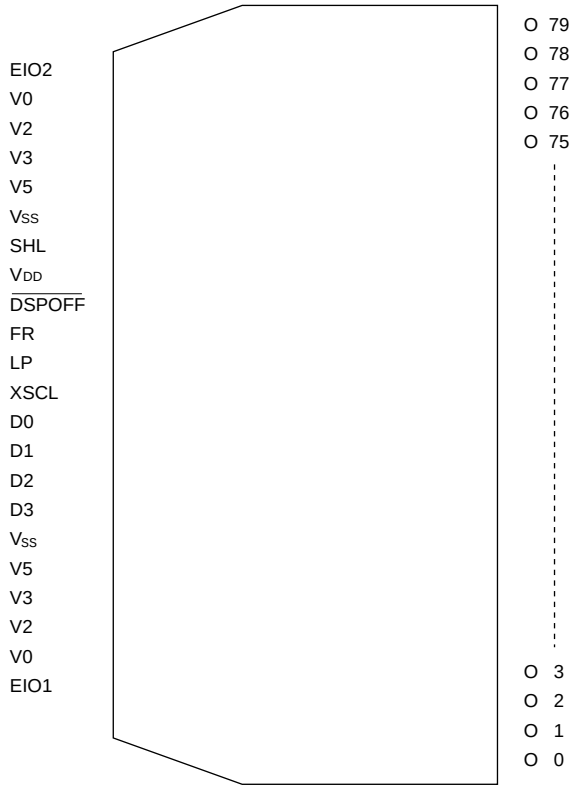
AN EXAMPLE OF CONNECTION

Block diagram of a large sized LCD



An example of TAB pin layout with SED1640T (Examination)

Note: This is not to specify the dimensions of the TAB.



6. SED1648
Dot Matrix LCD Segment Driver

CONTENTS

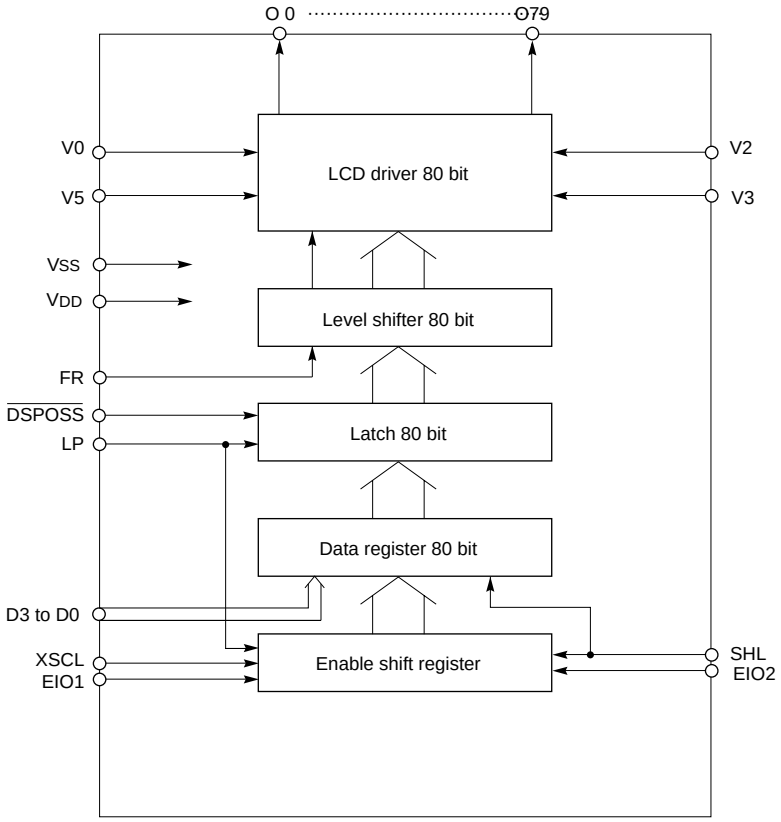
OVERVIEW

The SED1648 is an 80 output segment (column) driver which is suitable for driving a very high capacity dot-matrix LCD panels.
It is intended to be used in conjunction with the SED1651 as a pair.
The SED1648 is featured in a high quality of picture in LCD display. It employs a high-speed enable chain system which is favorable to a low-power driving. Allowed to be operated with a low voltage in the logic system power supply, it can meet a wide range of applications.

FEATURES

- Number of LCD drive output segments: 80
- Low current consumption
- Low voltage operation: –2.7 V (Max.)
- Wide range of LCD drive voltages* –8 V to –28 V
- High-speed and low-power data transfer enabled by means of a
- 4-bit bus and chain enable support
  Shift clock frequency+ 6.5 MHZ (at –2.7 V)
  10.0 MHZ (at –4.5 V)
- Selectable pin output shift direction
- Adjustable offset bias of LCD power to a V_{DD} level
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging SED1648D0A (AL-pad die form)
- No radial rays countermeasure taken in designing

BLOCK DIAGRAM



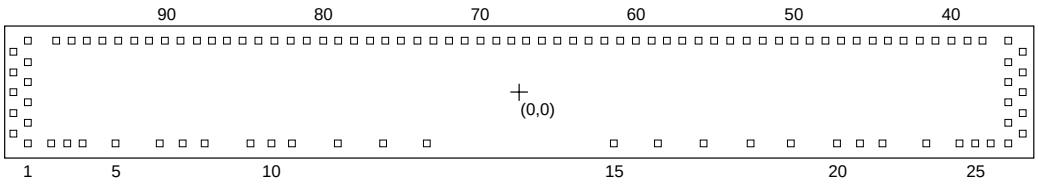
PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>O0 ~ O79</td><td>O</td><td>Segment (column) output for LCD driving
The output changes at the LP falling edge.</td><td>80</td></tr>
<tr><td>D0 ~ D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (Falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (Falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Enable input/output
To be set to input or output according to the SHL input level.
The output is reset by the LP input. Upon the end of fetching of 80-bit data, the system starts up automatically to “H”.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO pin I/O control input When data is input to (D3, D2 ... D0) pins sequentially in order of (a3, a2, a1, a0), (b3, b2, b1, b0) ... (t3, t2, t1, t0), the relationship between the data and segment output becomes as shown in the table below:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a3</td><td>a2</td><td>a1</td><td>. . .</td><td>t2</td><td>t1</td><td>t0</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>t0</td><td>t1</td><td>t2</td><td>. . .</td><td>a1</td><td>a2</td><td>a3</td><td>Input</td><td>Output</td></tr>
</table>
(Note) The relationship between the data and segment output is determined irrespective of the number of shift clock inputs.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output AC converted signal input</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V V_{SS}: –2.7 V to –5.5 V</td><td>3</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power supply</td><td>LCD drive circuit power supply
V_{DD}: 0 V V_5: –8 V to –28 V
$V_{DD} \geq V_0 \geq V_2 \geq 6/9\ V_5$
*1 $3/9\ V_5 \geq V_3 \geq V_5$</td><td>8</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>Forced blank input
Making the “L” output into V_0 level forcibly.</td><td>1</td></tr>
</table>

*1 Be sure to connect the V0 to V5 pair to their LCD power, respectively.

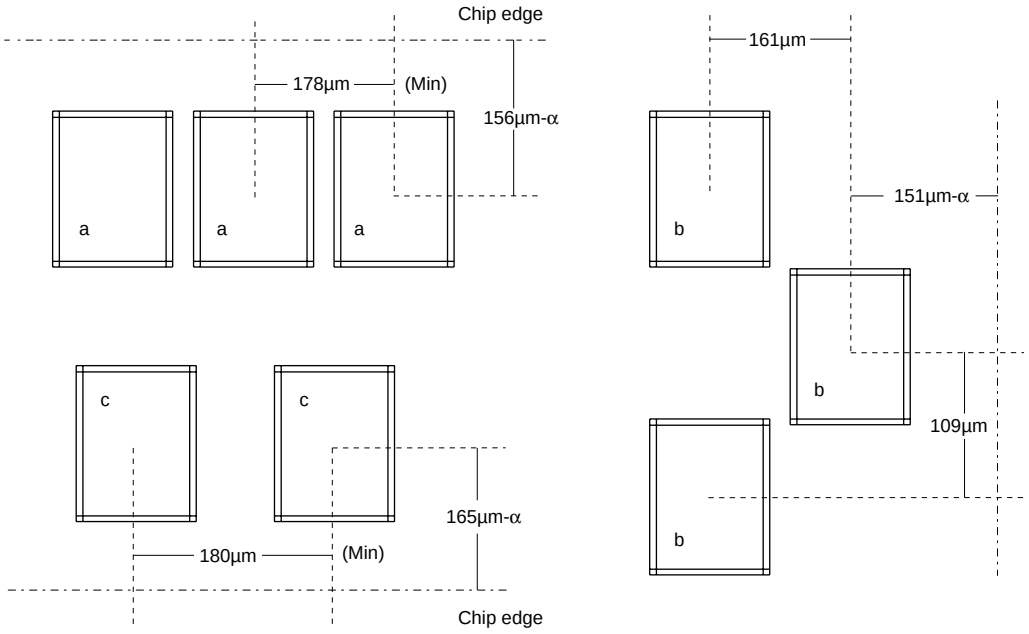
Total: 107 (including five NC’ s

PAD LAYOUT AND COORDINATES



Chip size: ..... 11.93 mm × 1.45 mm
Chip thickness: ..... 0.400 mm (Typ.)

1) Au pad specifications (SED16480D0A)



Pad	a	Opening (X, Y)	100 × 120µm	PAD No 38 to 97
Pad	b	Opening (X, Y)	110 × 110µm	PAD No 28 to 37, 98 to 107
Pad	c	Opening (X, Y)	110 × 110µm	PAD No 1 to 27

Unit (μm)

PAD		Actual dimensions	
NO.	NAME	X	Y
1	EIO2	–5653	–560
2	V0	–5297	–560
3	V2	–5117	–560
4	V3	–4936	–560
5	V5	–4547	–560
6	V_{SS}	–4091	–560
7	DUMMY	–3839	–560
8	SHL	–3587	–560
9	DUMMY	–3065	–560
10	DUMMY	–2828	–560
11	V_{DD}	–2590	–560
12	DSPOFF	–2086	–560
13	FR	–1583	–560
14	LP	–1079	–560
15	XSCL	1079	–560
16	D0	1583	–560
17	D1	2086	–560
18	D2	2590	–560
19	DUMMY	3065	–560
20	D3	3587	–560
21	DUMMY	3839	–560
22	V_{SS}	4091	–560
23	V5	4594	–560
24	V3	4984	–560
25	V2	5164	–560
26	V0	5345	–560
27	EIO1	5653	–560
28	O0	5814	–414
29	O1	5653	–305
30	O2	5814	–196
31	O3	5653	–86
32	O4	5814	23
33	O5	5653	132
34	O6	5814	241
35	O7	5653	351
36	O8	5814	460
37	O9	5653	569
38	O10	5268	569

PAD		Actual dimensions	
NO.	NAME	X	Y
39	O11	5090	569
40	O12	4911	569
41	O13	4732	569
42	O14	4554	569
43	O15	4375	569
44	O16	4197	569
45	O17	4018	569
46	O18	3839	569
47	O19	3661	569
48	O20	3482	569
49	O21	3304	569
50	O22	3125	569
51	O23	2946	569
52	O24	2768	569
53	O25	2589	569
54	O26	2411	569
55	O27	2232	569
56	O28	2053	569
57	O29	1875	569
58	O30	1696	569
59	O31	1518	569
60	O32	1339	569
61	O33	1160	569
62	O34	982	569
63	O35	803	569
64	O36	625	569
65	O37	446	569
66	O38	267	569
67	O39	89	569
68	O40	–89	569
69	O41	–267	569
70	O42	–446	569
71	O43	–625	569
72	O44	–803	569
73	O45	–982	569
74	O46	–1160	569
75	O47	–1339	569
76	O48	–1518	569

PAD		Actual dimensions	
NO.	NAME	X	Y
77	O49	–1696	569
78	O50	–1875	569
79	O51	–2053	569
80	O52	–2232	569
81	O53	–2411	569
82	O54	–2589	569
83	O55	–2768	569
84	O56	–2946	569
85	O57	–3125	569
86	O58	–3304	569
87	O59	–3482	569
88	O60	–3661	569
89	O61	–3839	569
90	O62	–4018	569
91	O63	–4197	569
92	O64	–4375	569
93	O65	–4554	569
94	O66	–4732	569
95	O67	–4911	569
96	O68	–5090	569
97	O69	–5268	569
98	O70	–5653	569
99	O71	–5814	460
100	O72	–5653	351
101	O73	–5814	241
102	O74	–5653	132
103	O75	–5814	23
104	O76	–5653	–86
105	O77	–5814	–195
106	O78	–5653	–305
107	O79	–5814	–414

FUNCTIONAL DESCRIPTION

Enable shift register

This is a bidirectional shift register with which the shift direction is selected by SHL input. The output of this shift register is used to store the data bus signals to data register.
When the enable signal is in the disable status, the internal clock signal and data bus are fixed to "L" and the system is made into the power save mode.
When using two or more segment drivers, connect the EIO pin of each driver in a cascade arrangement and the EIO pin of the leading driver to "V_{DD}". (See the connection example in 11.)
Since the enable controller circuit automatically detects that the data for 80 bits have been fetched thoroughly and then transfers the enable signal to the controller, it is not necessary to provide the control signal using the control LSI.

Data register

This is a register used to convert the data bus signal into serial or parallel signal through the enable shift register output. Consequently, the relationship between the serial display data and segment output is determined irrespective of the number of shift clock inputs.

Latch

This latch is used to fetch the content of data register at the LP falling edge trigger and to send its output to the level shifter.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

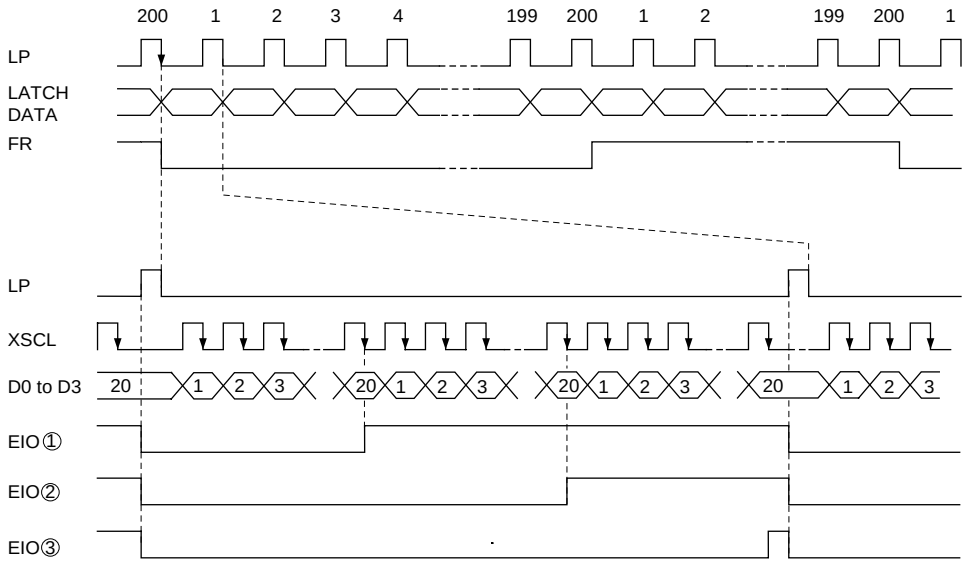
LCD driver

This driver outputs the LCD drive voltage.
The relationship among the data bus signal, AC converted signal FR and segment output voltage is as shown in the table below:

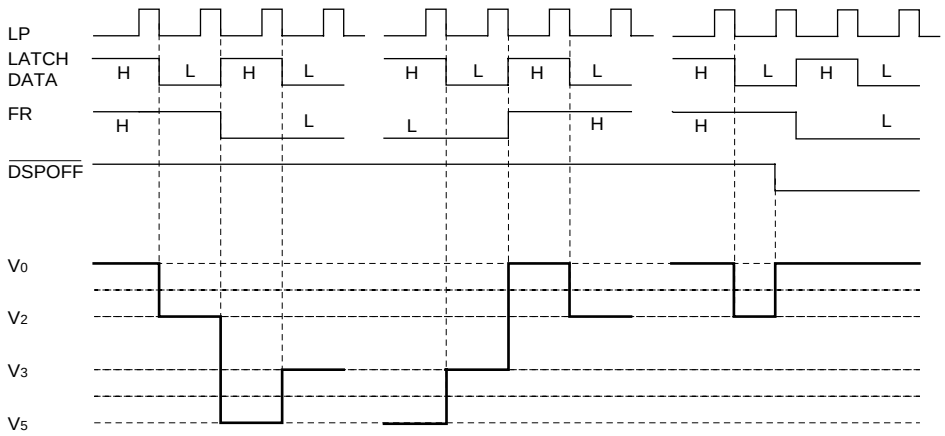
$\overline{DSPOFF}$	Data bus signal	FR	O output voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	–	–	V_0

TIMING CHART

When the duty is 1/200 (Reference Example)



① to ③ stand for a cascade No. of driver.

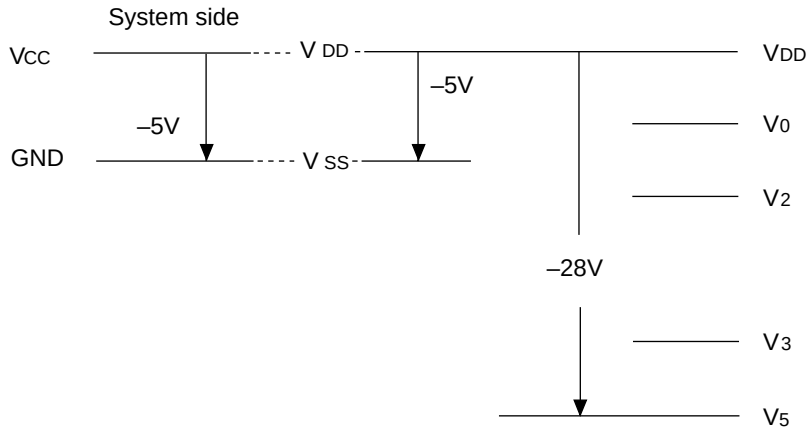


ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_2, V_3	V_5–0.3 to V_{DD}+0.3	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage	V_O	V_{SS}–0.3 to V_{DD}+0.3	V
EIO output current	I_O	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg 1	–65 to +150	°C

Notes:
1. The storage temperature 1 stipulates the temperature by unit of a chip.
2. The voltage of V_0, V_2 and V_3 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$.



3. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.

ELECTRICAL CHARACTERISTICS

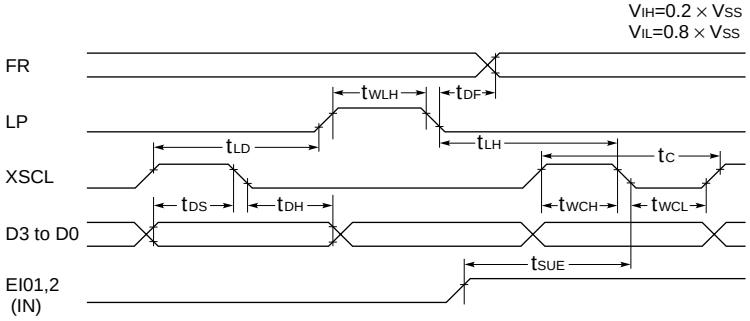
DC characteristics

Unless otherwise specified, $V_{DD} = V_0 = 0V$, $V_{SS} = -5.0V \pm 10\%$ and Ta = –40 to 85°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	V_{SS}=–2.7 to –5.5V	–28.0	–	–12.0	V	V_5
Operation enable voltage	V_5	Function	–	–	–8.0	V	V_5
Supply voltage (2)	V_0	Recommended value	V_{DD}–2.5	–	V_{DD}	V	V_0
Supply voltage (3)	V_2	Recommended value	3/9V_5	–	V_{DD}	V	V_2
Supply voltage (4)	V_3	Recommended value	V_5	–	6/9V_5	V	V_3
"H" input voltage	V_{IH}	V_{SS}=–2.7 to –5.5V	0.2V_{SS}	–	–	V	EIO1, EIO2, FR, D0 ~ D3, XSCL, SHL, LP, $\overline{DSPOFF}$
"L" input voltage	V_{IL}	V_{SS}=–2.7 to –5.5V	–	–	0.8V_{SS}	V	EIO1, EIO2, FR, D0 ~ D3, XSCL, SHL, LP, $\overline{DSPOFF}$
"H" output voltage	V_{OH}	V_{SS}=–2.7 to –5.5V, I_{OH}=–0.6mA	V_{DD}–0.4	–	–	V	EIO1, EIO2
"L" output voltage	V_{OL}	V_{SS}=–2.7 to –5.5V, I_{OL}=0.6mA	–	–	V_{SS}+0.4	V	EIO1, EIO2
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	–	–	2.0	µA	D0 to D3, LP, FR XSCL, SHL, $\overline{DSPOFF}$
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$	–	–	5.0	µA	EIO1, EIO2
Static current	I_{SS}	V_5=–28.0 to –14.0V $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	–	–	25	µA	V_{SS}
Output resistance	R_{SEG}	ΔV_{ON}=0.5V Ta=25°C V_5=–20.0V V_3=13/15·V_5 V_2=2/15·V_5 $V_0=V_{DD}$	–	1.5	1.9	KΩ	O0 to O79
Average operating current consumption (1)	I_{SS}	V_{SS}=–5.0V, $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$, f_{XSCL}=2.69MHz f_{LP}=16.8KHz, f_{FR}=70Hz Input data: Dice display at no load	–	0.10	0.2	mA	V_{SS}
		V_{SS}=–3.0V Other conditions are the same as V_{SS} = –5 V	–	0.07	0.15		
Average operating current consumption (2)	I_5	V_{SS}=–5.0V, V_0=0.0V, V_2=–9.3V V_3=–18.6V, V_5=–28.0V Other conditions are the same as in the item of ISS.	–	0.02	0.05	mA	V_5
Input pin capacitance	C_I	Freq.=1MHz Ta=25°C By unit of a chip	–	–	8	pF	D0 to D3, LP, FR XSCL, SHL, $\overline{DSPOFF}$
Input/output pin capacitance	$C_{I/O}$	Freq.=1MHz Ta=25°C By unit of a chip	–	–	15	pF	EIO1, EIO2

AC CHARACTERISTICS

Input timing characteristics



VSS=–5.0V±0.5V, Ta=–40 to 85°C

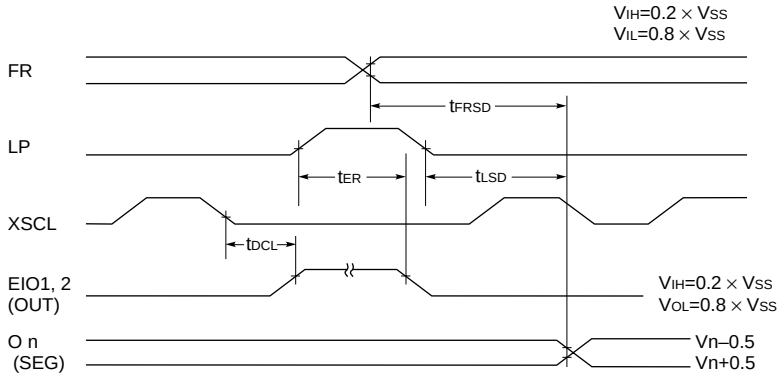
Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	t_C	–	100	–	ns
XSCL “H” pulsewidth	t_{WCH}	–	30	–	ns
XSCL “L” pulsewidth	t_{WCL}	–	30	–	ns
Data setup time	t_{DS}	–	20	–	ns
Data hold time	t_{DH}	–	10	–	ns
XSCL-rise to LP-rise time	t_{LD}	–	0	–	ns
LP-fall to XSCL-fall time	t_{LH}	–	40	–	ns
LP “H” pulsewidth	t_{WLH}	*3	40	–	ns
Allowable FR delay time	t_{DF}	–	–900	+900	ns
EIO setup time	t_{SUE}	–	35	–	ns

VSS=–4.5V to –2.7V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	t_C	VSS=–2.7V *1	153	–	ns
		VSS=–3.0V *2	133	–	
XSCL “H” pulsewidth	t_{WCH}	–	50	–	ns
XSCL “L” pulsewidth	t_{WCL}	–	50	–	ns
Data setup time	t_{DS}	–	30	–	ns
Data hold time	t_{DH}	–	15	–	ns
XSCL-rise to LP-rise time	t_{LD}	–	0	–	ns
LP-fall to XSCL-fall time	t_{LH}	VSS=–2.7V	75	–	ns
		VSS=–3.0V	65	–	
LP “H” pulsewidth	t_{WLH}	VSS=–2.7V *3	75	–	ns
		VSS=–3.0V *3	65	–	
Allowable FR delay time	t_{DF}	–	–900	+900	ns
EIO setup time	t_{SUE}	VSS=–2.7V	60	–	ns
		VSS=–3.0V	50	–	

*1 Equivalent to 6.5 MHz
*2 Equivalent to 7.5 MHz
*3 t_{WLH} stipulates the time when LP is “H” and XSCL is “L”.
*4 t_r and t_f of input signal are stipulated by unit of 20 ns.

Output timing characteristics



VDD=–5.0±0.5V, V5=–12.0 to –28.0V

Parament	Symbol	Condition	Min.	Max.	Unit
EIO reset time	t_{ER}	CL=15pF (EIO)	–	90	ns
EIO output delay time	t_{DCL}		–	55	ns
LP to SEG output delay time	t_{LSD}	CL=100pF (On)	–	200	ns
FR to SEG output delay time	t_{FRSD}		–	400	ns

VDD=–4.5V to 2.7V, V5=–12.0 to –28.0V

Parament	Symbols	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	CL=15pF (EIO)		–	150	ns
EIO output delay time	t_{DCL}		VSS=–2.7V	–	85	ns
			VSS=–3.0V	–	75	
LP to SEG output delay time	t_{LSD}	CL=100pF (On)		–	400	ns
FR to SEG output delay time	t_{FRSD}			–	800	ns

*1 t_r and t_f of input signal are stipulated by unit of 20 ns.

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is optimum to divide the resistance of potential between V_5 and V_{DD} to drive the LCD using the voltage follower with an operational amplifier. In taking into consideration of such a case using the operational amplifier, the maximum potential level V_0 for LCD driving has been made a separate pin from V_{DD}. When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD}.
When no operational amplifier is used, connect V_0 and V_{DD} close to the IC chip.

When a series resistance exists in the power supply line of V_5 and V_{DD}, a voltage drop of V_5 and V_{DD} occurs at the LSI power supply pin, the relationship with the LCD' s intermediate potential ($V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$) cannot be met, this causing the LSI to be broken down in some cases. When a protection resistor is inserted, it is necessary to stabilize the voltage by capacitance.

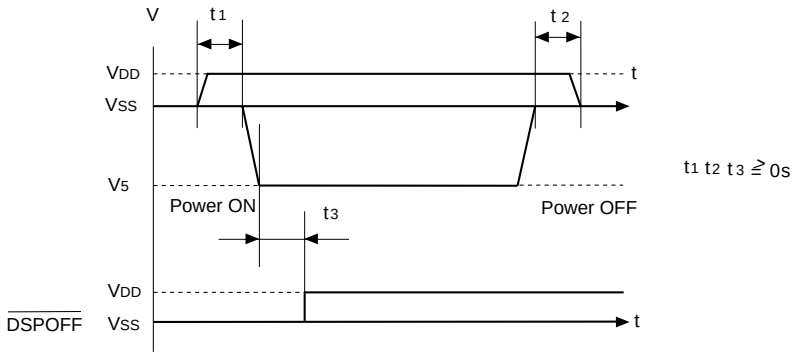
Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating or above V_{SS} =–2.6 V, and when the LCD driving signal is output before the applied voltage to the LCD driving system is stabilized, an overcurrent flows and LSI breaks down in some cases.
It is recommended to make the potential of LCD drive output into V_0 level using the display off function ($\overline{DSPOFF}$) until the LCD driving system voltage is stabilized.

Be sure to follow the power ON/OFF sequence as shown below:

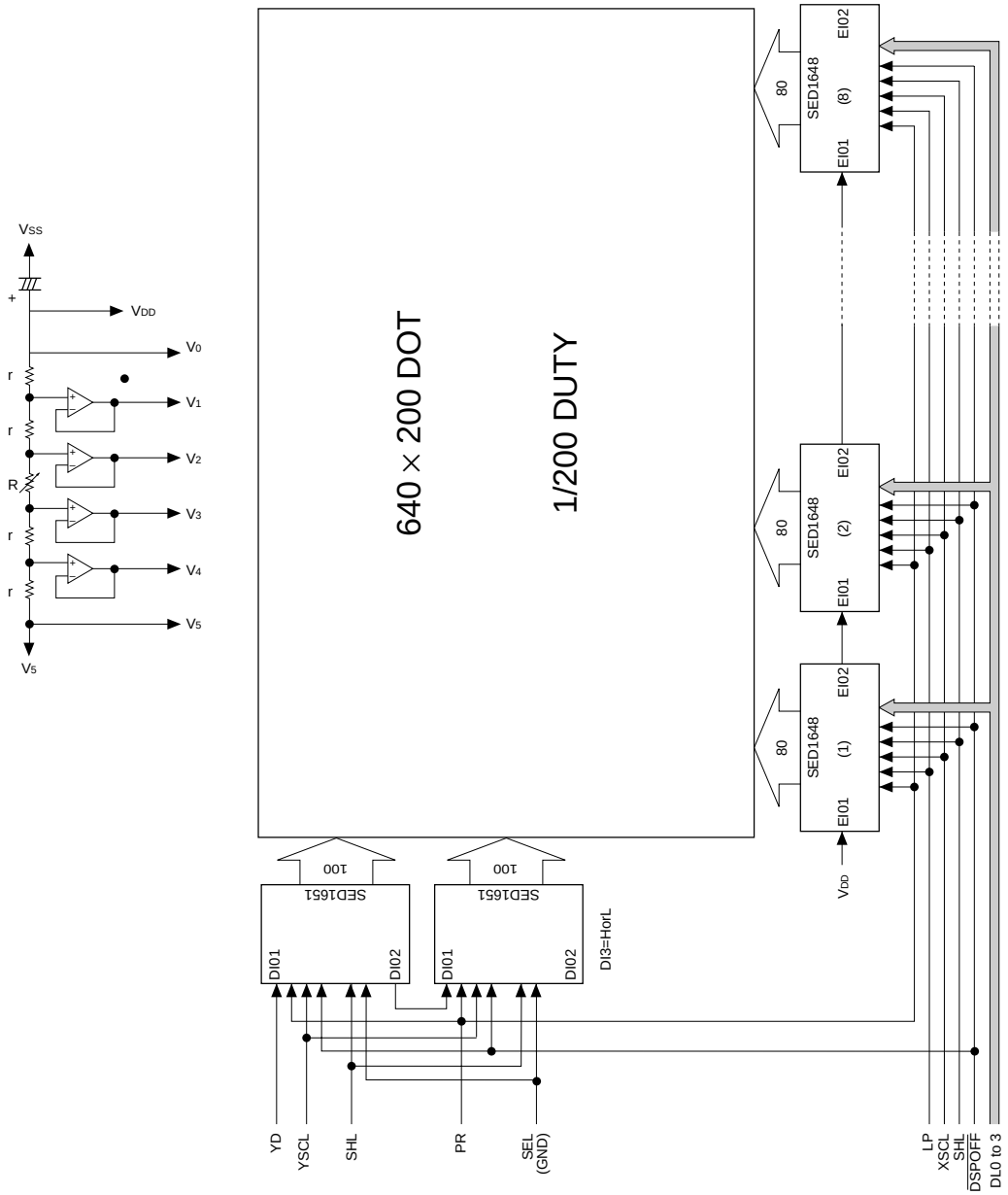
At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

For a countermeasure to such overcurrent, it is effective to put a high-speed melting fuse or protection resistor in series with the LCD power unit.
It is then required to select the optimum value in the protection resistance according to the capacitance of LC cell.



TYPICAL CIRCUIT DIAGRAM

Configuration Drawing of Large Screen LCD



7. SED1610FAA
Dot Matrix LCD Common Driver

CONTENTS

OVERVIEW

The SED1610FAA is an 86 output common (row) driver for driver for driving high capacity, high duty cycle dot matrix LCD displays. It is intended to be used with the SED1600FAA.

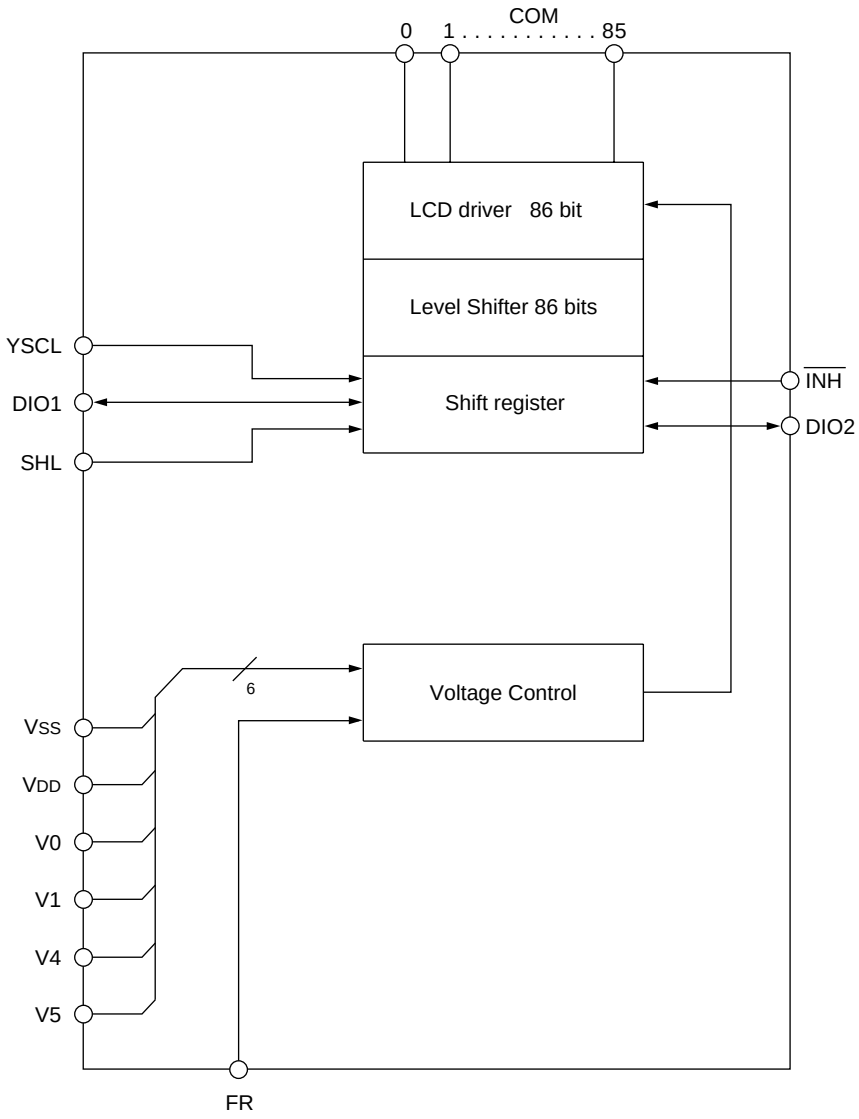
The SED1610FAA can operate with a wide range of LCD drive voltages. V0 is isolated from VDD allowing the use of op-amps for generating the LCD drive voltages.

This combination of features make the SED1610FAA a highly flexible driver suitable for a wide variety of LCD displays.

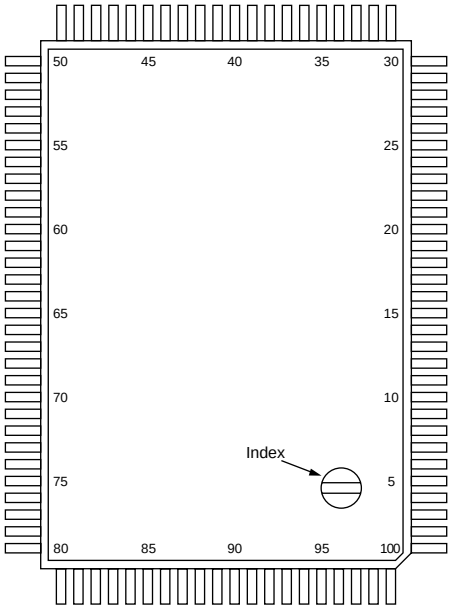
FEATURES

- 86 row drive outputs
- Maximum Configuration: 640×48 pixels when used with the SED1600FAA
- Wide range of LCD drive voltages: 12 to 28 V
- Selectable output shift direction
- Display blanking available
- Isolated V0
- Single 5.0V ±10% logic power supply
- Low power, Si-gate CMOS
- 100-pin QFP (Plastic)

BLOCK DIAGRAM



PACKAGE OUTLINE



PINOUT

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	COM2	26	COM27	51	COM51	76	COM76
2	COM3	27	COM28	52	COM52	77	COM77
3	COM4	28	COM29	53	COM53	78	COM78
4	COM5	29	COM30	54	COM54	79	COM79
5	COM6	30	COM31	55	COM55	80	COM80
6	COM7	31	COM32	56	COM56	81	COM81
7	COM8	32	COM33	57	COM57	82	COM82
8	COM9	33	COM34	58	COM58	83	COM83
9	COM10	34	COM35	59	COM59	84	COM84
10	COM11	35	COM36	60	COM60	85	COM85
11	COM12	36	COM37	61	COM61	86	DIO2
12	COM13	37	COM38	62	COM62	87	$\overline{INH}$
13	COM14	38	COM39	63	COM63	88	FR
14	COM15	39	COM40	64	COM64	89	YSCL
15	COM16	40	COM41	65	COM65	90	SHL
16	COM17	41	COM42	66	COM66	91	V_{DD}
17	COM18	42	COM43	67	COM67	92	V_{SS}
18	COM19	43	COM44	68	COM68	93	V0
19	COM20	44	COM45	69	COM69	94	V1
20	COM21	45	COM46	70	COM70	95	V4
21	COM22	46	COM47	71	COM71	96	V5
22	COM23	47	COM48	72	COM72	97	DIO1
23	COM24	48	COM49	73	COM73	98	COM0
24	COM25	49	COM50	74	COM74	99	COM1
25	COM26	50	NC	75	COM75	100	NC

BLOCK DESCRIPTION

Shift Register

This 86 bit bidirectional shift register is clocked by YSCL. The shift direction and serial input and output pins are selected by SHL (see section 2). The parallel output of this shift register is enabled by the $\overline{INH}$ input.

Normally a single “1”, supplied by the YD output of a controller, is shifted through the register to scan the common drive outputs.

Level Shifter, Voltage Control and LCD Driver

The level shifter converts TTL level voltages from the shift register to levels compatible with the LCD driver circuity using the $\overline{INH}$ and FR signal input and voltages from the voltage control circuitry. the common drive voltages generated are shown below.

$\overline{INH}$	Data	FR	COM Output	
H	H	H	V5	Pixel selected
		L	V0	
	L	H	V1	Pixel not selected
		L	V4	
L	Forced L	H	V1	Pixel not selected
		L	V4	

PIN DESCRIPTION

COM0 to COM85 LCD common driver outputs

$\overline{\text{INH}}$ Active low inhibit input. When $\overline{\text{INH}}$ is active, all common drive outputs go to "off", that is V4 when FR=0 and V1 when FR=1.

YSCL Shift clock input. Data is shifted into the driver on the falling edge of this clock.

SHL Shift direction and data input/output pin select input.

SHL	COM output shift direction	DIO	
		1	2
L	85 ← 0	Input	Output
H	85 → 0	Output	Input

DIO1, DIO2 Serial data input and output lines. The function of these lines is determined by SHL.

FR LCD AC drive signal input

V_{DD}, V_{SS} Logic power supply inputs

V0, V1, V4, V5 LCD drive voltage inputs

$V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to V_{DD}+0.3	V
Input pin voltage (1)	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Output pin voltage (1)	V_O	V_{SS}–0.3 to V_{DD}+0.3	V
Output pin current (1)	I_O	20	mA
Output pin current (2)	I_{OSEG}	20	mA
Operating temperature	Topr	–20 to +75	°C
Storage temperature 1	Tstg 1	–65 to +150	°C
Soldering temperature × time	Tsol	260, 10	°C, s
Allowable power dissipation	P_D	300	mW

Notes:

1. All voltages are referred to V_{DD} = 0V.
2. V0, V1, and V4 must satisfy the condition $V_{DD} \geq V0, V1, V4 \geq V5$.
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced during the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

ELECTRICAL SPECIFICATION

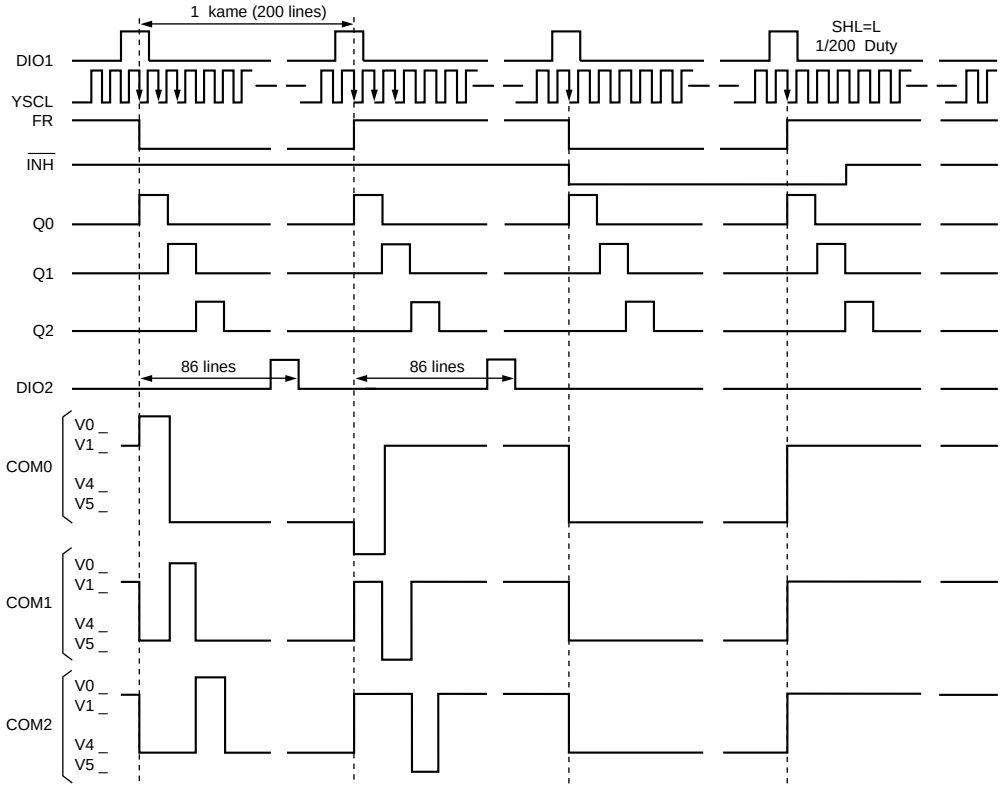
DC Characteristics

Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0V±10% and Ta = –20 to 75 °C

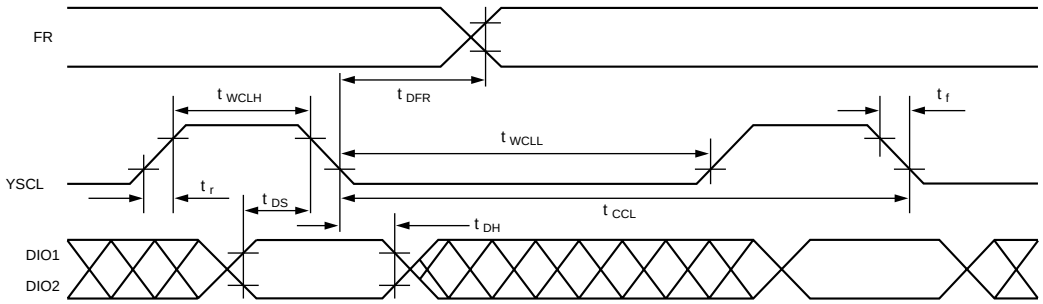
Parameter	Symbol	Condition			Rating			Unit	Pin
					Min.	Typ.	Max.		
Operating voltage (1)	—				–5.5	–5.0	–4.5	V	V_{SS}
Recommended operating voltage	—				–28.0		–12.0	V	V5
	—				–2.5	—	0	V	V0
	—				2/9xV5	—	V_{DD}	V	V1
	—				V5	—	7/9xV5	V	V4
"H" input voltage	V_{IH}				0.2V_{SS}			V	DIO1, DIO2, YSCL, FD, SHL, $\overline{INH}$
"L" input voltage	V_{IL}						0.8V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH} = –0.3 mA			–0.4			V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL} = 0.3 mA					V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$					2.0	µA	YSCL, SHL, $\overline{INH}$, FR
	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$					5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V5 = –12.0 to –28.0V V_{IH} = V_{DD}, V_{IL} = V_{SS}					25	µA	V_{DD}
Output resistance	R_{COM}	|ΔV_{ON}| =0.5V	Output level V1, V4	V5=–20.0V		0.40	0.80	kΩ	COM0-COM85
				V5=–14.0V		0.50	1.00		
				V5=–8.0V		0.60	1.20		
			Output level V0, V5	V5=–20.0V		0.60	1.20		
				V5=–14.0V		0.70	1.40		
				V5=–8.0V		0.90	1.80		
Supply current (1)	I_{SS1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12MHz Frame period = 16.67ms, Input data: "H" every 1/200 duty No-load				7	15.0	µA	V_{SS}
Supply current (2)	I_{SS2}	V_{SS} = –5.0V, V1 = –2.0V, V4 = –18.0V, V5 = –20.0V Other conditions are same as I_{SS1}.				7	15.0	µA	V5
Input pin capacitance	C_I	Ta = 25 °C					8.0	pF	YSCL, SHL, $\overline{INH}$, FR
	$C_{I/O}$						15.0	pF	DIO1, DIO2

AC Characteristics

Sample timing



Input timing



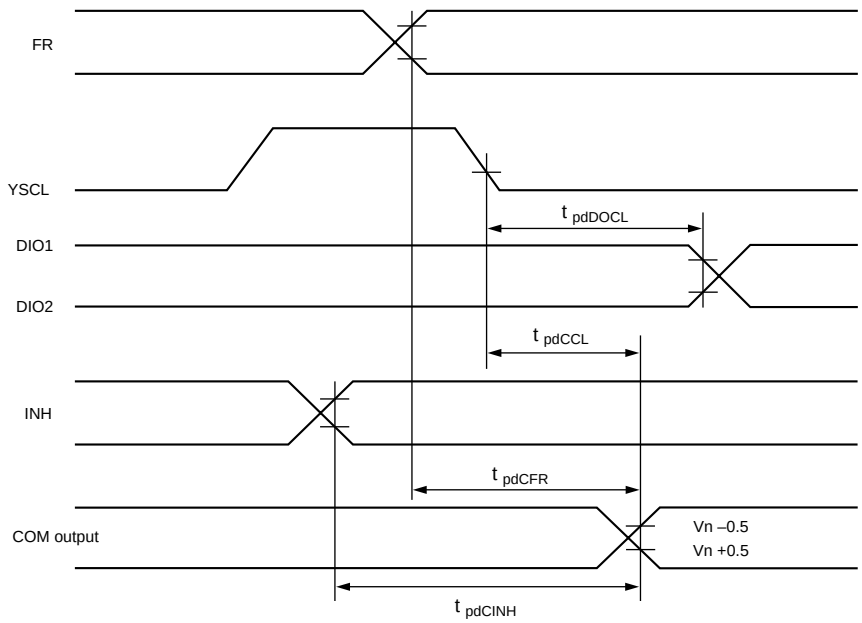
V_{IH}=0.2 x V_{SS}

V_{IL}=0.8 x V_{SS}

Ta = –20 to 75 °C, V_{SS} = –5.0V±10%

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL period	t_{CCL}		500		ns
YSCL "H" pulse width	t_{WCLH}		70		ns
YSCL "L" pulse width	t_{WCLL}		330		ns
Data setup time	t_{DS}		100		ns
Data hold time	t_{DH}		10		ns
Allowable FR delay time	t_{DFR}		–500	500	ns
Input signal rise time	t_r			50	ns
Input signal fall time	t_f			50	ns

Output Timing



$V_{IH}=V_{OH}=0.2 \times V_{SS}$

$V_{IL}=V_{OL}=0.8 \times V_{SS}$

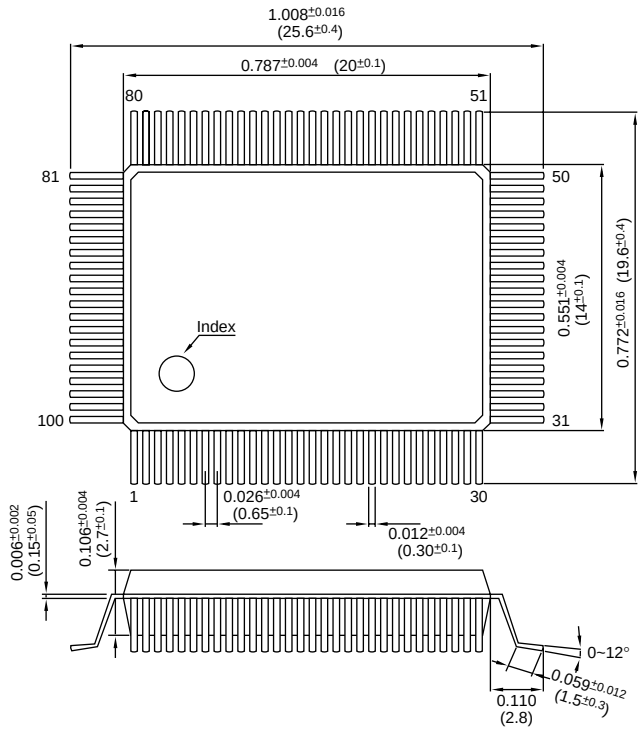
Ta = –20 to 75 °C, V_{SS} = –5.0V±10%

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
(YSCL-fall to DIO) delay time	t_{pdDOCL}	C_L = 15 pF	30	300	ns
(YSCL-fall to COM output) delay time	t_{pdCCL}	V5 = –12.0 to –28.0V C_L = 100 pF		30	µs
($\overline{INH}$ to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}			3.0	µs

Mechanical Specifications

SED1601F

Dimensions: inches(mm)



APPLICATION NOTES

Generating LCD Drive Voltages

The LCD drive voltages need to be accurately and stably generated if a good quality display is to be achieved.

The easiest way to generate these voltages is to use a resistive divider network, however is should be noted that LCD panels present a significant capacitive load, resulting in high transient currents when the segment drive voltages are switched. It is good practice to put surge compensating capacitors in the divider network, but if the source resistance of the network is too high, distortion of the drive waveform will still result. In this case the only solution is to reduce the divider network source resistance

Bacause low divider network source resistance increases the system current consumption, if you are disigning with low power operation in mind, it is recommended that a voltage follower op-amp be used to generate the LCD drive voltages. The driver is designed so that V0 is isolated from V_{DD}, allowing op-amps to be used. Note that V_{DD} –V0 should be less than 2.5V as a higher potential difference will degrade the LCD drive capability of the SED1610F. If a resistive divider network is used, V_{DD} and V0 should be tied together.

System Power-up

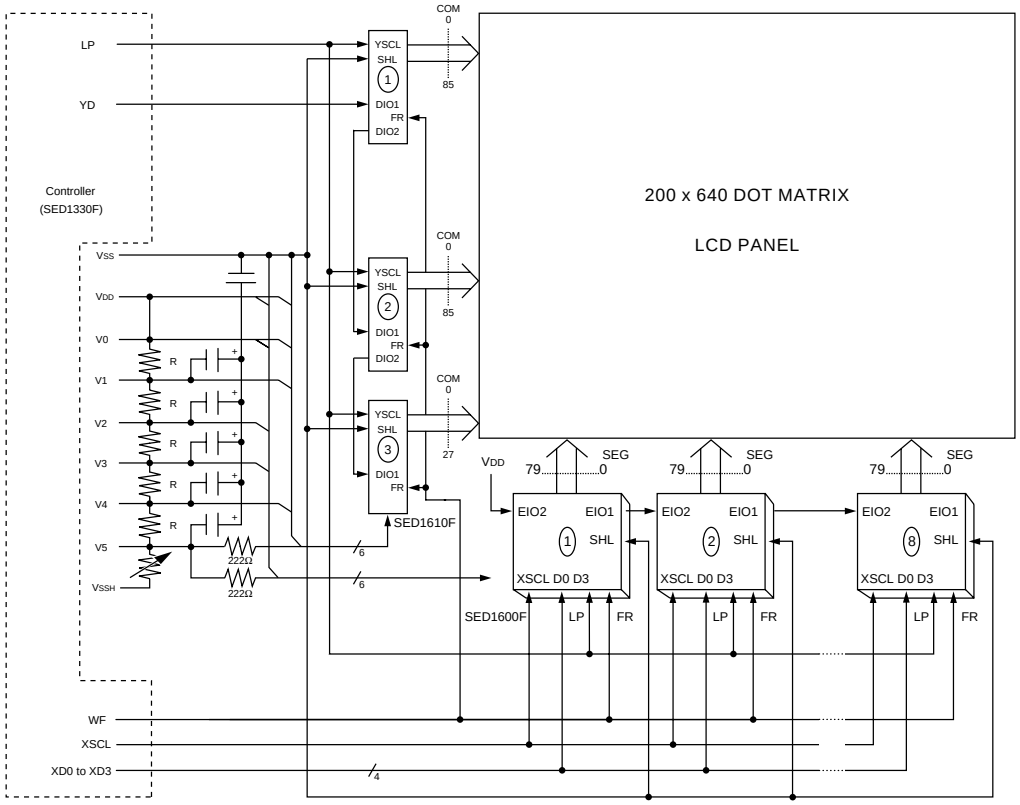
If LCD drive level voltages are connected to the driver **BEFORE** the logic circuits are powered up, large currents will flow in the device, **DAMAGING** the chip.

POWER ON: Logic power on before, or simultaneously with, LCD power on.

POWER OFF: LCD power off before, or simultaneously with, logic power off.

It is recommended that a current limiting resistor of 22Ω, or larger, is placed in series with V5.

Typical Application



8. SED1651
Dot Matrix LCD Common Driver

CONTENTS

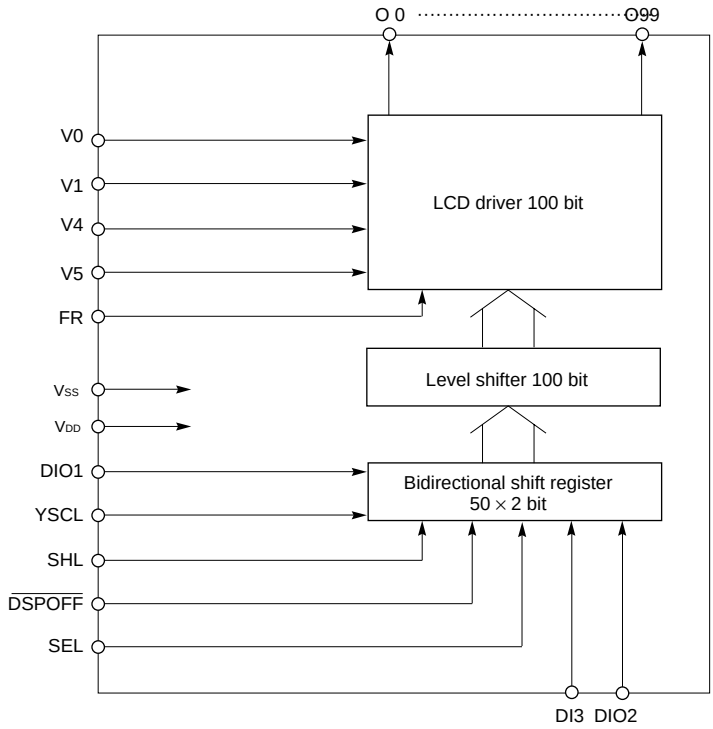
OVERVIEW

The SED1651 is a 100 output low-power resistance common)row) driver which is suitable for driving a very high capacity dotmatrix LCD panels. It is intended to be used in conjunction with the SED1648 as a pair.
Since the SED1651 is so designed to drive LCD's over a wide range of voltages, and also the maximum potential V_0 of its LCD driving bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel.

FEATURES

- Number of LCD drive output segments: 100
- Super slim chip configuration
- Common output ON resistance: 750Ω (Typ.)
- Display capacity ... Possible to display 640 × 480 dots.
- Selectable pin output shift direction
- No bias display OFF function
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –8 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging SED1651D$_{0A}$ (AL-pad die form)
- No radial rays countermeasure taken in designing

BLOCK DIAGRAM

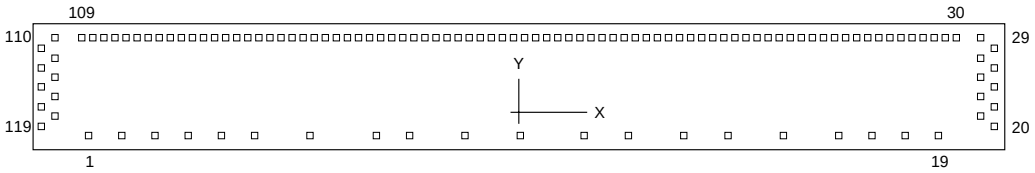


PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>O0 to O99</td><td>O</td><td>LCD drive common (row) output
The output changes at the YSCL falling edge.</td><td>80</td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>50 × 2 bits bidirectional shift register serial data input/output
To be set to input or output according to the SHL input
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>This is the input pin of scanning pulse in the 50 × 2 bits configuration.
When SEL = L, the DI3 pin to V_{SS} or GND.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Selection input of bidirectional shift register operating mode
H ... 50 × 2 (DI3 input) L ... 100</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input
The scanning data is shifted at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO pin I/O control input
<table>
<tr><th>SHL</th><th>O output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 → 49 50 → 99</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>99 → 50 49 → 0</td><td>Ourput</td><td>Input</td></tr>
</table>
When SEL = “H”, the DI3 input is set to O50 (SHL = “L”) or O49 (SHL = “H”).
When SEL = “L”, the D13 input is ignored and the DIO inputs are shifted continuously.</td><td>1</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>LCD display blanking control input
When “L” is input, the content of shift register is cleared and all common outputs become the V_0 level instantaneously.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output converted signal input</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V (GND) V_{SS}: –2.7 V to –5.5 V</td><td>3</td></tr>
<tr><td>V0, V1,
V4, V5</td><td>Power supply</td><td>LCD drive power supply V_5: –8 V to –28 V
$V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$</td><td>8</td></tr>
</table>

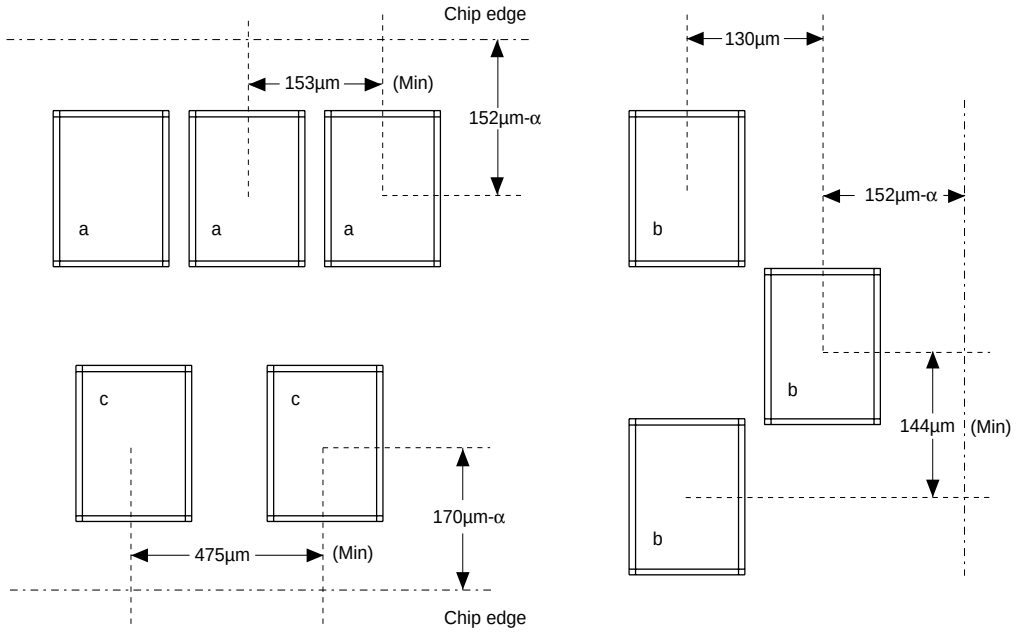
Respectively
Total: 119

PAD LAYOUT AND COORDINATES



Chip size: ..... 13.43 mm × 1.76 mm
Chip thickness: ..... 400 µm (Typ.)

1) AL pad specifications (SED1651D0A)



Pad	a	Opening (X, Y)	110 × 110µm	PAD No 30 to 109
Pad	b	Opening (X, Y)	110 × 110µm	PAD No 20 to 29, 110 to 119
Pad	c	Opening (X, Y)	110 × 110µm	PAD No 1 to 19

Unit (μm)

PAD		Actual dimensions	
NO.	NAME	X	Y
1	DIO2	–5985	–709
2	V0	–5510	
3	V1	–5035	
4	V4	–4560	
5	V5	–4038	
6	V_{SS}	–3164	
7	SEL	–2280	
8	SHL	–1767	
9	DI3	–1064	
10	YSCL	–181	
11	V_{DD}	770	
12	$\overline{\text{DSPOFF}}$	1283	
13	FR	2176	
14	V_{SS}	2879	
15	V5	3753	
16	V4	4560	
17	V1	5035	
18	V0	5510	
19	DIO1	5985	
20	O0	6560	–610
21	O1	6430	–466
22	O2	6560	–321
23	O3	6430	–177
24	O4	6560	–32
25	O5	6430	112
26	O6	6560	257
27	O7	6430	401
28	O8	6560	545
29	O9	6430	690
30	O10	6079	727
31	O11	5925	
32	O12	5771	
33	O13	5617	
34	O14	5463	
35	O15	5310	
36	O16	5156	
37	O17	5002	
38	O18	4848	
39	O19	4694	
40	O20	4540	
41	O21	4386	
42	O22	4232	

PAD		Actual dimensions	
NO.	NAME	X	Y
43	O23	4078	727
44	O24	3924	
45	O25	3771	
46	O26	3617	
47	O27	3463	
48	O28	3309	
49	O29	3155	
50	O30	3001	
51	O31	2847	
52	O32	2693	
53	O33	2539	
54	O34	2385	
55	O35	2232	
56	O36	2078	
57	O37	1924	
58	O38	1770	
59	O39	1616	
60	O40	1462	
61	O41	1308	
62	O42	1154	
63	O43	1000	
64	O44	846	
65	O45	693	
66	O46	539	
67	O47	385	
68	O48	231	
69	O49	77	
70	O50	–77	
71	O51	–231	
72	O52	–385	
73	O53	–539	
74	O54	–693	
75	O55	–846	
76	O55	–1000	
77	O57	–1154	
78	O58	–1308	
79	O59	–1462	
80	O60	–1616	
81	O61	–1770	
82	O62	–1924	
83	O63	–2078	
84	O64	–2232	

PAD		Actual dimensions	
NO.	NAME	X	Y
85	O65	–2385	727
86	O66	–2539	
87	O67	–2693	
88	O68	–2847	
89	O69	–3001	
90	O70	–3155	
91	O71	–3309	
92	O72	–3463	
93	O73	–3617	
94	O74	–3771	
95	O78	–3924	
96	O76	–4078	
97	O77	–4232	
98	O78	–4386	
99	O79	–4540	
100	O80	–4694	
101	O81	–4848	
102	O82	–5002	
103	O83	–5156	
104	O84	–5310	
105	O85	–5463	
106	O86	–5617	
107	O87	–5771	
108	O88	–5925	
109	O89	–6079	
110	O90	–6430	690
111	O91	–6560	545
112	O92	–6430	401
113	O93	–6560	257
114	O94	–6430	112
115	O95	–6560	–32
116	O96	–6430	–177
117	O97	–6560	–321
118	O98	–6430	–466
119	O99	–6560	–610

FUNCTIONAL DESCRIPTION

Shift register

This is a bidirectional shift register to transfer common data.
Being a 50 × 2 bits configuration, this register can select 50 × 2 bits or 100 bits according to the status of SEL.
When the 50 × 2 bits configuration is selected, the input of the 50-bit shift register becomes D13.

Level shifter

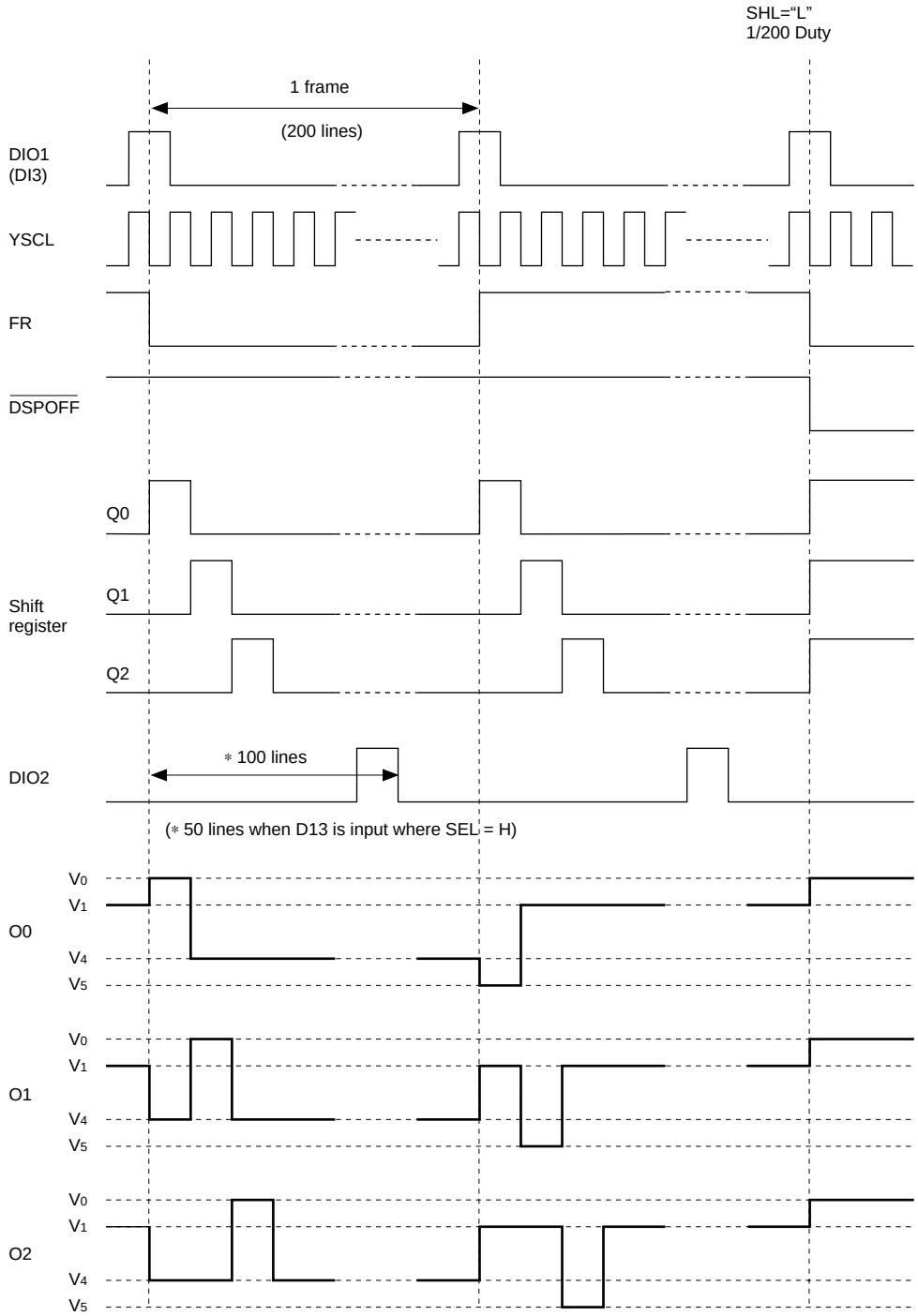
This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver

This driver outputs the LCD drive voltage.
The relationship among the display blanking signal $\overline{\text{DSPOFF}}$, contents of shift register, AC converted signal FR and On output voltage is as shown in the table below:

$\overline{\text{DSPOFF}}$	Content of shift register	FR	O output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	–	–	V_0	–

TIMING CHART



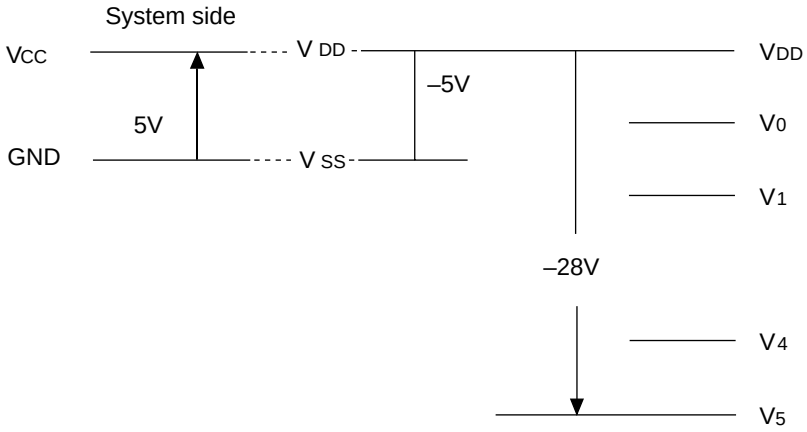
ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltage	V_I	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg 1	–65 to +150	°C

Notes*

1. The voltage of V_0, V_1, V_4 and V_5 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$.



2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V or less can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.

ELECTRICAL CHARACTERISTICS

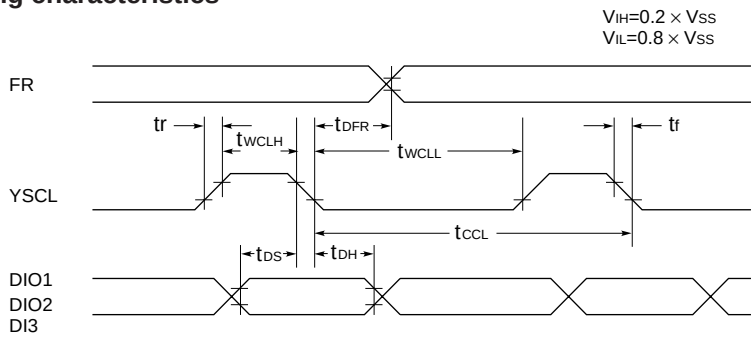
DC characteristics

Unless otherwise specified, $V_{DD} = V_0 = 0V$, $V_{SS} = -5.5V$–$2.7V$, Ta = –40 to 85°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–12.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–8.0	V	V_5
Supply voltage (2)	V_0	–	2.5	–	0	V	V_0
Supply voltage (3)	V_1	–	$2/9 \cdot V_5$	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	–	V_5	–	$7/9 \cdot V_5$	V	V_4
"H" input voltage	V_{IH}	–	$0.2 \cdot V_{SS}$	–	–	V	DIO1, DIO2, FR, YSCL, SHL, DI3 $\overline{DSPOFF}$, SEL
"L" input voltage	V_{IL}	–	–	–	$0.8 \cdot V_{SS}$	V	
"H" output voltage	V_{OH}	I_{OH}=–0.3mA	V_{DD}–0.4	–	–	V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL}=0.3mA	–	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	–	–	2.0	µA	YSCL, SHL, DI3 $\overline{DSPOFF}$, FR, SEL
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	–	–	5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5=–12.0 ~ –28.0V $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔV_{ON}=0.5V $V_0=V_{DD}$, V_1=–1.5V V_4=–18.5V V_5=–20.0V	–	0.75	1.0	KΩ	O0~O99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$, f_{YSCL}=12KHz Frame frequency=60Hz Input data: 1/200 Ta=25°C ?	–	7	15	µA	V_{SS}
		V_{SS}=–3.0V Other conditions are the same as V_{SS} = –5.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0V, V_0=0V, V_1=1.5V, V_4=18.5V, V_{EE}=V5=–20.0V Other conditions are the same as in the item of ISS 1.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{DSPOFF}$, FR, DI3, SEL
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

AC CHARACTERISTICS

Input timing characteristics



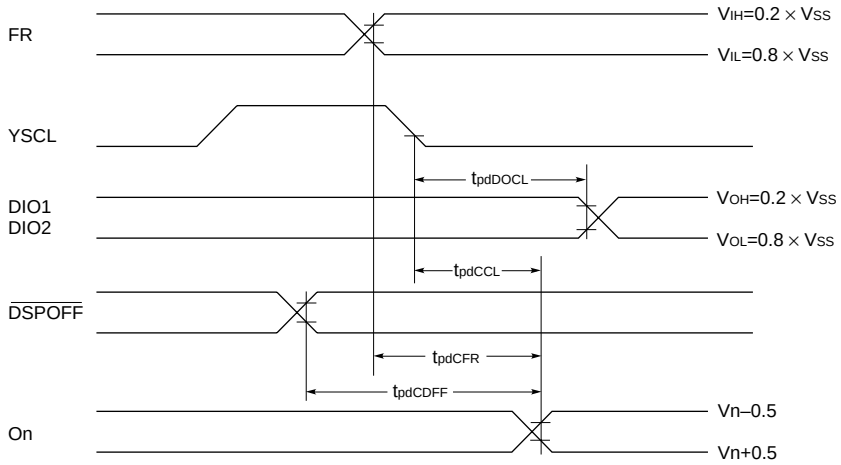
VSS=–5.0V±0.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	500	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	70	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	100	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–300	300	ns

VSS=–5.0V±0.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	1000	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	160	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	200	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

Output timing characteristics



VSS=–5.0±10%, Ta=–40 to +85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	tpdDOCL	CL=15pF	–	350	ns
(YSCL - fall to On output) delay time	tpdCCL	V5=–12.0 to –28.0V	–	1.0	µs
($\overline{\text{DSPOFF}}$ to On output) delay time	tpdCDOFF				
(FR to On Output) delay time	tpdCFR	CL=100pF	–	1.0	µs

VSS=–4.5–2.7V, Ta=–40 to +85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	tpdDOCL	CL=15pF	–	400	ns
(YSCL - fall to On output) delay time	tpdCCL	V5=–12.0 to –28.0V	–	2.0	µs
($\overline{\text{DSPOFF}}$ to On output) delay time	tpdCDOFF				
(FR to On Output) delay time	tpdCFR	CL=100pF	–	2.0	µs

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is optimum to divide the resistance of potential between V_{DDH} and GND to drive the LCD using the voltage follower with an operational amplifier. In taking into consideration of such a case using the operational amplifier, the maximum potential level V_0 for LCD driving has been made a separate pin from V_{DD}.
When no operational amplifier is used in V_0, set $V_0 = V_{DD}$.
When a resistive divider is used, set it to a resistance value as low as possible in the system power capacity.
When a series resistance exists in the power supply line of V_{DD}, a voltage drop of V_{DD} occurs at the LSI power supply pin, the relationship with the LCD's intermediate potential ($V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$) cannot be met, this causing the LSI to be broken down in some cases. When a protection resistor is inserted, it is necessary to stabilize the voltage by capacitance.

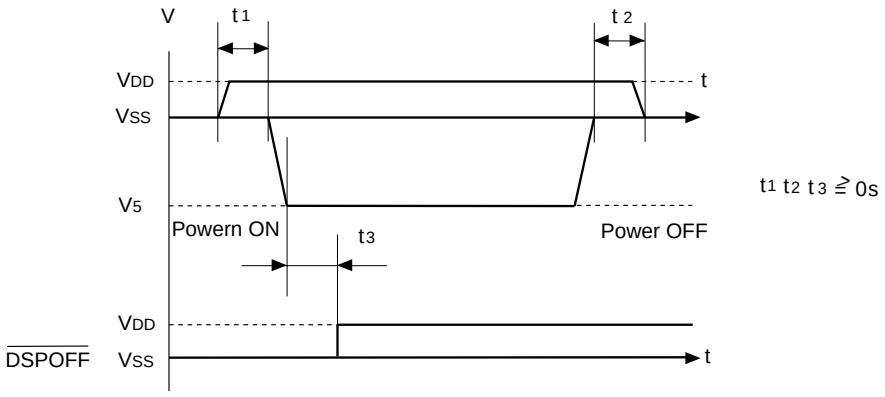
Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating or above V_{SS} = –2.5 V, an overcurrent flows and LSI breaks down in some cases.
To avoid this, it is recommended to suppress the potential of LCD drive output to V_0 level using the display off function ($\overline{DSPOFF}$) until the LCD driving system voltage is stabilized.

Be sure to follow the power ON/OFF sequence as shown below:

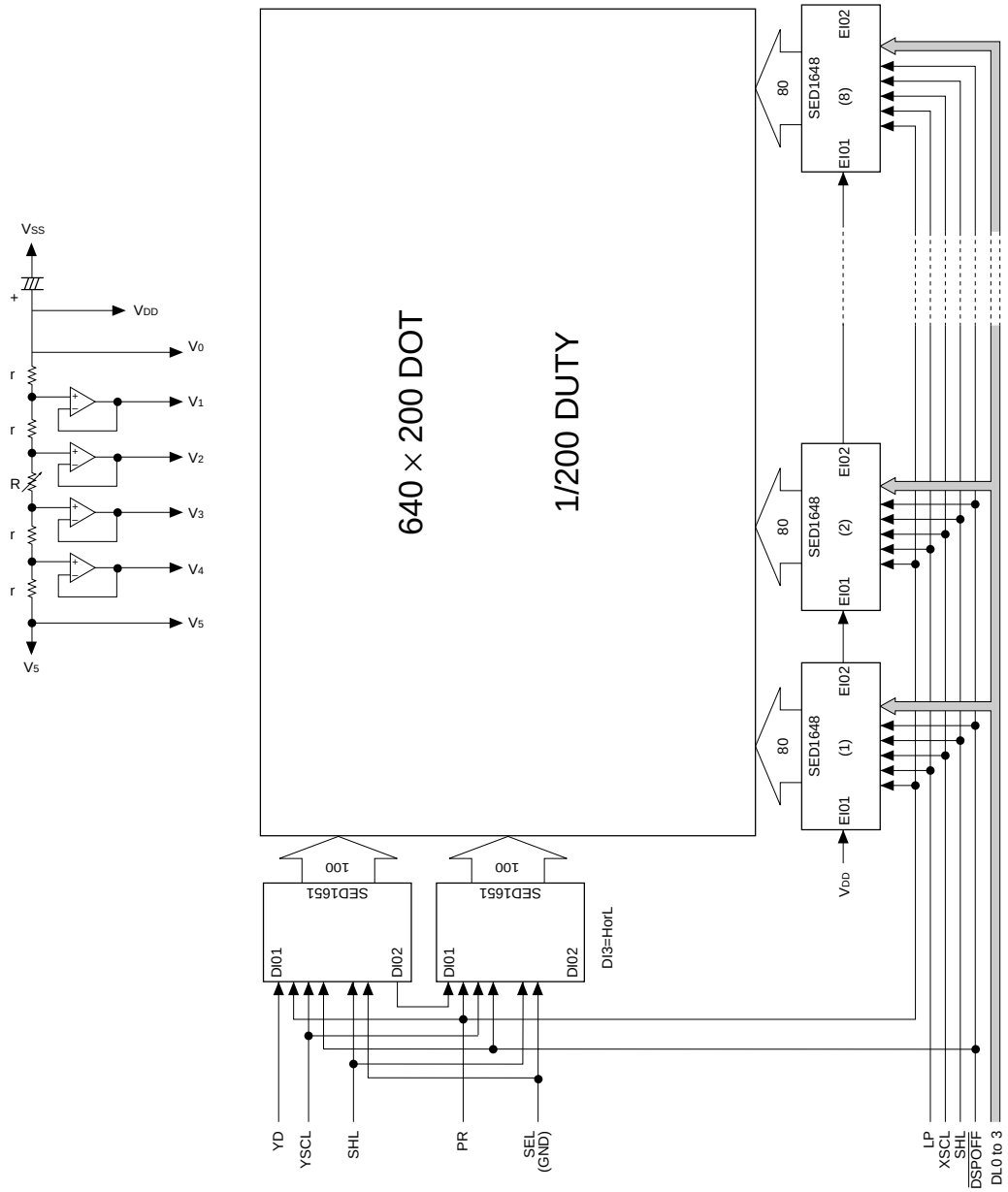
At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

For a countermeasure to such overcurrent, it is effective to put a high-speed melting fuse or protection resistor in series with the LCD power unit.
It is then required to select the optimum value in the protection resistance according to the capacitance of LC cell.



TYPICAL CIRCUIT DIAGRAM

Configuration Drawing of Large Screen LCD



9. SED1670
Dot Matrix LCD Common Driver

CONTENTS

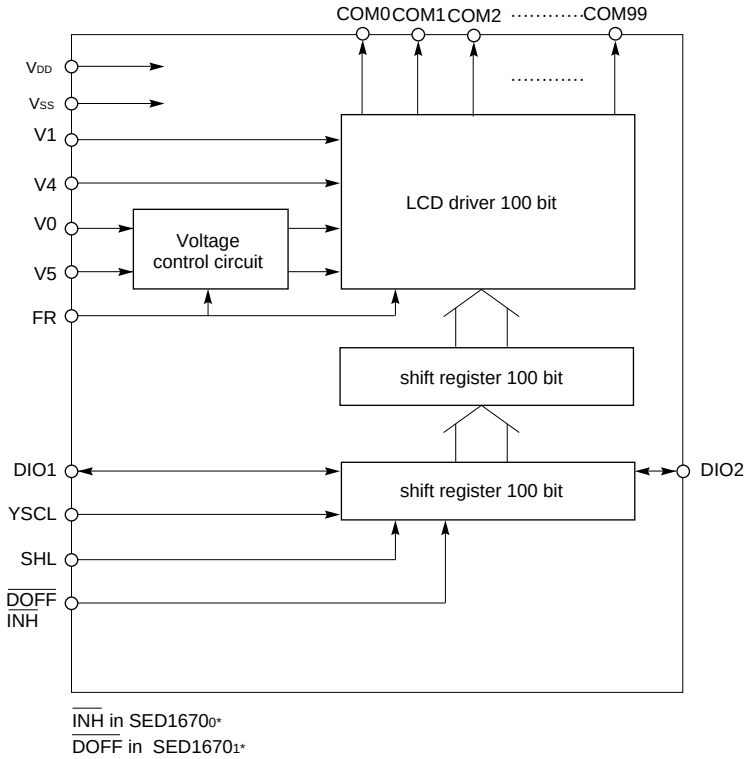
OVERVIEW

The SED1670 is a 100 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels upto a duty ratio of 1/300. It is intended to be used in conjunction with the SED1640D or SED1606D as a pair.
Since the SED1670 is so designed to drive LCDs over a wide range of voltages, and also the maximum potential V_0 of its LCD drive bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel.
And the SED1670 can display 65 x 132 panel when used as a common driver of RAM buit-in driver, SED1531.

FEATURES

- Number of LCD drive output segments: 100
- Common output ON resistance: 700 Ω (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640 × 480 dots when used in combination with SED 1640D or SED1606D.
- Selectable pin output shift direction
- No-bias display OFF function (*1*)
- Instantaneous display blanking enabled by inhibit function (*0*)
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –7 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging
  SED1670D$_{0A}$ (AL-pad die form)
  SED1670D$_{1A}$
  SED1670D$_{0B}$ (Au bump die form)
  SED1670D$_{1B}$
  SED1670T$_{0A}$ (TCP die form)
  SED1670T$_{1A}$
- No radial rays countermeasure taken in designing

BLOCK DIAGRAM

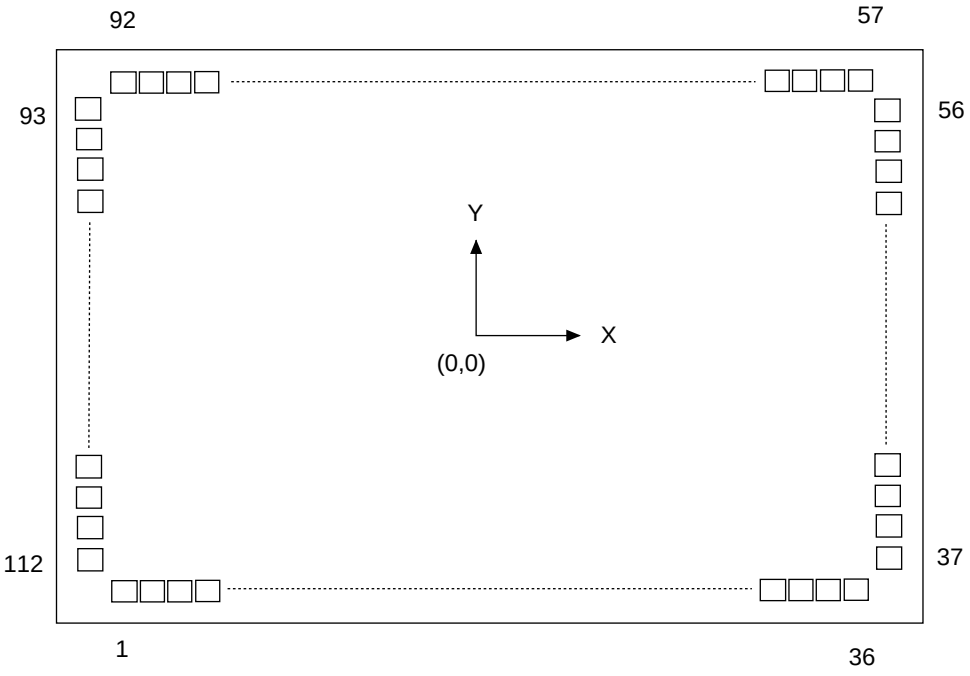


PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>COM0 to COM099</td><td>O</td><td>LCD drive common (row) output
The output changes at the YS CL falling edge.</td><td>100</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>100-bit shift register serial data input/output
To be set to input or output according to the SHL input
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input
The scanning data is shifted at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO pin I/O control input
<table>
<tr><th>SHL</th><th>COM output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 → 99</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>99 → 0</td><td>Ourput</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{\text{DOFF}}$</td><td>I</td><td>LCD display blanking control input
When “L” is input, the content of shift register is cleared and all common outputs become the V_0 level instantaneously (SED1670D_{1B}).</td><td>1</td></tr>
<tr><td>($\overline{\text{INH}}$)</td><td>I</td><td>LCD drive display blanking control input
When “L” is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously.
Common output = V_4 (when FR = L)
Common output = V_1 (when FR = H) (SED1670D_{0B})</td><td>(1)</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output AC converted signal input</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V (GND) V_{SS}: –5.0 V</td><td>2</td></tr>
<tr><td>V0, V1, V4, V5</td><td>Power supply</td><td>LCD drive power supply V_5: –7 V to –28 V
$V_{DD} \geq V_0 \geq V_1 > V_4 \geq V_5$</td><td>4</td></tr>
</table>

$\overline{\text{INH}}$ for SED1670*$_{0*}$ Total: 112
$\overline{\text{DOFF}}$ for SED1671*$_{1*}$

PAD LAYOUT AND COORDINATES



Chip size ..... 5.49mm × 3.03mm
Chip thickness ..... 525μm (Au-bump die from)
400μm (Al-Pad die from)

1) Au bump specification reference values

Bump specific : High Quarity Au bump
Bump size : 90μm × 90μm
Bump height : 17μm ~ 28μm

2) AL Pad specification reference values

Pad Opening : 100μm × 100μm

PAD		Actual dimensions	
NO.	NAME	X	Y
1	COM5	-2187	-1357
2	6	-2058	
3	7	-1929	
4	8	-1799	
5	9	-1670	
6	10	-1541	
7	11	-1412	
8	12	-1283	
9	13	-1153	
10	14	-1024	
11	15	-895	
12	16	-766	
13	17	-637	
14	18	-507	
15	19	-378	
16	20	-249	
17	21	-120	
18	22	10	
19	23	139	
20	24	268	
21	25	397	
22	26	526	
23	27	656	
24	28	785	
25	29	914	
26	30	1043	
27	31	1172	
28	32	1302	
29	33	1431	
30	34	1560	
31	35	1689	
32	36	1818	
33	37	1948	
34	38	2077	
35	39	2206	
36	40	2335	-1357
37	41	2584	-1231
38	42	2584	-1094
39	43	2584	-969
40	44	2584	-840

PAD		Actual dimensions	
NO.	NAME	X	Y
41	COM45	2584	-711
42	46		-581
43	47		-452
44	48		-323
45	49		-194
46	50		-65
47	51		65
48	52		194
49	53		323
50	54		452
51	55		581
52	56		711
53	57		840
54	58		969
55	59		1098
56	60	2584	1231
57	61	2298	1357
58	62	2168	
59	63	2039	
60	64	1910	
61	65	1781	
62	66	1652	
63	67	1522	
64	68	1393	
65	69	1264	
66	70	1135	
67	71	1006	
68	72	876	
69	73	747	
70	74	618	
71	75	489	
72	76	360	
73	77	230	
74	78	101	
75	79	-28	
76	80	-157	
77	81	-286	
78	82	-416	
79	83	-545	
80	84	-674	1357

PAD		Actual dimensions	
NO.	NAME	X	Y
81	COM85	-803	1357
82	86	-932	
83	87	-1062	
84	88	-1191	
85	89	-1320	
89	90	-1449	
87	91	-1578	
88	92	-1708	
89	93	-1837	
90	94	-1966	
91	95	-2095	
92	96	-2224	1357
93	97	-2473	1334
94	98		1201
95	99		1071
96	DIO2		941
97	$\overline{\text{DOFF}}$		715
(97)	($\overline{\text{INH}}$)		
98	FR		585
99	YSCL		455
100	SHL		325
101	V_{DD}		185
102	V_{SS}		46
103	V0		-112
104	V1		-252
105	V4		-391
106	V5		-531
107	DIO1		-671
108	COM0		-810
109	1		-941
110	2		-1071
111	3		-1201
112	4	-2473	-1334

PAD No. 97: $\overline{\text{INH}}$ for SED1670✻0✻
$\overline{\text{DOFF}}$ for SED1670✻1✻

FUNCTIONAL DESCRIPTION

Shift register

This is a bidirectional shift register to transfer common data.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver circuit

This driver outputs the LCD drive voltage.
The relationship among the display blanking signal DOFF, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below:

(SED1670*1*)

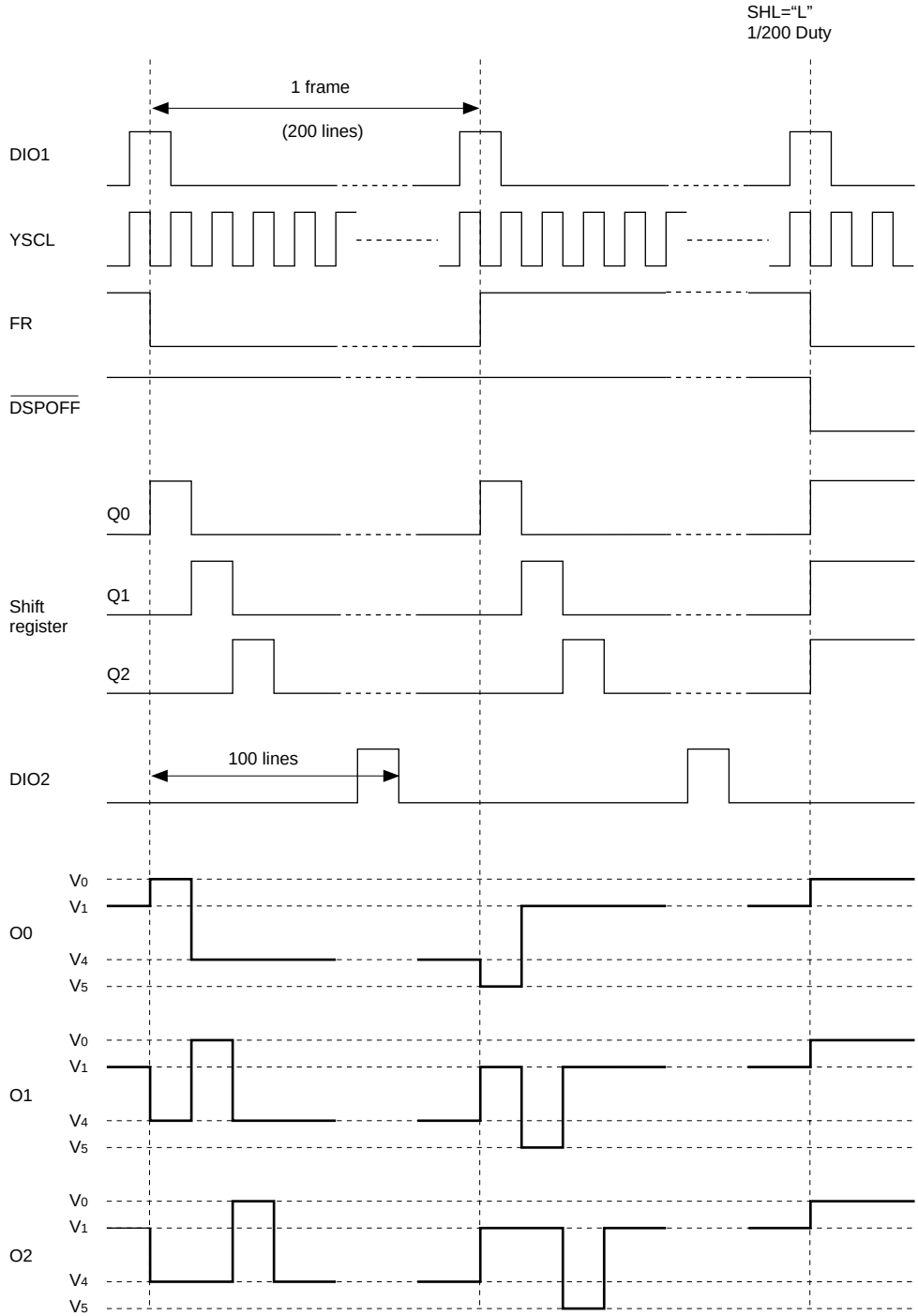
$\overline{DOFF}$	Contents of shift register	FR	COM output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	Fixed to L	–	V_0	–

The relationship among the display blanking signal INH, contents of the shift register, AC converted signal FR and COM output voltage is as shown in the table below:

(SED1670*0*)

INH	Contents of shift register	FR	COM output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	Fixed to L	H	V_1	(Non-select level)
		L	V_4	

TIMING CHART (SED1670D1B)



The V1 or V4 non-select level is output corresponding to the FR in SED1670D0B or $\overline{INH}$=L, respectively.

ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltage	V_I	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg	–65 to +150	°C

Notes:

1. The voltage of V_0, V_1 and V_4 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.

ELECTRICAL CHARACTERISTICS

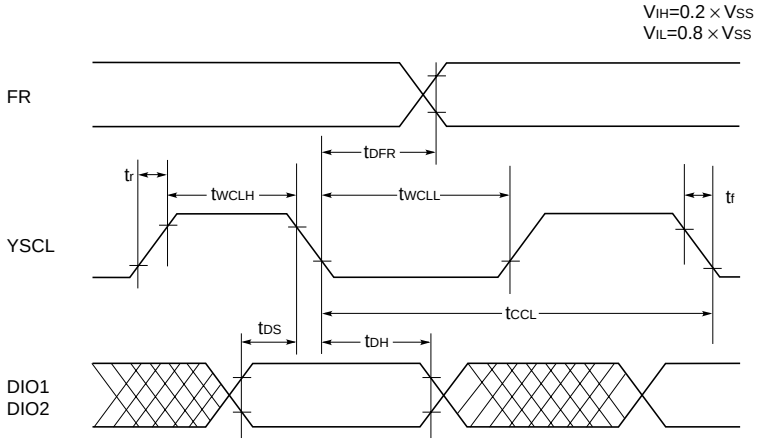
DC characteristics

Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V±10%, Ta = –40 to 85°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–7.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–7.0	V	V_5
Supply voltage (2)	V_0	Recommended value	–2.5	–	0	V	V_0
Supply voltage (3)	V_1	Recommended value	2/9·V_5	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	Recommended value	V_5	–	7/9·V_5	V	V_4
"H" input voltage (1)	V_{IH}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	DIO1, DIO2, YSCL, SHL, FR
"L" input voltage (1)	V_{IL}		V_{SS}	–	0.8V_{SS}	V	
"H" input voltage (2)	V_{IHT}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	$\overline{DOFF}$, $\overline{INH}$
"L" input voltage (2)	V_{ILT}		V_{SS}	–	0.85V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH}=–0.3mA I_{OH}=–0.2mA (V_{SS}=–2.7 to –4.5V)	–0.4	–	0	V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL}=+0.3mA I_{OL}=+0.2mA (V_{SS}=–2.7 to –4.5V)	V_{SS}	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	V_{SS} ≤ V_{IN} ≤ 0V	–	–	2.0	µA	YSCL, SHL, $\overline{DOFF}$, $\overline{INH}$, FR
Input/output leakage current	$I_{LI/O}$	V_{SS} ≤ V_{IN} ≤ 0V	–	–	5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5=–7.0 to –28.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔVON =0.5V; V_5= –20.0V; When the V_1, V_4, V_0 or V_5 level is output	–	0.70	1.40	KΩ	COM0~COM99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, V_{IH}=VDD, V_{IL}=V_{SS}, f_{YSCL}=12KHz, Frame frequency=60Hz Input data; "H" at no load every 1/200 duty	–	7	15	µA	V_{SS}
		Other conditions are the same as V_{SS} = –3.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0, V,=–2.0V, V_4=–18.0V, V_5=–20.0V Other conditions are the same as in the item of I_{SS1}.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{DOFF}$, $\overline{INH}$, FR
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

AC CHARACTERISTICS

Input timing characteristics



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

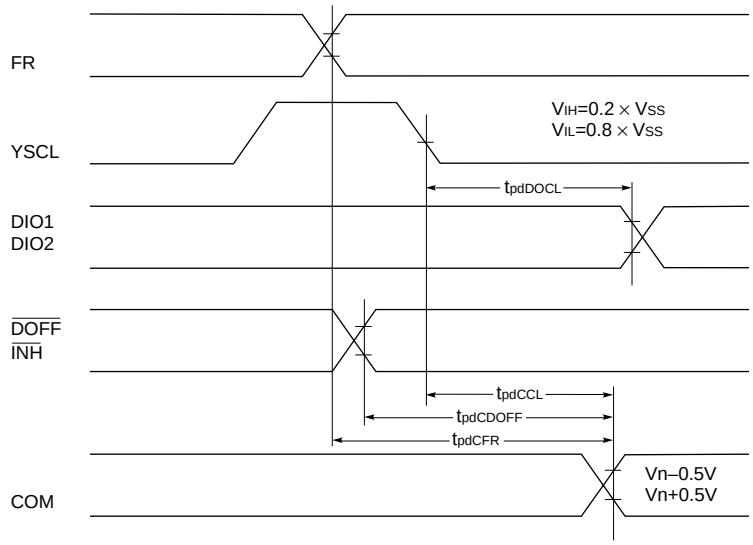
Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	500	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	70	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	100	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	1000	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	160	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	200	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

The standard applicable to t_{CCL}, t_{WCLH}, t_{WCLL} and t_{DS} when V_{SS} = –2.4 V shall be 1.3 times of that applies when V_{SS} = –2.7V to –4.5V.

Output timing characteristics



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	C_L=15pF	30	300	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V C_L=100pF	–	3.0	µs
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}		–	3.0	µs

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	C_L=15pF	60	600	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V C_L=100pF	–	3.0	µs
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}		–	3.0	µs

The standard applicable at V_{SS} = –2.4V shall be the same as that employed when V_{SS} = –2.7V to –4.5V.

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is the most simple to divide the resistance of potential as shown in the connection example. On the other hand, to obtain a high quality display, it is necessary to raise the accuracy and constancy of each voltage level and to set the divided resistance value as low as possible in the range of system power capacity.
Especially when a low-power LCD driving is required, set the divided resistance to a higher value and drive the LCD with a voltage follower by means of operational amplifier instead. In taking into consideration of a case where the operational amplifier is employed, the maximum potential level V0 for LCD driving has been isolated from the V_{DD} pin.
When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD}.
When no operational amplifier is used, connect V_0 and V_{DD} pins.

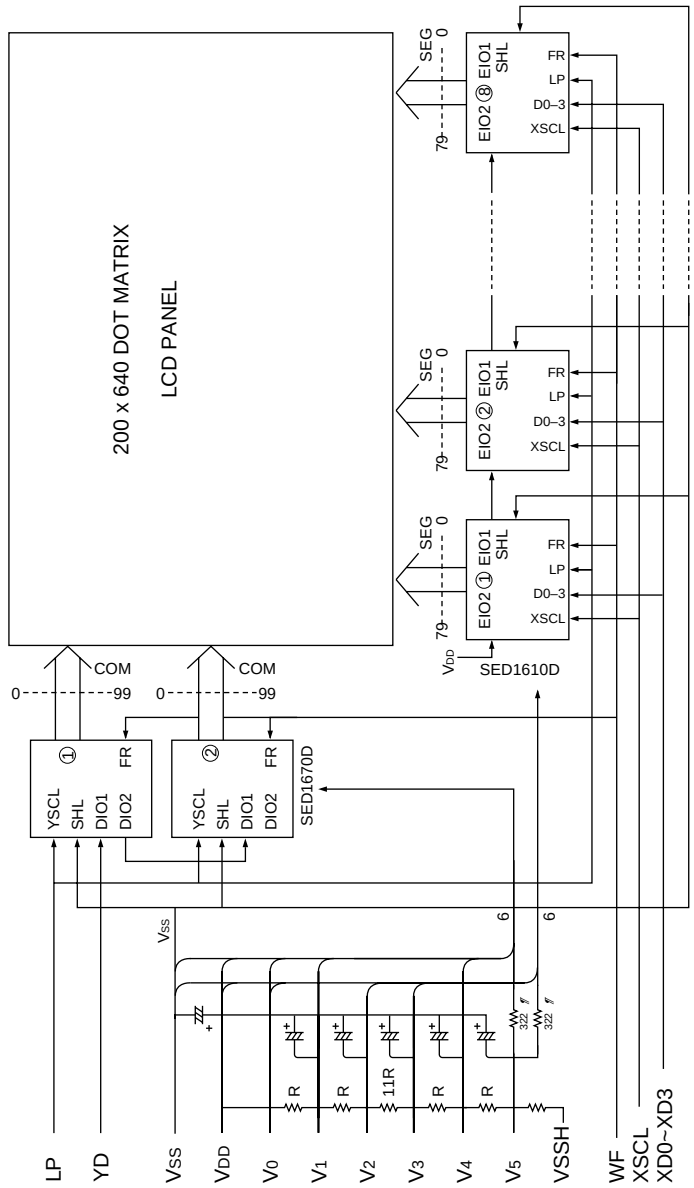
Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating, an overcurrent flows and LSI breaks down in some cases.

Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

CONNECT EXAMPLE



Note *1 It must be provided as the protective resister against overcurrent. Also, the bypass capacitor (0.01 μF) for noise suppression must be provided near to VSS and V5 terminals on each LSI.

DIFFERENT POINTS FROM REPLACEMENT PRODUCT

	SED1670*0*	SED1631**
Function	Bidirectional shift register $\overline{INH}$ 100 output segments	Bidirectional shift register $\overline{INH}$ 100 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	–
PAD coordinates	Different from the equivalent product	–

	SED1670*1*	SED1635**
Function	Bidirectional shift register $\overline{DOFF}$ 100 output segments	Bidirectional shift register $\overline{DOFF}$ 100 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	–
PAD coordinates	Different from the equivalent product	–

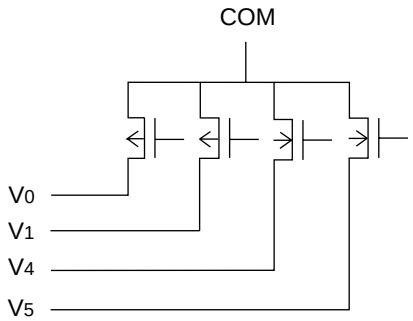


Fig. 1

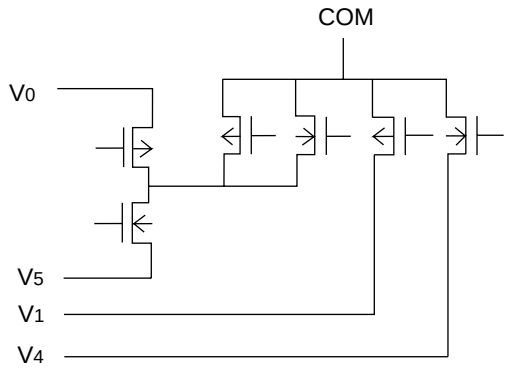


FIg. 2

10. SED1672
Dot Matrix LCD Common Driver

CONTENTS

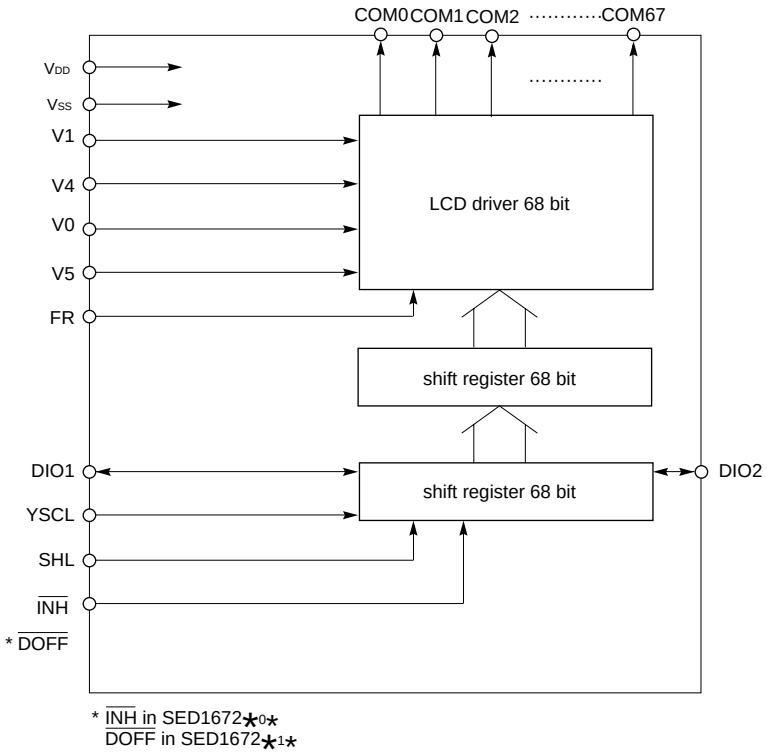
OVERVIEW

The SED1672 is a 68 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels up to a duty ratio of 1/300. It is intended to be used in conjunction with the SED1606 as a pair.
Since the SED1606 is so designed to drive LCD's over a wide range of voltages, and also the maximum potential V_0 of its LCD drive bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
The SED1672 is featured in its simple pad layout which is easy in mounting PC boards in addition to its selectable bidirectional driver output sequence. It also has 68 LCD output segments of high pressure resistance and low output impedance.
It can display the 65 × 132 panel when used as the expansion driver of SED1531 being built in RAM (SED1672*1*).

FEATURES

- Number of LCD drive output segments: 68
- Common output ON resistance: 700 Ω (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640 × 480 dots when used in combination with SED1606.
- Selectable pin output shift direction
- Instantaneous display blanking enabled by inhibit function (*0* type)
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –7 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging
  SED1672D0A (AL-pad die form)
  SED1672D1A
  SED1672F0A (80-pin QFP5)
- No radial rays countermeasure taken in designing
- Non-bias display off function

BLOCK DIAGRAM



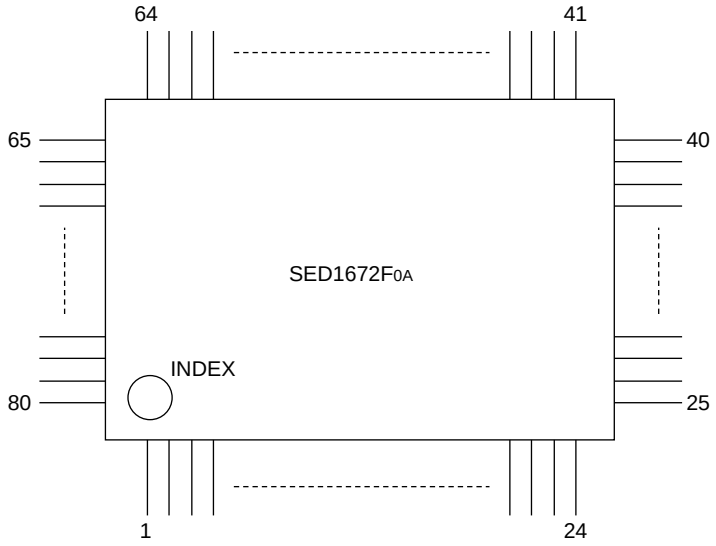
PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>COM0 to COM67</td><td>O</td><td>LCD drive common (row) output
The output changes at the YSCL falling edge.</td><td>68</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>100-bit shift register serial data input/output
To be set to input or output according to the SHL input
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input
The scanning data is shifted at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Display data latch pulse input (Falling edge trigger)
Shift direction selection and DIO pin I/O control input
<table>
<tr><th>SHL</th><th>COM output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 → 67</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>67 → 0</td><td>Ourput</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>LCD display blanking control input when “L” is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously. (SED1672✻1✻)</td><td>1</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>LCD display blanking control input
When “L” is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously.
Common output = V_4 (when FR = L)
Common output = V_1 (when FR = H) (SED1672✻0✻)</td><td>(1)</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output AC converted signal input</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V (GND) V_{SS}: –5.0 V</td><td>2</td></tr>
<tr><td>V_0, V_1, V_4, V_5</td><td>Power supply</td><td>LCD drive power supply V_5: –7 V to –28 V
$V_{DD} \geq V_0 \geq V_1 > V_4 \geq V_5$</td><td>4</td></tr>
</table>

$\overline{INH}$ in SED1672✻0✻
$\overline{DOFF}$ in SED1672✻1✻

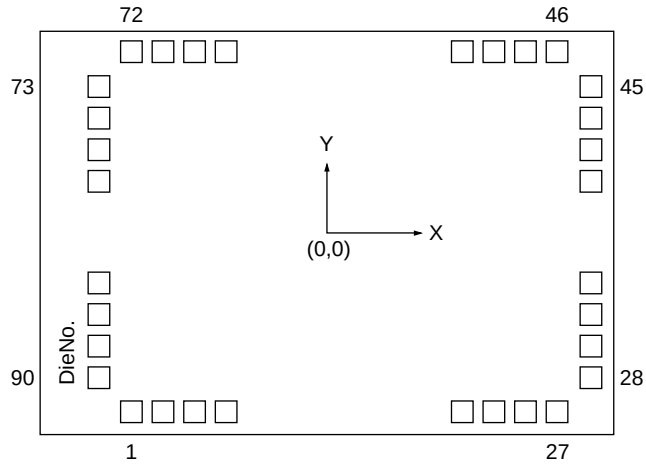
PIN LAYOUT

Package type: QFP–5 80pin



PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name
1	COM 3	21	COM 23	41	COM 43	61	COM 63
2	COM 4	22	COM 24	42	COM 44	62	COM 64
3	COM 5	23	COM 25	43	COM 45	63	COM 65
4	COM 6	24	COM 26	44	COM 46	64	COM 66
5	COM 7	25	COM 27	45	COM 47	65	COM 67
6	COM 8	26	COM 28	46	COM 48	66	DIO2
7	COM 9	27	COM 29	47	COM 49	67	$\overline{INH}$
8	COM 10	28	COM 30	48	COM 50	68	FR
9	COM 11	29	COM 31	49	COM 51	69	YSCL
10	COM 12	30	COM 32	50	COM 52	70	SHL
11	COM 13	31	COM 33	51	COM 53	71	V_{DD}
12	COM 14	32	COM 34	52	COM 54	72	V_{SS}
13	COM 15	33	COM 35	53	COM 55	73	V_0
14	COM 16	34	COM 36	54	COM 56	74	V_1
15	COM 17	35	COM 37	55	COM 57	75	V_4
16	COM 18	36	COM 38	56	COM 58	76	V_5
17	COM 19	37	COM 39	57	COM 59	77	DIO1
18	COM 20	38	COM 40	58	COM 60	78	COM 0
19	COM 21	39	COM 41	59	COM 61	79	COM 1
20	COM 22	40	COM 42	60	COM 62	80	COM 2

PAD LAYOUT AND PAD COORDINATE



Chip size: 4.27 × 3.03 mm
Chip thickness: 400 µm (for AL pad product) and 525 µm (for BUMP product).
AL pad product: Pad opening is 100 × 100 µm.
BUMP product: Vertical Au bump.
Bump size is 90 × 90 µm.
Bump height is 17 to 25 µm.

PAD NO.	PIN NAME	X	Y
1	DM	–1579	–1357
2	COM 3	–1449	
3	COM 4	–1320	
4	COM 5	–1191	
5	COM 6	–1062	
6	COM 7	–933	
7	COM 8	–803	
8	COM 9	–674	
9	COM 10	–545	
10	COM 11	–416	
11	COM 12	–287	
12	COM 13	–154	
13	COM 14	–28	
14	COM 15	101	
15	COM 16	230	
16	COM 17	359	
17	COM 18	489	
18	COM 19	618	
19	COM 20	747	
20	COM 21	876	
21	COM 22	1005	
22	COM 23	1135	
23	COM 24	1264	
24	COM 25	1393	
25	COM 26	1522	
26	DM	1651	
27	DM	1781	–1357
28	DM	1976	–1098
29	COM 27	1976	–969
30	COM 28	1976	–840

PAD NO.	PIN NAME	X	Y
31	COM 29	1976	–711
32	COM 30		–581
33	COM 31		–452
34	COM 32		–323
35	COM 33		–194
36	COM 34		–65
37	COM 35		65
38	COM 36		194
39	COM 37		323
40	COM 38		452
41	COM 39		581
42	COM 40		711
43	COM 41		840
44	COM 42		969
45	DM	1976	1098
46	DM	1743	1357
47	DM	1614	
48	COM 43	1485	
49	COM 44	1355	
50	COM 45	1226	
51	COM 46	1097	
52	COM 47	968	
53	COM 48	839	
54	COM 49	709	
55	COM 50	580	
56	COM 51	451	
57	COM 52	322	
58	COM 53	193	
59	COM 54	63	
60	COM 55	–66	1357

PAD NO.	PIN NAME	X	Y
61	COM 56	–195	1357
62	COM 57	–324	
63	COM 58	–453	
64	COM 59	–583	
65	COM 60	–712	
66	COM 61	–841	
67	COM 62	–970	
68	COM 63	–1099	
69	COM 64	–1229	
70	COM 65	–1358	
71	COM 66	–1487	
72	DM	–1616	1357
73	DM	–1865	1201
74	COM 67		1071
75	DIO2		941
76	*1 $\overline{\text{INH}}$		715
77	FR		585
78	YSCL		455
79	SHL		325
80	V_{DD}		195
81	V_{SS}		55
82	V_0		–112
83	V_1		–252
84	V_4		–391
85	V_5		–531
86	DIO1		–671
87	COM 0		–810
88	COM 1		–941
89	COM 2		–1071
90	DM	–1865	–1201

*1 PAD No. 76: $\overline{\text{INH}}$ for SED1672✻0✻
$\overline{\text{DOFF}}$ for SED1672✻1✻

FUNCTIONAL DESCRIPTION

Shift register

This is a bidirectional shift register to transfer common data.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver circuit

This driver outputs the LCD drive voltage.
The relationship among the display blanking signal $\overline{INH}$, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below:

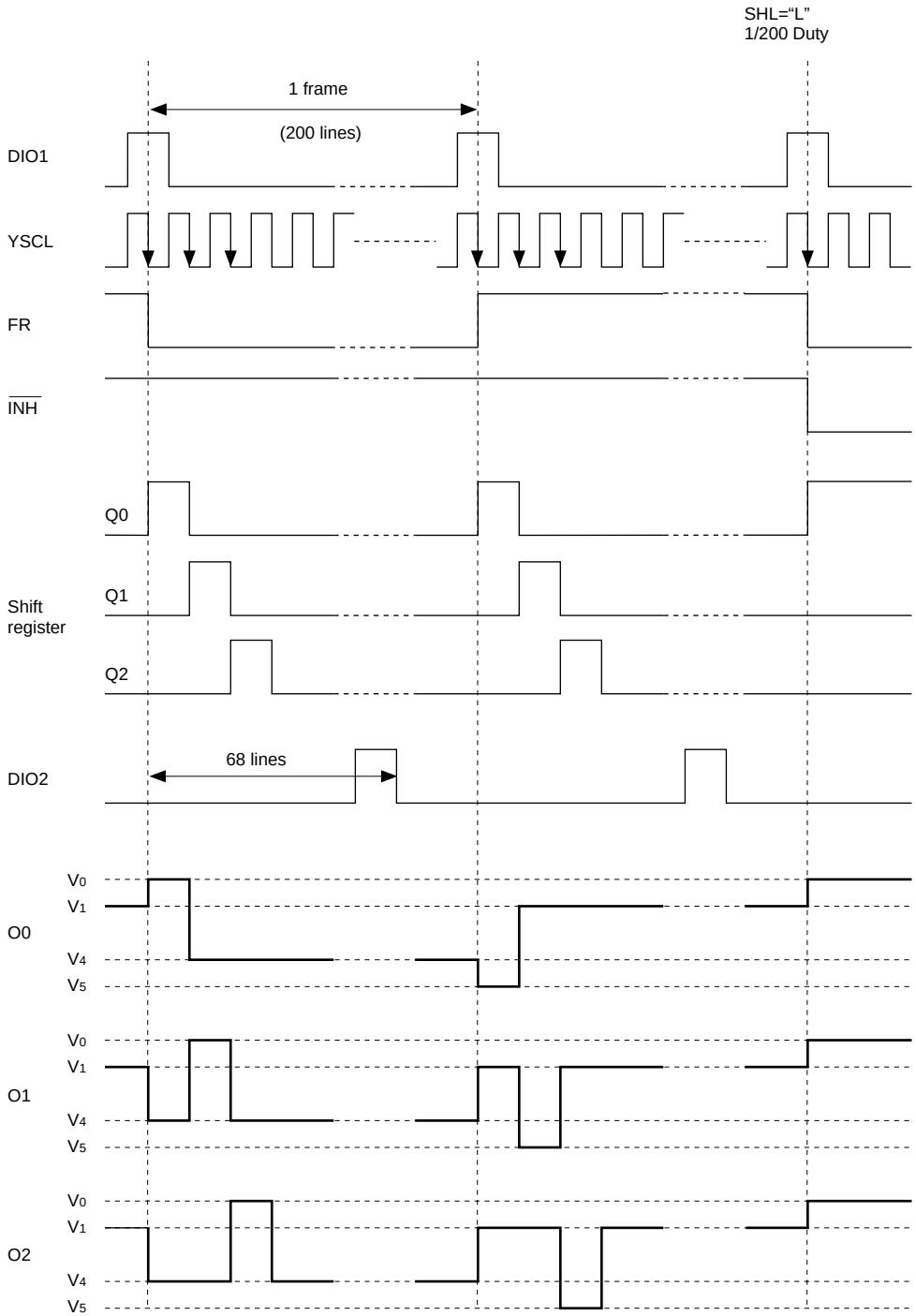
(SED1672*0*)

INH	Contents of shift register	FR	COM output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	Fixed to L	H	V_1	(Non-select level)
		L	V_4	

The relationship among the display blanking signal $\overline{INH}$, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below.

$\overline{DOFF}$	Contents of shift register	FR	COM output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	Fixed to L	—	V_0	(Non-select level)

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltage	V_I	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature	Tstg	–65 to +150	°C
Soldering temperature and time	Tsol	260°C · 10sec	–

Notes:

1. The voltage of V_0, V1 and V_4 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.
3. All the above voltage is based on V_{DD} = 0 V.

ELECTRICAL CHARACTERISTICS

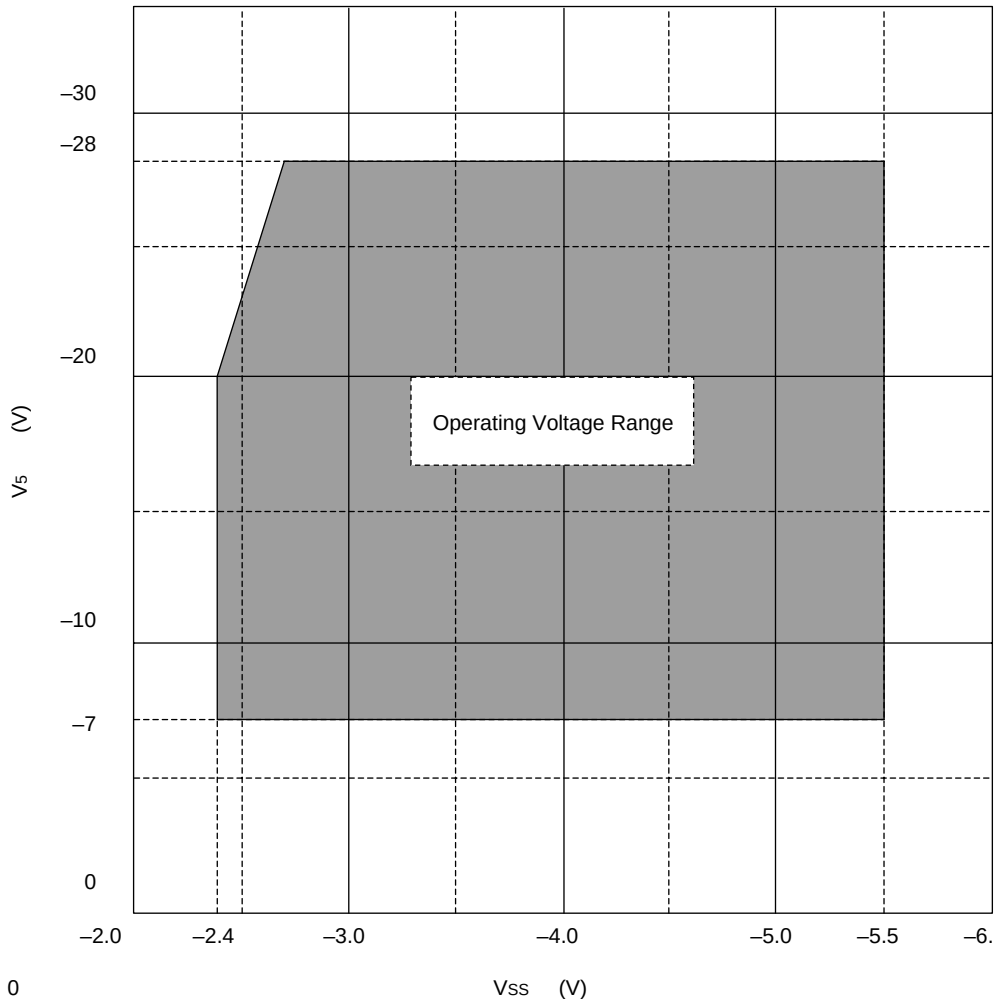
DC characteristics

Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V±10%, Ta = –40 to 85°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–7.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–7.0	V	V_5
Supply voltage (2)	V_0	Recommended value	–2.5	–	0	V	V_0
Supply voltage (3)	V_1	Recommended value	2/9·V_5	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	Recommended value	V_5	–	7/9·V_5	V	V_4
"H" input voltage (1)	V_{IH}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	DIO1, DIO2, YSCL, SHL, FR
"L" input voltage (1)	V_{IL}		V_{SS}	–	0.8V_{SS}	V	
"H" input voltage (2)	V_{IHT}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	$\overline{INH}$
"L" input voltage (2)	V_{ILT}		V_{SS}	–	0.85V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH}=–0.3mA I_{OH}=–0.2mA (V_{SS}=–2.7 to –4.5V)	–0.4	–	0	V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL}=+0.3mA I_{OL}=+0.2mA (V_{SS}=–2.7 to –4.5V)	V_{SS}	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	–	–	2.0	µA	YSCL, SHL, $\overline{INH}$, FR
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	–	–	5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5=–7.0 to –28.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔVON =0.5V, V_5= –20.0V, When the V_1, V_4, V_0 or V_5 level is output	–	0.70	1.40	KΩ	COM0 to COM99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, V_{IH}=VDD, V_{IL}=V_{SS}, f_{YSCL}=12KHz, Frame frequency=60Hz Input data; "H" at no load every 1/200 duy	–	7	15	µA	V_{SS}
		Other conditions are the same as V_{SS} = –3.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0V, V_1=–2.0V, V_4=–18.0V, V_5=–20.0V Other conditions are the same as in the item of I_{SS1}.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{INH}$, FR
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

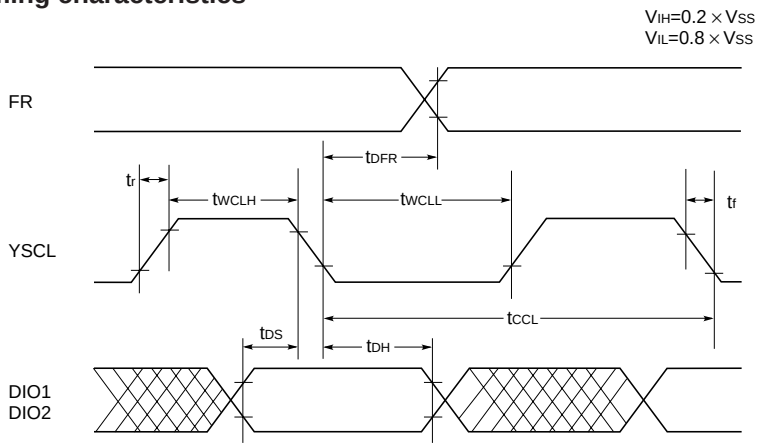
Operating Voltage Range V_{SS} – V_5

V_5 voltage must be set within the following operating voltage range of V_{SS} – V_5.



AC CHARACTERISTICS

Input timing characteristics



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

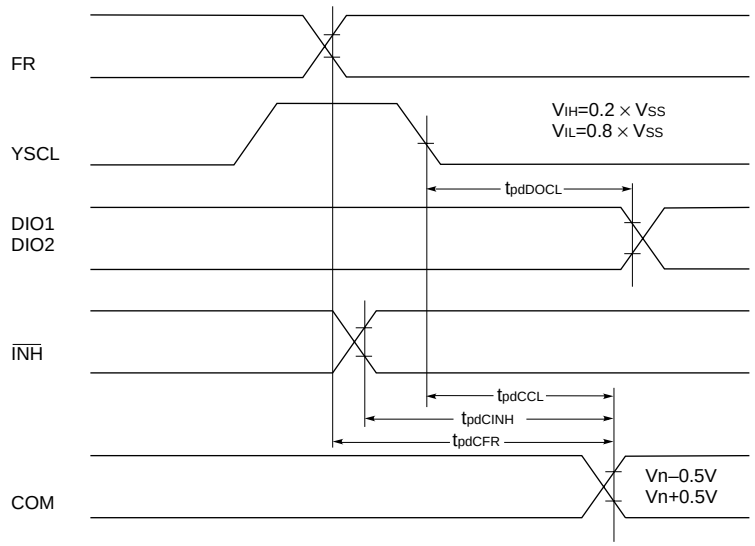
Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	500	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	70	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	100	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	1000	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	160	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	200	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

The standard applicable to t_{CCL}, t_{WCLH}, t_{WCLL}, t_{DS} and t_{DH} when V_{SS} = –2.4 V must be 1.3 times of that applies when V_{SS} = –2.7 V to –4.5 V.

Output timing characteristics



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	C_L=15pF	30	300	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V	–	3.0	µs
($\overline{INH}$ to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}	C_L=100pF	–	3.0	µs

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	C_L=15pF	60	600	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V	–	3.0	µs
($\overline{INH}$ to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}	C_L=100pF	–	3.0	µs

The standard applicable when V_{SS} = –2.4 V must be 1.3 times of that applies when V_{SS} = –2.7 V to –4.5 V.

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is the most simple to divide the resistance of potential as shown in the connection example.
On the other hand, to obtain a high quality display, it is necessary to raise the accuracy and constancy of each voltage level and to set the divided resistance value as low as possible in the range of system power capacity.
Especially when a low-power LCD driving is required, set the divided resistance to a higher value and drive the LCD with a voltage follower by means of operational amplifier instead. In taking into consideration of a case where the operational amplifier is employed, the maximum potential level V_0 for LCD driving has been isolated from the V_{DD} pin. When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD}.
When no operational amplifier is used, connect V_0 and V_{DD} pins.

Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating, an overcurrent flows and LSI breaks down in some cases.

Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

Precautions:

Users of this development specification are reminded of the following precautions.

1. This development specification is subject to change without previous notice.
2. This specificatino does not warrant the user to exercise the industrial property right or other rights, nor does this specification vest such rights to the user.
   Application examples provided in this specification are solely intended to ensure better understanding of the product. The manufacturer shall not be liable for any circuit related problem arising from using such examples.
   Numeric representation of measure or size provided in the characteristics table is one obtained from the numeric line.
3. No part of this specification may be reproduced or duplicated in any form or by any means without the written permission of the manufacturer.
4. As for use of semiconductor elements, users are required to pay attention to the following points.
   [Precautions on the Product Handling in Light]
   Characteristics of semiconductor elements are changed if they are exposed to light. Thus, exposing this IC to light can result in its in malfunction. In order to prevent IC malfunctioning due to light, make sure that the following measures are taken for the boards or products equipped with our IC.
   (1) Design and mounting procedure employed do not allow light to IC.
   (2) The inspection process is implemented in the environment that does not allow light to IC.
   (3) Light shielding measures are established not only for surface of IC but also for rear face and side faces, too.

DIFFERENT POINTS FROM REPLACEMENT PRODUCT

	SED1672*0*	SED1630**
Function	Bidirectional shift register $\overline{INH}$ 68 output segments	Bidirectional shift register $\overline{INH}$ 68 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	–
PAD coordinates	Different from the equivalent product	–

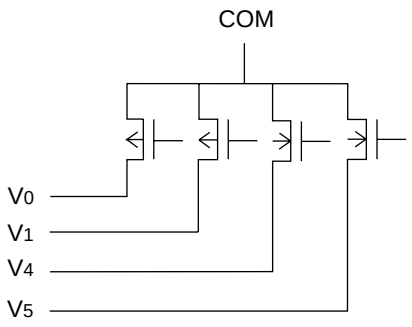


Fig. 1

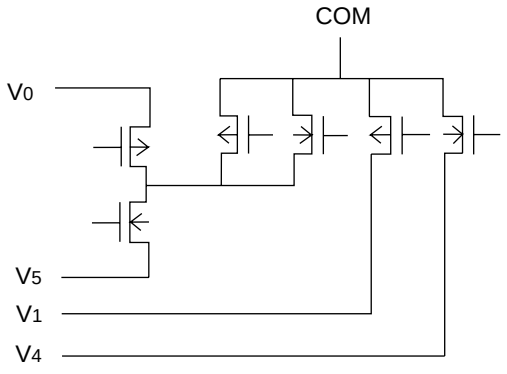


FIg. 2

11. SED1681
LCD Driver

CONTENTS

OVERVIEW

The SED1681 is a dot-matrix LCD segment driver for small, high-contrast display panels with duty cycles ranging from 1/8 to 1/32. The segment driver incorporates 80 driver circuits with input and output data interfaced serially.

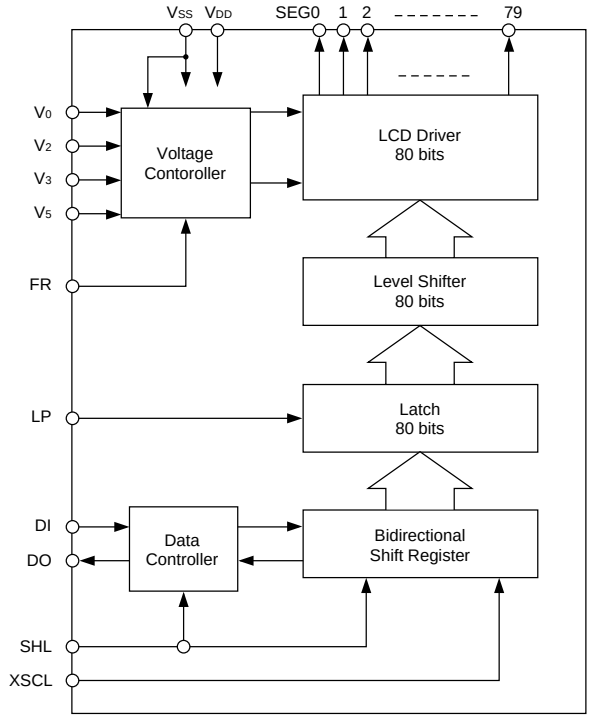
The SED1681 is designed for use as a display expansion driver for use either with dedicated LCD controllers such as the SED1278F and SED1200F, or with 4-bit micro-controller devices. It also shares a common interface with the SED1181F.

The SED1681 is available as chips (SED1681D0A) or in 100-pin QFPs (SED1681F0A).

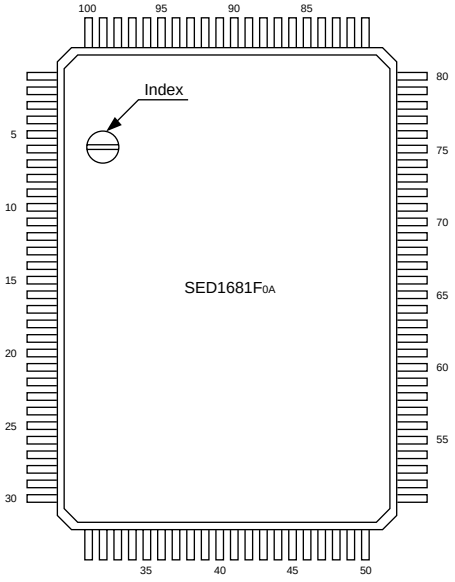
FEATURES

- 80 LCD segment driver outputs
- Display duty cycles ranging from 1/8 to 1/32
- Serial input and output data pins
- Chips (SED1681D0A) or 100-pin QFPs (SED1681F0A)

BLOCK DIAGRAM



PINOUT



FUNCTIONAL DESCRIPTION

Shift Register

Teh SED1681 contains a static 80-bit bidirectional shift register. The serial display data is shifted into the register on the falling edge of the XSCL clock input signal.

Data Controller

The data controller switches the input data into the bidirectional shift register, as selected by the SHL pin. If the SHL pin is at VSS, the data is shifted in from bit 0 towards bit 79. If SHL is at VDD, the data shift direction is reversed, as shown in the figure below.

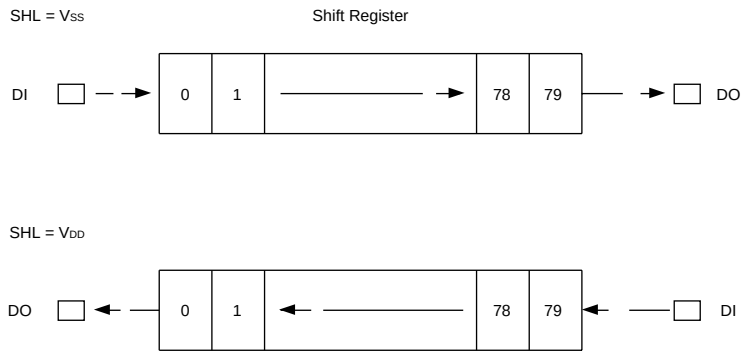


Figure 1. Data Shift Direction

Latch

Input data from the shift register is latched on the falling edge of LP. The latch outputs drive the level shift inputs.

Level Shifter

The level shifter converts the logic-level signal from latch to the voltage levels required by the LCD drivers.

LCD Driver and Voltage Control Circuit

The LCD drivers drive individual segments of the display matrix. The output voltage is determined by the frame signal FR and the latched display data, as shown in the table below.

Latched Data	FR	SEG Output Voltage
H	H	V5
	L	V0
L	H	V3
	L	V2

LCD Drive Voltages

The LCD driver requires accurate voltage supplies for optimum display contrast. The values of these voltages for different duty cycle displays are shown in the table below. Note that V_1 and V_4 are used by the row drivers and are not connected to the SED1681.

Power Supply	Duty Cycle, Bias	
	1/8, 1/4	1/16, 1/5
V_{DD}	V_{DD}	V_{DD}
V_1	$1/4 \times V_5$	$1/5 \times V_5$
V_2	$2/4 \times V_5$	$2/5 \times V_5$
V_3	$2/4 \times V_5$	$3/5 \times V_5$
V_4	$3/4 \times V_5$	$4/5 \times V_5$
V_5	V_5	V_5

PIN DESCRIPTION

Pin name	I/O	Description	Number of pins
SEG0 to SEG79	O	Liquid crystal segment drive outputs Segment outputs change on the falling edge of the LP input signal.	1 to 30, 51 to 100
XSCL	I	Shift clock input Shift register data is shifted on the falling edge of this signal.	40
LP	I	Display data strobe Data from the shift register is strobed on to the display data latch on the falling edge of this signal.	37
DI	I	Serial data input	41
DO	O	Serial data output	42
SHL	I	Shift direction select This pin selects the data shift direction from bit 0 towards bit 79 or in reverse.	39
FR	I	Liquid crystal frame signal input	44
V_{DD}	—	Ground	46
V_{SS}	—	Logic power supply	36
V_0, V_2, V_3, V_5	—	LCD drive voltage supply inputs These voltages should satisfy the following conditions. $V_{DD} \geq V_0$, $V_{DD} \geq V_2 \geq 1/2 \times V_5$, $1/2 \times V_5 \geq V_3 \geq V_5$	32 to 25
NC	—	No connection	31, 38, 43, 45, 47 to 50

SPECIFICATIONS

Absolute Maximum Ratings

V_{DD} = 0V

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–15.0 to +0.3	V
Supply voltage (3)	V_0, V_2, V_3	–15.0 to +0.3	V
Input pin voltage	V_I	V_{SS}–0.3 to +0.3	V
Output pin voltage	V_O	V_{SS}–0.3 to +0.3	V
Power dissipation	P_D	300	mW
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–65 to +150	°C
Soldering temperature and time (at lead)	Tsol	260°C for 10s	—

Notes:

Never use wave soldering to mount packages, or any other method that applies excessive thermal stress to package, as this will reduce its heat dissipation capacity.

DC Characteristics

Ta = –20 to 75°C, V_{SS} = –5.0V ±10%, V_{DD} = 0V unless started otherwise

Parameter	Symbol	Condition	Pin	Rating			Unit
				Min.	Typ.	Max.	
Supply voltage (1)	V_{SS}		V_{SS}	–6.0	–5.0	–2.4	V
Recommended operating voltage	V_5		V_5	–12.0	—	–3.0	V
Permitted operating voltage. See note	V_5	Operating limits	V_5	–12.0	—	–2.5	V
Supply voltage (2)	V_2	Recommended value	V_2	1/2×V_5	—	V_{DD}	V
Supply voltage (3)	V_3	Recommended value	V_3	V_5	—	1/2×V_5	V

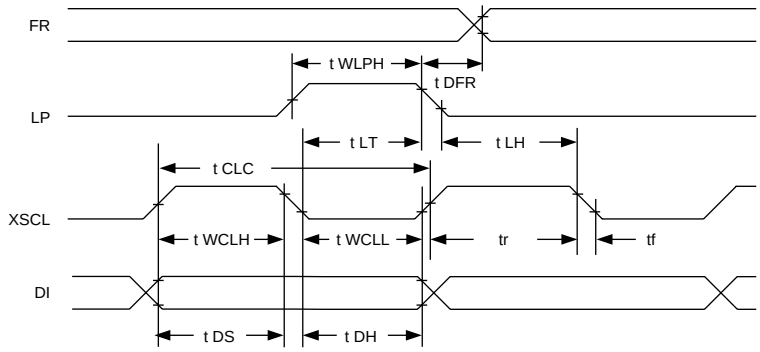
Parameter	Symbol	Condition		Rating			Unit	Pin
				Min.	Typ.	Max.		
"H" input voltage	V_{IH}			0.2V_{SS}	—	V_{DD}	V	DI, XSCL, LP, SHL, FR,
"L" input voltage	V_{IL}			V_{SS}	—	0.8V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH} = –0.6 mA		–0.4	—	—	V	D0
"L" output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V	
Input leakage current	I_{LI}	0V ≤ V_{IN} ≤ V_{SS}		—	0.05	2.0	µA	SHL, FR, XSCL, LP
Output leakage current	I_{LO}	0V ≤ V_{OUT} ≤ V_{SS}		—	0.05	5.0	µA	D0
Quiescent current	I_O	V5 = –12.0, V_{SS} = –6.0V V_{IH} = V_{DD}		—	0.05	30.0	µA	V_{DD}
Output resistance	R_{SEG}	|ΔV_{ON}| = 0.1V Ta = 25°C	V5=–8.0V	—	1.5	3.0	kΩ	SEG0 to SEG79
			V5=–5.0V	—	3.0	8.0		
			V5=–3.0V	—	10.0	50.0		
Supply current (1)	$I_{SS\ OP}$	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 400 kHz LP = 520 µs, FR period = 16.7 ms, all data inputs are alternate 1 and 0 data, all outputs open		—	250	350	µA	V_{SS}
Supply current (2)	I_{SOP}	V_{SS} = –4.5V, V2 = –4.8V, V3 = –7.2V, V_{SSH} = –12.0V Other conditions are for $I_{SS\ OP}$		—	10	16.0	µA	V_5
Input pin capacitance	C_I	Ta = 25 °C		—	5.0	8.0	pF	SHL, FR, XSCL, LP

Notes:

This parameter specifies the range of V_5 over which operation is possible. The driver ON-resistance for the particular LCD panel being used may result in V_5 exceeding the recommended operating range. The V_5 operating voltage should be determined experimentally and component changes made, if necessary, to ensure operation within the recommended range.

AC Characteristics

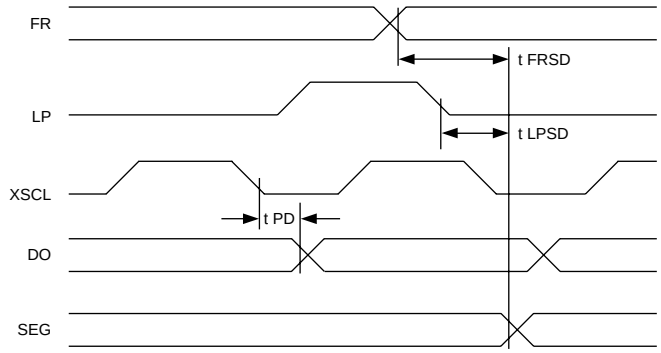
Input timing



Ta = –20 to 75°C, V_{SS} = –6.0 to –2.4V unless started otherwise

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
Shift clock period	t_{CLC}		1.0	—	µs
Shift clock HIGH-level pulse width	t_{WCLH}		450	—	ns
Shift clock LOW-pulse width	t_{WCLL}		450	—	ns
Data setup time	t_{DS}		140	—	ns
Data hold time	t_{DH}		100	—	ns
Latch pulse HIGH-level pulse width	t_{WLPH}		200	—	ns
Shift clock to latch pulse interval	t_{LT}		200	—	ns
Latch hold time	t_{LH}		100	—	ns
Frame signal delay time	t_{DFR}		–500	500	ns
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_f		—	50	ns

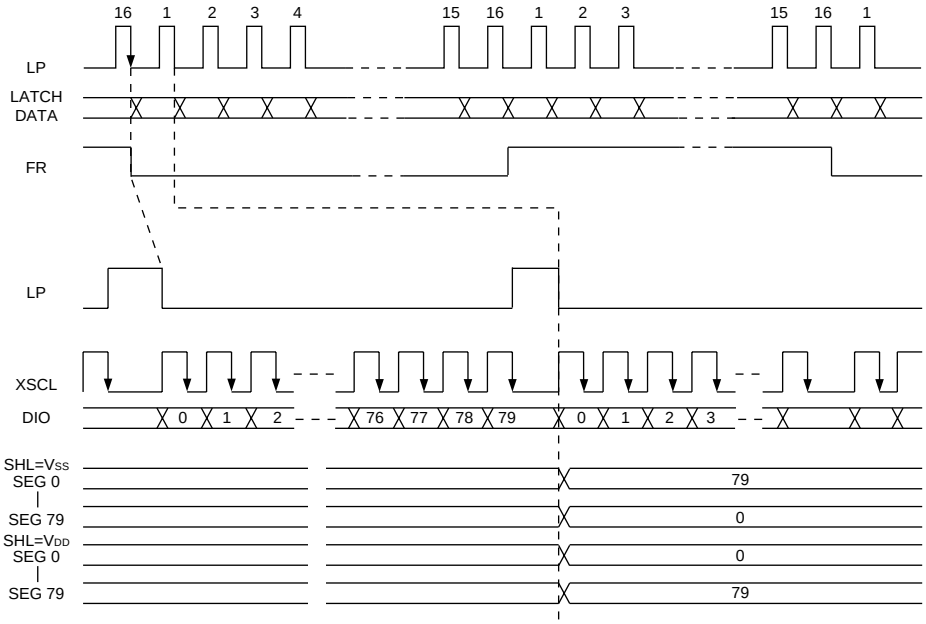
Output Timing

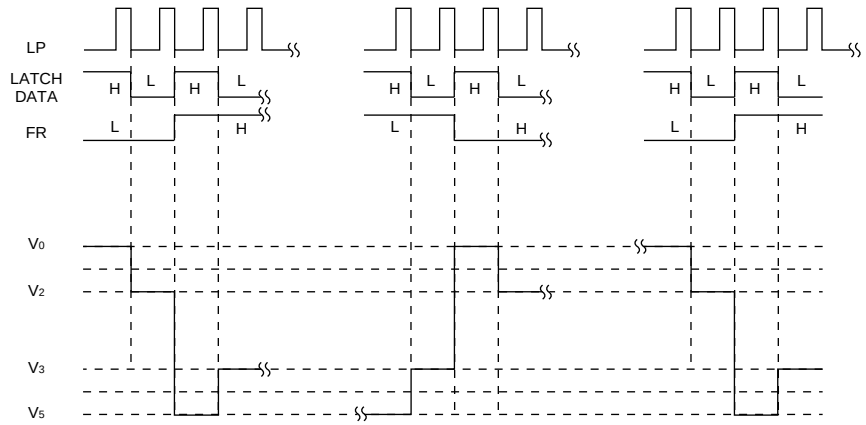


Ta = –20 to 75 °C, V_{SS} = –6.0 to –2.4V, V5 + –12.0 to –3.0V unless started otherwise

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
Serial data output delay time	t_{PD}	C_L = 15 pF	—	250	ns
LP to segment output delay time	t_{LPSD}	C_L = 100 pF	—	4.5	µs
FR to segment output delay time	t_{FRSD}		—	4.5	µs

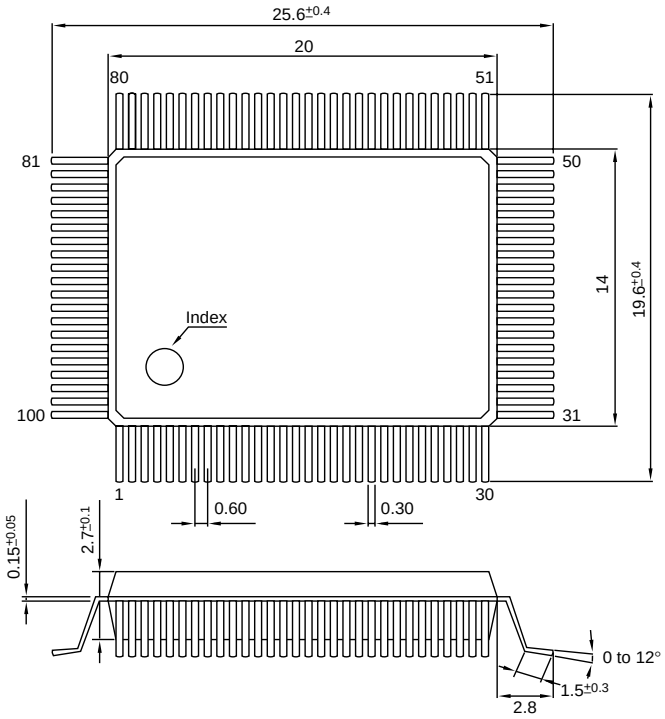
Timing Diagrams for 1/16 Duty Cycle





Package Dimensions

SED1681F0A



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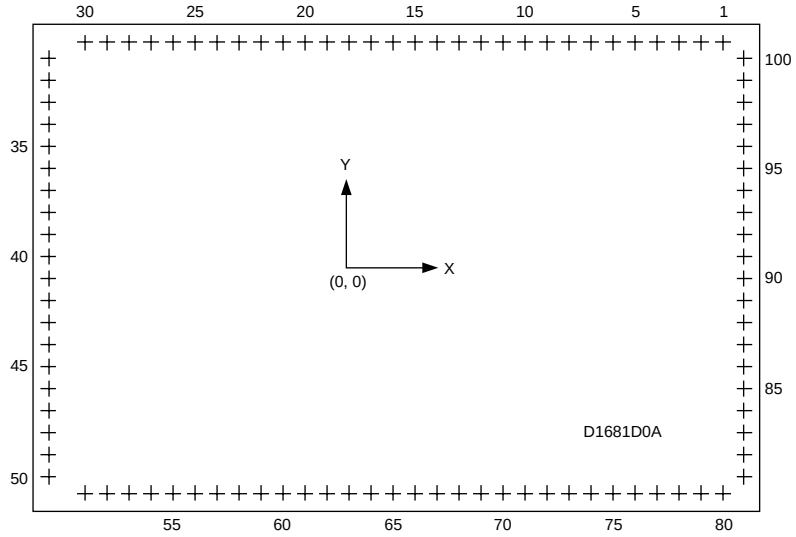


Chip Specification	Dimension [mm]
Chip size5.59×3.50	
Pad pitch0.160 min.	
Chip thickness	0.40 ±0.025
Pad size0.10×0.10	

Pad coordinates

Pad		X [µm]	Y [µm]
Number	Name		
1	SEG 29	2461	1588
2	28	2261	1588
3	27	2069	1588
4	26	1885	1588
5	25	1709	1588
6	24	1538	1588
7	23	1366	1588
8	22	1203	1588
9	21	1040	1588
10	20	880	1588
11	19	720	1588
12	18	560	1588
13	17	400	1588
14	16	240	1588
15	15	80	1588
16	14	–80	1588
17	13	–240	1588
18	12	–400	1588
19	11	–560	1588
20	10	–720	1588
21	9	–880	1588
22	8	–1040	1588
23	7	–1203	1588
24	6	–1366	1588
25	5	–1538	1588
26	4	–1709	1588
27	3	–1885	1588
28	2	–2069	1588
29	1	–2261	1588
30	0	–2461	1588
31	NC	–2632	1548
32	V_5	–2632	1374
33	V_0	–2632	1206
34	V_3	–2632	1040
35	V_2	–2632	881

Pad		X [µm]	Y [µm]
Number	Name		
36	V_{SS}	–2632	721
37	LP	–2632	561
38	NC	–2632	401
39	SHL	–2632	241
40	XSCL	–2632	81
41	DI	–2632	–79
42	DO	–2632	–239
43	NC	–2632	–399
44	FR	–2632	–559
45	NC	–2632	–719
46	V_{DD}	–2632	–879
47	NC	–2632	–1039
48	NC	–2632	–1204
49	NC	–2632	–1372
50	NC	–2632	–1546
51	SEG 79	–2461	–1588
52	78	–2261	–1588
53	77	–2069	–1588
54	76	–1885	–1588
55	75	–1709	–1588
56	74	–1538	–1588
57	73	–1366	–1588
58	72	–1203	–1588
59	71	–1040	–1588
60	70	–880	–1588
61	69	–720	–1588
62	68	–560	–1588
63	67	–400	–1588
64	66	–240	–1588
65	65	–80	–1588
66	64	80	–1588
67	63	240	–1588
68	62	400	–1588
69	61	560	–1588
70	60	720	–1588

Pad		X [µm]	Y [µm]
Number	Name		
71	SEG59	880	–1588
72	58	1040	–1588
73	57	1203	–1588
74	56	1366	–1588
75	55	1538	–1588
76	54	1709	–1588
77	53	1885	–1588
78	52	2069	–1588
78	51	2261	–1588
80	50	2461	–1588
81	49	2632	–1546
82	48	2632	–1372
83	47	2632	–1204
84	46	2632	–1039
85	45	2632	–879
86	44	2632	–719
87	43	2632	–559
88	42	2632	–399
89	41	2632	–239
90	40	2632	–79
91	39	2632	81
92	38	2632	241
93	37	2632	401
94	36	2632	561
95	35	2632	721
96	34	2632	881
97	33	2632	1041
98	32	2632	1206
99	31	2632	1374
100	30	2632	1548

APPLICATION NOTES

Power-on and Power-off

The SED1681 can be permanently damaged, by excessive input current, if the LCD driver supply voltage is applied before the logic supply voltage. To prevent this, ensure that the power-on and power-off sequence below is followed.

- Power-on

  Apply power to the logic circuitry (V_{SS}) BEFORE or at the same time as applying power to the driver circuitry.

- Power-off

  Remove power from the logic circuitry AFTER or at the same time as removing power from the driver circuitry.

  As an additional precaution against excessive current flow, insert a resistor of about 100Ω is series with V5.

LCD Drive Voltages

The simplest method for obtaining the LCD driver voltages is to use a resistive voltage divider, as shown in the figure below. The values os these resistors are a compromise between the stability required by the LCD and the capacity of the power supply. Since the optimum driver voltages vary with temperature, variable resistor VR should be used. Ensure that the maximum rating of the LCD supply voltage V5 is not exceeded when VR is short circuited.

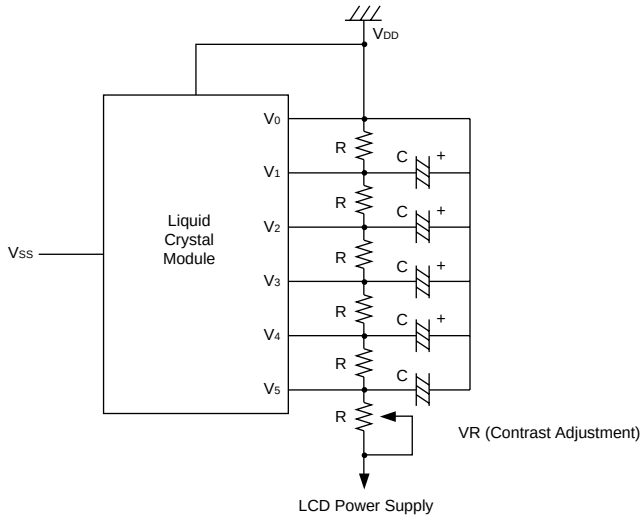


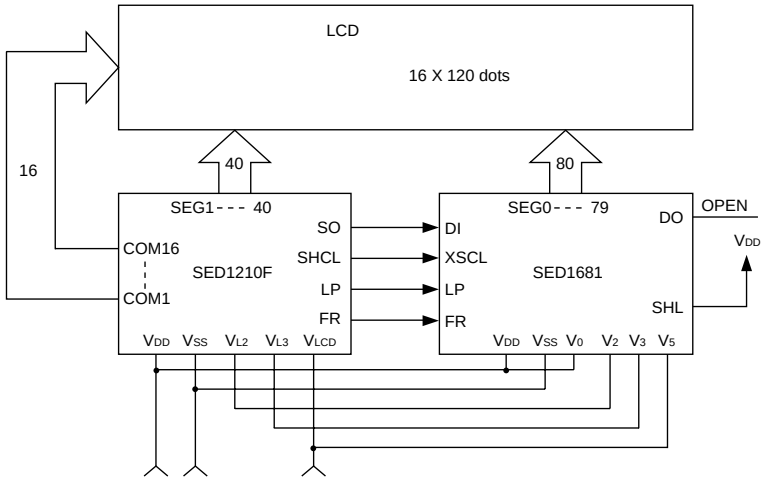
Figure 2. LCD Supply Voltages for 1/16 Duty Cycle

The LCD panel presents a highly capacitive load to the drivers. To reduce ringing of the driver output waveforms and to minimize problems such as reduced contrast and half-tone displays, the divider resistors should have as low a value as possible, as determined by the capacity of the power supply and the allowed power dissipation of the LCD module.

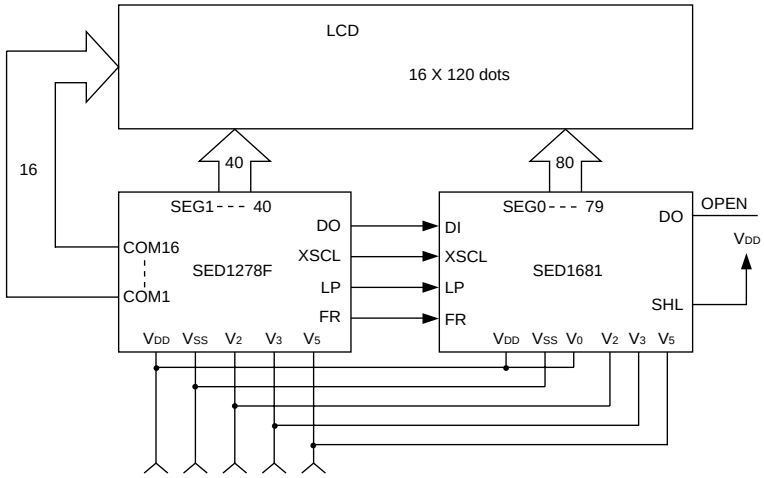
To reduce power supply noise use small-value bypass capacitors from each supply voltage to ground as shown in the figure above. Capacitor values should not be any larger than necessary.

TYPICAL APPLICATION CIRCUITS

Connection to SED1210F



Connection to SED1278F



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