3. SED1606
Dot Matrix LCD Segment Driver

CONTENTS

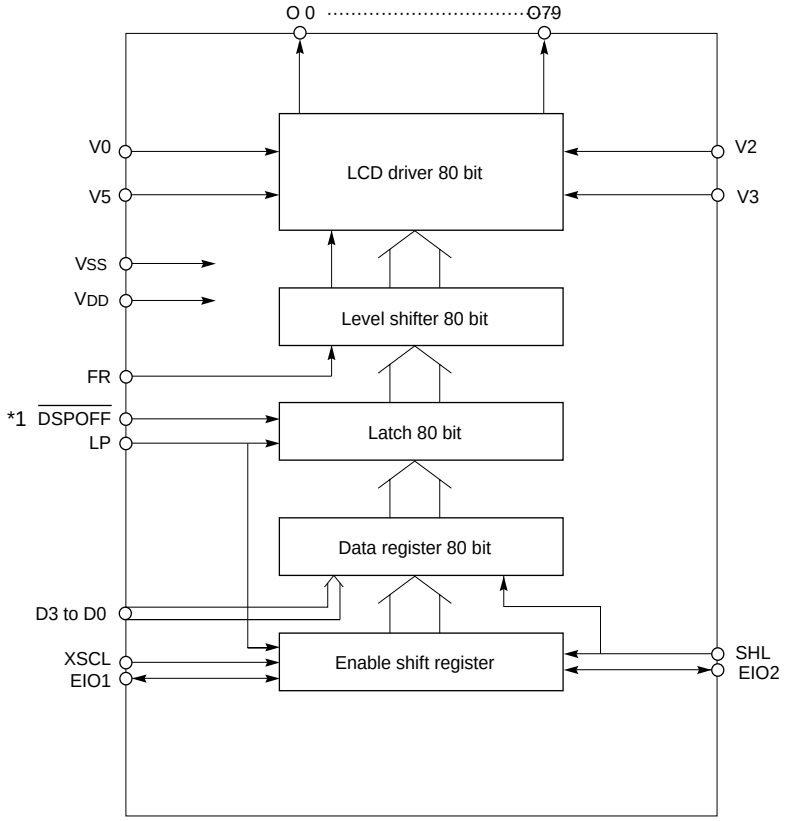
OVERVIEW

The SED1606 is an 80 output segment (column) driver which is suitable for driving a very high capacity dot-matrix LCD panels. It is intended to be used in conjunction with the SED1670/72 as a pair.
The SED1606 is featured in a high quality of picture in LCD display. It employs a high-speed enable chain system which is favorable to a low-power driving. Allowed to be operated with a low voltage in the logic system power supply, it can meet a wide range of applications.

FEATURES

- Number of LCD drive output segments: 80
- Low current consumption
- Low voltage operation: –2.7 V (Max.)
- Wide range of LCD drive voltages: –8 V to –28 V
- High-speed and low-power data transfer enabled by means of a 4-bit bus and chain enable support
  Shift clock frequency: 6.5 MHZ (at –2.7 V)
  10.0 MHZ (at –4.5 V)
- Selectable pin output shift direction
- Adjustable offset bias of LCD power to a V_{DD} level
- Logic system power supply : –2.7 V to –5.5 V
- Chip packaging
  SED1606D0A (AL-pad die form)
  SED1606D0B (Au bump die form)
  SED1606D1A (AL-pad die form)
  SED1606D1B (Au bump die form)
  PKG SED1606F0A (QFP5-100 pin)
- No radial rays countermeasure taken in designing

BLOCK DIAGRAM



1 Dummy terminal NC when SED1606D0 is used.
DSPOFF terminal when SED1606D1* is used

PIN DESCRIPTION

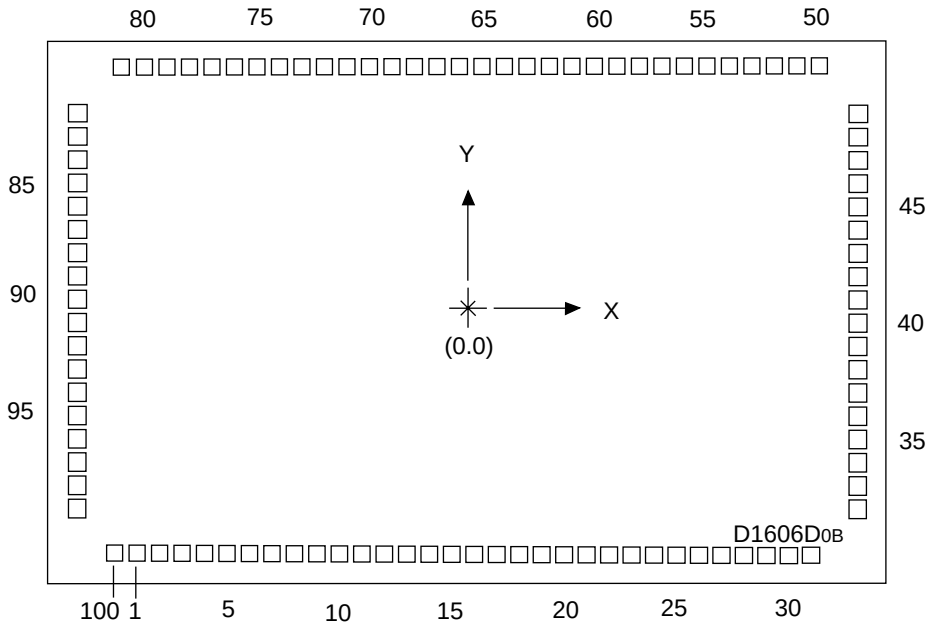
<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>O0 ~ O79</td><td>O</td><td>Segment (column) output for LCD driving
The output changes at the LP falling edge.</td><td>80</td></tr>
<tr><td>D0 ~ D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (Falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (Falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Enable input/output
To be set to input or output according to the SHL input level.
The output is reset by the LP input. Upon the end of fetching of 80-bit data, the system starts up automatically to “H”.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO pin I/O control input When data is input to (D3, D2 ... D0) pins sequentially in order of (a3, a2, a1, a0), (b3, b2, b1, b0) ... (t3, t2, t1, t0), the relationship between the data and segment output becomes as shown in the table below:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a3</td><td>b2</td><td>c1</td><td>. . .</td><td>t2</td><td>t1</td><td>t0</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>t0</td><td>t1</td><td>t2</td><td>. . .</td><td>a1</td><td>a2</td><td>a3</td><td>Input</td><td>Output</td></tr>
</table>
(Note) The relationship between the data and segment output is determined irrespective of the number of shift clock inputs.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output AC converted signal input</td><td>1</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>Force input of blank
V0 level is forcibly set by entering “L” level (available with SED1606D1∗ alone).</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V V_{SS}: –2.7 V to –5.5 V</td><td>2</td></tr>
<tr><td>V0, V2, V3, V5

*1</td><td>Power supply</td><td>LCD drive circuit power supply
V_{DD}: 0 V V_5: –8 V to –28 V
$V_{DD} \geq V_0 \geq V_2 \geq 6/9\ V_5$
$3/9\ V_5 \geq V_3 \geq V_5$
When used at a same potential, V_0 and V_{DD} are used by grounding them close to the IC chip.</td><td>4</td></tr>
</table>

*1 Be sure to connect V_0 to V_5 to their LCD power, respectively.

Total: 100
SED1606D0∗ (including four NC’4)
SED1606D1∗ (including four NC’3)

PAD LAYOUT AND COORDINATES



Chip size: ..... 5.59 mm × 3.50 mm
Pad pitch: ..... 0.153 mm (Min.)
Chip thickness: ..... 0.400 mm (AL-pad die form)
0.525 mm (Au-bump die form)

Au bump specifications [Reference values]

Bump size: 117μm × 109μm ± 20 um
Bump height: 17μm to 28μm (Details shall be stipulated in the delivery specification.)

AL-pad die form

Pad Opening 87×76μm

Unit (μm)

PAD		Actual dimensions	
NO.	NAME	X	Y
1	O0	–2227	–1578
2	O1	–2073	
3	O2	–1920	
4	O3	–1766	
5	O4	–1612	
6	O5	–1459	
7	O6	–1305	
8	O7	–1152	
9	O8	–998	
10	O9	–845	
11	O10	–691	
12	O10	–537	
13	O12	–384	
14	O13	–230	
15	O14	–76	
16	O15	77	
17	O16	231	
18	O17	384	
19	O18	538	
20	O19	692	
21	O20	845	
22	O21	999	
23	O22	1152	
24	O23	1306	
25	O24	1460	
26	O25	1613	
27	O26	1767	
28	O27	1921	
29	O28	2074	
30	O29	2228	
31	O30	2381	
32	O31	2622	–1346
33	O32		–1188
34	O33		–1029

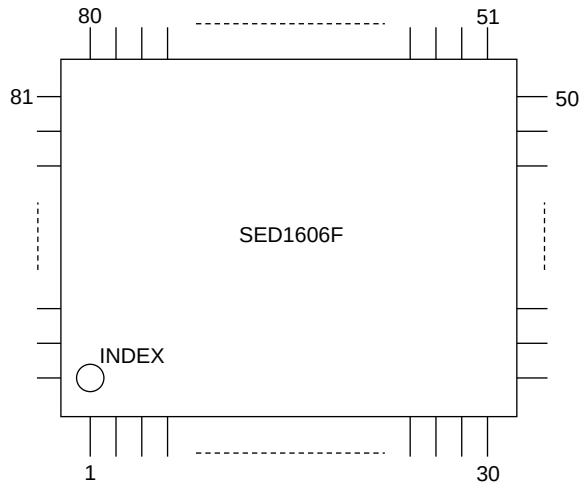
PAD		Actual dimensions	
NO.	NAME	X	Y
35	O34	2622	–871
36	O35		–713
37	O36		–554
38	O37		–396
39	O38		–238
40	O39		–79
41	O40		79
42	O41		238
43	O42		396
44	O43		554
45	O44		713
46	O45		871
47	O46		1029
48	O47		1188
49	O48		1346
50	O49	2381	1578
51	O50	2228	
52	O51	2074	
53	O52	1921	
54	O53	1767	
55	O51	1613	
56	O55	1460	
57	O56	1306	
58	O57	1152	
59	O58	999	
60	O59	845	
61	O60	692	
62	O61	538	
63	O62	384	
64	O63	231	
65	O64	77	
66	O65	–76	
67	O66	–230	
68	O67	–384	

PAD		Actual dimensions	
NO.	NAME	X	Y
69	O68	–537	1578
70	O69	–691	
71	O70	–846	
72	O71	–998	
73	O72	–1152	
74	O73	–1305	
75	O74	–1459	
76	O75	–1613	
77	O76	–1766	
78	O77	–1920	
79	O78	–2073	
80	O79	–2227	
81	EIO2	–2381	
82	D0	–2622	1346
83	D1		1192
84	D2		1039
85	D3		885
86	Dummy		732
87	Dummy		578
88	Dummy		424
89	*1		271
90	V_{DD}		106
91	V_{SS}		–58
92	V0		–224
93	V2		–389
94	V3		–553
95	V5		–718
96	SHL	–2611	–885
97	XSCL		–1039
98	LP		–1192
99	FR		–1346
100	EIO1	–2381	–1578

1: Pad No.89 is dummy when SED1606D0 is used.
It will be DSPOFF with SED1606D1*.

PIN LAYOUT

Package Type: QFP–5 100pin



PIN No.	NAME	PIN No.	NAME	PIN No.	NAME	PIN No.	NAME	PIN No.	NAME
1	O0	21	O20	41	O40	61	O60	81	EIO2
2	O1	22	O21	42	O41	62	O61	82	D0
3	O2	23	O22	43	O42	63	O62	83	D1
4	O3	24	O23	44	O43	64	O63	84	D2
5	O4	25	O24	45	O44	65	O64	85	D3
6	O5	26	O25	46	O45	66	O65	86	NC
7	O6	27	O26	47	O46	67	O66	87	NC
8	O7	28	O27	48	O47	68	O67	88	NC
9	O8	29	O28	49	O48	69	O68	89	*1
10	O9	30	O29	50	O49	70	O69	90	V_{DD}
11	O10	31	O30	51	O50	71	O70	91	V_{SS}
12	O11	32	O31	52	O51	72	O71	92	V0
13	O12	33	O32	53	O52	73	O72	93	V2
14	O13	34	O33	54	O53	74	O73	94	V3
15	O14	35	O34	55	O54	75	O74	95	V5
16	O15	36	O35	56	O55	76	O75	96	SHL
17	O16	37	O36	57	O56	77	O76	97	XSCL
18	O17	38	O37	58	O57	78	O77	98	LP
19	O18	39	O38	59	O58	79	O78	99	FR
20	O19	40	O39	60	O59	80	O79	100	EIO1

1: Pad No.89 is dummy when SED1606D0 is used.
It will be DSPOFF with SED1606D1*.

FUNCTIONAL DESCRIPTION

Enable shift register

This is a bidirectional shift register with which the shift direction is selected by SHL input. The output of this shift register is used to store the data bus signals to data register.
When the enable signal is in the disable status, the internal clock signal and data bus are fixed to "L" and the system is made into the power save mode.
When using two or more segment drivers, connect the EIO pin of each driver in a cascade arrangement and the EIO pin of the leading driver to "V_{DD}".
Since the enable controller circuit automatically detects that the data for 80 bits have been fetched thoroughly and then transfers the enable signal to the controller, it is not necessary to provide the control signal using the control LSI.

Data register

This is a register used to convert the data bus signal into serial or parallel signal through the enable shift register output. Consequently, the relationship between the serial display data and segment output is determined irrespective of the number of shift clock inputs.

Latch

This latch is used to fetch the content of data register at the LP falling edge trigger and to send its output to the level shifter.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver

This driver outputs the LCD drive voltage.
The relationship among the data bus signal, AC converted signal FR and segment output voltage is as shown in the table below:

(SED1606D0*)

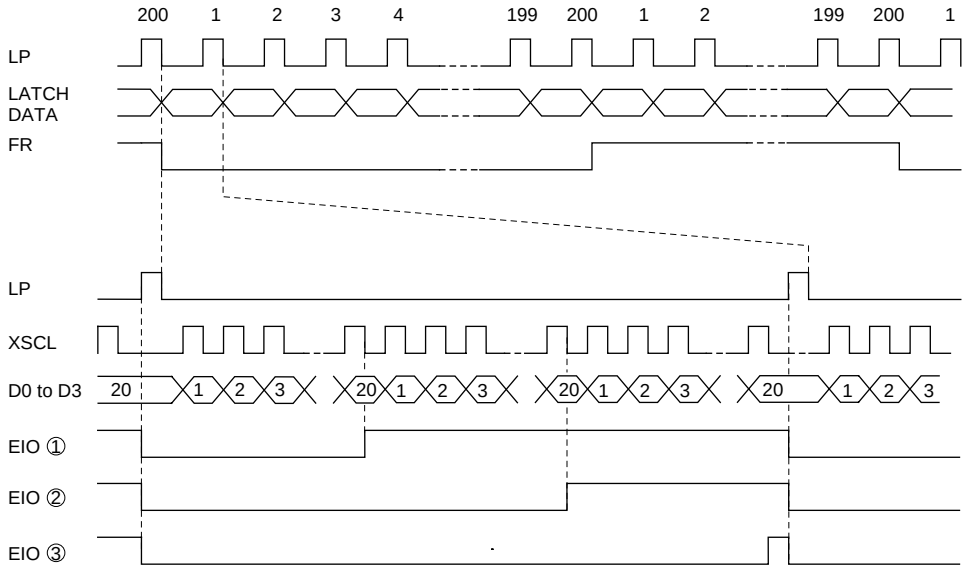
Data bus signal	FR	O output voltage
H	H	V_0
	L	V_5
L	H	V_2
	L	V_3

(SED1606D1*)

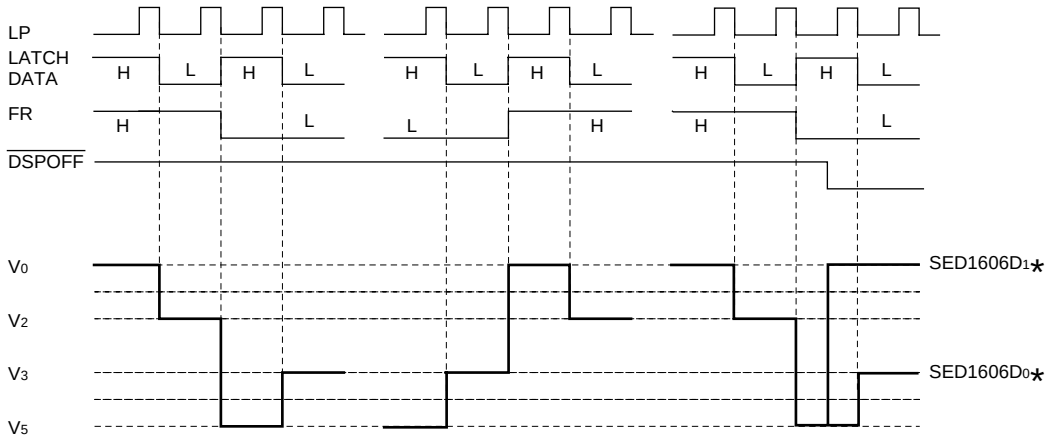
$\overline{DSPOFF}$	Data bus signal	FR	O output voltage
H	H	H	V_0
		L	V_5
H	L	H	V_2
		L	V_3
L	—	—	V_0

TIMING CHART

When the duty is 1/200 (Reference Example)



① to ③ stand for a cascaade No. of driver.



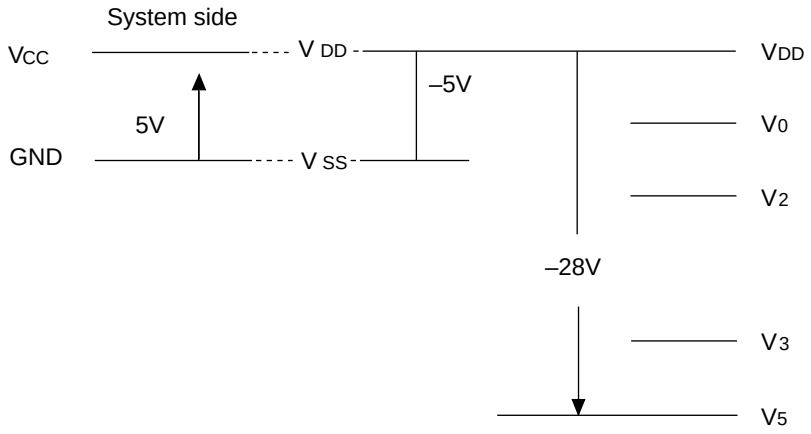
When SED1606D1* is used:
The driver output is forcibly switched to
V0 output upon switching of $\overline{\text{DSPOFF}}$

ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V_5	–30.0 to +0.3	V
Power voltage (3)	V_0, V_2, V_3	V_5–0.3 to V_{DD}+0.3	V
Input voltage	V_I	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage	V_O	V_{SS}–0.3 to V_{DD}+0.3	V
EIO output current	I_O	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg 1	–65 to +150	°C

Notes:
1. The storage temperature 1 stipulates the temperature by unit of a chip.
2. The voltage of V_0, V_2 and V_3 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$.



3. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.

ELECTRICAL CHARACTERISTICS

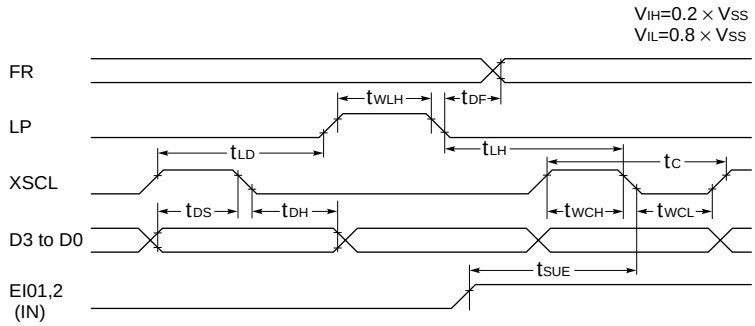
DC characteristics

Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V±10% and Ta = –40 to 85°C.

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–		–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	V_{SS}=–2.7 to –5.5V		–28.0	–	–12.0	V	V_5
Operation enable voltage	V_5	Function		–	–	–8.0	V	V_5
Supply voltage (2)	V_0	Recommended value		V_{DD}–2.5	–	V_{DD}	V	V_0
Supply voltage (3)	V_2	Recommended value		3/9V_5	–	–	V	V_2
Supply voltage (4)	V_3	Recommended value		V_5	–	6/9V_5	V	V_3
"H" input voltage	V_{IH}	V_{SS}=–2.7 to –5.5V		0.2V_{SS}	–	–	V	EIO1, EIO2, FR, D0 to D3, XSCL, SHL, LP
"L" input voltage	V_{IL}			–	–	0.8V_{SS}	V	
"H" output voltage	V_{OH}	V_{SS}=–2.7 to –5.5V	I_{OH}=–0.6mA	V_{DD}–0.4	–	–	V	EIO1, EIO2
"L" output voltage	V_{OL}		I_{OL}=0.6mA	–	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		–	–	2.0	µA	D0 to D3, LP, FR XSCL, SHL
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$		–	–	5.0	µA	EIO1, EIO2
Static current	I_{SS}	V5=–28.0 to –14.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}		–	–	25	µA	V_{SS}
Output resistance	R_{SEG}	ΔV_{ON}=0.5V V_5=–20.0V V_3=13/15·V_5 V_2=2/15·V_5 V_0=V_{DD} Ta=25°C		–	1.2	1.6	KΩ	O0 to O79
Average operating current consumption (1)	I_{SS}	V_{SS}=–5.0V, V_{IH}=V_{DD} V_{IL}=V_{SS}, f_{XSCL}=2.69MHz f_{LP}=16.8KHz, f_{FR}=70Hz Input data: Dice display at no load		–	0.10	0.2	mA	V_{SS}
		V_{SS}=–3.0V Other conditions are the same as V_{SS} = -5 V		–	0.07	0.15		
Average operating current consumption (2)	I_5	V_{SS}=–5.0V, V_0=0.0V, V_2=–9.3V V_3=–18.6V, V_5=–28.0V Other conditions are the same as in the item of I_{SS}.		–	0.05	0.08	mA	V_5
Input pin capacitance	C_I	Freq.=1MHz Ta=25°C By unit of a chip		–	–	8	pF	D0 to D3, LP, FR XSCL, SHL
Input/output pin capacitance	$C_{I/O}$			–	–	15	pF	EIO1, EIO2

AC CHARACTERISTICS

Input timing characteristics



VSS=–5.0V±0.5V, Ta=–40 to 85°C

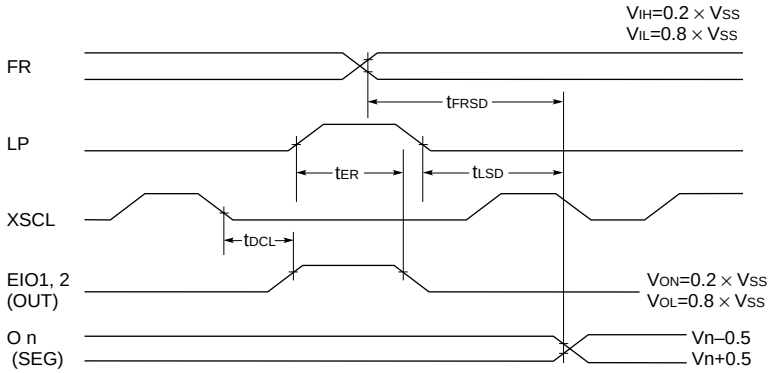
Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	t_C	–	100	–	ns
XSCL “H” pulsewidth	t_{WCH}	–	30	–	ns
XSCL “L” pulsewidth	t_{WCL}	–	30	–	ns
Data setup time	t_{DS}	–	20	–	ns
Data hold time	t_{DH}	–	10	–	ns
XSCL-rise to LP-rise time	t_{LD}	–	0	–	ns
LP-fall to XSCL-fall time	t_{LH}	–	40	–	ns
LP “H” pulsewidth	t_{WLH}	*3	40	–	ns
Allowable FR delay time	t_{DF}	–	–900	+900	ns
EIO setup time	t_{SUE}	–	35	–	ns

VSS=–4.5V to –2.7V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
XSCL period	t_C	VSS=–2.7V *1	153	–	ns
		VSS=–3.0V *2	133	–	
XSCL “H” pulsewidth	t_{WCH}	–	50	–	ns
XSCL “L” pulsewidth	t_{WCL}	–	50	–	ns
Data setup time	t_{DS}	–	30	–	ns
Data hold time	t_{DH}	–	15	–	ns
XSCL-rise to LP-rise time	t_{LD}	–	0	–	ns
LP-fall to XSCL-fall time	t_{LH}	VSS=–2.7V	75	–	ns
		VSS=–3.0V	65	–	
LP “H” pulsewidth	t_{WLH}	VSS=–2.7V *3	75	–	ns
		VSS=–3.0V *3	65	–	
Allowable FR delay time	t_{DF}	–	–900	+900	ns
EIO setup time	t_{SUE}	VSS=–2.7V	60	–	ns
		VSS=–3.0V	51	–	

*1 Equivalent to 6.5 MHz
*2 Equivalent to 7.5 MHz
*3 t_{WLH} stipulates the time when LP is “H” and XSCL is “L”.
*4 t_r and t_f of input signal are stipulated by unit of 20 ns.
*5 At a high-speed operation, t_r and t_f = {t_C – (t_{DCL} + t_{SUE})}/2

Output timing characteristics



V_{DD}=–5.0±0.5V, V_5=–12.0 to –28.0V

Parament	Symbol	Condition	Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)	–	90	ns
EIO output delay time	t_{DCL}		–	55	ns
LP to SEG output delay time	t_{LSD}	C_L=100pF (On)	–	200	ns
FR to SEG output delay time	t_{FRSD}		–	400	ns

V_{DD}=–4.5V to 2.7V, V_5=–12.0 to –28.0V

Parament	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)		–	150	ns
EIO output delay time	t_{DCL}		V_{SS}=–2.7V	–	88	ns
			V_{SS}=–3.0V	–	77	ns
LP to SEG output delay time	t_{LSD}	C_L=100pF (On)		–	400	ns
FR to SEG output delay time	t_{FRSD}			–	800	ns

*1 t_r and t_f of input signal are stipulated by unit of 20 ns.
*2 At a high-speed operation, t_r and t_f = {t_C – (t_{DCL} + t_{SUE})}/2

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is optimum to divide the resistance of potential between V_5 and V_{DD} to drive the LCD using the voltage follower with an operational amplifier. In taking into consideration of such a case using the operational amplifier, the maximum potential level V_0 for LCD driving has been made a separate pin from V_{DD}.
When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD}.

When no operational amplifier is used, connect V_0 and V_{DD} close to the IC chip.
When a series resistance exists in the power supply line of V_5 and V_{DD}, a voltage drop of V_5 and V_{DD} occurs at the LSI power supply pin, the relationship with the LCD's intermediate potential ($V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5$) cannot be met, this causing the LSI to be broken down in some cases. When a protection resistor is inserted, it is necessary to stabilize the voltage by capacitance.

Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating or above V_{SS} = –2.6 V, and when the LCD driving signal is output before the applied voltage to the LCD driving system is stabilized, an overcurrent flows and LSI breaks down in some cases.

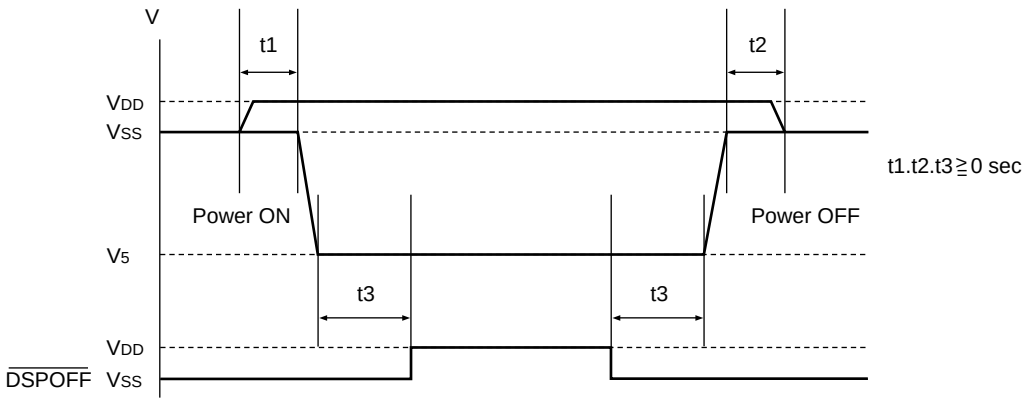
Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF .. LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

For a countermeasure to such overcurrent, it is effective to put a high-speed melting fuse or protection resistor in series with the LCD power unit.
It is then required to select the optimum value in the protection resistance according to the capacitance of LC cell.

Until the LCD driver voltage stabilizes. It is recommended to set the LCD driver output potential to V0 using the display off function (DSPOFF).

Power ON/OFF sequence when SED1606D1∗ is used



TYPICAL CIRCUIT DIAGRAM

Configuration Drawing of Large Screen LCD