5. SED1640
LCD Driver

CONTENTS

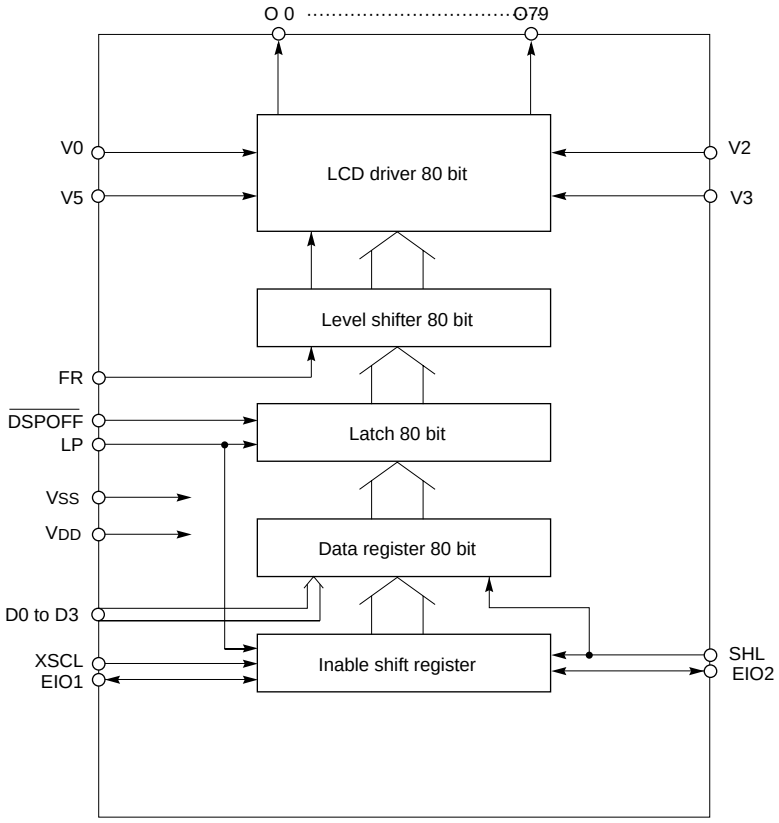
DESCRIPTION

The SED1640 is an 80 output segment (column) driver for use in combination with an SED1670/72.
It is provided with high-vision measure of the LCD display and adopts high speed inable chain system for low power operation and slim chip shape suitable for minimizing of the LCD panel. Also, low voltage operation of the logic power source suits a wide range of applications.

FEATURES

- LCD driver output number : 80
- Ultra-slim chip
- Low current consumption
- Low voltage operation : –2.7V max.
- Wide range of liquid crystal drive voltage : –8 to –28V
- High speed and low power data transfer is possible by adoption of the 4 bit bus inable chain system.
  Shift clock frequency
  6.5MHz (at –2.7V)
  7.5MHz (at –3.0V)
- Non-bias display off function
- Pin selection of the output shift direction is available.
- Offset bias regulation of the liquid crystal power is possible depending on the V_{DD} level.
- Logic system power source : –2.7V to –5.5V
- Product shapes
  Chip : SED1640D0B (Au bump article)
  Tab : SED1640T** (to be decided)

BLOCK DIAGRAM



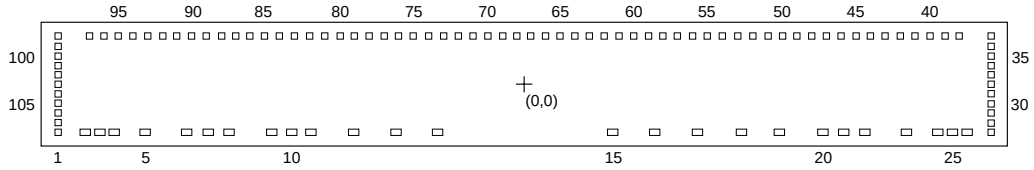
FUNCTIONS OF THE TERMINALS

<table>
<tr><th>Terminal names</th><th>I/O</th><th>Functions</th><th>Numbers of terminals</th></tr>
<tr><td>O0 ~ O79</td><td>O</td><td>LCD driving segment (column) output.
The output level varies by the trailing edge of the LP.</td><td>80</td></tr>
<tr><td>D0 ~ D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse input of display data (trailing edge trigger)</td><td>1</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Inable input and output.
Set to input or output depending on the SHL input level.
The output is reset by the LP input and, after receiving 80 bit data, it automatically rises to “H”.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shifting direction choice and input/output controlling input to the EIO terminal.
When data are input to (D3, D2 ...D0) terminals in the order of (a,b,c,d,e,f,g,h).....(w,x,y,z), relations between data and segment outputs are as follows:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">O Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>. . .</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>. . .</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>OUtput</td></tr>
</table>
(Note) Relations between data and segment outputs are determined independent from the shift clock number.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Input of the alternating signal of the LCD drive output.</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power source</td><td>Power supply for the logics V_{DD} : 0V
V_{SS} : –2.7 ~ –5.5V</td><td>3</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power source</td><td>Power supply for the LCD driver circuit
V_{DD} : 0V V_5 : –8 ~ –28V
$V_{DD} \geqq V_0 \geqq V_2 \geqq 6/9\ V_5$
*1 $3/9\ V_5 \geqq V_3 \geqq V_5$</td><td>8</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>Forced blank input
At the “L” level, it forces the output to V0 level.
* When using this function, the unit may be used in common with SED1670∗/∗.</td><td>1</td></tr>
</table>

*1 Be sure to connect pairs of V0 - V5 to respective LCD power sources.

Total 107 (including NC5)

PAD LAYOUT



Chip size ..... 11.59mm x 1.40mm
Pad pitch ..... 105µm (Min.)
Chip thickness ..... 625µm ±25µm

Au bump specification (SED1640D0B) reference values

Bump size	A	160µm × 80µm ±4µm	(Pad No. 2 ~ 26)
Bump size	B	86µm × 91µm ±4µm	(Pad No. 1, 27, 37 and 98)
Bump size	C	86µm × 68µm ±4µm	(Pad No. 28 ~ 36 and 99 ~ 107)
Bump size	D	82µm × 74µm ±4µm	(Pad No. 38 ~ 97)
Bump height	A ~ D	22.5 ±5.5µm	(Pad No. 1 ~ 107)

PAD COORDINATES

PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates
2	V0	–5345	–541
3	V2	–5164	
4	V3	–4984	
5	V5	–4594	
6	V_{SS}	–4091	
7	Dummy	–3839	
8	SHL	–3587	
9	Dummy	–3065	
10	Dummy	–2828	
11	V_{DD}	–2590	
12	$\overline{DSPOFF}$	–2086	
13	FR	–1583	
14	LP	–1079	
15	XSCL	1079	
16	D0	1583	
17	D1	2086	
18	D2	2590	
19	Dummy	3065	
20	D3	3587	
21	Dummy	3839	
22	V_{SS}	4091	
23	V5	4594	
24	V3	4984	
25	V2	5164	
26	V0	5345	
27	EIO1	5644	–544
28	O0		–426
29	O1		–320
30	O2		–215
31	O3		–109
32	O4		–4
33	O5		102
34	O6		207
35	O7		313
36	O8		418
37	O9		546

PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates
38	O10	5269	553
39	O11	5090	
40	O12	4912	
41	O13	4733	
42	O14	4554	
43	O15	4376	
44	O16	4197	
45	O17	4019	
46	O18	3840	
47	O19	3661	
48	O20	3483	
49	O21	3304	
50	O22	3126	
51	O23	2947	
52	O24	2768	
53	O25	2590	
54	O26	2411	
55	O27	2233	
56	O28	2054	
57	O29	1875	
58	O30	1697	
59	O31	1518	
60	O32	1340	
61	O33	1161	
62	O34	982	
63	O35	804	
64	O36	625	
65	O37	447	
66	O38	268	
67	O39	89	
68	O40	–89	
69	O41	–268	
70	O42	–447	
71	O43	–625	
72	O44	–804	
73	O45	–982	

PAD NO.	PAD NAME	X-axis of coordinates	Y-axis of coordinates
74	O46	–1161	553
75	O47	–1340	
76	O48	–1518	
77	O49	–1697	
78	O50	–1875	
79	O51	–2054	
80	O52	–2233	
81	O53	–2411	
82	O54	–2590	
83	O55	–2768	
84	O56	–2947	
85	O57	–3126	
86	O58	–3304	
87	O59	–3483	
88	O60	–3661	
89	O61	–3840	
90	O62	–4019	
91	O63	–4197	
92	O64	–4376	
93	O65	–4554	
94	O66	–4733	
95	O67	–4912	
96	O68	–5090	
97	O69	–5269	
98	O70	–5644	546
99	O71		418
100	O72		313
101	O73		207
102	O74		102
103	O75		–4
104	O76		–109
105	O77		–215
106	O78		–320
107	O79		–426
1	EIO2		–544

FUNCTIONS

Inable shift registor

The inable shift registor is a bidirectional shift registor wherewith the shift direction is determined by the SHL inputs and outputs of such shift registor are used to store data bus signals to the data registor. When inable signals are in the disable state, the internal clock signal and data bus are fixed to "L" to become the power save mode.
When using multiple units of the segment driver, EIO terminals of each driver should be connected by the cascade connection and the EIO terminals of the top end driver should be connected to "V_{DD}". (Refer to the example of the connection) Since the inable control circuit automatically detects when all the 80 bit data are taken in and automatically transfers the inable signal, control signals from a controlling LSI are not needed.

Data registor

This is a registor for serial and parallel conversion of data bus signals by means of the inable shift registor output. Consequently, the relations between the serial display data and segment outputs are determined independent from the shift clock input number.

Latch

It takes in the contents of the data registor by means of the trailing edge trigger of the LP to transmit the output to the level shifter.

Level shifter

This is a level interface circuit to convert the voltage level of signals from logic level to LCD driving level.

LCD driver

It outputs the LCD drive voltage.
Relations among data bus signals, alternating signals FR and the segment output voltage are given below.

$\overline{DSPOFF}$	Data bus signals	FR	O Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_0

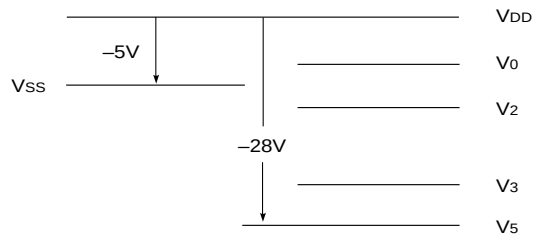
ABSOLUTE MAXIMUM RATING

Items	Symbols	Ratings	Unit
Power voltage (1)	V_{SS}	–7.0 ~ +0.3	V
Power voltage (2)	V_5	–30.0 ~ +0.3	V
Power voltage (3)	V_0, V_2, V_3	V_5–0.3 ~ V_{DD}+0.3	V
Input voltage	V_I	V_{SS}–0.3 ~ V_{DD}+0.3	V
Output voltage	V_O	V_{SS}–0.3 ~ V_{DD}+0.3	V
EIO output current	I_{O1}	20	mA
Working temperature	Topr	–40 ~ +85	°C
Storing temperature 1	Tstg 1	–65 ~ +150	°C
Storing temperature 2	Tstg 2	–55 ~ +100	°C

Note 1) All the above voltage is based on V_{DD} = 0V.

Note 2) The storing temperature 1 specifies that of chips proper and the storing temperature 2 specifies that of TAB packages.

Note 3) Voltage of V_0, V_2 and V_3 should always be maintained under a condition of $V_{DD} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5$.



Note 4) When logic power becomes floating state or if V_{SS} = –2.6 or beyond while the LCD driver power source is being applied, the LSI may be permanently damaged and avoid such circumstances.
Pay extra attention to the power sequence at times of turning on and turning off the power supply.

ELECTRICAL CHARACTERISTICS

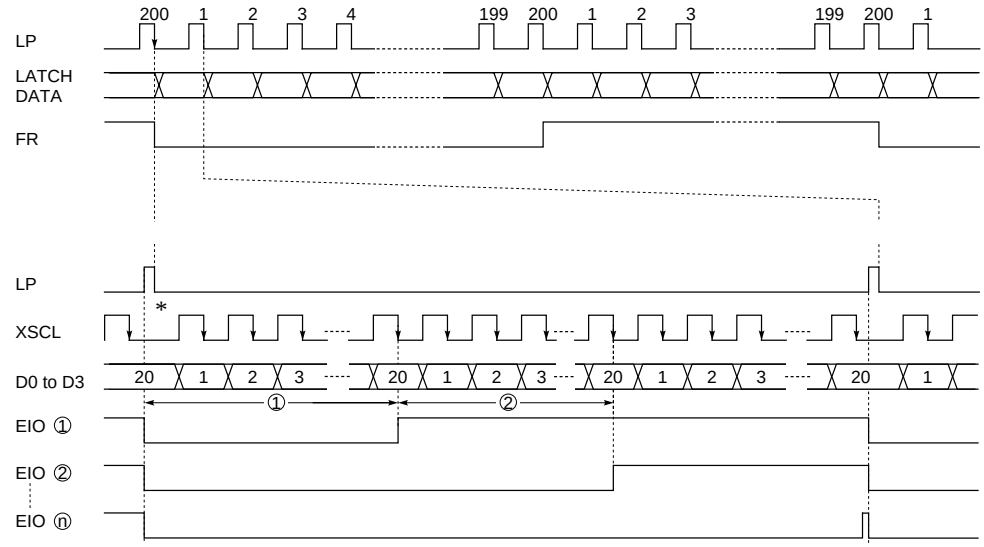
DC characteristics

Unless otherwise designated, V_{DD} = V0 = 0V, V_{SS} = –5.0V±10% and Ta = –40 to 85°C.

Items	Symbols	Conditions	Applicable terminals	Min.	Typ.	Max.	Unit
Power voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V_5	V_{SS}=–2.7 ~ –5.5V	V_5	–28.0		–12.0	V
Operatable voltage	V_5	Function	V_5			-8.0	V
Power voltage (2)	V_0	Recommended value	V_0	V_{DD}–2.5		V_{DD}	V
Power voltage (3)	V_2	Recommended value	V_2	3/9V_5			V
Power voltage (4)	V_3	Recommended value	V_3	V_5		6/9V_5	V
High level input voltage	V_{IH}	V_{SS}=–2.7 ~ –5.5V	EIO1, EIO2, FR, D0 ~ D3, XSCL, SHL, LP, $\overline{DSPOFF}$	0.2V_{SS}			V
Low level input voltage	V_{IL}					0.8V_{SS}	V
High level output	V_{OH}	V_{SS}=–2.7 ~ –5.5V, I_{OH}=–0.6mA	EIO1, EIO2	V_{DD}–0.4			V
Low level output voltage	V_{OL}	I_{OL}=0.6mA				V_{SS}+0.4	V
Input leak current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{DD}$	D0 ~ D3, LP, FR XSCL, SHL, $\overline{DSPOFF}$			2.0	µA
Input and output leak current	$I_{LI/O}$	$V_{SS} \leqq V_{IN} \leqq V_{DD}$	EIO1, EIO2			5.0	µA
Rest current	I_{SS}	V5=–28.0 ~ –14.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	V_{SS}			25	µA
Output resistance	R_{SEG}	ΔVON=0.5V V_5=–20.0V V_3=13/15•V5 V_2=2/15•V5 V_0=V_{DD}	O 0 ~ O 79		1.5	2.5	KΩ
Average operating current consumption (1)	I_{SS}	V_{SS}=–5.0V, V_{IH}=V_{DD} V_{IL}=V_{SS}, f_{XSCL}=2.69MHz f_{LP}=16.8KHz, f_{FR}=70Hz Input data: Diced display no-load	V_{SS}		0.10	0.2	mA
		V_{SS}=–3.0V Other conditions are the same as with V_{SS} =–5V			0.07	0.15	
Average operating current consumption (2)	I_5	V_{SS}=–5.0V, V_0=0.0V, V_2=–9.3V, V_3=–18.6V, V_5=–28.0V Other conditions are the same as with the item I_{SS}.	V5		0.02	0.05	mA
Input terminal capacity	C_I	Freq.=1MHz Ta=25°C Chips proper	D0 ~ D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$			8	pF
Input and output terminal capacity	$C_{I/O}$		EIO1, EIO2			15	pF

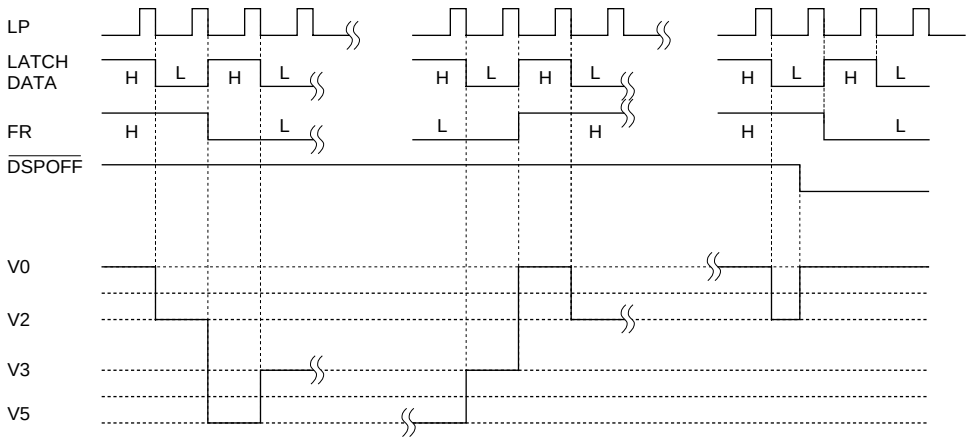
TIMING DIAGRAM

In case of 1/200 duty (an example)



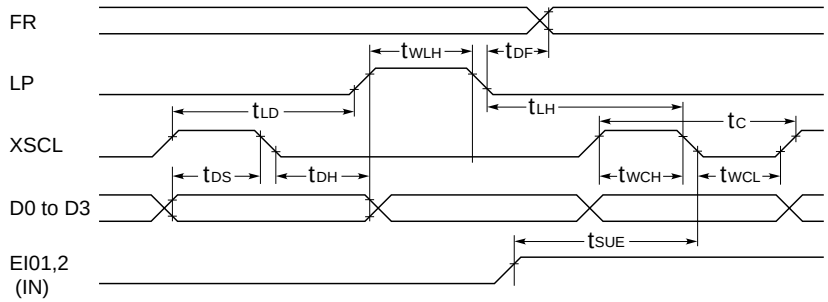
① ~ ⓝ indicate the cascade numbers of drivers.

* In case of high speed data transfer, it is necessary to secure a longer XSCL cycle in the timing of the LP pulse insertion in order to maintain the specified value of LP → XSCL (t_{LH}).



AC CHARACTERISTICS

Input timing characteristics



V_{SS}=–5.0V±0.5V, Ta=–40 ~ 85°C

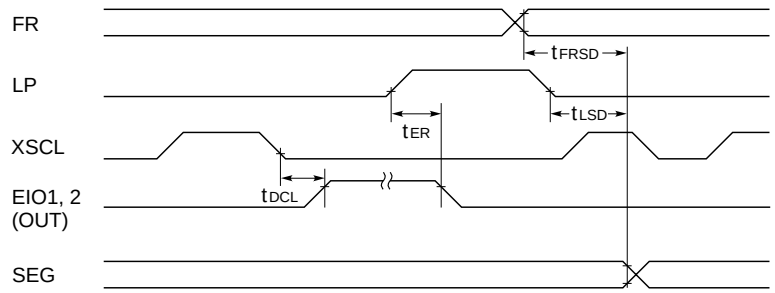
Items	Symbols	Conditions	Min.	Max.	Unit
XSCL cycle	t_C		100		ns
XSCL high level pulse duration	t_{WCH}		30		ns
XSCL low level pulse duration	t_{WCL}		30		ns
Data setup time	t_{DS}		30		ns
Data hold time	t_{DH}		20		ns
XSCL → LP rise time	t_{LD}		0		ns
LP → XSCL fall time	t_{LH}		40		ns
LP high level pulse duration	t_{WLH}	*3	40		ns
FR delay permissible time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}		35		ns

V_{SS}=–4.5V ~ 2.7V, Ta=–40 ~ 85°C

Items	Symbols	Conditions	Min.	Max.	Unit
XSCL cycle	t_C	V_{SS}=–2.7V *1	153		ns
		V_{SS}=–3.0V *2	133		
XSCL high level pulse duration	t_{WCH}		50		ns
XSCL low level pulse duration	t_{WCL}		50		ns
Data setup time	t_{DS}		50		ns
Data hold time	t_{DH}		30		ns
XSCL → LP rise time	t_{LD}		0		ns
LP → XSCL fall time	t_{LH}	V_{SS}=–2.7V	75		ns
		V_{SS}=–3.0V	65		
LP high level pulse duration	t_{WLH}	V_{SS}=–2.7V *3	75		ns
		V_{SS}=–3.0V *3	65		
FR delay permissible time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}	V_{SS}=–2.7V	50		ns
		V_{SS}=–3.0V	40		

*1 6.5MHz equivalence
*2 7.5MHz equivalence
*3 t_{WLH} specifies the time when LP is “H” and, at the same time, XSCL is “L”.

Output timing characteristics



V_{DD}=–5.0±0.5V, V5=–12.0 ~ –28.0V

Items	Symbols	Conditions	Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)		90	ns
EIO output delay time	t_{DCL}			55	ns
LP → SEG output delay time	t_{LSD}	C_L=100pF (0n)		200	ns
FR → SEG output delay time	t_{FRSD}			400	ns

V_{DD}=–4.5V ~ 2.7V, V5=–12.0 ~ –28.0V

Items	Symbols	Conditions		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L=15pF (EIO)			150	ns
EIO output delay time	t_{DCL}		V_{SS}=–2.7V		95	ns
			V_{SS}=–3.0V		85	ns
LP → SEG output delay time	t_{LSD}	C_L=100pF (0n)			400	ns
FR → SEG output delay time	t_{FRSD}				800	ns

REGARDING THE LCD DRIVING POWER

Methods to obtain necessary voltage levels

In order to obtain necessary voltage levels for driving of the LCD, it should be the best to divide the potential between V5 V_{DD} resistively to drive by means of the voltage follower by the operation amplifier. In consideration of the case of using the operation amplifier, the maximum potential level V0 and V_{DD} should be separated to independent terminals.

Nevertheless, if V0 potential drops below the V_{DD} potential increasing the potential difference, the capacity of the LCD driver decreases and, therefore, it is suggested that the potential difference between V0 ~ V_{DD} be maintained within 0V ~ 2.5V. When the operation amplifier is not used, V0 and V_{DD} should be connected.

As shown in the example of the connection, when using the resistive divider, set the resistance as low as the power capacity of the system allows.

When a series resistance exist in the power line of V5 (V_{DD}), voltage drop of V5 (V_{DD}) at the LSI current end occurs by I5 at times of signal changes and it becomes unable to maintain the relations of the LCD with intermediate potentials ($V_{DD} \geqq V0 \geqq V2 \geqq V3 \geqq V5$) leading to breakage of the LSI. When installing protective resistors, it is necessary to stabilize the voltage by their capacity.

Cautions when turning the power on and off

Since the LCD drive system voltage with this LSI is comparatively high, when high voltage is applied to the LCD drive system leaving the logic power floating or leaving V_{SS} = –2.6V or over or if LCD drive signals are output before the applied voltage to the LCD drive system is stabilized, excess current may flow to break the LSI. It therefore is suggested to bring the potential of the LCD drive output to the V0 level until the LCD drive system voltage gets stabilized using the _____ display-off function ($\overline{DSPOFF}$).

When turning the power on or off, follow the sequence below.

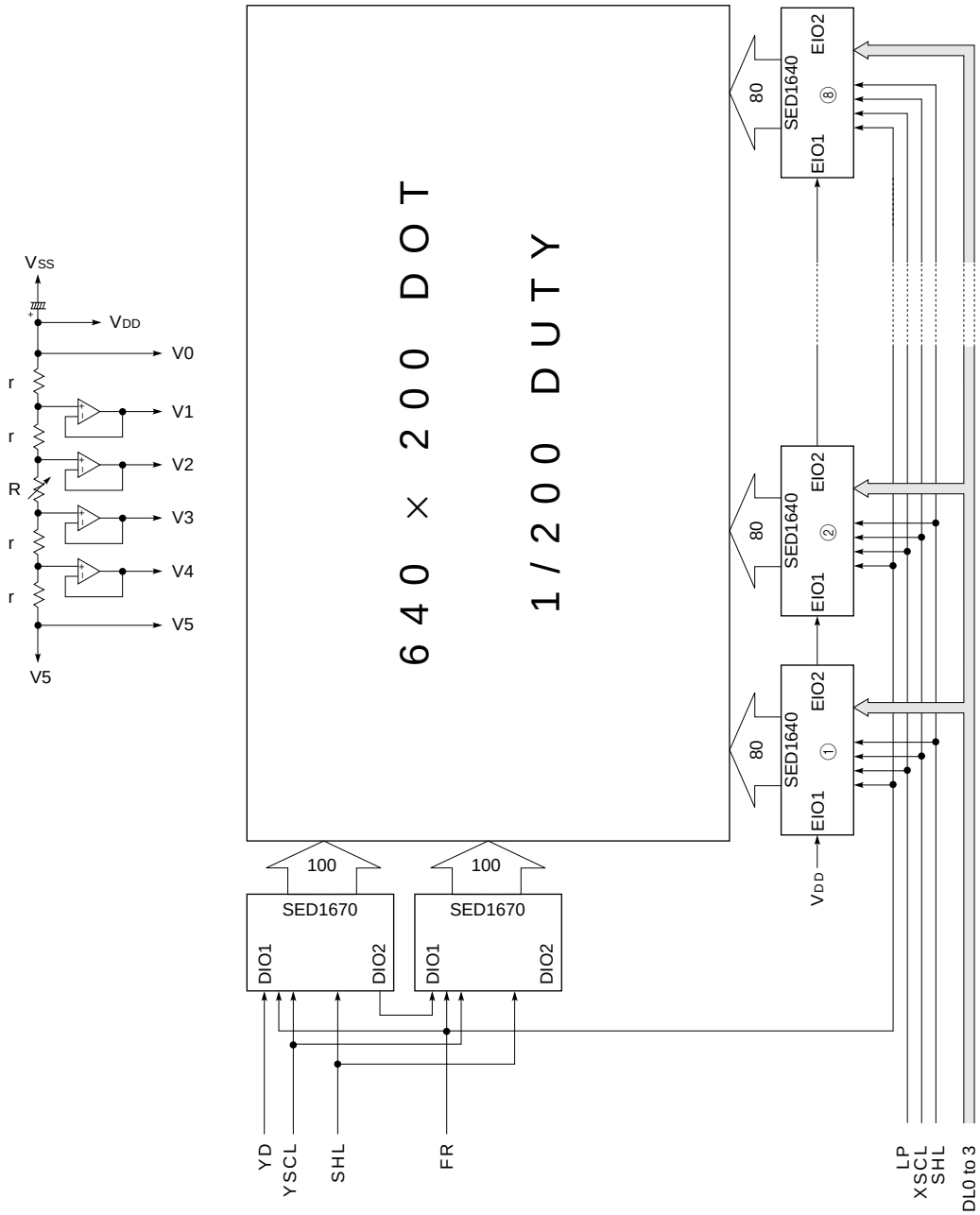
When turning on the power.....Logic systems ON → LCD drive system ON (or turn them on simultaneously).

When turning off the power.....LCD drive system OFF → Logic system OFF (or turn them off simultaneously).

Insert quick melting fuse in series to the LCD power source for prevention of an excess current flow. It is necessary to choose the optimum value for the protective resistance matching the capacity of the liquid crystal cells.

AN EXAMPLE OF CONNECTION

Block diagram of a large sized LCD



An example of TAB pin layout with SED1640T (Examination)

Note: This is not to specify the dimensions of the TAB.