

9. SED1670

Dot Matrix LCD Common Driver

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OVERVIEW

The SED1670 is a 100 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels upto a duty ratio of 1/300. It is intended to be used in conjunction with the SED1640D or SED1606D as a pair.

Since the SED1670 is so designed to drive LCDs over a wide range of voltages, and also the maximum potential V_0 of its LCD drive bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.

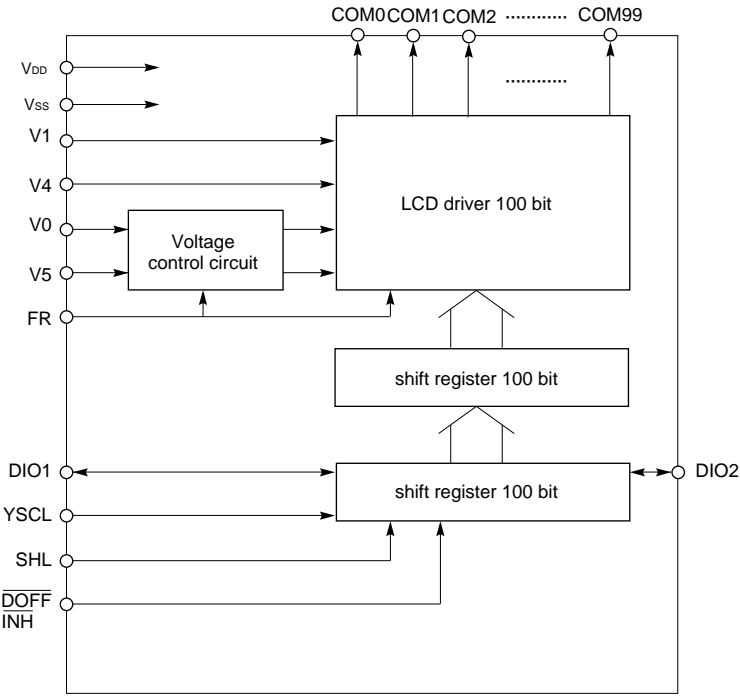
Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel.

And the SED1670 can display 65 x 132 panel when used as a common driver of RAM built-in driver, SED1531.

FEATURES

- Number of LCD drive output segments: 100
- Common output ON resistance: 700 Ω (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640 × 480 dots when used in combination with SED 1640D or SED1606D.
- Selectable pin output shift direction
- No-bias display OFF function (*1*)
- Instantaneous display blanking enabled by inhibit function (*0*)
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: -7 V to -28 V (Absolute maximum rated voltage: -30 V)
- Logic system power supply: -2.7 V to -5.5 V
- Chip packaging
 - SED1670D0A (AL-pad die form)
 - SED1670D1A
 - SED1670D0B (Au bump die form)
 - SED1670D1B
 - SED1670T0A (TCP die form)
 - SED1670T1A
- No radial rays countermeasure taken in designing

BLOCK DIAGRAM



$\overline{\text{INH}}$ in SED1670⁰
 $\overline{\text{DOFF}}$ in SED1670¹

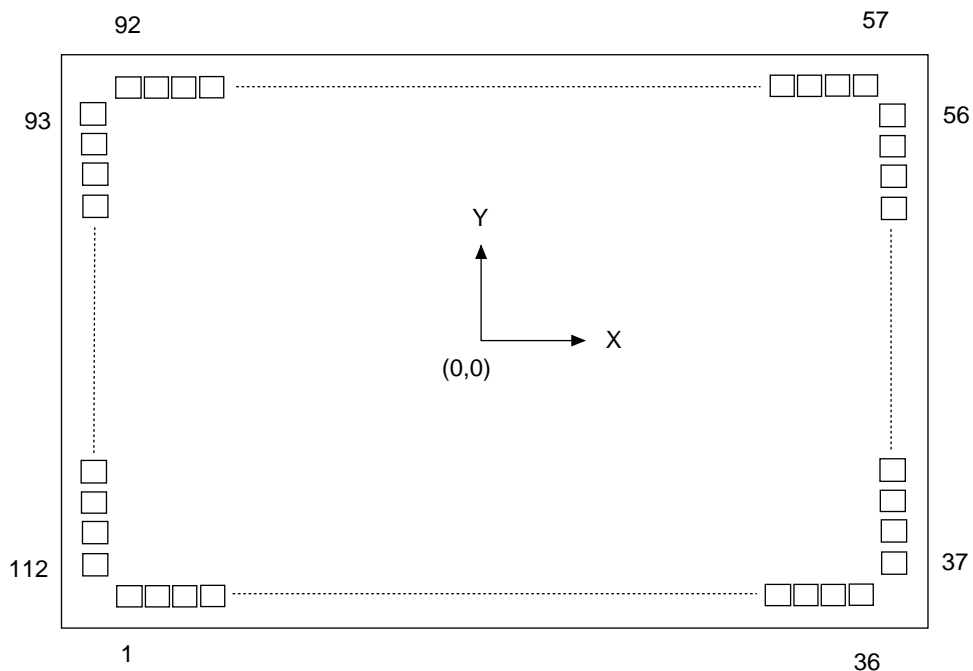
PIN DESCRIPTION

Pin name	I/O	Function	Number of pins												
COM0 to COM099	O	LCD drive common (row) output The output changes at the YS CL falling edge.	100												
DIO1, DIO2	I/O	100-bit shift register serial data input/output To be set to input or output according to the SHL input The output changes at the YSCL falling edge.	2												
YSCL	I	Serial data shift clock input The scanning data is shifted at the falling edge.	1												
SHL	I	Shift direction selection and DIO pin I/O control input <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SHL</th> <th>COM output shift direction</th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>0 → 99</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>H</td> <td>99 → 0</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>	SHL	COM output shift direction	DIO1	DIO2	L	0 → 99	Input	Output	H	99 → 0	Output	Input	1
SHL	COM output shift direction	DIO1	DIO2												
L	0 → 99	Input	Output												
H	99 → 0	Output	Input												
$\overline{\text{DOFF}}$	I	LCD display blanking control input When "L" is input, the content of shift register is cleared and all common outputs become the V_0 level instantaneously (SED1670D1B).	1												
$\overline{\text{INH}}$	I	LCD drive display blanking control input When "L" is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously. Common output = V_4 (when FR = L) Common output = V_1 (when FR = H) (SED1670D0B)	(1)												
FR	I	LCD drive output AC converted signal input	1												
V_{DD}, V_{SS}	Power supply	Logic power supply V_{DD} : 0 V (GND) V_{SS} : -5.0 V	2												
V_0, V_1, V_4, V_5	Power supply	LCD drive power supply V_5 : -7 V to -28 V $V_{DD} \geq V_0 \geq V_1 > V_4 \geq V_5$	4												

INH for SED1670*0*
DOFF for SED1671*1*

Total: 112

PAD LAYOUT AND COORDINATES



Chip size 5.49mm × 3.03mm
 Chip thickness 525μm (Au-bump die from)
 400μm (Al-Pad die from)

1) Au bump specification reference values

Bump specific : High Quality Au bump
 Bump size : 90μm × 90μm
 Bump height : 17μm ~ 28μm

2) AL Pad specification reference values

Pad Opening : 100μm × 100μm

PAD		Actual dimensions		PAD		Actual dimensions		PAD		Actual dimensions	
NO.	NAME	X	Y	NO.	NAME	X	Y	NO.	NAME	X	Y
1	COM5	-2187	-1357	41	COM45	2584	-711	81	COM85	-803	1357
2	6	-2058	↓	42	46	↓	-581	82	86	-932	↓
3	7	-1929	↓	43	47	↓	-452	83	87	-1062	↓
4	8	-1799	↓	44	48	↓	-323	84	88	-1191	↓
5	9	-1670	↓	45	49	↓	-194	85	89	-1320	↓
6	10	-1541	↓	46	50	↓	-65	89	90	-1449	↓
7	11	-1412	↓	47	51	↓	65	87	91	-1578	↓
8	12	-1283	↓	48	52	↓	194	88	92	-1708	↓
9	13	-1153	↓	49	53	↓	323	89	93	-1837	↓
10	14	-1024	↓	50	54	↓	452	90	94	-1966	↓
11	15	-895	↓	51	55	↓	581	91	95	-2095	↓
12	16	-766	↓	52	56	↓	711	92	96	-2224	1357
13	17	-637	↓	53	57	↓	840	93	97	-2473	1334
14	18	-507	↓	54	58	↓	969	94	98	↓	1201
15	19	-378	↓	55	59	↓	1098	95	99	↓	1071
16	20	-249	↓	56	60	2584	1231	96	DIO2	↓	941
17	21	-120	↓	57	61	2298	1357	97	DOFF	↓	715
18	22	10	↓	58	62	2168	↓	(97)	(INH)	↓	↓
19	23	139	↓	59	63	2039	↓	98	FR	↓	585
20	24	268	↓	60	64	1910	↓	99	YSCL	↓	455
21	25	397	↓	61	65	1781	↓	100	SHL	↓	325
22	26	526	↓	62	66	1652	↓	101	V _{DD}	↓	185
23	27	656	↓	63	67	1522	↓	102	V _{SS}	↓	46
24	28	785	↓	64	68	1393	↓	103	V ₀	↓	-112
25	29	914	↓	65	69	1264	↓	104	V ₁	↓	-252
26	30	1043	↓	66	70	1135	↓	105	V ₄	↓	-391
27	31	1172	↓	67	71	1006	↓	106	V ₅	↓	-531
28	32	1302	↓	68	72	876	↓	107	DIO1	↓	-671
29	33	1431	↓	69	73	747	↓	108	COM0	↓	-810
30	34	1560	↓	70	74	618	↓	109	1	↓	-941
31	35	1689	↓	71	75	489	↓	110	2	↓	-1071
32	36	1818	↓	72	76	360	↓	111	3	↓	-1201
33	37	1948	↓	73	77	230	↓	112	4	-2473	-1334
34	38	2077	↓	74	78	101	↓				
35	39	2206	↓	75	79	-28	↓				
36	40	2335	-1357	76	80	-157	↓				
37	41	2584	-1231	77	81	-286	↓				
38	42	2584	-1094	78	82	-416	↓				
39	43	2584	-969	79	83	-545	↓				
40	44	2584	-840	80	84	-674	1357				

PAD No. 97: $\overline{\text{INH}}$ for SED1670*0*
DOFF for SED1670*1*

FUNCTIONAL DESCRIPTION

Shift register

This is a bidirectional shift register to transfer common data.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver circuit

This driver outputs the LCD drive voltage.

The relationship among the display blanking signal $\overline{\text{DOFF}}$, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below:

(SED1670*1*)

$\overline{\text{DOFF}}$	Contents of shift register	FR	COM output voltage	
H	H	H	V5	(Select level)
		L	V0	
	L	H	V1	(Non-select level)
		L	V4	
L	Fixed to L	–	V0	–

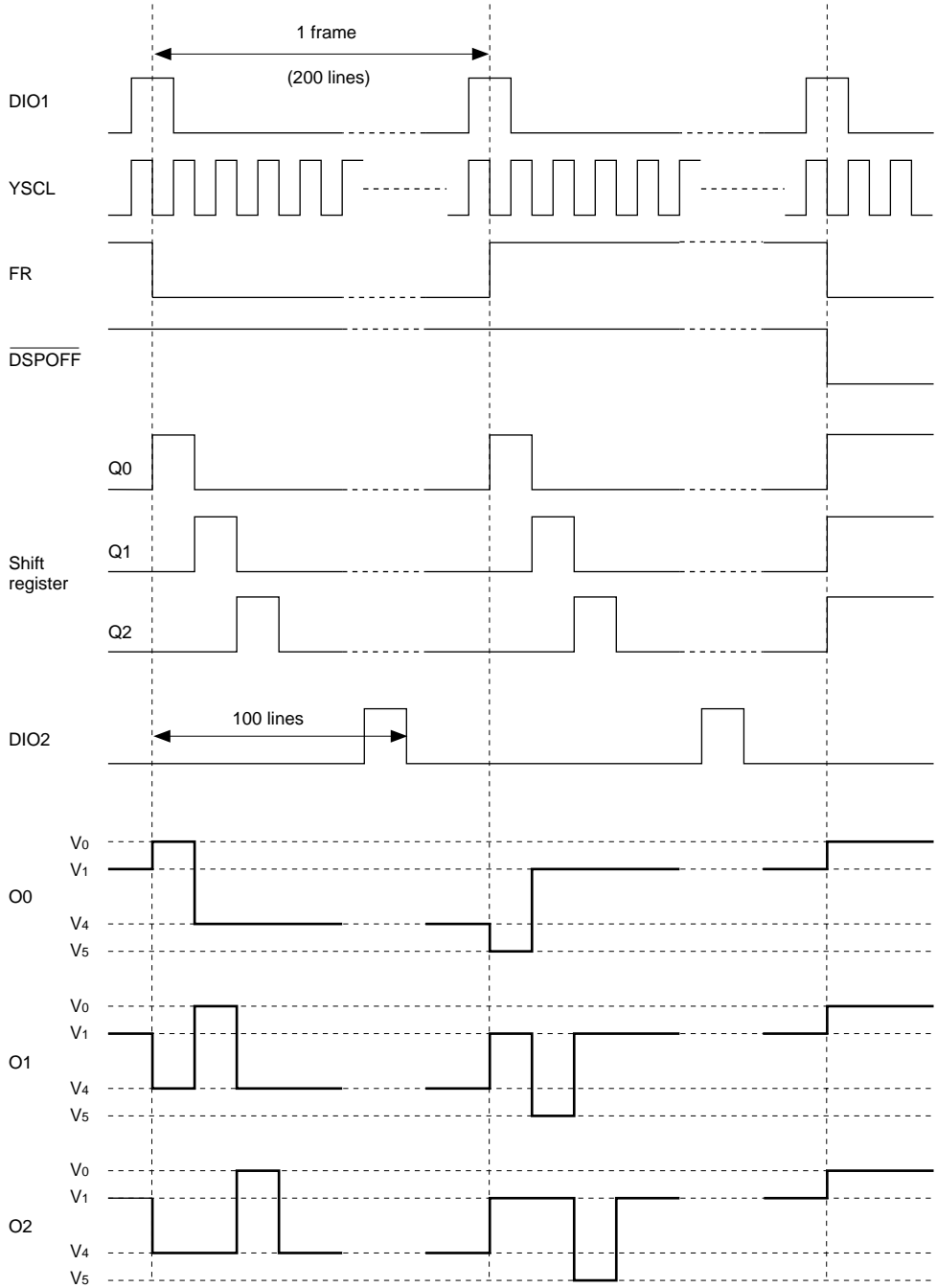
The relationship among the display blanking signal INH, contents of the shift register, AC converted signal FR and COM output voltage is as shown in the table below:

(SED1670*0*)

INH	Contents of shift register	FR	COM output voltage	
H	H	H	V5	(Select level)
		L	V0	
	L	H	V1	(Non-select level)
		L	V4	
L	Fixed to L	H	V1	(Non-select level)
		L	V4	

TIMING CHART (SED1670D1B)

SHL="L"
1/200 Duty



The V1 or V4 non-select level is output corresponding to the FR in SED1670D0B or $\overline{INH}=L$, respectively.

ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V _{SS}	-7.0 to +0.3	V
Supply voltage (2)	V ₅	-30.0 to +0.3	V
Supply voltage (3)	V ₀ , V ₁ , V ₄	V ₅ -0.3 to +0.3	V
Input voltage	V _I	V _{SS} -0.3 to +0.3	V
Output voltage	V _O	V _{SS} -0.3 to +0.3	V
Output current (1)	I _O	20	mA
Output current (2)	I _{OCOM}	20	mA
Operating temperature	T _{opr}	-40 to + 85	°C
Storing temperature 1	T _{stg}	-65 to +150	°C

Notes:

1. The voltage of V₀, V₁ and V₄ must always satisfy the condition of V_{DD} ≥ V₀ ≥ V₁ ≥ V₄ ≥ V₅.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = -2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.

Care should be taken to the power supply sequence especially in the system power ON or OFF.

ELECTRICAL CHARACTERISTICS

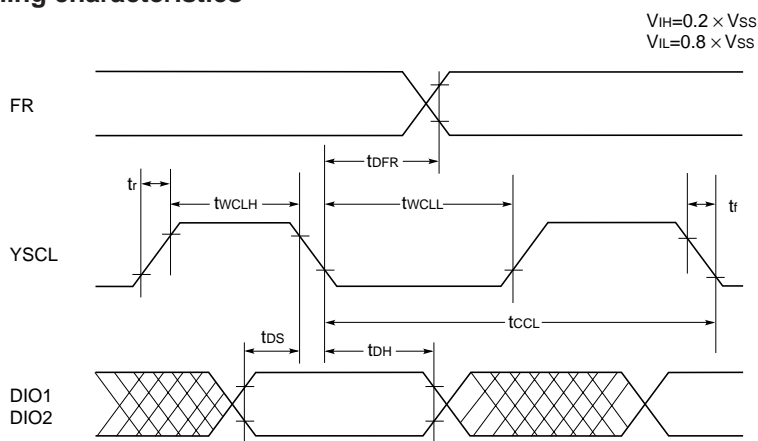
DC characteristics

Unless otherwise specified, $V_{DD} = V_0 = 0V$, $V_{SS} = -5.0V \pm 10\%$, $T_a = -40$ to $85^\circ C$.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–7.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–7.0	V	V_5
Supply voltage (2)	V_0	Recommended value	–2.5	–	0	V	V_0
Supply voltage (3)	V_1	Recommended value	$2/9 \cdot V_5$	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	Recommended value	V_5	–	$7/9 \cdot V_5$	V	V_4
"H" input voltage (1)	V_{IH}	$V_{SS} = -2.7V$ to $-5.5V$	$0.2V_{SS}$	–	0	V	DIO1, DIO2, YSCL, SHL, FR
"L" input voltage (1)	V_{IL}		V_{SS}	–	$0.8V_{SS}$	V	
"H" input voltage (2)	V_{IHT}	$V_{SS} = -2.7V$ to $-5.5V$	$0.2V_{SS}$	–	0	V	\overline{DOFF} , \overline{INH}
"L" input voltage (2)	V_{ILT}		V_{SS}	–	$0.85V_{SS}$	V	
"H" output voltage	V_{OH}	$I_{OH} = -0.3mA$ $I_{OH} = -0.2mA$ ($V_{SS} = -2.7$ to $-4.5V$)	–0.4	–	0	V	DIO1, DIO2
"L" output voltage	V_{OL}	$I_{OL} = +0.3mA$ $I_{OL} = +0.2mA$ ($V_{SS} = -2.7$ to $-4.5V$)	V_{SS}	–	$V_{SS} + 0.4$	V	
Input leakage current	I_{LI}	$V_{SS} \leq V_{IN} \leq 0V$	–	–	2.0	μA	YSCL, SHL, \overline{DOFF} , \overline{INH} , FR
Input/output leakage current	$I_{L/O}$	$V_{SS} \leq V_{IN} \leq 0V$	–	–	5.0	μA	DIO1, DIO2
Static current	I_{DDS}	$V_5 = -7.0$ to $-28.0V$ $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	–	–	25	μA	V_{DD}
Output resistance	R_{COM}	$\Delta V_{ON} = 0.5V$ $V_5 = -20.0V$ When the V_1, V_4, V_0 or V_5 level is output	–	0.70	1.40	$K\Omega$	COM0–COM99
Average operating current consumption (1)	I_{SS1}	$V_{SS} = -5.0V$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, $f_{SCL} = 12KHz$, Frame frequency = 60Hz Input data; "H" at no load every 1/200 duty Other conditions are the same as $V_{SS} = -3.0V$	–	7	15	μA	V_{SS}
			–	5	10		
Average operating current consumption (2)	I_{SS2}	$V_{SS} = -5.0$, $V_1 = -2.0V$, $V_4 = -18.0V$, $V_5 = -20.0V$ Other conditions are the same as in the item of I_{SS1} .	–	7	15	μA	V_5
Input pin capacitance	C_I	$T_a = 25^\circ C$	–	–	8	pF	YSCL, SHL, \overline{DOFF} , \overline{INH} , FR
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

AC CHARACTERISTICS

Input timing characteristics



Unless otherwise specified $V_{SS}=-5.0V \pm 10\%$, $T_a=-40$ to 85°C

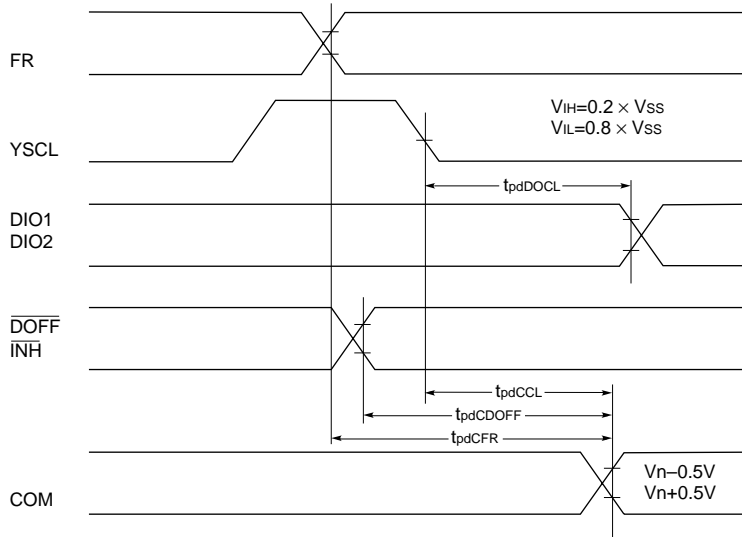
Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns
YSCL period	t_{cCL}	—	500	—	ns
YSCL "H" pulsewidth	t_{wCLH}	—	70	—	ns
YSCL "L" pulsewidth	t_{wCLL}	—	330	—	ns
Data setup time	t_{ds}	—	100	—	ns
Data hold time	t_{dH}	—	10	—	ns
Allowable FR delay time	t_{DFR}	—	-500	500	ns

Unless otherwise specified $V_{SS}=-2.7V$ to $-4.5V$, $T_a=-40$ to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns
YSCL period	t_{cCL}	—	1000	—	ns
YSCL "H" pulsewidth	t_{wCLH}	—	160	—	ns
YSCL "L" pulsewidth	t_{wCLL}	—	330	—	ns
Data setup time	t_{ds}	—	200	—	ns
Data hold time	t_{dH}	—	10	—	ns
Allowable FR delay time	t_{DFR}	—	-500	500	ns

The standard applicable to t_{cCL} , t_{wCLH} , t_{wCLL} and t_{ds} when $V_{SS} = -2.4V$ shall be 1.3 times of that applies when $V_{SS} = -2.7V$ to $-4.5V$.

Output timing characteristics



Unless otherwise specified $V_{SS} = -5.0V \pm 10\%$, $T_a = -40$ to $85^\circ C$

Paramant	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	$C_L = 15pF$	30	300	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	$V_5 = -7.0$ to $-28.0V$ $C_L = 100pF$	-	3.0	μs
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}				

Unless otherwise specified $V_{SS} = -2.7V$ to $-4.5V$, $T_a = -40$ to $85^\circ C$

Paramant	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	$C_L = 15pF$	60	600	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	$V_5 = -7.0$ to $-28.0V$ $C_L = 100pF$	-	3.0	μs
(DOFF to COM output) delay time	$t_{pdCDOFF}$				
(INH to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}				

The standard applicable at $V_{SS} = -2.4V$ shall be the same as that employed when $V_{SS} = -2.7V$ to $-4.5V$.

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is the most simple to divide the resistance of potential as shown in the connection example. On the other hand, to obtain a high quality display, it is necessary to raise the accuracy and constancy of each voltage level and to set the divided resistance value as low as possible in the range of system power capacity.

Especially when a low-power LCD driving is required, set the divided resistance to a higher value and drive the LCD with a voltage follower by means of operational amplifier instead. In taking into consideration of a case where the operational amplifier is employed, the maximum potential level V_0 for LCD driving has been isolated from the V_{DD} pin.

When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD} .

When no operational amplifier is used, connect V_0 and V_{DD} pins.

Note in power ON/OFF

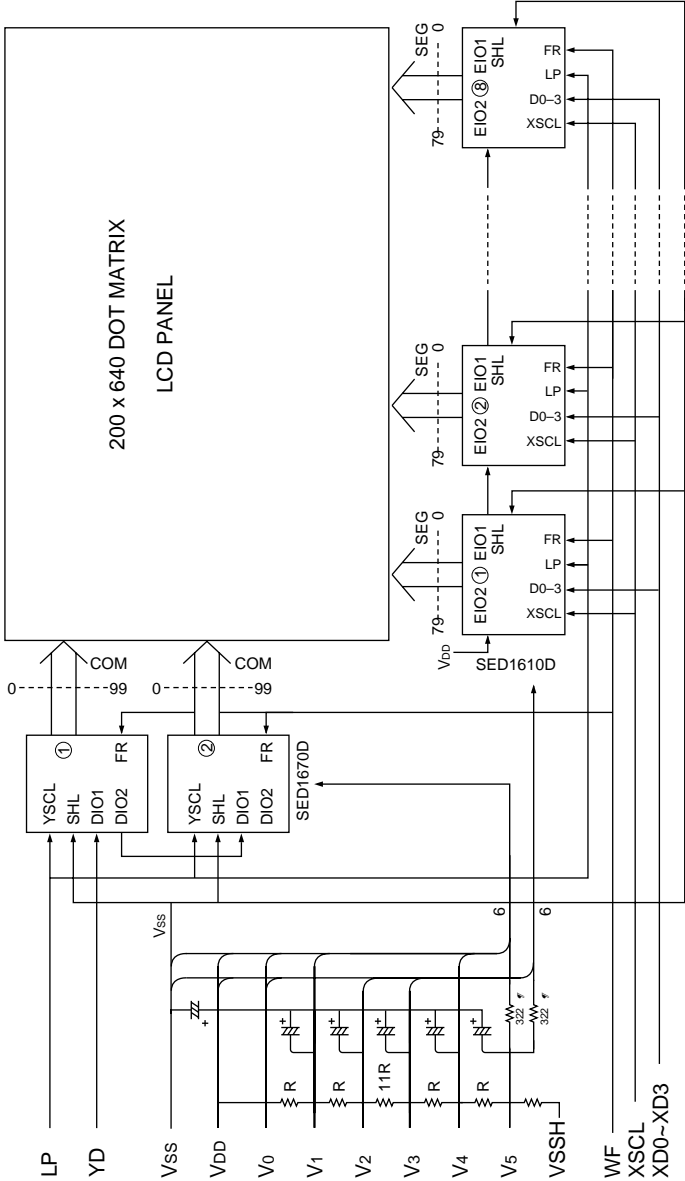
Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating, an overcurrent flows and LSI breaks down in some cases.

Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both

At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

CONNECT EXAMPLE



Note *1 It must be provided as the protective resistor against overcurrent. Also, the bypass capacitor (0.01 μF) for noise suppression must be provided near to Vss and V5 terminals on each LSI.

DIFFERENT POINTS FROM REPLACEMENT PRODUCT

	SED1670*0*	SED1631**
Function	Bidirectional shift register $\overline{\text{INH}}$ 100 output segments	Bidirectional shift register $\overline{\text{INH}}$ 100 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	-
PAD coordinates	Different from the equivalent product	-

	SED1670*1*	SED1635**
Function	Bidirectional shift register $\overline{\text{DOFF}}$ 100 output segments	Bidirectional shift register $\overline{\text{DOFF}}$ 100 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	-
PAD coordinates	Different from the equivalent product	-

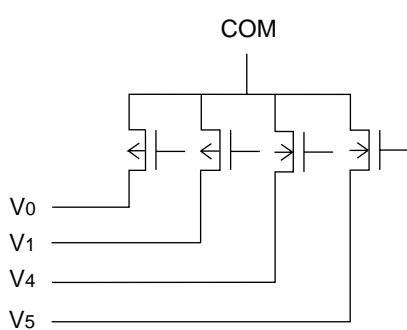


Fig. 1

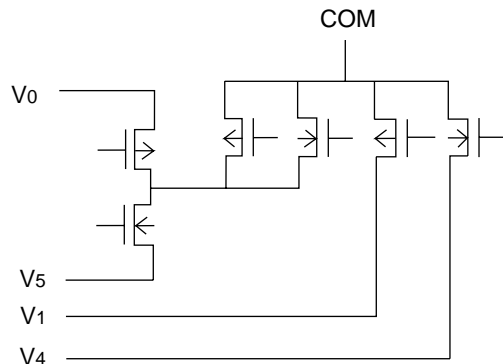


Fig. 2 @