10. SED1672
Dot Matrix LCD Common Driver

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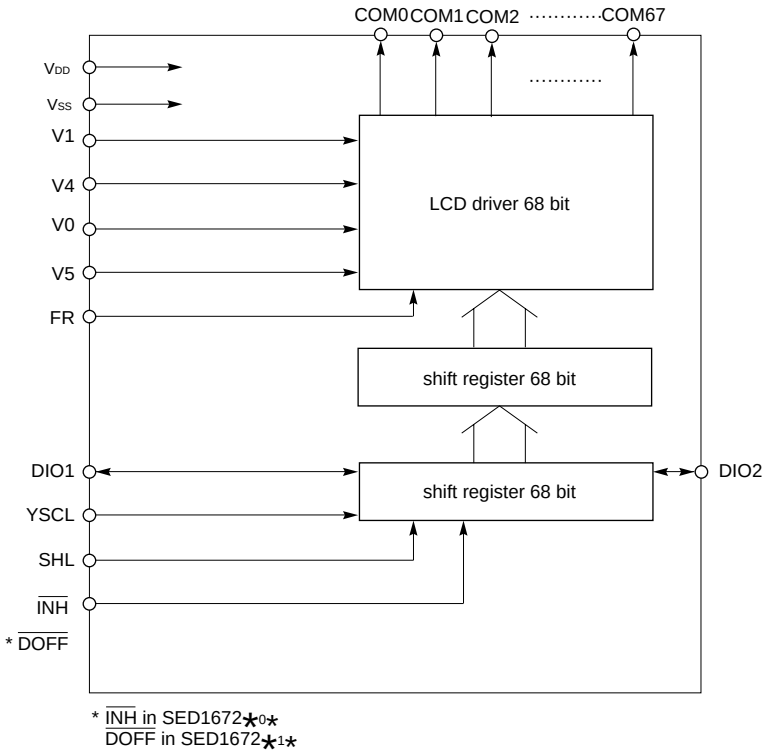
OVERVIEW

The SED1672 is a 68 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels up to a duty ratio of 1/300. It is intended to be used in conjunction with the SED1606 as a pair.
Since the SED1606 is so designed to drive LCD's over a wide range of voltages, and also the maximum potential V_0 of its LCD drive bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
The SED1672 is featured in its simple pad layout which is easy in mounting PC boards in addition to its selectable bidirectional driver output sequence. It also has 68 LCD output segments of high pressure resistance and low output impedance.
It can display the 65 × 132 panel when used as the expansion driver of SED1531 being built in RAM (SED1672*1*).

FEATURES

- Number of LCD drive output segments: 68
- Common output ON resistance: 700 Ω (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640 × 480 dots when used in combination with SED1606.
- Selectable pin output shift direction
- Instantaneous display blanking enabled by inhibit function (*0* type)
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –7 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging
  SED1672D0A (AL-pad die form)
  SED1672D1A
  SED1672F0A (80-pin QFP5)
- No radial rays countermeasure taken in designing
- Non-bias display off function

BLOCK DIAGRAM



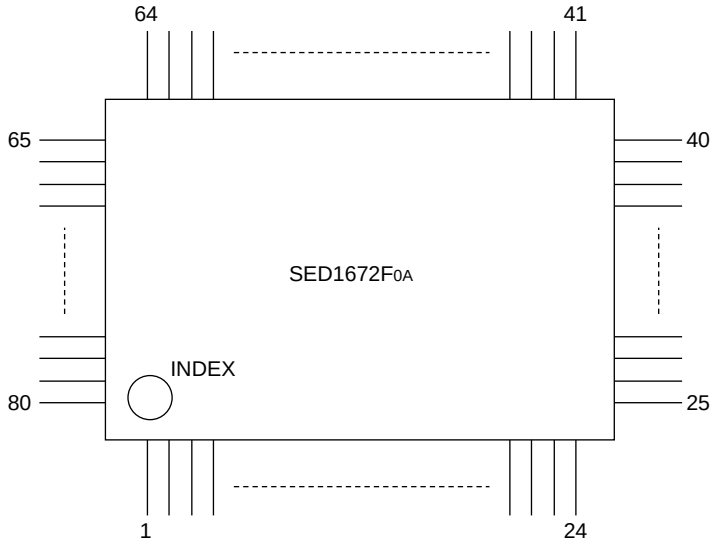
PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>COM0 to COM67</td><td>O</td><td>LCD drive common (row) output
The output changes at the YSCL falling edge.</td><td>68</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>100-bit shift register serial data input/output
To be set to input or output according to the SHL input
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input
The scanning data is shifted at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Display data latch pulse input (Falling edge trigger)
Shift direction selection and DIO pin I/O control input
<table>
<tr><th>SHL</th><th>COM output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 → 67</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>67 → 0</td><td>Ourput</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>LCD display blanking control input when “L” is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously. (SED1672✻1✻)</td><td>1</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>LCD display blanking control input
When “L” is input, the content of shift register is cleared and all common outputs become the non-select level instantaneously.
Common output = V_4 (when FR = L)
Common output = V_1 (when FR = H) (SED1672✻0✻)</td><td>(1)</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output AC converted signal input</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V (GND) V_{SS}: –5.0 V</td><td>2</td></tr>
<tr><td>V_0, V_1, V_4, V_5</td><td>Power supply</td><td>LCD drive power supply V_5: –7 V to –28 V
$V_{DD} \geq V_0 \geq V_1 > V_4 \geq V_5$</td><td>4</td></tr>
</table>

$\overline{INH}$ in SED1672✻0✻
$\overline{DOFF}$ in SED1672✻1✻

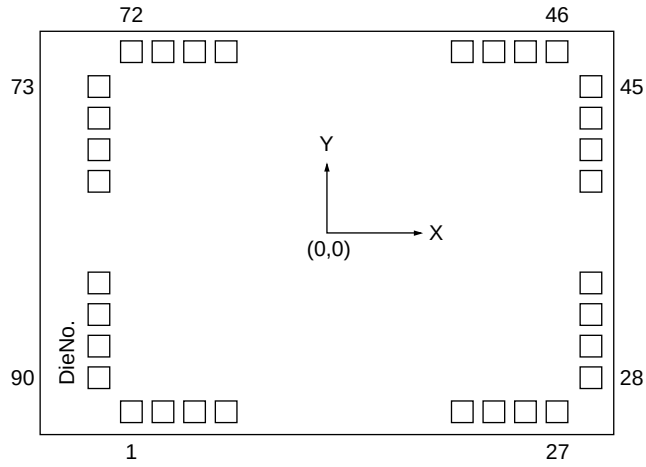
PIN LAYOUT

Package type: QFP–5 80pin



PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name
1	COM 3	21	COM 23	41	COM 43	61	COM 63
2	COM 4	22	COM 24	42	COM 44	62	COM 64
3	COM 5	23	COM 25	43	COM 45	63	COM 65
4	COM 6	24	COM 26	44	COM 46	64	COM 66
5	COM 7	25	COM 27	45	COM 47	65	COM 67
6	COM 8	26	COM 28	46	COM 48	66	DIO2
7	COM 9	27	COM 29	47	COM 49	67	$\overline{INH}$
8	COM 10	28	COM 30	48	COM 50	68	FR
9	COM 11	29	COM 31	49	COM 51	69	YSCL
10	COM 12	30	COM 32	50	COM 52	70	SHL
11	COM 13	31	COM 33	51	COM 53	71	V_{DD}
12	COM 14	32	COM 34	52	COM 54	72	V_{SS}
13	COM 15	33	COM 35	53	COM 55	73	V_0
14	COM 16	34	COM 36	54	COM 56	74	V_1
15	COM 17	35	COM 37	55	COM 57	75	V_4
16	COM 18	36	COM 38	56	COM 58	76	V_5
17	COM 19	37	COM 39	57	COM 59	77	DIO1
18	COM 20	38	COM 40	58	COM 60	78	COM 0
19	COM 21	39	COM 41	59	COM 61	79	COM 1
20	COM 22	40	COM 42	60	COM 62	80	COM 2

PAD LAYOUT AND PAD COORDINATE



Chip size: 4.27 × 3.03 mm
Chip thickness: 400 µm (for AL pad product) and 525 µm (for BUMP product).
AL pad product: Pad opening is 100 × 100 µm.
BUMP product: Vertical Au bump.
Bump size is 90 × 90 µm.
Bump height is 17 to 25 µm.

PAD NO.	PIN NAME	X	Y
1	DM	–1579	–1357
2	COM 3	–1449	
3	COM 4	–1320	
4	COM 5	–1191	
5	COM 6	–1062	
6	COM 7	–933	
7	COM 8	–803	
8	COM 9	–674	
9	COM 10	–545	
10	COM 11	–416	
11	COM 12	–287	
12	COM 13	–154	
13	COM 14	–28	
14	COM 15	101	
15	COM 16	230	
16	COM 17	359	
17	COM 18	489	
18	COM 19	618	
19	COM 20	747	
20	COM 21	876	
21	COM 22	1005	
22	COM 23	1135	
23	COM 24	1264	
24	COM 25	1393	
25	COM 26	1522	
26	DM	1651	
27	DM	1781	–1357
28	DM	1976	–1098
29	COM 27	1976	–969
30	COM 28	1976	–840

PAD NO.	PIN NAME	X	Y
31	COM 29	1976	–711
32	COM 30		–581
33	COM 31		–452
34	COM 32		–323
35	COM 33		–194
36	COM 34		–65
37	COM 35		65
38	COM 36		194
39	COM 37		323
40	COM 38		452
41	COM 39		581
42	COM 40		711
43	COM 41		840
44	COM 42		969
45	DM	1976	1098
46	DM	1743	1357
47	DM	1614	
48	COM 43	1485	
49	COM 44	1355	
50	COM 45	1226	
51	COM 46	1097	
52	COM 47	968	
53	COM 48	839	
54	COM 49	709	
55	COM 50	580	
56	COM 51	451	
57	COM 52	322	
58	COM 53	193	
59	COM 54	63	
60	COM 55	–66	1357

PAD NO.	PIN NAME	X	Y
61	COM 56	–195	1357
62	COM 57	–324	
63	COM 58	–453	
64	COM 59	–583	
65	COM 60	–712	
66	COM 61	–841	
67	COM 62	–970	
68	COM 63	–1099	
69	COM 64	–1229	
70	COM 65	–1358	
71	COM 66	–1487	
72	DM	–1616	1357
73	DM	–1865	1201
74	COM 67		1071
75	DIO2		941
76	*1 $\overline{\text{INH}}$		715
77	FR		585
78	YSCL		455
79	SHL		325
80	V_{DD}		195
81	V_{SS}		55
82	V_0		–112
83	V_1		–252
84	V_4		–391
85	V_5		–531
86	DIO1		–671
87	COM 0		–810
88	COM 1		–941
89	COM 2		–1071
90	DM	–1865	–1201

*1 PAD No. 76: $\overline{\text{INH}}$ for SED1672✻0✻
$\overline{\text{DOFF}}$ for SED1672✻1✻

FUNCTIONAL DESCRIPTION

Shift register

This is a bidirectional shift register to transfer common data.

Level shifter

This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver circuit

This driver outputs the LCD drive voltage.
The relationship among the display blanking signal $\overline{INH}$, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below:

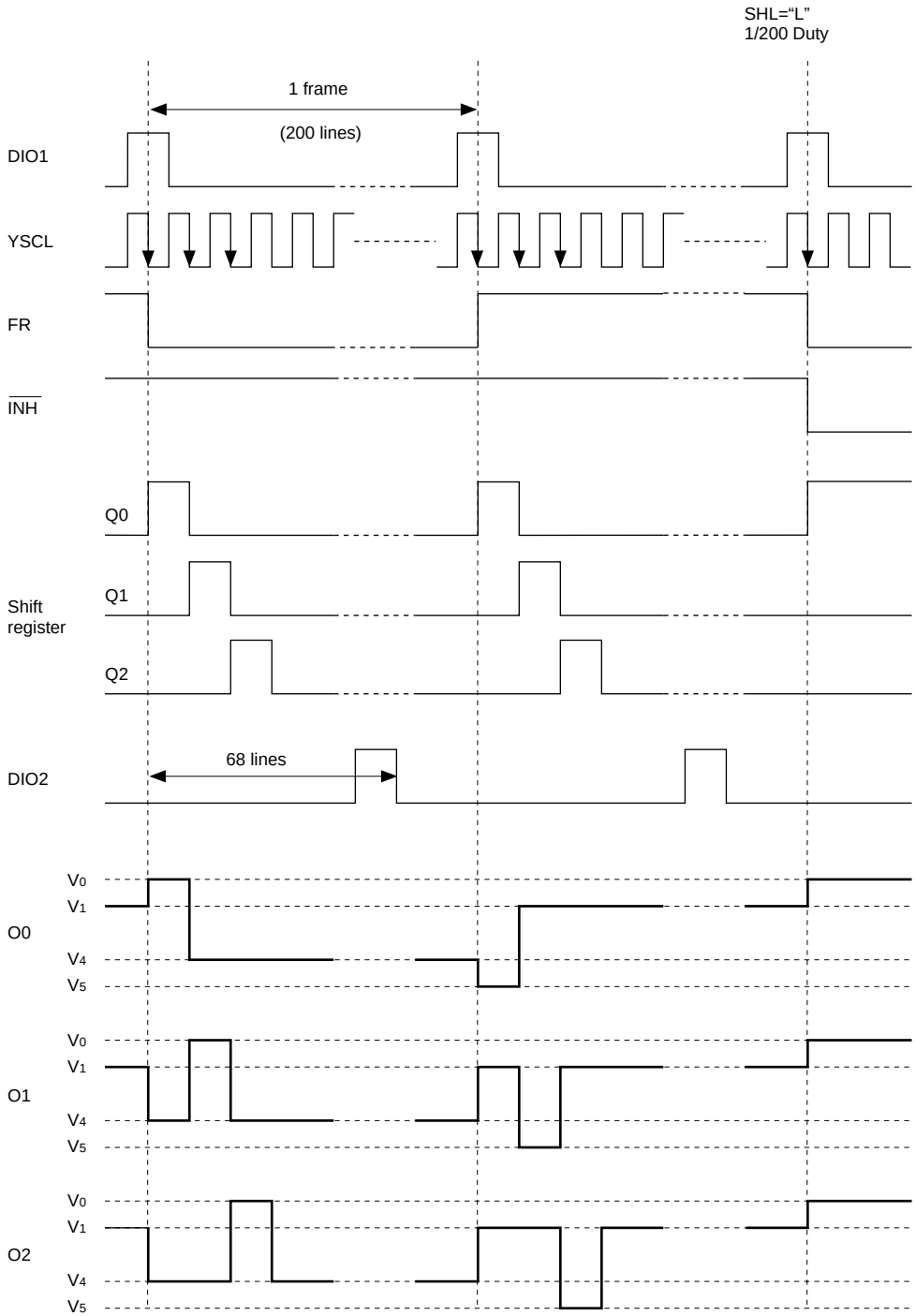
(SED1672*0*)

INH	Contents of shift register	FR	COM output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	Fixed to L	H	V_1	(Non-select level)
		L	V_4	

The relationship among the display blanking signal $\overline{INH}$, contents of shift register, AC converted signal FR and common output voltage is as shown in the table below.

$\overline{DOFF}$	Contents of shift register	FR	COM output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	Fixed to L	—	V_0	(Non-select level)

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltage	V_I	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature	Tstg	–65 to +150	°C
Soldering temperature and time	Tsol	260°C · 10sec	–

Notes:

1. The voltage of V_0, V1 and V_4 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.
3. All the above voltage is based on V_{DD} = 0 V.

ELECTRICAL CHARACTERISTICS

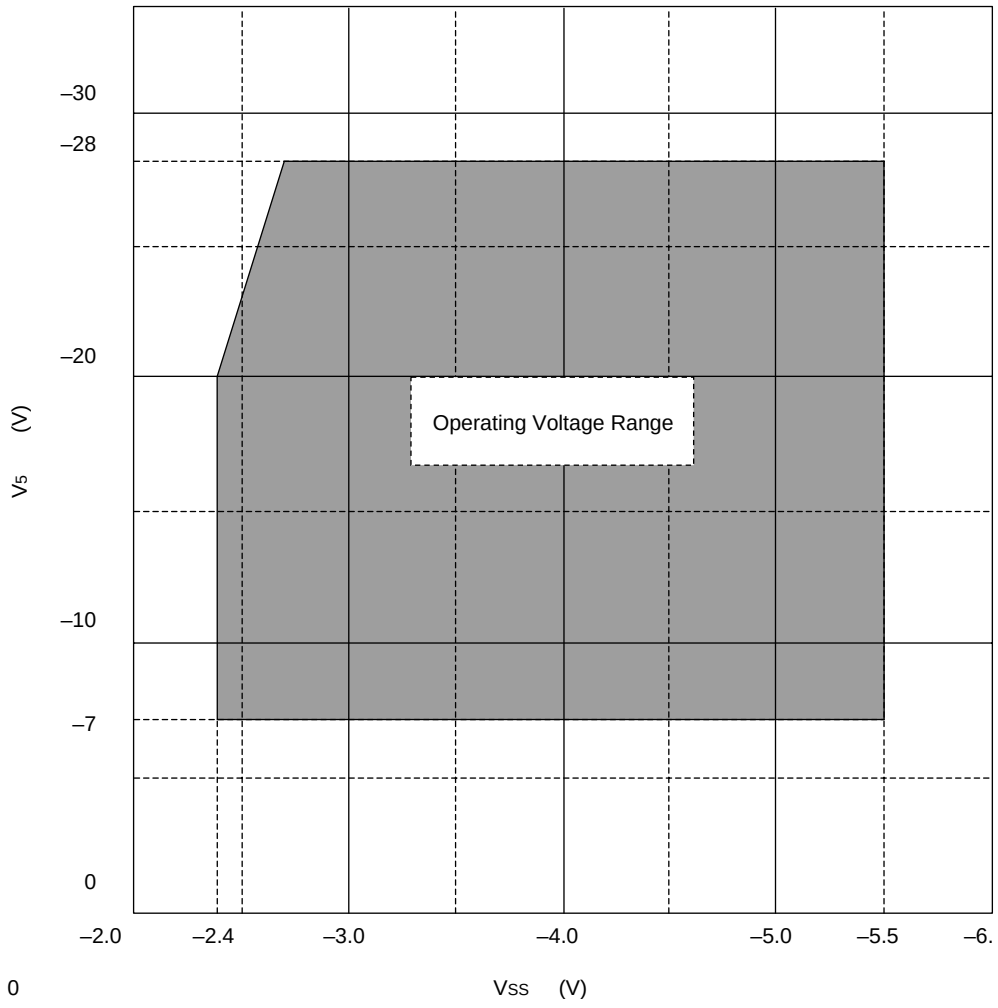
DC characteristics

Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V±10%, Ta = –40 to 85°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–7.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–7.0	V	V_5
Supply voltage (2)	V_0	Recommended value	–2.5	–	0	V	V_0
Supply voltage (3)	V_1	Recommended value	2/9·V_5	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	Recommended value	V_5	–	7/9·V_5	V	V_4
"H" input voltage (1)	V_{IH}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	DIO1, DIO2, YSCL, SHL, FR
"L" input voltage (1)	V_{IL}		V_{SS}	–	0.8V_{SS}	V	
"H" input voltage (2)	V_{IHT}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	$\overline{INH}$
"L" input voltage (2)	V_{ILT}		V_{SS}	–	0.85V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH}=–0.3mA I_{OH}=–0.2mA (V_{SS}=–2.7 to –4.5V)	–0.4	–	0	V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL}=+0.3mA I_{OL}=+0.2mA (V_{SS}=–2.7 to –4.5V)	V_{SS}	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	–	–	2.0	µA	YSCL, SHL, $\overline{INH}$, FR
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	–	–	5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5=–7.0 to –28.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔVON =0.5V, V_5= –20.0V, When the V_1, V_4, V_0 or V_5 level is output	–	0.70	1.40	KΩ	COM0 to COM99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, V_{IH}=VDD, V_{IL}=V_{SS}, f_{YSCL}=12KHz, Frame frequency=60Hz Input data; "H" at no load every 1/200 duy	–	7	15	µA	V_{SS}
		Other conditions are the same as V_{SS} = –3.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0V, V_1=–2.0V, V_4=–18.0V, V_5=–20.0V Other conditions are the same as in the item of I_{SS1}.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{INH}$, FR
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

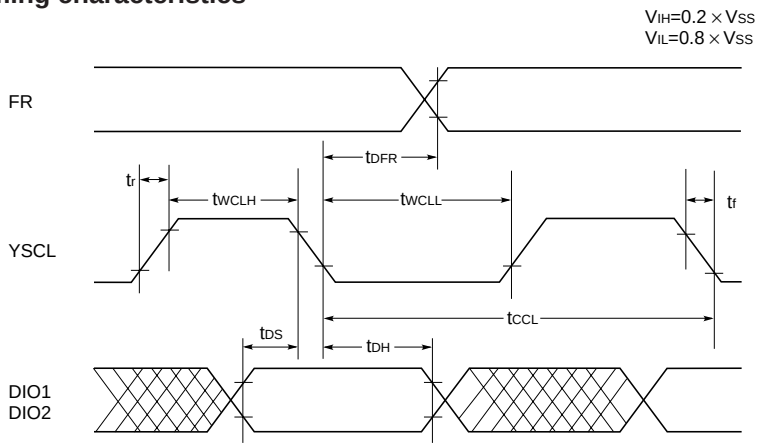
Operating Voltage Range V_{SS} – V_5

V_5 voltage must be set within the following operating voltage range of V_{SS} – V_5.



AC CHARACTERISTICS

Input timing characteristics



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

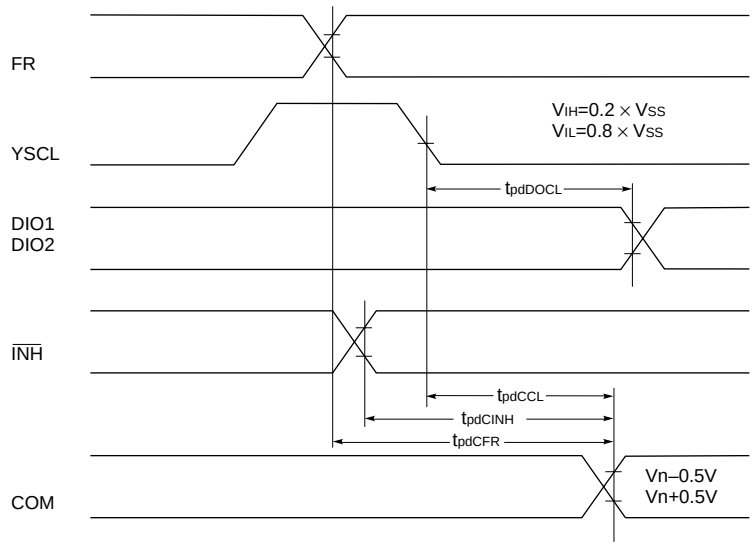
Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	500	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	70	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	100	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	1000	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	160	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	200	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

The standard applicable to t_{CCL}, t_{WCLH}, t_{WCLL}, t_{DS} and t_{DH} when V_{SS} = –2.4 V must be 1.3 times of that applies when V_{SS} = –2.7 V to –4.5 V.

Output timing characteristics



Unless otherwise specified V_{SS}=–5.0V±10%, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	C_L=15pF	30	300	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V	–	3.0	µs
($\overline{INH}$ to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}	C_L=100pF	–	3.0	µs

Unless otherwise specified V_{SS}=–2.7V to –4.5V, Ta=–40 to 85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	t_{pdDOCL}	C_L=15pF	60	600	ns
(YSCL - fall to COM output) delay time	t_{pdCCL}	V_5=–7.0 to –28.0V	–	3.0	µs
($\overline{INH}$ to COM output) delay time	t_{pdCINH}				
(FR to COM output) delay time	t_{pdCFR}	C_L=100pF	–	3.0	µs

The standard applicable when V_{SS} = –2.4 V must be 1.3 times of that applies when V_{SS} = –2.7 V to –4.5 V.

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is the most simple to divide the resistance of potential as shown in the connection example.
On the other hand, to obtain a high quality display, it is necessary to raise the accuracy and constancy of each voltage level and to set the divided resistance value as low as possible in the range of system power capacity.
Especially when a low-power LCD driving is required, set the divided resistance to a higher value and drive the LCD with a voltage follower by means of operational amplifier instead. In taking into consideration of a case where the operational amplifier is employed, the maximum potential level V_0 for LCD driving has been isolated from the V_{DD} pin. When the potential of V_0 lowers than that of V_{DD} and the potential difference between the two becomes larger, however, the capacity of LCD drive output driver lowers. To avoid it, use the system with the potential difference of 0 V to 2.5 V between V_0 and V_{DD}.
When no operational amplifier is used, connect V_0 and V_{DD} pins.

Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating, an overcurrent flows and LSI breaks down in some cases.

Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

Precautions:

Users of this development specification are reminded of the following precautions.

1. This development specification is subject to change without previous notice.
2. This specificatino does not warrant the user to exercise the industrial property right or other rights, nor does this specification vest such rights to the user.
   Application examples provided in this specification are solely intended to ensure better understanding of the product. The manufacturer shall not be liable for any circuit related problem arising from using such examples.
   Numeric representation of measure or size provided in the characteristics table is one obtained from the numeric line.
3. No part of this specification may be reproduced or duplicated in any form or by any means without the written permission of the manufacturer.
4. As for use of semiconductor elements, users are required to pay attention to the following points.
   [Precautions on the Product Handling in Light]
   Characteristics of semiconductor elements are changed if they are exposed to light. Thus, exposing this IC to light can result in its in malfunction. In order to prevent IC malfunctioning due to light, make sure that the following measures are taken for the boards or products equipped with our IC.
   (1) Design and mounting procedure employed do not allow light to IC.
   (2) The inspection process is implemented in the environment that does not allow light to IC.
   (3) Light shielding measures are established not only for surface of IC but also for rear face and side faces, too.

DIFFERENT POINTS FROM REPLACEMENT PRODUCT

	SED1672*0*	SED1630**
Function	Bidirectional shift register $\overline{INH}$ 68 output segments	Bidirectional shift register $\overline{INH}$ 68 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	–
PAD coordinates	Different from the equivalent product	–

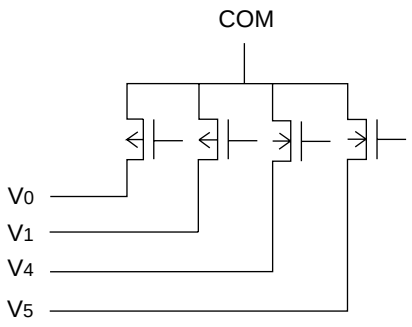


Fig. 1

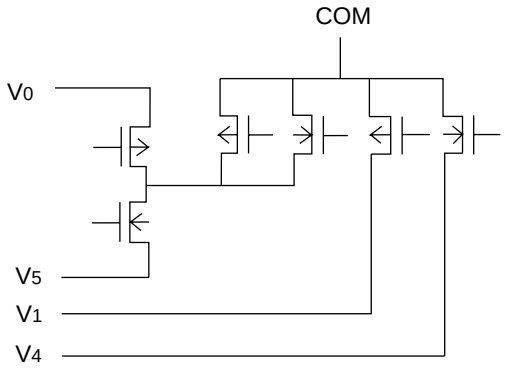


FIg. 2