MF426-03a

EPSON

SED1700 Series

LCD Drivers

Technical Manual

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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SED1700 Series Selection Guide

■LCD drivers for large-sized displays

High-speed drivers for large-sized dot-matrix displays that complement SEIKO EPSON's dedicated LCD controllers.

SED1700 series

● **Segment drivers**

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Data bus	Package	Application
SED1722D0A	4.5–5.5	14Å¦40	1/100 –1/500	80	4-bit parallel	Al pad chip	Used with the SED1733
SED1722F0A						QFP5-100pin	
SED1724D0A					8-bit parallel	Al pad chip	
SED1724F0A						QFP5-100pin	
SED1742D1B	2.7–5.5			160	4-bit parallel	Au bump chip	Used with the SED1743
SED1742T0A						TCP (Outer lead pitch 0.18mm)	
SED1744D1B					8-bit parallel	Au bump chip	
SED1744T0A						TCP (Outer lead pitch 0.18mm)	
SED1748D0B		14–42				Au bump chip	
SED1748T0A						TCP (Outer lead pitch 0.092mm)	
SED1758D0B						Au bump chip	
SED1758T0A						Slim TCP (Outer lead pitch 0.092 mm)	
SED1758T0B						Flex TCP (Outer lead pitch 0.092 mm)	
SED1758T0G						Ultra slim TCP (Outer lead pitch 0.080 mm)	
SED1752T0A				240		Slim TCP (Outer lead pitch 0.070 mm)	
SED1752T0B						Ultra slim TCP (Outer lead pitch 0.070 mm)	
SED17A0T0A*						Ultra slim TCP (Outer lead pitch 0.070 mm)	
SED1756D0A	4.5–5.5	14–40	1/100 –1/400	240	8-bit parallel	Al pad chip (For COG)	Used with the SED1755

* : Under development

● **Common Drivers**

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Outputs	Package	Application
SED1733D0A	4.5–5.5	14–40	1/100 –1/400	100	Al pad chip	
SED1733F0A					QFP5-128pin	
SED1743D1B	2.7–5.5		1/100 –1/500	160	Au bump chip	
SED1743T0A					TCP (Outer lead pitch 0.18mm)	
SED1741D1B		14–42		100	Au bump chip	
SED1741T1B*					TCP	
SED1753D0B				120	Au bump chip	
SED1753T0A					TCP	
SED1755D0A				240	Al pad chip (For COG)	Used with the SED1756

* : Under development

■LCD drivers for grayscale displays

Controlling the lighting time, they avail gray-scale displays in 16 or 64 levels on the LCD panel. The applicable type of panel differs depending on the speed, withstanding voltage and driving method.

● **MIM LCD Drivers**

SED1760 series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Data bus	Package	Application
SED1765D0A	4.5–5.5	14–40	1/100–1/500	160	–	4-bit parallel x 2	Al pad chip	For MIM-type displays
SED1765D0B							Au bump chip	PWM technology
SED1765T0A							TCP (Outer lead pitch: 0.18mm)	16-level gray
SED1766D0A							Al pad chip	For STN-type displays
SED1766D0B							Au bump chip	PWM technology
SED1766T0A							TCP (Outer lead pitch: 0.18mm)	16-level gray

● **TFT LCD Drivers**

SED1770 series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment outputs	Data inputs	Package	Application
SED1770D0A	4.5–5.5	5–17	–	160	3 (R,G,B)	Au bump chip	For MIM- or TFT-type displays
SED1771D0A			–	162			

1. SED1741D1B
LCD Driver

Contents

1. OVERVIEW

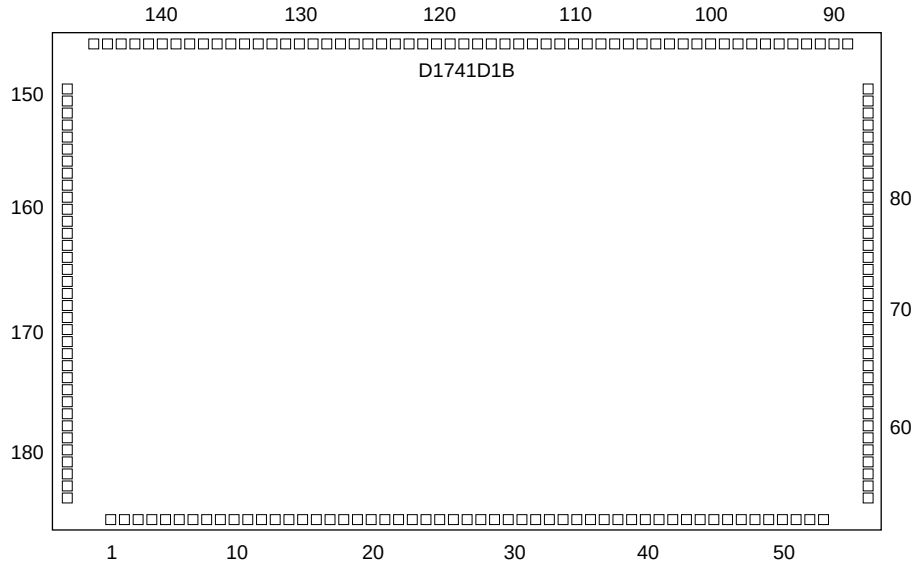
The SED1741 is a 100-output low output resistance common (low) driver most applicable to drive the extra large-capacity dot matrix liquid crystal panel, which is paired with the SED1742, SED1744 SED1748 SED1758. It can be applied in a wide range of applications, as the range of the liquid crystal drive voltage is wide, with capacity to potential high-resolution application, and the long type chip layout allows for smaller LCD panels.

The pad layout that allows easy mounting of the board, bidirectional selection of driver output sequence, high pressure resistance, 50 × 2 pairs of low output impedance LCD output allows the highest driver use efficiency against the 1/200, 1/400 duty panels.

2. FEATURES

- LCD drive outputs : 100 (50 × 2 structure)
- Low-voltage operation time : 2.7 V min
- Common output ON resistance : 0.7 kOhm (Typ.)
- High duty drive applicable : 1/500
- Output shift direction pin selectable
- Clock stop detection circuit incorporated
- Non-bias display off function
- Long side-ways chip
- Offset bias of liquid crystal power supply against VDDH, GND level adjustable
- Wide range of liquid crystal drive voltage : +8 to +42 V
- Logic system power supply : 2.7 to 5.5 V
- Shipment : Chip SED1741D1B
  TCP SED1741T**

3. PAD ARRANGEMENT



Chip size	7.30 mm × 4.48 mm
Pad pitch	108 um (Min.)
Chip thickness	525 um ±25 um

1) Au Bump specifications (SED 1741D1B) Referencial value

Scribe horizontal × Scribe vertical ±tolerance

Bump size A 72 µm × 93 µm ±4 µm (Pad No. 1 to 15, 39 to 183)
Bump size B 93 µm × 106 µm ±4 µm (Pad No. 16 to 33, 38)
Bump size C 93 µm × 93 µm ±4 µm (Pad No. 34 to 37)

4. PAD COORDINATES

SED 1741 Pad Center coordinate

Unit : um

PAD NO.	PIN NAME	X	Y	PAD NO.	PIN NAME	X	Y	PAD NO.	PIN NAME	X	Y
1	NC	– 3228	– 2064	63	NC	3474	– 866	125	0 56	– 704	2064
2	NC	– 3120		64	-NC		– 758	126	57	– 812	
3	NC	– 3012		65	NC		– 650	127	58	– 921	
4	NC	– 2903		66	NC		– 542	128	59	– 1029	
5	NC	– 2795		67	NC		– 433	129	60	– 1137	
6	NC	– 2687		68	NC		– 325	130	61	– 1245	
7	NC	– 2578		69	0 0		– 217	131	62	– 1354	
8	NC	– 2470		70	1		– 108	132	63	– 1462	
9	NC	– 2362		71	2		0	133	64	– 1570	
10	NC	– 2253		72	3		108	134	65	– 1679	
11	NC	– 2145		73	4		217	135	66	– 1787	
12	NC	– 2037		74	5		325	136	67	– 1895	
13	NC	– 1929		75	6		433	137	68	– 2004	
14	NC	– 1820		76	7		542	138	69	– 2112	
15	NC	– 1712	↓	77	8		650	139	70	– 2220	
16	DIO2	– 1550	– 2058	78	9		758	140	71	– 2328	
17	DIO1	– 1417		79	10		866	141	72	– 2437	
18	GND	– 1284		80	11		975	142	73	– 2545	
19	SEL	– 1151		81	12		1083	143	74	– 2653	
20	OP1	– 1018		82	13		1191	144	75	– 2762	
21	C1	– 885		83	14		1300	145	76	– 2870	
22	IP1	– 752		84	15		1408	146	77	– 2978	
23	C2	– 619		85	16		1516	147	78	– 3087	
24	IP2	– 486		86	17		1625	148	79	– 3195	↓
25	DI3	– 353		87	18		1733	149	80	– 3474	1841
26	IP3	– 220		88	19	↓	1841	150	81		1733
27	SHL	– 87		89	20	3195	2064	151	82		1625
28	YSCL	46		90	21	3087		152	83		1516
29	IP4	179		91	22	2978		153	84		1408
30	INH	312		92	23	2870		154	85		1300
31	OP2	445		93	24	2762		155	86		1191
32	V_{CC}	578		94	25	2653		156	87		1083
33	FR	711	↓	95	26	2545		157	88		975
34	V5	872	– 2026	96	27	2437		158	89		866
35	V4	1034		97	28	2328		159	90		758
36	V1	1195		98	29	2220		160	91		650
37	V0	1357	↓	99	30	2112		161	92		542
38	V_{DDH}	1550	– 2058	100	31	2004		162	93		433
39	NC	1712	– 2064	101	32	1895		163	94		325
40	NC	1820		102	33	1787		164	95		217
41	NC	1929		103	34	1679		165	96		108
42	NC	2037		104	35	1570		166	97		0
43	NC	2145		105	36	1462		167	98		– 108
44	NC	2253		106	37	1354		168	99		– 217
45	NC	2362		107	38	1245		169	NC		– 325
46	NC	2470		108	39	1137		170	NC		– 433
47	NC	2578		109	40	1029		171	NC		– 542
48	NC	2687		110	41	921		172	NC		– 650
49	NC	2795		111	42	812		173	NC		– 758
50	NC	2903		112	43	704		174	NC		– 866
51	NC	3012		113	44	596		175	NC		– 975
52	NC	3120		114	45	487		176	NC		– 1083
53	NC	3228	↓	115	46	379		177	NC		– 1191
54	NC	3474	– 1841	116	47	271		178	NC		– 1300
55	NC		– 1733	117	48	162		179	NC		– 1408
56	NC		– 1625	118	49	54		180	NC		– 1516
57	NC		– 1516	119	50	– 54		181	NC		– 1625
58	NC		– 1408	120	51	– 162		182	NC		– 1733
59	NC		– 1300	121	52	– 271		183	NC	↓	– 1841
60	NC		– 1191	122	53	– 379					
61	NC		– 1083	123	54	– 487					
62	NC	↓	– 975	124	55	– 596	↓				

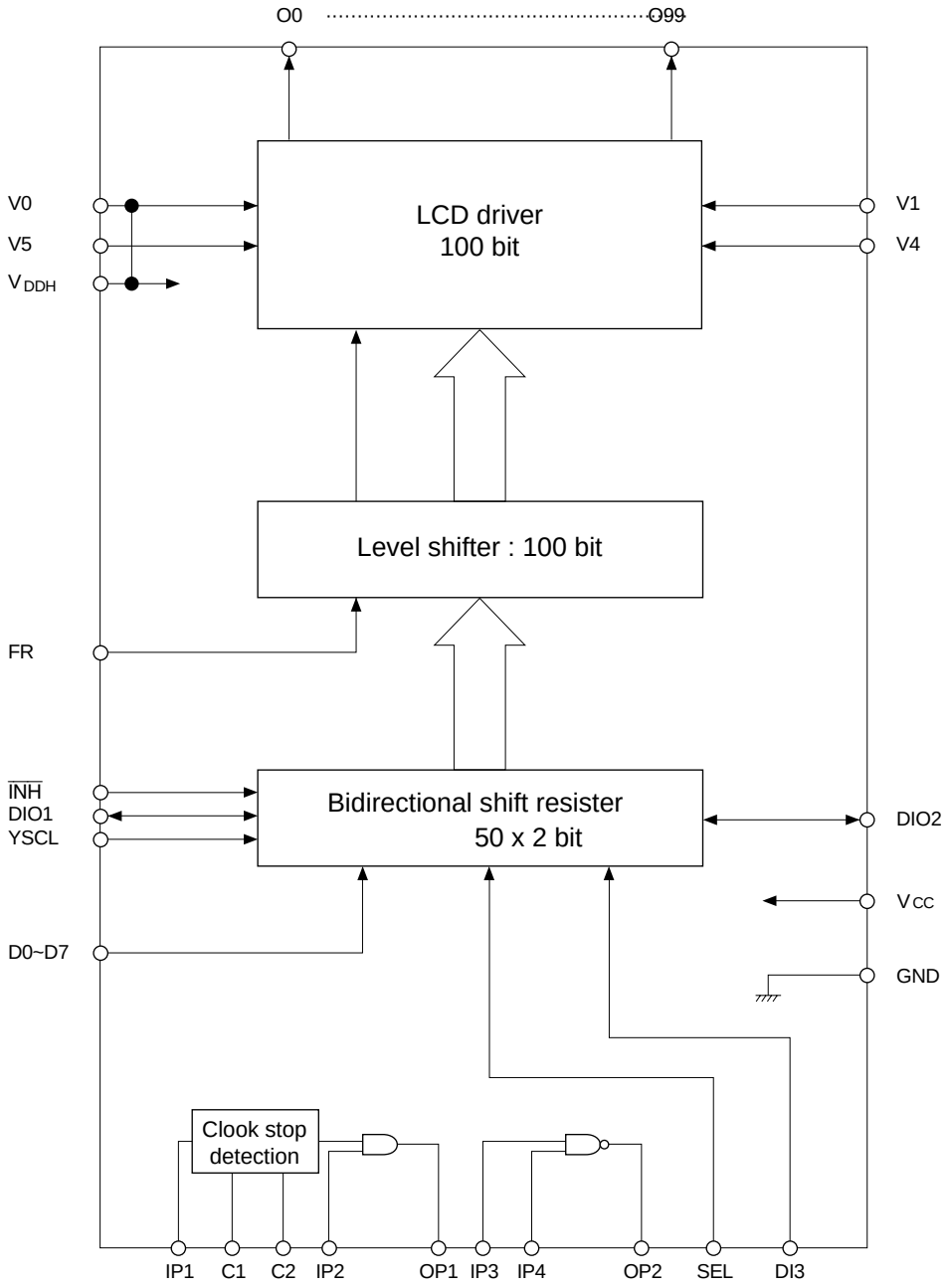
5. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Numbers of pins</th></tr>
<tr><td>O0~ O99</td><td>O</td><td>Common (low) output for liquid crystal drive.
Changes at the edge of YSCL fall.</td><td>100
NC 60</td></tr>
<tr><td>DIO1
DIO2
DI3</td><td>I/O

I</td><td>50 × 2 bit bidirectional shift register scan pulse
Set at the input or output by SHL input DI3
DI3 is the scan pulse input terminal for the 50 × 2 structure.
When SEL = L, connected DI3 = GBD.</td><td>3</td></tr>
<tr><td>SEL</td><td>I</td><td>Bidirectional shift register operation mode selection input.
H : 50 × 2 (DI3 input) L : 100</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input
Shifts the scan data at the edge of fall.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO terminal input/output control input
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">O Output shift direction</th><th colspan="2">DIO</th></tr>
<tr><th>DI01</th><th>DI02</th></tr>
<tr><td>L</td><td>0 ——————→ 99</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>99 ——————→ 0</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Liquid crystal drive output alternating signal input</td><td>1</td></tr>
<tr><td>VCC, GND</td><td>Power supply</td><td>Logical power supply GND : 0 V VCC : +2.7 to 5.5V</td><td>2</td></tr>
<tr><td>V0, V1, V4, V5, VDDH</td><td>Power supply</td><td>Liquid crystal drive power supply
GND : 0 V VDDH : +8 to +42V
VDDH (V0 ≥ V1 ≥ 8/9VDDH
1/9 VDDH ≥V4 ≥ V5 ≥ GND</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Liquid crystal display blanking control input
All common outputs become level V5 by low-level input</td><td>1</td></tr>
<tr><td>IP1</td><td>I</td><td>Stop detection clock input</td><td>1</td></tr>
<tr><td>IP2</td><td>I</td><td>Stop detection output and AND-applied signal input, with pull-down resister</td><td>1</td></tr>
<tr><td>C1</td><td>O</td><td>First electric charge hold terminal; external capacitor between GND</td><td>1</td></tr>
<tr><td>C2</td><td>O</td><td>Second electric charge hold terminal; external capacitor and resistor between GND</td><td>1</td></tr>
<tr><td>OP1</td><td>O</td><td>CLock stop detection output</td><td>1</td></tr>
<tr><td>IP3</td><td>I</td><td>NAND gate input; with pull-down resistor</td><td>1</td></tr>
<tr><td>IP4</td><td>I</td><td>NAND gate input</td><td>1</td></tr>
<tr><td>OP2</td><td>O</td><td>NAND gate output</td><td>1</td></tr>
</table>

Total 183 (NC 60)

6. BLOCK DIAGRAM



7. BLOCK FUNCTIONS

7-1 Shift Register

Bidirectional shift register for common data transfer.

7-2 Level Shifter

Voltage level interface circuit for conversion of the voltage level of the signal from logical level to liquid crystal drive level.

7-3 LCD Driver

Outputs liquid crystal drive voltage.
The relation between the display blanking signal INH, contents of shift register, alternating signal FR, and common output voltage is as shown below.

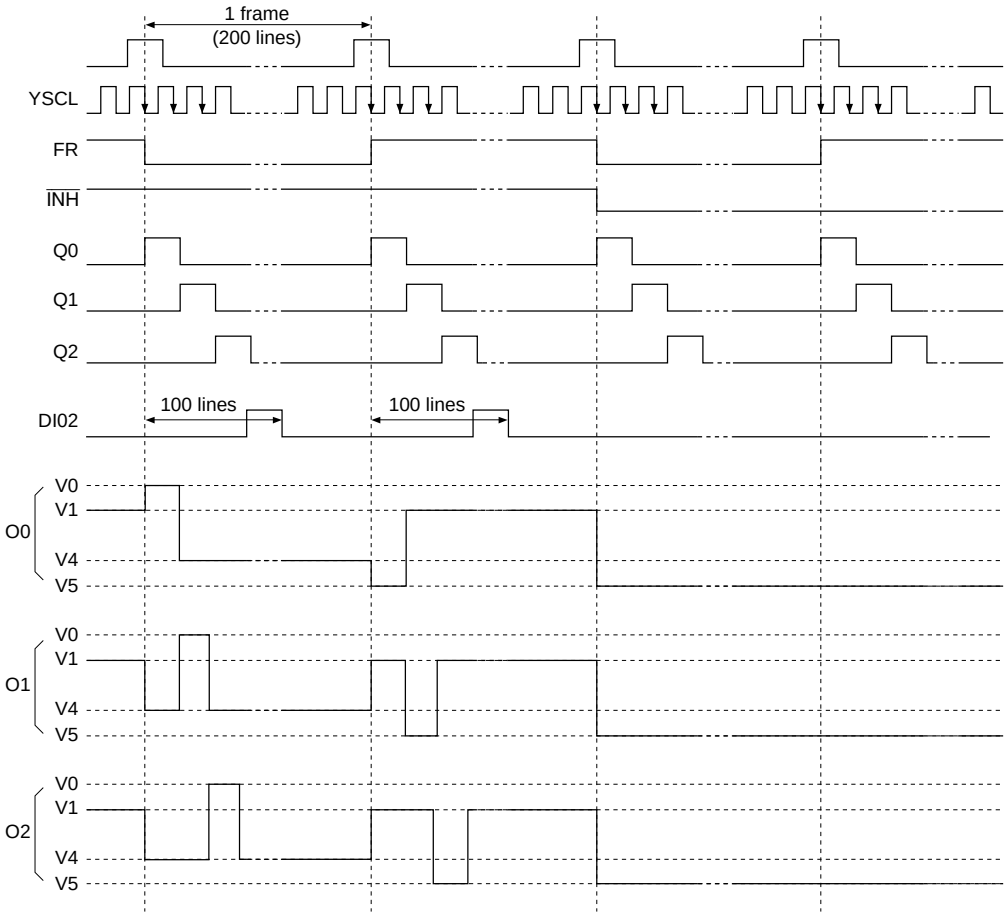
$\overline{INH}$	Shift register	FR	Output voltage
H	H	H	V_5
		L	V_0 (V_{DDH})
	L	H	V_1
		L	V_4
L	–	–	V_5

7-4 Clock Stop Detection Circuit

When the alternative drive clock stopped with voltage applied to the liquid crystal cell, the direct current of the liquid crystal cell may deteriorate. This circuit detects any stop of the alternative drive clock, and inputs the detected signal to the INH terminal, to prevent the voltage to be applied to the liquid crystal cell.

7-5 Timing Diagram

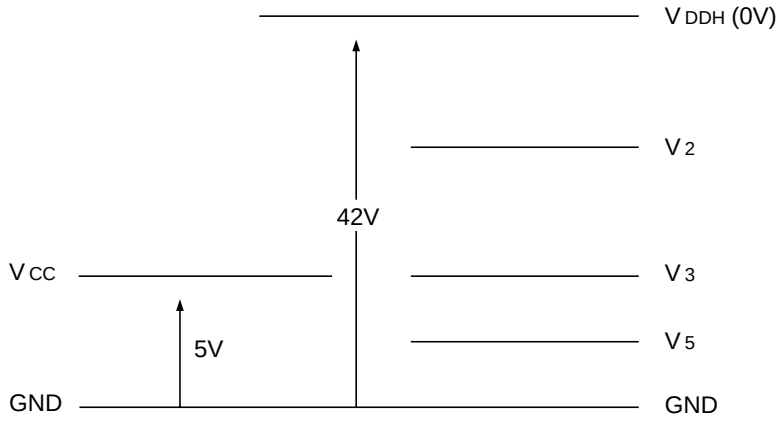
Timing diagram HSL = “L”
When it is 1/200 duty (example for reference)



8. ABSOLUTE MAXIMUM RATING

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 ~ +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 ~ +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	GND–0.3 ~ V_{DDH} + 0.3	V
Input voltage	V_I	GND–0.3 ~ V_{CC} + 0.3	V
Output voltage	V_O	GND–0.3 ~ V_{DD} + 0.3	V
EIO output current	I_{01}	20	mA
Working temperature	Topr	–20 ~ +75	°C
Storage temperature 1	Tstg1	–65 ~ +150	°C
Storage temperature 2	Tstg2	–55 ~ +100	°C

(Note 1) All stated voltages assume that GND = 0V.
(Note 2) Shelf temperature 1 is for individual chips, while shelf temperature 2 is for actual TCP mounted conditions.
(Note 3) V_0, V_2, V_3 voltages shall always maintain the condition of V_{DDH} (V_0) ≥ V2 ≥ V3 ≥ V5 ≥ GND.



(Note 4) Avoid floating status of the logical power supply during application of liquid crystal drive power, or fall of the power below V_{CC} = 2.6 V; the LSI may be destroyed permanently.
Special notice is required for the power sequence when turning on or off the system power.

9. ELECTRIC CHARACTERISTICS

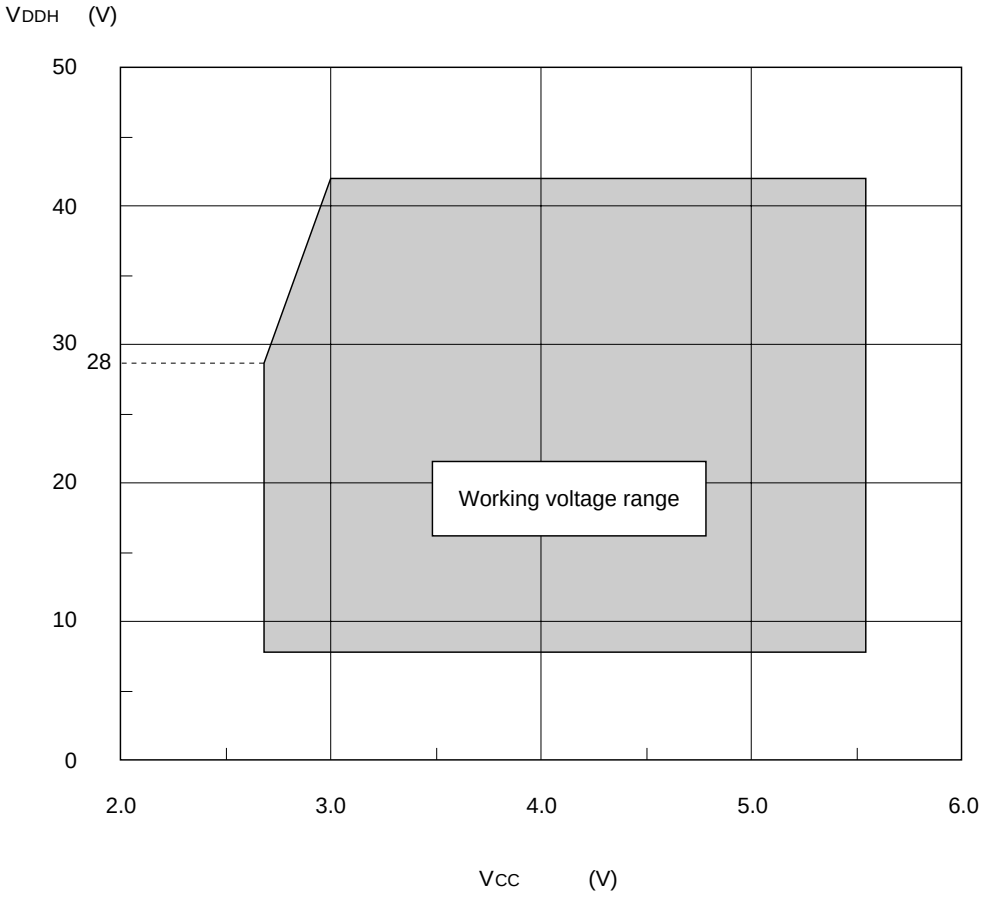
9-1 DC Characteristics

Unless otherwise specified, GND = 0V, V_{CC} = +5.0 V ±10%, Ta = –20 to 75°C

Item	Symbol	Condition		Applicable pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Recommended working voltage	V_{DDH} V_0			VDDH, V0	14.0		40.0	V
Workable voltage	V_{DDH}, V_0	Function only		VDDH, V0	8.0		42.0	V
Supply voltage (2)	V_1	Recommended value		V1	8/9V_{DDH}			V
Supply voltage (3)	V_4	Recommended value		V4	GND		1/9V_{DDH}	V
High level input voltage	V_{IH}	V_{CC} = 2.7 ~ 5.5V		DIO1,DIO2,DI3 IP1~4,SEL, FR YSCL, SHL,$\overline{INH}$	0.8V_{CC}			V
Low level input voltage	V_{IL}						0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC}= 2.7~ 5.5V	IOH = –0.3mA	DIO1, DIO2 OP1, OP2	V_{CC}–0.4			V
Low level output voltage	V_{OL}		IOL = 0.3mA				0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		DI3, SEL, FR YSCL, SHL, $\overline{INH}$			2.0	µA
Input current	I_{IH}	V_{IN} ≤ V_{CC} (IP4=C2=GND)		IP2, IP3	40	80	180	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		DIO1, DIO2			5.0	µA
Rest current	I_{GND}	V_{DDH} = 14.0~42.0V V_{IH} = V_{CC}, V_{IL}=GND		GND			25	µA
Output resistance	R_{COM}	△V_{ON} =0.5V	V_{DDH} =+30.0V	O 0~ O 99		0.65	2.0	KΩ
		Recom-mended condition	V_{DDH} =+20.0V			0.7	2.1	
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, fYSCL = 33.6KHz fFR = 70Hz Input data: 1/480, no-load		V_{CC}		9	20	µA
		V_{CC} = 2.7V Other conditions are the same as those when V_{CC} = 5V.				6	10	
Mean working current consumption (2)	I_{DDH}	V_{DDH} = V_0 = +30.0V V_1 = +28.0V, V_4 = +2.0V V_5 = 0, 0V, V_{CC} = +5.0V Other conditions are the same as those in the I_{DD} column.		V_{DDH}		4	25	µA
Input terminal capacity	CI	Freq. = 1 MHz Ta = 25°C Independent chips		DI3, IP1~4, SEL, FR, YSCL,SEL, $\overline{INH}$			8	pF
I/O terminal capacity	CI/0			DIO1, DIO2			15	pF

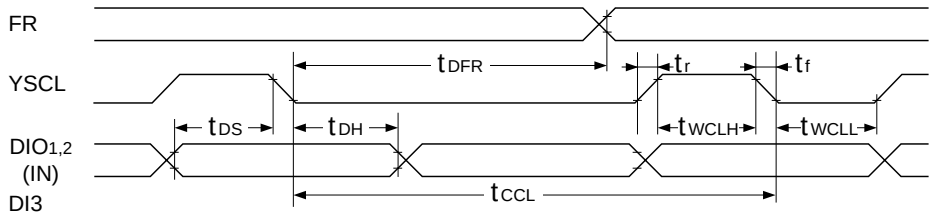
Operation voltage range VCC - VDDH

The VDDH voltage must be set within the following VCC - VDD operation voltage range.



9-2 AC Characteristics

Input timing characteristics



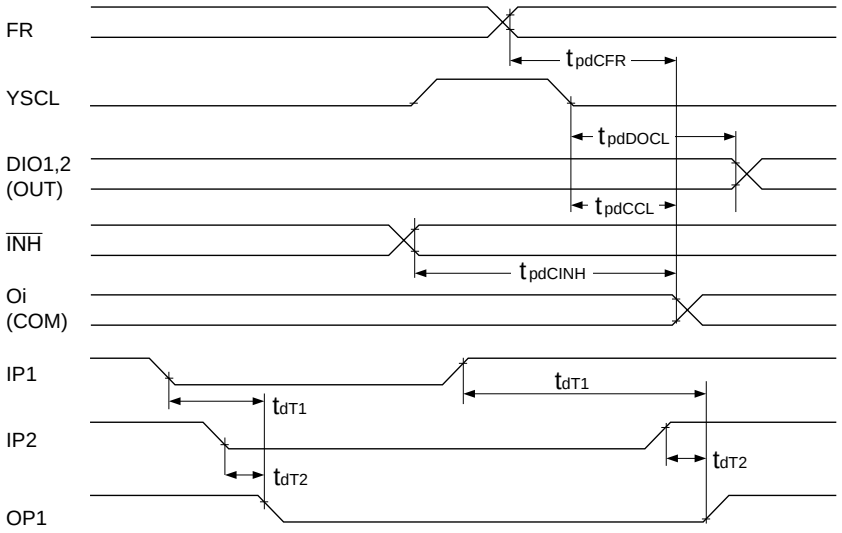
V_{CC} = +5.0V ±10%, Ta = –20 to 75°C

Items	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}		400		ns
YSCL high level pulse duration	t_{WCLH}		60		ns
YSCL low level pulse duration	t_{WCLL}		330		ns
Data setup time	t_{DS}		40		ns
Data hold time	t_{DH}		40		ns
FR delay allowance	t_{DFR}		–300	+300	ns
Input signal rise time	t_r			50	ns
Input signal fall time	t_f			50	ns

V_{CC} = +2.7V to 4.5V, Ta = –20 to 75°C

Items	Symbol	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}		800		ns
YSCL high level pulse duration	t_{WCLH}		80		ns
YSCL low level pulse duration	t_{WCLL}		660		ns
Data setup time	t_{DS}		50		ns
Data hold time	t_{DH}		50		ns
FR delay allowance	t_{DFR}		–400	+400	ns
Input signal rise time	t_r			100	ns
Input signal fall time	t_f			100	ns

Output timing characteristics



V_{CC} = +5.0V ±10%, V_{DDH} = +14.0 to +42.0V

Items	Symbol	Conditions	Min.	Max.	Units
YSCL→DIO output delay time	t_{pdDOCL}	C_L = 15pF		100	ns
YSCL→COM output delay time	t_{pdCCL}	V_{DDH} = 14.0V		160	ns
INH→COM output delay time	t_{pdCINH}	~45.0V		160	ns
FR→COM output delay time	t_{pdCFR}	C_L = 100pF		160	ns
IP1→OP1 output delay time	t_{d1}	C_L = 15pF		4C2•R2	ns
IP1→OP1 output reset time	t_{dT1}			2×YD cycle	ns
IP2→OP1 output delay time	t_{d2}			100	ns
IP2→OP1 output reset time	t_{dT2}			100	ns

V_{CC} = +2.7V to +4.5V, V_{DDH} = +14.0 to +28.0V

Items	Symbol	Conditions	Min.	Max.	Units
YSCL→DIO output delay time	t_{pdDOCL}	C_L = 15pF		200	ns
YSCL→COM output delay time	t_{pdCCL}	V_{DDH} = 14.0V		300	ns
INH→COM output delay time	t_{pdCINH}	~45.0V		300	ns
FR→COM output delay time	t_{pdCFR}	C_L = 100pF		300	ns
IP1→OP1 output delay time	t_{d1}	C_L = 15pF		4C2•R2	ns
IP1→OP1 output reset time	t_{dT1}			2×YD cycle	ns
IP2→OP1 output delay time	t_{d2}			200	ns
IP2→OP1 output reset time	t_{dT2}			200	ns

* YD: Scan start pulse
See Chapter 11 “Clock stop detection circuit” for details on C2R2.

10. LIQUID CRYSTAL DRIVE POWER

10-1 Formation of Voltage Levels

The optimum way to obtain the voltage levels to drive the liquid crystal, is to divide the resistance so that it can be driven by the voltage follower of the operation amplifier. The terminal for the maximum potential level V_0 and V_{DDH} of the liquid crystal drive is separated from the minimum potential level V_5 and GND, considering the use of the operation amplifier.
However, if the potential of V_0 (V_5) falls below (rises above) V_{DDH} (GND), causing the voltage to be too large, the capacity of the liquid crystal driver will deteriorate, so it is recommended that the voltage kept between 0 V and 2.5 V.
If the operation amplifier is not used, connect V_0 and V_{DDH}, V_5 and GND. When resistance division is to be used, set the resistance as low as possible within the allowable power range of the system.

When the V_{DDH} (GND) power line has serial resistance, the I_{DDH} at the change of the signal will cause V_{DDH} (GND) voltage fall at the LSI power terminal, disabling the relation of the LCD with the intermittent potential ($V_{DDH} = V_0 \geq V_1 \geq V_4 \geq V_5 \geq$ GND), thus causing large current to flow and destroy the LSI.
When inserting a protection resister, the voltage must be stabilized by the capacity.

10-2 Notes Upon Power On/Off

This LSI has high voltage in the liquid crystal system, and if voltage higher than 30 V is applied to the liquid crystal drive system with the power of the logic system at the floating level or below V_{CC} = 2.6 V, or if liquid crystal drive signal is output before the voltage applied to the liquid crystal drive system is stabilized, overcurrent flows to destroy the LSI.
Therefore, it is recommended to maintain the liquid crystal drive output voltage at the V_5 level till the voltage of the liquid crystal drive system stabilizes, using the display off function ($\overline{INH}$).

Observe the following power on/off sequence.

Power on Logic system on → liquid crystal drive system on, or simultaneously on
Power off Liquid crystal drive system on → logic system off, or simultaneously off

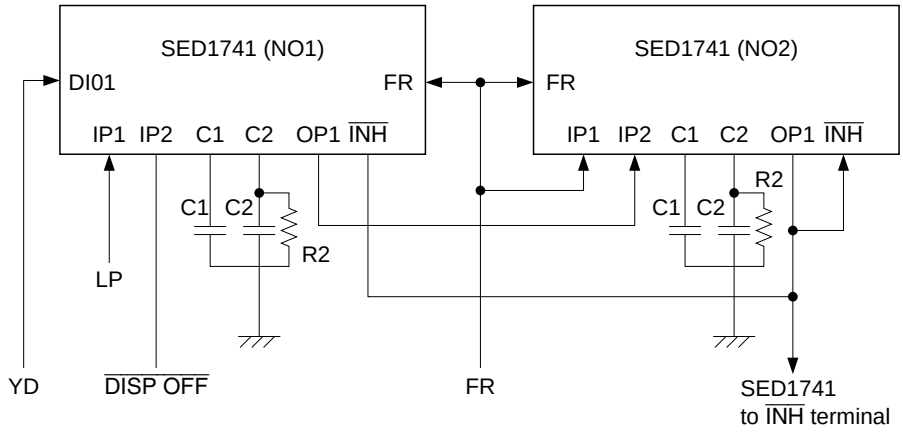
A fast melting fuse or protection resistance inserted in series with the liquid crystal power supply is effective as protection against overcurrent.

The optimum protection resistance must be selected from the capacity of the liquid crystal cell.

11. CLOCK STOP DETECTION CIRCUIT

The clock stop detection circuit sets OP1 at the "L" level when the operation signal from the controller stops. The OP1 terminal can be connected to the INH terminal so that voltage is not applied to the liquid crystal cell, and prevent the liquid crystal cell direct current deterioration occurred upon power off of the system.

◉ Example of circuit that stops the LP or FR signal



◉ Example of setting of C1, C2, R2

1. Set R2 at some MOhms.
2. While maintaining the relation of C1 ≫ C2, decide C1, C2, monitoring the output of OP1.

Reference : When the duty of the input signal IP1 shifts largely form 50%, the error of the following expression may become large.

$$C2 = \frac{\text{(IP1 input signal "L" pulse width time)}}{0.4 \cdot R2}$$

3. The following table shows an actual example.

	IP1 = LP	IP1 = FR
C1	0.47µF	0.47µF
C2	0.047µF	0.047µF
R2	3.3MΩ	3.3MΩ

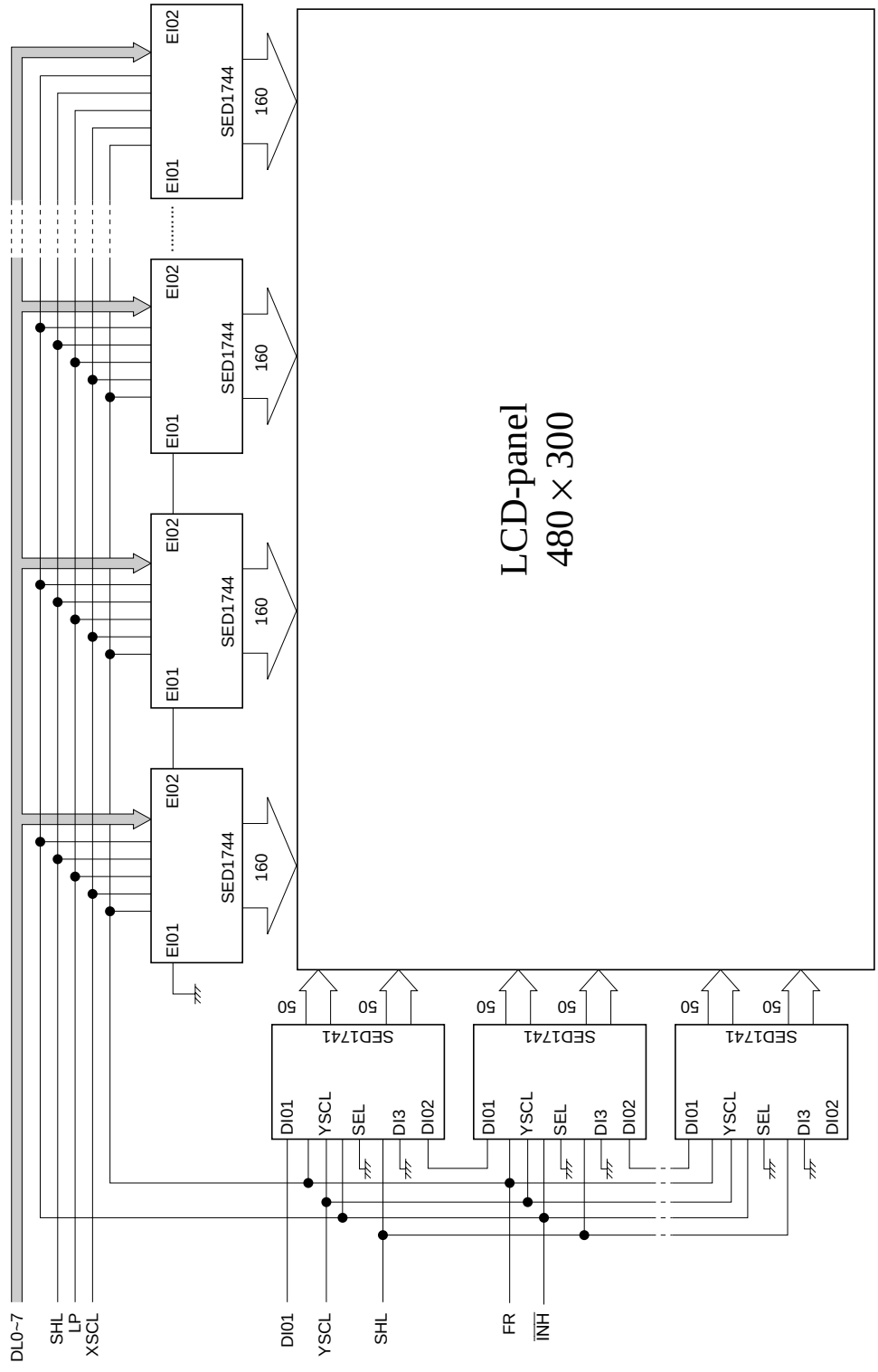
Conditions
YD tc = 17.8ms duty 0.14%
LP tc = 40.4us duty 0.35%
FR tc = 3.53ms duty 50%

When the stop detection circuit is not used, treat the terminal as follows.

- IP1 = C2 = "H", "L" or input signal DI3
  (When SEL = "L", it must be IP1 = C2 = DI3 = "H", "L".)
- Open OP1, OP2, C1, IP2, IP3
- IP4 = "H", "L" or input signal YSCL

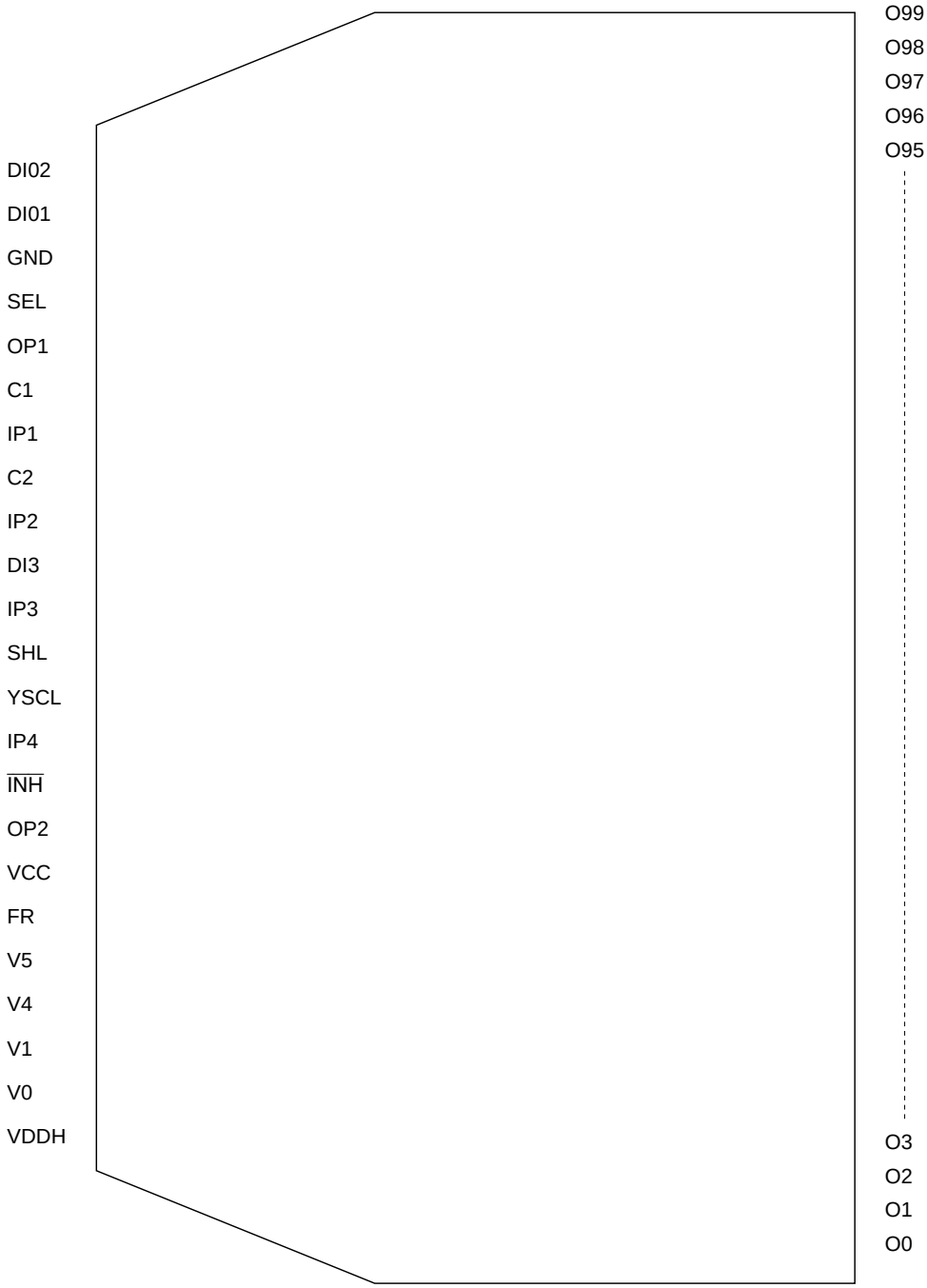
12. CONNECTION EXAMPLE

Large screen LCD structural diagram



13. SED 1741T TAB PIN ARRANGEMENT EXAMPLE

Note: This does not prescribe the external form of the tab.



2. SED1742
LCD Driver

Contents

1. OVERVIEW

The SED1742 is an LCD segment driver for high-resolution dot-matrix panels that incorporate 160 column driver outputs. It is designed for use in conjunction with the SED1743 row driver.

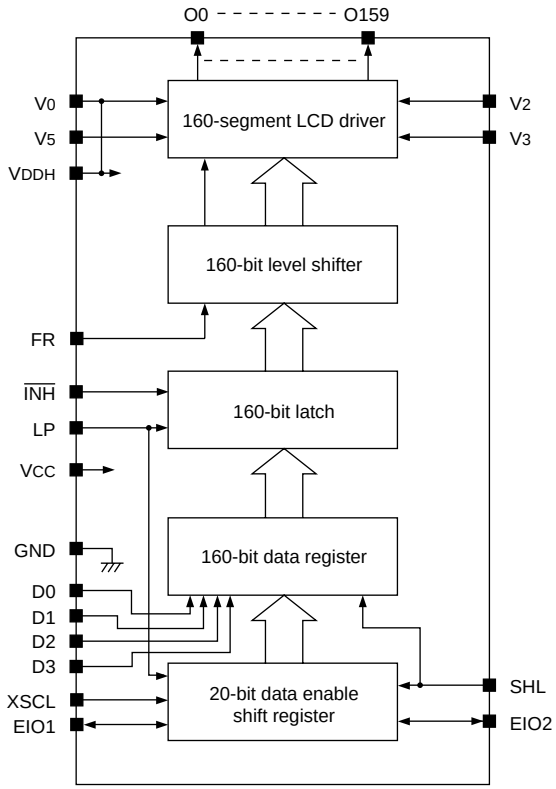
The SED1742 features a wide range of LCD drive voltages. The upper and lower drive voltages, V_0 and V_5, are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. As a result, the SED1742 is compatible with a large range of LCD panels.

The SED1742 uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver, thus simplifying system design. It also allows the SED1742 to be interfaced to either the SED1351F or SED1341 LCD controllers, or to any general-purpose microprocessor. The SED1742 operates from a 2.7 to 5.5 V supply and is available in both chip packages and tape-carrier packages (TCPs).

2. FEATURES

- 160 LCD segment drive outputs
- Supports dot-matrix displays up to 1120 × 750 pixels when used with the SED1743.
- 4-bit data bus
- Daisy-chained input/output enables
- Low-power, high-speed data transfer—12 MHz clock frequency at V_{CC} = 5 V ± 10% and 8 MHz clock frequency at V_{CC} = 2.7 V
- Pin-selectable output shift direction
- Adjustable LCD drive voltages
- Duty cycles up to 1/480
- Zero-bias display disable function
- Silicon-gate CMOS technology
- 2.7 to 5.5 V supply
- Chip (SED1742D$_{1B}$) or tape-carrier packages (SED1742T$_{0A}$)

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

Number	Name	Description
39 to 183, 1 to 15	O0 to O159	LCD segment drive outputs
16, 17	EIO2, EIO1	I/O enables
18	GND	Ground
19 to 22	D0 to D3	Display data inputs
23 to 26	NC	No connection
27	SHL	Shift direction select input
28	XSCL	Display data shift clock input. Negative-edge triggered
29	TEST	Test Input Tie LOW for normal operation.
30	$\overline{INH}$	Display blanking input. The SED1742 cannot be used with the SED1703 when $\overline{INH}$ is used.
31	LP	Display data latch strobe. Negative-edge triggered.
32	V_{CC}	Logic supply
33	FR	Segment drive signal polarity select input
34 to 38	V_5, V_3, V_2, V_0 and V_{DDH}	Segment drive voltage inputs

5. SPECIFICATIONS

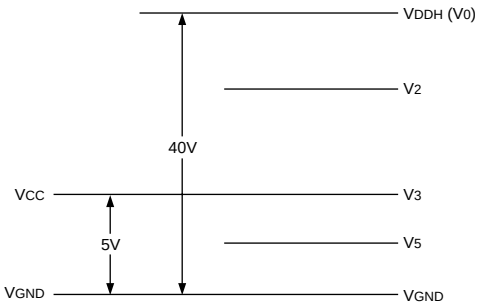
5-1 Absolute Maximum Ratings

V_{GND} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.3 to 7.0	V
	V_{DDH} (V_0)	–0.3 to 45.0	V
	V_2, V_3 and V_5	V_{GND} – 0.3 to V_{DDH} + 0.3	V
Input voltage range	V_I	V_{GND} – 0.3 to V_{CC} + 0.3	V
Output voltage range	V_O	V_{GND} – 0.3 to V_{CC} + 0.3	V
EIO output current	I_O	20	mA
Operating temperature range	Topg	–20 to 75	deg. C
Storage temperature range	Tstg	–65 to 150 ($SED1742D_{1B}$)	deg. C
		–55 to 100 ($SED1742T_{0A}$)	

Notes

1. Care should be taken during the power-on and power-off sequence. See Application Notes.
2. Display drive voltages should always be such that V_{DDH} (V_0) ≥ V_2 ≥ V_3 ≥ V_5 ≥ V_{GND} as shown in the following figure.



5-2 Recommended Operating Conditions

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	5	V
Segment driver supply voltage range	V_{DDH}	14 to 40	V

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	2.7	V
Segment driver supply voltage range	V_{DDH}	14 to 28	V

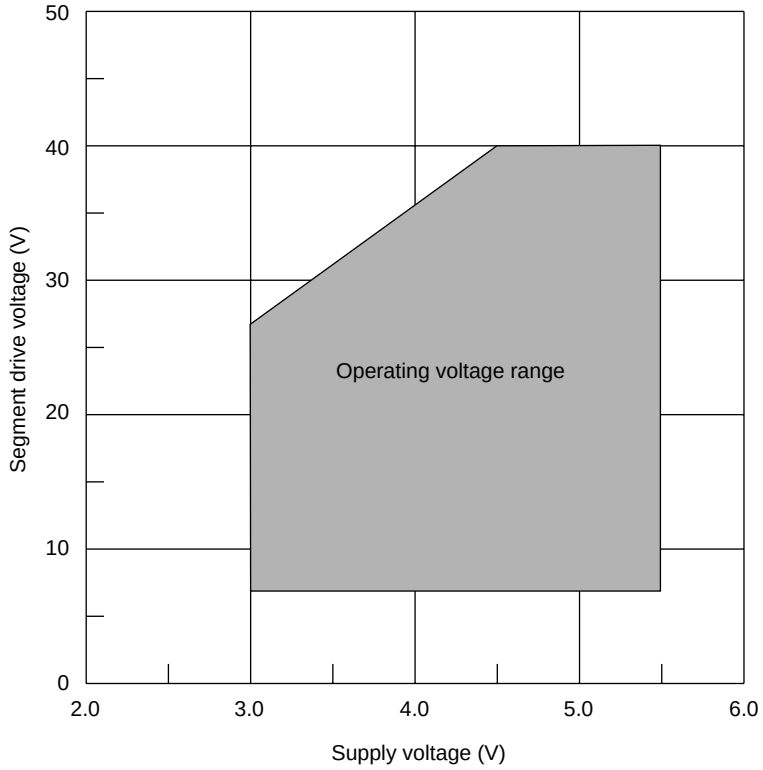
5-3 DC Electrical Characteristics

V_{CC} = 5 V ±10%, V_5 = 0 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
Segment driver supply voltage	V_{DDH}			8	—	—	V
Quiescent current	I_{GND}	V_{DDH} = 14 to 40 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}		—	—	25	µA
Operating current	I_{CC}	V_{CC} = 5 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}, f_{XSCL} = 5.38 MHz, f_{LP} = 33.6 kHz, frame frequency = 70 Hz, 1 bit alternating, Shimatsu display, no load		—	0.4	1.2	mA
		V_{CC} = 2.7 V, other conditions as above		—	0.2	0.6	mA
	I_{DDH}	V_{CC} = 5 V, V_3 = 4 V, V_2 = 26 V, V_{DDH} = V_0 = 30 V, V_5 = 0 V, other conditions as for I_{CC}		—	0.5	1.5	mA
Segment driver input voltage	V_2			7/9V_{DDH}	—	V_{DDH}	V
	V_3, V_5			V_{GND}	—	2/9V_{DDH}	V
LOW-level input voltage	V_{IL}	V_{CC} = 2.7 to 5.5 V		V_{GND}	—	0.2V_{CC}	V
HIGH-level input voltage	V_{IH}			0.8V_{CC}	—	V_{CC}	V
LOW-level output voltage	V_{OL}	V_{CC} = 2.7 to 5.5 V	I_{OH} = 0.6 mA	V_{GND}	—	0.4	V
HIGH-level output voltage	V_{OH}		I_{OH} = –0.6 mA	V_{CC} – 0.4	—	V_{CC}	V
Segment ON resistance	R_{SEG}	|ΔV_{ON}| = 0.5 V	V_{DDH} = 30 V	—	0.9	2.5	kΩ
			V_{DDH} = 20 V	—	1	3	
Input leakage current	I_{LI}	V_{GND} ≤ V_I ≤ V_{CC}		—	—	2	µA
Input/output leakage current	$I_{LI/O}$	V_{GND} ≤ V_I ≤ V_{CC}		—	—	5	µA
Input capacitance	C_I	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	8	pF
Input/output capacitance	$C_{I/O}$	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	15	pF

Operating voltage range

The maximum LCD supply voltage, V_{DDH}, depends on V_{CC} as shown in the following figure.



5.4 AC Electrical Characteristics

Input timing

V_{CC} = 5 V ±10%, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
XSCL period	t_C		83	—	ns
XSCL HIGH-level pulsewidth	t_{WCH}		30	—	ns
XSCL LOW-level pulsewidth	t_{WCL}		30	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		20	—	ns

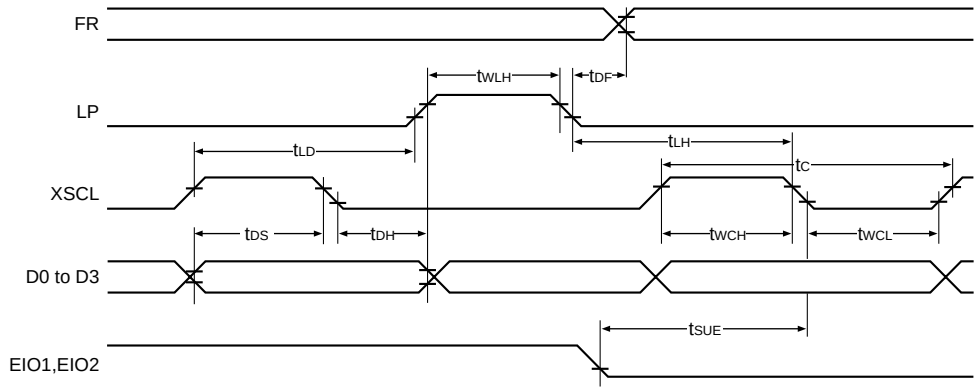
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
XSCL to LP rising edge	t_{LP}		–5	—	ns
LP to XSCL falling edge	t_{LH}		60	—	ns
LP HIGH-level pulsewidth	t_{WLH}	See note.	45	—	ns
FR delay time	t_{DF}		–300	300	ns
EIO setup time	t_{SUE}		35	—	ns

V_{CC} = 2.7 to 4.5 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
XSCL period	t_C		125	—	ns
XSCL HIGH-level pulsewidth	t_{WCH}		50	—	ns
XSCL LOW-level pulsewidth	t_{WCL}		50	—	ns
Data setup time	t_{DS}		50	—	ns
Data hold time	t_{DH}		30	—	ns
XSCL to LP rising edge	t_{LP}		0	—	ns
LP to XSCL falling edge	t_{LH}		120	—	ns
LP HIGH-level pulsewidth	t_{WLH}	See note.	90	—	ns
FR delay time	t_{DF}		–600	600	ns
EIO setup time	t_{SUE}		50	—	ns

Note
t_{WLH} indicates the period when XSCL is LOW and LP is HIGH.

Input timing waveform



Output timing

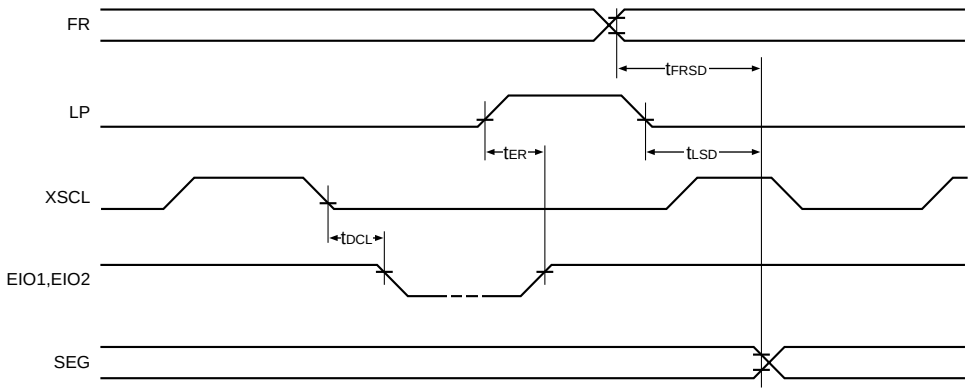
V_{CC} = 5 V ±10%, V_{DDH} = 14 to 40 V

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
EIO reset time	t_{ER}	C_L = 15 pF	—	120	ns
EIO output delay time	t_{DCL}		—	45	ns
LP to SEG delay time	t_{LSD}	C_L = 100 pF	—	200	ns
FR to SEG delay time	t_{FRSD}		—	400	ns

V_{CC} = 2.7 to 4.5 V, Ta = –20 to 75 deg. C

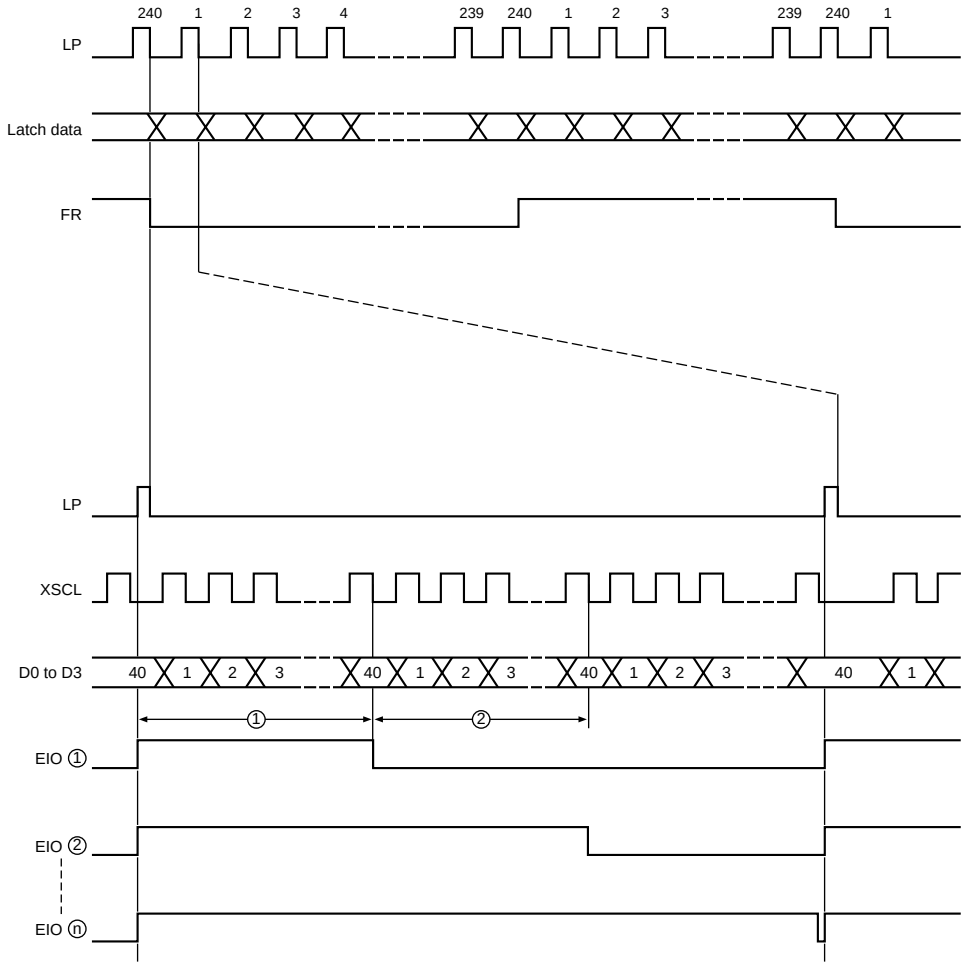
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
EIO reset time	t_{ER}	C_L = 15 pF	—	240	ns
EIO output delay time	t_{DCL}		—	72	ns
LP to SEG delay time	t_{LSD}	C_L = 100 pF	—	400	ns
FR to SEG delay time	t_{FRSD}		—	800	ns

Output timing waveform



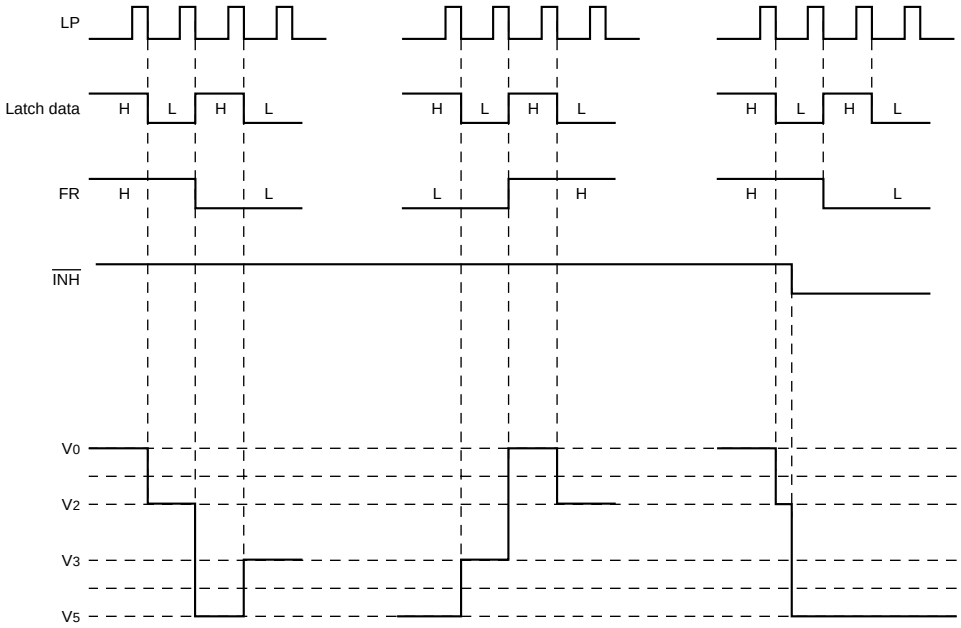
6. TIMING DIAGRAMS

1/240 Duty Cycle



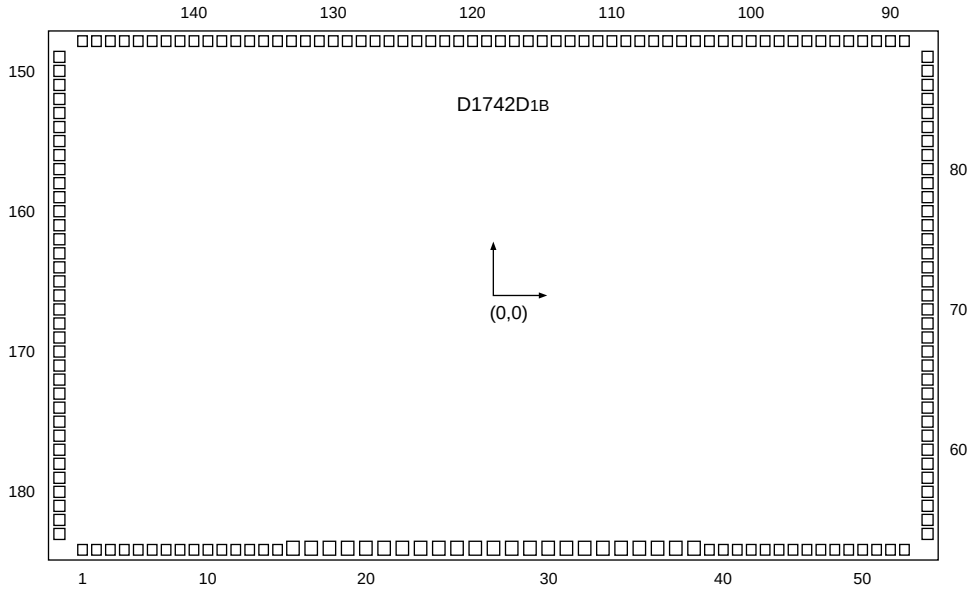
Notes

1. The circled numerals 1 to *n* denote the position of the device in the chain.
2. One cycle of XSCL should be lengthened to satisfy t_{LH} when high-speed data transfer takes place.


LP
Latch data
H
L
H
L
FR
H
L
INH
V0
V2
V3
V5

7. PACKAGE DIMENSIONS

7-1 Chip Package (SED1742D1B)



- ❒ Chip size: 7.30 × 4.48 mm
- ❒ Chip thickness: 525 ±25 µm
- ❒ Pad pitch: 108 µm (Min.)
- ❒ Gold bump dimensions (SED1742D1B):
  - Size A: 94 × 134 ±20 µm (pads 1 to 15, 39 to 183)
  - Size B: 115 × 148 ±20 µm (pads 16 to 33 and 38)
  - Size C: 115 × 134 ±20 µm (pads 34 to 37)

Pad coordinates

Unit: μm

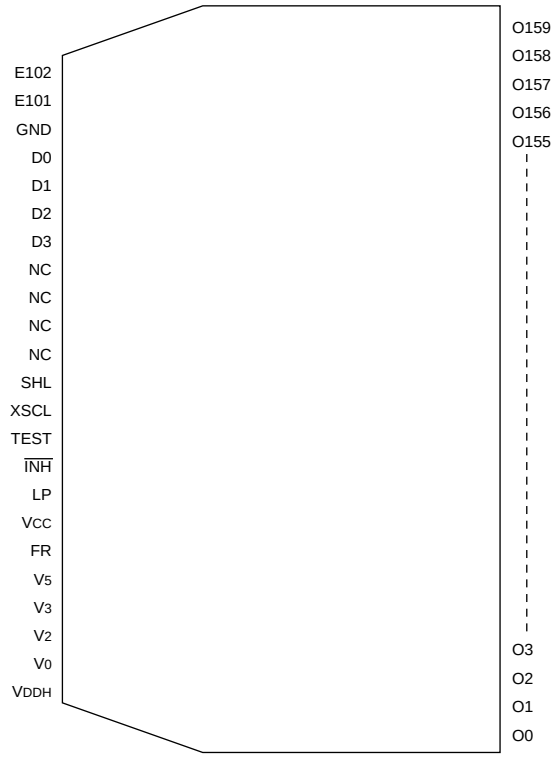
PAD No.	PAD Name	X	Y
1	O145	–3228	–2064
2	O146	–3120	↓
3	O147	–3012	
4	O148	–2903	
5	O149	–2795	
6	O150	–2687	
7	O151	–2578	
8	O152	–2470	
9	O153	–2362	
10	O154	–2253	
11	O155	–2145	
12	O156	–2037	
13	O157	–1929	
14	O158	–1820	
15	O159	–1712	
16	EIO2	–1550	–2058
17	EIO1	–1417	↓
18	GND	–1284	
19	D0	–1151	
20	D1	–1018	
21	D2	–885	
22	D3	–752	
23	NC	–619	
24	NC	–486	
25	NC	–353	
26	NC	–220	
27	SHL	–87	
28	XSCL	46	
29	TEST	179	
30	$\overline{INH}$	312	
31	LP	445	
32	V_{CC}	578	
33	FR	711	↓
34	V_5	872	–2026
35	V_3	1034	↓
36	V_2	1195	
37	V_0	1357	↓
38	V_{DDH}	1550	–2058
39	O0	1712	–2064
40	O1	1820	↓
41	O2	1929	
42	O3	2037	
43	O4	2145	
44	O5	2253	
45	O6	2362	
46	O7	2470	
47	O8	2578	
48	O9	2687	
49	O10	2795	
50	O11	2903	
51	O12	3012	
52	O13	3120	
53	O14	3228	↓
54	O15	3474	–1841
55	O16	↓	–1733
56	O17		–1625
57	O18		–1516
58	O19		–1408
59	O20		–1300
60	O21		–1191
61	O22	↓	–1083

PAD No.	PAD Name	X	Y
62	O23	3474	–975
63	O24	↓	–866
64	O25		–758
65	O26		–650
66	O27		–542
67	O28		–433
68	O29		–325
69	O30		–217
70	O31		–108
71	O32		0
72	O33		108
73	O34		217
74	O35		325
75	O36		433
76	O37		542
77	O38		650
78	O39		758
79	O40		866
80	O41		975
81	O42		1083
82	O43		1191
83	O44		1300
84	O45		1408
85	O46		1516
86	O47		1625
87	O48		1733
88	O49	↓	1841
89	O50	3195	2064
90	O51	3087	↓
91	O52	2978	
92	O53	2870	
93	O54	2762	
94	O55	2553	
95	O56	2545	
96	O57	2437	
97	O58	2328	
98	O59	2220	
99	O60	2112	
100	O61	2004	
101	O62	1895	
102	O63	1787	
103	O64	1679	
104	O65	1570	
105	O66	1462	
106	O67	1354	
107	O68	1245	
108	O69	1137	
109	O70	1029	
110	O71	921	
111	O72	812	
112	O73	704	
113	O74	596	
114	O75	487	
115	O76	379	
116	O77	271	
117	O78	162	
118	O79	54	
119	O80	–54	
120	O81	–162	
121	O82	–271	
122	O83	–379	↓

PAD No.	PAD Name	X	Y
123	O84	–487	2064
124	O85	–596	↓
125	O86	–704	
126	O87	–812	
127	O88	–921	
128	O89	–1029	
129	O90	–1137	
130	O91	–1245	
131	O92	–1354	
132	O93	–1462	
133	O94	–1570	
134	O95	–1679	
135	O96	–1787	
136	O97	–1895	
137	O98	–2004	
138	O99	–2112	
139	O100	–2220	
140	O101	–2328	
141	O102	–2437	
142	O103	–2545	
143	O104	–2653	
144	O105	–2762	
145	O106	–2870	
146	O107	–2978	
147	O108	–3087	
148	O109	–3195	↓
149	O110	–3474	1841
150	O111	↓	1733
151	O112		1625
152	O113		1516
153	O114		1408
154	O115		1300
155	O116		1191
156	O117		1083
157	O118		975
158	O119		866
159	O120		758
160	O121		650
161	O122		542
162	O123		433
163	O124		325
164	O125		217
165	O126		108
166	O127		0
167	O128		–108
168	O129		–217
169	O130		–325
170	O131		–433
171	O132		–542
172	O133		–650
173	O134		–758
174	O135		–866
175	O136		–975
176	O137		–1083
177	O138		–1191
178	O139		–1300
179	O140		–1408
180	O141		–1516
181	O142		–1625
182	O143		–1733
183	O144	↓	–1841

7-2 Tape-carrier Package

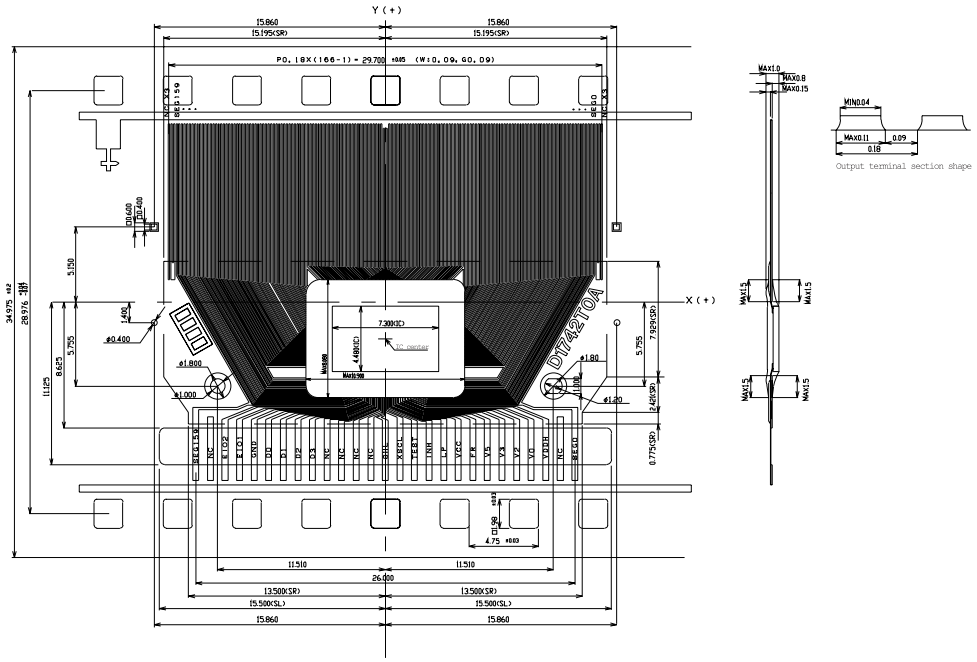
Tape-carrier pinout



Dimensional outline drawing

For reference

Unit: mm



8. FUNCTIONAL DESCRIPTION

8-1 Enable Shift Register

The enable shift register is a bidirectional shift register, where the shift direction is selected by SHL. SHL is also used to latch data from the data bus into the data register. The effect of SHL on the shift direction and on the input data sequence is shown in table 2.

Table 2. Data sequence and shift direction

SHL	LCD outputs							Shift direction	
	O159	O158	O157	…	O2	O1	O0	EIO1	EIO2
L	a	b	c	…	x	y	z	Output	Input
H	z	y	x	…	c	b	a	Input	Output

When the enable signal is inactive, the SED1742 is in standby mode with the internal clock stopped and the data bus held LOW. When multiple SED1742s are used, the enable input of the first device should be connected to ground and the enable input of each successive device should be connected to the enable output of the preceeding device.

When 160 data bits have been latched into the SED1742, the enable output goes LOW, eliminating the need for an external control circuit.

8-2 Data Register

The data register converts the input data into parallel display driver data under the control of the enable shift register.

8-3 Data Latch

The data latch latches the data into the level shifter on the falling edge of LP.

8-4 Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

8-5 LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in table 3.

Table 3. Driver output voltage

$\overline{INH}$	Input data	FR	Output voltage
H	H	H	V_0 (V_{DDH})
		L	V_5
	L	H	V_2
		L	V_3
L	×	×	V_5

× = don't care

9. APPLICATION NOTES

9-1 Voltage Levels

The recommended method of generating the LCD drive voltages, V_0 to V_5, is with a voltage divider between V_{DDH} and V_{GND}, buffered with voltage followers.

The lower drive level, V_5, is not necessarily at V_{GND}, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V_5 and V_{GND} of 2.5 V is recommended since the driver efficiency decreases as the differential increases. Connect V_5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints as shown in the Typical Application circuit.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V_0) ≥ V_2 ≥ V_3 ≥ V_5 ≥ V_{GND} breaks down. A stabilized power supply may be required when using the resistor network.

9-2 Power-up and Power-down Precautions

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1742 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9 V, excess current will flow into the SED1742 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

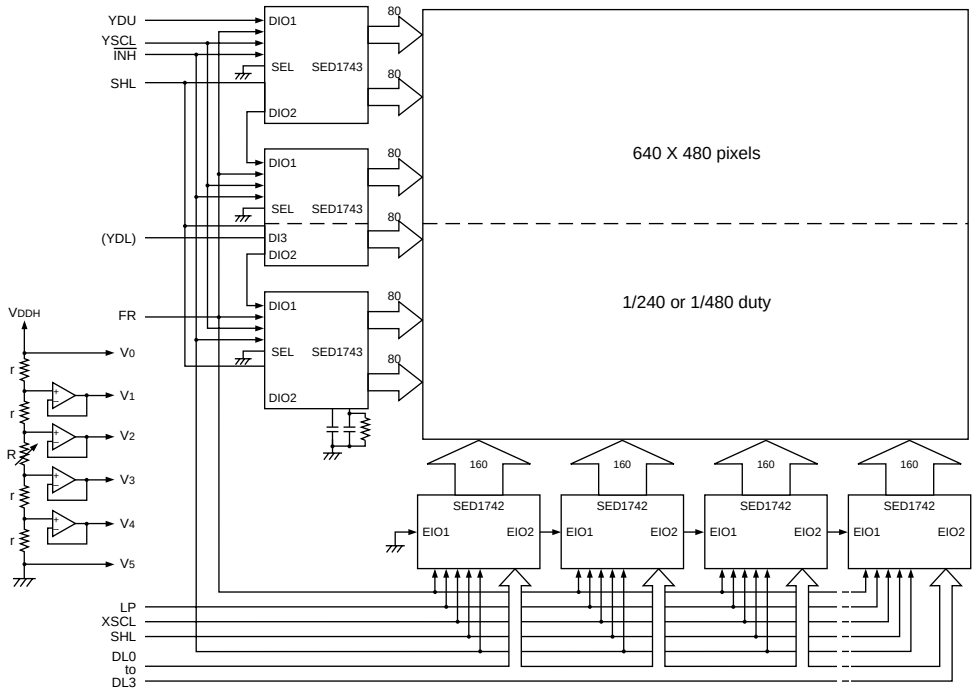
Power-up sequence: Power should be applied to V_{CC} before, or at the same time as, power is applied to the driver circuitry.

Power-down sequence: Power should be removed from V_{CC} after, or at the same time as, power is removed from the driver circuitry.

The SED1742 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. $\overline{INH}$ should be held LOW to hold the driver outputs at V_5 until the driver supplies have stabilized.

As an extra precaution, insert a fast-blow fuse in series with the driver supply.

10. TYPICAL APPLICATION



3. SED1743
LCD Driver

Contents

1. OVERVIEW

The SED1743 is an LCD common driver for high-resolution dot-matrix panels, which incorporates 160 row driver outputs. It is designed for use in conjunction with the SED1742 and SED1744 column drivers.

The SED1743 features a wide range of LCD drive voltages. The upper and lower drive voltages, V_0 and V_5, are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. As a result, the SED1743 is compatible with a large range of LCD panels.

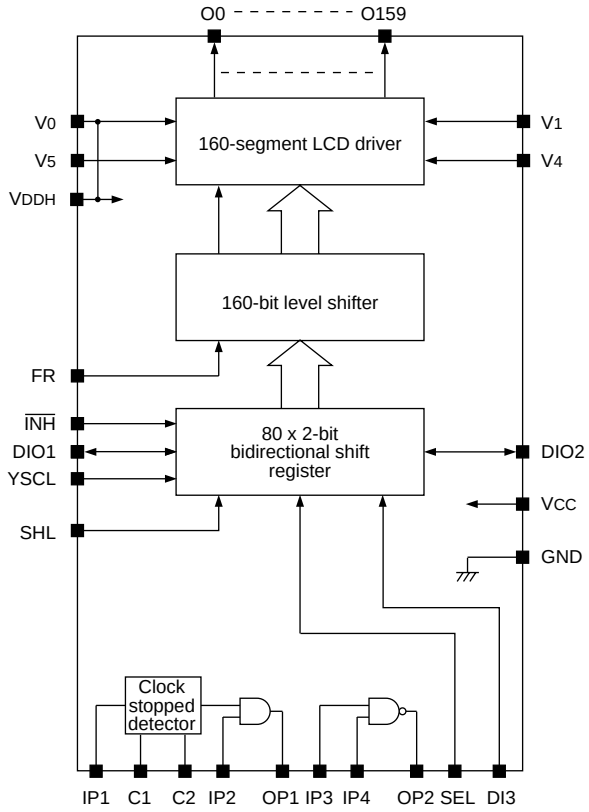
The SED1743 uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1743 operates from a 2.7 to 5.5 V supply and is available in both chip packages and tape-carrier packages (TCPs).

2. FEATURES

- 160 (80 × 2) LCD common drive outputs
- Pin-selectable output shift direction
- Adjustable LCD drive voltages
- Duty cycles up to 1/480
- Zero-bias display disable function
- Silicon-gate CMOS technology
- 1 kΩ typical output impedance
- 14 to 40 V LCD drive voltages
- 2.7 to 5.5 V supply
- Chip (SED1743D$_{1B}$) or tape-carrier packages (SED1743T$_{0A}$)

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

Number	Name	Description
39 to 183, 1 to 15	O0 to O159	LCD common drive outputs
16, 17	DIO2, DIO1	Serial data input/outputs
18	GND	Ground
19	SEL	Shift register mode select input
20	OP1	Clock monitor output
21	C1	First charge hold input. A capacitor should be connected between this pin and ground.
22	IP1	Halt detector clock input
23	C2	Second charge hold input. A resistor and capacitor should be connected between this pin and ground.
24	IP2	IP2 is connected to one input of an internal AND gate. The other input is connected to the halt detector output. Internal pulldown resistor
25	DI3	Scan pulse input when in 2×80 mode.
26	IP3	NAND gate input. Internal pulldown resistor
27	SHL	Shift direction select input
28	YSCL	Serial data shift clock. Negative-edge triggered.
29	IP4	NAND gate input
30	$\overline{\text{INH}}$	Display blanking input
31	OP2	NAND gate output
32	V_{CC}	Logic supply
33	FR	Common drive signal polarity select input
34 to 38	V_5, V_4, V_1, V_0 and V_{DDH}	Segment drive voltage inputs

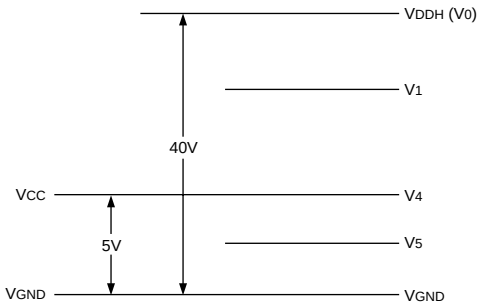
5. SPECIFICATIONS

5-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.3 to 7.0	V
	V_{DDH} (V_0)	–0.3 to 45.0	V
	V_1, V_4 and V_5	V_{GND} – 0.3 to V_{DDH} + 0.3	V
Input voltage range	V_I	V_{GND} – 0.3 to V_{CC} + 0.3	V
Output voltage range	V_O	V_{GND} – 0.3 to V_{CC} + 0.3	V
DIO output current	I_O	20	mA
Operating temperature range	Topg	–20 to 75	deg. C
Storage temperature range	Tstg	–65 to 150 (SED1743D$_{1B}$)	deg. C
		–55 to 100 (SED1743T$_{0A}$)	

Notes

1. Care should be taken during the power-on and power-off sequence. See Application Notes.
2. Display drive voltages should always be such that V_{DDH} (V_0) ≥ V_1 ≥ V_4 ≥ V_5 ≥ V_{GND} as shown in the following figure.



5-2 Recommended Operating Conditions

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	5	V
Segment driver supply voltage range	V_{DDH}	14 to 40	V

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	2.7	V
Segment driver supply voltage range	V_{DDH}	14 to 28	V

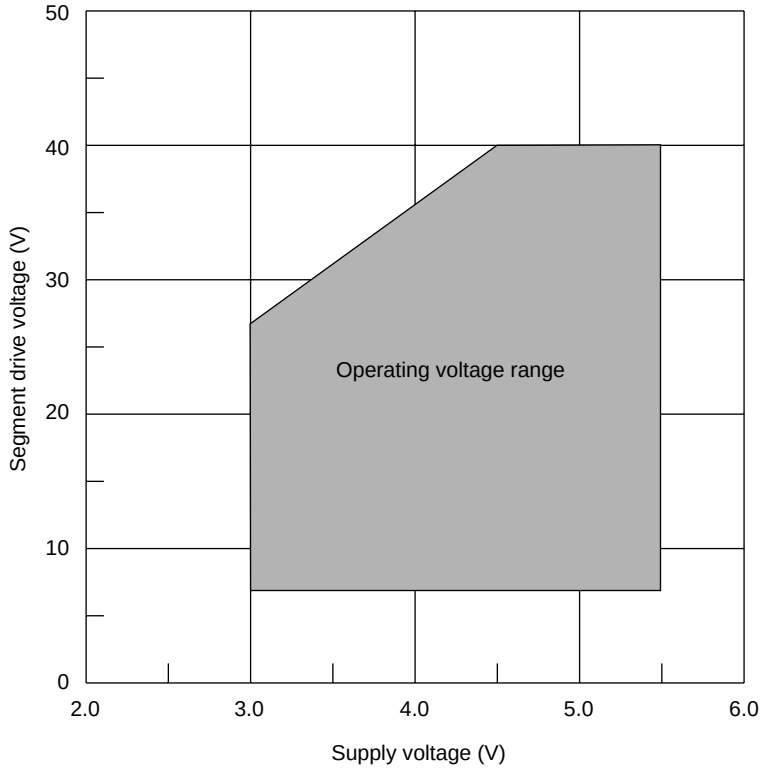
5-3 DC Electrical Characteristics

V_{CC} = 5 V ±10%, V_5 = 0 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
Quiescent current	I_{GND}	V_{DDH} = 14 to 40 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}		—	—	25	µA
Operating current	I_{CC}	V_{CC} = 5 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}, f_{YSCL} = 33.6 kHz, frame frequency = 70 Hz, no load		—	9	20	µA
		V_{CC} = 2.7 V, other conditions as above		—	6	10	µA
	I_{DDH}	V_{CC} = 5 V, V_{DDH} = V_0 = 30 V, V_1 = 28 V, V_4 = 2 V, V_5 = 0 V, other conditions as for I_{CC}		—	18	40	µA
Segment driver input voltage	V_1			8/9V_{DDH}	—	V_{DDH}	V
	V_4, V_5			V_{GND}	—	1/9V_{DDH}	V
LOW-level input voltage	V_{IL}	V_{CC} = 2.7 to 5.5 V		—	—	0.2V_{CC}	V
HIGH-level input voltage	V_{IH}			0.8V_{CC}	—	—	V
LOW-level output voltage	V_{OL}	V_{CC} = 2.7 to 5.5 V	I_{OH} = 0.3 mA	—	—	0.4	V
HIGH-level output voltage	V_{OH}		I_{OH} = –0.3 mA	V_{CC} – 0.4	—	—	V
Segment ON resistance	R_{COM}	|ΔV_{ON}| = 0.5 V	V_{DDH} = 30 V	—	1.0	2.3	kΩ
			V_{DDH} = 20 V	—	1.2	2.8	
LOW-level input leakage current	I_{LI}	V_{GND} ≤ V_I ≤ V_{CC}		—	—	2	µA
HIGH-level input leakage current	I_{HI}	V_I ≤ V_{CC}		40	80	180	µA
Input/output leakage current	$I_{LI/O}$	V_{GND} ≤ V_{IN} ≤ V_{CC}		—	—	5	µA
Input capacitance	C_I	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	8	pF
Input/output capacitance	$C_{I/O}$	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	15	pF

Operating voltage range

The maximum LCD supply voltage, V_{DDH}, depends on V_{CC}, as shown in the following figure.



5-4 AC Electrical Characteristics

Input timing

V_{CC} = 5 V ±10%, Ta = –20 to 75 deg. C

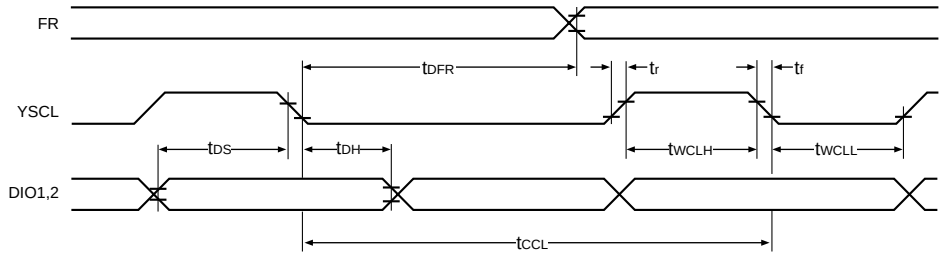
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL period	t_{CCL}		400	—	ns
YSCL HIGH-level pulsewidth	t_{WCLH}		70	—	ns
YSCL LOW-level pulsewidth	t_{WCHL}		330	—	ns
Data setup time	t_{DS}		100	—	ns

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
Data hold time	t_{DH}		40	—	ns
FR delay time	t_{DFR}		–300	300	ns
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_f		—	50	ns

V_{CC} = 2.7 to 4.5 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL period	t_{CCL}		800	—	ns
YSCL HIGH-level pulsewidth	t_{WCLH}		140	—	ns
YSCL LOW-level pulsewidth	t_{WCHL}		660	—	ns
Data setup time	t_{DS}		200	—	ns
Data hold time	t_{DH}		80	—	ns
FR delay time	t_{DFR}		–600	600	ns
Input signal rise time	t_r		—	100	ns
Input signal fall time	t_f		—	100	ns

Input timing waveform



Output timing

V_{CC} = 5 V ±10%, V_{DDH} = 14 to 40 V

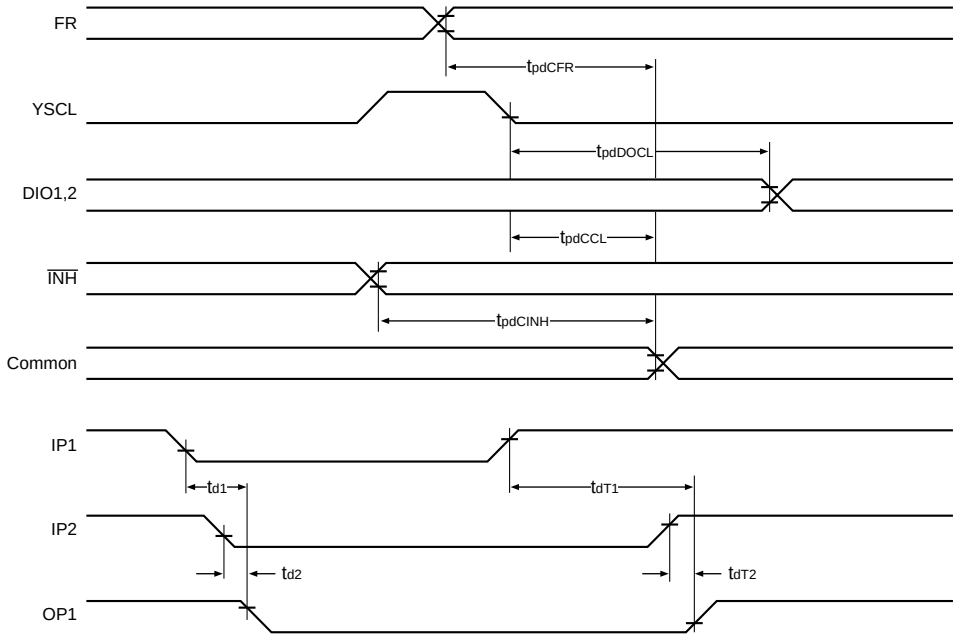
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL to DIO delay time	t_{pdDOCL}	C_L = 15 pF	—	300	ns
YSCL to common output delay time	t_{pdCCL}	C_L = 100 pF	—	700	ns
INH common output delay time	t_{pdCINH}		—	700	ns
FR to common output delay time	t_{pdCFR}		—	700	ns
IP1 to OP1 delay time	t_{d1}	C_L = 15 pF	—	4C2R2	ns
IP1 to OP1 release time	t_{dT1}		—	$2t_{YD}$	ns
IP2 to OP1 delay time	t_{d2}		—	100	ns
IP2 to OP1 release time	t_{dT2}		—	100	ns

V_{CC} = 3.0 to 4.5 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL to DIO delay time	t_{pdDOCL}	C_L = 15 pF	—	600	ns
YSCL to common output delay time	t_{pdCCL}	C_L = 100 pF	—	1400	ns
INH common output delay time	t_{pdCINH}		—	1400	ns
FR to common output delay time	t_{pdCFR}		—	1400	ns
IP1 to OP1 delay time	t_{d1}	C_L = 15 pF	—	4C2R2	ns
IP1 to OP1 release time	t_{dT1}		—	$2t_{YD}$	ns
IP2 to OP1 delay time	t_{d2}		—	200	ns
IP2 to OP1 release time	t_{dT2}		—	200	ns

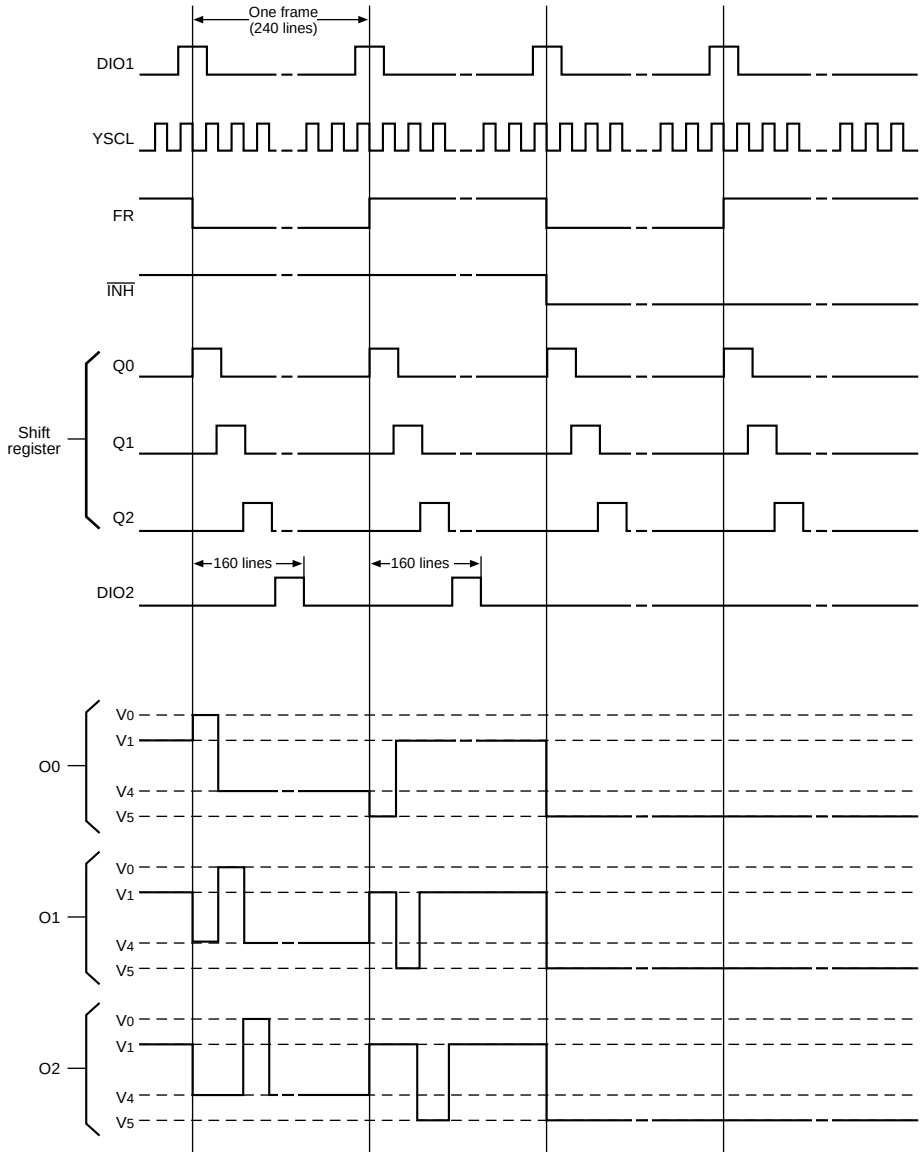
Note
YD is the scan start pulse. See the clock monitor circuit diagram for values of C2 and R2.

Output timing waveform



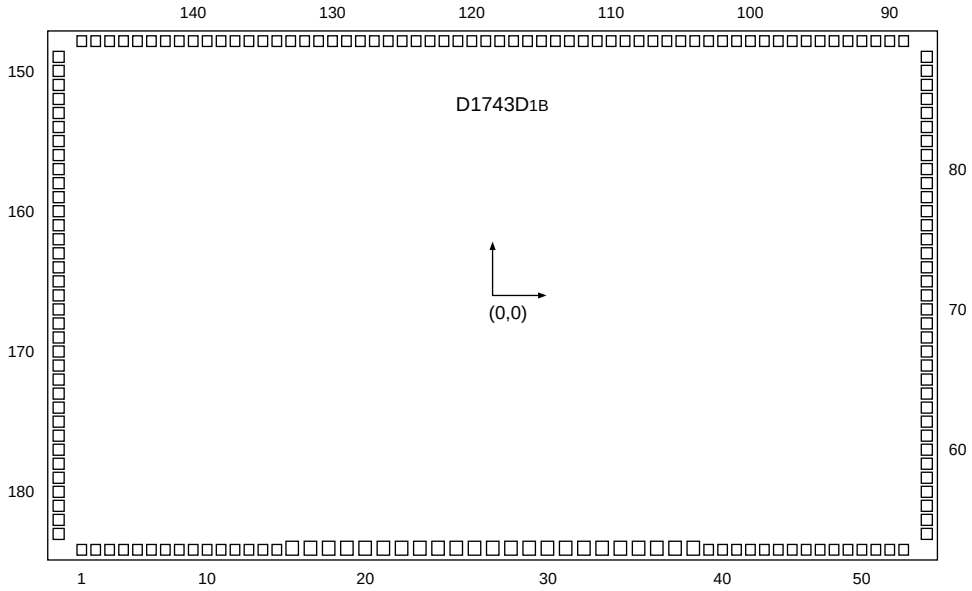
6. TIMING DIAGRAMS

1/240 Duty Cycle



7. PACKAGE DIMENSIONS

7-1 Chip Package (SED1743D1B)



- ❒ Chip size: 7.30 × 4.48 mm
- ❒ Chip thickness: 525 ±25 µm
- ❒ Pad pitch: 108 µm (Min.)
- ❒ Gold bump dimensions (SED1743D1B):
  - Size A: 94 × 134 ±20 µm (pads 1 to 15, 39 to 183)
  - Size B: 115 × 148 ±20 µm (pads 16 to 33 and 38)
  - Size C: 115 × 134 ±20 µm (pads 34 to 37)

Pad coordinates

Unit: μm

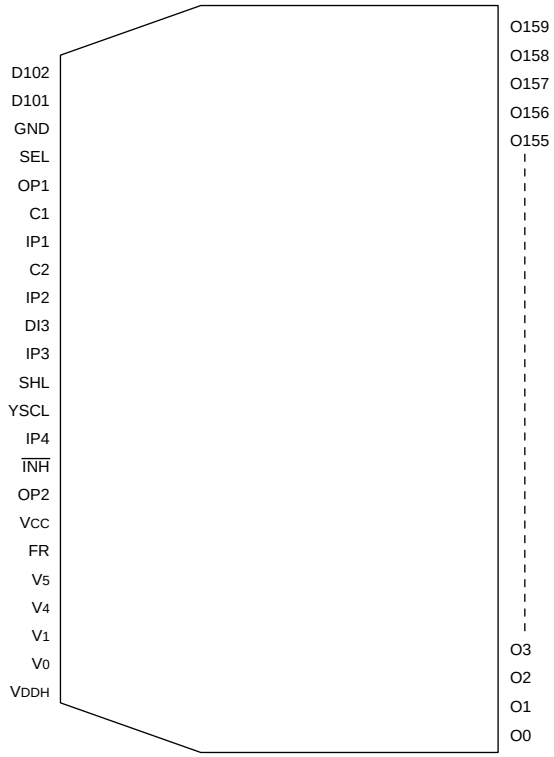
PAD No.	PAD Name	X	Y
1	O145	–3228	–2064
2	O146	–3120	↓
3	O147	–3012	
4	O148	–2903	
5	O149	–2795	
6	O150	–2687	
7	O151	–2578	
8	O152	–2470	
9	O153	–2362	
10	O154	–2253	
11	O155	–2145	
12	O156	–2037	
13	O157	–1929	
14	O158	–1820	
15	O159	–1712	
16	DIO2	–1550	–2058
17	DIO1	–1417	↓
18	GND	–1284	
19	SEL	–1151	
20	OP1	–1018	
21	C1	–885	
22	IP1	–752	
23	C2	–619	
24	IP2	–486	
25	DI3	–353	
26	IP3	–220	
27	SHL	–87	
28	YSCL	46	
29	IP4	179	
30	$\overline{\text{INH}}$	312	
31	OP2	445	
32	V_{CC}	578	
33	FR	711	
34	V_5	872	–2026
35	V_4	1034	↓
36	V_1	1195	
37	V_0	1357	
38	V_{DDH}	1550	–2058
39	O0	1712	–2064
40	O1	1820	↓
41	O2	1929	
42	O3	2037	
43	O4	2145	
44	O5	2253	
45	O6	2362	
46	O7	2470	
47	O8	2578	
48	O9	2687	
49	O10	2795	
50	O11	2903	
51	O12	3012	
52	O13	3120	
53	O14	3228	
54	O15	3474	–1841
55	O16	↓	–1733
56	O17		–1625
57	O18		–1516
58	O19		–1408
59	O20		–1300
60	O21		–1191
61	O22	↓	–1083

PAD No.	PAD Name	X	Y
62	O23	3474	–975
63	O24	↓	–866
64	O25		–758
65	O26		–650
66	O27		–542
67	O28		–433
68	O29		–325
69	O30		–217
70	O31		–108
71	O32		0
72	O33		108
73	O34		217
74	O35		325
75	O36		433
76	O37		542
77	O38		650
78	O39		758
79	O40		866
80	O41		975
81	O42		1083
82	O43		1191
83	O44		1300
84	O45		1408
85	O46		1516
86	O47		1625
87	O48		1733
88	O49	↓	1841
89	O50	3195	2064
90	O51	3087	↓
91	O52	2978	
92	O53	2870	
93	O54	2762	
94	O55	2553	
95	O56	2545	
96	O57	2437	
97	O58	2328	
98	O59	2220	
99	O60	2112	
100	O61	2004	
101	O62	1895	
102	O63	1787	
103	O64	1679	
104	O65	1570	
105	O66	1462	
106	O67	1354	
107	O68	1245	
108	O69	1137	
109	O70	1029	
110	O71	921	
111	O72	812	
112	O73	704	
113	O74	596	
114	O75	487	
115	O76	379	
116	O77	271	
117	O78	162	
118	O79	54	
119	O80	–54	
120	O81	–162	
121	O82	–271	
122	O83	–379	↓

PAD No.	PAD Name	X	Y
123	O84	–487	2064
124	O85	–596	↓
125	O86	–704	
126	O87	–812	
127	O88	–921	
128	O89	–1029	
129	O90	–1137	
130	O91	–1245	
131	O92	–1354	
132	O93	–1462	
133	O94	–1570	
134	O95	–1679	
135	O96	–1787	
136	O97	–1895	
137	O98	–2004	
138	O99	–2112	
139	O100	–2220	
140	O101	–2328	
141	O102	–2437	
142	O103	–2545	
143	O104	–2653	
144	O105	–2762	
145	O106	–2870	
146	O107	–2978	
147	O108	–3087	
148	O109	–3195	↓
149	O110	–3474	1841
150	O111	↓	1733
151	O112		1625
152	O113		1516
153	O114		1408
154	O115		1300
155	O116		1191
156	O117		1083
157	O118		975
158	O119		866
159	O120		758
160	O121		650
161	O122		542
162	O123		433
163	O124		325
164	O125		217
165	O126		108
166	O127		0
167	O128		–108
168	O129		–217
169	O130		–325
170	O131		–433
171	O132		–542
172	O133		–650
173	O134		–758
174	O135		–866
175	O136		–975
176	O137		–1083
177	O138		–1191
178	O139		–1300
179	O140		–1408
180	O141		–1516
181	O142		–1625
182	O143		–1733
183	O144	↓	–1841

7-2 Tape-carrier Package

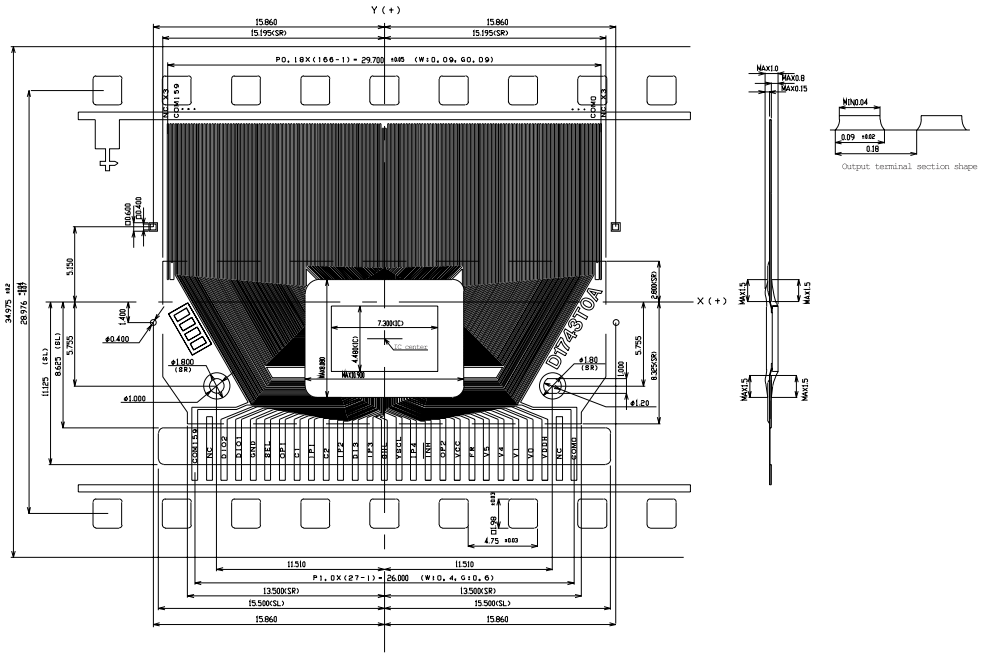
Tape-carrier pinout



Dimensional Outline Drawing

SED1743T0A

For reference



Unit: mm

8. FUNCTIONAL DESCRIPTION

8-1 Shift Register

The shift register is a bidirectional shift register, where the shift direction is selected by SHL. The effect of SHL on the shift direction and on the input data sequence is shown in table 1.

Table 1. Data sequence and shift direction

SHL	LCD outputs							Shift direction	
	O159	O158	O157	…	O2	O1	O0	DIO1	DIO2
L	a	b	c	…	x	y	z	Input	Output
H	z	y	x	…	c	b	a	Output	Input

SEL is used to select the operating mode of the shift register. When SEL is HIGH, 2×80 mode is selected. When SEL is LOW, 1×160 MODE mode is selected.

8-2 Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

8-3 LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in table 2.

Table 2. Driver output voltage

$\overline{INH}$	Input data	FR	Output voltage
H	H	H	V5
		L	V_0 (V_{DDH})
	L	H	V_1
		L	V_4
L	×	×	V_5

Note
× = don't care

8-4 Clock Monitor

The LCD panel can be damaged if a DC signal is applied to the segments. This situation can occur when the AC drive clock stops while power is applied to the display. The clock monitor circuit detects this condition and sends OP1 LOW. If OP1 is connected to $\overline{INH}$, the display is protected from damage. See Application Notes.

9. APPLICATION NOTES

9-1 Voltage Levels

The recommended method of generating the LCD drive voltages, V_0 to V_5, is with a voltage divider between V_{DDH} and V_{GND}, buffered with voltage followers.

The lower drive level, V_5, is not necessarily at V_{GND}, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V_5 and V_{GND} of 2.5 V is recommended since the driver efficiency decreases as the differential increases. Connect V_5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints as shown in the Typical Application circuit.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V_0) ≥ V_1 ≥ V_4 ≥ V_5 ≥ V_{GND} breaks down. A stabilized power supply may be required when using the resistor network.

9-2 Power-up and Power-down Precautions

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1743 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9 V, excess current will flow into the SED1743 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

Power-up sequence: Power should be applied to V_{CC} before, or at the same time as, power is applied to the driver circuitry.

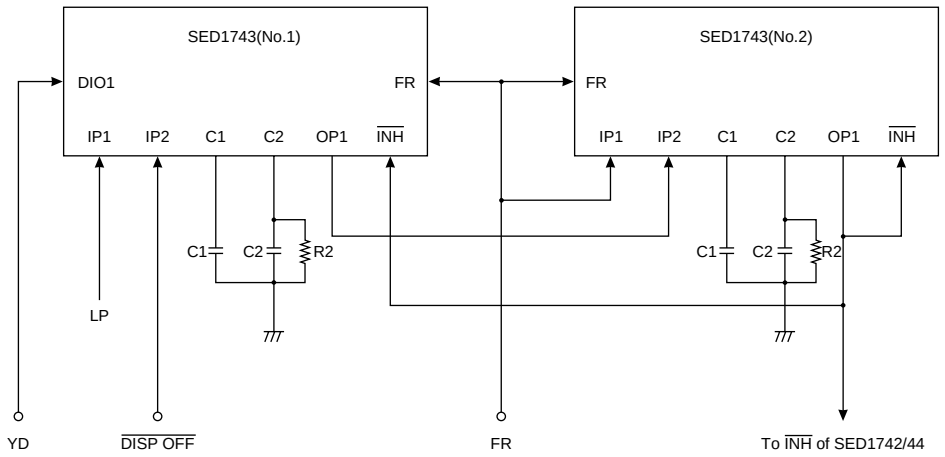
Power-down sequence: Power should be removed from V_{CC} after, or at the same time as, power is removed from the driver circuitry.

The SED1743 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. $\overline{INH}$ should be held LOW to hold the driver outputs at V_5 until the driver supplies have stabilized.

As an additional protective measure, insert a fast-blow fuse in series with the driver supply.

9-3 Clock Monitor Circuit

The clock monitor circuit sets OP1 LOW whenever the clock signals from the controller stops. Connecting OP1 to $\overline{INH}$ ensures that DC does not flow into the LCD panel.



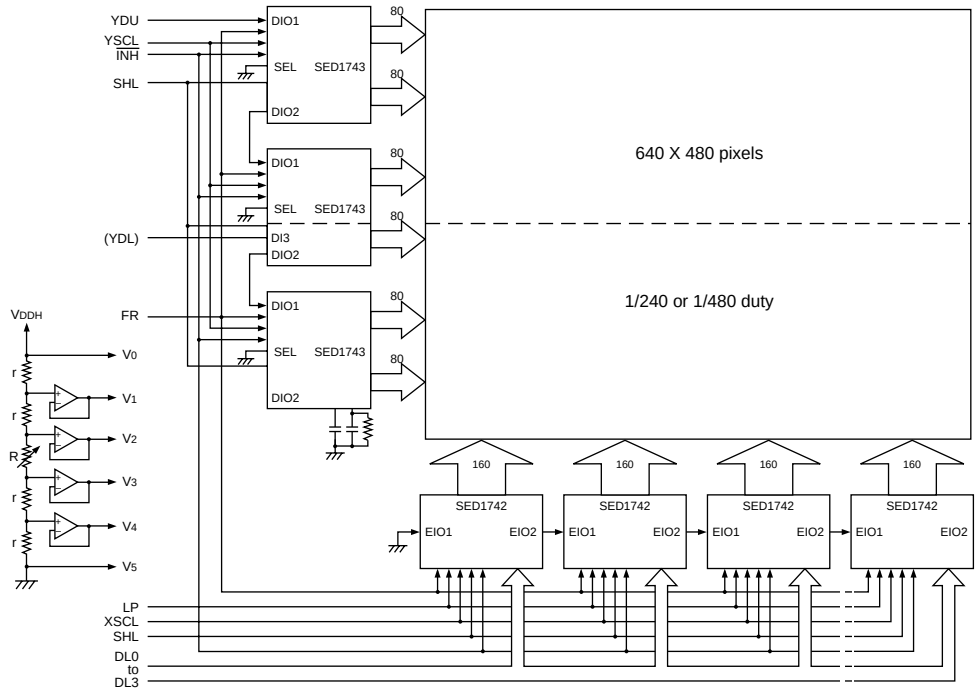
R2 is typically several MΩ and C1 and C2 are determined while monitoring OP1. C1 should be much larger than C2. Typical values under various signal conditions are shown in table 3.

Table 3. Driver output voltage

Input signal	C1	C2	R2
LP	0.47 µF	0.047 µF	3.3 MΩ
FR	0.47 µF	0.047 µF	3.3 MΩ

Notes
YD: tc = 17.8 ms, duty = 0.14 %
LP: tc = 40.4 ms, duty = 0.35 %
FR: tc = 3.53 ms, duty = 50 %
When the clock monitor feature is not required, tie IP1, IP2, IP3 and C2 LOW, and leave OP1, OP2 and C1 OPEN.

10. TYPICAL APPLICATION



4. SED1744
LCD Driver

Contents

1. OVERVIEW

The SED1744 is an LCD segment driver for high-resolution dot-matrix panels, which incorporates 160 column driver outputs. It is designed for use in conjunction with the SED1743 row driver.

The SED1744 features a wide range of LCD drive voltages. The upper and lower drive voltages, V_0 and V_5, are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. As a result, the SED1744 is compatible with a large range of LCD panels.

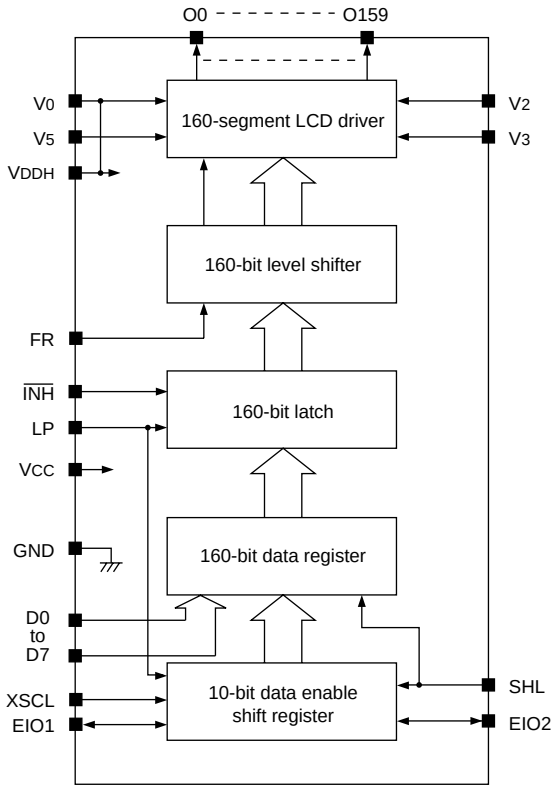
The SED1744 uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1744 operates from a 2.7 to 5.5 V supply and is available in both chip packages and tape-carrier packages (TCPs).

2. FEATURES

- 160 LCD segment drive outputs
- 8-bit data
- Daisy-chained input/output enables
- Low-power, high-speed data transfer—12 MHz clock frequency at V_{CC} = 5 V ± 10% and 8 MHz clock frequency at V_{CC} = 2.7 V
- Adjustable LCD drive voltages
- Duty cycles up to 1/480
- Zero-bias display disable function
- Silicon-gate CMOS technology
- 2.7 to 5.5 V supply
- Chip (SED1744D$_{1B}$) or tape-carrier packages (SED1744T$_{0A}$)

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

Number	Name	Description
39 to 183, 1 to 15	O0 to O159	LCD segment drive outputs
16, 17	EIO2, EIO1	I/O enable lines
18	GND	Ground
19 to 26	D0 to D7	Display data inputs
27	SHL	Shift direction select input
28	XSCL	Display data shift clock input. Negative-edge triggered
29	TEST	Test Input Tie LOW for normal operation.
30	$\overline{INH}$	Display blanking input. The SED1744 cannot be used with the SED1703 when $\overline{INH}$ is used.
31	LP	Display data latch strobe. Negative-edge triggered.
32	V_{CC}	Logic supply
33	FR	Segment drive signal polarity select input
34 to 38	V_5, V_3, V_2, V_0 and V_{DDH}	Segment drive voltage inputs

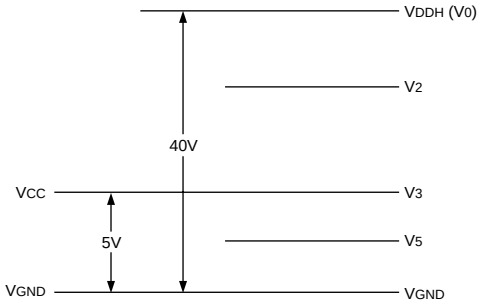
5. SPECIFICATIONS

5-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.3 to 7.0	V
	V_{DDH} (V_0)	–0.3 to 45.0	V
	V_2, V_3 and V_5	V_{GND} – 0.3 to V_{DDH} + 0.3	V
Input voltage range	V_I	V_{GND} – 0.3 to V_{CC} + 0.3	V
Output voltage range	V_O	V_{GND} – 0.3 to V_{CC} + 0.3	V
EIO output current	I_O	20	mA
Operating temperature range	Topg	–20 to 75	deg. C
Storage temperature range	Tstg	–65 to 150 ($SED1744D_{1B}$)	deg. C
		–55 to 100 ($SED1744T_{0A}$)	

Notes

1. Care should be taken during the power-on and power-off sequence. See Application Notes.
2. Display drive voltages should always be such that V_{DDH} (V_0) ≥ V_2 ≥ V_3 ≥ V_5 ≥ V_{GND} in the following figure.



5-2 Recommended Operating Conditions

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	5	V
Segment driver supply voltage range	V_{DDH}	14 to 40	V

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	2.7	V
Segment driver supply voltage range	V_{DDH}	14 to 28	V

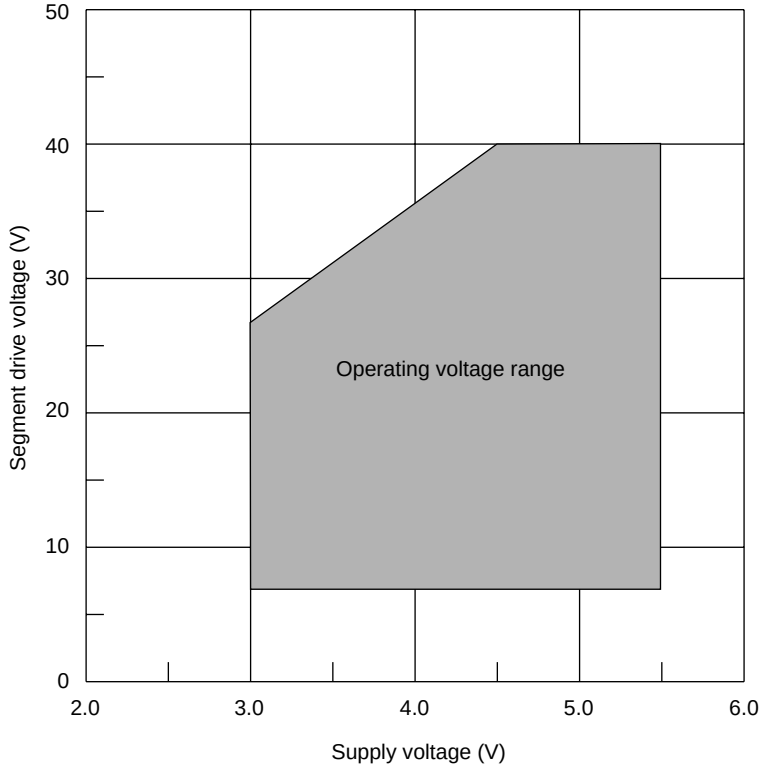
5-3 DC Electrical Characteristics

V_{CC} = 5 V ±10%, V_5 = 0 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
Segment driver supply voltage	V_{DDH}			8	—	—	V
Quiescent current	I_{GND}	V_{DDH} = 14 to 40 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}		—	—	25	µA
Operating current	I_{CC}	V_{CC} = 5 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}, f_{XSCL} = 5.38 MHz, f_{LP} = 33.6 kHz, frame frequency = 70 Hz, 1 bit alternating, Shimatsu display, no load		—	0.4	1.2	mA
		V_{CC} = 2.7 V, other conditions as above		—	0.2	0.6	mA
	I_{DDH}	V_{DDH} = V_0 = 30 V, V_{CC} = 5 V, V_3 = 4 V, V_2 = 26 V, other conditions as for I_{CC}		—	0.5	1.5	mA
Segment driver input voltage	V_2			7/9V_{DDH}	—	—	V
	V_3, V_5			V_{GND}	—	2/9V_{DDH}	V
LOW-level input voltage	V_{IL}	V_{CC} = 2.7 to 5.5 V		—	—	0.2V_{CC}	V
HIGH-level input voltage	V_{IH}			0.8V_{CC}	—	—	V
LOW-level output voltage	V_{OL}	V_{CC} = 2.7 to 5.5 V	I_{OH} = 0.6 mA	—	—	0.4	V
HIGH-level output voltage	V_{OH}		I_{OH} = –0.6 mA	V_{CC} – 0.4	—	—	V
Segment ON resistance	R_{SEG}	|ΔV_{ON}| = 0.5 V	V_{DDH} = 30 V	—	0.9	2.5	kΩ
			V_{DDH} = 20 V	—	1	3	
Input leakage current	I_{LI}	V_{GND} ≤ V_I ≤ V_{CC}		—	—	2	µA
Input/output leakage current	$I_{LI/O}$	V_{GND} ≤ V_I ≤ V_{CC}		—	—	5	µA
Input capacitance	C_I	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	8	pF
Input/output capacitance	$C_{I/O}$	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	15	pF

Operating voltage range

The maximum LCD supply voltage, V_{DDH}, depends on V_{CC}, as shown in the following figure.



5.4 AC Electrical Characteristics

Input timing

V_{CC} = 5 V ±10%, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
XSCL period	t_C		83	—	ns
XSCL HIGH-level pulsewidth	t_{WCH}		30	—	ns
XSCL LOW-level pulsewidth	t_{WCL}		30	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		20	—	ns

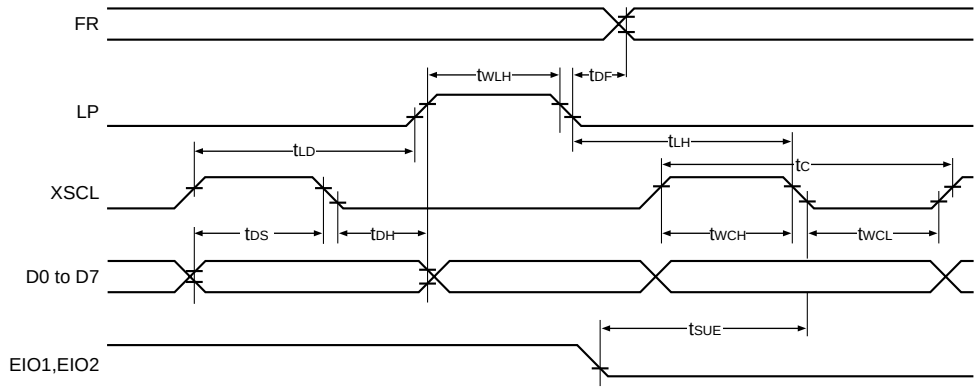
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
XSCL to LP rising edge	t_{LP}		–5	—	ns
LP to XSCL falling edge	t_{LH}		60	—	ns
LP HIGH-level pulsewidth	t_{WLH}	See note.	45	—	ns
FR delay time	t_{DF}		–300	300	ns
EIO setup time	t_{SUE}		35	—	ns

V_{CC} = 2.7 to 4.5 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
XSCL period	t_C		125	—	ns
XSCL HIGH-level pulsewidth	t_{WCH}		50	—	ns
XSCL LOW-level pulsewidth	t_{WCL}		50	—	ns
Data setup time	t_{DS}		50	—	ns
Data hold time	t_{DH}		30	—	ns
XSCL to LP rising edge	t_{LP}		0	—	ns
LP to XSCL falling edge	t_{LH}		120	—	ns
LP HIGH-level pulsewidth	t_{WLH}	See note.	90	—	ns
FR delay time	t_{DF}		–600	600	ns
EIO setup time	t_{SUE}		50	—	ns

Note
t_{WLH} indicates the period when XSCL is LOW and LP is HIGH.

Input timing waveform



Output timing

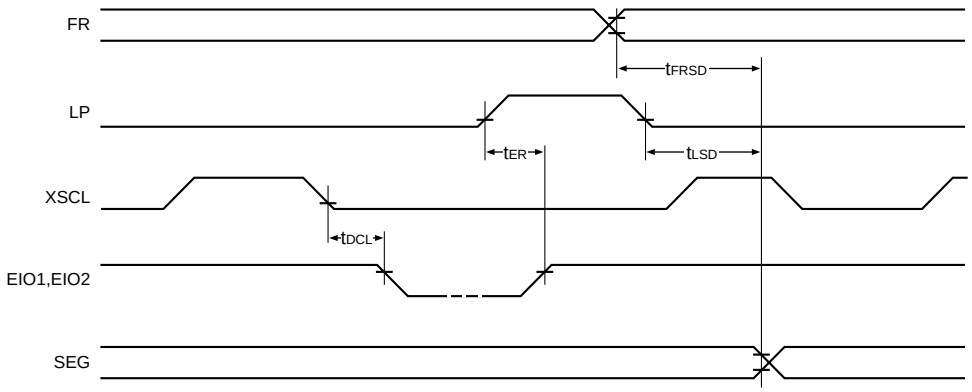
V_{CC} = 5 V ±10%, V_{DDH} = 14 to 40 V

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
EIO reset time	t_{ER}	C_L = 15 pF	—	120	ns
EIO output delay time	t_{DCL}		—	45	ns
LP to SEG delay time	t_{LSD}	C_L = 100 pF	—	200	ns
FR to SEG delay time	t_{FRSD}		—	400	ns

V_{CC} = 2.7 to 4.5 V, V_{DDH} = –14 to 28 V

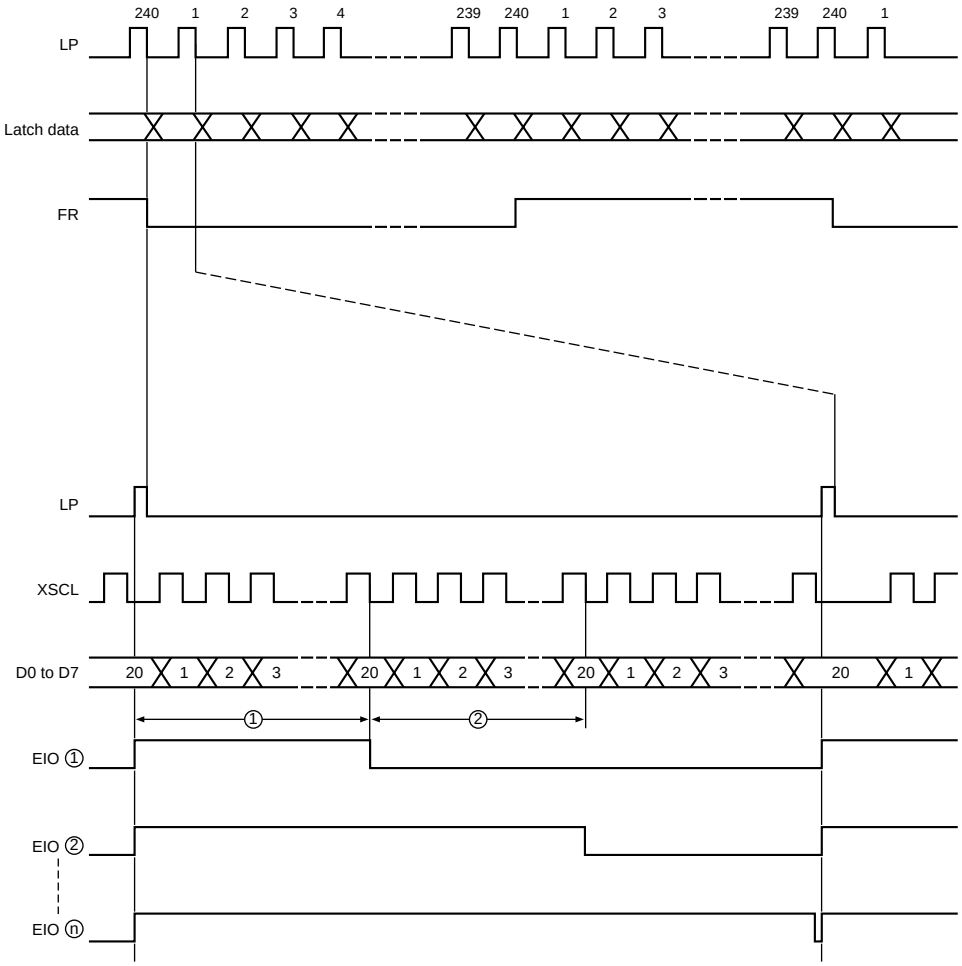
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
EIO reset time	t_{ER}	C_L = 15 pF	—	240	ns
EIO output delay time	t_{DCL}		—	72	ns
LP to SEG delay time	t_{LSD}	C_L = 100 pF	—	400	ns
FR to SEG delay time	t_{FRSD}		—	800	ns

Output timing waveform



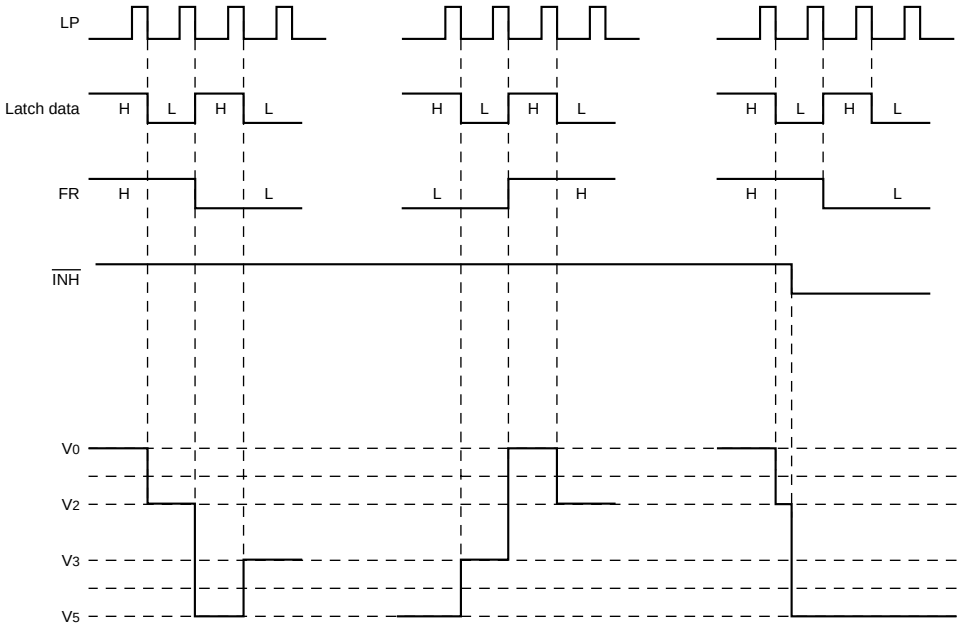
6. TIMING DIAGRAMS

1/240 Duty Cycle



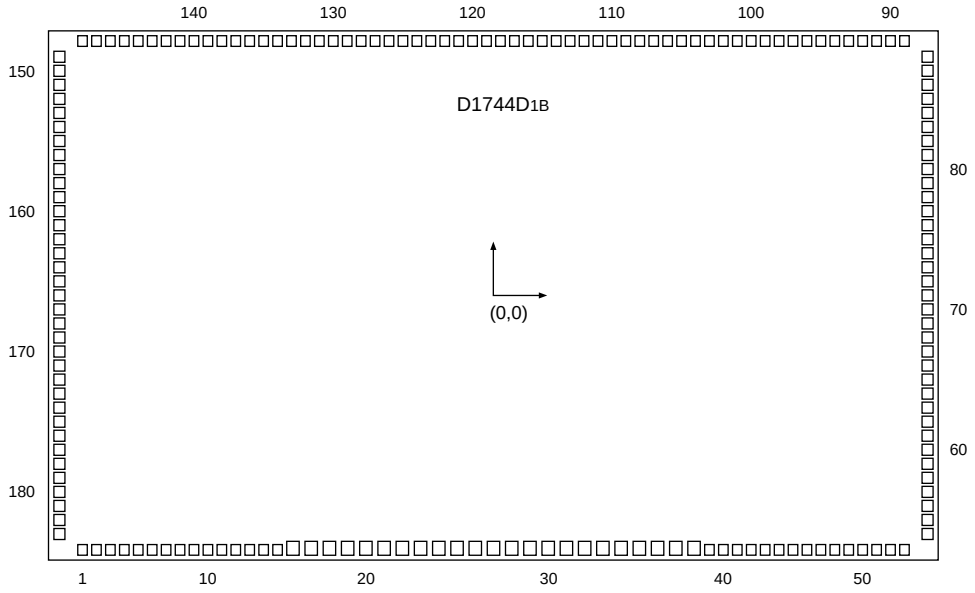
Notes

1. The circled numerals 1 to *n* denote the position of the device in the chain.
2. When transferring data at high speed, one cycle of XSCL must be lengthened to satisfy t_{LH}.


LP
Latch data
H
L
H
L
FR
H
L
INH
V0
V2
V3
V5

7. PACKAGE DIMENSIONS

7-1 Chip Package (SED1744D1B)



- ❒ Chip size: 7.30 × 4.48 mm
- ❒ Chip thickness: 525 ±25 µm
- ❒ Pad pitch: 108 µm (Min.)
- ❒ Gold bump dimensions (SED1744D1B):
  - Size A: 94 × 134 ±20 µm (pins 1 to 15, 39 to 183)
  - Size B: 115 × 148 ±20 µm (pins 16 to 33 and 38)
  - Size C: 115 × 134 ±20 µm (pins 34 to 37)

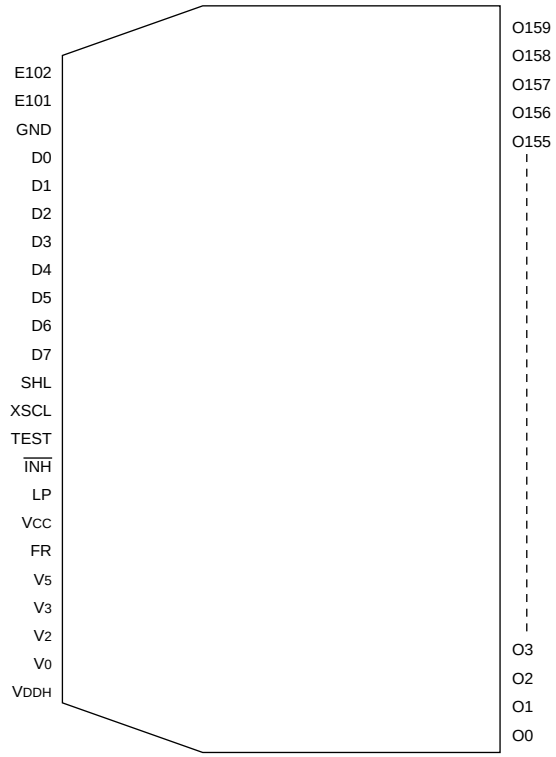
Pad coordinates

Unit: μm

PAD No.	PAD Name	X	Y
1	O145	–3228	–2064
2	O146	–3120	↓
3	O147	–3012	
4	O148	–2903	
5	O149	–2795	
6	O150	–2687	
7	O151	–2578	
8	O152	–2470	
9	O153	–2362	
10	O154	–2253	
11	O155	–2145	
12	O156	–2037	
13	O157	–1929	
14	O158	–1820	
15	O159	–1712	
16	EIO2	–1550	–2058
17	EIO1	–1417	↓
18	GND	–1284	
19	D0	–1151	
20	D1	–1018	
21	D2	–885	
22	D3	–752	
23	D4	–619	
24	D5	–486	
25	D6	–353	
26	D7	–220	
27	SHL	–87	
28	XSCL	46	
29	TEST	179	
30	$\overline{INH}$	312	
31	LP	445	
32	V_{CC}	578	
33	FR	711	↓
34	V_5	872	–2026
35	V_3	1034	↓
36	V_2	1195	
37	V_0	1357	↓
38	V_{DDH}	1550	–2058
39	O0	1712	–2064
40	O1	1820	↓
41	O2	1929	
42	O3	2037	
43	O4	2145	
44	O5	2253	
45	O6	2362	
46	O7	2470	
47	O8	2578	
48	O9	2687	
49	O10	2795	
50	O11	2903	
51	O12	3012	
52	O13	3120	
53	O14	3228	↓
54	O15	3474	–1841
55	O16	↓	–1733
56	O17		–1625
57	O18		–1516
58	O19		–1408
59	O20		–1300
60	O21		–1191
61	O22	↓	–1083
62	O23	3474	–975
63	O24	↓	–866
64	O25		–758
65	O26		–650
66	O27		–542
67	O28		–433
68	O29		–325
69	O30		–217
70	O31		–108
71	O32		0
72	O33		108
73	O34		217
74	O 35		325
75	O36		433
76	O37		542
77	O38		650
78	O39		758
79	O40		866
80	O41		975
81	O42		1083
82	O43		1191
83	O44		1300
84	O45		1408
85	O46		1516
86	O47		1625
87	O48		1733
88	O49	↓	1841
89	O50	3195	2064
90	O51	3087	↓
91	O52	2978	
92	O53	2870	
93	O54	2762	
94	O55	2553	
95	O56	2545	
96	O57	2437	
97	O58	2328	
98	O59	2220	
99	O60	2112	
100	O61	2004	
101	O62	1895	
102	O63	1787	
103	O64	1679	
104	O65	1570	
105	O66	1462	
106	O67	1354	
107	O68	1245	
108	O69	1137	
109	O70	1029	
110	O71	921	
111	O72	812	
112	O73	704	
113	O74	596	
114	O75	487	
115	O76	379	
116	O77	271	
117	O78	162	
118	O79	54	
119	O80	–54	
120	O81	–162	
121	O82	–271	↓
122	O83	–379	2064
123	O84	–487	2064
124	O85	–596	↓
125	O86	–704	
126	O87	–812	
127	O88	–921	
128	O89	–1029	
129	O90	–1137	
130	O91	–1245	
131	O92	–1354	
132	O93	–1462	
133	O94	–1570	
134	O95	–1679	
135	O96	–1787	
136	O97	–1895	
137	O98	–2004	
138	O99	–2112	
139	O100	–2220	
140	O101	–2328	
141	O102	–2437	
142	O103	–2545	
143	O104	–2653	
144	O105	–2762	
145	O106	–2870	
146	O107	–2978	
147	O108	–3087	
148	O109	–3195	↓
149	O110	–3474	1841
150	O111	↓	1733
151	O112		1625
152	O113		1516
153	O114		1408
154	O115		1300
155	O116		1191
156	O117		1083
157	O118		975
158	O119		866
159	O120		758
160	O121		650
161	O122		542
162	O123		433
163	O124		325
164	O125		217
165	O126		108
166	O127		0
167	O128		–108
168	O129		–217
169	O130		–325
170	O131		–433
171	O132		–542
172	O133		–650
173	O134		–758
174	O135		–866
175	O136		–975
176	O137		–1083
177	O138		–1191
178	O139		–1300
179	O140		–1408
180	O141		–1516
181	O142		–1625
182	O143		–1733
183	O144	↓	–1841

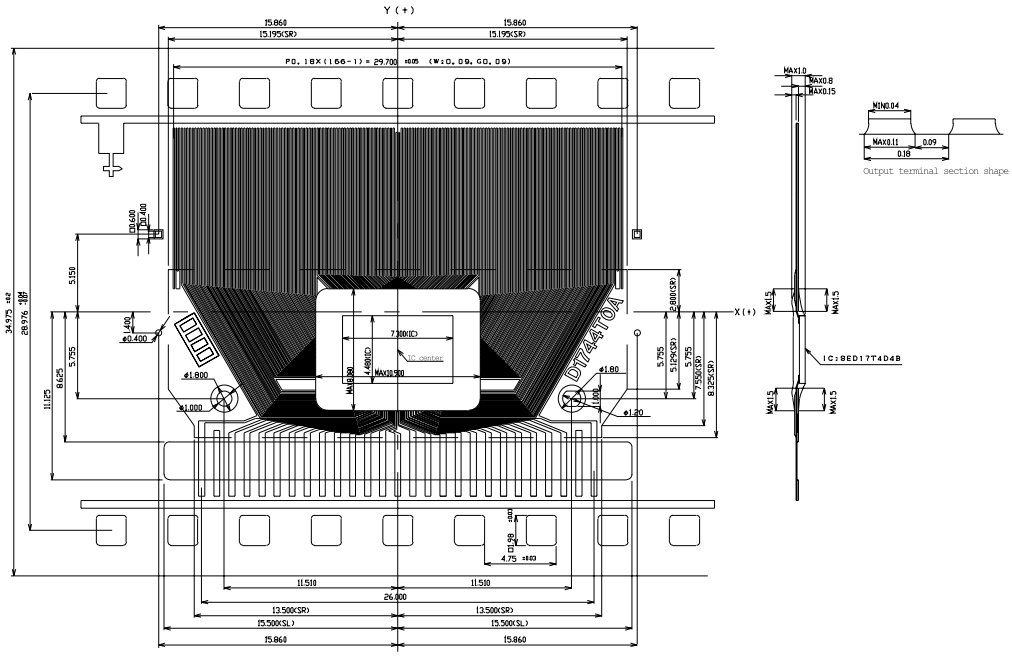
7.2 Tape-carrier Package

Tape-carrier pinout



Dimensional outline drawing

For reference



Unit: mm

8. FUNCTIONAL DESCRIPTION

8-1 Enable Shift Register

The enable shift register is a bidirectional shift register, where the shift direction is selected by SHL. SHL is also used to latch data from the data bus into the data register. The effect of SHL on the shift direction and on the input data sequence is shown in table 1.

Table 1. Data sequence and shift direction

SHL	LCD outputs							Shift direction	
	O159	O158	O157	…	O2	O1	O0	DIO1	DIO2
L	a	b	c	…	x	y	z	Output	Input
H	z	y	x	…	c	b	a	Input	Output

When the enable signal is inactive, the SED1744 is in standby mode, where the internal clock is stopped and the data bus held LOW. When multiple SED1744s are used, the enable input of the first device should be connected to ground and the enable input of each successive device should be connected to the enable output of the preceeding device.

When 160 data bits have been latched into the SED1744, the enable output goes LOW, eliminating the need for an external control circuit.

8-2 Data Register

The data register converts the input data into parallel display driver data under the control of the enable shift register.

8-3 Data Latch

The data latch latches the data into the level shifter on the falling edge of LP.

8-4 Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

8-5 LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in table 2.

Table 2. Driver output voltage

$\overline{INH}$	Input data	FR	Output voltage
H	H	H	V_0 (V_{DDH})
		L	V_5
	L	H	V_2
		L	V_3
L	×	×	V_5

Note

× = don't care

9. APPLICATION NOTES

9-1 Voltage Levels

The recommended method of generating the LCD drive voltages, V_0 to V_5, is with a voltage divider between V_{DDH} and GND, buffered with voltage followers.

The lower drive level, V_5, is not necessarily at GND, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V_5 and GND of 2.5 V is recommended since the driver efficiency decreases as the differential increases. Connect V_5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints as shown in the Typical Application circuit.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V_0) ≥ V_2 ≥ V_3 ≥ V_5 ≥ GND breaks down. A stabilized power supply may be required when using the resistor network.

9-2 Power-up and Power-down Precautions

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1744 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9 V, excess current will flow into the SED1744 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

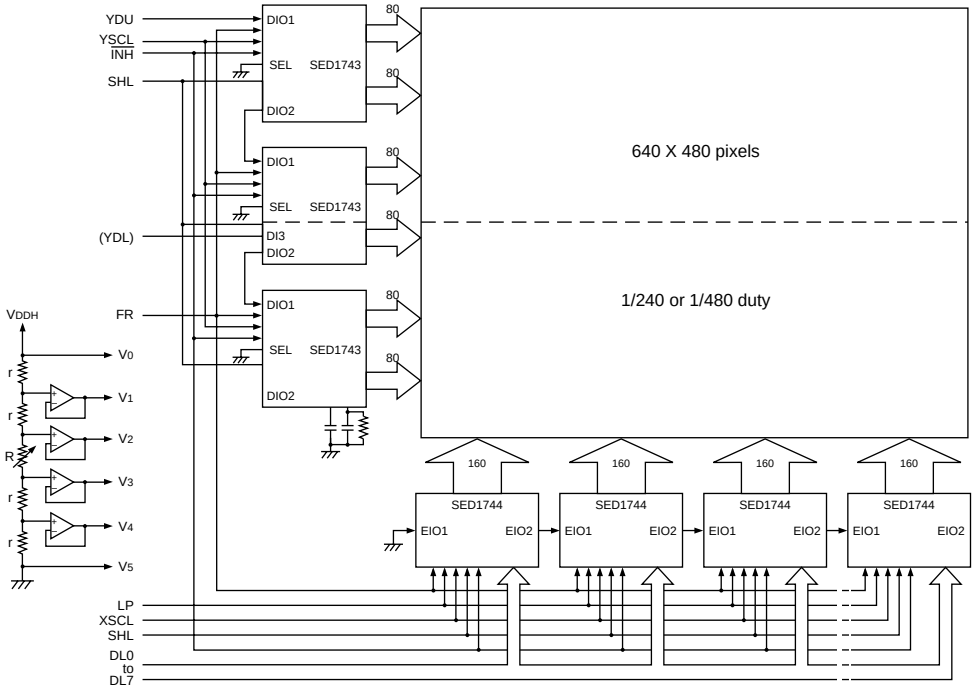
Power-up sequence: Power should be applied to V_{CC} before, or at the same time as, power is applied to the driver circuitry.

Power-down sequence: Power should be removed from V_{CC} after, or at the same time as, power is removed from the driver circuitry.

The SED1744 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. $\overline{INH}$ should be held LOW to hold the driver outputs at V_5 until the driver supplies have stabilized.

As an additional protective measure, insert a fast-blow fuse in series with the driver supply.

10. TYPICAL APPLICATION



5. SED1748
LCD Driver

Contents

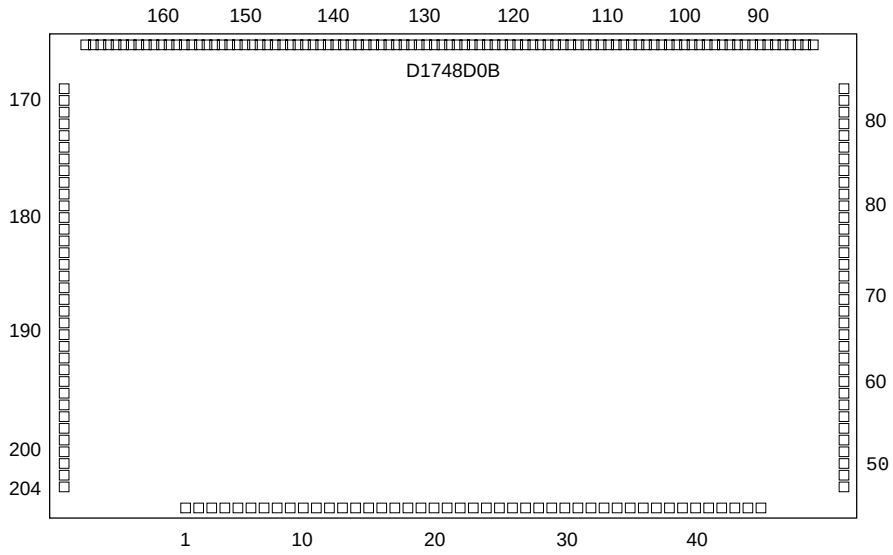
1. OVERVIEW

The SED1748 is a 160-output segment (column) driver most applicable to drive the extra large-capacity color STN dot matrix liquid crystal panel, which is used in pair with the SED1743.
It allows for potential high-resolution LCD, with the high-speed enable chain system favorable for the low power trend, and the long type chip advantageous for more portable size LCD panel. The low voltage high speed operation of the logic system allows for a wide range of application.

2. FEATURES

- LCD drive outputs : 160
- Low-voltage operation time : 2.7 V min
- High duty drive applicable : 1/500 (reference)
- Wide liquid crystal drive voltage range : +8 to +42 V (V_{CC} = 3 to 5.5 V)
- 8-bit bus enable chain system allows high-speed and low power data transmission
  Shift clock frequency 16.0 MHz (5 V ±10%)
  10.0 MHz (2.7 V)
- Long side-ways chip
- Non-bias display off function
- Offset bias of liquid crystal power supply against V_0, GND level adjustable
- Logic system power supply : 2.7 to 5.5 V
- Shipment : Chip SED1748D$_{0B}$
  TCP SED1748T **

3. PAD ARRANGEMENT



Chip size	7.30 mm × 4.48 mm
Pad pitch	81.7 μm (Min.)
Chip thickness	525 μm ± 25 μm

1) Au Bump specifications (SED 1748D0B) Referential value
   Bump size A 97 μm × 88 μm ±4 μm (Pad No. 1 to 44)
   Bump size B 82 μm × 80 μm ±4 μm (Pad No. 45 to 48, 66 to 81, 168 to 183, 201 to 204)
   Bump size C 82 μm × 70 μm ±4 μm (Pad No. 49 to 65, 184 to 200)
   Bump size D 65 μm × 164 μm ±4 μm (Pad No. 82 to 85, 164 to 167)
   Bump size E 53 μm × 164 μm ±4 μm (Pad No. 86 to 163)

4. PAD COORDINATES

Unit : μm

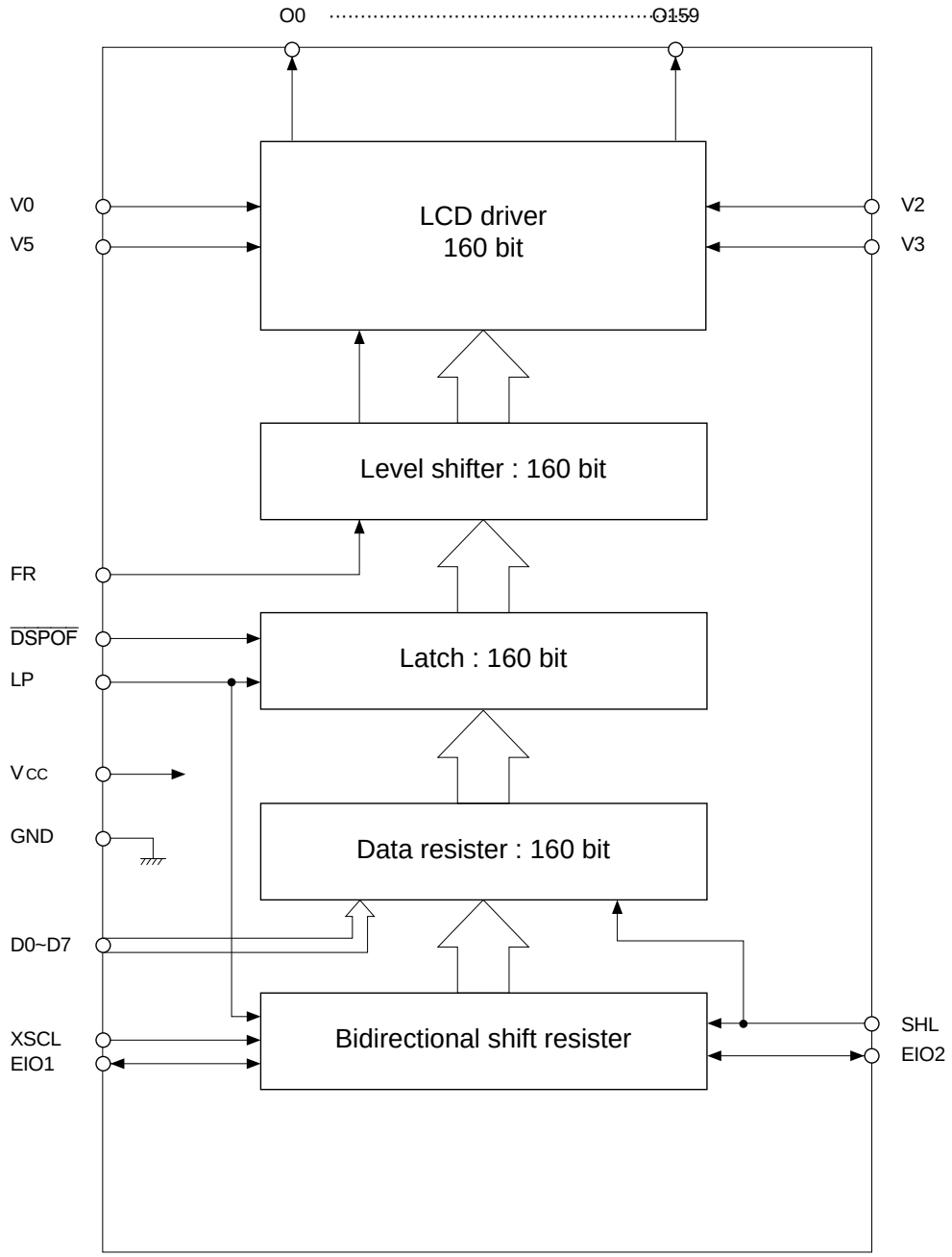
PAD NO.	PIN NAME	X	Y	PAD NO.	PIN NAME	X	Y	PAD NO.	PIN NAME	X	Y
1	GND	– 2757	– 2080	70	0 25	3492	505	139	0 94	– 1185	2051
2	↓	– 2630		71	26		616	140	95	– 1266	
3	EIO2	– 2500		72	27		726	141	96	– 1348	
4	↓	– 2373		73	28		836	142	97	– 1430	
5	FR	– 2244		74	29		946	143	98	– 1511	
6	↓	– 2117		75	30		1056	144	99	– 1593	
7	DSPOFF	– 1987		76	31		1167	145	100	– 1675	
8	↓	– 1860		77	32		1277	146	101	– 1757	
9	LP	– 1731		78	33		1387	147	102	– 1838	
10	↓	– 1604		79	34		1497	148	103	– 1920	
11	XSCL	– 1474		80	35		1607	149	104	– 2002	
12	↓	– 1347		81	36	↓	1718	150	105	– 2083	
13	D0	– 1218		82	37	3512	2051	151	106	– 2165	
14	↓	– 1091		83	38	3419		152	107	– 2247	
15	D1	– 961		84	39	3326		153	108	– 2328	
16	↓	– 834		85	40	3233		154	109	– 2410	
17	D2	– 705		86	41	3145		155	110	– 2492	
18	↓	– 578		87	42	3064		156	111	– 2574	
19	D3	– 448		88	43	2982		157	112	– 2655	
20	↓	– 321		89	44	2900		158	113	– 2737	
21	D4	– 192		90	45	2819		159	114	– 2819	
22	↓	– 65		91	46	2737		160	115	– 2900	
23	D5	65		92	47	2655		161	116	– 2982	
24	↓	192		93	48	2574		162	117	– 3064	
25	D6	321		94	49	2492		163	118	– 3145	
26	↓	448		95	50	2410		164	119	– 3233	
27	D7	578		96	51	2328		165	120	– 3326	
28	↓	705		97	52	2247		166	121	– 3419	
29	EIO1	834		98	53	2165		167	122	– 3512	↓
30	↓	961		99	54	2083		168	123	– 3492	1718
31	SHL	1091		100	55	2002		169	124		1607
32	↓	1218		101	56	1920		170	125		1497
33	NC	1347		102	57	1838		171	126		1387
34	↓	1474		103	58	1757		172	127		1277
35	V_{CC}	1604		104	59	1675		173	128		1167
36	↓	1731	↓	105	60	1593		174	129		1056
37	V5	1860	– 2055	106	61	1511		175	130		946
38	↓	1987	↓	107	62	1430		176	131		836
39	V3	2117	– 2040	108	63	1348		177	132		726
40	↓	2244	↓	109	64	1266		178	133		616
41	V2	2373	– 2024	110	65	1185		179	134		505
42	↓	2500	↓	111	66	1103		180	135		395
43	V0	2630	– 2009	112	67	1021		181	136		285
44	↓	2757	↓	113	68	940		182	137		175
45	O 0	3492	– 2088	114	69	858		183	138		65
46	1		– 1978	115	70	776		184	139		– 41
47	2		– 1868	116	71	694		185	140		– 142
48	3		– 1758	117	72	613		186	141		– 242
49	4		– 1652	118	73	531		187	142		– 343
50	5		– 1551	119	74	449		188	143		– 444
51	6		– 1451	120	75	368		189	144		– 544
52	7		– 1350	121	76	286		190	145		– 645
53	8		– 1249	122	77	204		191	146		– 746
54	9		– 1149	123	78	123		192	147		– 846
55	10		– 1048	124	79	41		193	148		– 947
56	11		– 947	125	80	– 41		194	149		– 1048
57	12		– 846	126	81	– 123		195	150		– 1149
58	13		– 746	127	82	– 204		196	151		– 1249
59	14		– 645	128	83	– 286		197	152		– 1350
60	15		– 544	129	84	– 368		198	153		– 1451
61	16		– 444	130	85	– 449		199	154		– 1551
62	17		– 343	131	86	– 531		200	155		– 1652
63	18		– 242	132	87	– 613		201	156		– 1758
64	19		– 142	133	88	– 694		202	157		– 1868
65	20		– 41	134	89	– 776		203	158		– 1978
66	21		65	135	90	– 858		204	159	↓	– 2088
67	22		175	136	91	– 940					
68	23		285	137	92	– 1021					
69	24	↓	395	138	93	– 1103	↓				

5. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Numbers of pins</th></tr>
<tr><td>O 0 ~
O 159</td><td>O</td><td>Liquid crystal drive segment (column) output
The output changes at the edge of LP fall.</td><td>160</td></tr>
<tr><td>D0 ~ D7</td><td>I</td><td>Display data input</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (Fall edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (Fall edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable input.output
Set at input or output by the SHL input level.
Output is reset by input of LP, and automatically falls to “L” as soon as 160 bits of data is collected.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection, and EIO terminal input/output control input
When data is input to the (D0, D1, ... D7) terminals in sequence of (a0, a1, ... a6, a7) (b0, b1, ... b6, b7) (t0,t1, ... t6, t7), the relation between the data and the segment is as follows.
<table>
<tr><td>S H L</td><td colspan="7">O Output</td><td colspan="2">EIO</td></tr>
<tr><td>L</td><td>159</td><td>158</td><td>157</td><td></td><td>2</td><td>1</td><td>0</td><td>EIO1</td><td>EIO2</td></tr>
<tr><td>L</td><td>a0</td><td>a1</td><td>a2</td><td>···</td><td>t5</td><td>t6</td><td>t7</td><td>output</td><td>input</td></tr>
<tr><td>H</td><td>t7</td><td>t6</td><td>t5</td><td>···</td><td>a2</td><td>a1</td><td>a0</td><td>input</td><td>output</td></tr>
</table>
(Note) The relation between the data and shift segment output is decided regardless of the number of clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Liquid crystal drive output alternating signal input.</td><td>1</td></tr>
<tr><td>VCC, GND</td><td>Power supply</td><td>Logical power supply GND : 0 V VCC : +3.3, +5 V</td><td>2</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power supply</td><td>Liquid crystal drive power supply
GND : 0 V V0 : +14 to +42V
V0 ≥ V2 ≥ 7/9 V0
2/9 V0 ≥ V3 ≥ V5 ≥ GND</td><td>4</td></tr>
<tr><td>$\overline{\text{DSPOF}}$</td><td>I</td><td>Forced bias fixed input
The output is forced to the V5 level at the “L” level.
* When using this function, it cannot be paired with the SED 1703.</td><td>1</td></tr>
</table>

Total 182
(including 1 NC)

6. BLOCK DIAGRAM



7. BLOCK FUNCTIONS

7-1 Enable Shift Register

The enable shift registerer is a bidirectional shift register which shift direction is selected by the SHL input.
The shift register output is used to store the data bus signal in the data register.
When the enable signal is disabled, the internal clock signal and data bus are fixed to “L”, and it enters the power save mode.
When using multiple segment drivers, cascade connection is to be made on the EIO terminals of the drivers and the EIO terminal of the first driver is to be connected to the “GND”. (See 11. “Connection example”.)
The enable control circuit automatically detection that collection of the 160-bit data is completed, and automatically transmits the enable signal, so there is no need of the control signal by the control LSI.

7-2 Data Register

This register is used for serial/parallel conversion of the data bus signal by the enable shift register output. Thus, the relation between the serial display data and the segment output is decided regardless of the shift clock inputs.

7-3 Latch

Collects the contents of the data register at the LP fall edge trigger, and transmits the output to the level shifter.

7-4 Level Shifter

Level interface circuit used to convert the voltage level of the signal from the logic system level to the liquid crystal drive level.

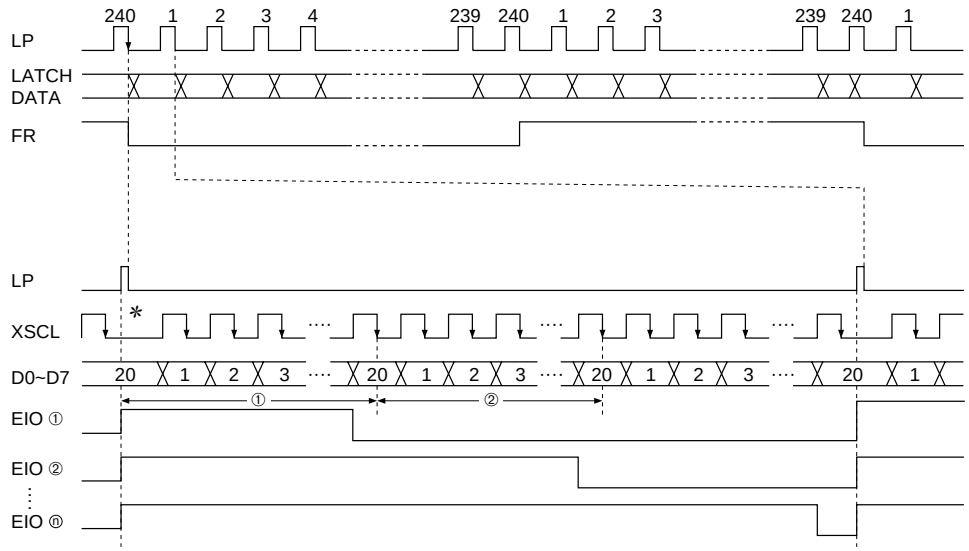
7-5 LCD Driver

Outputs liquid crystal drive voltage.
The relation between the data bus signal, alternating signal FR, and segment output voltage is as shown below.

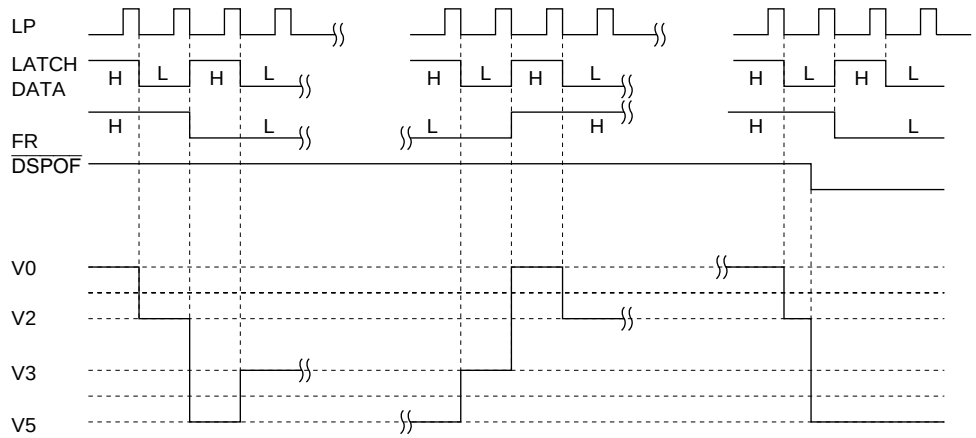
$\overline{\text{DSPOF}}$	Data bus signal	FR	Driver Output voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	–	–	V_5

7-6 Timing Diagram

Timing diagram
When it is 1/240 duty (example for reference)



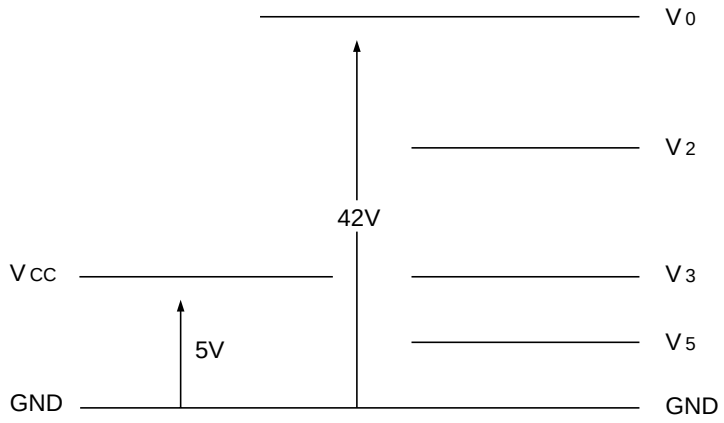
① to ⓝ are the driver's cascade numbers.
* In high-speed data transmission, the XSCL period may need to be longer in the LP pulse insertion timing, so as to secure the LP → XSCL (t_{LH}) standard.



8. ABSOLUTE MAXIMUM RATING

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 ~ +7.0	V
Supply voltage (2)	V_0	–0.3 ~ +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	GND–0.3 ~ V_0 + 0.3	V
Input voltage	V_I	GND–0.3 ~ V_{CC} + 0.3	V
Output voltage	V_O	GND–0.3 ~ V_{CC} + 0.3	V
EIO output current	I_{01}	20	mA
Working temperature	Topr	–30 ~ +85	°C
Storage temperature 1	Tstg1	–65 ~ +150	°C
Storage temperature 2	Tstg2	–55 ~ +100	°C

(Note 1) All stated voltages assume that GND = 0V.
(Note 2) Shelf temperature 1 is for individual chips, while shelf temperature 2 is for actual TAB mounted conditions.
(Note 3) V_0, V_2, V_3 voltages shall always maintain the condition of $V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



(Note 4) Avoid floating status of the logical power supply during application of liquid crystal drive power, or fall of the power below V_{CC} = 2.6 V; the LSI may be destroyed permanently.
Special notice is required for the power sequence when turning on or off the system power.

9. ELECTRIC CHARACTERISTICS

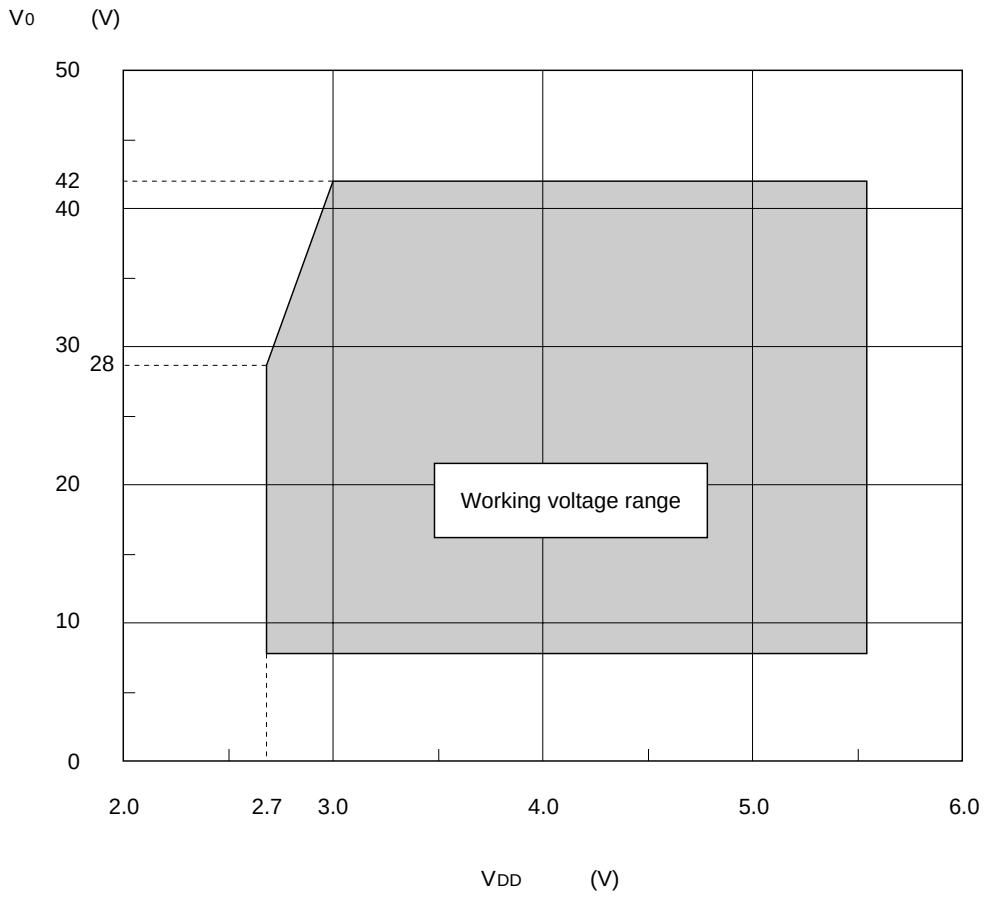
9-1 DC Characteristics

Unless otherwise specified, GND = 0V, V_{CC} = +5.0 V ±10%, Ta = –30 to 85°C

Item	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}		V_{CC}	2.7		5.5	V
Recommended working voltage	V_0		V0	14.0		40.0	V
Workable voltage	V_0	Function only	V0	8.0		42.0	V
Supply voltage (2)	V_2	Recommended value	V2	7/9V_0			V
Supply voltage (3)	V_3	Recommended value	V3	GND		2/9V_0	V
High level input voltage	V_{IH}	V_{CC} = 2.7 ~ 5.5V	EIO1,EIO2,FR D0~D7, XSCL, SHL, LP, DSPOF	0.8V_{CC}			V
Low level input voltage	V_{IL}					0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC}= 2.7~5.5V, I_{OH} = –0.6mA	EIO1, EIO2,	V_{CC}–0.4			V
Low level output voltage	V_{OL}	V_{CC}= 2.7~5.5V, I_{OL} = 0.6mA				0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0~D7, LP, FR, XSCL, SHL, DSPOF			2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	EIO1, EIO2			5.0	µA
Rest current	I_{GND}	V_0 = 14.0~42.0V, V_{IH} = V_{CC}, V_{IL}=GND	GND			25	µA
Output resistance	R_{SEG}	△V_{ON} =0.5V Recommended condition, V_0 =+36.0V, 1/24	O0~O159	0.62	1.9		KΩ
		△V_{ON} =0.5V Recommended condition, V_0 =+26.0V, 1/20			0.68	2.0	KΩ
Output resistance in-chip deviation	△R_{SEG}	△V_{ON} = 0.5V, V_0 = +36.0V, 1/24	O0~O159			90	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} = 5.38MHz, f_{LP} = 33.6KHz, f_{FR} = 70Hz, Input data: check display, no-load	V_{CC}		0.5	1.1	mA
		V_{CC} = 3.0V, Other conditions are the same as those when V_{CC} = 5V.			0.2	0.6	mA
Mean working current consumption (2)	I_0	V_0 = +30.0V, V_{CC} = +5.0V, V_3 = +4.0V, V_2 = +26.0V, V_5 = 0.0V, Other conditions are the same as those in the I_{CC} column.	V0		0.15	0.9	mA
Input terminal capacity	C_I	Freq. = 1 MHz, Ta = 25°C, Independent chips	D0~D7, LP, FR, XSCL, SHL, DSPOF			8	pF
I/O terminal capacity	$C_{I/O}$	Freq. = 1 MHz, Ta = 25°C, Independent chips	EIO1, EIO2			15	pF

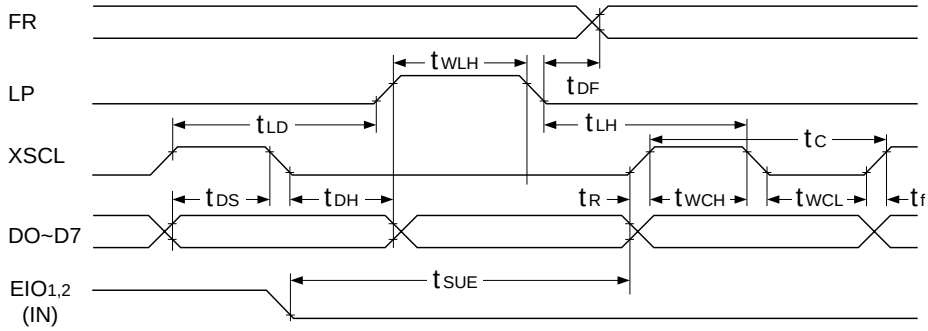
Operation voltage range V_{CC} - V_0

The V_0 voltage must be set within the following V_{CC} - V_0 operation voltage range.



9-2 AC Characteristics

Input timing characteristics



V_{CC} = +5.0V ±10%, Ta = –30 to 85°C

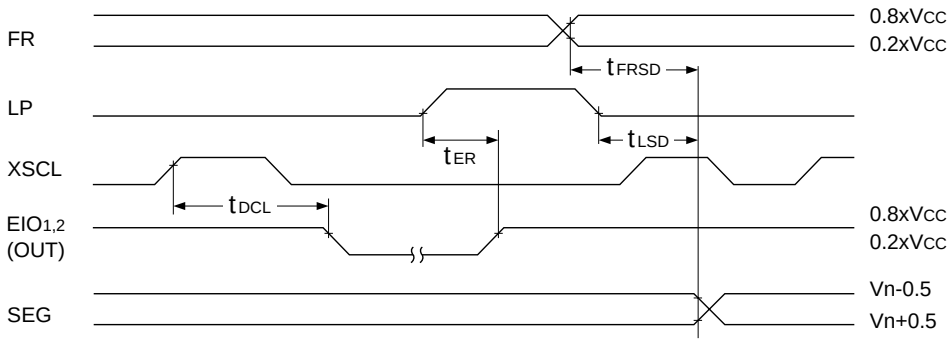
Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	t_r, $t_f \leq$ 11ns *3	62		ns
XSCL high level pulse duration	t_{WCH}		20		ns
XSCL low level pulse duration	t_{WCL}		20		ns
Data setup time	t_{DS}		10		ns
Data hold time	t_{DH}		10		ns
XSCL → LP rise time	t_{LD}		–5		ns
XSCL → LP fall time	t_{LH}		30		ns
LP high-level pulse width	t_{WLH}	*1	40		ns
		*2	35		ns
FR delay allowance	t_{DF}		–300	+300	ns
EIO set-up time	t_{SUE}		30		ns
Input signal variation time	t_r, t_f	*4		50	ns

V_{CC} = +2.7V to 4.5V, Ta = –30 to 85°C

Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	t_C	t_r, $t_f \leq$ 15ns *3	100		ns
XSCL high level pulse duration	t_{WCH}		35		ns
XSCL low level pulse duration	t_{WCL}		35		ns
Data setup time	t_{DS}		15		ns
Data hold time	t_{DH}		10		ns
XSCL → LP rise time	t_{LD}		–10		ns
XSCL → LP fall time	t_{LH}		60		ns
LP high-level pulse width	t_{WLH}	*1	75		ns
		*2	65		ns
FR delay allowance	t_{DF}		–300	+300	ns
EIO set-up time	t_{SUE}		40		ns
Input signal variation time	t_r, t_f	*4		50	ns

*1 t_{WLH} prescribes the LP "H" and XSCL "L" time, when LP is input during the "L" period of XSCL.
*2 t_{WLH} when LP rises from the XSCL "H" period (the definition is the same as the above *1).
*3 It is limited to $t_r + t_{rf} \leq (t_C - t_{WCL} - t_{WCL})$, when the shift clock (XSCL) is operated in high-speed mode.
*4 When high-speed data transmission is done with continuous shift clock, the maximum of the LP signal $t_r + t_f$ is $(t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH})$.

Output timing characteristics



V_{CC} = +5.0V ±10%, V_{DDH} = +14.0 to +42.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15pF (EIO)		120	ns
EIO output delay time	t_{DCL}			45	ns
LP→SEG output delay time	t_{LSD}	C_L = 100pF (O n)		200	ns
FR→SEG output delay time	t_{FRSD}			400	ns

V_{CC} = +2.7V to 4.5V, V_0 = +14.0 to +28.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15pF (EIO)		240	ns
EIO output delay time	t_{DCL}			85	ns
LP→SEG output delay time	t_{LSD}	C_L = 100pF (O n)		400	ns
FR→SEG output delay time	t_{FRSD}			800	ns

10. LIQUID CRYSTAL DRIVE POWER

10-1 Formation of Voltage Levels

The optimum way to obtain the voltage levels to drive the liquid crystal, is to divide the resistance so that it can be driven by the voltage follower of the operation amplifier. The terminal for the minimum potential level V5 and GND of the liquid crystal drive is separated, considering the use of the operation amplifier. However, if the potential of V5 rises above GND potential, causing the voltage to be too large, the capacity of the liquid crystal driver will deteriorate, so it is recommended that the voltage kept between 0 V and 2.5 V.
If the operation amplifier is not used, connect V5 and GND. When resistance division is to be used, set the resistance as low as possible within the allowable power range of the system.

When the V0 (GND) power line has serial resistance, the I0 at the change of the signal will cause V0 (GND) voltage fall at the LSI power terminal, disabling the relation of the LCD with the intermittent potential (V0 ≥ V1 ≥ V4 ≥ V5 ≥ GND), thus destroying the LSI.
When inserting a protection resister, the voltage must be stabilized by the capacity.

10-2 Notes Upon Power On/Off

This LSI has high voltage in the liquid crystal system, and if voltage higher than 30 V is applied to the liquid crystal drive system with the power of the logic system at the floating level or below V_{CC} = 2.6 V, or if liquid crystal drive signal is output before the voltage applied to the liquid crystal drive system is stabilized, overcurrent flows to destroy the LSI.
Therefore, it is recommended to maintain the liquid crystal drive output voltage at the V5 level till the voltage of the liquid crystal drive system stabilizes, using the display off function ($\overline{DSPOF}$).

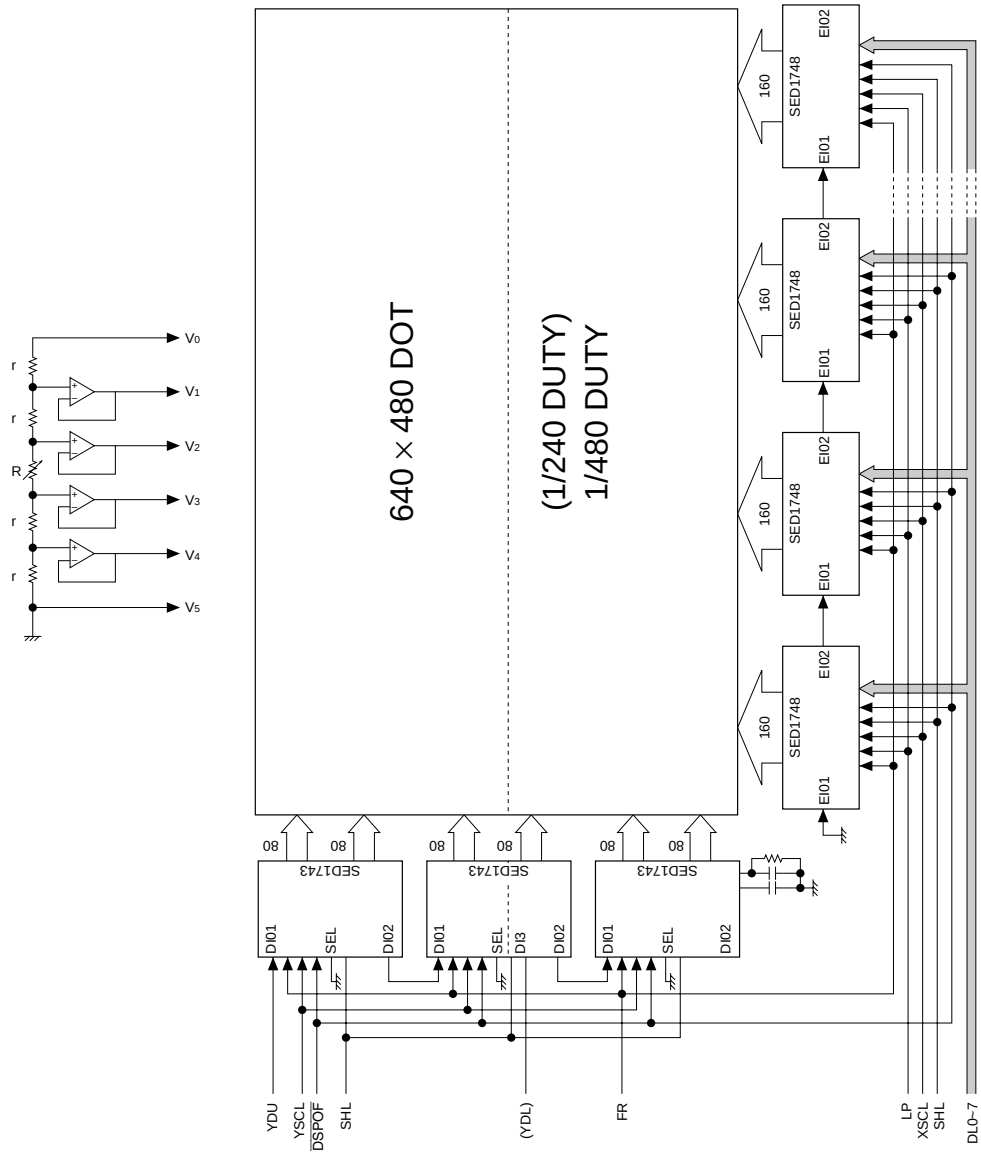
Observe the following power on/off sequence.

Power on Logic system on → liquid crystal drive system on, or simultaneously on
Power off Liquid crystal drive system on → logic system off, or simultaneously off

A fast melting fuse or protection resistance inserted in series with the liquid crystal power supply is effective as protection against overcurrent.
The optimum protection resistance must be selected from the capacity of the liquid crystal cell.

11. CONNECTION EXAMPLE

Large screen LCD structural diagram



6. SED1752
LCD Driver

Contents

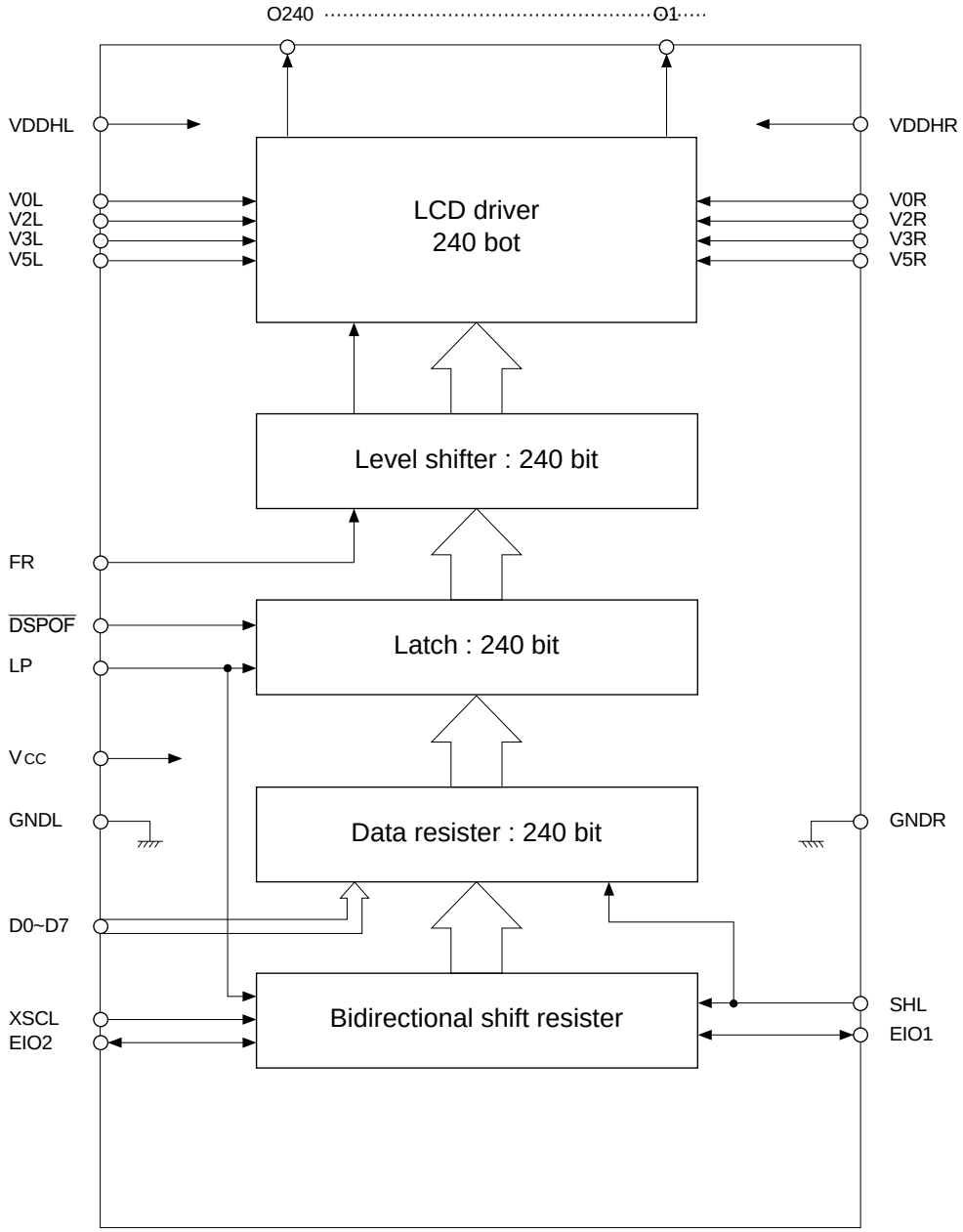
1. OUTLINE

SED1752 is a 240 output segment (column) LCD driver suitable for driving of colored STN dot-matrix LCD panels of a larger capacity, for use in combination with SED1743.
Contributing to making clearer LCD picture quality, this IC employs the high speed enable chain method and is slim-chip configuration which is more advantageous for miniaturization of the LCD panel. SED1752 is also capable of low-voltage and high-speed logic operations and fits to a wide range of applications.

2. FEATURES

- Number of LCD drive output segments: 240
- Low voltage operation: 2.7V min.
- High duty drive: 1/500 (an example)
- Wide LCD drive voltage range: + 8 to + 42V (V_{DD} = 3 to 5.5V)
- High speed and low power consumption data transfer is possible by adoption of the 8-bit bus enable chain method:
  Shift clock frequencies: 20.0 MHz (5V ±10%)
  10.0 MHz (2.7V)
- Slim-chip configuration
- Non-bias display off function
- Pin-selection of the output shift direction is available
- Offset bias regulation of LCD power for respective V_{DDH} and GND levels is possible
- Logic operation power supply: 2.7 ~ 5.5V
- Shipped status: TCP SED1752T**
- This IC is not radiation resistant

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Numbers of pins</th></tr>
<tr><td>O1~ O240</td><td>O</td><td>LCD driving segment (column) output.
The output varies at the falling edge of LP.</td><td>240</td></tr>
<tr><td>D0~D7</td><td>I</td><td>Display data input terminals</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>For input of the shift clock signals of the display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>For input of the latch pulse signals of the display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O.
Setting to I or O is determined by the SHL input level.
The output is reset by the LP input and when 240 bit equivalent data are received, it falls to “L” automatically.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO terminal I/O control signal input.
When data are input to terminals D_0, D_1 ....,D_7 in the order of F_0, F_1 .....,F_7 first, and in the order of L0, L1, outputs are as follows:
F (First), L (Last)
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><td>O240</td><td>O239</td><td>O238</td><td></td><td>O3</td><td>O2</td><td>O1</td><td>EIO1</td><td>EIO2</td></tr>
<tr><td>L</td><td>L0</td><td>L1</td><td>L2</td><td>...</td><td>F5</td><td>F6</td><td>F7</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>F7</td><td>F6</td><td>F5</td><td>...</td><td>L2</td><td>L1</td><td>L0</td><td>Output</td><td>Input</td></tr>
</table>
(Note) The relations between the data and segment outputs are determined independent from the number of the shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>For input of alternating current LCD drive signals.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL
GNDR</td><td>Power supply</td><td>Logic operation power supply: GND: 0V
V_{CC}: +3.3, +5V</td><td>2</td></tr>
<tr><td>V_{DDHL}, V_{DDHR}</td><td rowspan="5">Power supply</td><td>LCD drive power supply V_{DDH}</td><td rowspan="5">GND: 0V V_{DDH}:14~42V
$V_{DDH} \geq V_0 \geq V_2 \geq 7/9 V_0$
$2/9\ V_0 \geq V_3 \geq V_5 \geq$ GND</td><td rowspan="5">10</td></tr>
<tr><td>V0L,V0R</td><td>" V_0</td></tr>
<tr><td>V2L, V2R</td><td>" V_2</td></tr>
<tr><td>V3L, V3R</td><td>" V_3</td></tr>
<tr><td>V5L, V5R</td><td>" V_5</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>For forced bias fixed input.
“L” level output is forcefully made to V_5 level.
* When using this function, combined use with SED1703 is not applicable.</td><td>1</td></tr>
<tr><td></td><td></td><td>Total</td><td>268</td></tr>
</table>

5. FUNCTION OF EACH BLOCK

5-1 Enable shift resister

The enable shift register is a bidirectional shift register of which the shift direction is being selected by the SHL input and the shift register output is used to store data bus signals into the data register.
When the enable signal is in disabled state, the internal clock signal and the data bus are fixed to "L", thus going into a power saving mode.
When using multiple number of segment drivers, make cascade connection of EIO terminals of respective drivers to connect the EIO terminal of the top driver to "GND". (Refer to Clause 10. Connection examples)
Since the enable control circuit automatically senses completion of receiving 240 bit equivalent data to transfer the enable signal automatically, control signal of a separate control LSI is not needed.

5-2 Data register

This register works to make series or parallel conversion of data bus signals according to the enable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independent from the number of the shift clock inputs.

5-3 Latch

It takes in the content of the data register at the falling edge trigger to transfer the output to the level shifter.

5-4 Level shifter

This is a level interface circuit to convert the voltage level of signals from the logic operation level to LCD drive level.

5-5 LCD driver

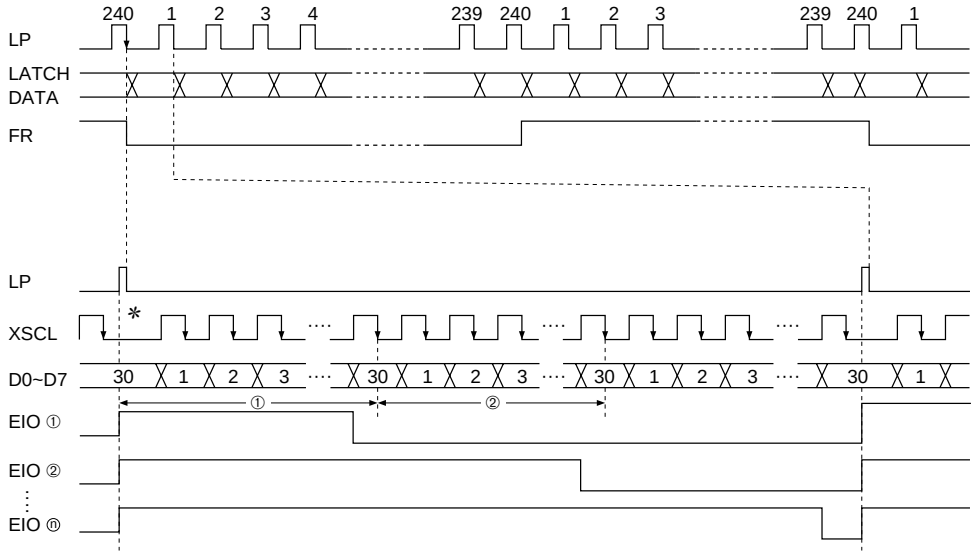
It outputs the LCD driving voltage.
Given below are the relations between data bus signals, alternating current signal FR levels and segment output voltages.

$\overline{\text{DSPOF}}$	Data bus signals	FR	Voltage outputs of the driver
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	–	–	V_5

5-6 Timing diagram

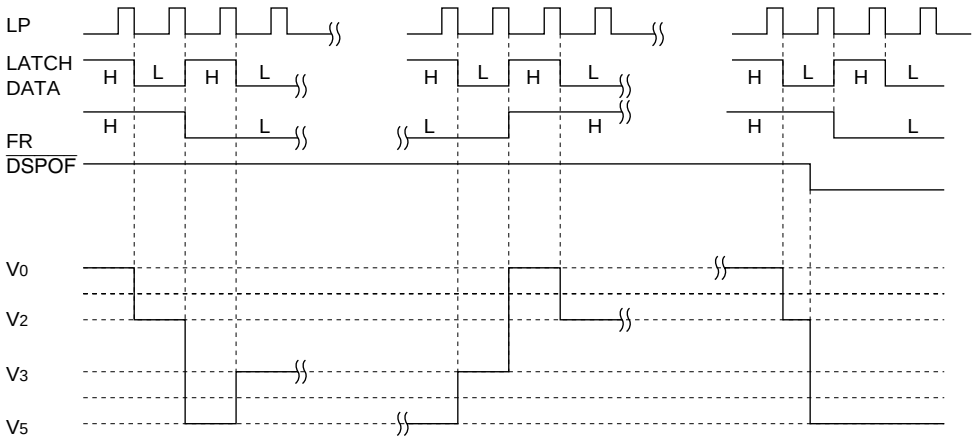
Timing diagram

In case of 1/240 Duty (an example)



① ~ ⓝ stands for the cascade numbers of the driver.

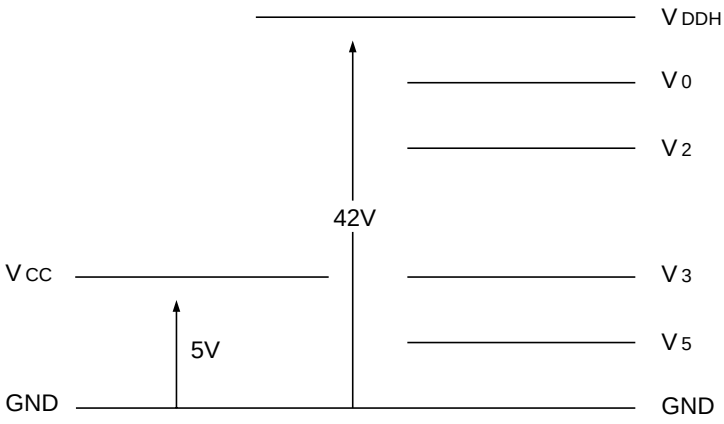
* When making high speed data transfer, it becomes necessary to secure a longer XSCL cycle when determining the LP pulse insertion timing in order to maintain the specified value of LP → XSCL (t_{LH}).



6. ABSOLUTE MAXIMUM RATINGS

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	–0.3 to V_{CC} + 0.3	V
Output voltage	V_O	–0.3 to V_{CC} + 0.3	V
EIO output current	I_{01}	20	mA
Working temperature	Topr	–30 to +85	°C
Storage temperature	Tstg	–55 to +100	°C

(Note 1) All the voltage ratings are based on GND = 0V.
(Note 2) The storage temperature 1 is applicable to independent chips and the storage temperature 2 is applicable to the TCP modular state.
(Note 3) V_0, V_2, V_3 and V_5 should always be in the order of $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



(Note 4) If the logic operation power goes into a floating state or if V_{CC} drops to 2.6V or below while the LCD driving power is being applied, the LSI may be damaged. Therefore, keep from occurrence of the aforementioned status.
Specifically, pay close attention to the power supply sequence at times of turning the system power on and off.

7. ELECTRICAL CHARACTERISTICS

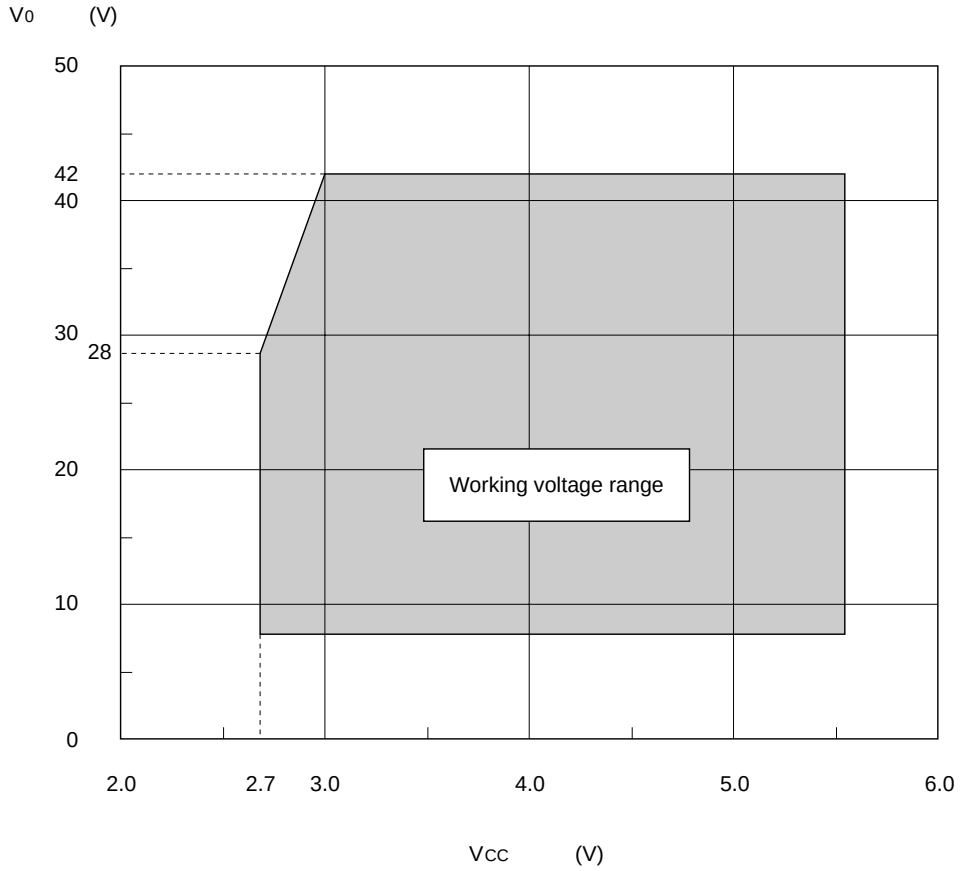
7-1 DC characteristics

Unless otherwise specified, GND = 0V, V_{CC} = +5.0 V ±10%, Ta = –30 to 85°C

Item	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}	—	V_{CC}	2.7	—	5.5	V
Recommended working voltage	V_0	—	V0L,VDDHL	14.0	—	40.0	V
Workable voltage	V_0	Function only	V0R,VDDHL	8.0	—	42.0	V
Supply voltage (2)	V_2	Recommended value	V2L, V2R	7/9 V_0	—	V_0	V
Supply voltage (3)	V_3	Recommended value	V3L, V3R	GND	—	2/9 V_0	V
High level input voltage	V_{IH}	V_{DD} = 2.7 ~ 5.5V	EIO1,EIO2,FR D0~D7,$\overline{XSCL}$ $\overline{SHL}$,LP,$\overline{DSPOF}$	0.8V_{CC}	—	—	V
Low level input voltage	V_{IL}			—	—	0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC}= 2.7~5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{CC}–0.4	—	—	V
Low level output voltage	V_{OL}	V_{CC}= 2.7~5.5V, I_{OL} = 0.6mA		—	—	0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0~D7,LP,FR XSCL, SHL $\overline{DSPOF}$	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	EIO1, EIO2	—	—	5.0	µA
Static current	I_{GND}	V_0 = 14.0~42.0V V_{IH} = V_{CC}, V_{IL}=GND	GND	—	—	25	µA
Output resistance	R_{SEG}	△V_{ON} =0.5V Recommended condition: V_0 =+36.0V, 1/24	O1~O240	—	0.65	0.85	KΩ
		△V_{ON} =0.5V Recommended condition: V_0 =+26.0V, 1/20		—	0.70	1.0	
In-chip deviation of output resistance	△R_{SEG}	△V_{ON}=0.5V V_0 = +36.0V, 1/24	O1~O240	—	—	95	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, fXSCL = 5.38MHz fLP = 33.6kHz, fFR = 70Hz Input data: Checkered indication, no-load	V_{CC}	—	0.75	1.7	mA
		V_{CC} = +3.0V Other conditions are the same as those when V_{CC} = 5V.		—	0.3	0.9	
Mean working current consumption (2)	I_O	V_0 = +30.0V V_{CC} = +5.0V, V_3 = +4.0V V_2 = +26.0V, V_5 = +0.0V Other conditions are the same as those in the I_{DD} column.	V0L, V0R	—	0.25	1.4	mA
Input terminal capacity	C_I	Freq. = 1 MHz Ta = 25°C Independent chips	D0~D7, LP, FR, $\overline{XSCL}$, $\overline{SHL}$, $\overline{DSPOF}$	—	—	8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2	—	—	15	pF

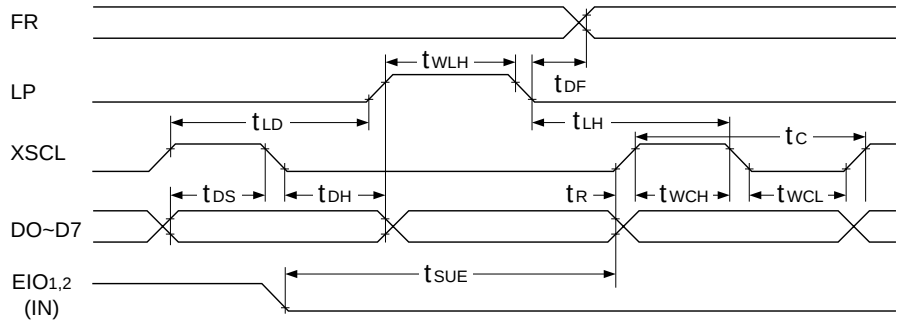
Working voltage range VCC - V0

The V0 voltage should be set up within the VCC - V0 working voltage range given below.



7-2 AC CHARACTERISTICS

Input timing characteristics



V_{CC} = 5.0V ±10%, Ta = –30 to 85°C

Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	tc	*3, *5	55	—	ns
XSCL high level pulse duration	t_{WCH}	All timing	20	—	ns
XSCL low level pulse duration	t_{WCL}	signals are	20	—	ns
Data setup time	t_{DS}	based on 20%	10	—	ns
Data hold time	t_{DH}	and 80% of V_{CC}.	10	—	ns
XSCL → LP rise time	t_{LD}		0	—	ns
LP → XSCL fall time	t_{LH}		35	—	ns
LP high level pulse duration	t_{WLH}	*1	40	—	ns
		*2	35	—	ns
FR delay allowance	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		30	—	ns
Input signal variation time	t_r, t_f	*4	—	50	ns

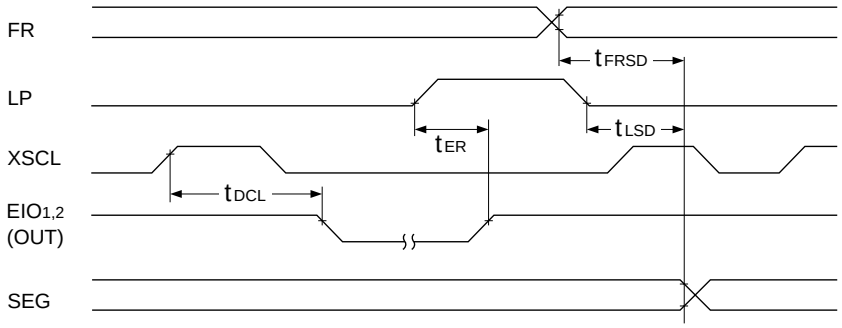
V_{CC} = 2.7V to 4.5V, Ta = –30 to 85°C

Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	tc	*3, *5	100	—	ns
XSCL high level pulse duration	t_{WCH}	All timing	35	—	ns
XSCL low level pulse duration	t_{WCL}	signals are	35	—	ns
Data setup time	t_{DS}	based on 20%	15	—	ns
Data hold time	t_{DH}	and 80% of V_{CC}.	10	—	ns
XSCL → LP rise time	t_{LD}		–10	—	ns
LP → XSCL fall time	t_{LH}		60	—	ns
LP high level pulse duration	t_{WLH}	*1	75	—	ns
		*2	65	—	ns
FR delay allowance	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		40	—	ns
Input signal variation time	t_r, t_f	*4	—	50	ns

Notes: *1 The "t_{WLH}" specifies the time when the LP is at "H" and, at the same time, when XSCL is at "L", when LP is being input while the XSCL is at "L".

* 2 The "t_{WLH}" (its definition is same as *1) when LP rises while XSCL is at "H".
* 3 High speed operation of the shift clocks (XSCL) should only be made under a condition of $t_r + t_f \leq (t_C - t_{WCL} - t_{WCH})$.
* 4 When making high speed data transfer using continuous shift clocks, $t_r + t_f$ of the LP signals should be upto $(t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH})$ at the maximum.
* 5 When "tc" is set to 60 nsec or less, "Ta" must be 55°C or less.

Output timing characteristics



V_{CC} = +5.0V ±10%, V_0 = +14.0 to +42.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EIO)	—	120	ns
EIO output delay time	t_{DCL}		—	55	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (O n)	—	200	ns
FR → SEG output delay time	t_{FRSD}		—	400	ns

V_{CC} = +2.7V to 4.5V, V_0 = +14.0 to +28.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EIO)	—	240	ns
EIO output delay time	t_{DCL}		—	85	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (O n)	—	400	ns
FR → SEG output delay time	t_{FRSD}		—	800	ns

8. LCD DRIVING POWER SUPPLY

8-1 Setting up respective voltage levels

When setting up respective voltage levels for LCD drive, it is the best way to resistively divide the potential between V_0 - GND to drive the LCD by means of voltage follower using an operation amplifier.
In consideration of the case of using an operation amplifier, the LCD driving minimum potential level V5 and GND are separated and independent terminals are used.
However, since the efficacy of the LCD driving output driver deteriorates when the potential of V_5 goes up beyond the GND potential to enlarge the potential difference, always keep the potential difference of V_5 - V_{SS} at 0V to 2.5V.
When a resistance exists in series in the power supply line of V_0 (GND), Io at signal changes causes voltage drop at V_0 (GND) of the supply terminals of the LSI disabling it to maintain the relations of the LCD with intermediate potentials of ($V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND), thus leading to breakdown or destruction of the LSI.
When using a protective resistor, do not fail to stabilize the voltage using an appropriate capacitance.

8-2 Precautions when turning the power on and off

Since the LCD drive voltage of these LSIs is comparatively high, if a high voltage of 30V or more is applied to the LCD drive circuit with the logic operation power made floating or with the V_{CC} lowered to 2.6V or less, or when LCD drive signals are output before applied voltage to the LCD drive circuits is stabilized, excess current flows through to possibly lead to breakdown or to destroy the LSI.
It is therefore suggested to maintain the potential of the LCD drive output to V_5 level until the LCD drive circuit voltage is stabilized, using the display off function ($\overline{DSPOF}$).
Maintain the following sequences when turning the power on and off:

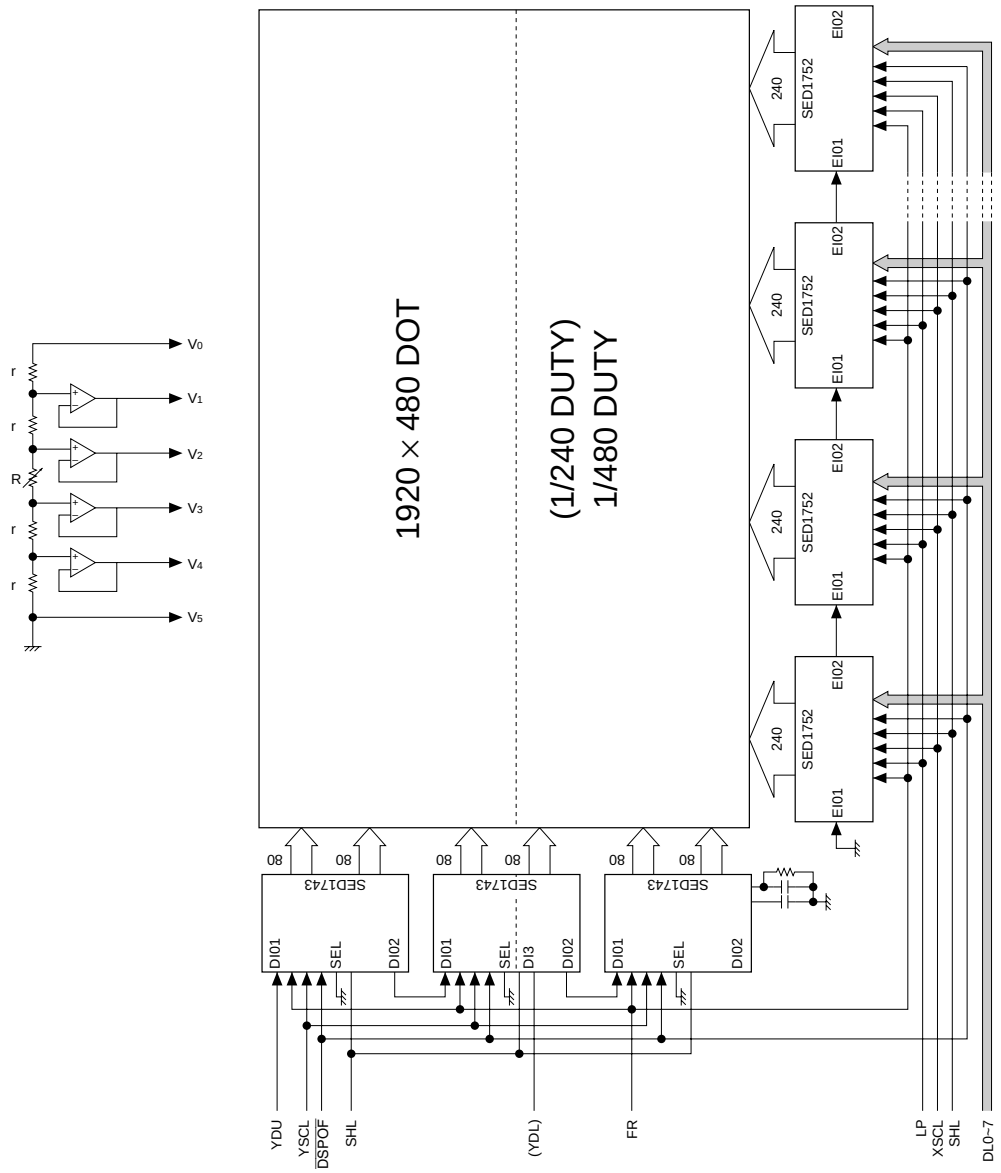
When turning the power on: Turn on the logic operation power → turn on the LCD drive power or turn them on simultaneously.

When turning the power off: Turn off the LCD drive power → turn off the logic operation power or turn them off simultaneously.

For protection against excess current, insert a quick melting fuse in series in the LCD drive power line.
When using a protective resistor, select the optimum resistance value depending on the capacitance of the LCD cells.

9. A CONNECTION EXAMPLE

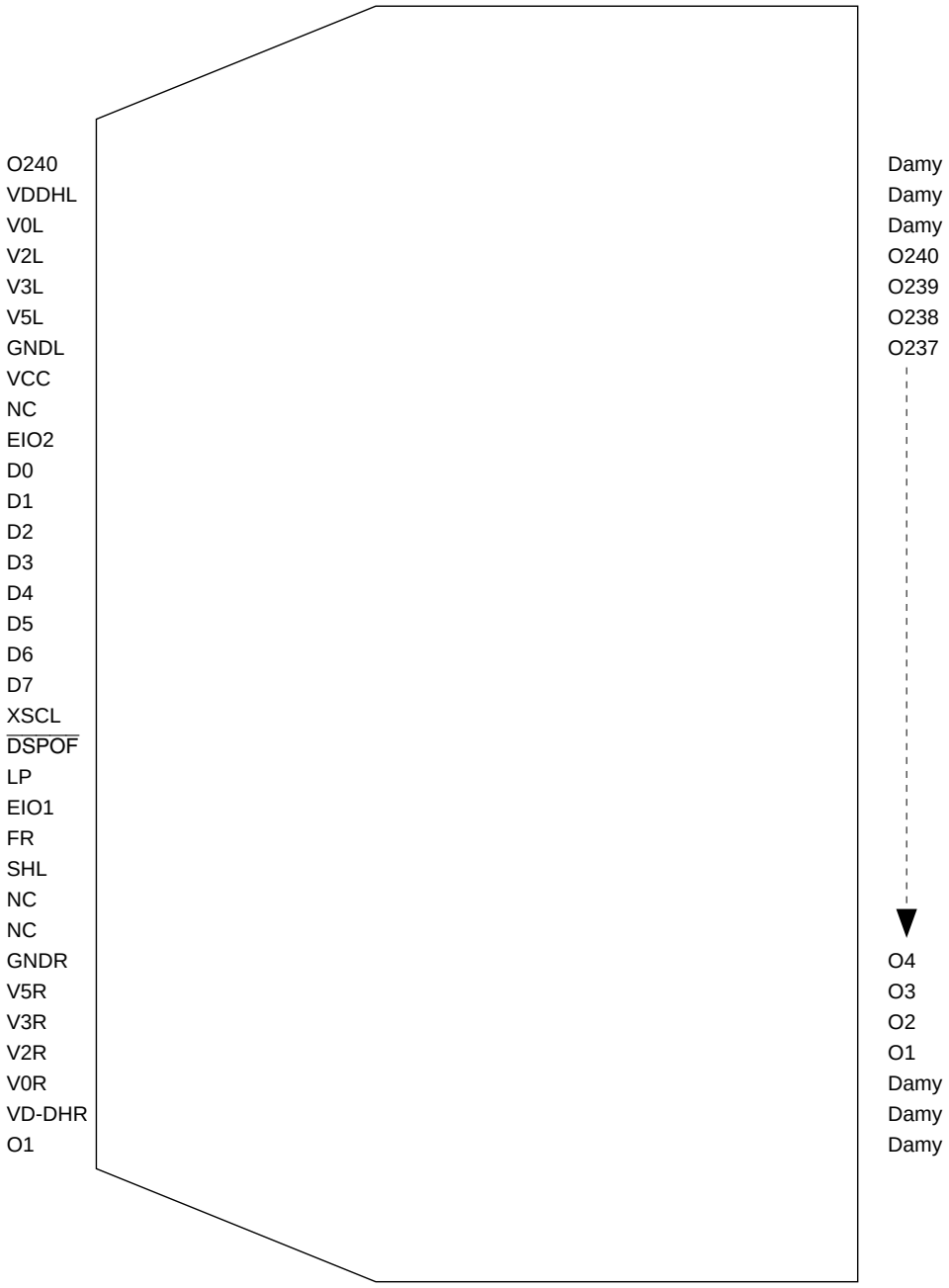
Block diagram of a large-plane LCD



For reference

10. SED1752T TCP PIN ARRANGEMENT EXAMPLE

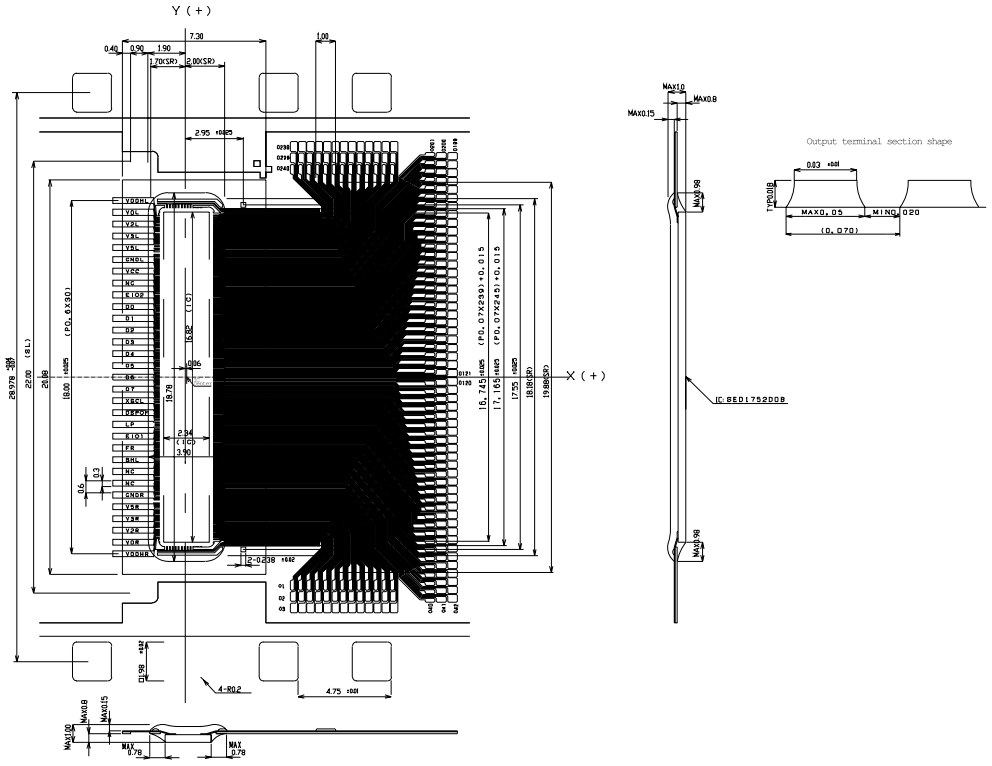
Remark: This drawing is not meant to determine the contour of the TCP.



11. DIMENSIONAL OUTLINE DRAWING

SED1752T0A

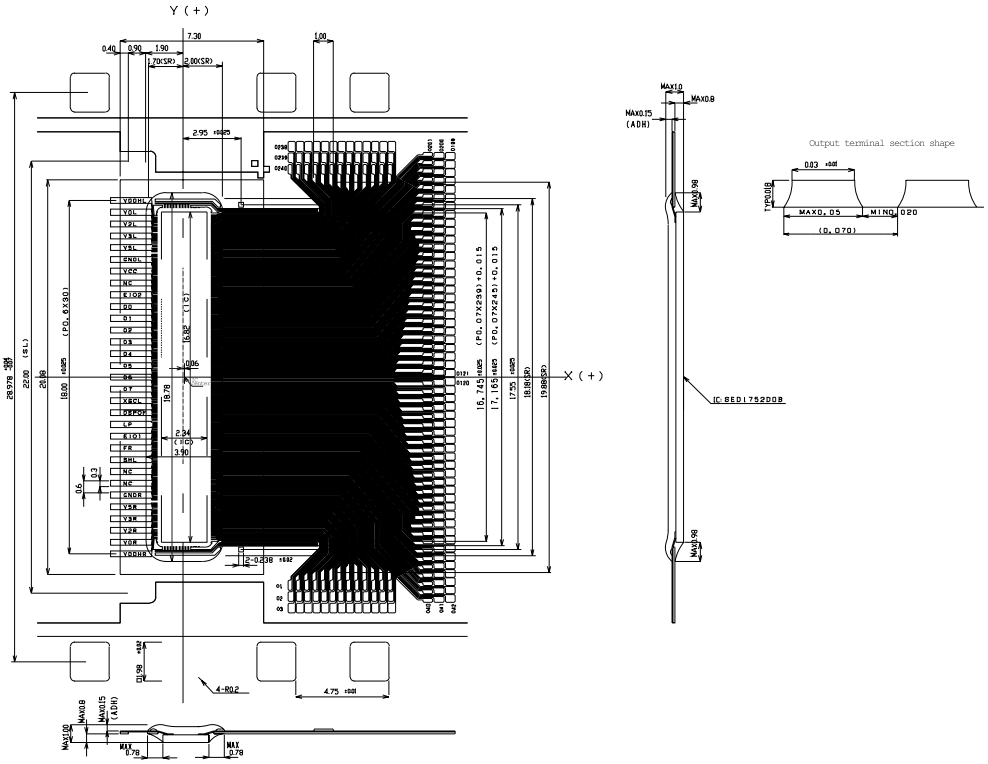
For reference



Unit: mm

SED1752T0B

For reference



Unit: mm

7. SED1753
LCD Driver

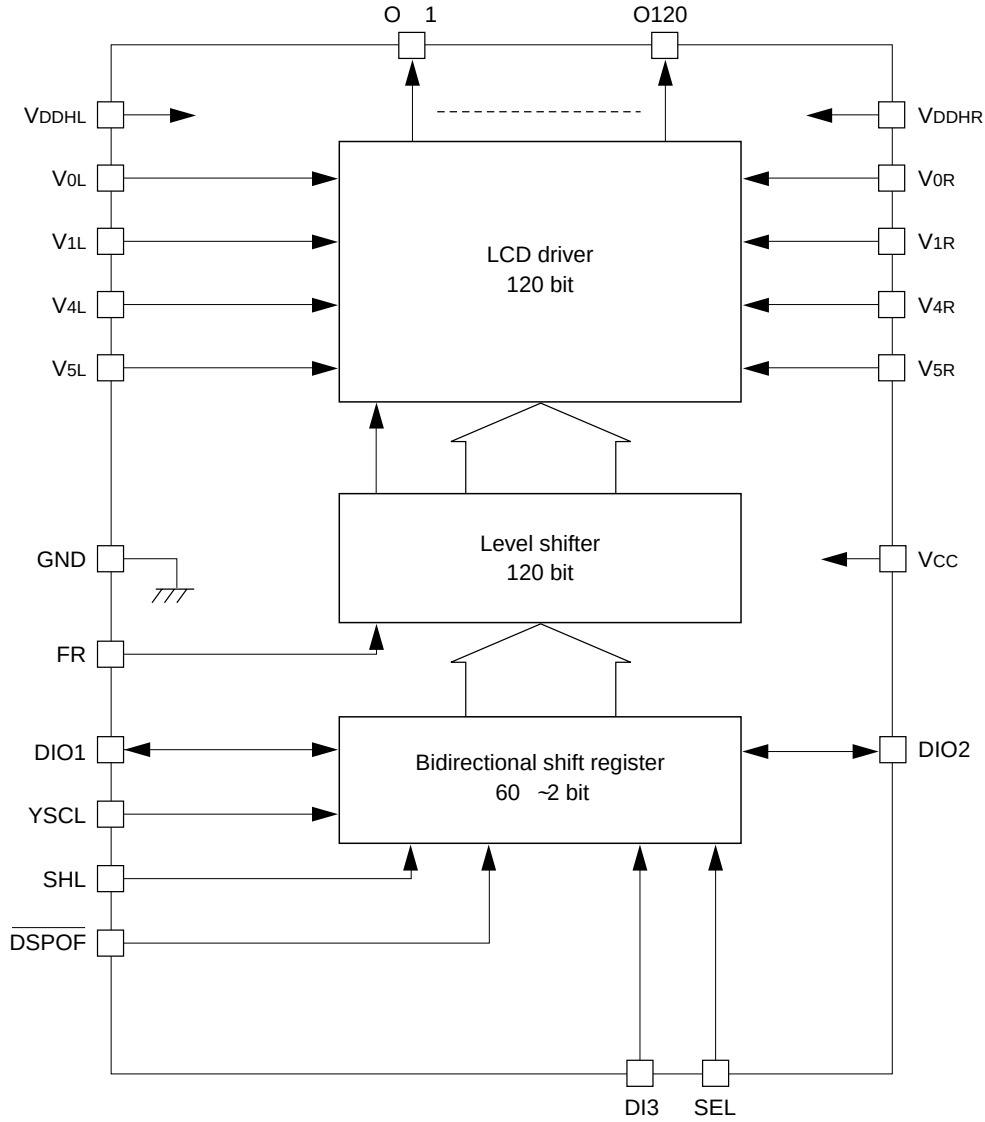
Contents

The SED1753 is a 120-output low output resistance-common (low) driver most suited to drive the extra large-capacity dot matrix liquid crystal panel. It is used paired with the SED1752 and DES1758. It ensures high-resolution thanks to the wide LCD drive voltage range.
This driver can be employed in a wide range of applications for the long type chip layout suited for smaller LCD panels. It promises the highest driver efficiency for panels with 1/240, 1/300 and 1/480 duty thanks to bidirectional driver output sequences, higher tension resistance than current models and 60 × 2 pairs of low output impedance LCD output.

FEATURES

- 120 LCD drive outputs (60 × 2 structure)
- Common output ON resistance: 0.3KΩ (Typ.)
- Applicable for high duty : 1/480 (Reference)
- Pin selectable output shift direction
- Non-bias display off function
- Long-sideways chip
- LCD power offset bias adjustable corresponding to V_{DDH} and GND levels
- Wide LCD drive voltage range: 8V to 42V
- Logic system power supply: 2.7 to 5.5V
- Package: TCP
- This IC is not designed for radiation protection

BLOCK DIAGRAM



BLOCK FUNCTIONS

Shift register

Bidirectional shift register for common data transfer. It has 60 × 2 bit structure, and allows selection between 60 × 2 bit and 120 bit depending on state of SEL.
When 60 × 2 bit structure is selected, input to the succeeding 60 bit shift register is DI3.

Level shifter

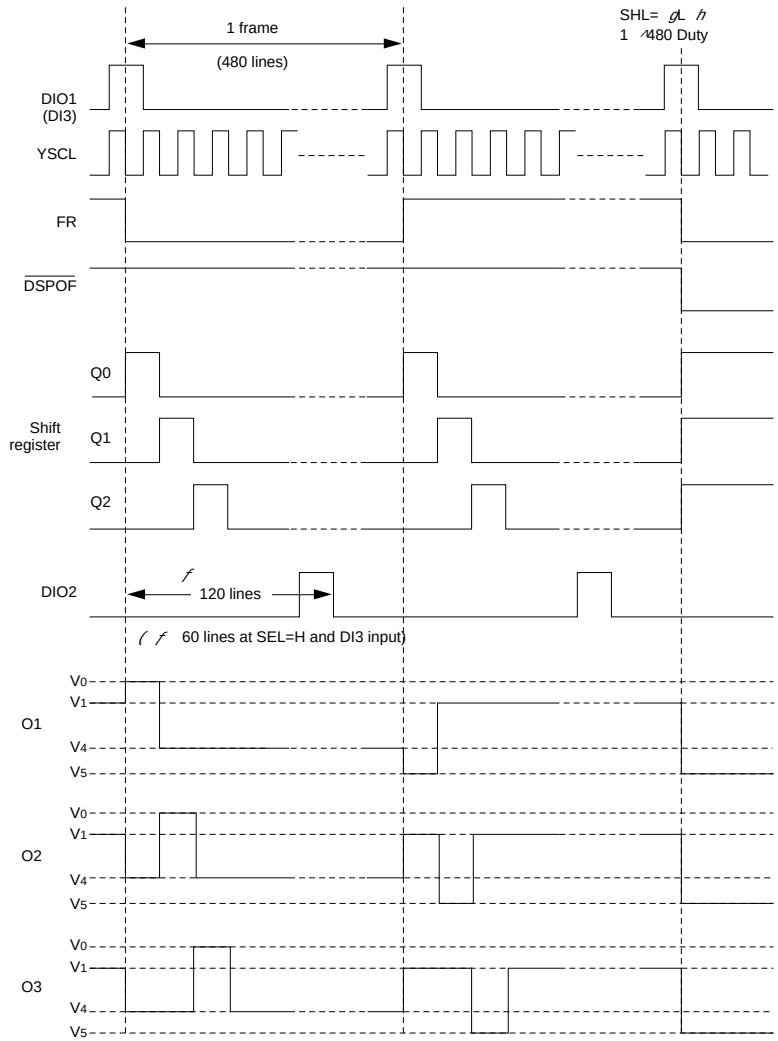
Voltage level interface circuit for converting voltage level of a signal from logic system level to LCD drive level.

LCD driver

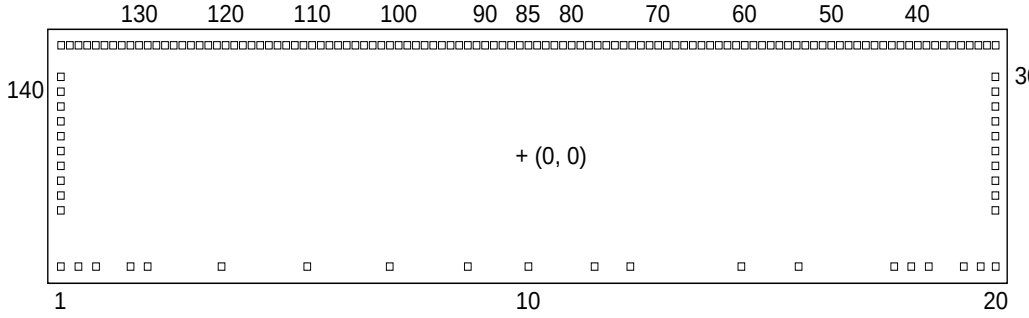
Outputs LCD drive voltage. The following table shows the relation between display blanking signal $\overline{DSPOF}$, shift register contents, frame signal FR and common output voltage.

$\overline{DSPOF}$	Shift register contents	FR	On output voltage	
H	H	H	V_5	On level
		L	V_0	
	L	H	V_1	Off level
		L	V_4	
L	—	—	V_5	—

Timing diagram



BUMP LAYOUT



Chip size	9.41 mm × 2.23 mm
Pad pitch	83.6 µm
Chip thickness	625 µm × 25 µm

1) Au bump specification (SED1753D0B) (For reference)
Au vertical bump

	Scribe horizonal	×	Scribe vertical	±	tolerance	
Bump size A	75.1 µm	×	79.8 µm	±	4 µm	(Pad No. 1 to 22, 147, 148)
Bump size B	74.1 µm	×	74.1 µm	±	4 µm	(Pad No. 23 to 30, 139 to 146)
Bump size C	65.6 µm	×	80.8 µm	±	4 µm	(Pad No. 31 to 35, 134 to 138)
Bump size D	54.2 µm	×	80.8 µm	±	4 µm	(Pad No. 36 to 84, 86 to 133)
Bump size E	98.8 µm	×	80.8 µm	±	4 µm	(Pad No. 85)
Bump thickness	17 to 28 µm					

BUMP CENTER COORDINATE

PAD No.	PIN Name	X	Y
1	Dummy	-4536	-940
2	V1L	-4393	-940
3	V4L	-4236	-909
4	V5L	-3899	-940
5	Dummy	-3748	-940
6	GND	-2992	-957
7	DI01	-2144	-952
8	FR	-1349	-952
9	$\overline{\text{DSP0F}}$	-573	-952
10	SHL	-13	-952
11	SEL	652	-952
12	DI3	1010	-952
13	YSCL	2077	-952
14	DI02	2636	-952
15	VCC	3560	-952
16	Dummy	3729	-952
17	V5R	3899	-952
18	V4R	4236	-909
19	V1R	4392	-940
20	*1	4535	-940
21	V0R	4524	-477
22	VDDHR	4524	-324
23	Dummy	4542	-175
24	O120	4542	-52
25	O119	4542	72
26	O118	4542	195
27	O117	4542	319
28	O116	4542	442
29	O115	4542	566
30	O114	4542	689
31	*2	4546	959
32	O113	4451	959
33	O112	4356	959
34	O111	4261	959
35	O110	4166	959
36	O109	4077	959
37	O108	3993	959
38	O107	3910	959
39	O106	3826	959
40	O105	3743	959
41	O104	3659	959
42	O103	3575	959
43	O102	3492	959
44	O101	3408	959
45	O100	3325	959
46	O99	3241	959
47	O98	3157	959
48	O97	3074	959
49	O96	2990	959
50	O95	2907	959
51	O94	2823	959
52	O93	2739	959
53	O92	2656	959
54	O91	2572	959
55	O90	2489	959
56	O89	2405	959
57	O88	2321	959
58	O87	2238	959
59	O86	2154	959
60	O85	2071	959
61	O84	1987	959
62	O83	1903	959

PAD No.	PIN Name	X	Y
63	O82	1820	959
64	O81	1736	959
65	O80	1653	959
66	O79	1569	959
67	O78	1485	959
68	O77	1402	959
69	O76	1318	959
70	O75	1235	959
71	O74	1151	959
72	O73	1067	959
73	O72	984	959
74	O71	900	959
75	O70	817	959
76	O69	733	959
77	O68	649	959
78	O67	566	959
79	O66	482	959
80	O65	399	959
81	O64	315	959
82	O63	231	959
83	O62	148	959
84	O61	64	959
85	O60	–42	959
86	O59	–148	959
87	O58	–231	959
88	O57	–315	959
89	O56	–399	959
90	O55	–482	959
91	O54	–566	959
92	O53	–649	959
93	O52	–733	959
94	O51	–817	959
95	O50	–900	959
96	O49	–984	959
97	O48	–1067	959
98	O47	–1151	959
99	O46	–1235	959
100	O45	–1318	959
101	O44	–1402	959
102	O43	–1485	959
103	O42	–1569	959
104	O41	–1653	959
105	O40	–1736	959
106	O39	–1820	959
107	O38	–1903	959
108	O37	–1987	959
109	O36	–2071	959
110	O35	–2154	959
111	O34	–2238	959
112	O33	–2321	959
113	O32	–2405	959
114	O31	–2489	959
115	O30	–2572	959
116	O29	–2656	959
117	O28	–2739	959
118	O27	–2823	959
119	O26	–2907	959
120	O25	–2990	959
121	O24	–3074	959
122	O23	–3157	959
123	O22	–3241	959
124	O21	–3325	959

PAD No.	PIN Name	X	Y
125	O20	–3408	959
126	O19	–3492	959
127	O18	–3575	959
128	O17	–3659	959
129	O16	–3743	959
130	O15	–3826	959
131	O14	–3910	959
132	O13	–3993	959
133	O12	–4077	959
134	O11	–4166	959
135	O10	–4261	959
136	O9	–4356	959
137	O8	–4451	959
138	*2	–4546	959
139	O7	–4542	689
140	O6	–4542	566
141	O5	–4542	442
142	O4	–4542	319
143	O3	–4542	195
144	O2	–4542	72
145	O1	–4542	–52
146	Dummy	–4542	–175
147	VDDHL	–4545	–324
148	V0L	–4545	–477

*1: Do not connect with other terminals as the setting is GND level.
*2: Do not connect with other terminals as the setting is VDDH level.

PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Numbers of pins</th></tr>
<tr><td>O1 to O120</td><td>O</td><td>LCD drive common (low) output.
The output changes at the YSCL falling edge.</td><td>120</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>60 × 2 bit bidirectional shift register scan pulse.
The pin is set to input or output depending on the SHL input.
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>Scan pulse input pin for 60 × 2 bit structure.
DI3 is connected to GND when SEL is at low-level.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Selective input of the bidirectional shift register operation modes.
H: 60 × 2 (DI3 input). L: 120.</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input.
It shifts scan data at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO pin I/O control signal input.
<table>
<tr><th>SHL</th><th>O output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>H</td><td>1 ⟶ 60 61 ⟶ 120</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>120 ⟶ 61 60 ⟶ 1</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{\text{DSPOF}}$</td><td>I</td><td>Liquid crystal display blanking control signal input.
Entering “L” causes all common outputs to go V_5 level.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output frame signal input.</td><td>1</td></tr>
<tr><td>GND, V_{CC}</td><td>Power</td><td>Logic operation power.
GND: 0V V_{CC}: +2.7V to 5.5V</td><td>2</td></tr>
<tr><td>V_{0L}, V_{1L}, V_{4L}
V_{5L}, V_{DDH}
V_{0R}, V_{1R}, V_{4R}
V_{5R}, V_{DDHR}</td><td>Power</td><td>LCD drive power.*1
GND: 0V V_{DDH}: 8V to 42V
$V_{DDH} \geq V_0 \geq V_1 \geq 8/9V_{DDH}$
$1/9V_{DDH} \geq V_4 \geq V_5 \geq$ GND</td><td>10</td></tr>
<tr><td></td><td></td><td>Total</td><td>140</td></tr>
</table>

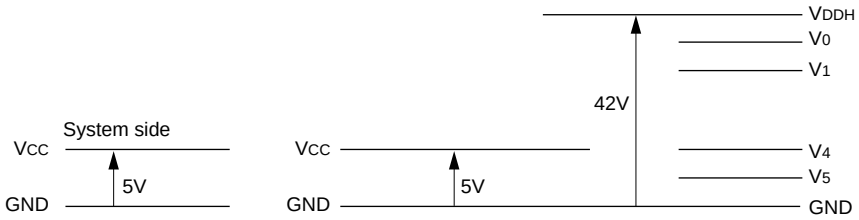
*1: Each pair of V_{DDH} and V_0 to V_5 must be connected to the LCD drive power supply. The above LCD drive power voltage range indicates the recommended value.

ABSOLUTE MAXIMUM RATING

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_1, V_4, V_5	GND – 0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} + 0.3	V
DIO output current	I_0	20	mA
Operating temperature	Topr	–40 to +85	°C
Chip storage temperature	Tstg1	–65 to +150	°C
TCP product storage temperature	Tstg2	–55 to +125	°C

Note 1: ALL stated voltages assume GND = 0V.

Note 2: V_0, V_1, V_4 and V_5 voltages shall always satisfy the condition of $V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq GND$.



Note 3: Do not allow the logic power goes floating state or drop below V_{CC} = 2.6V while applying the LCD drive power. Otherwise, the LSI could be permanently damaged. Special care is needed for the system power on or off sequences.

ELECTRIC CHARACTERISTICS

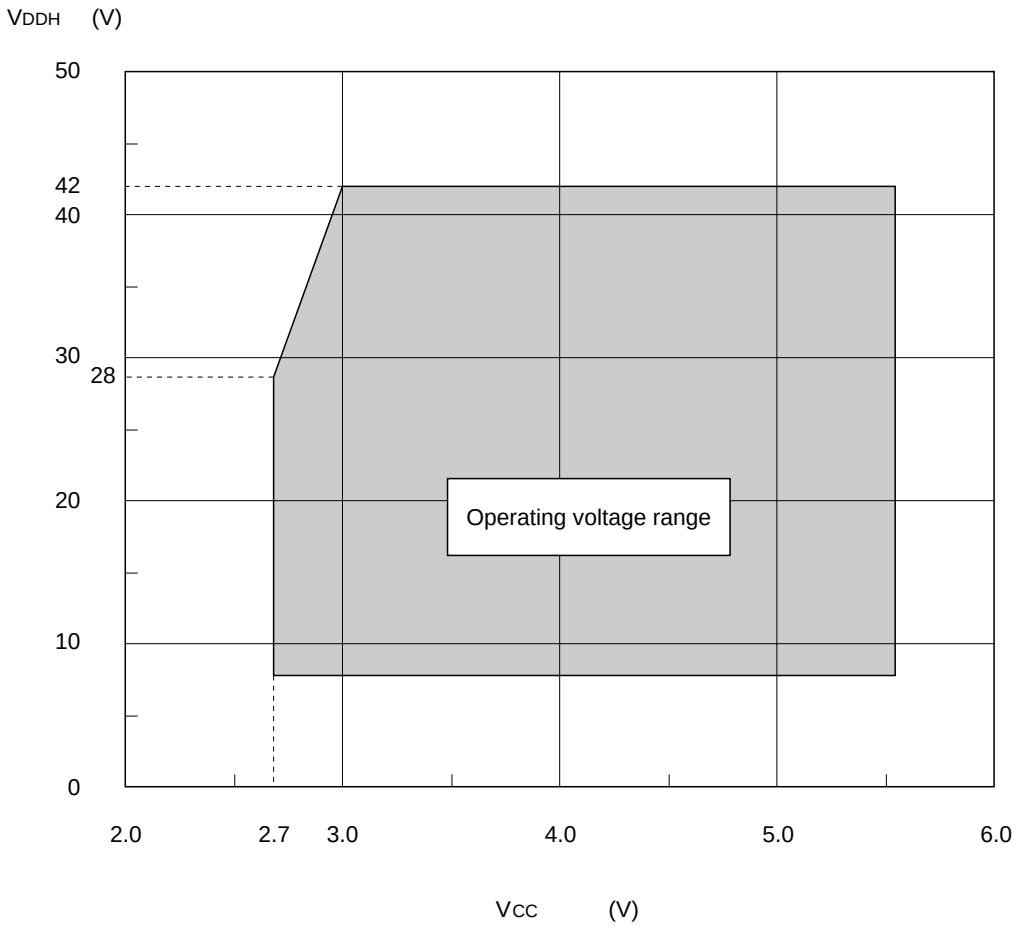
DC Characteristics

Except where otherwise specified,
GND = V_5 = 0V, V_{CC} = 5.0V±10%, Ta = –40 to 85°C are assumed.

Items	Codes	Conditions		Applicable pins	Min.	Typ.	Max.	Units
Supply voltage (1)	V_{CC}	—		V_{CC}	2.7	5.0	5.5	V
Recommended operating voltage	V_{DDH}	V_{CC} = 2.7 to 5.5V		V_{DDHL}, V_{DDHL} V_{0L}, V_{0R}	14.0	—	40.0	V
Operatable voltage	V_{DDH}	Function			8.0	—	42.0	V
Supply voltage (2)	V_1	Recommended value		V_{1L}, V_{1R}	8/9•V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V_4	Recommended value		V_{4L}, V_{4R}	GND	—	1/9•V_{DDH}	V
High-level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		DIO1, DIO2, FR, YSCL,	0.8•V_{CC}	—	—	V
Low-level input voltage	V_{IL}			SHL, DI3 $\overline{\text{DSPOF}}$, SEL	—	—	0.2•V_{CC}	V
High-level output voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = –0.3mA	DIO1, DIO2	V_{CC} – 0.4	—	—	V
Low-level output voltage	V_{OL}		I_{OL} = 0.3mA		—	—	GND + 0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		YSCL, SHL, DI3, $\overline{\text{DSPOF}}$, FR, SEL	—	—	2.0	µA
I/O current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		DIO1, DIO2	—	—	5.0	µA
Rest current	I_{GND}	V_{DDH} = 14.0 to 42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{COM}	ΔVON = 0.5V Ta = 25°C	V_{DDH} = +36.0V, 1/24	O1 to O120	—	0.29	0.48	KΩ
			V_{DDH} = +26.0V, 1/20		—	0.3	0.5	
In-chip deviation	ΔR_{COM}	V_{DDH} = +36.0V, 1/24 bias			—	—	50	Ω
Mean operating current (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{YSCL} = 33.6KHz f_{FR} = 70Hz, input data: 1/480 Ta = 25°C, no load		V_{CC}	—	13	26	µA
		V_{CC} = 3.0V Other conditions are the same as when V_{CC} = 5.0V.			—	8	18	
Mean operating current (2)	I_{DDH}	V_{DDH} = V_0 = 30.0V, V_1 = 28.0V V_4 = 2.0V, V_5 = 0.0V, V_{CC} = 5.0V Other conditions are the same as those in the Icc column.		V_{DDHL} V_{DDHR}	—	8	20	µA
Input terminal capacity	C_I	Freq. = 1MHz Ta = 25°C Independent chips		YSCL, SHL, $\overline{\text{DSPOF}}$, FR, DI3, SEL	—	—	8	pF
I/O terminal capacity	$C_{I/O}$			DIO1, DIO2	—	—	15	pF

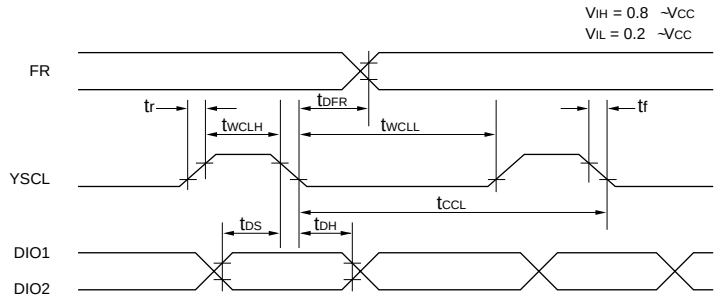
Operating voltage range V_{CC}–V_{DDH}

The V_{DDH} voltage must be selected within the following V_{CC} and V_{DDH} operating voltage range.



AC Characteristics

Input timing characteristics



(VCC = +5.0V ±10%, Ta = –40 to +85°C)

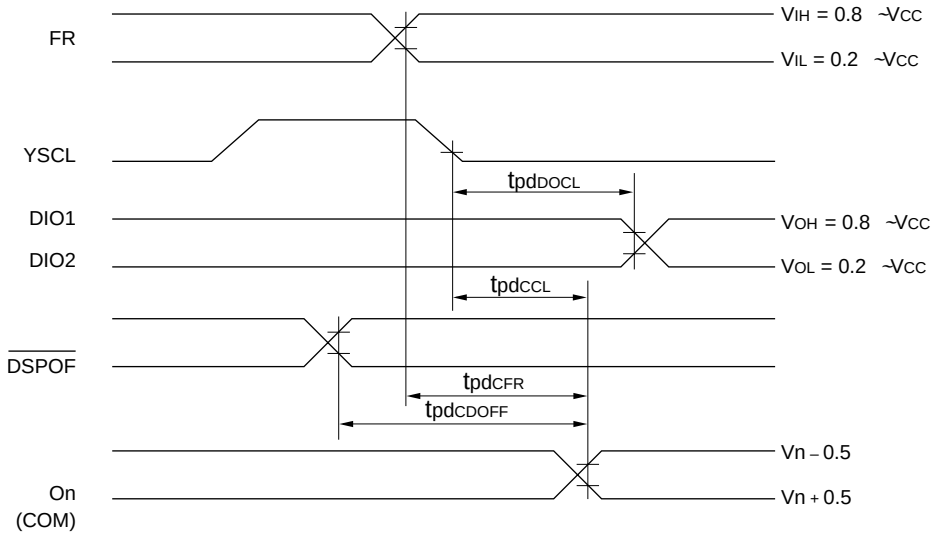
Items	Codes	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	400	—	ns
YSCL high-level pulse width	t_{WCLH}	—	60	—	ns
YSCL low-level pulse width	t_{WCLL}	—	330	—	ns
Data setup time	t_{DS}	—	50	—	ns
Data hold time	t_{DH}	—	40	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

(VCC = 2.7V to 4.5V, Ta = –40 to +85°C)

Items	Codes	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	800	—	ns
YSCL high-level pulse width	t_{WCLH}	—	80	—	ns
YSCL low-level pulse width	t_{WCLL}	—	660	—	ns
Data setup time	t_{DS}	—	90	—	ns
Data hold time	t_{DH}	—	70	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

*1: t_{DFR}: FR signal transition point and LP signal falling timing must be basically selected within the range in which normal On output waveform is produced at 0ns.

Output timing characteristics



(VCC = 5.0V ±10%, VDDH = 14.0 to 42.0V, Ta = –40 to +85°C)

Items	Symbols	Conditions	Min.	Max.	Units
YSCL falling edge → DIO delay time	t_{pdDOCL}	CL = 15pF	—	100	ns
YSCL falling edge → On output delay time	t_{pdCCL}	CL = 100pF	—	200	ns
$\overline{DSPOF}$ → On output delay time	$t_{pdCDOFF}$				
FR → On output delay time	t_{pdCFR}		—	300	ns

(VCC = 2.7V to 4.5V, VDDH = 14.0 to 28.0V, Ta = –40 to +85°C)

Items	Symbols	Conditions	Min.	Max.	Units
YSCL falling edge → DIO delay time	t_{pdDOCL}	CL = 15pF	—	200	ns
YSCL falling edge → On output delay time	t_{pdCCL}	CL = 100pF	—	400	ns
$\overline{DSPOF}$ → On output delay time	$t_{pdCDOFF}$				
FR → On output delay time	t_{pdCFR}		—	600	ns

LCD DRIVE POWER SUPPLY

Setting up respective voltage levels

When setting up respective voltage levels for LCD drive, it is the best way to resistively divide the potential between V_{DDH}–GND to drive the LCD by means of voltage follower using an operation amplifier.

In consideration of the case of using an operation amplifier, the LCD driving minimum potential V_0 and V_{DDH} are separated and independent terminals are used. Likewise, the LCD driving minimum potential V_5 and GND are separated and independent terminals are used.

Normally, V_0–V_{DDH} and V_5–GND are connected respectively, and V_1 and V_4 are driven by means of voltage follower. When driving V_0 by means of voltage follower, the potential difference between V_{DDH}–V_0 must be kept at 0V to 2.5V since efficacy of the LCD driving output driver deteriorates if V_0 potential goes beyond V_{DDH}.

When resistance exists in series in the power supply lines of GND and V_{DDH}, I_{DDH} at signal change causes voltage drop at GND and V_{DDH} of the supply terminals of the LSI disabling them to maintain current relations with the LCD intermediate potentials of ($V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq$ GND), thus leading to breakdown or destruction of the LSI.

When using a protective resistor, do not fail to stabilize the voltage using appropriate capacitance.

On stabilizing the voltage

For preventing an adverse effect due to noise introduced by the supply signal lines on the mounting board, it is recommended to insert bias capacitors, as needed, between power supplies (GND–V_{CC} and GND–V_{DDH}) to stabilize voltage.

Precautions for turning power on or off

Since the LCD drive voltage of these LSIs is high, it can be permanently damaged by excess current if high voltage is applied to the LCD drive circuit with the logic operation power being made floating or the Vccs lowered to 2.6V or less, or when LCD drive signals are output before applied voltage to the LCD drive circuit is stabilized. It is, therefore, suggested to maintain potential of the LCD drive output to V_5 level until the LCD drive circuit voltage is stabilized, using the display off function ($\overline{DSPOF}$).

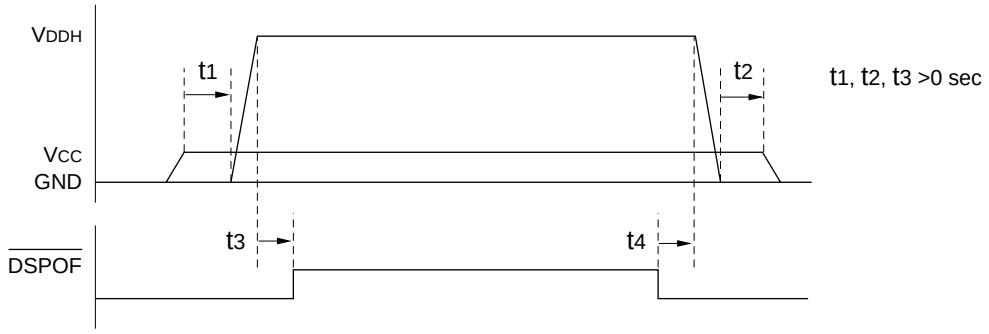
Maintain the following sequences when turning power on or off.

When turning power on:

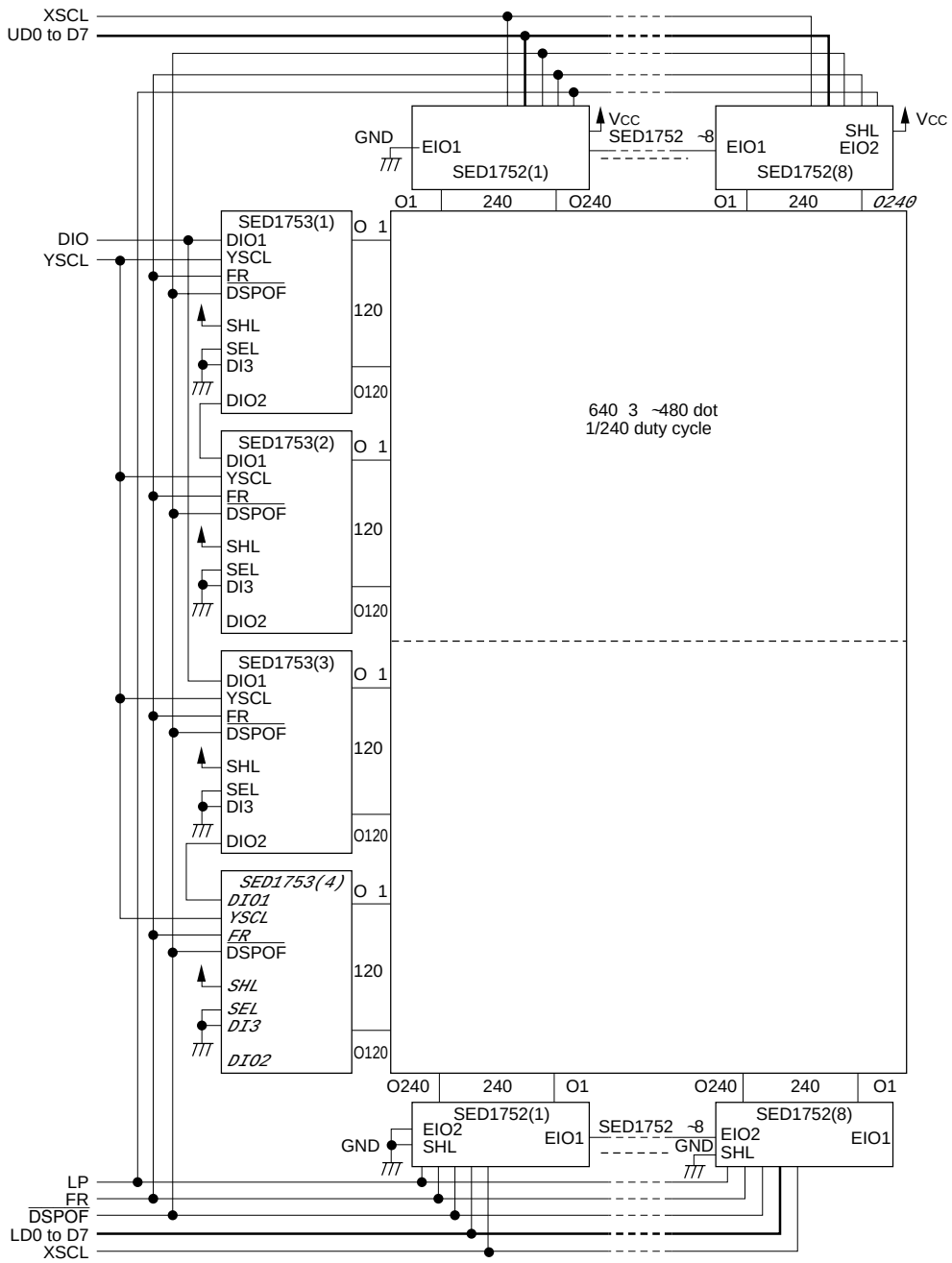
Turn on the logic operation power →
turn on the LCD drive power or turn them on simultaneously.

When turning power off:

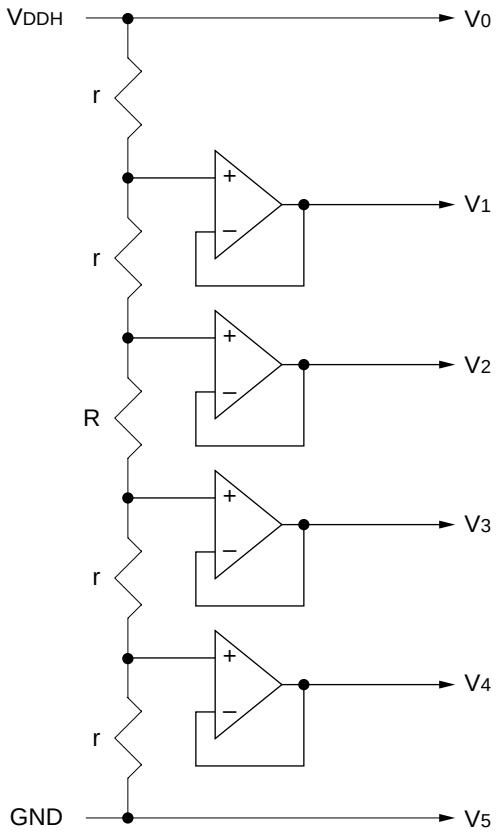
Turn off the LCD drive power →
turn off the logic operation power or turn them off simultaneously.



SAMPLE CIRCUIT



Sample LCD Power Supply Circuit

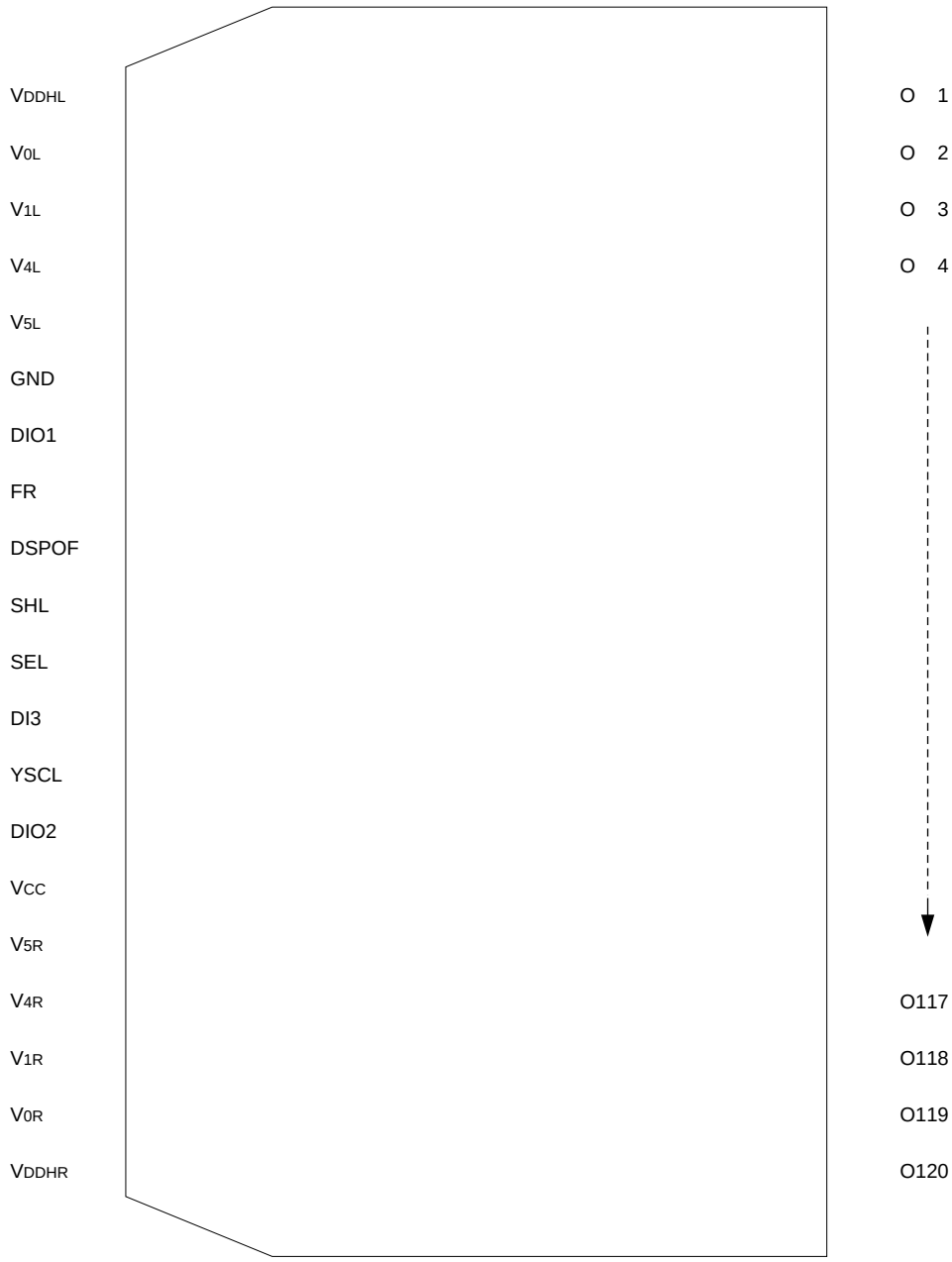


- Smoothing capacitance must be added to the LCD drive power supplies (V_0–V_5) at an appropriate location on the LCD module.
- V_0, V_1, V_4 and V_5 supply power to the SED1753 V_0, V_2, V_3 and V_5 supply power to the SED1752.
- Supplies logic operation voltage to respective ICs.
- For suppressing noise, bias capacitor must be added to an appropriate location between GND–V_{CC} and GND–V_{DDH} to stabilize the supply voltage.
  The high tension resistant supply (GNDR and GNDL) line must be be separated from the logic operation supply (GND) line.

TCP

A Sample SED1753T**TCP Pin Layout

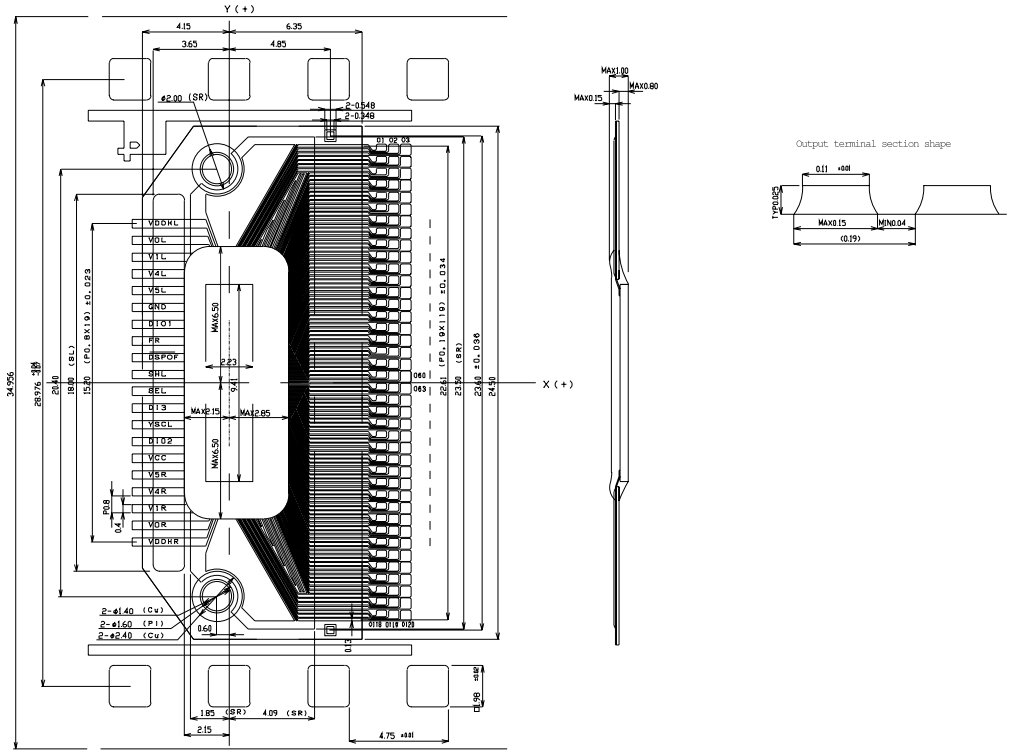
Note: This drawing is not meant to determine contour of the TCP.



DIMENSIONAL OUTLINE DRAWING

SED1753T0A

For reference



Unit: mm

8. SED1758
LCD Driver

Contents

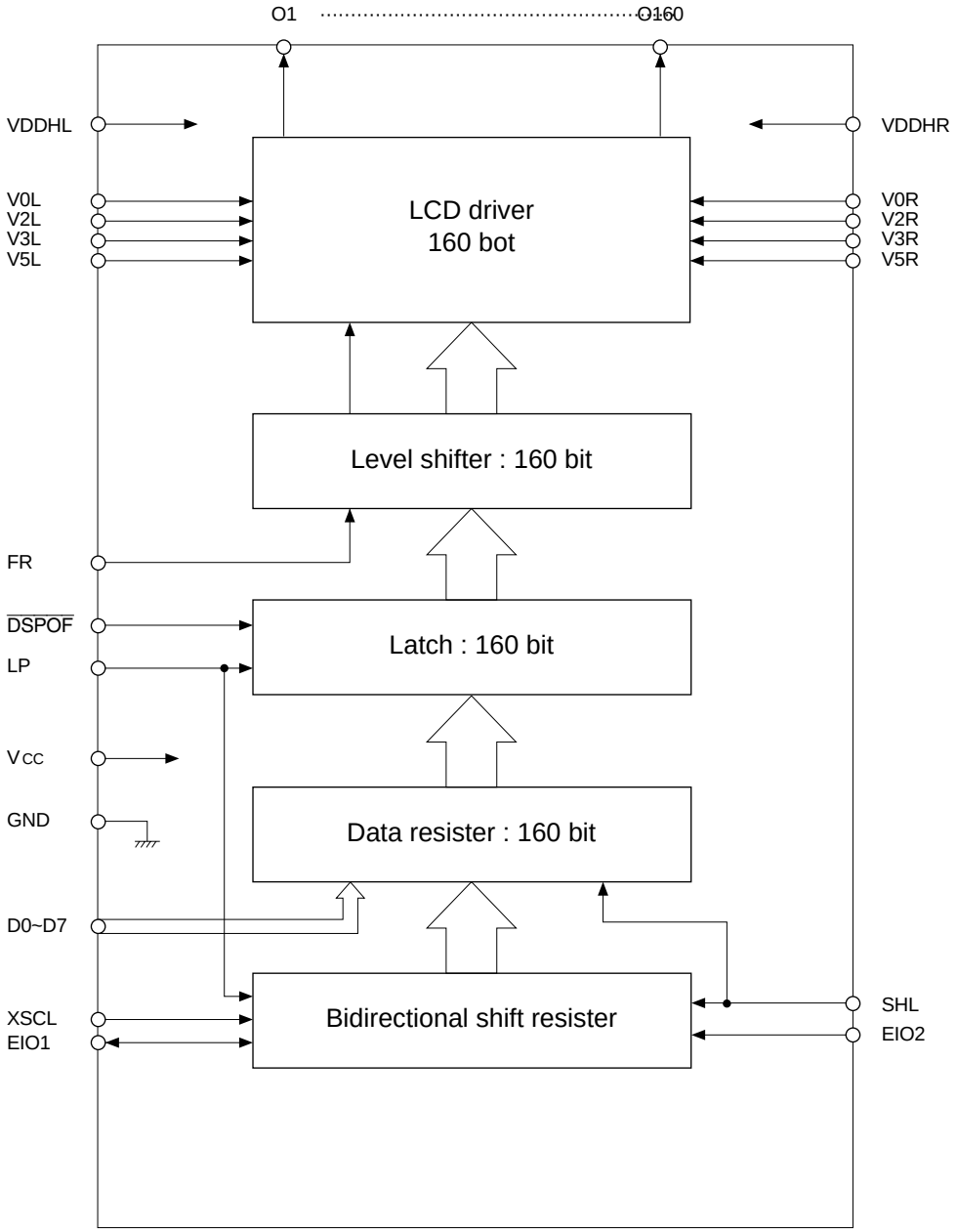
1. OUTLINE

SED1758 is a 160 output segment (column) LCD driver suitable for driving of colored STN dot-matrix LCD panels of a larger capacity, for use in combination with SED1743.
Contributing to making clearer LCD picture quality, this IC employs the high speed enable chain method and is slim-chip configuration which is more advantageous for miniaturization of the LCD panel. SED1758 is also capable of low-voltage and high-speed logic operations and fits to a wide range of applications.

2. FEATURES

- Number of LCD drive output segments: 160
- Low voltage operation: 2.7V min.
- High duty drive: 1/500 (an example)
- Wide LCD drive voltage range: + 8 to + 42V (V_{DD} = 3 to 5.5V)
- High speed and low power consumption data transfer is possible by adoption of the 8-bit bus enable chain method:
  Shift clock frequencies: 18.0 MHz (5V ±10%)
  10.0 MHz (2.7V)
- Slim-chip configuration
- Non-bias display off function
- Pin-selection of the output shift direction is available
- Offset bias regulation of LCD power for respective V_{DDH} and GND levels is possible
- Logic operation power supply: 2.7 ~ 5.5V
- Shipped status: TCP SED1758T**
- This IC is not radiation resistant

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Numbers of pins</th></tr>
<tr><td>O1~ O160</td><td>O</td><td>LCD driving segment (column) output.
The output varies at the falling edge of LP.</td><td>160</td></tr>
<tr><td>D0~D7</td><td>I</td><td>Display data input terminals</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>For input of the shift clock signals of the display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>For input of the latch pulse signals of the display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O.
Setting to I or O is determined by the SHL input level.
The output is reset by the LP input and when 160 bit equivalent data are received, it falls to “L” automatically.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO terminal I/O control signal input.
When data are input to terminals (D_0, D_1 .....D_7) in the order of (a_0, a_1 .....a_6 and a_7), (b_0.....b_6 and b_7) .....(t_0, t_1.....t_6 and t_7), the relations between the data and segment outputs become as follows:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><th>O1</th><th>O2</th><th>O3</th><th></th><th>O158</th><th>O159</th><th>O160</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a7</td><td>a6</td><td>a5</td><td>...</td><td>t2</td><td>t1</td><td>t0</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>t0</td><td>t1</td><td>t2</td><td>...</td><td>a5</td><td>a6</td><td>a7</td><td>Output</td><td>Input</td></tr>
</table>
(Note) The relations between the data and segment outputs are determined independent from the number of the shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>For input of alternating current LCD drive signals.</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power supply</td><td>Logic operation power supply: GND: 0V
V_{CC}: +3.3, +5V</td><td>2</td></tr>
<tr><td>V_{DDHL}, V_{DDHR}
V0L,V0R
V2L, V2R
V3L, V3R
V5L, V5R</td><td>Power supply</td><td>LCD drive power supply V_{DDH} — GND: 0V V_{DDH}:14~42V
" V_0 — $V_{DDH} \geq V_0 \geq V_2 \geq 7/9 V_0$
" V_2
" V_3 — 2/9 $V_0 \geq V_3 \geq V_5 \geq V_{SS}$
" V_5</td><td>10</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>For forced bias fixed input.
“L” level output is forcefully made to V_5 level.
* When using this function, combined use with SED1703 is not applicable.</td><td>1</td></tr>
<tr><td></td><td></td><td>Total</td><td>187</td></tr>
</table>

5. FUNCTION OF EACH BLOCK

5-1 Enable shift resister

The enable shift register is a bidirectional shift register of which the shift direction is being selected by the SHL input and the shift register output is used to store data bus signals into the data register.
When the enable signal is in disabled state, the internal clock signal and the data bus are fixed to "L", thus going into a power saving mode.
When using multiple number of segment drivers, make cascade connection of EIO terminals of respective drivers to connect the EIO terminal of the top driver to "GND". (Refer to Clause 10. Connection examples)
Since the enable control circuit automatically senses completion of receiving 160 bit equivalent data to transfer the enable signal automatically, control signal of a separate control LSI is not needed.

5-2 Data register

This register works to make series or parallel conversion of data bus signals according to the enable shift register output. Consequently, the relations between the serial display data and segment outputs are determined independent from the number of the shift clock inputs.

5-3 Latch

It takes in the content of the data register at the falling edge trigger to transfer the output to the level shifter.

5-4 Level shifter

This is a level interface circuit to convert the voltage level of signals from the logic operation level to LCD drive level.

5-5 LCD driver

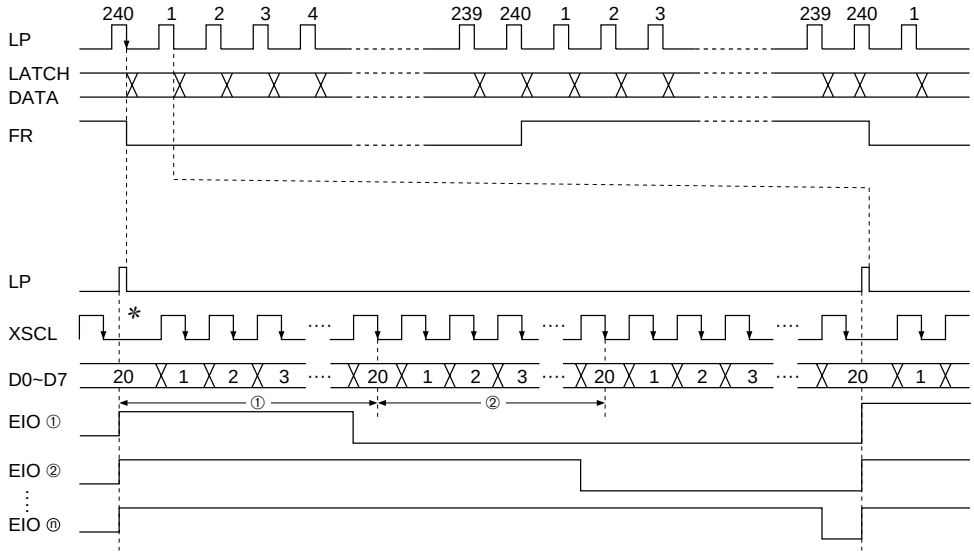
It outputs the LCD driving voltage.
Given below are the relations between data bus signals, alternating current signal FR levels and segment output voltages.

$\overline{\text{DSPOF}}$	Data bus signals	FR	Voltage outputs of the driver
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	–	–	V_5

5-6 Timing diagram

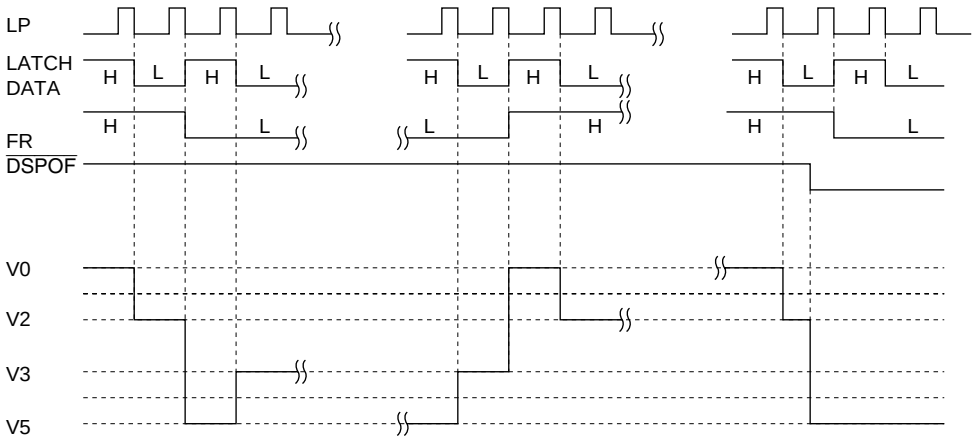
Timing diagram

In case of 1/240 Duty (an example)



① ~ ⓝ stands for the cascade numbers of the driver.

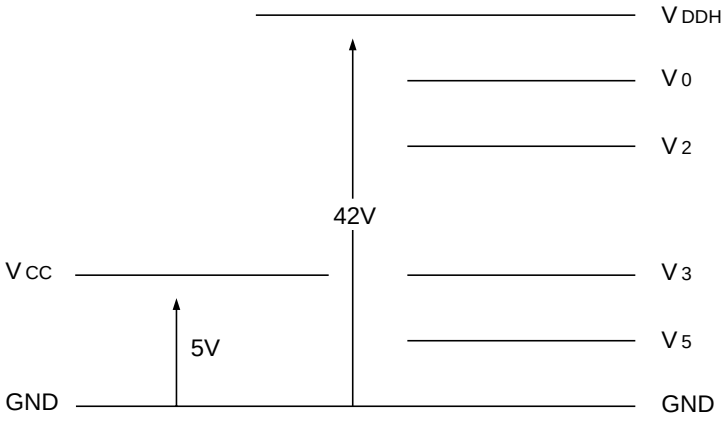
* When making high speed data transfer, it becomes necessary to secure a longer XSCL cycle when determining the LP pulse insertion timing in order to maintain the specified value of LP → XSCL (t_{LH}).



6. ABSOLUTE MAXIMUM RATINGS

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	–0.3 to V_{CC} + 0.3	V
Output voltage	V_O	–0.3 to V_{CC} + 0.3	V
EIO output current	I_{01}	20	mA
Working temperature	Topr	–30 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

(Note 1) All the voltage ratings are based on GND = 0V.
(Note 2) The storage temperature 1 is applicable to independent chips and the storage temperature 2 is applicable to the TCP modular state.
(Note 3) V_0, V_2, V_3 and V_5 should always be in the order of $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



(Note 4) If the logic operation power goes into a floating state or if V_{CC} drops to 2.6V or below while the LCD driving power is being applied, the LSI may be damaged. Therefore, keep from occurrence of the aforementioned status.
Specifically, pay close attention to the power supply sequence at times of turning the system power on and off.

7. ELECTRICAL CHARACTERISTICS

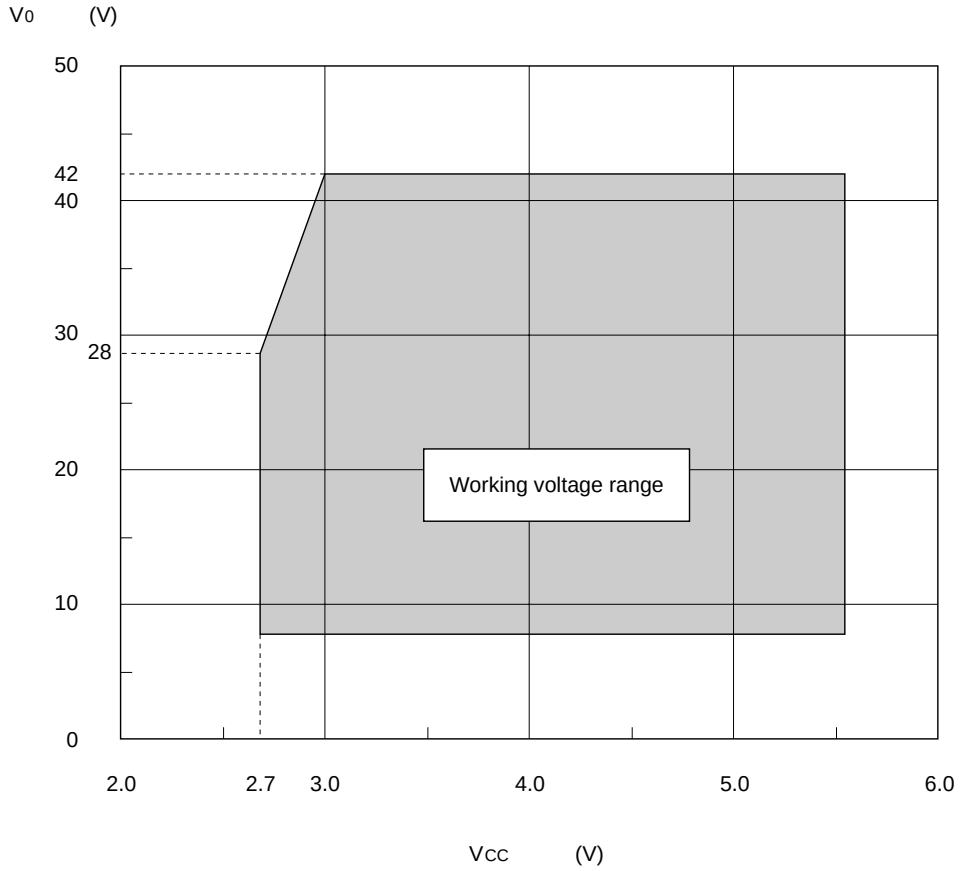
7-1 DC characteristics

Unless otherwise specified, GND = 0V, V_{CC} = +5.0 V ±10%, Ta = –30 to 85°C

Item	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}		V_{CC}	2.7		5.5	V
Recommended operating voltage	V_0		V0L,VDDHL	14.0		40.0	V
Operating voltage	V_0	Function only	V0R,VDDHL	8.0		42.0	V
Supply voltage (2)	V_2	Recommended value	V2L, V2R	7/9 V_0		V_0	V
Supply voltage (3)	V_3	Recommended value	V3L, V3R	GND		2/9 V_0	V
High level input voltage	V_{IH}	V_{DD} = 2.7 ~ 5.5V	EIO1,EIO2,FR D0~D7,XSCL SHL,LP,DSPOF	0.8V_{CC}			V
Low level input voltage	V_{IL}					0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC}= 2.7~5.5V, I_{OH} = –0.6mA	EIO1, EIO2	V_{CC}–0.4			V
Low level output voltage	V_{OL}	V_{CC}= 2.7~5.5V, I_{OL} = 0.6mA				0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	D0~D7,LP,FR XSCL, SHL DSPOF			2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}	EIO1, EIO2			5.0	µA
Rest current	I_{GND}	V_0 = 14.0~42.0V V_{IH} = V_{CC}, V_{IL}=GND	GND			25	µA
Output resistance	R_{SEG}	△V_{ON} =0.5V Recommended condition: V_0 =+36.0V, 1/24	O1~O160		0.85	2.6	KΩ
		△V_{ON} =0.5V Recommended condition: V_0 =+26.0V, 1/20			0.90	2.6	
In-chip deviation of output resistance	△R_{SEG}	△V_{ON}=0.5V V_0 = +36.0V, 1/24	O1~O160			90	Ω
Mean working current consumption (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, fXSCL = 5.38MHz fLP = 33.6kHz, fFR = 70Hz Input data: Checkered indication, no-load	V_{CC}		0.5	1.1	mA
		V_{CC} = +3.0V Other conditions are the same as those when V_{CC} = 5V.			0.2	0.6	
Mean working current consumption (2)	I_O	V_0 = +30.0V V_{CC} = +5.0V, V_3 = +4.0V V_2 = +26.0V, V_5 = +0.0V Other conditions are the same as those in the I_{DD} column.	V0L, V0R		0.15	0.9	mA
Input terminal capacity	C_I	Freq. = 1 MHz Ta = 25°C Independent chips	D0~D7, LP, FR, XSCL, SHL, DSPOF			8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2			15	pF

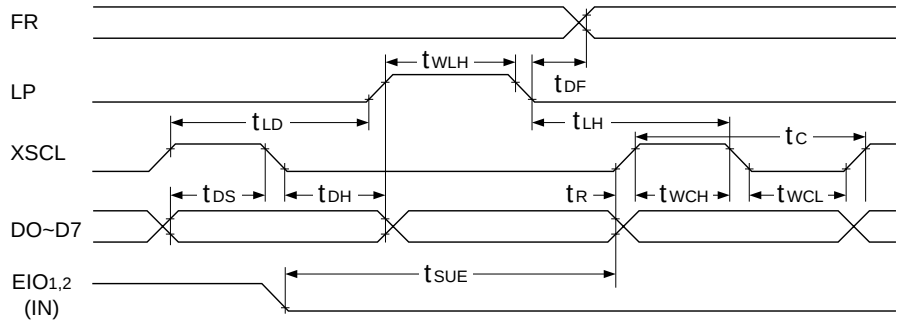
Working voltage range VCC - V0

The V0 voltage should be set up within the VCC - V0 working voltage range given below.



7-2 AC characteristics

Input timing characteristics



V_{CC} = 5.0V ±10%, Ta = –30 to 85°C

Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	tc	tr, tf≤11ns *3	62		ns
XSCL high level pulse duration	tWCH		20		ns
XSCL low level pulse duration	tWCL		20		ns
Data setup time	tDS		10		ns
Data hold time	tDH		10		ns
XSCL → LP rise time	tLD		–5		ns
LP → XSCL fall time	tLH		30		ns
LP high level pulse duration	tWLH	*1	40		ns
		*2	35		ns
FR delay allowance	tDF		–300	+300	ns
EIO setup time	tSUE		30		ns
Input signal variation time	tr, tf	*4		50	ns

V_{CC} = 2.7V to 4.5V, Ta = –30 to 85°C

Items	Symbol	Conditions	Min.	Max.	Units
XSCL cycle	tc	tr, tf≤15ns *3	100		ns
XSCL high level pulse duration	tWCH		35		ns
XSCL low level pulse duration	tWCL		35		ns
Data setup time	tDS		15		ns
Data hold time	tDH		10		ns
XSCL → LP rise time	tLD		–10		ns
LP → XSCL fall time	tLH		60		ns
LP high level pulse duration	tWLH	*1	75		ns
		*2	65		ns
FR delay allowance	tDF		–300	+300	ns
EIO setup time	tSUE		40		ns
Input signal variation time	tr, tf	*4		50	ns

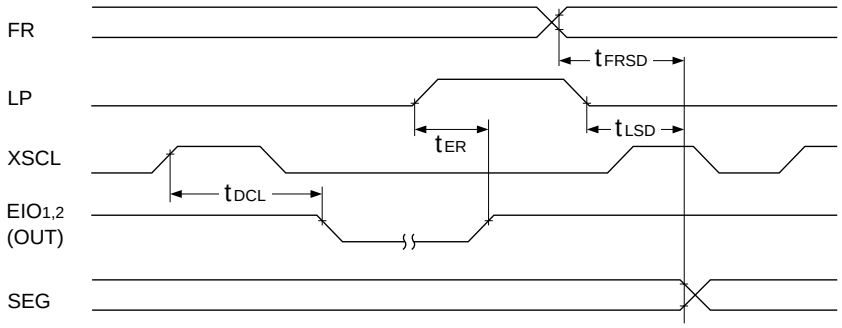
Notes: *1 The "t_{WLH}" specifies the time when the LP is at "H" and, at the same time, when XSCL is at "L", when LP is being input while the XSCL is at "L".

* 2 The "t_{WLH}" (its definition is same as *1) when LP rises while XSCL is at "H".

* 3 High speed operation of the shift clocks (XSCL) should only be made under a condition of $t_r + t_f \leq (t_C - t_{WCL} - t_{WCH})$.

* 4 When making high speed data transfer using continuous shift clocks, $t_r + t_f$ of the LP signals should be upto $(t_C + t_{WCH} - t_{LD} - t_{WLH} - t_{LH})$ at the maximum.

Output timing characteristics



V_{CC} = +5.0V ±10%, V_0 = +14.0 to +42.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EIO)		120	ns
EIO output delay time	t_{DCL}			55	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (O n)		200	ns
FR → SEG output delay time	t_{FRSD}			400	ns

V_{CC} = +2.7V to 4.5V, V_0 = +14.0 to +28.0V

Items	Symbol	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15 pF (EIO)		240	ns
EIO output delay time	t_{DCL}			85	ns
LP → SEG output delay time	t_{LSD}	C_L = 100 pF (O n)		400	ns
FR → SEG output delay time	t_{FRSD}			800	ns

8. LCD DRIVING POWER SUPPLY

8-1 Setting up respective voltage levels

When setting up respective voltage levels for LCD drive, it is the best way to resistively divide the potential between V_0 - GND to drive the LCD by means of voltage follower using an operation amplifier.
In consideration of the case of using an operation amplifier, the LCD driving minimum potential level V5 and GND are separated and independent terminals are used.
However, since the efficacy of the LCD driving output driver deteriorates when the potential of V_5 goes up beyond the GND potential to enlarge the potential difference, always keep the potential difference of V_5 - V_{SS} at 0V to 2.5V.
When a resistance exists in series in the power supply line of V_0 (GND), Io at signal changes causes voltage drop at V_0 (GND) of the supply terminals of the LSI disabling it to maintain the relations of the LCD with intermediate potentials of ($V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND), thus leading to breakdown or destruction of the LSI.
When using a protective resistor, do not fail to stabilize the voltage using an appropriate capacitance.

8-2 Precautions when turning the power on and off

Since the LCD drive voltage of these LSIs is comparatively high, if a high voltage of 30V or more is applied to the LCD drive circuit with the logic operation power made floating or with the V_{CC} lowered to 2.6V or less, or when LCD drive signals are output before applied voltage to the LCD drive circuits is stabilized, excess current flows through to possibly lead to breakdown or to destroy the LSI.
It is therefore suggested to maintain the potential of the LCD drive output to V_5 level until the LCD drive circuit voltage is stabilized, using the display off function ($\overline{DSPOF}$).
Maintain the following sequences when turning the power on and off:

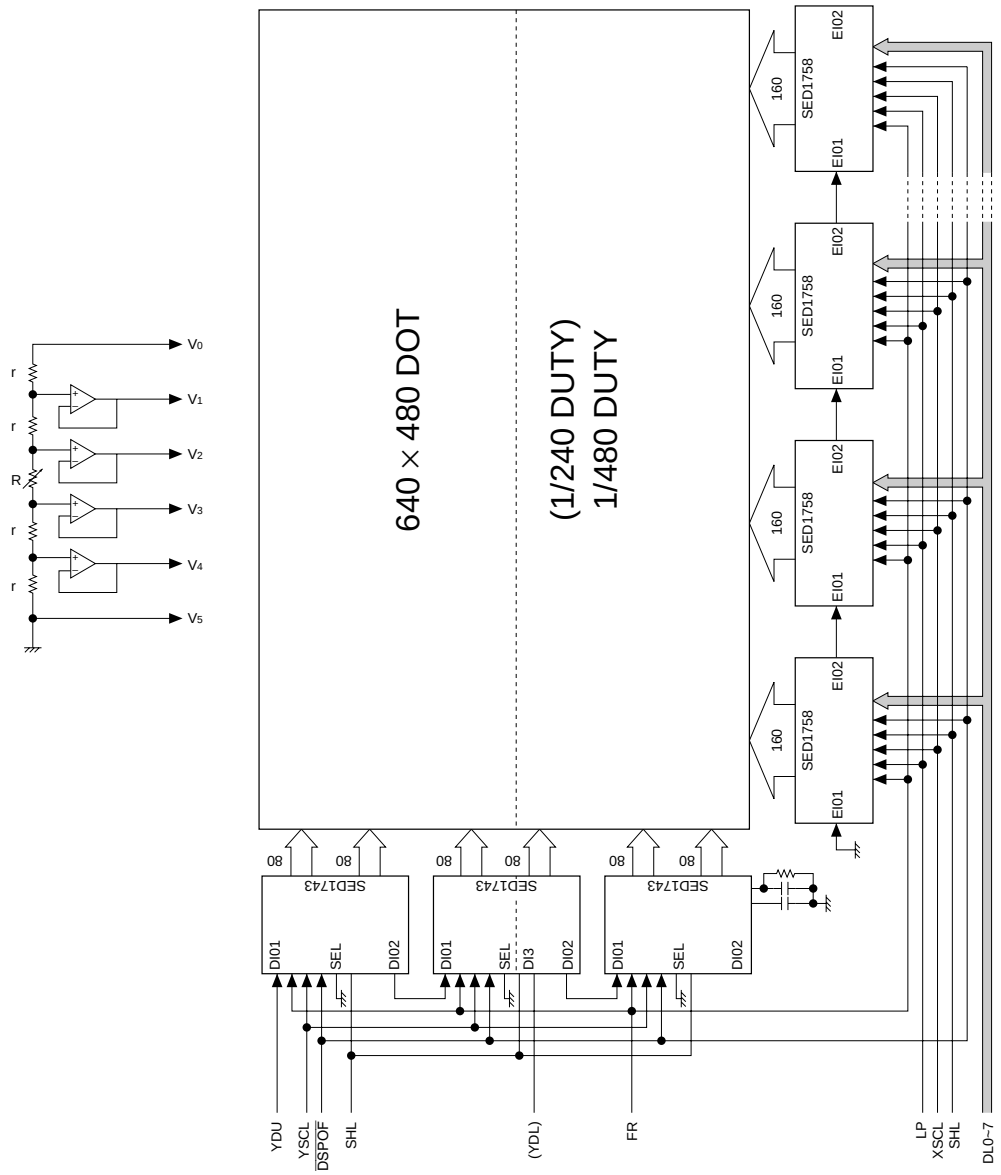
When turning the power on: Turn on the logic operation power → turn on the LCD drive power or turn them on simultaneously.

When turning the power off: Turn off the LCD drive power → turn off the logic operation power or turn them off simultaneously.

For protection against excess current, insert a quick melting fuse in series in the LCD drive power line.
When using a protective resistor, select the optimum resistance value depending on the capacitance of the LCD cells.

9. A CONNECTION EXAMPLE

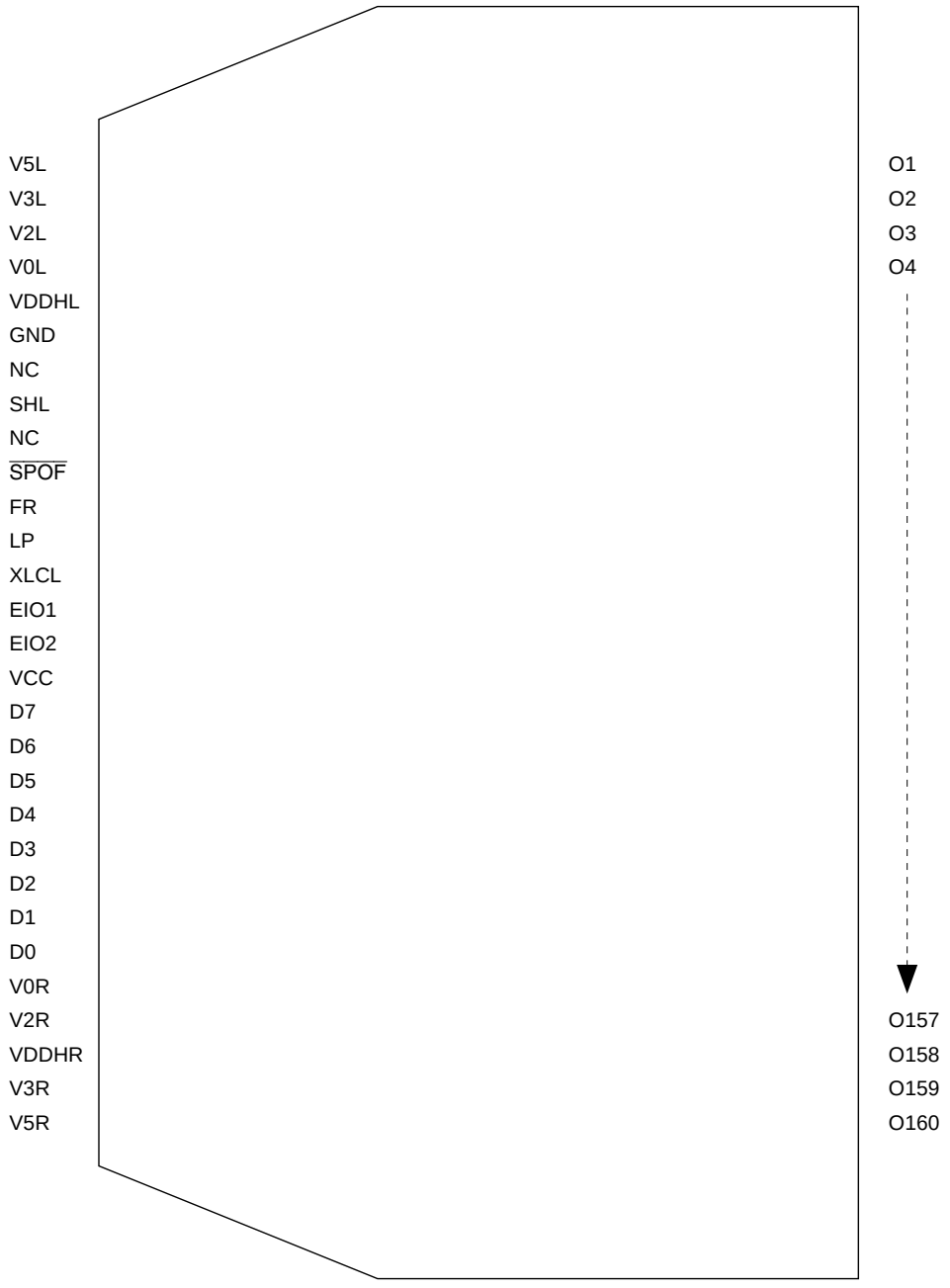
Block diagram of a large-plane LCD



For reference

10. SED1758T TCP PIN ARRANGEMENT EXAMPLE

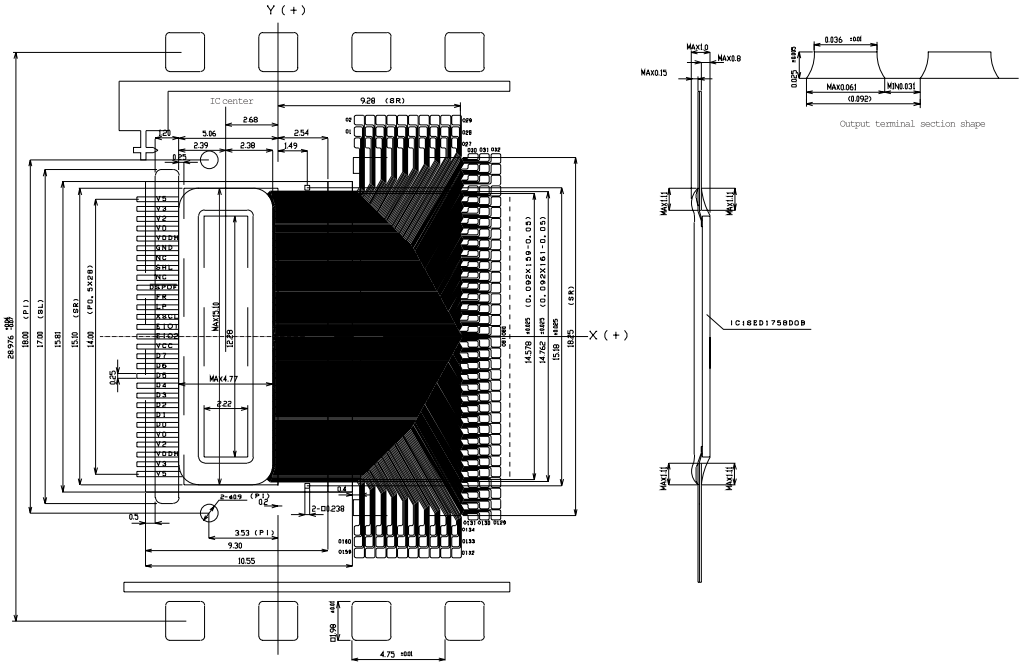
Remark: This drawing is not meant to determine the contour of the TCP.



11. DIMENSIONAL OUTLINE DRAWING

SED1758T0A

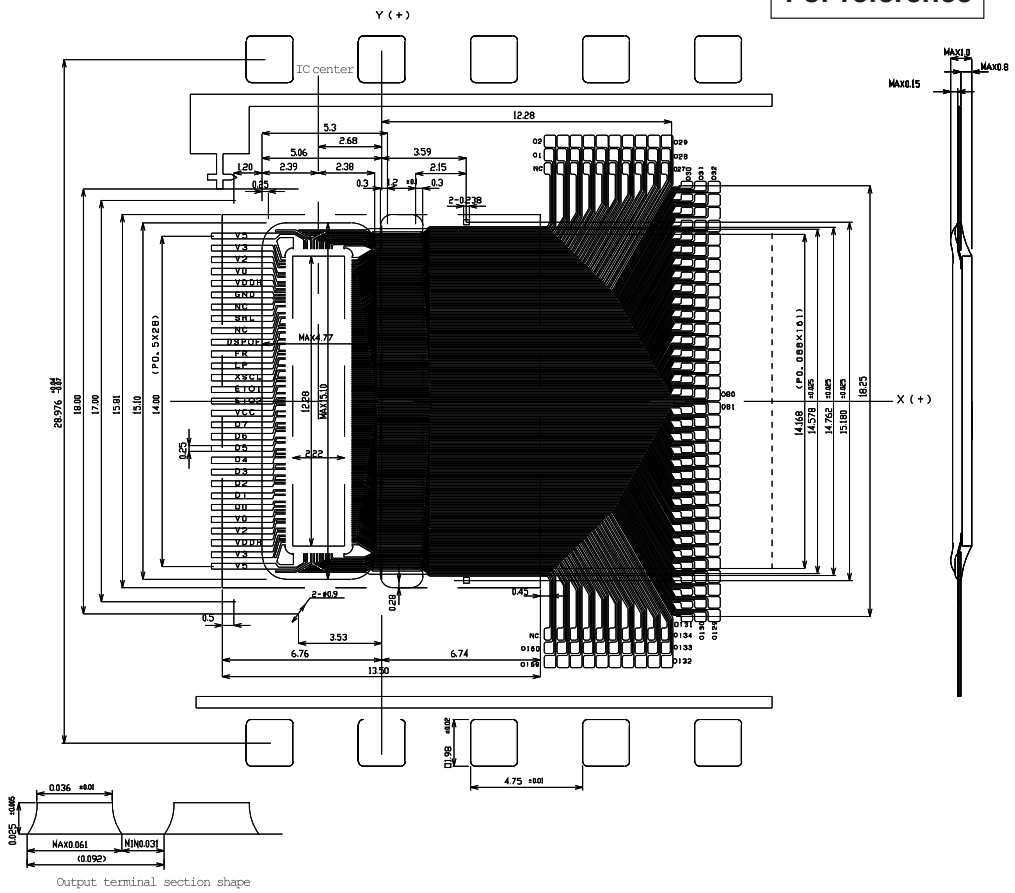
For reference



Unit: mm

SED1758T0B

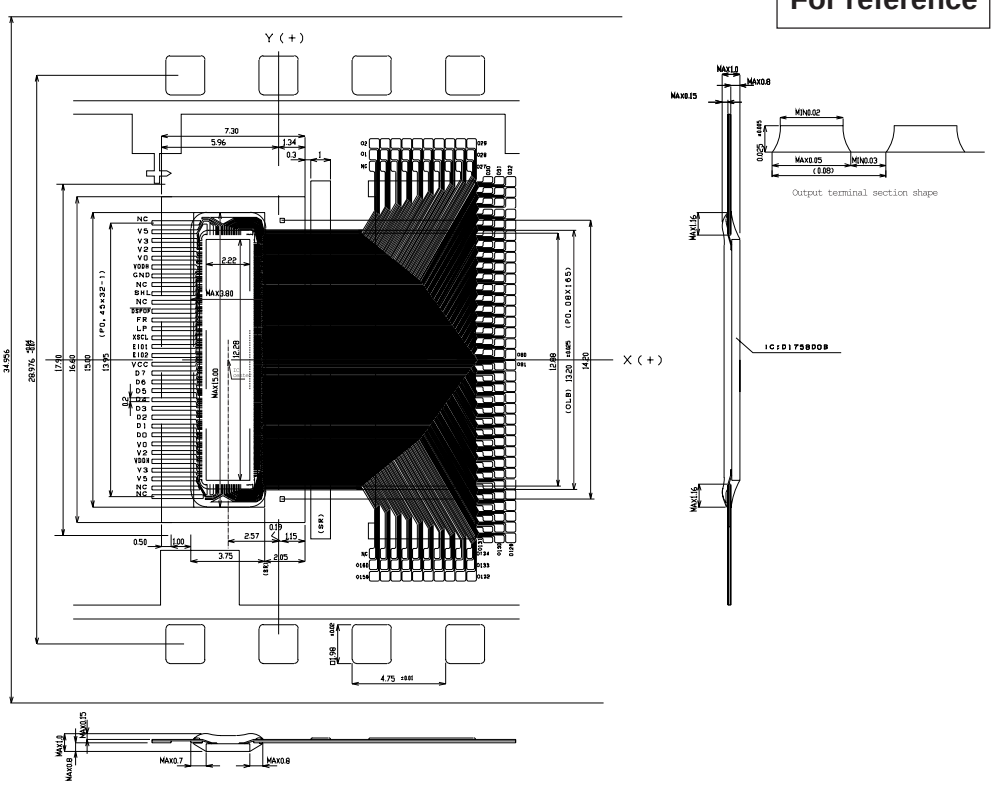
For reference



Unit: mm

SED1758T0G

For reference



Unit: mm

9. SED17A2
LCD Segment Driver

Contents

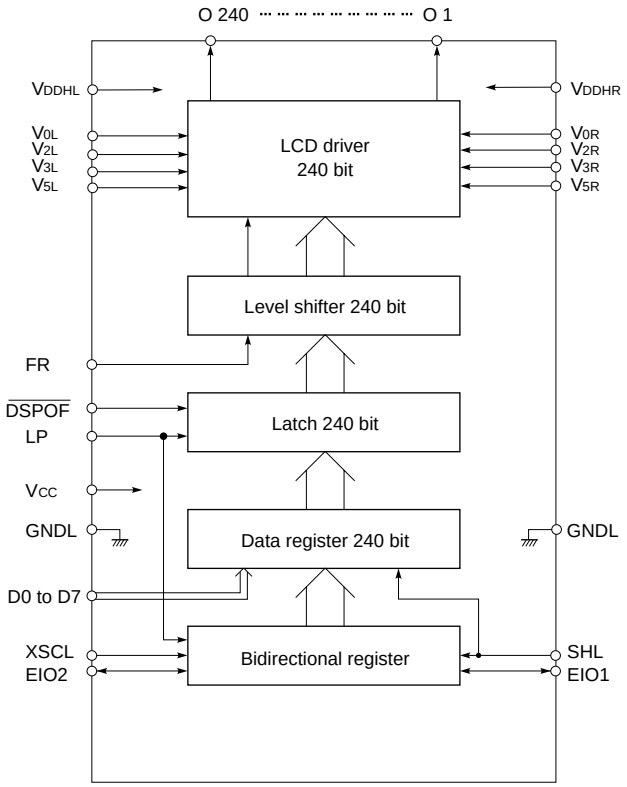
1. OVERVIEW

SED17A2T is a 240-output segment (column) driver suited for large capacity, color STN dot matrix liquid crystal panels. It is used paired with the SED1753.
It is designed for high resolution LCD display, employs high speed enable chain technique for achieving low-power and equips with long type chip layout suited for smaller LCD panels. SED17A2T's low voltage, high speed logic operation capability offers it a wide range of applications.

2. FEATURES

- LCD drive outputs: 240
- Lower operating voltage: 2.7V minimum
- Applicable to high duty drive: 1/500 (for reference)
- Wide LCD drive voltage range:
  +8V to +42V (V_{CC} = 3 to 5.5V)
- High speed and low-power data transfer supported by the 8 bit bus, enable chain approach
  Shift clock frequency …30.0MHz (5V±10%)
  …20.0MHz (3.0V)
  …18.0MHz (2.7V)
- Slimmer chip shape
- Non-bias display off function
- Pin selectable output shift direction
- LCD power bias is offset adjustable according to V_{DDH} or GND level
- Logic operation power: 2.7V to 5.5V
- Package : TCP … SED17A2T**
- This IC is not designed for radiation and light protection

3. BLOCK DIAGRAM



4. BLOCK FUNCTIONS

Enable register

Enable register is a bidirectional register which allows direction select by the SHL input. The shift register output is used for storing the data bus signal to the data register.
As long as the enable signal is disabled, the internal clock signal and data bus are fixed to low-level to introduce the power save mode to the system.
When multiple segment drivers are used, EIO terminals on respective drivers are cascade connected and EIO terminal on the first driver is connected to GND (see the connection example). The enable control circuit automatically detects the end of acquisition of 240 bit of data and transfers the enable signal automatically. Therefore, control signal from the control LSI is no more needed.

Data register

It is a register for converting the data bus signal to and from parallel and serial using the enable shift register output. Therefore, relations between serial display data and segment output is determined independent of number of shift clocks entered.

Latch

Acquires the data register contents at the LP falling edge trigger, then sends it to the level shifter.

Level shifter

A level interface circuit for converting voltage level of a signal from logic system level to LCD drive level.

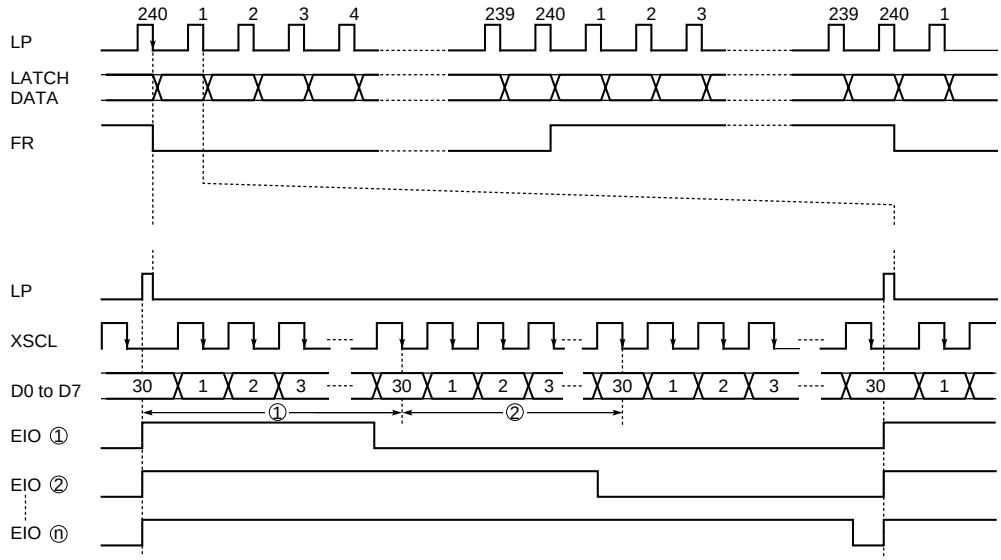
LCD driver

Outputs the LCD drive voltage.
The following table shows relations between data bus signal, frame signal FR and segment output voltage.

$\overline{\text{DSPOF}}$	Data bus signal	FR	Driver output voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_5

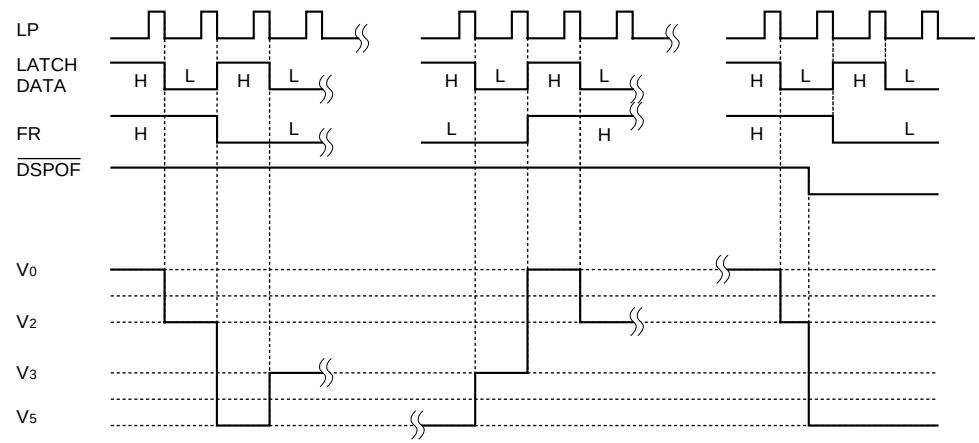
Timing Diagram

Timing Diagram
For 1/240 duty (For reference)



① and ⓝ represent the driver cascade number.

* In high speed data transfer, a longer XSCL cycle must be selected in the LP pulse insertion timing for satisfying the LP→XSCL (t_{LH}) requirement.



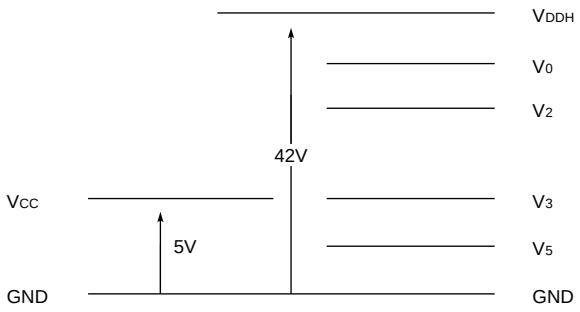
5. PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>No. of pins</th></tr>
<tr><td>O1 to O240</td><td>O</td><td>LCD drive segment (column) output. The output changes at the LP falling edge.</td><td>240</td></tr>
<tr><td>D0 to D3-7</td><td>I</td><td>Display data input</td><td>8</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch pulse input (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable input or output.
It is set to either input or output depending on the SHL input level. The output is reset as the LP is entered and automatically shifted to low-level as 160 bit of data has been acquired.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and EIO pin I/0 control signal input. The following shows the relation between data and segment output when data is entered to (D0 through D7) pins in the order of F0 through F7 being followed by L0 through and L7.
<table>
<tr><td>F (First), L (last)</td></tr>
</table>
<table>
<tr><td rowspan="2">SHL</td><td colspan="8">O (Output)</td><td colspan="2">EIO</td></tr>
<tr><td>O240</td><td>O239</td><td>O238</td><td></td><td>O3</td><td>O2</td><td>O1</td><td>EIO1</td><td>EIO2</td></tr>
<tr><td>L</td><td>F7</td><td>F6</td><td>F5</td><td>•••</td><td>L2</td><td>L1</td><td>L0</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>L0</td><td>L1</td><td>L2</td><td>•••</td><td>F5</td><td>F6</td><td>F7</td><td>Input</td><td>Output</td></tr>
</table>
Note: Relation between data and segment output is determined independent of number of shift locks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output frame signal input.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL
GNDR</td><td>Power supply</td><td>Logic operation power GND : 0V V_{CC}: +3.3V, +5V</td><td>3</td></tr>
<tr><td>V_{DDHL}, V_{0L}
V_{2L}, V_{3L},V_{5L},
V_{DDHR}, V_{0R},
V_{2R}, V_{3R}, V_{5R}</td><td>Power supply</td><td>LCD drive circuit power GND : 0V V_{DDH}: +14 to +42V
$V_{DDH} \geq V_0 \geq V_2 \geq 7/9V_0$
$2/9V_0 \geq V_3 \geq V_5 \geq$ GND</td><td>10</td></tr>
<tr><td>$\overline{DSPOF}$</td><td>I</td><td>Forced bias fixed input.
At low-level, it forces the output to V_5 level.
* This function is not available when the SED17A2T is paired with the SED1703.</td><td>1</td></tr>
</table>

6. ABSOLUTE MAXIMUM RATING

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	GND –0.3 to V_{DDH} +0.3	V
Input voltage	T_I	GND –0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} +0.3	V
EIO output current	I_{OI}	20	mA
Operating temperature	T_{opr}	–30 to +85	°C
Storage temperature	T_{stg}	–55 to +100	°C

Note 1: GND = 0V is assumed for all voltages.
Note 2: Storage temperature assumes that TCP has been mounted.
Note 3: V_0, V_2, V_3 and V_5 voltage must always satisfy $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



Note 4: Do not allow the logic operation power goes to floating state or V_{CC} goes to 2.6V or less while LCD drive circuit power is applied. Otherwise, LSI can be permanently damaged. Special care is needed for the system power on or off sequences.

7. ELECTRIC CHARACTERISTICS

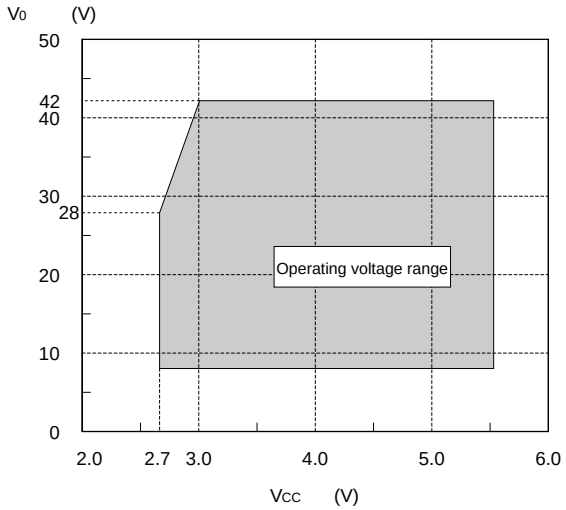
DC Characteristics

Except where otherwise specified, GND = V_5 = 0V, V_{CC} = +5.0V±10% and Ta= –30 to 85°C are assumed.

Items	Codes	Conditions		Min.	Typ.	Max.	Units	Applicable pins
Supply voltage (1)	V_{CC}			2.7	—	5.5	V	V_{CC}
Recommended operating voltage	V_0			14.0	—	40.0	V	V_{0L}, V_{DDHL}
Operatable voltage	V_0	Function		8.0	—	42.0	V	V_{0R}, V_{DDHL}
Supply voltage (2)	V_2	Recommended value		7/9V_0	—	V_0	V	V_{2L}, V_{2R}
Supply voltage (3)	V_3	Recommended value		GND	—	2/9V_0	V	V_{3L},V_{3R}
High level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		0.8V_{CC}	—	—	V	EIO1, EIO2, FR D0 to D7, XSCL SHL, LP, $\overline{DSPOF}$
Low level input voltage	V_{IL}			—	—	0.2V_{CC}	V	
High level output voltage	V_{OH}	V_{CC} =	I_{OH} = – 0.6mA	V_{CC} – 0.4	—	—	V	EIO1, EIO2
Low level output voltage	V_{OL}	2.7 to 5.5V	I_{OH} = 0.6mA	—	—	0.4	V	
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		—	—	2.0	µA	D0 to D7, LP, FR XSCL, SHL, $\overline{DSPOF}$
I/O leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		—	—	5.0	µA	EIO1, EIO2
Rest current	I_{GND}	V_0 = 14.0 to 42.0V V_{IH} = V_{CC}, V_{IL} = GND		—	—	25	µA	GND
Output resistance	R_{SEG}	ΔVON = 0.5V	V_0 = +36.0V, 1/24	—	0.80	1.1	kΩ	O0 to
		Recommended condition	V_0 = +26.0V, 1/20	—	0.85	1.2	—	O240
Output resistance in-chip deviation	ΔR_{SEG}	ΔVON = 0.5 V_0 = +36.0V, 1/24		—	—	95	Ω	O1 to O240
Mean operating current (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{XSCL} = 5.38MHz f_{LP} = 33.6KHz, f_{FR} = 70Hz Input data: Check display, no load		—	0.75	1.7	mA	V_{CC}
		V_{CC} = +3.0V Other conditions are the same as when Vcc = 5V		—	0.3	0.9		
Mean operating current (2)	I_0	V_0 = + 30.0V V_{CC} = +5.0V, V_3 = +4.0V V_2 = +26.0V, V_5 = 0.0V Other conditions are the same as shown in the I_{CC} column		—	0.25	1.4	mA	V_0
Input terminal capacity	C_I	Freq. 1MHz Ta = 25°C		—	—	8	pF	D0 to D7, LP, FR XSCL, SHL, $\overline{DSPOF}$
I/O terminal capacity	$C_{I/O}$	Independent chips		—	—	15	pF	EIO1, EIO2

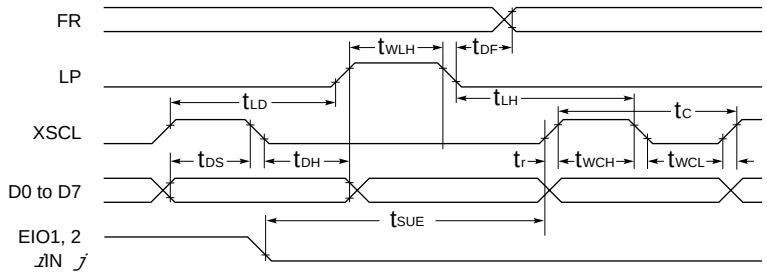
Operating Voltage Range V_{CC}-V_0

V_0 voltage must be selected within the V_{CC}-V_0 operating voltage range as shown below.



AC Characteristics

Input Timing Characteristics



(VCC = +5.0V±10%, Ta = –30 to 85°C)

Items	Codes	Conditions	Min.	Max.	Units
XSCL cycle	t_C	*2	33	—	ns
XSCL high-level pulse width	t_{WCH}		9	—	ns
XSCL low-level pulse width	t_{WCL}	20% and 80% of V_{CC}	9	—	ns
Data setup time	t_{DS}	are assumed for all	5	—	ns
Data hold time	t_{DH}	timing.	5	—	ns
XSCL→LP rise time	t_{LD}		–0	—	ns
LP→XSCLE fall time	t_{LH}		25	—	ns
LP high-level pulse width	t_{WLH}	*1	15	—	ns
Allowable FR delay time	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		5	—	ns
Input signal change time	t_{r1}, t_{f1}	*3	—	50	ns
DSPOF signal change time	t_{r2}, t_{f2}		—	100	ns

(VCC = +2.7V to 4.5V, Ta = –30 to 85°C)

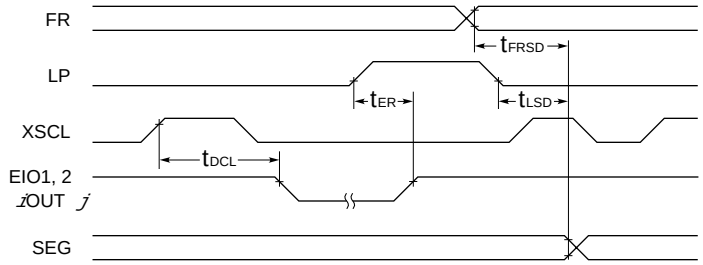
Items	Codes	Conditions	Min.	Max.	Units
XSCL cycle	t_C	VCC = 3.0 to 4.5V	50	—	ns
		*2	55	—	ns
XSCL high-level pulse width	t_{WCH}		15	—	ns
XSCL low-level pulse width	t_{WCL}	20% and 80% of V_{CC}	15	—	ns
Data setup time	t_{DS}	are assumed for all	10	—	ns
Data hold time	t_{DH}	timing.	10	—	ns
XSCL→LP rise time	t_{LD}		–0	—	ns
LP→XSCLE fall time	t_{LH}		30	—	ns
LP high-level pulse width	t_{WLH}	*1	25	—	ns
Allowable FR delay time	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		10	—	ns
Input signal change time	t_{r1}, t_{f1}	*3	—	50	ns
DSPOF signal change time	t_{r2}, t_{f2}		—	100	ns

*1: t_{WLH} regulates high-level period of LP and low-level period of XSCL if LP is entered while XSCL is at low-level.

*2: High speed shift clock (XSCL) operation is regulated by the condition $t_r+t_f \le (t_C-t_{WCL}-t_{WCH})$.

*3: When high speed data transfer is done with continuous shift clock, maximum of the LP signal t_r+t_f is $(t_C+t_{WCH}-t_{LD}-t_{WLH}-t_{LH})$.

Output Timing Characteristics



(V_{CC} = +5.0V±10%, V_0 = +14.0 to 42.0V)

Items	Codes	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	CL (EIO) = 15pF	—	50	ns
EIO output delay time	t_{DCL}		—	25	ns
LP→SEG output delay time	t_{LSD}	CL (On) = 100pF	—	200	ns
FR→SEG output delay time	t_{FRSD}		—	400	ns

(V_{CC} = +2.7V to 4.5V, V_0 = +14.0 to 28.0V)

Items	Codes	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	CL (EIO) = 15pF	—	80	ns
EIO output delay time	t_{DCL}		—	50	ns
LP→SEG output delay time	t_{LSD}	CL (On) = 100pF	—	400	ns
FR→SEG output delay time	t_{FRSD}		—	800	ns

8. LCD DRIVE POWER SUPPLY

Setting up different voltage levels

When setting up respective voltage levels for LCD drive, the best way would be to resistively divide the potential between V_0-GND by means of voltage follower using an operation amplifier. In consideration of the case of using an operation amplifier, the LCD driving minimum potential V_5 and GND are separated and independent terminals are used.

However, since efficacy of the LCD driving output driver deteriorates when the potential of V_5 goes up beyond the GND potential, the potential difference between V_5-GND must always be kept at 0V to 2.5V.

When a resistance exists in series in the V_0 (GND) power supply line, I0 at signal changes causes voltage drop at V_0 (GND) of the LSI supply terminals disabling it to maintain the relations with the LCD potentials of ($V_{DDH} = V_0 \geq V_2 \geq V_3 \geq V_5 \geq$ GND). This could result in permanent damage of the LSI.

When a protective resister is employed, the voltage must be stabilized using an appropriate capacitance.

Precautions for turning power on or off

Since the LCD drive voltage of these LSIs are high, if a voltage of 30V or above is applied to the LCD drive circuit when the logic operation power is floating, the V_{CC} is lowered to 2.6V or less or LCD drive signals are output before applied voltage to the LCD drive circuit is stabilized, excess current flows through possibly damaging the LSI.

It is therefore suggested to maintain the potential of the LCD drive to V_5 level until the LCD drive circuit power is stabilized. Use the display off function ($\overline{DSPOF}$) for this purpose.

Maintain the following sequences when turning power on or off.

When turning power on: Turn on the logic operation power → turn on the LCD drive power or turn them on simultaneously.

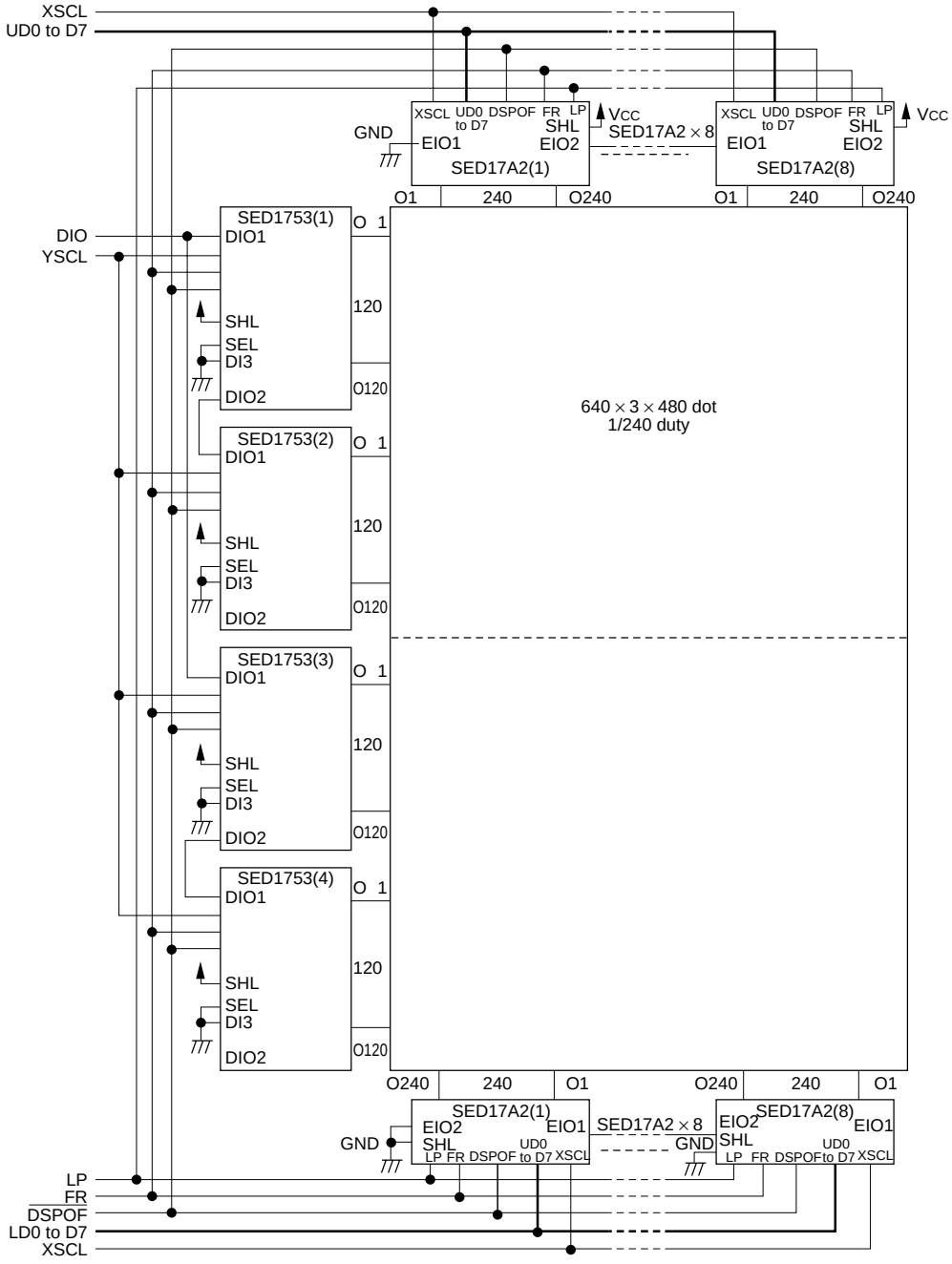
When turning power off: Turn off the LCD drive power → turn off the logic operation power or turn them off simultaneously.

As a protection against excess current, insert a quick melting fuse in series in the LCD drive power line.

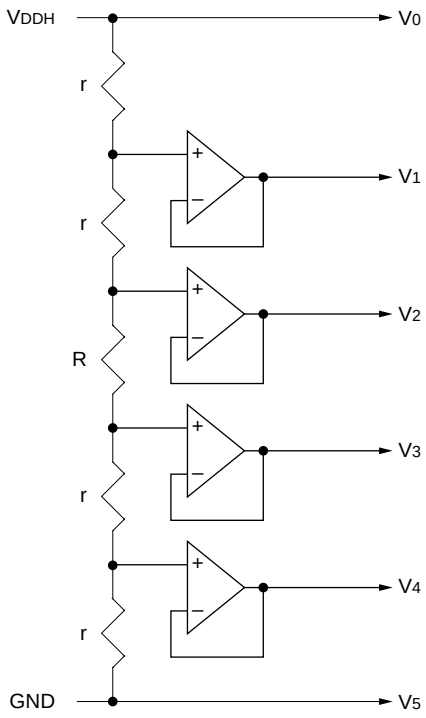
When using a protective resistor, an optimum resistance value must be selected considering the capacitance of the liquid crystal cells.

9. SAMPLE CIRCUIT

Large Screen LCD Structural Diagram



A Sample LCD Power Supply



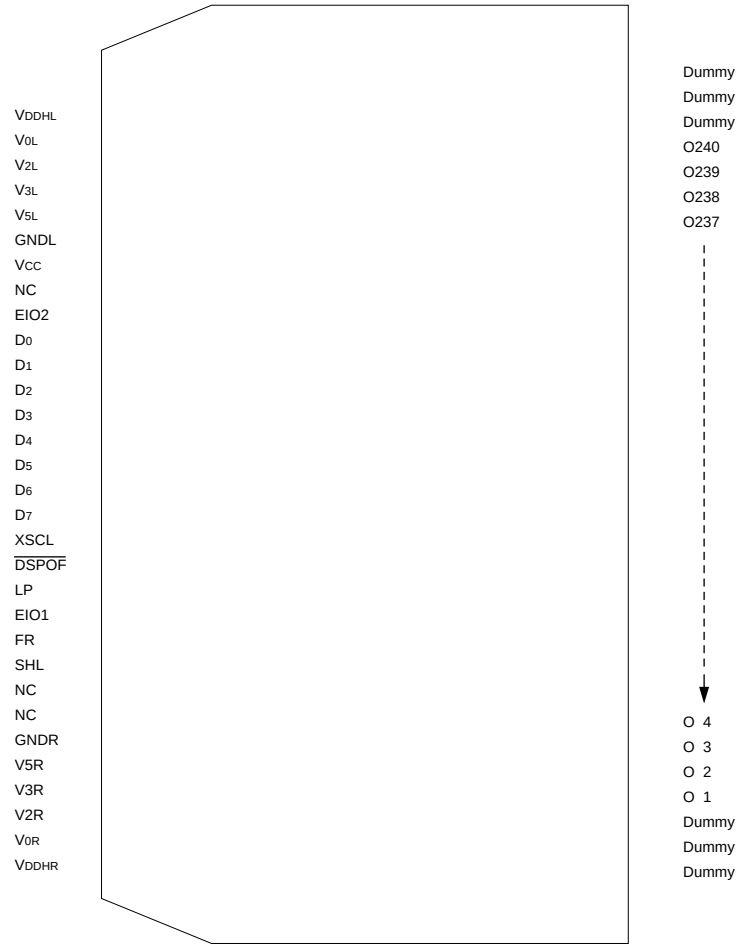
- Smoothing capacitance must be added to the LCD drive power (V_0-V_5) at an appropriate position on the LCD module.
- V_0, V_1, V_4 and V_5 supply power to the SED1753 and V_0, V_2, V_3 and V_5 are used supplying power to the SED17A2T.
- Supplies logic operation voltage to respective ICs.
- Bias capacitors must be installed to appropriate positions between GND-V_{CC} and GND-V_{DDH} for stabilizing voltage and, thus, to provide protection against noise.

  The high tension resistant power (GNDR, GNDL) line might as well be separated from that for the logic operation power (GND) line.

10. TCP

Sample SED17A2T** TCP Pin Layout

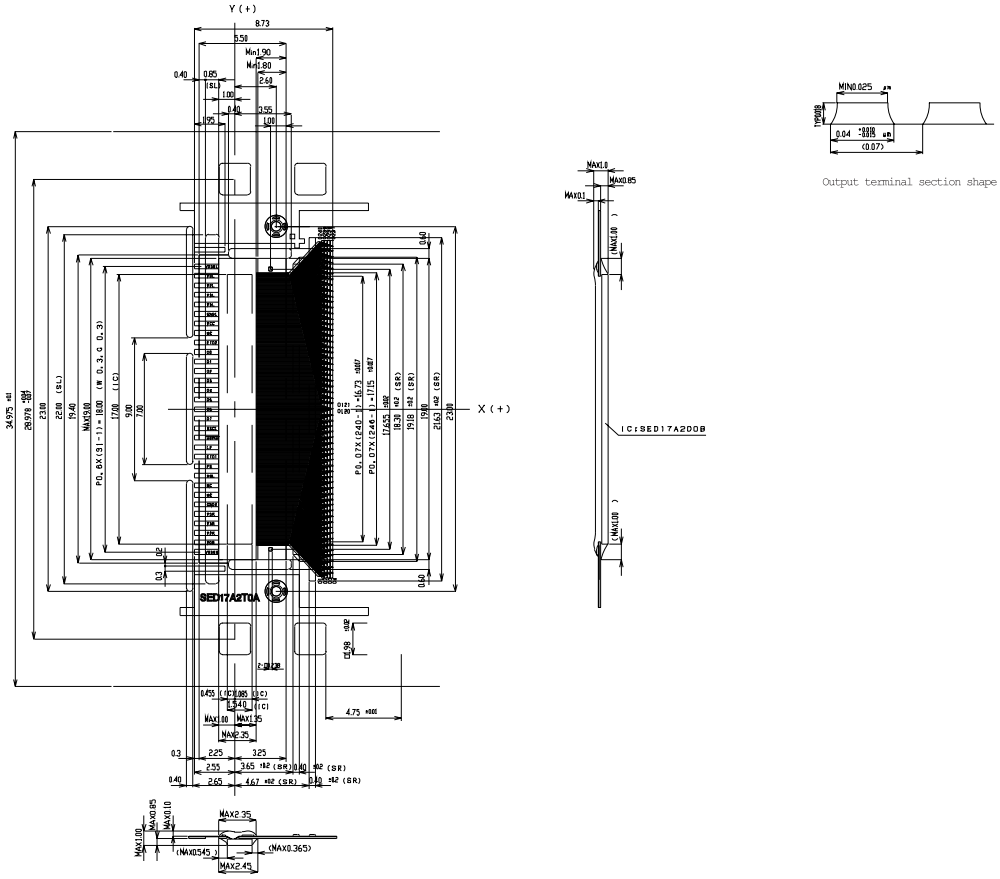
Note: It is not intended to regulate contour of TCP.



11. DIMENSIONAL OUTLINE DRAWING

SED17A2T0A

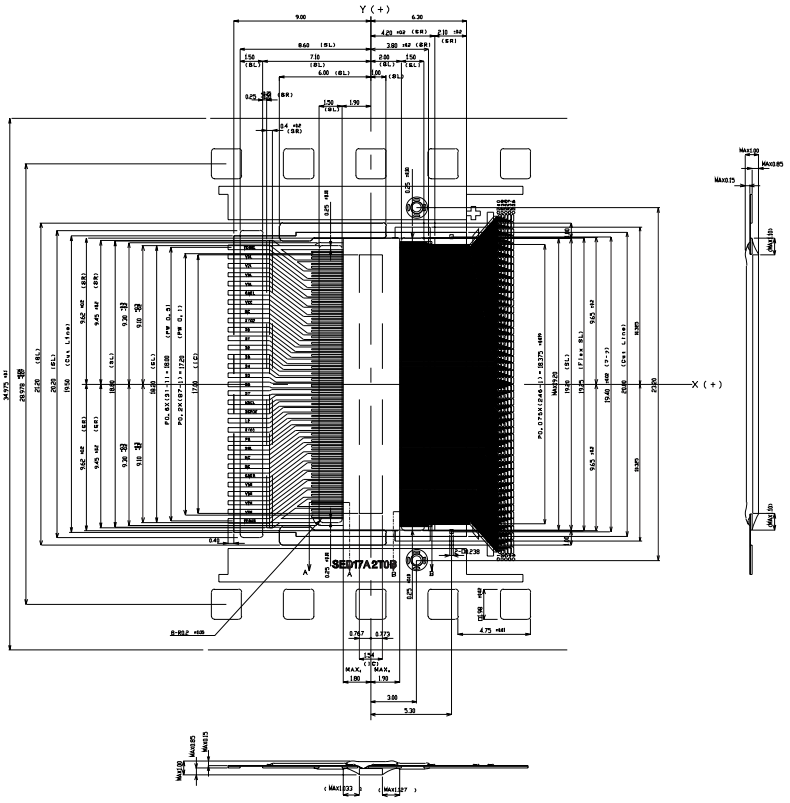
For reference

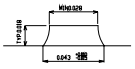


Unit: mm

SED17A2T0B

For reference



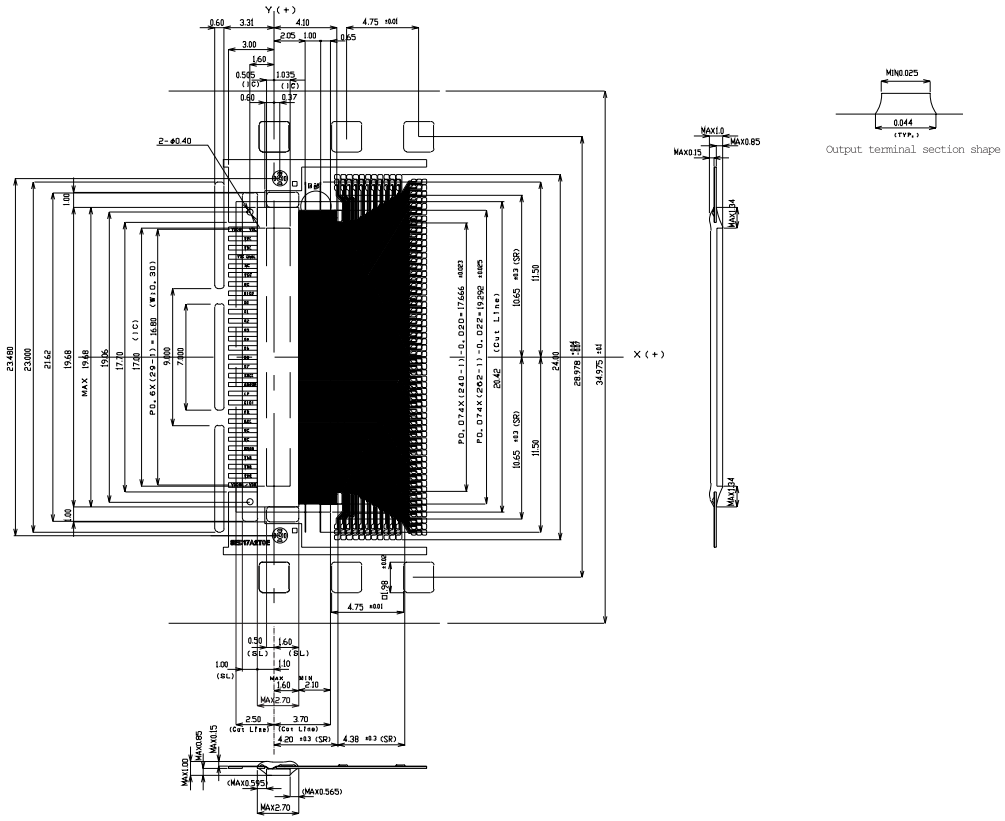


Output terminal section shape

Unit: mm

SED17A2T0E

For reference



Unit: mm

10. SED1765
LCD Segment Driver

Contents

SED1765 is designed for weighting the gray-scale utilizing the PWM (Pulse Width Modulation) technique. It enables gray-scale display on large size, dot matrix liquid crystal panels.
More than ever uniform gray-scale display on MIM liquid panels has been realized by maintaining the common impedance for the liquid crystal ON level potential at low level.

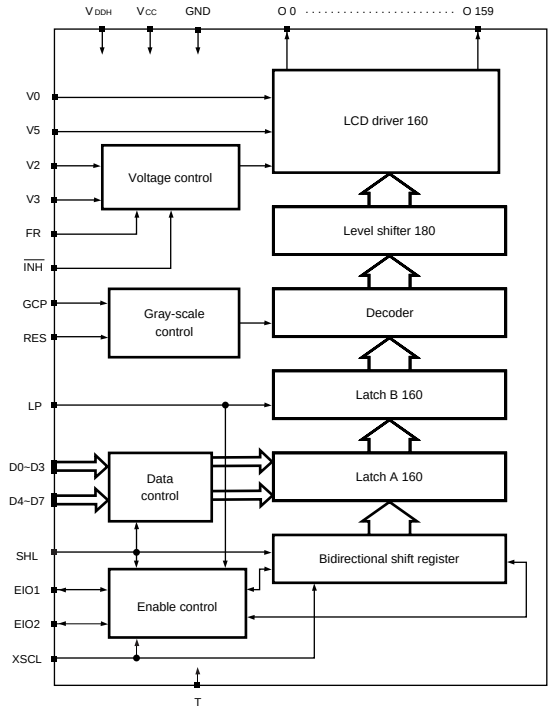
FEATURES

(1) 16 gray-scale LCD driver
- 4bit × 2 structure gray-scale signals
- Easier correction according to given characteristics of liquid crystal.
- Designed for 4 and 8 gray-scales, too.

(2) 160-LCD drive output
(3) Operating frequency
- 12MHz, maximum (when the automatic enable signal transfer function is used) Capable of operating 640 × 480 dot from the screen.
- 16MHz, maximum (when the automatic enable signal transfer function is not used)

(4) LCD drive voltage range from +14 to +40V
(5) Display blanking using the inhibit function
(6) Pin-selectable output shift direction
(7) Cascade connection and low-power realized through the automatic enable signal transfer function (enable signal from the control is no more needed)
(8) Offset voltage of LCD drive power can be adjusted corresponding to V_{DDH} or GND level
(9) 5.0V ±10% logic operation power
(10) CMOS silicon gate process
(11) Packages
Chip: • SED1765D0A (Aℓ pad)
• SED1765D0B (Au bump)
TCP: • SED1765T0A

BLOCK DIAGRAM



BLOCK FUNCTIONS

Gray-scale control circuit

A divider circuit used for dividing the gray-scale generation clock signal entered to the GCP terminal and transferring it to the decoder. This circuit is reset on the falling edge of the LP or RES inputs or when the $\overline{INH}$ input is LOW.

Data control circuit

This circuit reorders the gray-scale data entered to the D0 to D3 and D4 to D7 pins as specified by the SHL input, then, transfers data to the internal bus.
As long as the enable signal is disabled, internal data is fixed to low-level by the enable control circuit.

Enable control circuit

As long as the enable signal is disabled, this circuit holds the internal clock signal and data bus at low-level to introduce the power save mode to the system. When multiple segment drivers are used, EIO pins of the drivers are cascaded and the first driver EIO pin is connected to GND.
The enable control circuit automatically detects the end of 160 bit of data and transfers the enable signal automatically. Therefore, the control signal from the control LSI is no more needed.
The EIO output is reset by the LP input.

Shift register

This register shifts the latch A control signal as the shift clock is entered.
Shift direction is selected by the SHL input.

Latch A

Latch A signal from the shift register is used for sequentially latching the gray-scale data present on the internal bus.

Latch B

Latch B is used for acquiring the Latch A data on the falling edge of LP.

Decoder

Synchronizing with signal from the gray-scale control circuit, this circuit generates pulse width specified by the gray-scale data.

Level shifter

A level interface circuit for converting a signal voltage from V_{CC} system level to V_{DDH} system level.

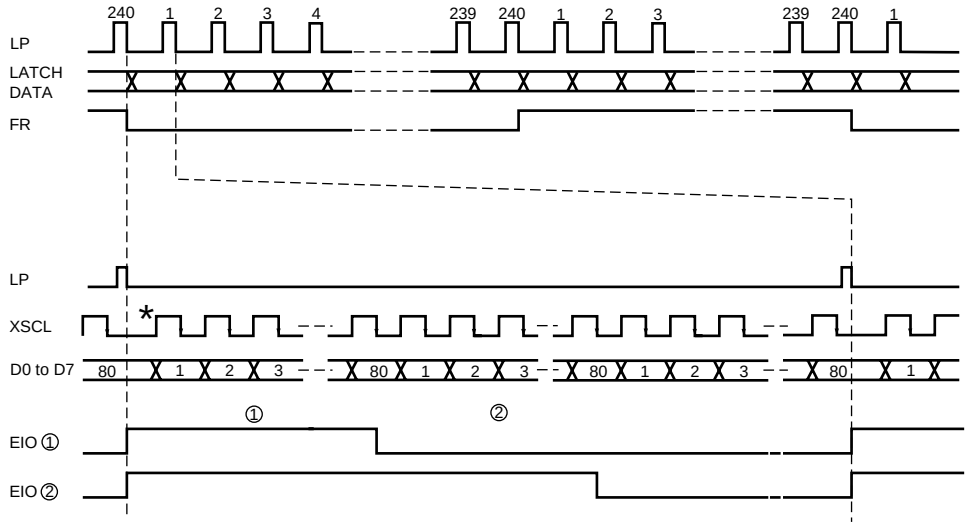
LCD drivers and voltage control circuit

They are used for generating the LCD drive voltage.
The following table shows relations between display data, frame signal FR and segment output voltage.

$\overline{INH}$	Display data	FR	Output voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	H	V_2
		L	V_3

Timing Chart

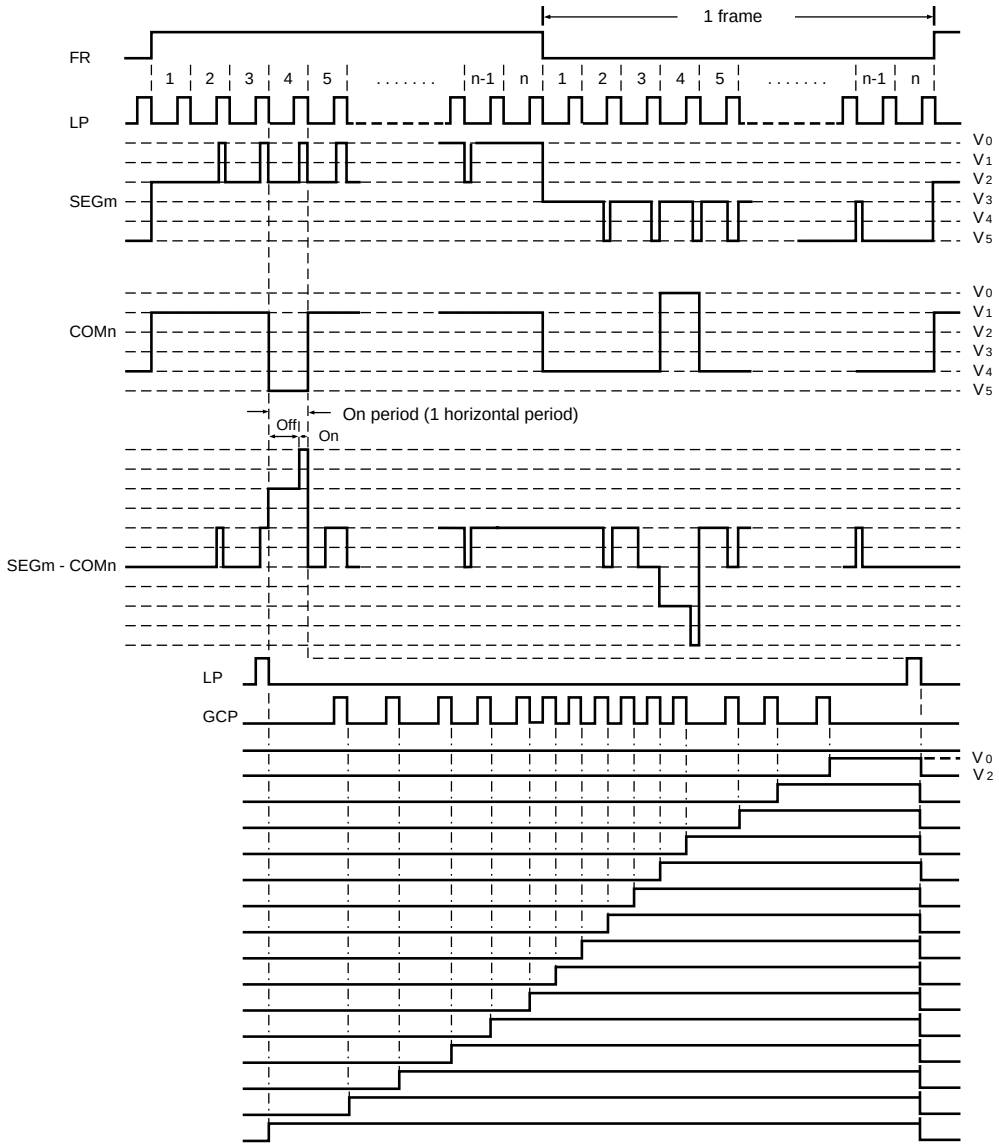
Timing Diagram
For 1/240 duty



① and ② represent the driver cascade number.

* In a high speed data transfer, longer XSCL cycle than the above is needed in the LP pulse insertion timing so that the LP→XSCL requirement can be met.

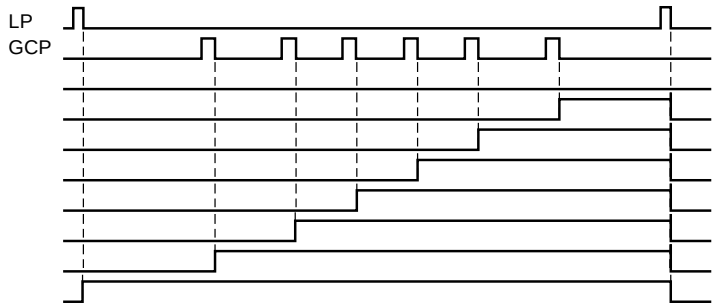
Gray-scale Data and LCD Output Waveform (For 16-level gray-scale)



(D0, D1, D2 and D3) correspond to (D4, D5, D6 and D7), respectively.

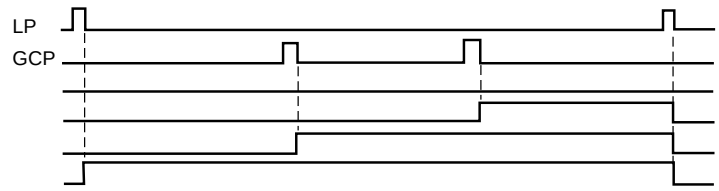
LCD output waveform as gray-scale data (for 8-level gray-scale)

Gray Scale	Gray-scale data			
	D3	D2	D1	D0
0	1	0	0	0
1	1	0	0	1
2	1	0	1	0
3	1	0	1	1
4	1	1	0	0
5	1	1	0	1
6	1	1	1	0
7	1	1	1	1



LCD output waveform as gray-scale data (for 4-level gray-scale)

Gray Scale	Gray-scale data			
	D3	D2	D1	D0
0	1	1	0	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1



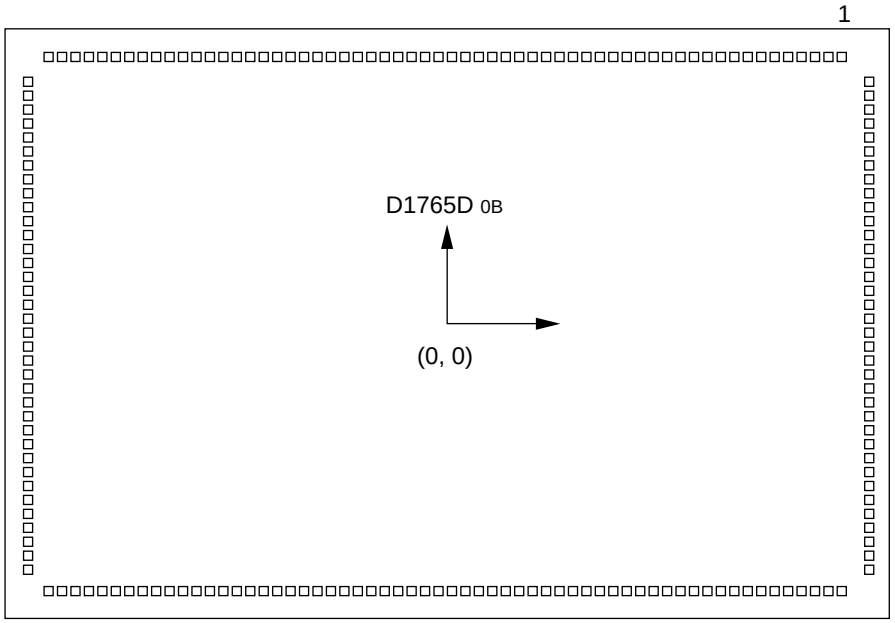
PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Power</th><th>No. of pins</th></tr>
<tr><td>O0 to O159</td><td>O</td><td>LCD drive segment (column) output.
The output changes at the falling edge of LP.</td><td>V_0 to V_5</td><td>160</td></tr>
<tr><td>D0 to D3
D4 to D7</td><td>I</td><td>Gray-scale generating 4 bit data input.
D4, D0 : LSB
D7, D3 : MSB</td><td>GND to V_{CC}</td><td>8
(1)</td></tr>
<tr><td>XSCL</td><td>I</td><td>Clock signal input.
Actuates shift register at the falling edge.</td><td>↑</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data latch signal input.
Latches display data at the falling edge.</td><td>↑</td><td>1</td></tr>
<tr><td>EIO1 to 2</td><td>I/O</td><td>Enable I/O.
When cascaded, it is connected to succeeding EIO.
Changes at falling edge of XSCL.</td><td>↑</td><td>2</td></tr>
<tr><td>GCP</td><td>I</td><td>Gray-scale generating clock signal input.
Activated at falling edge.</td><td>↑</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>PWM waveform reset signal input.
PWM waveform is set to OFF level as RES is entered.</td><td>↑</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift register direction select signal input.
When D0 to D3 and D4 to D7 are matched to An and Bn, respectively.
The following table shows the relation between the gray-scale data and segment output. (n indicates sequence of data.)
<table>
<tr><th rowspan="2">SHL</th><th colspan="8">O (SEG output)</th><th colspan="2">EIO</th></tr>
<tr><th>159</th><th>158</th><th>157</th><th></th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>A0</td><td>B0</td><td>A1</td><td>…</td><td>B78</td><td>A79</td><td>B79</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>B79</td><td>A79</td><td>B78</td><td>…</td><td>A1</td><td>B0</td><td>A0</td><td>Input</td><td>Output</td></tr>
</table></td><td>↑</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Frame signal input</td><td>↑</td><td>1</td></tr>
<tr><td>GND</td><td>Power</td><td>Common power supply</td><td>—</td><td>1</td></tr>
<tr><td>V_{CC}</td><td>Power</td><td>Logic operation power</td><td>—</td><td>1</td></tr>
<tr><td>V0, V2, V3
V5, V_{DDH}</td><td>Power</td><td>LCD drive bias power
$V_{DDH} \geq V_0 > V_2 \geq 7/9V_{DDH}$, $2/9V_{DDH} \geq V_3 > V_5 \geq$ GND</td><td>—</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Inhibit signal input.
It goes active when shifted to low-level and all segment outputs go OFF level (V_2 and V_3).</td><td>GND to V_{CC}</td><td>1</td></tr>
<tr><td>T</td><td>I</td><td>Test input. Normally, low-level is selected.</td><td>↑</td><td>1</td></tr>
</table>

Pins in ( ) are N.C pins. Total 186 pins.

PAD

Pad Layout



	x	y
Chip size	8.80 mm	×5.62 mm
Pad pitch	0.134 mm (Min.)	

1) A1 pad specification (SED1765D0A)
   Chip thickness 0.525 mm ± 0.025 mm
   x y
   Pad opening A
   100µm × 100µm
   For pads other than No. 36, 37, 38, 39 or 40.
   Pad opening B
   160µm × 100µm
   For pad No. 36, 37, 38, 39 or 40.
   (In the size, x denotes the direction in parallel with the scribe line)

2) Au bump specification (SED1765D0B) (For reference)
   Chip thickness 0.525 mm ± 0.025 mm
   x y
   Bump size A
   102µm × 100µm ± 20µm
   For pads other than No. 36, 37, 38, 39 or 40.
   Bump size B
   186µm × 100µm ± 20µm
   For pad No. 36, 37, 38, 39 or 40.
   (In the size, x denotes the direction in parallel with the scribe line)

Note: Positions of V0 to V5 of Pad No. 36-39 are different from those on the SED1766.

Pad Center Coordinate

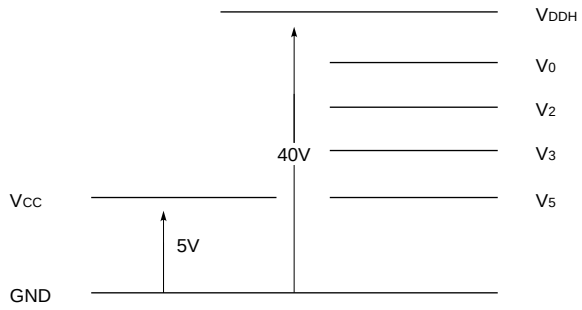
Unit: μm

PAD No.	PIN Name	X	Y
1	O146	3950	2643
2	147	3814	2643
3	148	3678	2643
4	149	3542	2643
5	150	3406	2643
6	151	3270	2643
7	152	3134	2643
8	153	2998	2643
9	154	2862	2643
10	155	2726	2643
11	156	2590	2643
12	157	2454	2643
13	158	2318	2643
14	159	2182	2643
15	EIO2	1998	2643
16	EIO1	1858	2643
17	GND	1718	2643
18	D0	1578	2643
19	D1	1438	2643
20	D2	1298	2643
21	D3	1158	2643
22	D4	1018	2643
23	D5	878	2643
24	D6	738	2643
25	D7	598	2643
26	NC	458	2643
27	SHL	318	2643
28	HSCL	178	2643
29	TEST	38	2643
30	$\overline{INH}$	–102	2643
31	LP	–242	2643
32	RES	–382	2643
33	GCP	–522	2643
34	V_{CC}	–662	2643
35	FR	–802	2643
36	V_0	–1032	2643
37	V_5	–1262	2643
38	V_3	–1492	2643
39	V_2	–1722	2643
40	V_{DDH}	–1952	2643
41	O0	–2182	2643
42	1	–2318	2643
43	2	–2454	2643
44	3	–2590	2643
45	4	–2726	2643
46	5	–2862	2643
47	6	–2998	2643
48	7	–3134	2643
49	8	–3270	2643
50	9	–3406	2643
51	10	–3542	2643
52	11	–3678	2643
53	12	–3814	2643
54	13	–3950	2643
55	14	–4230	2379
56	15	–4230	2243
57	16	–4230	2107
58	17	–4230	1971
59	18	–4230	1835
60	19	–4230	1699
61	20	–4230	1563
62	21	–4230	1427
63	O22	–4230	1291
64	23	–4230	1155
65	24	–4230	1019
66	25	–4230	883
67	26	–4230	747
68	27	–4230	611
69	28	–4230	475
70	29	–4230	339
71	30	–4230	203
72	31	–4230	67
73	32	–4230	–69
74	33	–4230	–205
75	34	–4230	–341
76	35	–4230	–477
77	36	–4230	–613
78	37	–4230	–749
79	38	–4230	–885
80	39	–4230	–1021
81	40	–4230	–1157
82	41	–4230	–1293
83	42	–4230	–1429
84	43	–4230	–1565
85	44	–4230	–1701
86	45	–4230	–1837
87	46	–4230	–1973
88	47	–4230	–2109
89	48	–4230	–2245
90	49	–4230	–2381
91	50	–3954	–2643
92	51	–3820	–2646
93	52	–3686	–2643
94	53	–3522	–2643
95	54	–3418	–2643
96	55	–3284	–2643
97	56	–3150	–2643
98	57	–3016	–2643
99	58	–2882	–2643
100	59	–2748	–2643
101	60	–2614	–2643
102	61	–2480	–2643
103	62	–2346	–2643
104	63	–2212	–2643
105	64	–2078	–2643
106	65	–1944	–2643
107	66	–1810	–2643
108	67	–1676	–2643
109	68	–1542	–2643
110	69	–1408	–2643
111	70	–1274	–2643
112	71	–1140	–2643
113	72	–1006	–2643
114	73	–872	–2643
115	74	–738	–2643
116	75	–604	–2643
117	76	–470	–2643
118	77	–336	–2643
119	78	–202	–2643
120	79	–68	–2643
121	80	68	–2643
122	81	202	–2643
123	82	336	–2643
124	83	470	–2643
125	O84	604	–2643
126	85	738	–2643
127	86	872	–2643
128	87	1006	–2643
129	88	1140	–2643
130	89	1274	–2643
131	90	1408	–2643
132	91	1542	–2643
133	92	1676	–2643
134	93	1810	–2643
135	94	1944	–2643
136	95	2078	–2643
137	96	2212	–2643
138	97	2346	–2643
139	98	2480	–2643
140	99	2614	–2643
141	100	2748	–2643
142	101	2882	–2643
143	102	3016	–2643
144	103	3150	–2643
145	104	3284	–2643
146	105	3418	–2643
147	106	3552	–2643
148	107	3686	–2643
149	108	3820	–2643
150	109	3954	–2643
151	110	4230	–2381
152	111	4230	–2245
153	112	4230	–2109
154	113	4230	–1973
155	114	4230	–1837
156	115	4230	–1701
157	116	4230	–1565
158	117	4230	–1429
159	118	4230	–1293
160	119	4230	–1157
161	120	4230	–1021
162	121	4230	–885
163	122	4230	–749
164	123	4230	–613
165	124	4230	–477
166	125	4230	–341
167	126	4230	–205
168	127	4230	–69
169	128	4230	67
170	129	4230	203
171	130	4230	339
172	131	4230	475
173	132	4230	611
174	133	4230	747
175	134	4230	883
176	135	4230	1019
177	136	4230	1155
178	137	4230	1291
179	138	4230	1427
180	139	4230	1563
181	140	4230	1699
182	141	4230	1835
183	142	4230	1971
184	143	4230	2107
185	144	4230	2243
186	145	4230	2379

ABSOLUTE MAXIMUM RATING

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 to V_{DDH} + 0.3	V
Input voltage	VI	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	–20 to +75	°C
Storage temperature (1)	Tstg1	–65 to +150	°C
Storage temperature (2)	Tstg2	–55 to +100	°C

Note 1: GND = 0V is assumed for all voltages.
Note 2: Storage temperature (1) is for independent chips and (2) is for when TAB is mounted.
Note 3: V_{DDH}, V_0, V_2, V_3 and V_5 voltage must always satisfy the condition $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



Note 4: Do not allow the logic operation power go floating state while the LCD drive circuit power is being applied. Otherwise, the LSI can be permanently destroyed.
Special care is needed for the system power on or off sequences.

ELECTRIC CHARACTERISTICS

DC Characteristics

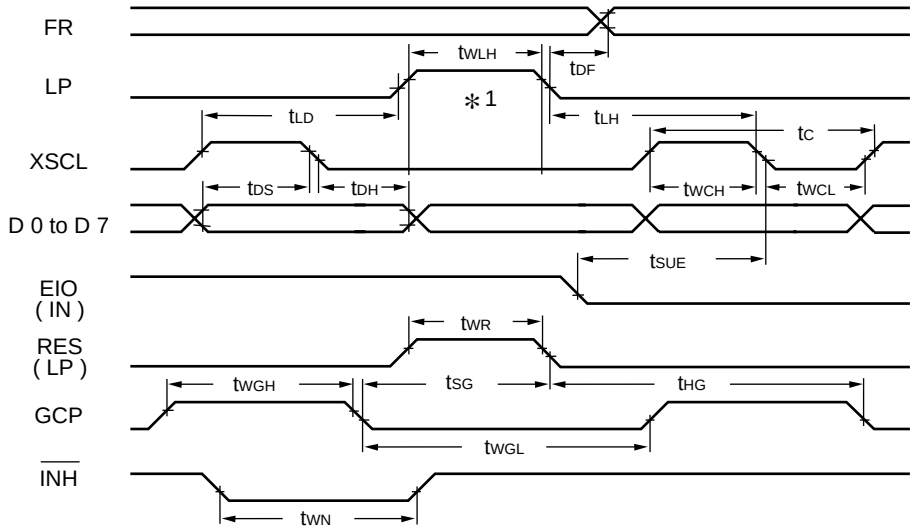
Unless otherwise specified, GND = 0V, V_{CC} = +5.0V ± 10%, Ta = –20 to +75°C

Item	Codes	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}		V_{CC}	4.5	5.0	5.5	V
Supply voltage (2)	V_{DDH}		V_{DDH}	14.0	—	40.0	V
On-level input voltage	V_0	$V_0 \geq V_2 \geq V_3 \geq V_5$	V_0	$V_{DDH} - 2.5$	—	V_{DDH}	V
Off-level input voltage (1)	V_2	Recommended value	V_2	$7/9 \times V_{DDH}$	—	V_{DDH}	V
Off input voltage (2)	V_3, V_5		V_3, V_5	GND	—	$2/9 \times V_{DDH}$	V
High-level input voltage	V_{IH}		All input pins	$0.8 \times V_{CC}$	—	V_{CC}	V
Low-level input voltage	V_{IL}			GND	—	$0.2 \times V_{CC}$	V
High-level output voltage	V_{OH}	I_{OH} = –0.4mA	EIO1	$V_{CC} - 0.4$	—	V_{CC}	V
Low-level output voltage	V_{OL}	I_{OL} = 0.4mA	EIO2	GND	—	0.4	V
Input leak current	I_{LI}	GND ≤ V_I ≤ V_{CC}	Other than EIO	—	—	2.0	µA
I/O leak current	$I_{LI/O}$	GND ≤ V_I ≤ V_{CC}	EIO1, 2	—	—	5.0	µA
Rest current	I_{GND}	V_{DDH} = 14.0 to 40.0V V_{IH} = V_{CC}, V_{IL} = GND	GND	—	—	25	µA
Output resistance *1	R0	V_{ON} = 0.5V, V_{DDH} = 10.0V	O0 to O159	—	2.0	6.5	kΩ
		V_{ON} = 0.5V, V_{DDH} = 20.0V		—	1.5	3.5	
		V_{ON} = 0.5V, V_{DDH} = 30.0V		—	1.3	3.0	
Operating current (1)	I_{CC}	V_{CC} = 5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{XSCL} = 10.8MHz f_{LP} = 33.8kHz, f_{GCP} = 0.54MHz, f_{FR} = 70Hz D0 to D7 = F0F0· · ·,	V_{CC}	—	2.5	5.0	mA
Operating current (2)	I_{DDH}	V_{CC} = 5.0V V_5 = 0V, V_3 = 4V V_2 = 26V, V_0 = V_{DDH} = 30V All other conditions are the same as those listed in I_{CC} column	V_{DDH}	—	0.5	1.2	mA
Input capacitance *2	C_I	Ta = 25°C, Freq. = 1MHz	Other than EIO	—	—	8.0	pF
I/O capacitance *2	$C_{I/O}$	Ta = 25°C, Freq. = 1MHz	EIO 1, 2	—	—	15.0	pF

* 1: To be selected within the specified input voltage ranges of V_0, V_2, V_3 and V_5.
* 2: Chip package only.

AC Characteristics

Input Timing Characteristics

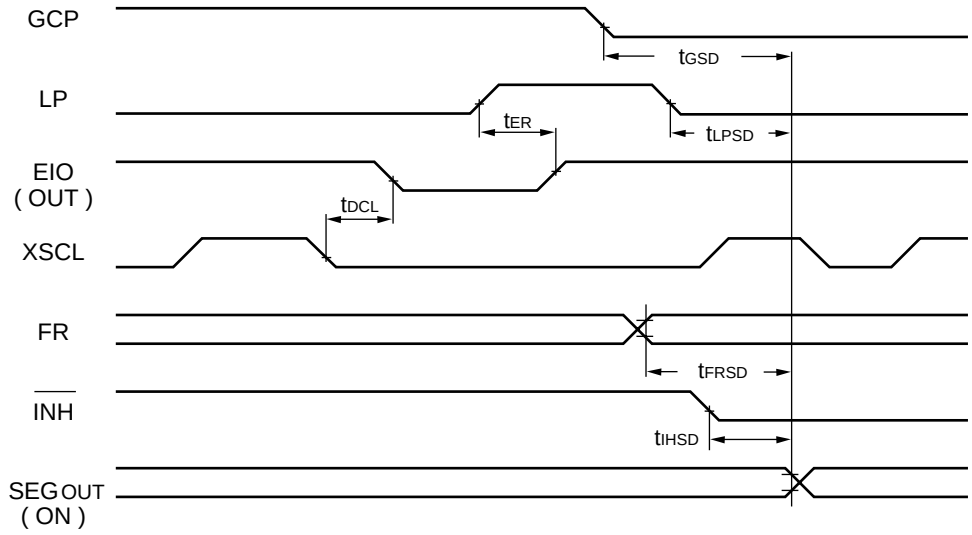


V_{CC} = +5.0V±10%, Ta = –20 to 75°C

Items	Codes	Conditions	Min.	Max.	Units
XSCL cycle	t_C	For independent IC operation	62	—	ns
		When enable signal transfer function is used	83	—	ns
XSCL high-level pulse width	t_{WCH}		25	—	ns
XSCL low-level pulse width	t_{WCL}		25	—	ns
EIO setup time	t_{SUE}		36	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		20	—	ns
XSCL → LP rising time	t_{LD}		0	—	ns
LP → XSCL falling time	t_{LH}		200	—	ns
LP pulse width	t_{WLH}	*1	80	—	ns
RES pulse width	t_{WR}		100	—	ns
INH low-level pulse width	t_{WN}		100	—	ns
GCP high-level pulse width	t_{WGH}		80	—	ns
GCP low-level pulse width	t_{WGL}		80	—	ns
Allowable FR delay time	t_{DF}		–300	+300	ns
GCP setup time	t_{SG}	Applicable to LP	200	—	ns
GCP hold time	t_{HG}	and RES signals	200	—	ns

*1: t_{WLH} indicates the time LP is HIGH as well as time XSCL is LOW.

Output Timing Characteristics



(V_{CC} = +5.0V ± 10%, V_{DDH} = +14.0 to +40.0V, Ta = –20 to +75°C)

Items	Codes	Conditions	Min.	Max.	Units
EIO reset time	t_{ER}	C_L = 15pF	—	120	ns
EIO output delay time	t_{DCL}		—	45	ns
LP → SEG (On) output delay time	t_{LPSD}	C_L = 100pF	—	0.6	µs
FR → SEG (On) output delay time	t_{FRSD}		—	0.8	µs
$\overline{INH}$ → SEG (On) output delay time	t_{IHSD}		—	0.6	µs
GCP → SEG (On) output delay time	t_{GSD}		—	0.6	µs

LCD DRIVE POWER SUPPLY

Setting up respective voltage levels

A desired LCD drive voltage level can be most easily obtained by dividing potential resistively. The resistive division approach ensures selecting accurate voltage level and providing stable voltage that are indispensable for high resolution display. This approach enables to select the lowest level allowable within the system supply capacity.

When low-power is needed, a higher value is set for the resistive division, then each voltage level is driven by means of voltage following using an operation amplifier.

In consideration of the case of using an operation amplifier, maximum LCD drive potential V_0 is separated from V_{DDH} and independent terminals are used. However, since efficacy of the LCD driving output driver deteriorates when the potential V_0 goes below V_{DDH} potential, potential difference between V_0-V_{DHH} must be at 0V to 2.5V. When an operation amplifier is not used, V_0 and V_{DDH} are connected.

Precautions for power on or off

Excessive current resulted from high voltage applied to the LCD drive circuit can damage the LSI.

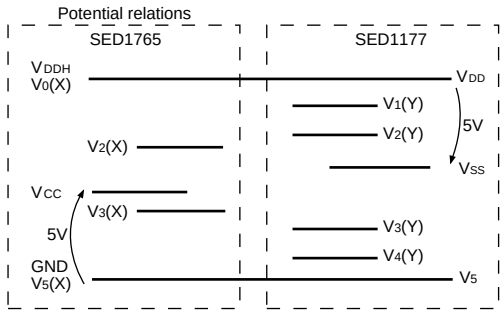
Therefore, the following sequences must be maintained when turning power on or off.

When turning power on:	Turn on V_{CC} power → turn on the V_{DHH} power or turn them on simultaneously.
When turning power off:	Turn off V_{DDH} power → turn V_{CC} power or turn them off simultaneously.

For protection against excessive current, insert a quick melting fuse in series in respective power supplies.

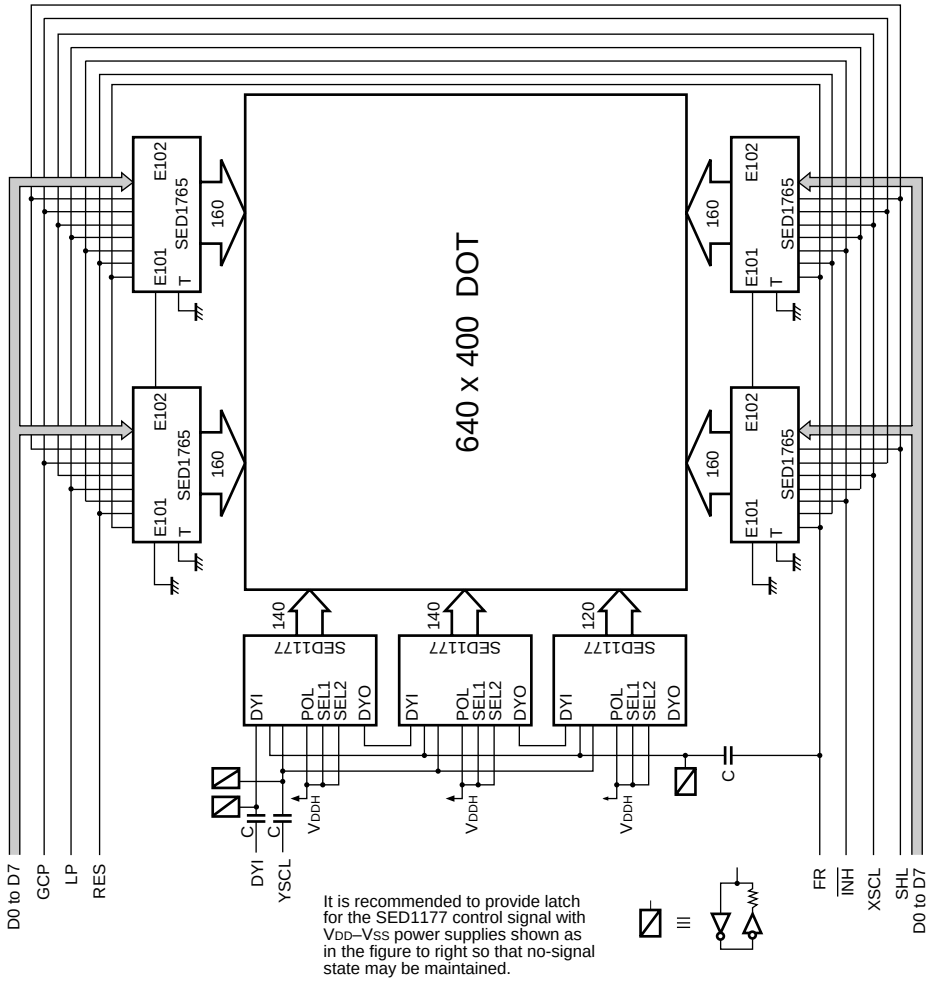
CIRCUIT EXAMPLE

An Example of Large Screen LCD Structure



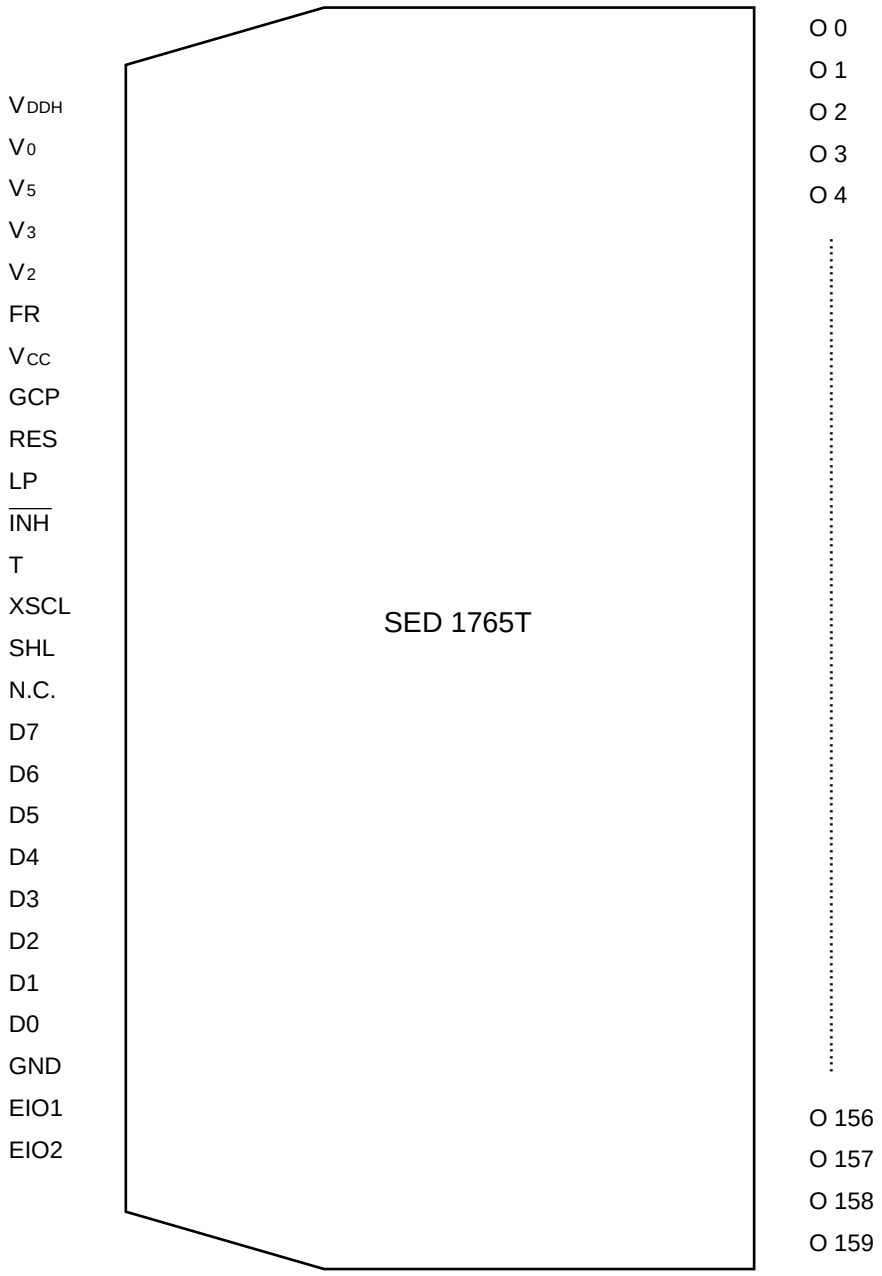
GND : SED1765 common ground
V_{CC} : SED1765 logic operation positive power supply
V_{DDH} : SED1177 common ground
V_{SS} : SED1177 logic operation negative power supply

LCD power supply V_{LCD} (V_0 to V_5) must satisfy the following condition:
V_{DDH} (V_{DD}) ≥ V_{LCD} ≥ GND (V_5)
The control signal between amplitude V_{CC}-GND is supplied to the SED1177 via capacitance C.



TCP

A Sample Pin Layout

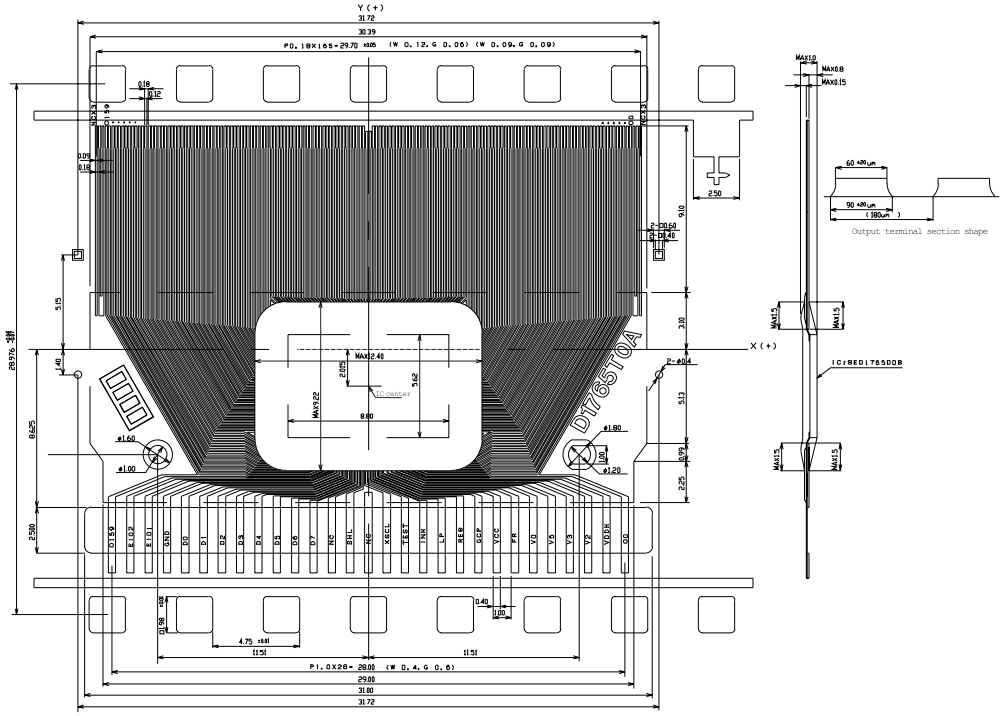


Note: The above is not intended to determine contour of TCP.

DIMENSIONAL OUTLINE DRAWING

SED1765T0A

For reference



Unit: mm

11. SED1766
LCD Segment Driver

Contents

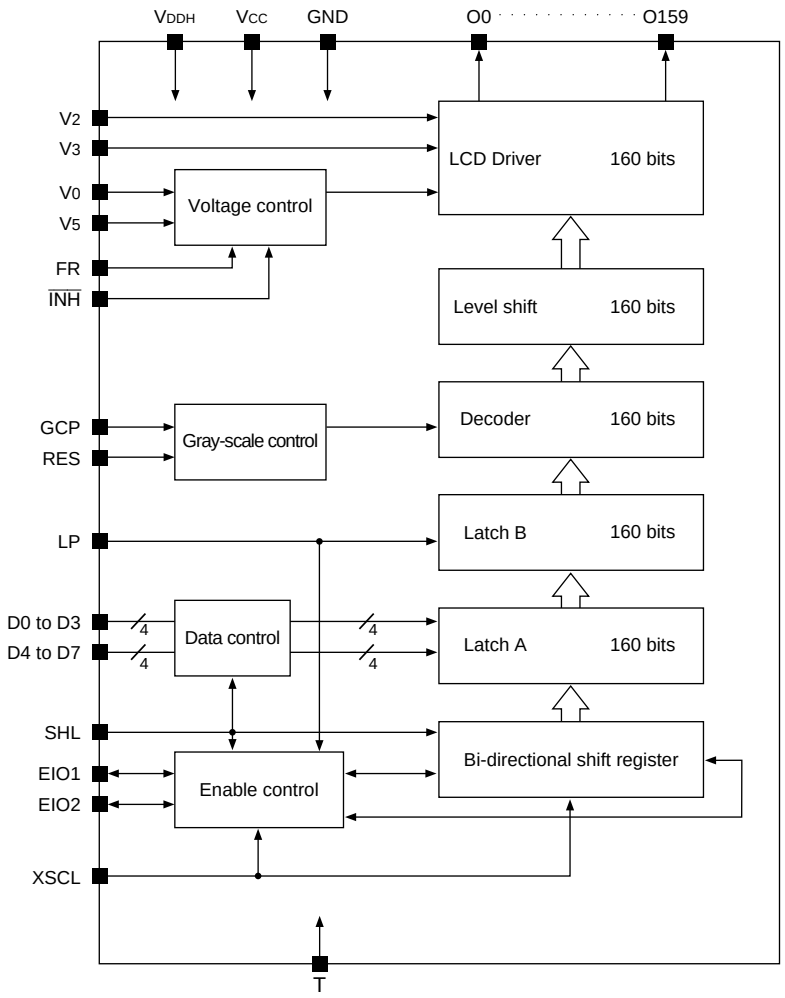
1. OVERVIEW

The SED1766 is a segment (column) driver for high-capacity dot matrix liquid crystal panels. It incorporates 160 high-voltage segment (column) drivers, and is designed for use in conjunction with the SED1703 common (row) driver device. The SED1766 uses a PWM (Pulse Width Modulation) technique to provide 16, 8, or 4-level gray-scale displays without ghosting. An external pulse controller circuit can be used to control the gray-scale pulse position within the horizontal interval. The high number of output drivers integrated into the SED1766 simplifies circuit design of large-screen LCD drive circuits. For example by using the SED1766 with the SED1703 a complete 640 × 480 gray-scale display can be implemented with as few as seven chips.

2. FEATURES

- 16, 8 or 4-level PWM gray-scale LCD driver
- Output pulse can be positioned in the center or to the right edge of the horizontal interval
- Supports gray-scale gamma correction
- Two parallel 4-bit inputs
- 160 LCD drive outputs
- Maximum clock speed of 12 MHz allows a 640 × 480 pixel display with daisy-chain enable
- Speeds up to 16 MHz are possible using external enable generation
- Wide 14 to 40 V range of LCD drive voltages
- Display blanking function
- Output shift direction is pin-selectable
- Automatic enable signal propagation allows cascade connection and decreased power consumption
- Adjustable LCD drive voltage offset relative to ground and supply
- Single 5.0 V ±10% logic power supply
- CMOS Si-gate process
- Packages:
  - Al pad chip: SED1766D0A
  - Au bump pad chip: SED1766D0B

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

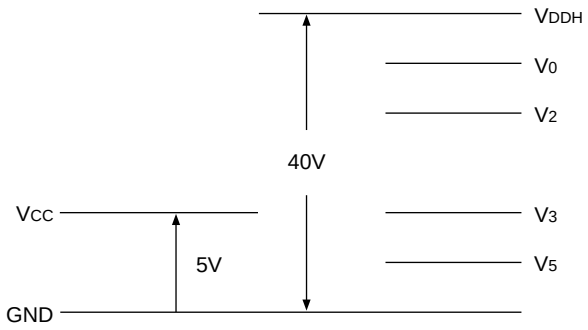
Pin Name	Input/ Output	Description
O0 to O159	O	Segment drive outputs
D0 to D3, D4 to D7	I	4-bit gray-scale data inputs D0 and D4 are the LSBs of each 4-bit nibble.
XSCL	I	Segment data shift clock input Data is shifted into the driver on the falling edge of XSCL.
LP	I	Segment data latch strobe Data is latched on the falling edge of LP.
EIO1, EIO2	I/O	Daisy chain enable input/outputs configured by SHL.
GCP	I	Gray-scale reference clock input.
RES	I	PWM mode control input See timing diagrams. V_{OFF} refers to drive voltages V2 and V3, V_{ON} refers to drive voltages V0 and V5. Before RES pulse: $V_{OFF} \rightarrow V_{ON}$ transition mode. After RES pulse: $V_{ON} \rightarrow V_{OFF}$ transition mode.
SHL	I	Shift direction select input This signal configures EIO1, EIO2 and selects the shift register shift direction. A*n* is input on D0 to D3 and B*n* on D4 to D7.
FR	I	LCD AC-drive waveform input
$\overline{INH}$	I	Display blanking input When LOW, all outputs go to OFF levels.
GND	—	Ground
V_{CC}	—	Logic power supply
V0, V2, V3, V5, V_{DDH}	—	LCD drive voltage supply inputs These voltages should satisfy the following conditions. $V_{DDH} \geq V_0 > V_2 \geq 7/9V_{DDH}$, $2/9V_{DDH} \geq V_3 > V_5 \geq$ GND
T	I	Test input Tie low.

5. SPECIFICATIONS

5-1 Absolute Maximum Rating

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 ~ +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 ~ +45.0	V
Supply voltage (3)	V_0, V_2, V_3, V_5	–0.3 ~ V_{DDH} + 0.3	V
Input voltage	V_I	–0.3 ~ V_{CC} + 0.3	V
Working temperature	Topr	–20 ~ +75	°C
Storage temperature 1	Tstg	–65 ~ +150	°C

Note: Drive voltages should satisfy the following conditions. $V_{DDH} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq GND$.



5-2 DC Characteristics

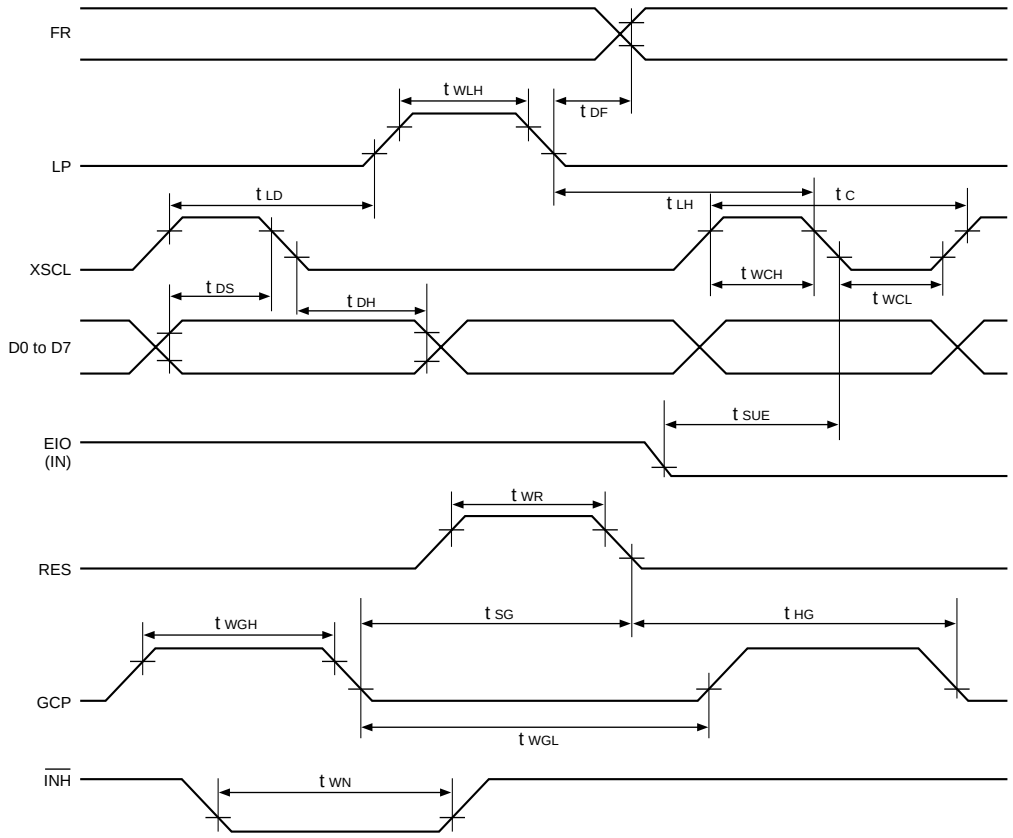
Unless otherwise specified, V_5 = 0V, Ta = –20 to 75°C

Item	Symbol	Condition		Applicable pin	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{CC}			V_{CC}	4.5	5.0	5.5	V
Supply voltage (2)	V_{DDH}			V_{DDH}	14.0	—	40.0	V
Input voltage	V_0	$V_0 \geq V_2 \geq V_3 \geq V_5$		V0	V_{DDH}–2.5	—	V_{DDH}	V
Input voltage (1)	V_2			V2	7/9×V_{DDH}	—	V_{DDH}	V
Input voltage (2)	V_3, V_5			V3, V5	GND	—	2/9×V_{DDH}	V
HIGH-level input voltage	V_{IH}			All input pins.	0.8×V_{CC}	—	V_{CC}	V
LOW-level input voltage	V_{IL}				GND	—	0.2×V_{CC}	V
HIGH-level output voltage	V_{OH}	I_{OH}=–0.4 mA		EIO1, EIO2	V_{CC}–0.4	—	V_{CC}	V
LOW-level output voltage	V_{OL}	I_{OH}=0.4 mA			GND	—	0.4	V
Input leakage current	I_{LI}	GND≤V_I≤V_{CC}		All pins except EIO	—	—	2.0	µA
I/O leakage current	$I_{LI/O}$	GND≤V_I≤V_{CC}		EIO1, EIO2	—	—	5.0	µA
Quiescent current	I_{GND}	V_{DDH}=14.0 to 40.0V, V_{IH}=V_{CC}, V_{IL}=GND		GND	—	—	25	µA
Segment output ON resistance See note 1.	R_O	V_{ON}=0.5V	V_{DDH}=10.0V	O0 to O159	—	2.0	6.5	kΩ
			V_{DDH}=20.0V		—	1.5	3.5	
			V_{DDH}=30.0V		—	1.3	3.0	
Operating current (1)	I_{CC}	V_{CC}=5.0 V, V_{IH}=V_{CC}, V_{IL}=GND, f_{XSCL}=10.8 MHz, f_{LP}=33.8 kHz, f_{GCP}=0.54 MHz, f_{FR}=70 Hz, D0 to D7=F0F0.., alternating		V_{CC}	—	2.5	5.0	mA
Operating current (2)	I_{DDH}	V_{CC}=5.0 V, V_5=0 V, V_3=4 V, V_2=26 V, V_0=V_{DDH}=30 V, other conditions same as I_{CC}		V_{DDH}	—	0.5	1.2	mA
Input capacitance See note 2.	C_I	Ta=25°C, Freq.=1 MHz		All pins except EIO	—	—	8.0	pF
I/O capacitance See note 2.	$C_{I/O}$	Ta=25°C, Freq.=1 MHz		EIO1, EIO2	—	—	15.0	pF

Notes: 1. Within the specified ranges of V_0, V_2, V_3 and V_4.
2. Chip package only.

5-3 AC Characteristics

- **Input timing**



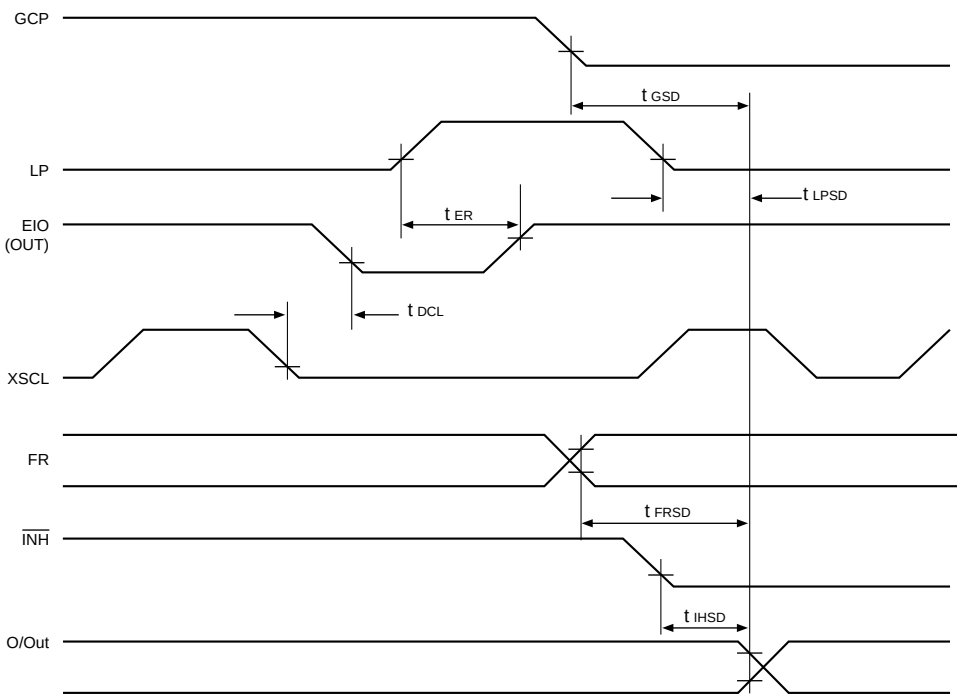
Note: For timing of LP pulse input, omit one XSCL clock cycle.

Unless otherwise specified, V_{CC} = 5.0V ±10%, Ta = –20 to 75°C

Items	Symbol	Conditions	Min.	Max.	Units
Shift clock period	t_C	IC operating alone	62	—	ns
		Using enable transfer function	83	—	
Shift clock HIGH-level pulsewidth	t_{WCH}		25	—	ns
Shift clock LOW-level pulsewidth	t_{WCL}		25	—	ns
EIO setup time	t_{SUE}		36	—	ns
Data setup time	t_{DS}		30	—	ns
Data hold time	t_{DH}		20	—	ns
Shift clock to latch pulse interval	t_{LD}		0	—	ns
Latch hold time	t_{LH}		200	—	ns
LP pulsewidth	t_{WLH}	See note.	80	—	ns
RES pulsewidth	t_{WR}		100	—	ns
$\overline{INH}$ pulsewidth	t_{WN}		100	—	ns
GCP HIGH-level pulsewidth	t_{WGH}		80	—	ns
GCP LOW-level pulsewidth	t_{WGL}		80	—	ns
FR delay time	t_{DF}		–300	+300	ns
GCP setup time	t_{SG}	Applicable to LP and RES signal	200	—	ns
GCP hold time	t_{HG}		200	—	ns

Note: t_{WLH} indicates the time XSCL is LOW as well as the time that LP is HIGH.

- **Output timing**



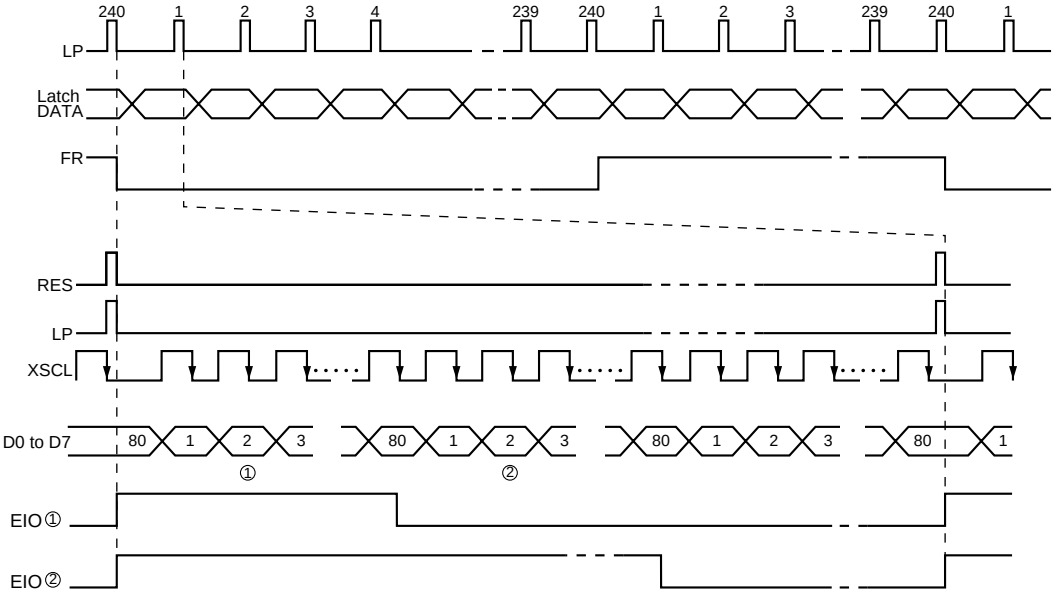
$V_H = 0.8 \times V_{CC}$
$V_L = 0.2 \times V_{CC}$

Unless otherwise specified, V_{DDH} = 14.0 to 40.0 V, Ta = –20 to 75°C

Items	Symbol	Conditions	Min.	Max.	Units
EIO output reset time	t_{ER}	C_L = 15 pF	—	120	ns
EIO output delay time	t_{DCL}		—	45	
LP to segment output delay time	t_{LPSD}	C_L = 100 pF	—	0.6	µs
FR to segment output delay time	t_{FRSD}		—	0.8	µs
$\overline{INH}$ to segment output delay time	t_{IHSD}		—	0.6	µs
GCP to segment output delay time	t_{GSD}		—	0.6	µs

5-4 Timing Diagrams

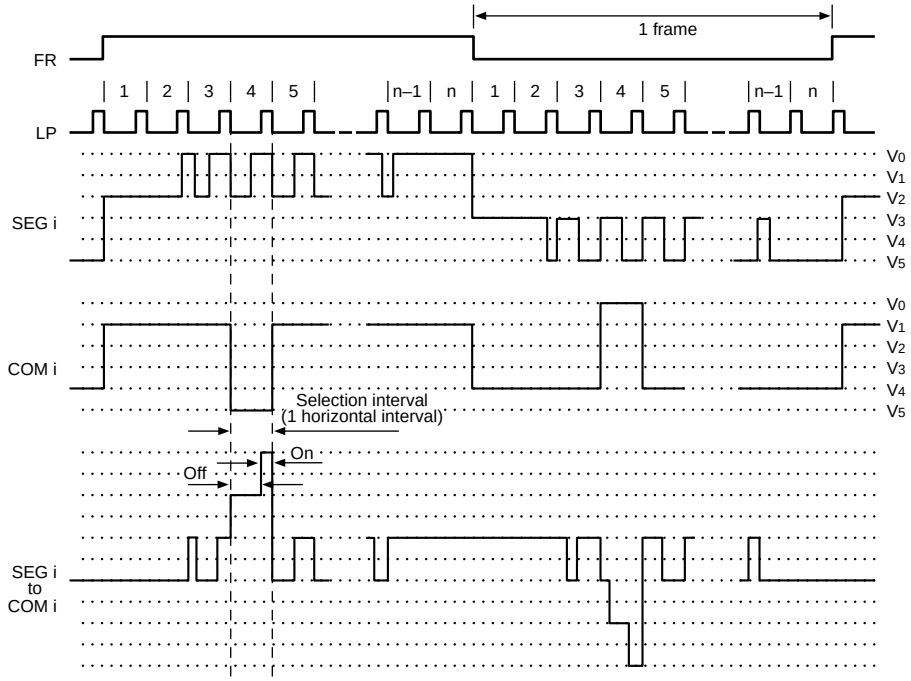
- **1/240 Duty Cycle**



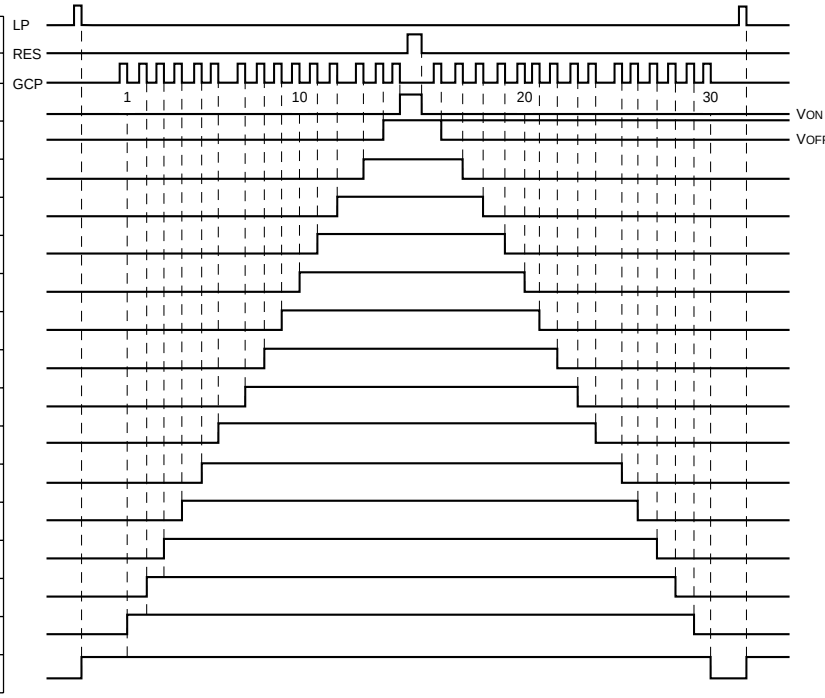
$V_H = 0.8 \times V_{CC}$
$V_L = 0.2 \times V_{CC}$

Notes: 1. Circled numerals denote the position of the device in the cascade chain.
2. With high-spoeed data transfer, it is necessary to delay the transition of XSCL following the LP pulse falling edge, to ensure that the minimum LP to XSCL time specification is met.

- **16-level gray-scale data and LCD output waveforms**



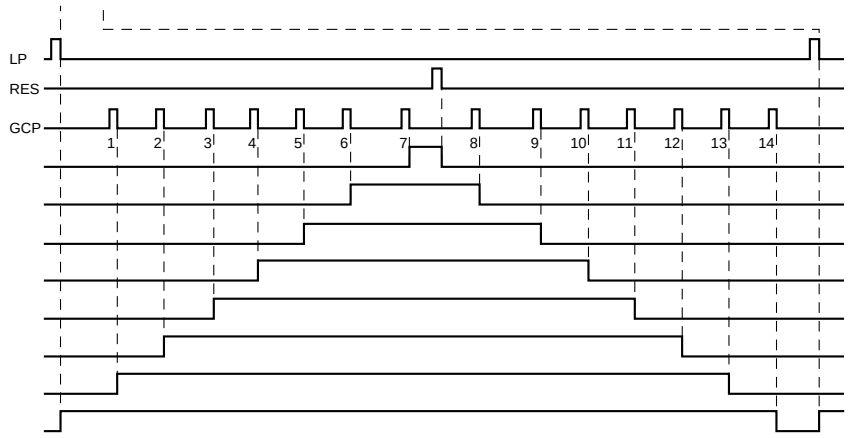
Gray scale	Gray scale data			
	D3	D2	D1	D0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



Note: (D0, D1, D2, D3) also refer to (D4, D5, D6, D7).

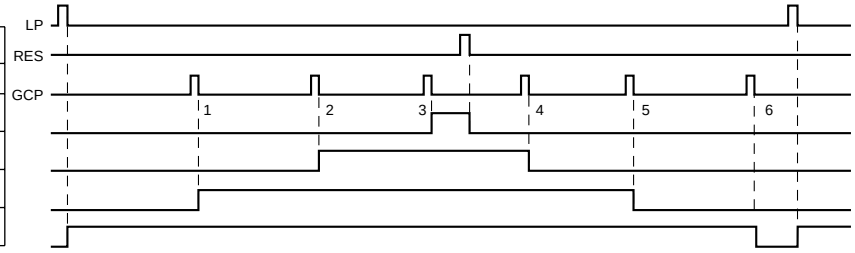
- **8-level gray-scale data and LCD output waveforms**

Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	0	0	0
1	1	0	0	1
2	1	0	1	0
3	1	0	1	1
4	1	1	0	0
5	1	1	0	1
6	1	1	1	0
7	1	1	1	1



- **4-level gray-scale data and LCD output waveforms**

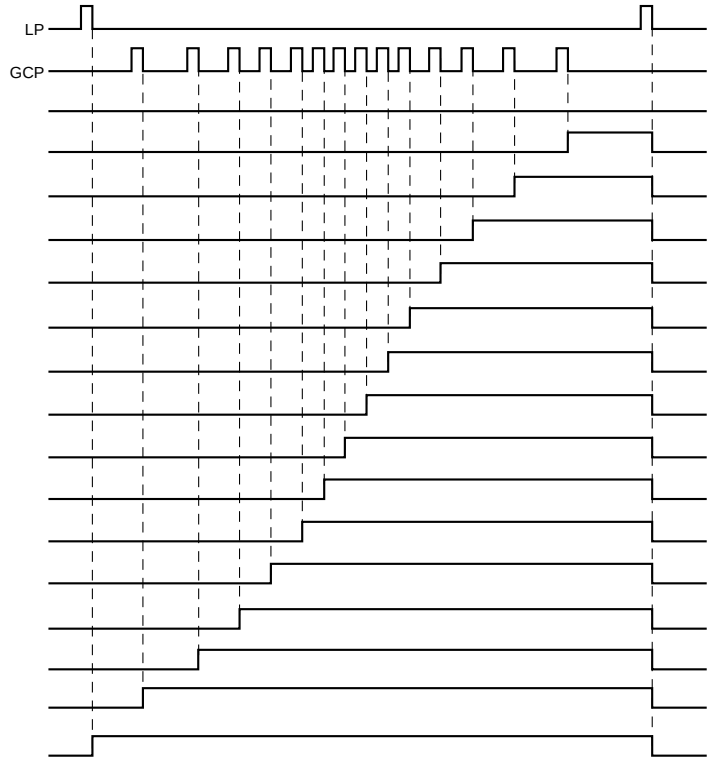
Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	1	0	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1



Note: The segment outputs change state on the falling edge of the fifteenth GCP pulse following an LP or RES pulse, regardless of the value of the gray-scale data.

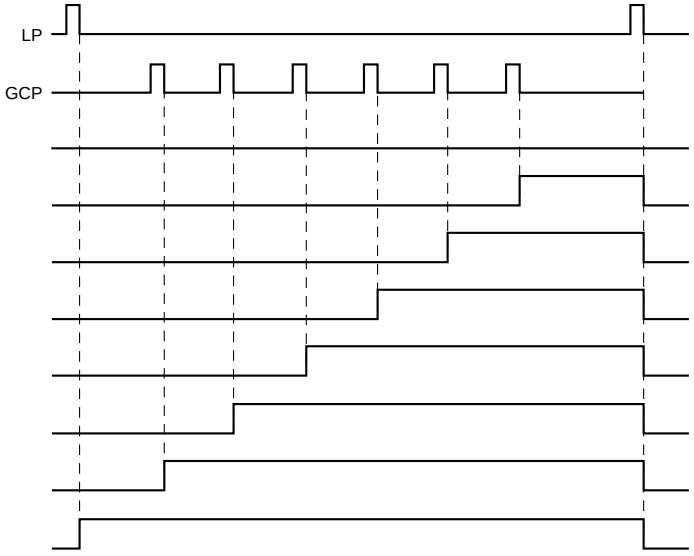
- **Right-hand PWM mode 16-level gray-scale data and LCD output waveforms**

Gray scale	Gray scale data			
	D3	D2	D1	D0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



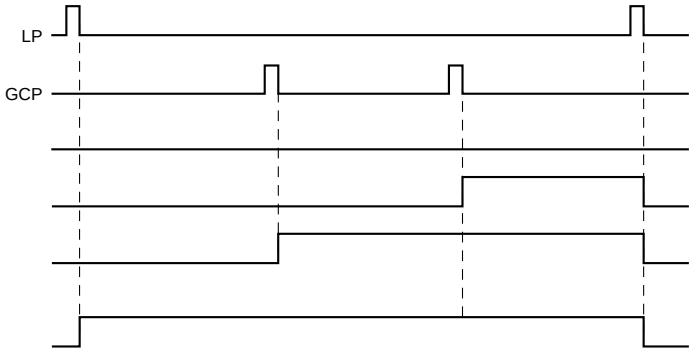
- **Right-hand PWM mode 8-level gray-scale data and LCD output waveforms**

Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	0	0	0
1	1	0	0	1
2	1	0	1	0
3	1	0	1	1
4	1	1	0	0
5	1	1	0	1
6	1	1	1	0
7	1	1	1	1



- **Right-hand PWM mode 4-level gray-scale data and LCD output waveforms**

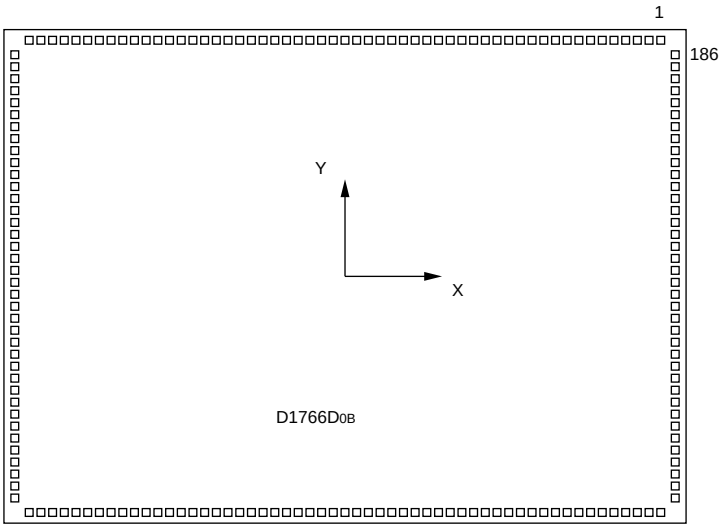
Gray scale	Gray scale data			
	D3	D2	D1	D0
0	1	1	0	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1



5-5 Package Dimensions

• Chip Package (SED1766D0A and SED1766D0B)

– Pad Layout



Chip size: 8.80 × 5.62
Pad pitch: 0.134 mm min.

- Al pad (SED1766D0A)
  Chip thickness: 0.525 ±0.025 mm
  Pad size, type A: 100 µm × 100 µm (All pads except 36, 37, 38, 39, 40)
  Pad size, type B: 160 µm × 100 µm (Pads 36, 37, 38, 39, 40)

- Au bump pad (SED1766D0B)
  Chip thickness: 0.525 mm ±0.025 mm
  Pad size, type A: 102 µm × 100 µm ±20 µm (All pads except 36, 37, 38, 39, 40)
  Pad size, type B: 186 µm × 100 µm ±20 µm (Pads 36, 37, 38, 39, 40)

Note: Sizes are specified as x-dimension × y-dimension. X is parallel to the scrib-line.

– Pad Coordinates

PAD No.	PAD Name	X	Y
1	O146	3950	2643
2	O147	3814	↓
3	O148	3678	
4	O149	3542	
5	O150	3406	
6	O151	3270	
7	O152	3134	
8	O153	2998	
9	O154	2862	
10	O155	2726	
11	O156	2590	
12	O157	2454	
13	O158	2318	
14	O159	2182	
15	EIO2	1998	
16	EIO1	1858	
17	GND	1718	
18	D0	1578	
19	D1	1438	
20	D2	1298	
21	D3	1158	
22	D4	1018	
23	D5	878	
24	D6	738	
25	D7	598	
26	NC	458	
27	SHL	318	
28	XSCL	178	
29	TEST	38	
30	$\overline{INH}$	–102	
31	LP	–242	
32	RES	–382	
33	GCP	–522	
34	V_{CC}	–662	
35	FR	–802	
36	V_2	–1032	
37	V_3	–1262	
38	V_5	–1492	
39	V_0	–1722	
40	V_{DDH}	–1952	
41	O0	–2182	
42	O1	–2318	
43	O2	–2454	
44	O3	–2590	
45	O4	–2726	
46	O5	–2862	
47	O6	–2998	
48	O7	–3134	
49	O8	–3270	
50	O9	–3406	
51	O10	–3542	
52	O11	–3689	
53	O12	–3814	
54	O13	–3950	↓
55	O14	–4230	2379
56	O15	↓	2243
57	O16		2107
58	O17		1971
59	O18		1835
60	O19		1699
61	O20		1563
62	O21	↓	1427

PAD No.	PAD Name	X	Y
63	O22	–4230	1291
64	O23	↓	1155
65	O24		1019
66	O25		883
67	O26		747
68	O27		611
69	O28		475
70	O29		339
71	O30		203
72	O31		67
73	O32		–69
74	O33		–205
75	O34		–341
76	O35		–477
77	O36		–613
78	O37		–749
79	O38		–885
80	O39		–1021
81	O40		–1157
82	O41		–1293
83	O42		–1429
84	O43		–1565
85	O44		–1701
86	O45		–1837
87	O46		–1973
88	O47		–2109
89	O48		–2245
90	O49	↓	–2381
91	O50	–3954	–2643
92	O51	–3820	↓
93	O52	–3686	
94	O53	–3522	
95	O54	–3418	
96	O55	–3284	
97	O56	–3150	
98	O57	–3016	
99	O58	–2882	
100	O59	–2748	
101	O60	–2614	
102	O61	–2480	
103	O62	–2346	
104	O63	–2212	
105	O64	–2078	
106	O65	–1944	
107	O66	–1810	
108	O67	–1676	
109	O68	–1542	
110	O69	–1408	
111	O70	–1274	
112	O71	–1140	
113	O72	–1006	
114	O73	–872	
115	O74	–738	
116	O75	–604	
117	O76	–470	
118	O77	–336	
119	O78	–202	
120	O79	–68	
121	O80	68	
122	O81	202	
123	O82	336	
124	O83	470	↓

PAD No.	PAD Name	X	Y
125	O84	604	–2643
126	O85	738	↓
127	O86	872	
128	O87	1006	
129	O88	1140	
130	O89	1274	
131	O90	1408	
132	O91	1542	
133	O92	1676	
134	O93	1810	
135	O94	1944	
136	O95	2078	
137	O96	2212	
138	O97	2346	
139	O98	2480	
140	O99	2614	
141	O100	2748	
142	O101	2882	
143	O102	3016	
144	O103	3150	
145	O104	3284	
146	O105	3418	
147	O106	3552	
148	O107	3686	
149	O108	3820	
150	O109	3954	↓
151	O110	4230	–2381
152	O111	↓	–2245
153	O112		–2109
154	O113		–1973
155	O114		–1837
156	O115		–1701
157	O116		–1565
158	O117		–1429
159	O118		–1293
160	O119		–1157
161	O120		–1021
162	O121		–885
163	O122		–749
164	O123		–613
165	O124		–477
166	O125		–341
167	O126		–205
168	O127		–69
169	O128		67
170	O129		203
171	O130		339
172	O131		475
173	O132		611
174	O133		747
175	O134		883
176	O135		1019
177	O136		1155
178	O137		1291
179	O138		1427
180	O139		1563
181	O140		1699
182	O141		1835
183	O142		1971
184	O143		2107
185	O144		2243
186	O145	↓	2379

6. FUNCTIONAL DESCRIPTION

6-1 Gray-Scale Control Circuit

This is a divider circuit for the gray-scale generation clock signal input on pin GCP, with an output to the decoder. The divider circuit is reset on the falling edge of the RES or LP inputs or when the $\overline{INH}$ input is LOW.

6-2 Data Control Circuit

This circuit reorders the gray-scale data input on the D0 to D3 and D4 to D7 pins, into the order specified by the SHL input, and puts them on the internal data bus. When power save mode is activated, by an inactive enable signal, the data control circuit holds all bus lines LOW.

6-3 Enable Controller

This circuit puts the device into the power save mode when the enable signal is inactive and causes the data bus and the internal clock to be held LOW.

In systems with more than one segment driver, the enable inputs and outputs are cascaded, and the enable input at the head of the chain is connected to ground. The enable controller counts the number of input data bits and sets the enable output LOW to allow the next device in the chain to start loading data. This configuration eliminates the need for the controlling device to generate enable control signals.

The EIO output is reset HIGH by the LP input.

6-4 Shift Register

Segment data shift register generates the latch A control signal from the segment data shift clock. The direction of data shift is selected by the HSL pin as shown in the table below.

SHL	O(SEG Output)							EIO	
	159	158	157	.....	2	1	0	1	2
L	A0	B0	A1	.....	B78	A79	B79	Output	Input
H	B79	A79	B78	.....	A1	B0	A0	Input	Output

6-5 Latch A

The gray-scale data present on the internal data bus is latched by the latch control signal from the shift register.

6-6 Latch B

The data in latch A is latched into latch B on the falling edge of LP.

6-7 Decoder

This circuit is locked to the signal from the gray-scale controller and generates a pulse width corresponding to the gray-scale data value.

6-8 Level Shifter

The level shifter converts the logic-level signal from latch B to the voltage levels required by the LCD drivers.

6-9 LCD Drivers and Voltage Control Circuit

The LCD drivers drive individual columns of the display matrix with the voltage determined by the inhibit signal $\overline{INH}$, the frame signal FR, and the latched display data. This is shown in the table below.

$\overline{INH}$	Display Data	FR	Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	H	V_2
		L	V_3

6-10 LCD Drive in Right-Hand PWM Mode

By using the LP and GCP signals as shown in the timing diagrams, and holding RES LOW, the PWM pulse can be set to the right-hand side of the horizontal interval.

7. APPLICATION NOTES

7-1 Voltage Levels

The recommended method of obtaining the various LCD drive voltages is a voltage divider between V_{DDH} and ground, buffered by op-amp voltage followers connected to the V_0 to V_5 inputs. The SED1702 separates V_0 from V_{DDH}, and V_5 from ground, allowing the use of op-amps that do not swing all the way to the positive rail or ground.

Note, however, that driver efficiency decreases the larger the difference between V_0 and V_{DDH}, or between V_5 and ground. Keep these differences to less than 2.5 V for optimum operation.

A simple resistive divider without op-amps can also be used. V_0 is connected to V_{DDH}, and V_5 to ground. The value of the resistors should be low as permitted by the capacity of the power supply, to give the most accurate and stable bias voltages.

7-2 Power-up and Power-down Precautions

Due to the high supply voltage of the driver circuitry, excessive current will flow into the SED1702 if the driver supply is applied when the 5 V logic supply is not connected, permanently damaging the device. To prevent this, ensure that the driver supply is never on when the logic supply is off.

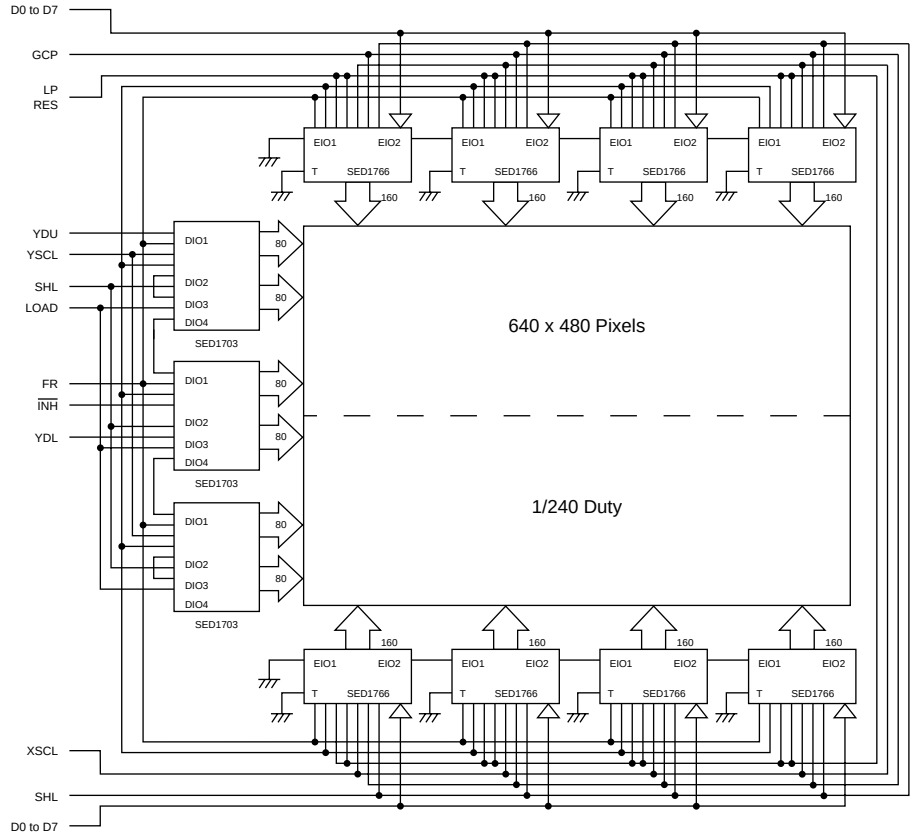
Power-on: Apply power to the logic circuitry BEFORE, or at the same time as, applying power to the driver circuitry.

Power-off: Remove power from the logic circuitry AFTER, or at the same time as, removing power from the driver circuitry.

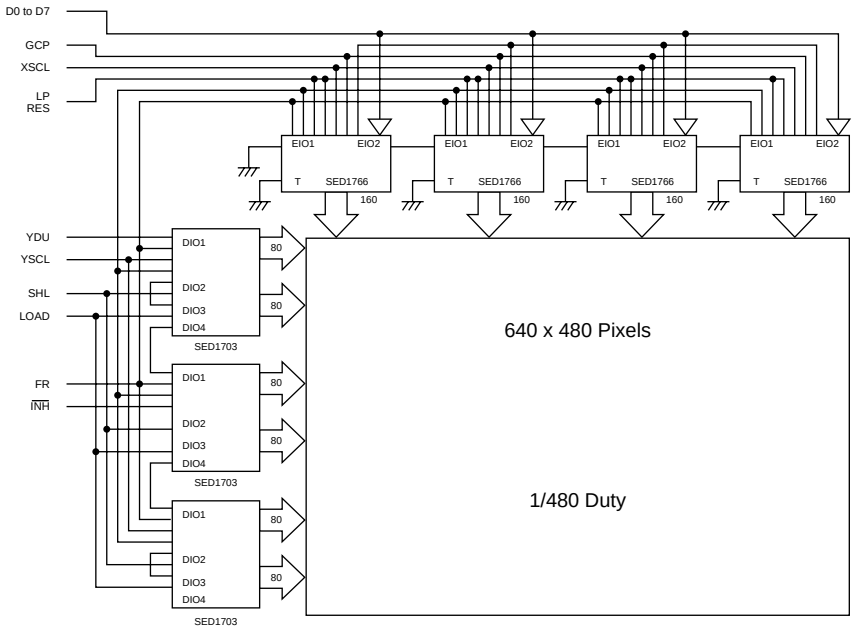
As an additional measure to safe guard against excessive current flow, insert a high-speed fuse in series with each drive voltage input.

8. TYPICAL APPLICATION CIRCUITS

- **Large-screen LCD, 1/240 duty cycle**



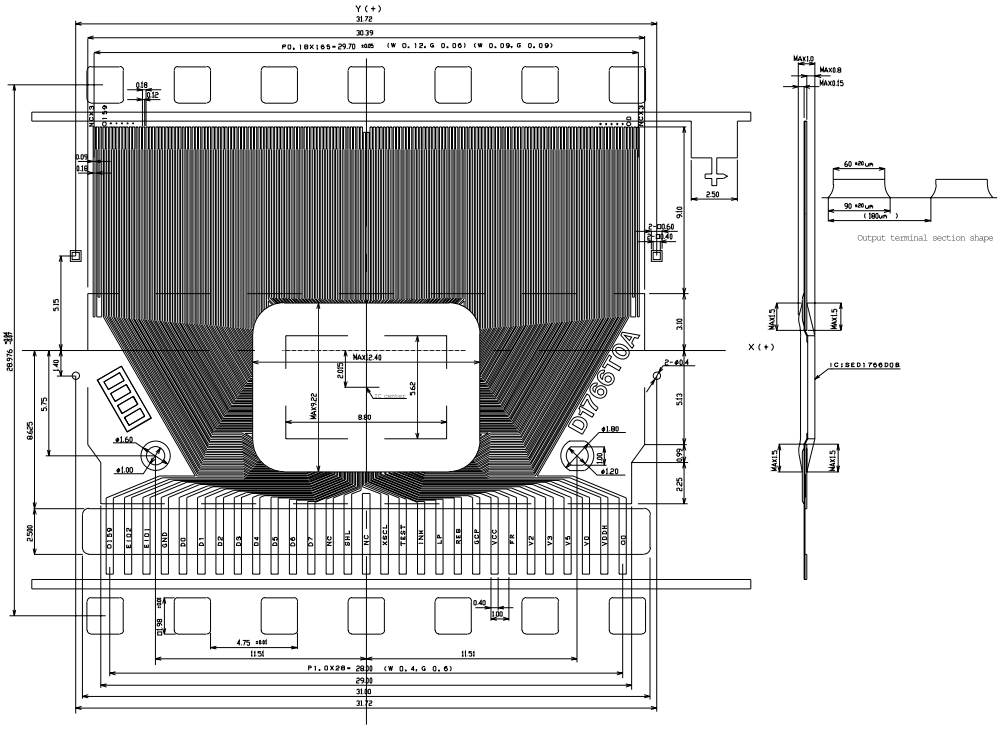
- **Large-screen LCD, 1/480 duty cycle**



9. DIMENSIONAL OUTLINE DRAWING

SED1766T0A

For reference



Unit: mm

12. SED1770
LCD Segment Driver

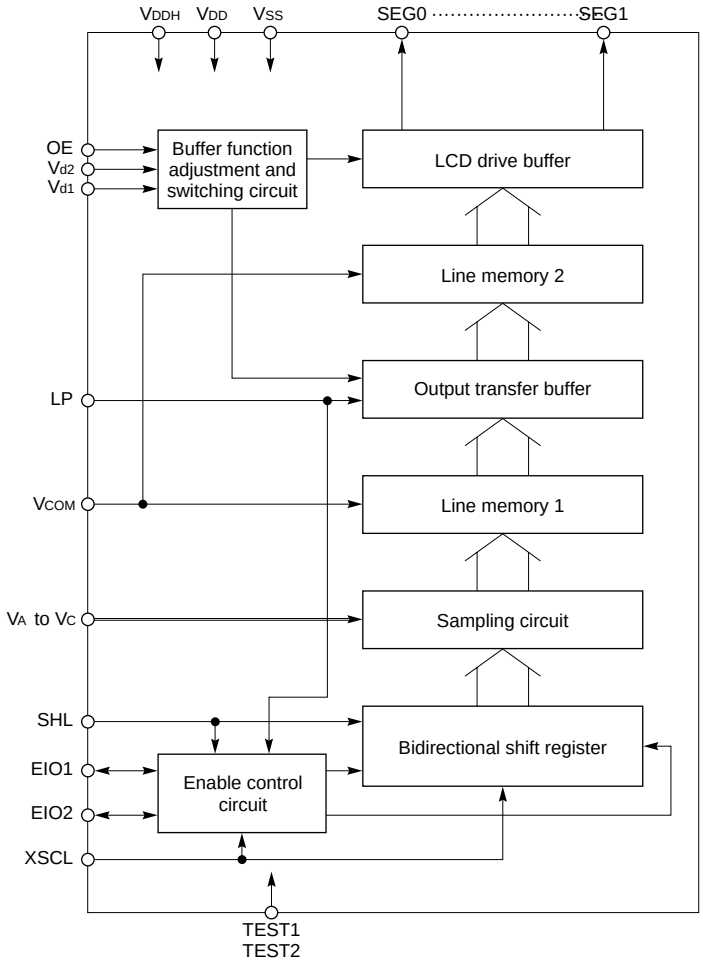
Contents

SED1770 series are segment driving LCD drivers used for the MIM liquid crystal analog grayscale and TFT liquid crystal panels. It outputs voltage having the same level as that of analog input signal.

FEATURES

- LCD drive outputs:
  160 for SED1770D0A
  162 (54 for each of R, G and B 54) for SED1771D0A
- LCD drive supply voltage range: +5V to +17V
- Operating frequency: 10MHz, maximum.
- Output load capacity: 200pF, maximum.
- Bidirectional shift register
- Cascade connection and low-power realized by employment of the automatic enable transfer function (this supersedes the enable signal generation using the controller)
- Logic operation power: 5.0V ± 10%
- CMOS silicon gate process
- The following switching is now available through the Al master slice
  - 160 outputs/162 outputs
  - 1:1 and 1:3 correspondence between shift register and analog switch
- Package: Shipped as chip (with Au bump)

BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Power</th><th>No. of pins</th></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Shift register data input/output.
Connected to the succeeding EIO in the cascade connection.
Changes at the XSCL rising edge.</td><td>V_{DD}
to
V_{SS}</td><td>2</td></tr>
<tr><td>XSCL</td><td>I</td><td>Clock signal input.
Actuates the shift register at rising and falling edge.</td><td>↑</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Display data clutch signal input.
Switches data at rising edge.</td><td>↑</td><td>1</td></tr>
<tr><td>OE</td><td>I</td><td>LCD drive buffer function switching signal input.
High-level: Large current driving
Low-level: Small current driving</td><td>↑</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift register direction select signal input.
<table>
<tr><th>SHL</th><th>EIO1</th><th>EIO2</th><th>SEG output</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td><td>0→1→2→ ⋯ 158→159</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td><td>159→158→ ⋯ 2→1→0</td></tr>
</table></td><td>↑</td><td>1</td></tr>
<tr><td>TEST1
TEST2</td><td>I</td><td>Test signal input. Normally Low-level is selected.
Pull down is not incorporated.</td><td>↑</td><td>2</td></tr>
<tr><td>V_{d1}
V_{d2}</td><td>I</td><td>Buffer function adjust signal input.
Function of the output transfer buffer and LCD drive buffer can be varied depending on the voltage applied to this pin.
V_{d1}: Selects the output transfer buffer function.
V_{d2}: Selects the LCD drive buffer function.</td><td>V_{DDH}
to
V_{SS}</td><td>2</td></tr>
<tr><td>V_A
V_B
V_C</td><td>I</td><td>Analog signal input.
Inputs image signals (R, G and B).</td><td>↑</td><td>3</td></tr>
<tr><td>SEG0
to
SEG159*</td><td>O</td><td>LCD drive segment output.
Used for sample holding the analog signal input (V_A, V_B and V_C) data to generate output matching to that level.
The following shows correspondence between the input and output:
$V_A \rightarrow$ SEG0, 3, 6, ⋯, $V_B \rightarrow$ SEG1, 4, 7, ⋯,
$V_C \rightarrow$ SEG2, 5, 8, ⋯.</td><td>↑</td><td>160</td></tr>
<tr><td>V_{COM}</td><td>I</td><td>Sample hold reference voltage input.
Reference power of the sample hold circuit.
Usually, center potential of analog signal inputs (V_A, V_B and V_C) is entered.</td><td>↑</td><td>1</td></tr>
<tr><td>V_{DDH}</td><td>P</td><td>High tension resistant supply terminal on LSI.
V_{DDH} pins are connected each other externally.</td><td>—</td><td>2</td></tr>
<tr><td>V_{DD}</td><td>P</td><td>LSI logic operation power supply terminal.</td><td>—</td><td>1</td></tr>
<tr><td>V_{SS}</td><td>P</td><td>LSI common GND.
V_{SS} pins are connected each other externally.</td><td>—</td><td>3</td></tr>
</table>

Total number of pins: 183

(NC: 3)

(*) SED1771D0A has 162 outputs and 161 SEGs, so 2 more pins are added.

PAD

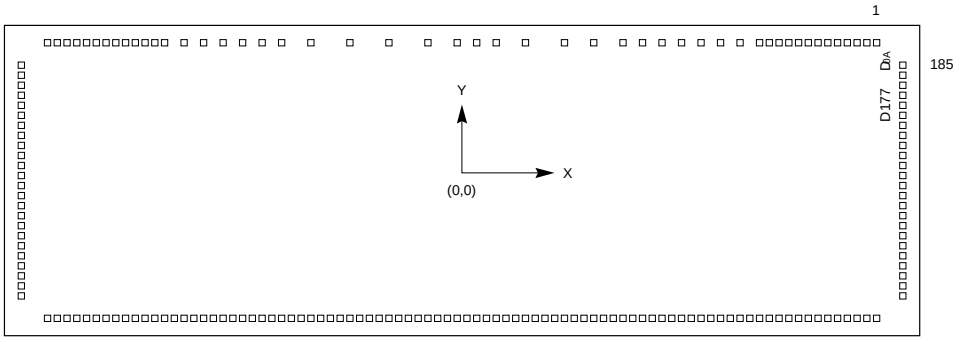
Pad Layout

Chip size: 11.27mm × 3.79mm
Pad pitch: 0.12mm (minimum)

* For Au bump specification
Chip thickness: 0.525mm ± 0.025mm

	X	Y	PAD No
Bump size A:	350µm ×	150µm ± 20µm	23, 24, 28, 29, 30, 31
Bump size B:	200µm ×	150µm ± 20µm	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 32, 33, 34, 35, 36, 37
Bump size C:	95µm ×	150µm ± 20µm	Other than the above

(In the above, X is assumed for the direction in parallel with the scribe line.)



Pad Coordinate

Unit: μm

PAD No.	PIN Name	X	Y
1	SEG148	5210	1699
2	149	5090	1699
3	150	4970	1699
4	151	4850	1699
5	152	4730	1699
6	153	4610	1699
7	154	4490	1699
8	155	4370	1699
9	156	4250	1699
10	157	4130	1699
11	158	4010	1699
12	159	3890	1699
13	160*	3770	1699
14	161*	3650	1699
15	TEST1	3400	1699
16	OE	3150	1699
17	LP	2900	1699
18	XSCL	2650	1699
19	SHL	2400	1699
20	EIO2	2150	1699
21	EIO1	1900	1699
22	TEST2	1650	1699
23	V_{SS}	1270	1699
24	V_{DDH}	830	1699
25	V_{d1}	440	1699
26	V_{d2}	190	1699
27	V_{COM}	–60	1699
28	V_{SS}	–450	1699
29	V_{DD}	–890	1699
30	V_{DDH}	–1330	1699
31	V_{SS}	–1770	1699
32	V_A	–2150	1699
33	(N.C.)	–2400	1699
34	V_B	–2650	1699
35	(N.C.)	–2900	1699
36	V_C	–3150	1699
37	(N.C.)	–3400	1699
38	SEG0	–3650	1699
39	1	–3770	1699
40	2	–3890	1699
41	3	–4010	1699
42	4	–4130	1699
43	5	–4250	1699
44	6	–4370	1699
45	7	–4490	1699
46	8	–4610	1699
47	9	–4730	1699
48	10	–4850	1699
49	11	–4970	1699
50	12	–5090	1699
51	13	–5210	1699
52	14	–5436	1343
53	15	–5436	1223
54	16	–5436	1103
55	17	–5436	983
56	18	–5436	863
57	19	–5436	743
58	20	–5436	623
59	21	–5436	503
60	22	–5436	383
61	23	–5436	263
62	24	–5436	143
63	SEG25	–5436	23
64	26	–5436	–97
65	27	–5436	–217
66	28	–5436	–337
67	29	–5436	–457
68	30	–5436	–577
69	31	–5436	–697
70	32	–5436	–817
71	33	–5436	–937
72	34	–5436	–1057
73	35	–5436	–1177
74	36	–5436	–1297
75	37	–5436	–1417
76	38	–5100	–1699
77	39	–4980	–1699
78	40	–4860	–1699
79	41	–4740	–1699
80	42	–4620	–1699
81	43	–4500	–1699
82	44	–4380	–1699
83	45	–4260	–1699
84	46	–4140	–1699
85	47	–4020	–1699
86	48	–3900	–1699
87	49	–3780	–1699
88	50	–3660	–1699
89	51	–3540	–1699
90	52	–3420	–1699
91	53	–3300	–1699
92	54	–3180	–1699
93	55	–3060	–1699
94	56	–2940	–1699
95	57	–2820	–1699
96	58	–2700	–1699
97	59	–2580	–1699
98	60	–2460	–1699
99	61	–2340	–1699
100	62	–2220	–1699
101	63	–2100	–1699
102	64	–1980	–1699
103	65	–1860	–1699
104	66	–1740	–1699
105	67	–1620	–1699
106	68	–1500	–1699
107	69	–1380	–1699
108	70	–1260	–1699
109	71	–1140	–1699
110	72	–1020	–1699
111	73	–900	–1699
112	74	–780	–1699
113	75	–660	–1699
114	76	–540	–1699
115	77	–420	–1699
116	78	–300	–1699
117	79	–180	–1699
118	80	–60	–1699
119	81	60	–1699
120	82	180	–1699
121	83	300	–1699
122	84	420	–1699
123	85	540	–1699
124	86	660	–1699
125	SEG87	780	–1699
126	88	900	–1699
127	89	1020	–1699
128	90	1140	–1699
129	91	1260	–1699
130	92	1380	–1699
131	93	1500	–1699
132	94	1620	–1699
133	95	1740	–1699
134	96	1860	–1699
135	97	1980	–1699
136	98	2100	–1699
137	99	2220	–1699
138	100	2340	–1699
139	101	2460	–1699
140	102	2580	–1699
141	103	2700	–1699
142	104	2820	–1699
143	105	2940	–1699
144	106	3060	–1699
145	107	3180	–1699
146	108	3300	–1699
147	109	3420	–1699
148	110	3540	–1699
149	111	3660	–1699
150	112	3780	–1699
151	113	3900	–1699
152	114	4020	–1699
153	115	4140	–1699
154	116	4260	–1699
155	117	4380	–1699
156	118	4500	–1699
157	119	4620	–1699
158	120	4740	–1699
159	121	4860	–1699
160	122	4980	–1699
161	123	5100	–1699
162	124	5436	–1417
163	125	5436	–1297
164	126	5436	–1177
165	127	5436	–1057
166	128	5436	–937
167	129	5436	–817
168	130	5436	–697
169	131	5436	–577
170	132	5436	–457
171	133	5436	–337
172	134	5436	–217
173	135	5436	–97
174	136	5436	23
175	137	5436	143
176	138	5436	263
177	139	5436	383
178	140	5436	503
179	141	5436	623
180	142	5436	743
181	143	5436	863
182	144	5436	983
183	145	5436	1103
184	146	5436	1223
185	147	5436	1343

(*) Pins SEG160 and 161 are replaced by N.C with SED1770D0A.

BLOCK FUNCTIONS

Enable control circuit

When the enable signal is disabled, the internal clock signal is fixed to low-level to introduce the power save mode to the system.
When multiple segment drivers are used, respective EIO terminals of the drivers are cascade connected and EIO terminal of the first driver is connected to V_{SS}. If this setup is selected, sampling on the first driver starts from rising edge of XSCL. The enable control circuit automatically detects the end of 160 bit of data sampling and transfers the enable signal automatically. Thus, control signal from the control LSI is no more needed.
EIO output is reset by the LP input.

Shift register

It shifts the sampling signal upon entering the shift clock signal.
Shift direction is selected by the SHL input.

Sampling circuit

It starts sampling analog signals sequentially using the sampling signal from the shift register. The following shows correspondence between input and output in this procedure:
V_A to SEG0, 3, 6, ⋯ 159, V_B to SEG1, 4, 7, ⋯ 157, V_C to SEG2, 5, 8, ⋯ 158.

Line memory 1

Stores the analog data sampled by the sampling circuit.

Output transfer buffer

At rising edge of the LP, it transfers data in the line memory 1 to the line memory 2. And, at the same time, it switches the LCD drive output. When LP="H", XSCL="L" must be selected. Also, LP="L" must always be selected during the sampling.
This buffer function can be selected with V_{d1}.

Line memory 2

Retains the current LCD drive output voltage until it is switched to other voltage level.

LCD drive buffer

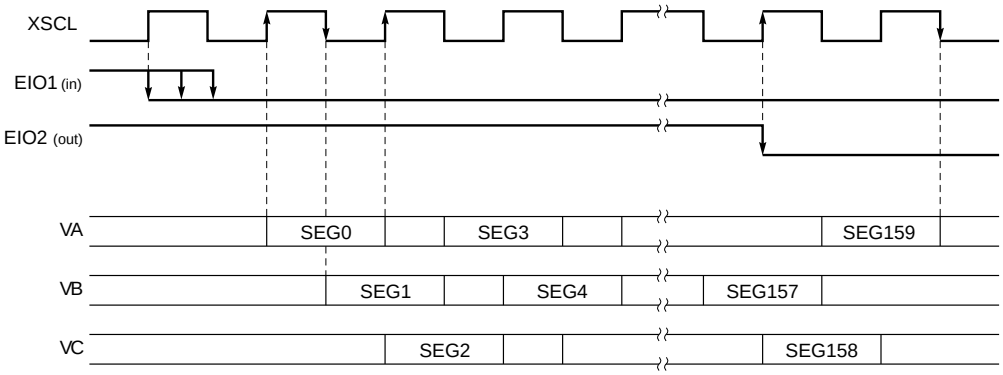
Outputs the LCD drive voltage.
This buffer function is adjusted with V_{d2} and switched with OE.

Buffer function adjustment and switching circuit

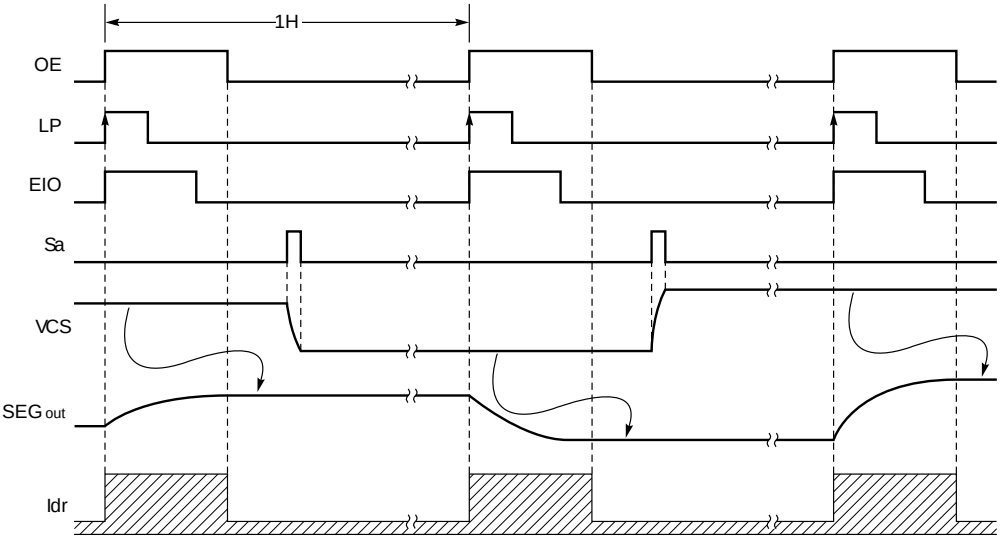
Used for selecting one of the two buffer functions. The buffer function goes minimum when both V_{d1} and V_{d2} set equal to V_{DDH}. Respective functions can be enhanced to support diverse LCD displays by lowering the potential.
Functional levels (output current) of the LCD driving buffer is switched with OE. When writing data to the panel, large current level is selected by setting OE="H". After the data has been written, it is driven with small current by selecting OE="L". This approach increases data write capability, prevents leakage during storage period and achieves low operating power.

Timing Chart

(When SHL="H", 160-output and 1:1 correspondence are specified)



Sampling starts from the XSCL rising edge that succeeds the EIO1 falling edge.



Sa: Sampling circuit analog switch input
V_{CS}: Potential on the sampling capacitor
I_{dr}: Magnitude of drive current

ABSOLUTE MAXIMUM RATING

(V_{SS} = 0V)

Items	Codes	Ratings	Units
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +25.0	V
Input pin voltage (Note 1)	V_{ID}	–0.3 to V_{DD} + 0.3	V
Input pin voltage (Note 2)	V_{IA}	–0.3 to V_{DDH} + 0.3	V
Storage temperature	Tstg	–65 to +150	°C
Operating temperature	Topr	–20 to +75	°C

Note 1: Applicable to EOI1, EOI2, XSCL, LP, OE, SHL, TEST1 and TEST2.
Note 2: Applicable to V_A, V_B, V_C, V_{d1}, V_{d2} and V_{COM}.

ELECTRIC CHARACTERISTICS

DC Characteristics

Except where otherwise specified, V_{SS} = 0V, V_{DD} = 5V ± 10%, V_{DDH} = 15V and Ta = –20 to +75°C are assumed.

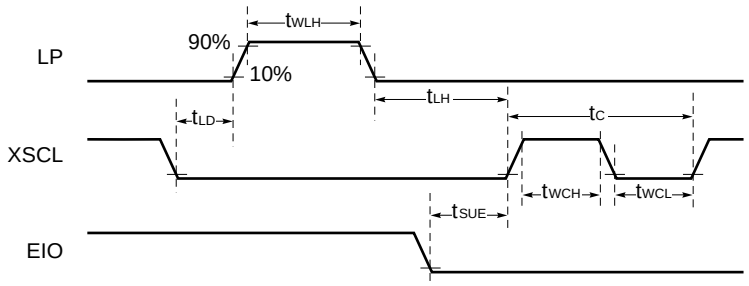
Item	Codes	Condition	Ratings			Unit	Applicable pins
			Min.	Typ.	Max.		
Supply voltage (1)	V_{DD}		4.5	—	5.5	V	V_{DD}
Supply voltage (2)	V_{DDH}		V_{DD}	—	17.0	V	V_{DDH}
High-level input voltage	V_{IH}		0.8 × V_{DD}	—	V_{DD}	V	Note 1
Low-level input voltage	V_{IL}		V_{SS}	—	0.2 × V_{DD}	V	
Input pin capacity	C_{ID}	Ta = 25°C	—	—	8.0	pF	Note 2
Input leak current	I_{LID}	0 < V_I < V_{DD}	—	—	2.0	µA	
High-level output voltage	V_{OH}	I_{OH} = –0.4mA	V_{DD} – 0.4	—	V_{DD}	V	
Low-level output voltage	V_{OL}	I_{OL} = 0.4mA	V_{SS}	—	0.4	V	EIO1
I/O pin capacity	$C_{I/O}$	Ta = 25°C	—	—	15.0	pF	EIO2
I/O leak current	$I_{LI/O}$	0 < V_I < V_{DD}	—	—	15.0	µA	
Analog input voltage	V_{video}		V_{SS} + 1.5	—	V_{DDH} – 1.5	V	V_A
Analog input capacity	C_{IA}		—	—	80	pF	V_B, V_C
Voltage deviation in outputs	dV_O		Max. – Min. = 100			mV	SEG0
I/O gain	G_V		95	—	105	%	to
"1" output current	I_{OH}	Note 3	—	0.1	—	mA	SEG161
"0" output current	I_{OL}	Note 4	—	0.1	—	mA	
Operating consumption (1)	I_{DD}	Note 5	—	—	5	mA	—
Operating consumption (2)	I_{DDH}	↑	—	—	15	mA	—

Note 1: EIO1, EIO2, XSCL, LP, OE, SHL, TEST1 and TEST2.
Note 2: XSCL, LP, OE, SHL, TEST1 and TEST2.
Note 3: V_{d2} = 12V, V_{video} = 13V and OE = "H".
Note 4: V_{d2} = 12V, V_{video} = 2V and OE = "H".
Note 5: f_{XSCL} = 10MHz, t_{IH} = 63.5µs, V_{video} = +2V to +13V, t_{OEH} (OE = "H") = 10µs and no load.

AC Characteristics

Except where otherwise specified, V_{SS} = 0V, V_{DD} = 5V ± 10%, V_{DDH} = 15V and Ta = –20 to +75°C are assumed.

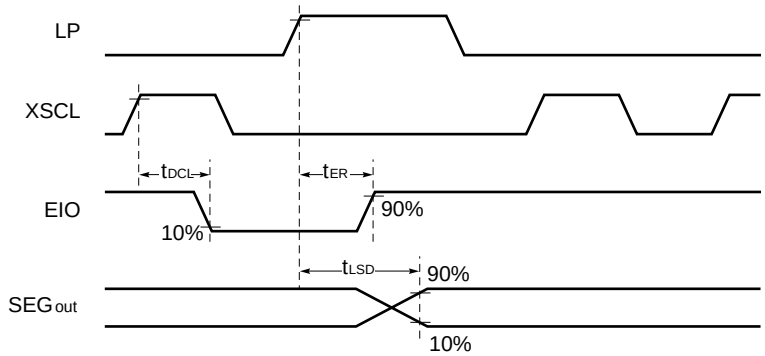
Input Timing Characteristics



Items	Codes	Conditions	Min.	Max.	Units
XSCL cycle	t_C		100	—	ns
XSCL High-level pulse width	t_{WCH}		40	—	ns
XSCL Low-level pulse width	t_{WCL}		40	—	ns
XSCL→LP rising time	t_{LD}		40	—	ns
LP pulse width	t_{WLH}	Note 1	2.5	—	µs
LP→XSCL time	t_{LH}		1	—	µs
EIO setup time	t_{SUE}		50	—	ns

Note 1: The time when XSCL is at low-level and LP is at high-level.

Output Timing Characteristics



Items	Codes	Conditions	Min.	Max.	Units
EIO output delay time	t_{DCL}	C_L = 15pF	—	40	ns
EIO output reset time	t_{ER}		—	120	ns
LP→SEGout delay time	t_{LSD}	V_{d1}, V_{d2} Note 1	—	15	µs

Note 1: $V_{d1} = V_{d2}$ = 12V, V_{video} = 2 to 13V, load capacity = 100pF and OE = "H".

AL MASTER SLICE

Al master slice of this LSI allows the following switching.

Switching among the number of output pins

160 outputs: Outputs EIO when sampling is done at SEG158. Where, SEG160 and 161 are replaced by N.C.

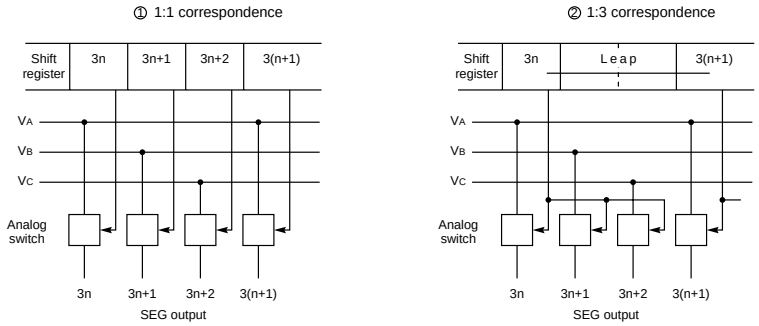
162 outputs: Outputs EIO when sampling is done at SEG160.

Note: In this case SHL is at high-level. When it is at low-level, the first output is SEG159 for ① and SEG161 for ②.

Correspondence between the product name

① The shift register and analog switch are coordinated one pair to one pair.

② Connect three analog switches to one stage of shift register, and operate the shift register every three stages.



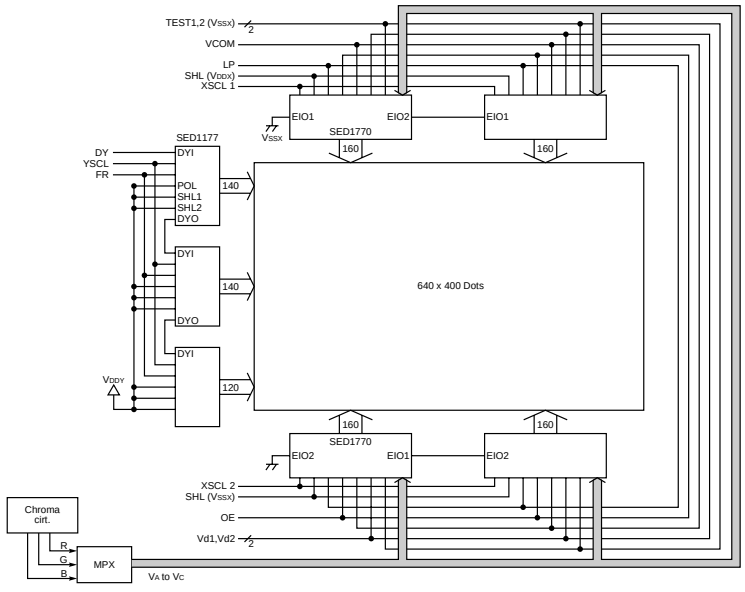
○ Correspondance to part name [n = 0 to 53]

SED1770D0A: ① 160 outputs, ② 1:1 correspondence is selected

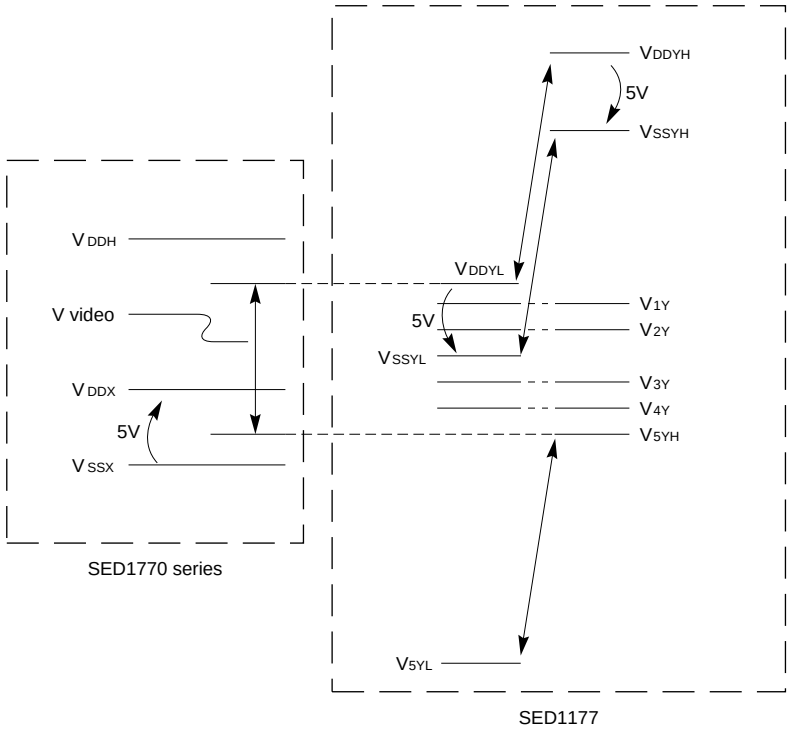
SED1771D0A: ① 162 outputs, ② 1:3 correspondence is selected

A SAMPLE CIRCUIT

Structural Diagram



Potential relations



The SED1177 power must be switched according to the video output range selected on the SED1770 series as shown below.

V_{DDYH}	⟺	V_{DDYL}
V_{SSYH}		V_{SSYL}
V_{5YH}		V_{5YL}

(V_{1Y}-V_{4Y} are common.)
Logic signal signal entered must corresponding to the respective potential level.

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