3. SED1743
LCD Driver

Contents

1. OVERVIEW

The SED1743 is an LCD common driver for high-resolution dot-matrix panels, which incorporates 160 row driver outputs. It is designed for use in conjunction with the SED1742 and SED1744 column drivers.

The SED1743 features a wide range of LCD drive voltages. The upper and lower drive voltages, V_0 and V_5, are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. As a result, the SED1743 is compatible with a large range of LCD panels.

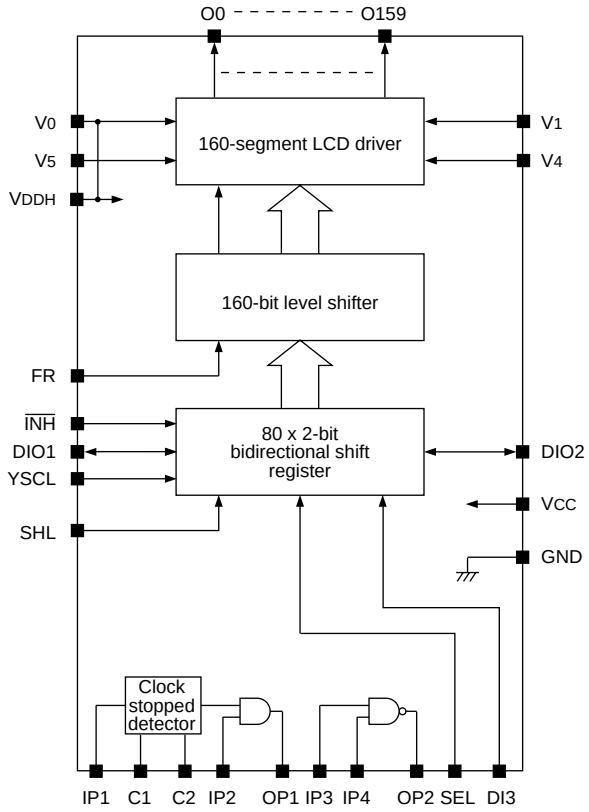
The SED1743 uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1743 operates from a 2.7 to 5.5 V supply and is available in both chip packages and tape-carrier packages (TCPs).

2. FEATURES

- 160 (80 × 2) LCD common drive outputs
- Pin-selectable output shift direction
- Adjustable LCD drive voltages
- Duty cycles up to 1/480
- Zero-bias display disable function
- Silicon-gate CMOS technology
- 1 kΩ typical output impedance
- 14 to 40 V LCD drive voltages
- 2.7 to 5.5 V supply
- Chip (SED1743D$_{1B}$) or tape-carrier packages (SED1743T$_{0A}$)

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

Number	Name	Description
39 to 183, 1 to 15	O0 to O159	LCD common drive outputs
16, 17	DIO2, DIO1	Serial data input/outputs
18	GND	Ground
19	SEL	Shift register mode select input
20	OP1	Clock monitor output
21	C1	First charge hold input. A capacitor should be connected between this pin and ground.
22	IP1	Halt detector clock input
23	C2	Second charge hold input. A resistor and capacitor should be connected between this pin and ground.
24	IP2	IP2 is connected to one input of an internal AND gate. The other input is connected to the halt detector output. Internal pulldown resistor
25	DI3	Scan pulse input when in 2×80 mode.
26	IP3	NAND gate input. Internal pulldown resistor
27	SHL	Shift direction select input
28	YSCL	Serial data shift clock. Negative-edge triggered.
29	IP4	NAND gate input
30	$\overline{\text{INH}}$	Display blanking input
31	OP2	NAND gate output
32	V_{CC}	Logic supply
33	FR	Common drive signal polarity select input
34 to 38	V_5, V_4, V_1, V_0 and V_{DDH}	Segment drive voltage inputs

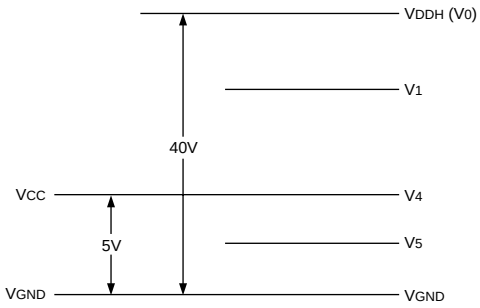
5. SPECIFICATIONS

5-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.3 to 7.0	V
	V_{DDH} (V_0)	–0.3 to 45.0	V
	V_1, V_4 and V_5	V_{GND} – 0.3 to V_{DDH} + 0.3	V
Input voltage range	V_I	V_{GND} – 0.3 to V_{CC} + 0.3	V
Output voltage range	V_O	V_{GND} – 0.3 to V_{CC} + 0.3	V
DIO output current	I_O	20	mA
Operating temperature range	Topg	–20 to 75	deg. C
Storage temperature range	Tstg	–65 to 150 (SED1743D$_{1B}$)	deg. C
		–55 to 100 (SED1743T$_{0A}$)	

Notes

1. Care should be taken during the power-on and power-off sequence. See Application Notes.
2. Display drive voltages should always be such that V_{DDH} (V_0) ≥ V_1 ≥ V_4 ≥ V_5 ≥ V_{GND} as shown in the following figure.



5-2 Recommended Operating Conditions

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	5	V
Segment driver supply voltage range	V_{DDH}	14 to 40	V

Ta = 25 deg. C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	2.7	V
Segment driver supply voltage range	V_{DDH}	14 to 28	V

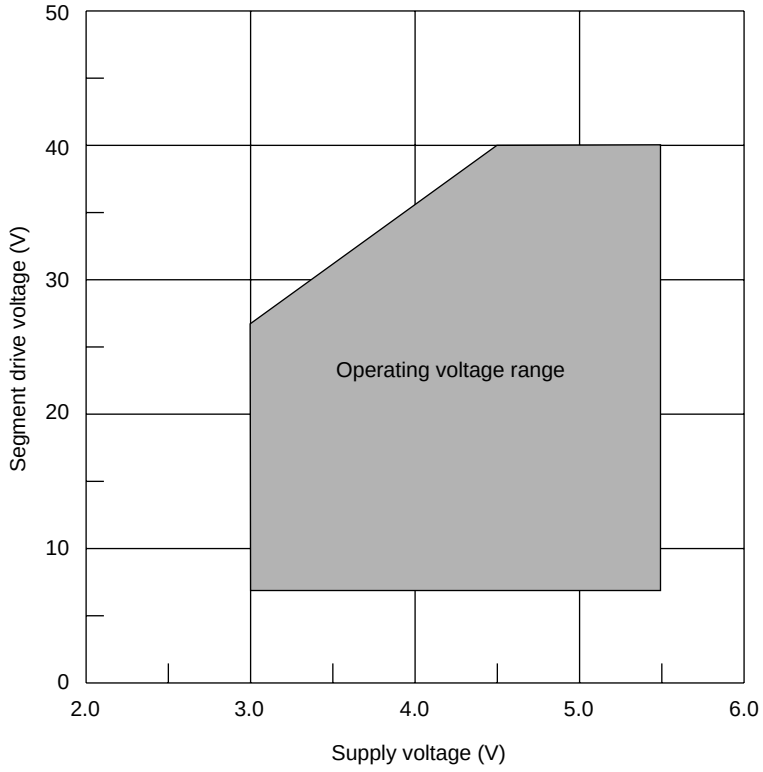
5-3 DC Electrical Characteristics

V_{CC} = 5 V ±10%, V_5 = 0 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
Quiescent current	I_{GND}	V_{DDH} = 14 to 40 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}		—	—	25	µA
Operating current	I_{CC}	V_{CC} = 5 V, V_{IH} = V_{CC}, V_{IL} = V_{GND}, f_{YSCL} = 33.6 kHz, frame frequency = 70 Hz, no load		—	9	20	µA
		V_{CC} = 2.7 V, other conditions as above		—	6	10	µA
	I_{DDH}	V_{CC} = 5 V, V_{DDH} = V_0 = 30 V, V_1 = 28 V, V_4 = 2 V, V_5 = 0 V, other conditions as for I_{CC}		—	18	40	µA
Segment driver input voltage	V_1			8/9V_{DDH}	—	V_{DDH}	V
	V_4, V_5			V_{GND}	—	1/9V_{DDH}	V
LOW-level input voltage	V_{IL}	V_{CC} = 2.7 to 5.5 V		—	—	0.2V_{CC}	V
HIGH-level input voltage	V_{IH}			0.8V_{CC}	—	—	V
LOW-level output voltage	V_{OL}	V_{CC} = 2.7 to 5.5 V	I_{OH} = 0.3 mA	—	—	0.4	V
HIGH-level output voltage	V_{OH}		I_{OH} = –0.3 mA	V_{CC} – 0.4	—	—	V
Segment ON resistance	R_{COM}	|ΔV_{ON}| = 0.5 V	V_{DDH} = 30 V	—	1.0	2.3	kΩ
			V_{DDH} = 20 V	—	1.2	2.8	
LOW-level input leakage current	I_{LI}	V_{GND} ≤ V_I ≤ V_{CC}		—	—	2	µA
HIGH-level input leakage current	I_{HI}	V_I ≤ V_{CC}		40	80	180	µA
Input/output leakage current	$I_{LI/O}$	V_{GND} ≤ V_{IN} ≤ V_{CC}		—	—	5	µA
Input capacitance	C_I	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	8	pF
Input/output capacitance	$C_{I/O}$	f = 1 MHz, Ta = 25 deg. C, chip package		—	—	15	pF

Operating voltage range

The maximum LCD supply voltage, V_{DDH}, depends on V_{CC}, as shown in the following figure.



5-4 AC Electrical Characteristics

Input timing

V_{CC} = 5 V ±10%, Ta = –20 to 75 deg. C

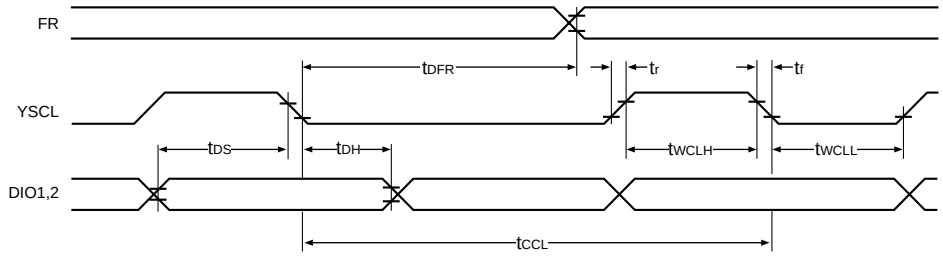
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL period	t_{CCL}		400	—	ns
YSCL HIGH-level pulsewidth	t_{WCLH}		70	—	ns
YSCL LOW-level pulsewidth	t_{WCHL}		330	—	ns
Data setup time	t_{DS}		100	—	ns

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
Data hold time	t_{DH}		40	—	ns
FR delay time	t_{DFR}		–300	300	ns
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_f		—	50	ns

V_{CC} = 2.7 to 4.5 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL period	t_{CCL}		800	—	ns
YSCL HIGH-level pulsewidth	t_{WCLH}		140	—	ns
YSCL LOW-level pulsewidth	t_{WCHL}		660	—	ns
Data setup time	t_{DS}		200	—	ns
Data hold time	t_{DH}		80	—	ns
FR delay time	t_{DFR}		–600	600	ns
Input signal rise time	t_r		—	100	ns
Input signal fall time	t_f		—	100	ns

Input timing waveform



Output timing

V_{CC} = 5 V ±10%, V_{DDH} = 14 to 40 V

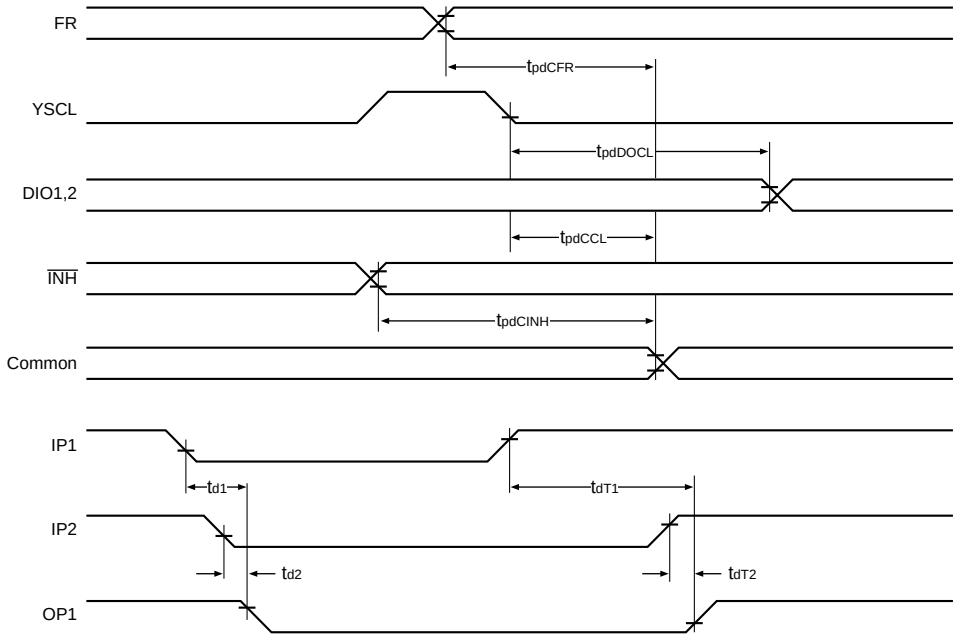
Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL to DIO delay time	t_{pdDOCL}	C_L = 15 pF	—	300	ns
YSCL to common output delay time	t_{pdCCL}	C_L = 100 pF	—	700	ns
INH common output delay time	t_{pdCINH}		—	700	ns
FR to common output delay time	t_{pdCFR}		—	700	ns
IP1 to OP1 delay time	t_{d1}	C_L = 15 pF	—	4C2R2	ns
IP1 to OP1 release time	t_{dT1}		—	$2t_{YD}$	ns
IP2 to OP1 delay time	t_{d2}		—	100	ns
IP2 to OP1 release time	t_{dT2}		—	100	ns

V_{CC} = 3.0 to 4.5 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
YSCL to DIO delay time	t_{pdDOCL}	C_L = 15 pF	—	600	ns
YSCL to common output delay time	t_{pdCCL}	C_L = 100 pF	—	1400	ns
INH common output delay time	t_{pdCINH}		—	1400	ns
FR to common output delay time	t_{pdCFR}		—	1400	ns
IP1 to OP1 delay time	t_{d1}	C_L = 15 pF	—	4C2R2	ns
IP1 to OP1 release time	t_{dT1}		—	$2t_{YD}$	ns
IP2 to OP1 delay time	t_{d2}		—	200	ns
IP2 to OP1 release time	t_{dT2}		—	200	ns

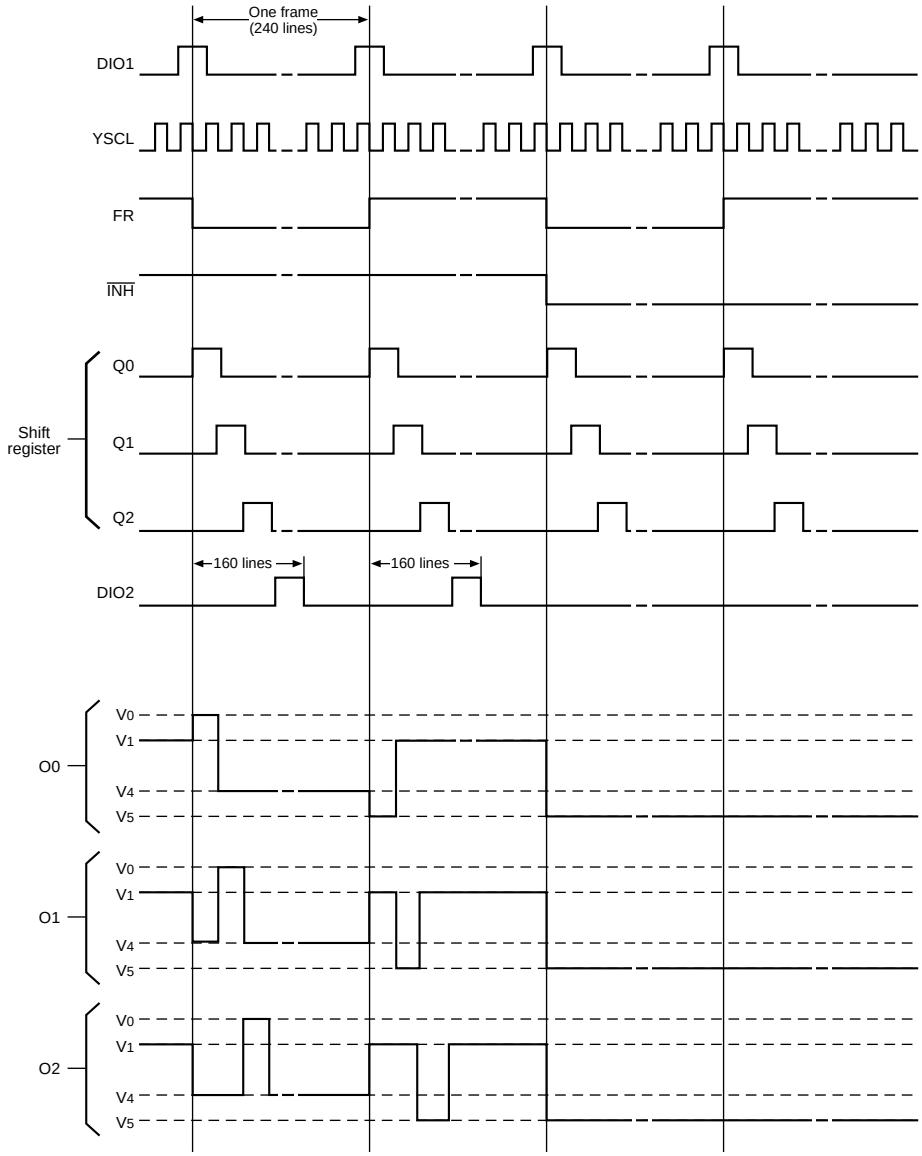
Note
YD is the scan start pulse. See the clock monitor circuit diagram for values of C2 and R2.

Output timing waveform



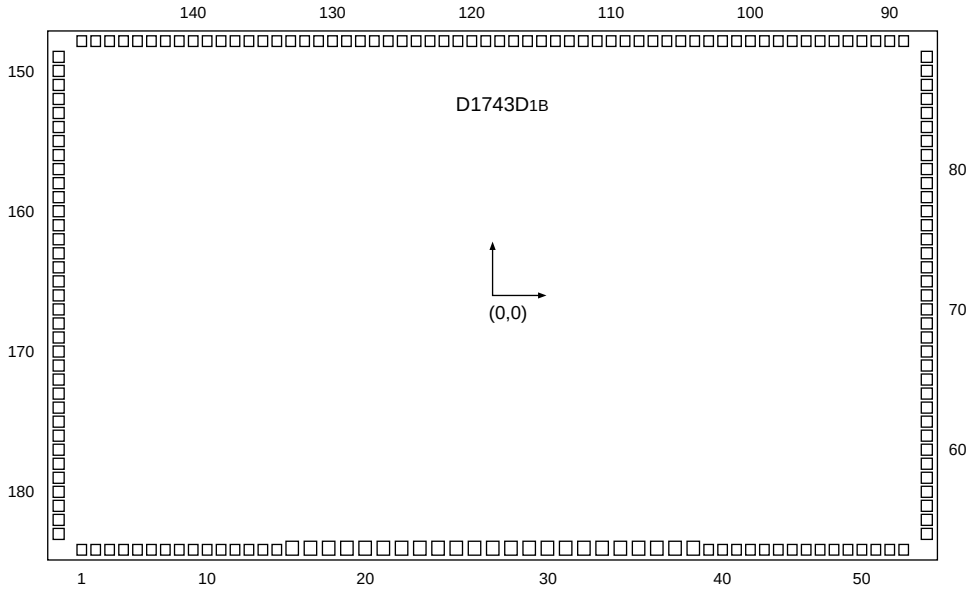
6. TIMING DIAGRAMS

1/240 Duty Cycle



7. PACKAGE DIMENSIONS

7-1 Chip Package (SED1743D1B)



- ❒ Chip size: 7.30 × 4.48 mm
- ❒ Chip thickness: 525 ±25 µm
- ❒ Pad pitch: 108 µm (Min.)
- ❒ Gold bump dimensions (SED1743D1B):
  - Size A: 94 × 134 ±20 µm (pads 1 to 15, 39 to 183)
  - Size B: 115 × 148 ±20 µm (pads 16 to 33 and 38)
  - Size C: 115 × 134 ±20 µm (pads 34 to 37)

Pad coordinates

Unit: μm

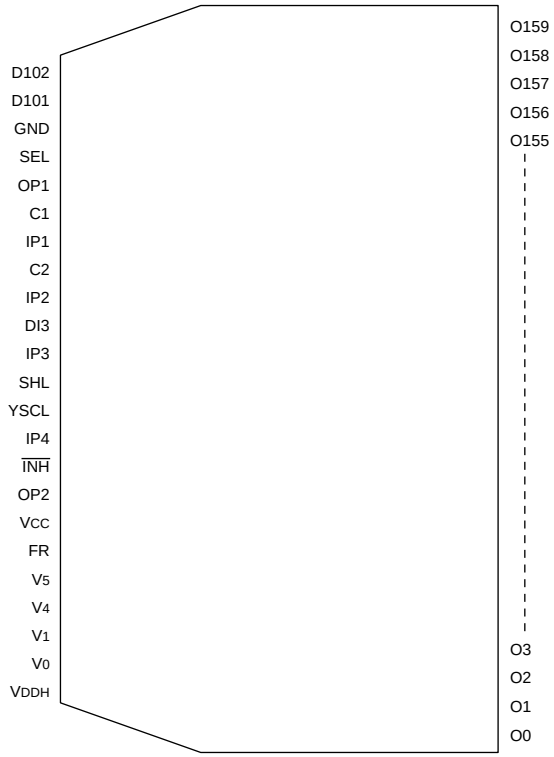
PAD No.	PAD Name	X	Y
1	O145	–3228	–2064
2	O146	–3120	↓
3	O147	–3012	
4	O148	–2903	
5	O149	–2795	
6	O150	–2687	
7	O151	–2578	
8	O152	–2470	
9	O153	–2362	
10	O154	–2253	
11	O155	–2145	
12	O156	–2037	
13	O157	–1929	
14	O158	–1820	
15	O159	–1712	
16	DIO2	–1550	–2058
17	DIO1	–1417	↓
18	GND	–1284	
19	SEL	–1151	
20	OP1	–1018	
21	C1	–885	
22	IP1	–752	
23	C2	–619	
24	IP2	–486	
25	DI3	–353	
26	IP3	–220	
27	SHL	–87	
28	YSCL	46	
29	IP4	179	
30	$\overline{\text{INH}}$	312	
31	OP2	445	
32	V_{CC}	578	
33	FR	711	
34	V_5	872	–2026
35	V_4	1034	↓
36	V_1	1195	
37	V_0	1357	
38	V_{DDH}	1550	–2058
39	O0	1712	–2064
40	O1	1820	↓
41	O2	1929	
42	O3	2037	
43	O4	2145	
44	O5	2253	
45	O6	2362	
46	O7	2470	
47	O8	2578	
48	O9	2687	
49	O10	2795	
50	O11	2903	
51	O12	3012	
52	O13	3120	
53	O14	3228	
54	O15	3474	–1841
55	O16	↓	–1733
56	O17		–1625
57	O18		–1516
58	O19		–1408
59	O20		–1300
60	O21		–1191
61	O22	↓	–1083

PAD No.	PAD Name	X	Y
62	O23	3474	–975
63	O24	↓	–866
64	O25		–758
65	O26		–650
66	O27		–542
67	O28		–433
68	O29		–325
69	O30		–217
70	O31		–108
71	O32		0
72	O33		108
73	O34		217
74	O35		325
75	O36		433
76	O37		542
77	O38		650
78	O39		758
79	O40		866
80	O41		975
81	O42		1083
82	O43		1191
83	O44		1300
84	O45		1408
85	O46		1516
86	O47		1625
87	O48		1733
88	O49	↓	1841
89	O50	3195	2064
90	O51	3087	↓
91	O52	2978	
92	O53	2870	
93	O54	2762	
94	O55	2553	
95	O56	2545	
96	O57	2437	
97	O58	2328	
98	O59	2220	
99	O60	2112	
100	O61	2004	
101	O62	1895	
102	O63	1787	
103	O64	1679	
104	O65	1570	
105	O66	1462	
106	O67	1354	
107	O68	1245	
108	O69	1137	
109	O70	1029	
110	O71	921	
111	O72	812	
112	O73	704	
113	O74	596	
114	O75	487	
115	O76	379	
116	O77	271	
117	O78	162	
118	O79	54	
119	O80	–54	
120	O81	–162	
121	O82	–271	
122	O83	–379	↓

PAD No.	PAD Name	X	Y
123	O84	–487	2064
124	O85	–596	↓
125	O86	–704	
126	O87	–812	
127	O88	–921	
128	O89	–1029	
129	O90	–1137	
130	O91	–1245	
131	O92	–1354	
132	O93	–1462	
133	O94	–1570	
134	O95	–1679	
135	O96	–1787	
136	O97	–1895	
137	O98	–2004	
138	O99	–2112	
139	O100	–2220	
140	O101	–2328	
141	O102	–2437	
142	O103	–2545	
143	O104	–2653	
144	O105	–2762	
145	O106	–2870	
146	O107	–2978	
147	O108	–3087	
148	O109	–3195	↓
149	O110	–3474	1841
150	O111	↓	1733
151	O112		1625
152	O113		1516
153	O114		1408
154	O115		1300
155	O116		1191
156	O117		1083
157	O118		975
158	O119		866
159	O120		758
160	O121		650
161	O122		542
162	O123		433
163	O124		325
164	O125		217
165	O126		108
166	O127		0
167	O128		–108
168	O129		–217
169	O130		–325
170	O131		–433
171	O132		–542
172	O133		–650
173	O134		–758
174	O135		–866
175	O136		–975
176	O137		–1083
177	O138		–1191
178	O139		–1300
179	O140		–1408
180	O141		–1516
181	O142		–1625
182	O143		–1733
183	O144	↓	–1841

7-2 Tape-carrier Package

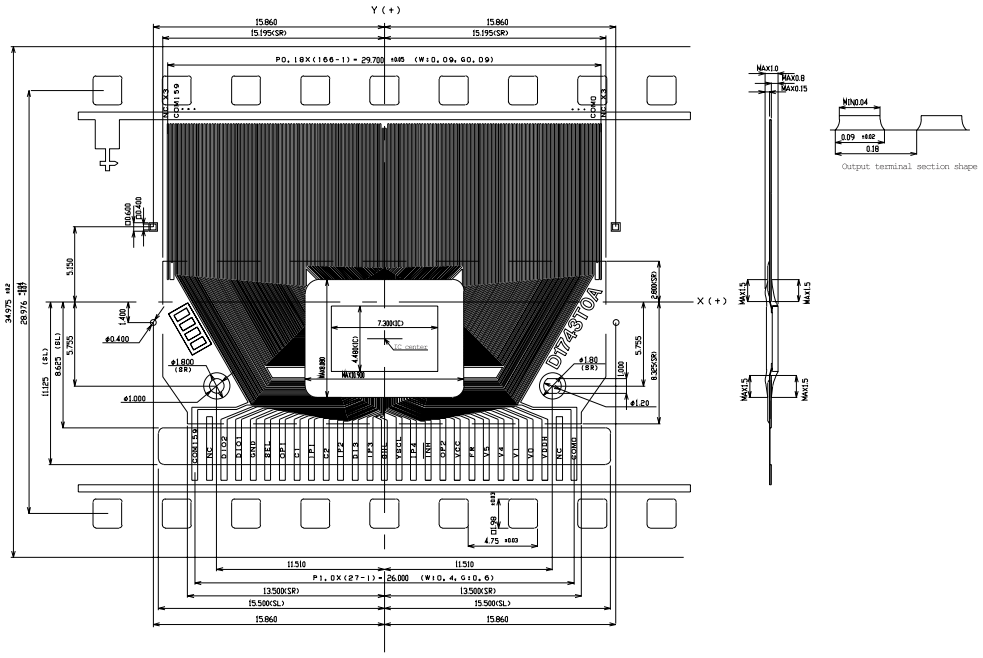
Tape-carrier pinout



Dimensional Outline Drawing

SED1743T0A

For reference



Unit: mm

8. FUNCTIONAL DESCRIPTION

8-1 Shift Register

The shift register is a bidirectional shift register, where the shift direction is selected by SHL. The effect of SHL on the shift direction and on the input data sequence is shown in table 1.

Table 1. Data sequence and shift direction

SHL	LCD outputs							Shift direction	
	O159	O158	O157	…	O2	O1	O0	DIO1	DIO2
L	a	b	c	…	x	y	z	Input	Output
H	z	y	x	…	c	b	a	Output	Input

SEL is used to select the operating mode of the shift register. When SEL is HIGH, 2×80 mode is selected. When SEL is LOW, 1×160 MODE mode is selected.

8-2 Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

8-3 LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in table 2.

Table 2. Driver output voltage

$\overline{INH}$	Input data	FR	Output voltage
H	H	H	V5
		L	V_0 (V_{DDH})
	L	H	V_1
		L	V_4
L	×	×	V_5

Note
× = don't care

8-4 Clock Monitor

The LCD panel can be damaged if a DC signal is applied to the segments. This situation can occur when the AC drive clock stops while power is applied to the display. The clock monitor circuit detects this condition and sends OP1 LOW. If OP1 is connected to $\overline{INH}$, the display is protected from damage. See Application Notes.

9. APPLICATION NOTES

9-1 Voltage Levels

The recommended method of generating the LCD drive voltages, V_0 to V_5, is with a voltage divider between V_{DDH} and V_{GND}, buffered with voltage followers.

The lower drive level, V_5, is not necessarily at V_{GND}, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V_5 and V_{GND} of 2.5 V is recommended since the driver efficiency decreases as the differential increases. Connect V_5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints as shown in the Typical Application circuit.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V_0) ≥ V_1 ≥ V_4 ≥ V_5 ≥ V_{GND} breaks down. A stabilized power supply may be required when using the resistor network.

9-2 Power-up and Power-down Precautions

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1743 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9 V, excess current will flow into the SED1743 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

Power-up sequence: Power should be applied to V_{CC} before, or at the same time as, power is applied to the driver circuitry.

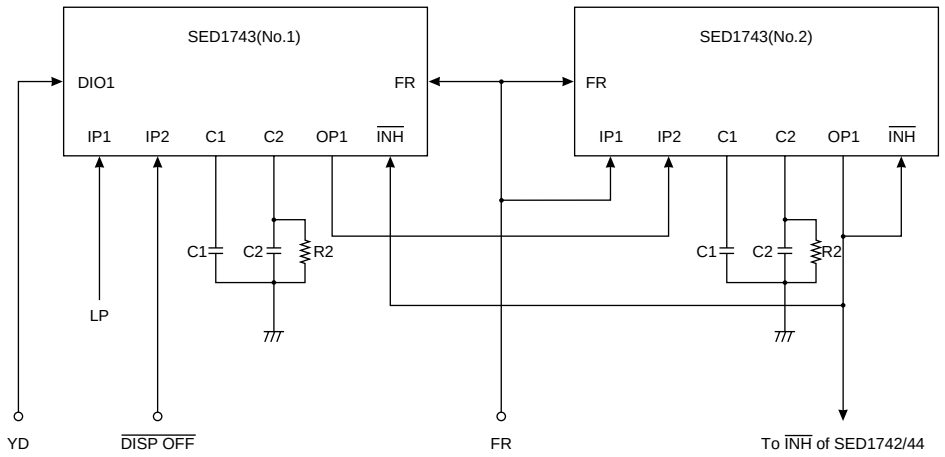
Power-down sequence: Power should be removed from V_{CC} after, or at the same time as, power is removed from the driver circuitry.

The SED1743 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. $\overline{INH}$ should be held LOW to hold the driver outputs at V_5 until the driver supplies have stabilized.

As an additional protective measure, insert a fast-blow fuse in series with the driver supply.

9-3 Clock Monitor Circuit

The clock monitor circuit sets OP1 LOW whenever the clock signals from the controller stops. Connecting OP1 to $\overline{INH}$ ensures that DC does not flow into the LCD panel.



R2 is typically several MΩ and C1 and C2 are determined while monitoring OP1. C1 should be much larger than C2. Typical values under various signal conditions are shown in table 3.

Table 3. Driver output voltage

Input signal	C1	C2	R2
LP	0.47 µF	0.047 µF	3.3 MΩ
FR	0.47 µF	0.047 µF	3.3 MΩ

Notes
YD: tc = 17.8 ms, duty = 0.14 %
LP: tc = 40.4 ms, duty = 0.35 %
FR: tc = 3.53 ms, duty = 50 %
When the clock monitor feature is not required, tie IP1, IP2, IP3 and C2 LOW, and leave OP1, OP2 and C1 OPEN.

10. TYPICAL APPLICATION