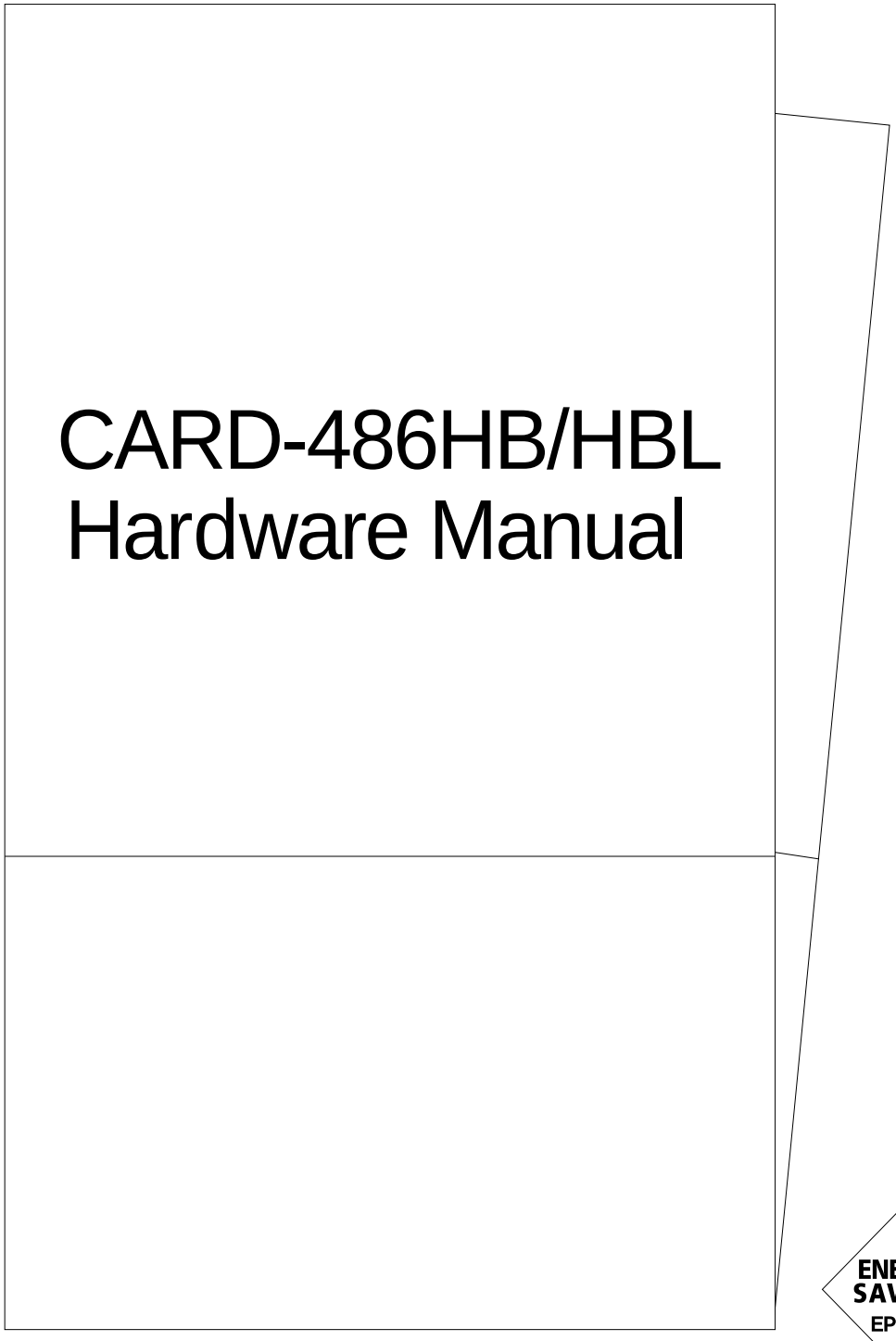
MF997-01

EPSON

CARD-486HB/HBL Hardware Manual



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1. BASIC SPECIFICATIONS

The SCE86436/SCE86406 Series (Card-486HB/486HBL) Card PCs have an ISA architecture card-sized main board. The basic configuration is described below. The CARD-486HB Card PC includes all of the functions listed below. The CARD-486HBL is a version of the CARD-486HB that does not include the video and FDC functions.

CPU

Intel 486SXSF 16MHz/33MHz (Intel)

I/O block

SPC8210 (Seiko-Epson)
SPC8221 (Seiko-Epson)
- Interrupt controller (82C59A-equivalent × 2)
- Programmable timer (82C54-equivalent × 2)
- DMA controller (82C37A-equivalent × 2)
- Memory mapper (74LS612-equivalent)
- Parallel I/O port
- Serial I/O port (16550-equivalent × 2)
- Real-time clock (146818-equivalent)
- IDE interface
  - Supports large-capacity IDE HDD (8.4GB)

Memory

- DRAM 1MB/4MB
- Flash ROM (for BIOS) 256K

Keyboard interface

8042 software emulation
- PS/2-style keyboard
- PS/2-style mouse

Video (This function is not included in the CARD-486HBL.)

SPC8110 (Seiko-Epson)
- CRT (800 × 600)
- STN mono/color (Single/Dual Panel) (800 × 600)
- TFT color (800 × 600)
- VRAM: 512K

FDC (This function is not included in the CARD-486HBL.)

- SPC2052 (Seiko-Epson)
- μPD765-equivalent
- Support for two drives
- Transfer speeds: 250kbps, 300kbps, 500kbps

CARD486HB Product List

Model No	CPU Clock	RAM
SCE8643600	16 MHz	1MB
SCE8643603	16 MHz	4MB
SCE8643605	33 MHz	4MB

CARD486HBL Product List

Model No	CPU Clock	RAM
SCE8640600	16 MHz	1MB
SCE8640603	16 MHz	4MB

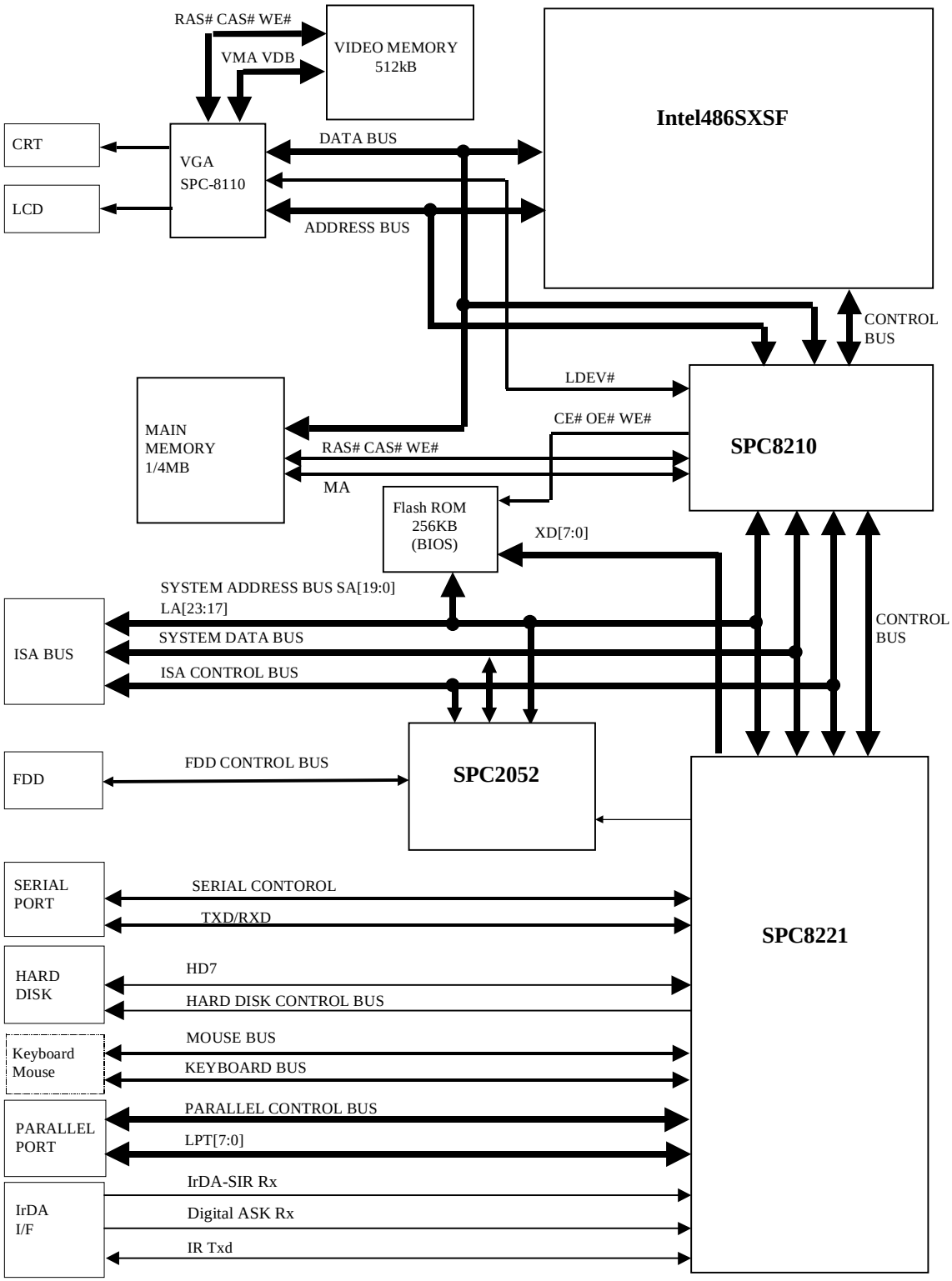
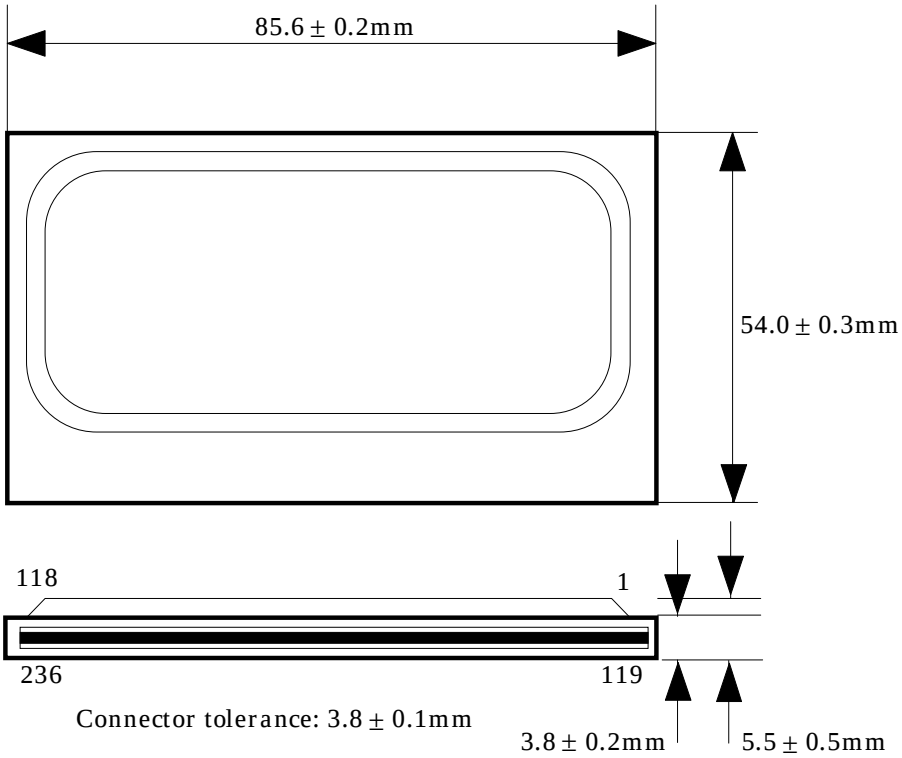


Figure 1.1 Block Diagram

2. PHYSICAL SPECIFICATIONS

2.1 Dimensions

85.6mm × 54.0mm × 5.5mm



2.2 Weight

About 38g

2.3 Installation Method

The SEK6669P01 (without ejector) and SEK6669P02 (with ejector) card-accepting connectors can be used.
The board on which the accepting connectors are to be mounted must be no more than 1.6mm thick.
The accepting connectors should be held in place with screws.
(Screw: M2.5 × 8 with hex nut)

CAUTION

During and just after use, the Card PC can get hot enough to burn you, so please observe the following precautions carefully:

- Make sure to advise anyone who could touch the Card PC, such as a service technician, that it gets very hot.
- If necessary to protect users, attach a notice about high temperature on the visible part of the Card PC.
- If necessary to protect users, make a cover to prevent anyone from touching the Card PC.

3. PIN CONFIGURATION

CARD-486HB Pin Configuration

1	GND	119	GND
2	GND	120	GND
3	EXDOTCLK	121	FPDOTCLK
4	LD6	122	LD7
5	LD4	123	LD5
6	LD2	124	LD3
7	LD0	125	LD1
8	FPVTIM	126	FPHTIM
9	FPAC	127	LD8
10	FPVCCON	128	FPVEEON
11	LD9	129	BLANK#
12	LD11	130	LD10
13	LD13	131	LD12
14	LD15	132	LD14
15	BLUE	133	BRTN
16	GREEN	134	GRTN
17	RED	135	RRTN
18	VSYNC	136	HSYNC
19	LD17	137	LD16
20	RESERVE	138	RESERVE
21	MSDATA	139	MSCLK
22	KBDATA	140	KBCLK
23	FDWP#	141	FDRD#
24	FDINDEX#	142	FDDCHG#
25	FDTRK0#	143	FDWE#
26	FDWD#	144	FDHIDEN
27	VCC5	145	VCC5
28	VCC5	146	VCC5
29	VCC3	147	VCC3
30	VCC3	148	VCC3
31	FDDS2#	149	FDDS1#
32	FDMT2#	150	FDMT1#
33	FDSIDE	151	FDSTEP#
34	FDDIR	152	RESERVE
35	RESERVE	153	DARX
36	COMBDTR#	154	COMBRI#
37	COMBCTS#	155	COMBRXD
38	COMBRTS#	156	COMBTXD
39	COMBDSR#	157	COMBDCD#
40	COMADTR#	158	COMARI#

41	COMACTS#	159	COMARXD
42	COMARTS#	160	COMATXD
43	COMADSR#	161	COMADCD#
44	IRRX	162	IRTX
45	LPTSTROBE#	163	LPTAFD#
46	LPTD0	164	LPTERROR#
47	LPTACK#	165	LPTBUSY
48	LPTPE	166	LPTSLCT
49	LPTD1	167	LPTINIT#
50	LPTD2	168	LPTSLCTIN#
51	LPTD3	169	LPTD4
52	LPTD5	170	LPTD6
53	LPTD7	171	LPTDIR
54	HDIR	172	HD7
55	HDENL#	173	HDENH#
56	HDCS0#	174	HDCS1#
57	SUSSTAT#	175	VBK
58	BATLOW#	176	EXTSMI#
59	GND	177	GND
60	GND	178	GND
61	BATWRN#	179	RESERVE
62	PWRGOOD	180	SRBTN#
63	SPKOUT	181	WDTIM#
64	FLOAT#	182	PGM
65	ROMCE0#	183	RESERVE
66	RESERVE	184	RESERVE
67	SD7	185	RESETDRV
68	SD6	186	IOCHCK#
69	SD5	187	IRQ9
70	SD4	188	DRQ2
71	SD3	189	WS0#
72	SD2	190	SMEMW#
73	SD1	191	SMEMR#
74	SD0	192	IOW#
75	IOCHRDY	193	IOR#
76	AEN	194	DACK3#
77	SA19	195	DRQ3
78	SA18	196	DACK1#
79	SA17	197	DRQ1
80	SA16	198	REF#

81	SA15	199	SCLK
82	VCC3	200	VCC3
83	VCC3	201	VCC3
84	VCC5	202	VCC5
85	VCC5	203	VCC5
86	SA14	204	IRQ7
87	SA13	205	IRQ6
88	SA12	206	IRQ5
89	SA11	207	IRQ4
90	SA10	208	IRQ3
91	SA9	209	DACK2#
92	SA8	210	TC
93	SA7	211	BALE
94	SA6	212	OSC
95	SA5	213	MEMCS16#
96	SA4	214	IOCS16#
97	SA3	215	IRQ10
98	SA2	216	IRQ11
99	SA1	217	IRQ12
100	SA0	218	IRQ15
101	SBHE#	219	IRQ14
102	LA23	220	DACK0#
103	LA22	221	DRQ0
104	LA21	222	DACK5#
105	LA20	223	DRQ5
106	LA19	224	DACK6#
107	LA18	225	DRQ6
108	LA17	226	DACK7#
109	MEMR#	227	DRQ7
110	MEMW#	228	MASTER#
111	SD8	229	SD12
112	SD9	230	SD13
113	SD10	231	SD14
114	SD11	232	SD15
115	SMOUT3	233	SMOUT2
116	SMOUT1	234	SMOUT0
117	GND	235	GND
118	GND	236	GND

CARD-486HBL Pin Configuration

1	GND	119	GND
2	GND	120	GND
3	RESERVE	121	RESERVE
4	RESERVE	122	RESERVE
5	RESERVE	123	RESERVE
6	RESERVE	124	RESERVE
7	RESERVE	125	RESERVE
8	RESERVE	126	RESERVE
9	RESERVE	127	RESERVE
10	RESERVE	128	RESERVE
11	RESERVE	129	RESERVE
12	RESERVE	130	RESERVE
13	RESERVE	131	RESERVE
14	RESERVE	132	RESERVE
15	RESERVE	133	RESERVE
16	RESERVE	134	RESERVE
17	RESERVE	135	RESERVE
18	RESERVE	136	RESERVE
19	RESERVE	137	RESERVE
20	RESERVE	138	RESERVE
21	MSDATA	139	MSCLK
22	KBDATA	140	KBCLK
23	RESERVE	141	RESERVE
24	RESERVE	142	RESERVE
25	RESERVE	143	RESERVE
26	RESERVE	144	RESERVE
27	VCC5	145	VCC5
28	VCC5	146	VCC5
29	VCC3	147	VCC3
30	VCC3	148	VCC3
31	RESERVE	149	RESERVE
32	RESERVE	150	RESERVE
33	RESERVE	151	RESERVE
34	RESERVE	152	RESERVE
35	RESERVE	153	DARX
36	COMBDTR#	154	COMBRI#
37	COMBCTS#	155	COMBRXD
38	COMBRTS#	156	COMBTXD
39	COMBDSR#	157	COMBDCD#
40	COMADTR#	158	COMARI#

41	COMACTS#	159	COMARXD
42	COMARTS#	160	COMATXD
43	COMADSR#	161	COMADCD#
44	IRRX	162	IRTX
45	LPTSTROBE#	163	LPTAFD#
46	LPTD0	164	LPTERROR#
47	LPTACK#	165	LPTBUSY
48	LPTPE	166	LPTSLCT
49	LPTD1	167	LPTINIT#
50	LPTD2	168	LPTSLCTIN#
51	LPTD3	169	LPTD4
52	LPTD5	170	LPTD6
53	LPTD7	171	LPTDIR
54	HDIR	172	HD7
55	HDENL#	173	HDENH#
56	HDCS0#	174	HDCS1#
57	SUSSTAT#	175	VBK
58	BATLOW#	176	EXTSMI#
59	GND	177	GND
60	GND	178	GND
61	BATWRN#	179	RESERVE
62	POWERGOOD	180	SRBTN#
63	SPKOUT	181	WDTIM#
64	FLOAT#	182	PGM
65	ROMCE0#	183	RESERVE
66	RESERVE	184	RESERVE
67	SD7	185	RESETDRV
68	SD6	186	IOCHCK#
69	SD5	187	IRQ9
70	SD4	188	DRQ2
71	SD3	189	WS0#
72	SD2	190	SMEMW#
73	SD1	191	SMEMR#
74	SD0	192	IOW#
75	IOCHRDY	193	IOR#
76	AEN	194	DACK3#
77	SA19	195	DRQ3
78	SA18	196	DACK1#
79	SA17	197	DRQ1
80	SA16	198	REF#

81	SA15	199	SCLK
82	VCC3	200	VCC3
83	VCC3	201	VCC3
84	VCC5	202	VCC5
85	VCC5	203	VCC5
86	SA14	204	IRQ7
87	SA13	205	IRQ6
88	SA12	206	IRQ5
89	SA11	207	IRQ4
90	SA10	208	IRQ3
91	SA9	209	DACK2#
92	SA8	210	TC
93	SA7	211	BALE
94	SA6	212	OSC
95	SA5	213	MEMCS16#
96	SA4	214	IOCS16#
97	SA3	215	IRQ10
98	SA2	216	IRQ11
99	SA1	217	IRQ12
100	SA0	218	IRQ15
101	SBHE#	219	IRQ14
102	LA23	220	DACK0#
103	LA22	221	DRQ0
104	LA21	222	DACK5#
105	LA20	223	DRQ5
106	LA19	224	DACK6#
107	LA18	225	DRQ6
108	LA17	226	DACK7#
109	MEMR#	227	DRQ7
110	MEMW#	228	MASTER#
111	SD8	229	SD12
112	SD9	230	SD13
113	SD10	231	SD14
114	SD11	232	SD15
115	SMOUT3	233	SMOUT2
116	SMOUT1	234	SMOUT0
117	GND	235	GND
118	GND	236	GND

4. PIN FUNCTIONS

The pin functions are described below for each of the interfaces.
The abbreviations in the "Type" column have the following meanings:

I:	Input pin
O:	Output pin
O OD:	Output pin open-drain output
IO:	Input/output pin
IO OD:	Input/output pin open-drain output

4.1 ISA Bus

Pin Name	Type	Functions
SA[19:17] SA[16:0]	O IO	System Address Bus These signals are used to indicate memory and I/O device addresses on the bus. These address signals are latched and held by this system and are valid during the bus cycle. In addition, when using the master function, these signals are driven by the device on the IO channel.
LA[23:17]	IO	Latchable Address Bus These signals are output as the address specification for the memory device on the bus. Along with the address signals, these signals specify addresses in memory space of up to 16MB on the bus. These signals are not latched by this system.
SBHE#	IO	System Byte High Enable Active Low When active, this signal indicates transmission of the most significant 8 bits (SD[15:8]) on the system data bus.
SD[15:0]	IO	System Data Bus This 16-bit data bus is used in the transmission of data between memory on the bus and the CPU and IO devices.
IOR#	IO	I/O Read Active Low This signal gives an I/O device permission to drive data on the bus.
IOW#	IO	I/O Write Active Low This signal instructs an I/O device to accept data from the bus.
IOCS16#	I	I/O chip select 16 Active low This input is a signal that indicates to the system that the data transfer on the bus is a 16-bit I/O transfer. In this system, 16-bit I/O transfers are executed with one wait cycle as the default; if this signal is not active, I/O transfers are performed with an 8-bit, 4-wait I/O cycle.
MEMR#	IO	Memory read Active low This signal gives a memory device permission to drive data on the bus.
MEMW#	IO	Memory write Active low This signal instructs an I/O device to accept data from the bus.
SMEMW#	O	System memory write Active low This signal is active when a memory write cycle is started for the 0-1 MB memory space on the bus.
SMEMW#	O	System memory read Active low This signal is active when a memory read cycle is started for the 0-1 MB memory space on the bus.
MEMCS16#	I	Memory chip select 16 Active low This input signal is used by the system to recognize 16-bit memory transfers. If this signal is not active, transfers are performed with the default 8-bit, 4-wait memory cycle.
AEN	O	Address enable When this signal is active, the DMA controller within this system controls the address bus, data bus, read command, and write command.
DRQ[7:5,3:0] DRQ2	I IO	DMA request Active high DMA data transfer request signal sent to this system. DRQ2 is output when the internal FDC is enabled, input when disabled.
DACK[7:5,3:0]#	O	DMA acknowledge Active low Each of these signals indicates that bus control has been released to the corresponding DMA channel.
TC	O	Terminal count Active high In a DMA transfer cycle this signal indicates that the DMA transfer has completed.

Pin Name	Type	Functions
REF#	IO OD	Refresh Active low When this signal is active, it indicates that the bus refresh cycle has either been requested or is in progress.
MASTER#	I	Master Active low The external bus master makes this signal active in order to acquire the control authority of the bus. Before the external bus master makes this signal active, however, it must first make DRQn# active and then receive DACKn#.
SCLK	O	System clock 50% duty ISA basic clock.
OSC	O	Oscillator 14.3 MHz 50% duty clock output. This signal is not synchronized with the system clock.
IOCHCK#	I	I/O channel check Active low This signal is used to notify the CARD-PC that an unrecoverable error or a parity error was generated in memory or by an I/O device on the bus. This signal is processed as an NMI by the CARD-PC.
IOCHRDY	IO OD	I/O channel ready Active high This signal terminates the bus cycle. If memory or an I/O device on the bus wants to extend the bus cycle, it can extend the cycle by serching for an effective address and command and then setting this signal low. Until this signal goes high, the system will continue to insert waits in the cycle.
WS0#	I	Zero wait state Active low Make this signal active in order to terminate the bus cycle without any wait states.
RESETDRV	O	Reset drive Active high System initialization signal. Initialize devices on the bus by using this signal.
BALE	O	Buffered address enable Active high The SA[19:0] address line is latched internally according to this signal. When LA [23:17] are used on an IO channel, this signal used to latch those signals.This signal is high throughout the DMA cycle.
IRQ[15, 14, 9] IRQ12 IRQ[11,10,7:3]	I O IO	Interrupt request Active high Interrupt request signal sent to this system. With regard to IRQ12 a mouse is being used (cannot be disabled). IRQ[11,10,4,3] are I/O according to the serial port setting. IRQ[7,5] are I/O according to the parallel port setting. IRQ[6] is I/O according to the FDC setting.

4.2 LCD Interfaces

(This function is not included in the CARD-486HBL.)

Pin Name	Type	Functions
LD[17:0]	O	Display data for flat panel display. These signals convey the display data for a flat panel display, and the output format supports both a 640 × 480 resolution passive matrix monochrome display and a TFT color display. LD8 is only required for a TFT color display.
FPVTIM	O	Vertical display timing signal for a flat panel display. This signal gives the timing for the start of a frame.
FPHTIM	O	Horizontal display timing signal for a flat panel display. This signal gives the timing for the start of a scan line.
FPDOTCLK	O	Data shift clock signal for a flat panel display. This signal provides the shift clock for the display data.
EXDOTCLK	O	Specify Flat Panel Data Shift Clock (normally not used)
FPVCCON	O	Flat panel display power supply control signal. This signal provides the power on timing for a panel for which power on timing is prescribed.
FPVEEON	O	Flat panel display power supply control signal. This signal provides the power on timing for a panel for which power on timing is prescribed.
FPAC	O	Liquid crystal AC signal. This signal is used when a simple matrix monochrome display panel requires a crystal AC conversion signal.
BLANK#	O	Flat panel data blank signal Indicates the blanking interval in which data should not be displayed on a TFT panel. Normally this controls the display enable (DE) signal for a flat panel.

4.3 CRT Interfaces

(This function is not included in the CARD-486HBL.)

Pin Name	Type	Functions
VSYNC	O	Vertical display timing. This signal provides the vertical sync signal for a CRT.
HSYNC	O	Horizontal display timing. This signal provides the horizontal sync signal for a CRT.
RED	O	Analog Color signal
RRTN	--	Red return signal.
GREEN	O	Analog Color signal
GRTN	--	Green return signal.
BLUE	O	Analog Color signal
BRTN	--	Blue return signal.

4.4 IDE Interfaces

Pin Name	Type	Functions
HDCS0#	O	Hard disk chip select 0 Active low 1F0H-1F7H select signal.
HDCS1#	O	Hard disk chip select 0 Active low 3F6H-3F7H select signal.
HDENH#	O	Hard disk buffer enable low Active low This signal is active during all 16-bit accesses to the disk, and can be used for buffer control of data bits DATA8-15 of the IDE drive interface.
HDENL#	O	Hard disk buffer enable low Active low This signal is active during all disk cycles, and can be used for buffer control of data bits DATA0-7 of the IDE drive interface.
HD7	IO	Hard disk bit 7 Bit 7 of the data bus in the hard disk interface. Only this line is controlled within the system.
HDIR	O	Hard disk bus data direction Outout for direction control of hard disk data buffer. This signal is high during read cycle.

4.5 FDD Interfaces

(This function is not included in the CARD-486HBL.)

Pin Name	Type	Functions
FDDS1#	OD	Drive select 1 Active low Used as a select signal for drive 1.
FDDS2#	OD	Drive select 2 Active low Used as a select signal for drive 2.
FDMT1#	OD	Motor on 1 Active low Used as a motor on signal for drive 1.
FDMT2#	OD	Motor on 2 Active low Used as a motor on signal for drive 2.
FDSTEP#	OD	Step Active low Stepping pulse signal indicating the number of steps the head must move.
FDDIR	OD	Direction This signal indicates the seek direction. When low it indicates inward movement, and when high outward movement.
FDSIDE	OD	Side Head selection signal. When low it selects head 1, and when high head 2.
FDRD#	I	Read data Data input read from drive.
FDWD#	OD	Write data Data input written to drive.
FDWE#	OD	Write enable Active low This signal controls writing to the drive.
FDWP#	I	Write protect Active low This signal from the drive indicates that the disk in the drive is write-protected.
FDDCHG#	I	Disk change Active low This signal from the drive indicates that the disk has been removed from the drive.
FDINDEX#	I	Index Active low This is the index detection signal from the drive.
FDTRK0#	I	Track 0 Active low This signal is used to notify the system that the head has detected track 0.
FDHIDEN	OD	High density select Active high When high, this signal indicates high density. The drive uses this signal to determine whether or not to operate in high density mode.

4.6 Keyboard Interfaces

Pin Name	Type	Functions
KBCLK	IO OD	Keyboard clock Clock signal for a PS/2-style keyboard interface
KBDATA	IO OD	Keyboard data Data signal for a PS/2-style keyboard interface

4.7 Mouse Interfaces

Pin Name	Type	Functions
MSCLK	IO OD	Mouse clock Clock signal for a PS/2-style mouse interface
MSDATA	IO OD	Mouse data Data signal for a PS/2-style mouse interface

4.8 Parallel Interfaces

Pin Name	Type	Functions
LPTSTROBE#	IO OD	Line printer strobe Active low This signal is used as a strobe for a peripheral on the parallel interface to read the data. In the high-speed parallel port mode this signal is used to indicate a write cycle.
LPTAFD#	IO OD	Line printer auto feed Active low When this signal is active, a parallel printer inserts a line feed after every line. In high-speed parallel port mode, this signal is used as a data strobe. This signal can be used as a data latch signal during write cycles and as a buffer enable signal during read cycle.
LPTBUSY	I	Line printer busy Active high This signal indicates that the printer is not able to accept data from the system.
LPTACK#	I	Line printer acknowledge Active low This signal indicates that data transfer has been completed and also to prepare for the next transfer.
LPTERROR#	I	Line printer error Active low This signal notifies the system of errors in peripheral devices.
LPTPE	I	Line printer paper end Active high This signal notifies the system taht the printer is out of paper.
LPTINIT#	IO OD	Line printer initialize Active low Initialization signal for the printer.
LPTSLCTIN#	IO OD	Line printer select in Active low Used to select the perip heral device currently connected to the port. In high-speed parallel port mode, this signal is used as an address strobe.
LPTSLCT	I	Line printer selected Active high Status signal sent to the system by a peripheral device in order to confirm that the system has selected the device.
LPTDIR	O	Line printer direction This signal is used for direction control for external buffers. Ordinarily low in ISA mode.
LPTD[7:0]	IO	Line printer data bus Unidirectional in ISA mode, bidirectional in PS/2 mode.

4.9 Serial Interfaces

Pin Name	Type	Functions
COMADCD# COMBDCD#	I	Data carrier detect Active low This signal indicates that the modem or data terminal has detected the carrier.
COMADTR# COMBDTR#	O	Data terminal ready Active low This signal indicates that the controller is ready for data transmission with respect to the modem or data terminal.
COMADSR# COMBDSR#	I	Data set ready Active low This signal indicates that the modem or data terminal is ready for data transmission with respect to the controller.
COMARTS# COMBRTS#	O	Request to send Active low This signal indicates that the controller has transmission data ready, and indicates a request to transmit data with respect to the modem or data terminal.
COMACTS# COMBCTS#	I	Clear to send Active low This signal indicates that the modem or data terminal is ready to receive data in response to a data transmission request.
COMARI# COMBRI#	I	Ring indicator Active low This signal indicates that the modem or data terminal has detected a telephone ringing signal. Alternatively, this signal can be used in this system as a wake-up signal from the suspend state.
COMATXD COMBTXD	O	Serial data transmission This output is the asynchronous serial data.
COMARXD COMBRXD	I	Serial data receive This input is the asynchronous serial data.
IRTX	O	Ir data transmission Transmission data for infrared communications
IRRX	I	IrDA-SIR format data receive IrDA-SIR format input signal.
DARX	I	Digital ASK data receive Digital ASK format input signal.

4.10 Power Management

Pin Name	Type	Functions
BATLOW#	I	Battery low Active low This signal is used to indicate to the system that there is no battery capacity. A system management interrupt is executed when this signal goes active.
BATWRN#	I	Battery warning Active low This signal is used to indicate a battery capacity warning to the system. A system management interrupt is not executed when this signal goes active.
SUSSTAT#	O	Suspend status Active low This signal indicates that the system is in the suspended state.
SRBTN#	I	Suspend resume button This signal is a suspend and resume request signal with respect to the system. This signal is latched internally to the system on a falling edge.
EXTSMI#	I	External system management interrupt Active low Input of a system management interrupt from an external device.
SMOUT[3:0]	O	System management out These signals can be used for standby control of local devices (hard disk, serial driver/receiver) on the output terminals for local standby control.
POWERGOOD	I	Power good Active high This signal indicates that the system power supply is normal. System reset is done when this signal is low level. Refer to the section on AC characteristics.

4.11 ROM Update Interfaces

Pin Name	Type	Functions
FLOAT#	I	ROM update signal
PGM	---	ROM write power supply When FLASH ROM is being read, PGM should be connected to GND or VCC5. When FLASH ROM is being written, 12V±5%, 30mA current should be supplied to PGM. 12V power supply is supplied after VCC5 is fixed.
ROMCE0#	IO	ROM update signal

4.12 Speaker Interfaces

Pin Name	Type	Functions
SPKOUT	O	Speaker out This can be used as a digital output for a speaker.
WDTIM#	O	Watchdog timer out Active low Watchdog timer output

4.13 Power Supply

Pin Name	Type	Functions
VCC3	---	System power 3.3 V ± 0.3 V Power supply for internal circuits
VCC5	---	System power 5.0 V ± 5% Power supply for external interfaces
VBK	---	Backup power supply for real time clock When VCC5 is supplied, the same voltage as VCC5 should be supplied. When VCC5 is not supplied, a backup voltage should be supplied.
GND	---	System ground

5. DETAILED DESCRIPTION OF FUNCTIONS

5.1 System Overview

CARD-486HB/486HBL has a system configuration based on the ISA architecture. This section provides an overview of the system memory configuration and basic I/O.

5.1.1 Memory map

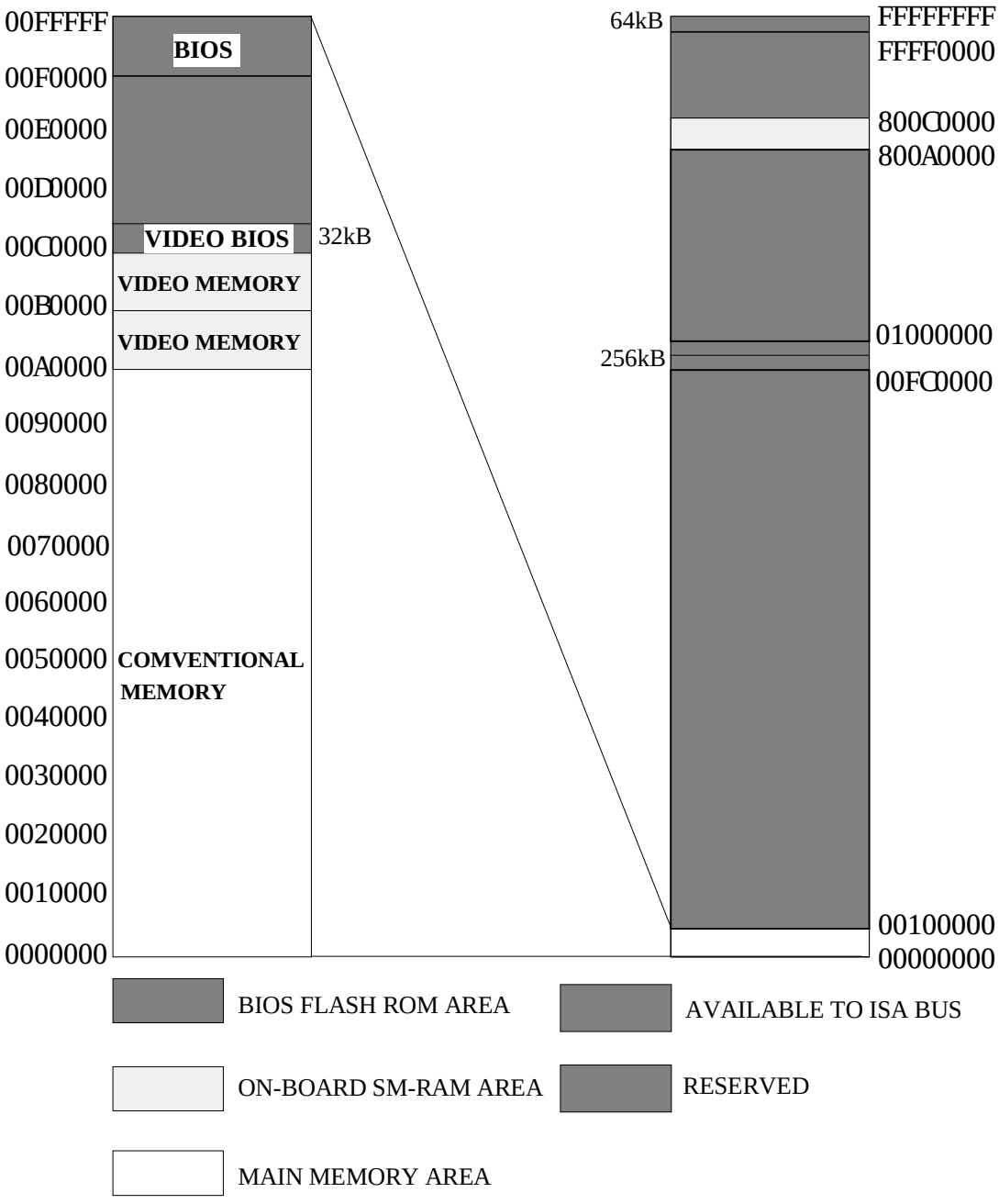


Fig. 5.1.1 System Memory Map (1MB)

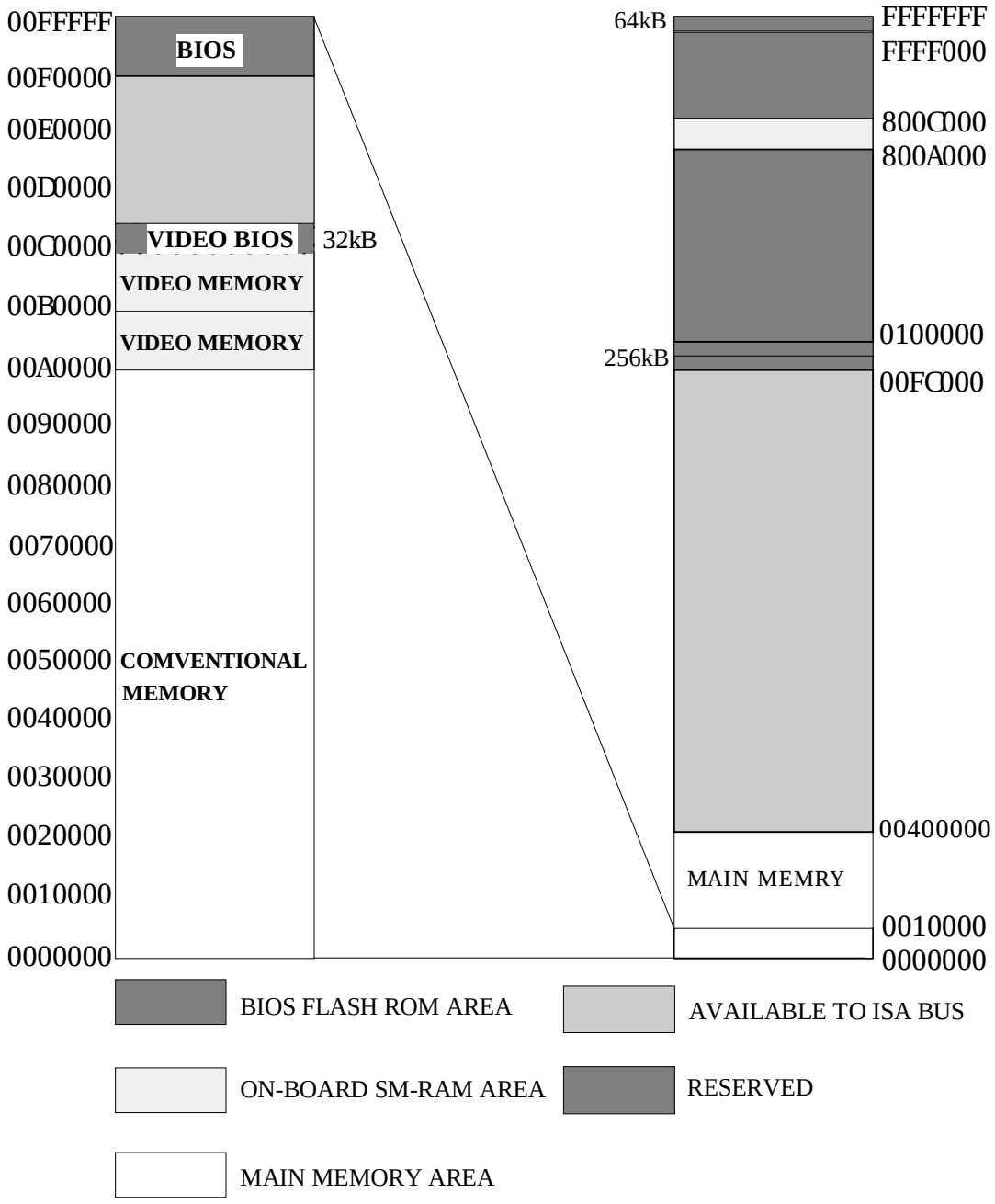


Fig. 5.1.2 System Memory Map (4MB)

Figures 5.1.1 and 5.1.2 depict the memory map. The CARD-486HB/486HBL has a 4GB memory space. Of this space, the lowest 16MB is open to the ISA bus. In addition, when accessing the CARD-486HB/486HBL's internal memory, the address is not output on the ISA bus, even if the address that is being accessed is within the ISA bus memory space.

The BIOS flash ROM space is mapped initially, but after initialization, the flash ROM is shadowed.

For details, refer to the Seiko Epson SPC 8210 manual.

5.1.2 DMA controllers

CARD-486HB/486HBL has two DMA controllers (equivalent to the 82C37A). The DMA channels in this system are shown in Table 5.1.1:

Controller 1

Channel number	Device allocated
CH0	Reserved
CH1	Reserved
CH2	Floppy disk
CH3	Reserved

Controller 2

Channel number	Device allocated
CH4	Cascade connection to controller 1
CH5	Reserved
CH6	Reserved
CH7	Reserved

Table 5.1.1 DMA Channels

Controller 1, which includes channels 0 to 3, is used for 8-bit data transfers. Between 8-bit I/O and 8-bit memory or 16-bit memory, transfer is possible in 8-bit units up to a block of 64K bytes.

Controller 2, which includes channels 4 to 7, is used principally for 16-bit data transfers, and since channel 4 is connected in cascade to controller 1 it is not available to the ISA bus. Channels 5 to 7 are available to the ISA bus, and can be used for 16-bit data transfers. In this case, between 16-bit I/O and 16-bit memory, transfer is possible in 16-bit units up to a block of 128K bytes.

The I/O addresses for the page registers used to support each DMA channel during DMA transfers are shown in Table 5.1.2. The DMA controllers have only 16-bit addressing capability, and these page registers are used to make up for this.

Page Registers	I/O Address(HEX)
DMA channel 0	0087h
DMA channel 1	0083h
DMA channel 2	0081h
DMA channel 3	0082h
DMA channel 5	008Bh
DMA channel 6	0089h
DMA channel 7	008Ah
Refresh	008Fh

Table 5.1.2 Page Register Address

Information relating to transfer timing is contained in the chapter on the ISA bus interface.

5.1.3 System interrputs and interrupt controller

The allocation of interrupts to causes in CARD-486HB/486HBL is as shown in the following table.

Level	Function
SMI	External system management interrupt Power management functions, keyboard emulation
NMI	Parity error or IOCHCK#
IRQ	Interrupts from the interrupt controller

The IRQ interrupts are interrupts from the interrupt controllers. The allocation of interrupt controller interrupts to causes in this system is as shown in the following table.

Interrupt Controller

Controller 1	Controller 2	Devices
IRQ0		Timer out 0
IRQ1		Keyboard
IRQ2		Cascade connection to controller 2
	IRQ8	Real time clock
	IRQ9	Coprocessor
	IRQ10	ISA or serial port
	IRQ11	ISA or serial port
	IRQ12	Mouse port
	IRQ13	ISA
	IRQ14	HDD
	IRQ15	ISA
IRQ3		Serial port 2 or ISA
IRQ4		Serial port 1 or ISA
IRQ5		Parallel port 2
IRQ6		FDD
IRQ7		Parallel port 1

5.1.4 Timer counter

The CARD-486HB/486HBL incorporates two 8254 equivalent timer-counters. Each has three independent timers. The following describes the applications of each and the inputs.

Timer 1

Channel 0	System timer
GATE0	Fixed at "ON"
CLK IN0	1.19 MHz
CLK OUT0	Connected to IRQ0 of interrupt controller 1

Channel 1	Refresh request
GATE1	Fixed at "ON"
CLK IN1	1.19 MHz
CLK OUT1	Refresh request

Channel 2	Speaker interface
GATE2	Controlled by port 61H
CLK IN2	1.19 MHz
CLK OUT2	Used to drive a speaker

Timer 2

Channel 0	SMI request
GATE0	Always on
CLK IN0	32 kHz
CLK OUT0	Used for SMI requests

Channel 1	Watchdog Out
GATE1	Always on
CLK IN1	4 kHz
CLK OUT1	Used for Watchdog Out

Channel 2	Power management alarm
GATE2	Controlled by Configuration Register
CLK IN2	1.19 MHz
CLK OUT2	Used for driving speaker interface

5.1.5 Real-time clock and CMOS RAM

CARD-486HB/486HBL has a real time clock which provides clock and calendar functions and CMOS RAM used to hold system configuration information. The real time clock is compatible with a 146818.

Power must be supplied constantly to the VBK pin in order to maintain the operation of the real time clock and the contents of CMOS RAM. When switching between the system power supply and the backup power supply, care is required to ensure that data is not lost. Care must be paid to the power supply sequence for the CARD-486HB/486HBL.

5.1.6 I/O MAP

I/O addresses 00h to 0FFh are allocated to basic I/O. The addresses from 100h to 3Fh are open to I/O channels, but caution is required when expanding I/O because the CARD-486HB/486HBL already have built-in I/O. The table below shows the I/O map. Note that the CARD-486HBL does not include VGA and FDC ports.

Address	Port	Register Name	Function
00h	00h RW	DMA Channel 0 base and current address	
	01h RW	DMA Channel 0 base and current word	
	02h RW	DMA Channel 1 base and current address	
	03h RW	DMA Channel 1 base and current word	
	04h RW	DMA Channel 2 base and current address	
	05h RW	DMA Channel 2 base and current word	
	06h RW	DMA Channel 3 base and current address	DMA Controller 1
	07h RW	DMA Channel 3 base and current word	82C37A Compatible
	08h WO	Command Resister	
	08h RO	Status Register	
	09h WO	Request Register	
	0Ah WO	Single-Mask Register	
	0Bh WO	Mode Register	
	0Ch WO	Clear Byte Pointer	
	0Dh RO	Master Clear	
	0Dh WO	Temporary Register	
	0Eh WO	Clear Mask Register	
0Fh	0Fh WO	Write all Mask Register	
10-1Fh		DMAC 1 Duplicated	
20h	20h WO	Initialization Control Word ICW1	
	20h WO	Operation Control Word OCW2	
	20h WO	Operation Control Word OCW3	
	20h RO	Interrupt Service Resister	
	20h RO	Interrupt Request Resister	Interrupt Controller 1
21h	21h WO	Initialization Control Word ICW2	82C59A Compatible
	21h WO	Initialization Control Word ICW3	
	21h WO	Initialization Control Word ICW4	
	21h RW	Operation Control Word OCW1	
	21h RW	Interrupt Mask Resister	
22-3Fh		Interrupt Controller 1 Duplicated	
40h	40h RW	Channel 0 Count	
	41h RW	Channel 1 Count	Timer Counter 1
	42h RW	Channel 2 Count	(8254 Compatible)
43h	43h RW	Command Register	
44-47h		Timer Counter 1 Duplicated	
48h	48h RW	Channel 0 Count	Timer Counter 2
	49h RW	Channel 1 Count	(8254 Compatible)
	4Ah RW	Channel 2 Count	
4Bh	4Bh RW	Command Register	
4C-4Fh		Timer Counter 2 Duplicated	
50-53h		Timer Counter 1 Duplicated	
54-57h		Timer Counter 1 Duplicated	
58-5Bh		Timer Counter 2 Duplicated	
5C-5Fh		Timer Counter 2 Duplicated	

Address	Port	Register Name	Function
60h	60h R	Keyboard controller data I/O input buffer	Keyboard Controller
	60h W	Keyboard controller data I/O output buffer	
61h	61h RW	Port B	
62h		Keyboard Contoller data Duplicated	
63h		Port B Duplicated	
64h	64h WO	Keyboard controller command	Keyboard Controller
	64h RO	Keyboard Controller Status	
65h		Port B Duplicated	
66h		Keyboard controller command/ Status Duplicated	
67h		Port B Duplicated	
68h		Keyboard Contoller data Duplicated	
69h		Port B Duplicated	
6Ah		Keyboard Contoller data Duplicated	
6Bh		Port B Duplicated	
6Ch		Keyboard controller command/ Status Duplicated	
6Dh		Port B Duplicated	
6Eh		Keyboard controller command/ Status Duplicated	
6Fh		Port B Duplicated	
70h	70h WO	CMOS RAM Address port and NMI Mask	RTC CMOS RAM
71h	71h RW	RTC CMOS RAM data port	
72-7Fh		RTC Duplicated	
80h	80h RW	Reserve	
	81h RW	Channel 2	
	82h RW	Channel 3	
	83h RW	Channel 1	
	84h RW	Reserved	
	85h RW	Reserved	
	86h RW	Reserved	DMA Memory Address
	87h RW	Channel 0	Mapper Page
	88h RW	Reserved	Register
	89h RW	Channel 6	
	8Ah RW	Channel 7	
	8Bh RW	Channel 5	
	8Ch RW	Reserved	
	8Dh RW	Reserved	
	8Eh RW	Reserved	
8Fh	8Fh RW	Refresh	
90-9Fh		Page Resister Duplicated	
0A0h	A0h WO	Initialization Control Word ICW1	
	A0h WO	Operation Control Word OCW2	
	A0h WO	Operation Control Word OCW3	
	A0h RO	Interrupt Service Resister	Interrupt Controller 2
	A0h RO	Interrupt Request Resister	82C59A Compatible
0A1h	A1h WO	Initialization Control Word ICW2	
	A1h WO	Initialization Control Word ICW3	
	A1h WO	Initialization Control Word ICW4	
	A1h RW	Operation Control Word OCW1	
	A1h RW	Interrupt Mask Resister	

Address	Port	Register Name	Function
0A2-0BFh		Interrupt Contoroller 2 Duplicated	
0C0h	C0h RW	DMA Channel 4 base and current address	Connection to DMA Controller 1
0C1h		0C0h Duplicated	
0C2h	C2h RW	DMA Channel 4 base and current word	Connection to DMA Controller 1
0C3h		0C2h Duplicated	
0C4h	C4h RW	DMA Channel 5 base and current address	
0C5h		0C4h Duplicated	
0C6h	C6h RW	DMA Channel 5 base and current word	DMA Controller 2
0C7h		0C6h Duplicated	82C37A Compatible
0C8h	C8h RW	DMA Channel 6 base and current address	
0C9h		0C8h Duplicated	
0CAh	Cah RW	DMA Channel 6 base and current word	
0CBh		0CAh Duplicated	
0CCh	CCh RW	DMA Channel 7 base and current address	
0CDh		0CCh Duplicated	
0CEh	CEh RW	DMA Channel 7 base and current word	
0CFh		0CEh Duplicated	
0Dh	D0h W0	Command Register	
	D0h RO	Status Register	
0D1h		0D0h Duplicated	
0D2h	D2h WO	Request Register	
0D3h		0D0h Duplicated	DMA Controller 2
0D4h	D4h WO	Mask register	82C37A Compatible
0D5h		0D4h Duplicated	
0D6h	D6h WO	Mode register	
0D7h		0D6h Duplicated	
0D8h	D8h WO	Clear Byte Pointer	
0D9h		0D8h Duplicated	
0DAh	DAh RO	Master Clear	
	DAh WO	Temporary Register	
0DBh		0DAh Duplicated	
0DCh	DCh WO	Clear Mask Register	
0DDh		0DCh Duplicated	
0DEh	DEh WO	Write all Mask Register	
0DFh		0DEh Duplicated	
0E0-0E4h			
0E5h	E5h RW	Configuration Resister Index	
0E6h			
0E7h	E7h RW	Configuration Resister Data	
0E8-0EFh			
0F0h	F0h WO	Mathematical Co-processor Resister 0	
0F1-1EFh			

Address	Port	Register Name	Function
1F0h	1F0h RW	Data Register	
	1F1h RO	Error Register	
	1F2h RW	Sector Count	Hard Disk Controller
	1F3h RW	Sector Number	
	1F4h RW	Cylinder Low	
	1F5h RW	Cylinder High	
	1F6h RW	SDH Register	
	1F7h RO	Status Register	
1F7h	1F7h WO	Command register	
1F8-277h			
278h	278h RW	LPT2 Data Port	
	279h RO	LPT2 Status Port	
	27Ah RW	LPT2 Control	Printer PORT 2
	27Bh RW	Automatic adress strobe register	
	27Ch RW	Automatic data strobe register	
	27Dh RW	Automatic data strobe register	
	27Eh RW	Automatic data strobe register	
27Fh	27Fh RW	Automatic data strobe register	
280-2F7h			
2F8h	2F8h RO	Receiver Buffer	
	2F8h WO	Transmit holding Buffer	
	2F8h RW	Divider Latch Least Significant Byte	
	2F9h RW	Divider Latch Most Significant Byte	
	2F9h RW	Interrupt Enable Register	
	2FAh RO	Interrupt Register	Serial PORT 2
	2FAh WO	FIFO control register	
	2FBh RW	Line Controller Register	
	2FCh RW	MODEM Control Register	
	2FDh RO	Status Register	
	2FEh RO	MODEM Status Register	
2FFh	2FFh RW	Scratch Register	
300-377h			
378h	378h RW	LPT1 Data Port	
	379h RO	LPT1 Status Port	
	37Ah RW	LPT1 Control	Printer PORT 1
	37Bh RW	Automatic data strobe register	
	37Ch RW	Automatic data strobe register	
	37Dh RW	Automatic data strobe register	
	37Eh RW	Automatic data strobe register	
37Fh	37Fh RW	Automatic data strobe register	
380-3B3h			
3B4h	3B4h RW	CRT Controller Index	
3B5h	3B5h RW	CRT Controller Data	VGA Controller
3BAh	3BAh W	Feature Control	(mono)
	3BAh R	Input status register	
3BB-3BFh			

Address	Port	Register Name	Function
3C0h	3C0h W	Attribute Controller Index/Data	
	3C1h R	Attribute Controller Index/Data	
	3C2h W	Miscellaneous Output	
	3C2h R	Input Status Register	
	3C3h RW	VGA Enable	
	3C4h RW	Sequencer Index	
	3C5h RW	Sequencer Data	
	3C6h RW	Video DAC Pixel Mask,Hidden DAC Register	
	3C7h W	Pixel Address Read Mode	VGA Controller
	3C7h R	DAC Status	
	3C8h RW	Pixel Mask Write Mode	
	3C9h RW	Pixel Data	
	3CAh R	Future Control Readback	
	3CCh R	Miscellaneous Output Readback	
	3CEh RW	Graphics Controller Index	
3CFh	3CFh RW	Graphics Controller Data	
3D4h	3D4h RW	CRT Controller Index	
3D5h	3D5h RW	CRT Controller Data	VGA Controller
	3DAh W	Feature Control	(color)
3DAh	3DAh R	Input status register	
3E0-3F1h			
3F2h	3F2h WO	Digital Output Register	Floppy Disk Controller
3F3h			
3F4h	3F4h RW	Main Status register	Floppy Disk Controller
	3F5h RW	Data Register	
	3F6h RO	Reserved for IDE	
3F7h	3F7h RO	Digital Input Resister	
	3F7h WO	diskette control register	Shared with IDE
3F8h	3F8h RO	Receiver Buffer	
	3F8h WO	Transmit holding Buffer	
	3F8h RW	Divider Latch Least Significant Byte	
	3F9h RW	Divider Latch Most Significant Byte	
	3F9h RW	Interrupt Enable Register	
	3FAh RO	Interrupt ID Register	Serial PORT 1
	3FAh WO	FIFO control register	
	3FBh RW	Line Control Register	
	3FCh RW	MODEM Control Register	
	3FDh RO	Status Register	
	3FEh RO	MODEM Status Register	
3FFh	3FFh RW	Scratch Register	

5.2 ISA Bus Interface

CARD-486HB/486HBL is equipped with the Industry Standard Architecture (ISA) bus structure, a worldwide standard architecture for personal computer systems. The ISA bus is controlled by the Intel 486SXSF CPU and CPUBus interface (SPC8210).

5.2.1 ISA Bus signals

Adrress bus signals

System Address bus (SA[19:0])
These signals are used to indicate memory and I/O device address on the bus. These addresses are latched and held, and are effective for the duration of the bus cycle. When master function is used, it is driven by the device on I/O channel.

Latchable Address bus (LA[23:17])
These signals are used to indicate memory device addresses on the bus. They are used together with the system address signals, and make it possible to access up to 16MB of memory on the bus. These signals are not latched.

System Byte High Enable (SBHE#)
When active, this signal (which is active low) indicates transmission of the most significant 8 bits (SD[15:8]) on the system data bus.

Data bus

System data bus(SD[15:0])
This 16-bit data bus is used in the transmission of data between memory on the bus and the CPU and I/O devices.

I/O control signals

I/O Read(IOR#)
This signal gives an I/O device permission to drive data on the bus.

I/O Write(IOW#)
This signal instructs an I/O device to accept data from the bus.

I/O Chip Select 16(IOCS16#)
This input is a signal that indicates to the system that the data transfer on the bus is a 16-bit I/O transfer. The default for 16-bit I/O transfer is one wait cycle. When not driven low, the default transfers a 4-wait 8-bit I/O cycle.

Memory control signals

MEMory Read(MEMR#)
This signal gives a memory device permission to drive data on the bus.

MEMory Write(MEMW#)
This signal instructs an I/O device to accept data from the bus.

Sytem MEMory Write(SMEMW#)
This signal is active when a memory write cycle is started for the 0-1MB memory space on the bus.

System MEMory Read(SMEMR#)
This signal is active when a memory read cycle is started for the 0-1MB memory space on the bus.

MEMory Chip Select 16(MEMCS16#)
This signal indicates a 16-bit memory transfer to the systme. When this signal is not active, the default memory bus cycle, a 4-wait 8-bit cycle, is used.

DMA Control Signals

Address ENable(AEN)
When this signal is active, the DMA controller within the system controls the address bus, data bus, read command, and write command.

DMA ReQuest(DRQ[7:5,3:0])
DMA data transfer request signal sent to the system.

DMA ACKnowledge (DACK[7:5,3:0])
This signal indicates that control of the bus was released to the DMA channel on which DMA transfer was requested.

Terminal Count (TC)
In the DMA transfer cycle, this signal indicates completion of the DMA channel transfer.

Refresh control signal

REFRESH(REF#)
When this signal is active, it indicates that the bus refresh cycle has either been requested or is in progress.

External master control signal

MASTER(MASTER#)
The external bus master makes this signal active in order to acquire the control authority of the bus. Before the external bus master makes this signal active, however, it must first make DRQn# active and then receive DACKn#.

Clock signals

System CLocK (SCLK)
This is 50% duty basic bus clock. Frequency of SCLK is determined by CPU clock frequency.

CPU CLOCK	SCLK freq.
16MHz	8MHz
33MHz	8.33MHz

Oscillator (OSC)
This is a 14.31818 MHz clock output. This signal is not synchronized to the system clock.

Other I/O channel signals

I/O CHannel ChcK(IOCHCK#)
This signal alerts the system when a parity error occurs in memory or an I/O device on the bus, or when an unrecoverble error occours. THis signal generates an NMI for the system.

I/O CHannel ReaDY(IOCHRDY)
This signal terminates the bus cycle. If memory or an I/O device on the bus wants to extend the bus cycle, it can extend the cycle by searching for an effective address and command and then setting thia signal low. Until this signal goes high, the system will continue to insert waits in the cycle.

ZERO Wait State(WS0#)
Make this signal initializes the system when the power is turned on. Initialize devices on the bus by using this signal. This signal is active for 50ms.

RESET DRiVe (RESETDRV)
This signal is used to initialize the system when the power is turned on. I/O channel initialization is performed using this signal.

Buffered Address Latch Enable (BALE)
This signal indicates that SA[19:0] and LA[23:17] are enabled and the CPU cycle or DMA cycle has started. On a falling edge of this signal bus data is used to latch LA[23:17]. In the DMA cycle, this signal remains high throughout the cycle.

Interrupt ReQuest(IRQ[15,14,12:9,7:3]
These signals are active high and are used as interrupt request signals. These signals are input asynchronously.

5.2.2 ISA bus cycles

The ISA bus supports the following types of cycles:

*Memory read
*Memory write
*I/O read
*I/O write
*DMA
*Refresh
*External bus master

THese cycles are explained in the following sections.

5.2.3 Memory read cycles

Fig. 5.2.1 shows the basic timing of the 16-bit memory read/write cycle in the ISA bus cycle. Fig. 5.2.2 shows the 8-bit memory read/write cycle. In both the 8- and 16-bit cycles, the system address lines SA[19:0] become valid within one system clock cycle previous to MEMR# becoming active. In the first bus cycle Ts, the system address becomes the valid address, and when the SCLK signal falls BALE becomes active. SA[19:2] are latched by the time of the Ts cycle within the CARD-486HB/486HBL, and output.

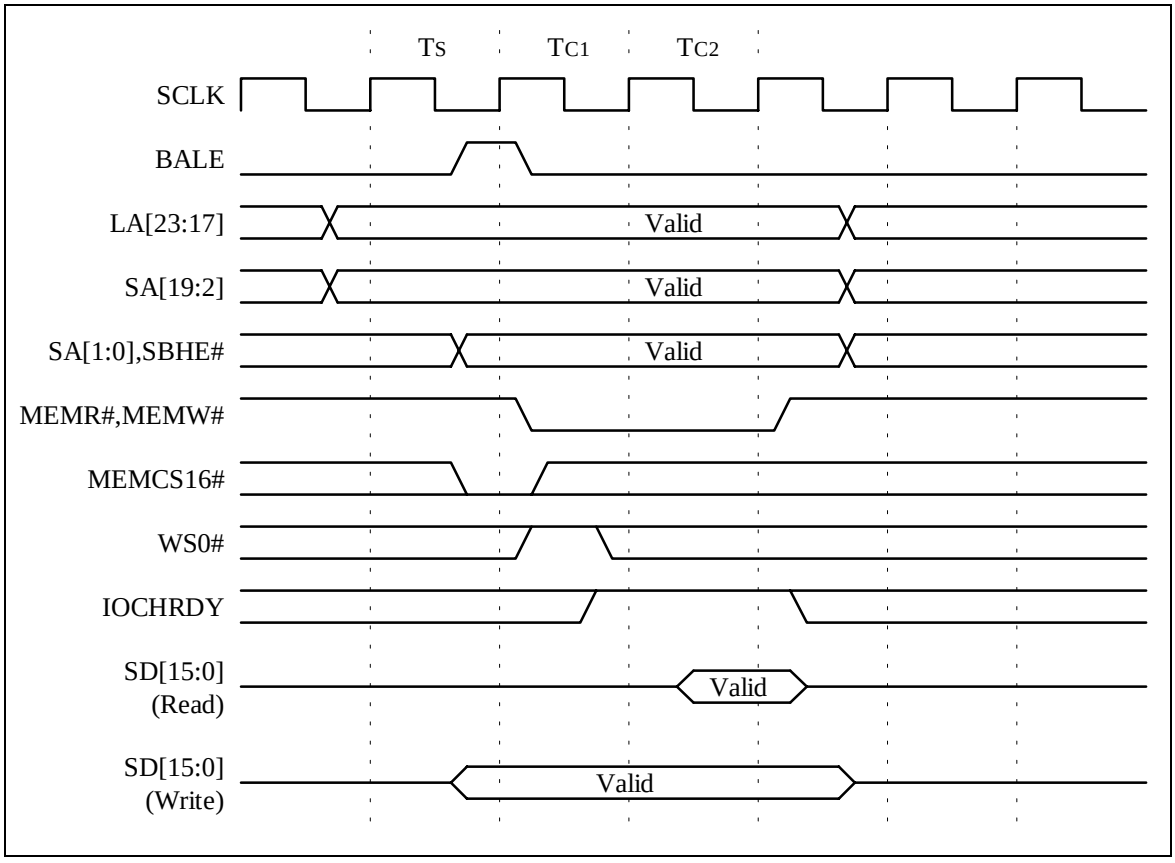


Figure 5.2.1 16-BIT ISA-Bus Memory Read/Write Cycle

16-bit memory transfers are carried out by an external device making MEMCS16# active. LA[23:17] become valid not later than the Tx cycle. MEMR# becomes valid following the SCLK falling edge in T_{C1}. In the 16-bit memory cycle, MEMR# becomes active in the first half of T_{C1}, and in the 8-bit memory cycle, MEMR# becomes active in the second half. In a 16-bit memory transfer, IOCHRDY is sampled for the last time 1 SYSCLK pulse before the end of the cycle. If at this time it is low, a 1 SYSCLK pulse wait is inserted. Thereafter, at the end of each of the Tc [cycles], it is sampled, and a 1 SYSCLK pulse wait is inserted. When IOCHRDY has become inactive, the cycle ends at the end of the next SYSCLK pulse.

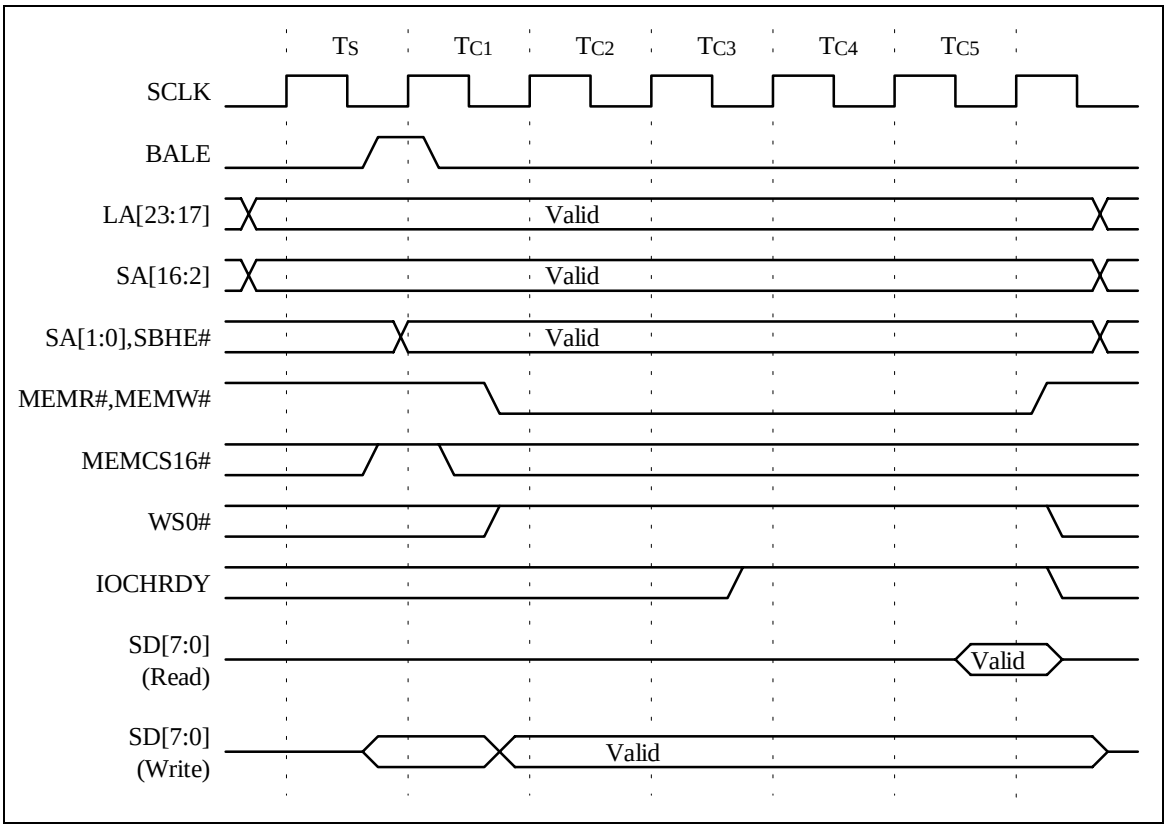


Figure 5.2.2 8-BIT ISA-Bus Memory Read/Write Cycle

In an 8-bit memory transfer, MEMCS16# is inactive. The CARD-486HB/486HBL samples this signal at the end of the Ts cycle, and if this signal is high, before sampling IOCHRDY, a 3-SCLK wait state is inserted. IOCHRDY is sampled at the end of T_{C5}, and if low, a 1 SCLK wait state is inserted. Thereafter, at the end of each of the Tc cycles, it is checked, and after IOCHRDY high is detected, after 1 SCLK cycle termination occurs. Fig. 5.2.4 is a timing chart showing the 8-bit ISA memory cycle when IOCHRDY is inactive.

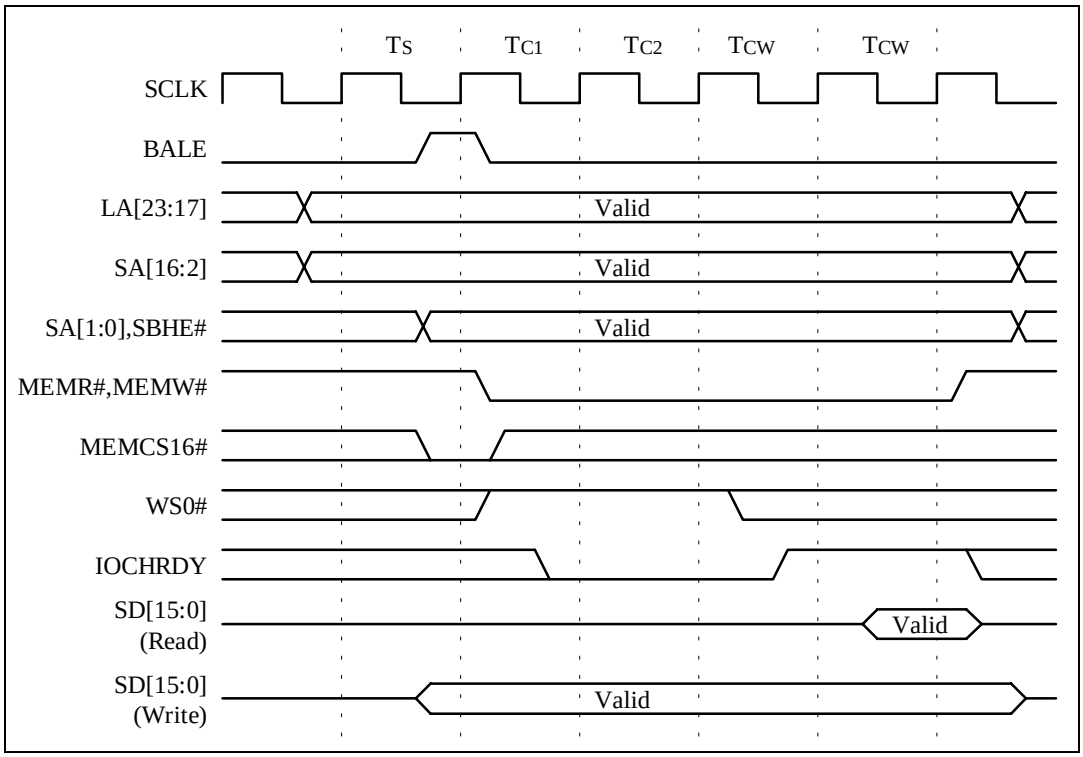


Figure 5.2.3 16-BIT ISA-Bus Memory Read/Write Cycle with IOCHRDY Deasserted

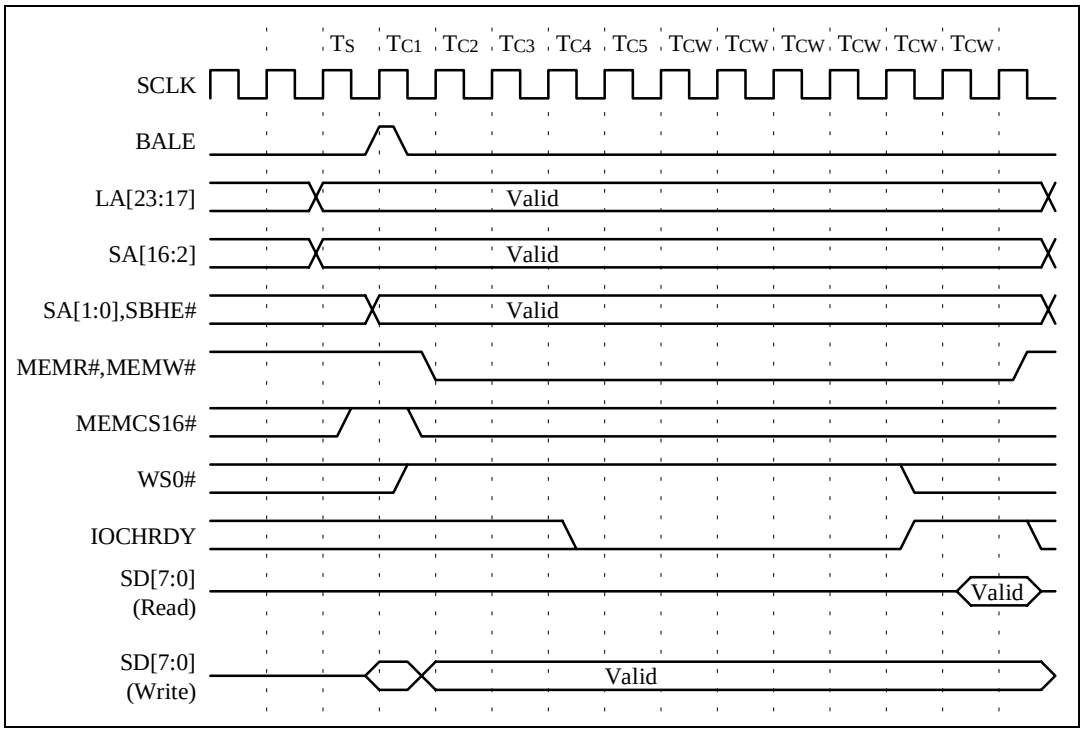


Fig. 5.2.4 8-BIT ISA-Bus Memory Read/Write Cycle with IOCHDRY Deasserted

In a 16-bit memory transfer, WS0# is sampled at the falling edge of T_{C1}, and if it is found to be low, this cycle ends here.

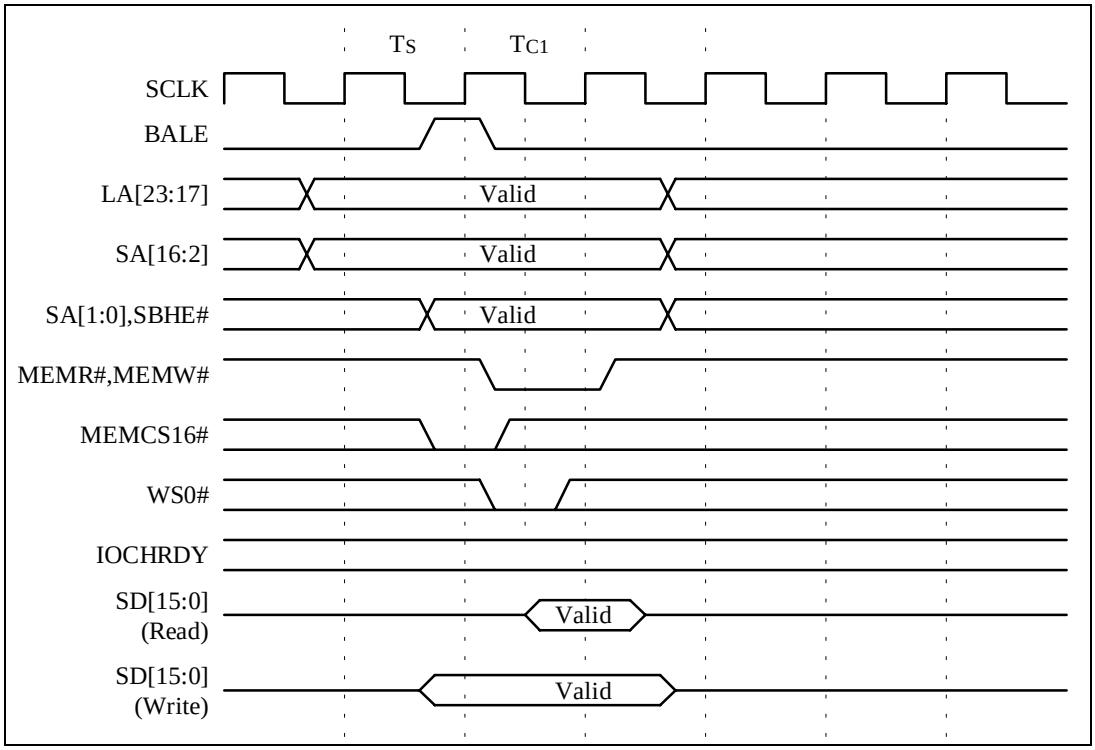


Fig. 5.2.5 16-BIT ISA-Bus Memory Read/Write Cycle with WS0# Asserted

In a 8-bit memory transfer, WS0# is sampled at the end of T_{C1}. At this time, if WS0# is active, the bus cycle ends with this cycle (T_{C2}). Fig. 5.2.6 is a timing chart showing the case where WS0# is used.

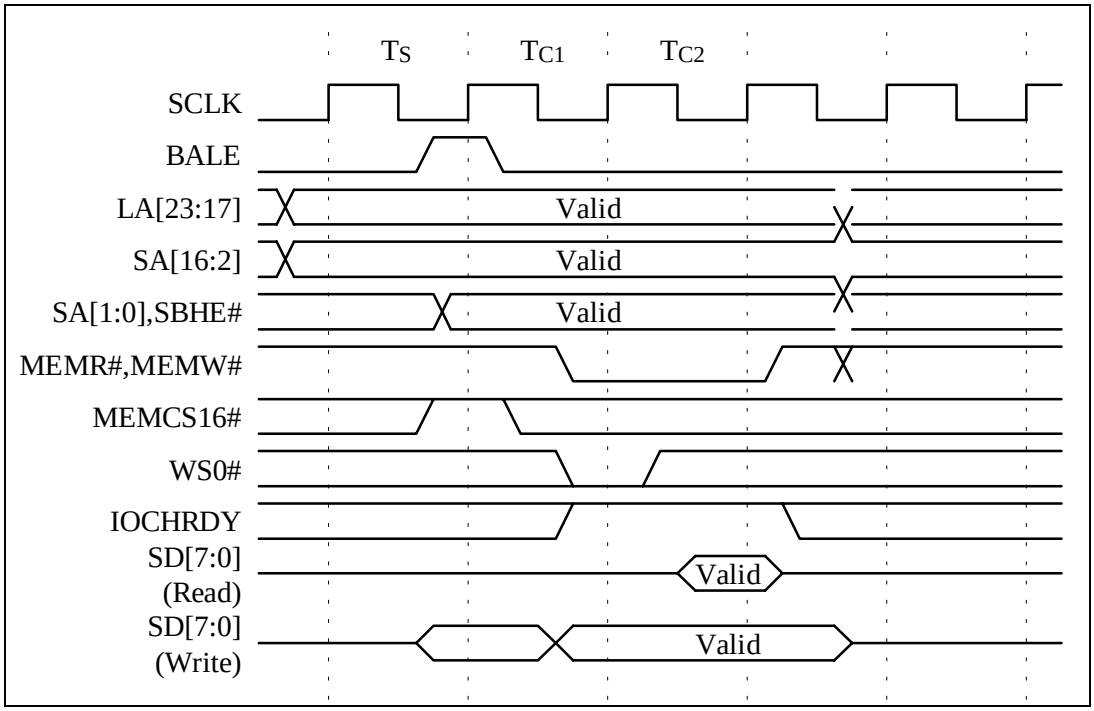


Fig. 5.2.6 ISA-Bus Memory Read/Write Cycle with WS0# Asserted

5.2.4 Memory write cycles

The memory write cycle is the same as the memory read cycle except for the following points. In the memory write cycle, MEMCS16# is sampled at the end of Ts. The write data is output in cycle Ts in the 16-bit cycle, and in cycle Tc1 in the 8-bit cycle.

5.2.5 I/O read cycles

Fig. 5.2.7 shows the basic timing for the ISA 16-bit I/O read/write cycle. Fig. 5.2.8 shows the basic timing for the ISA 8-bit I/O read/write cycle. IOCS16#, which corresponds to MEMCS16# in the memory cycle, distinguishes between 16-bit I/O transfers and 8-bit I/O transfers. MEMCS16# is latched at the end of Ts, but IOCS16# is not latched. As a result, assurance from Tc1 to the end of the cycle is required.

In the 16-bit memory cycle MEMR# and MEMW# become active from the beginning of Tc1, but in the 16-bit I/O cycle IOR# and IOW# become active in the second half of Tc1.

In the 16-bit I/O cycle WS0# is ignored. As a result, the 16-bit I/O cycle cannot be shorter than 3 SYSCLK cycles.

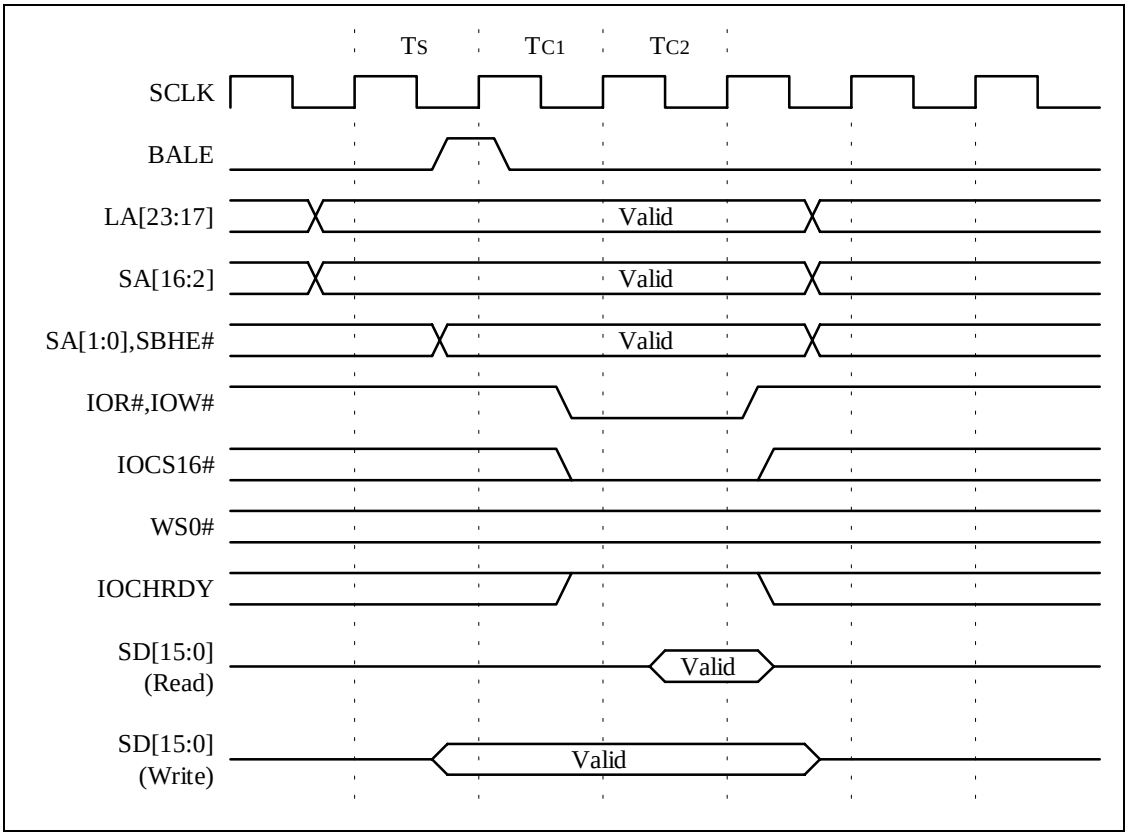


Figure 5.2.7 16-BIT ISA-Bus I/O Read/Write Cycle

In a 16-bit transfer, IOCS16# must be driven low by an external device on the ISA bus. IOCS16# is sampled at the end of T_{C1}. Moreover, LA[23:17] are, according to the CPU specification, always low in an I/O read/write cycle. At the falling edge of T_{C1}, IOR# is driven low, and at the end of the cycle the data is latched.

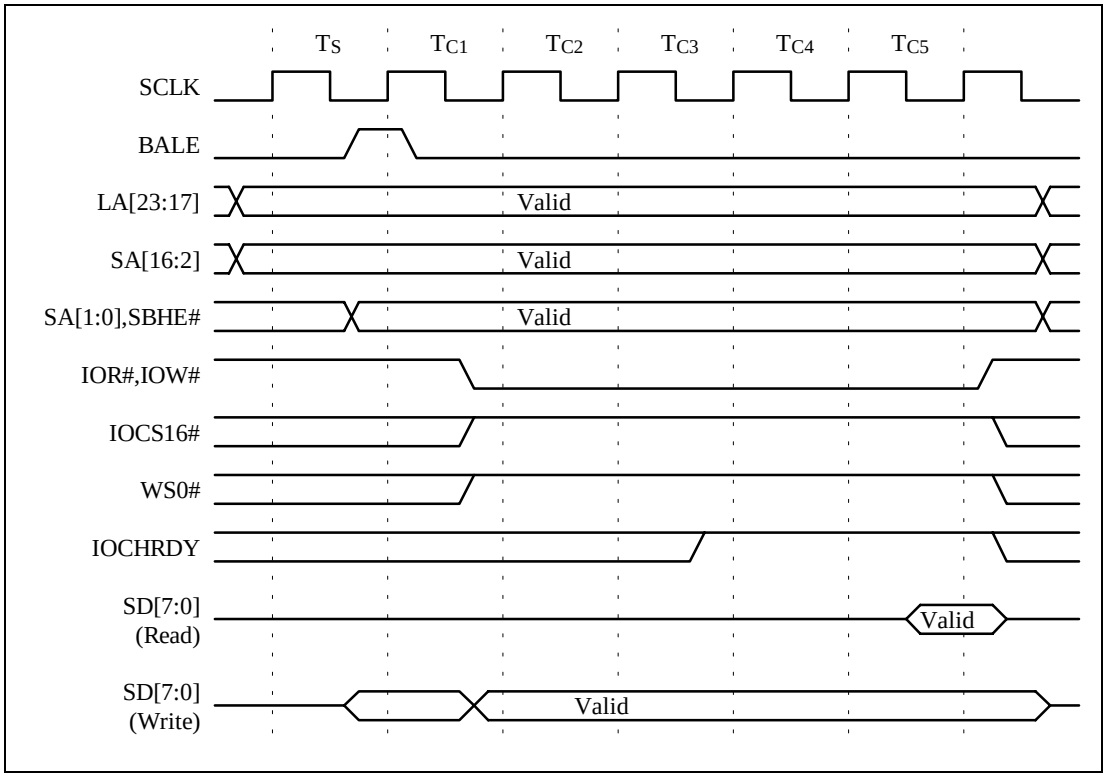


Figure 5.2.8 8-BIT ISA-Bus I/O Read/Write Cycle

In a 16-bit I/O transfer, IOCHRDY is sampled at the end of T_{C1}. If at this time IOCHRDY is found to be low, a 1 SCLK wait state is inserted, and it is sampled again at the beginning of the next cycle. If IOCHRDY is found to be high, this bus cycle ends after 1 SCLK cycle. At the end of the bus cycle, the data is latched by the CARD-486HB/486HBL.

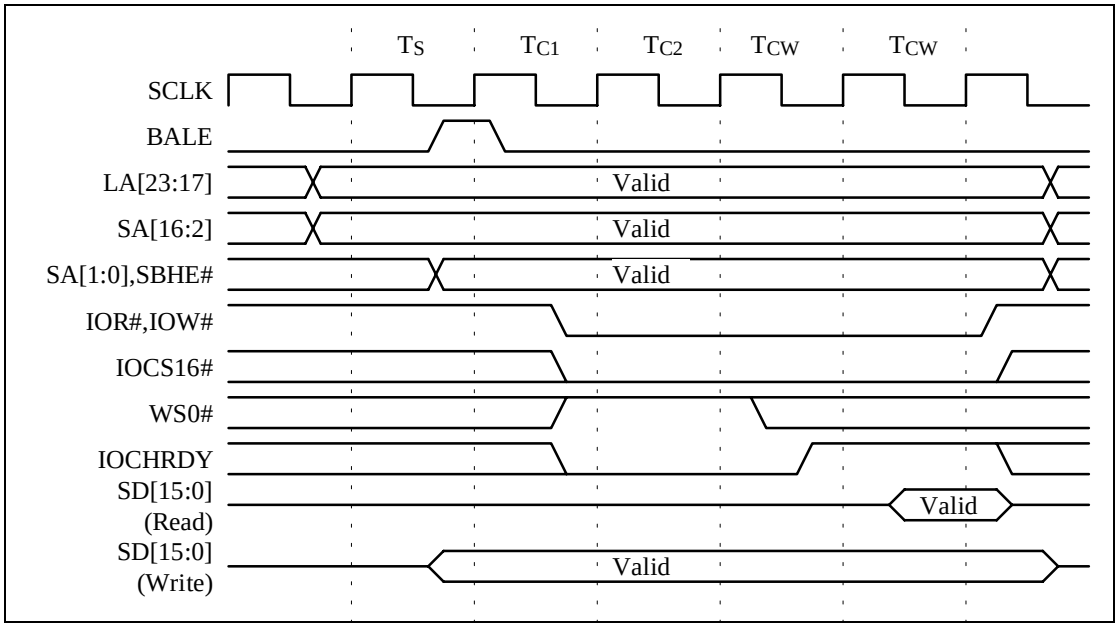


Figure 5.2.9 16-BIT ISA-Bus I/O Read/Write Cycle with IOCHRDY Deasserted

An 8-bit I/O device data transfer is carried out when IOCS16# is inactive. The CARD-486HB/486HBL samples this signal at the end of the Ts cycle, and if this signal is high, before sampling IOCHRDY, a 3-SCLK wait state is inserted. IOCHRDY is sampled at the end of T_{C4}, and until it is detected to be high, is sampled repetitively at the end of [each] Tc cycle. The bus cycle ends 1 SCLK cycle after IOCHRDY high is detected.

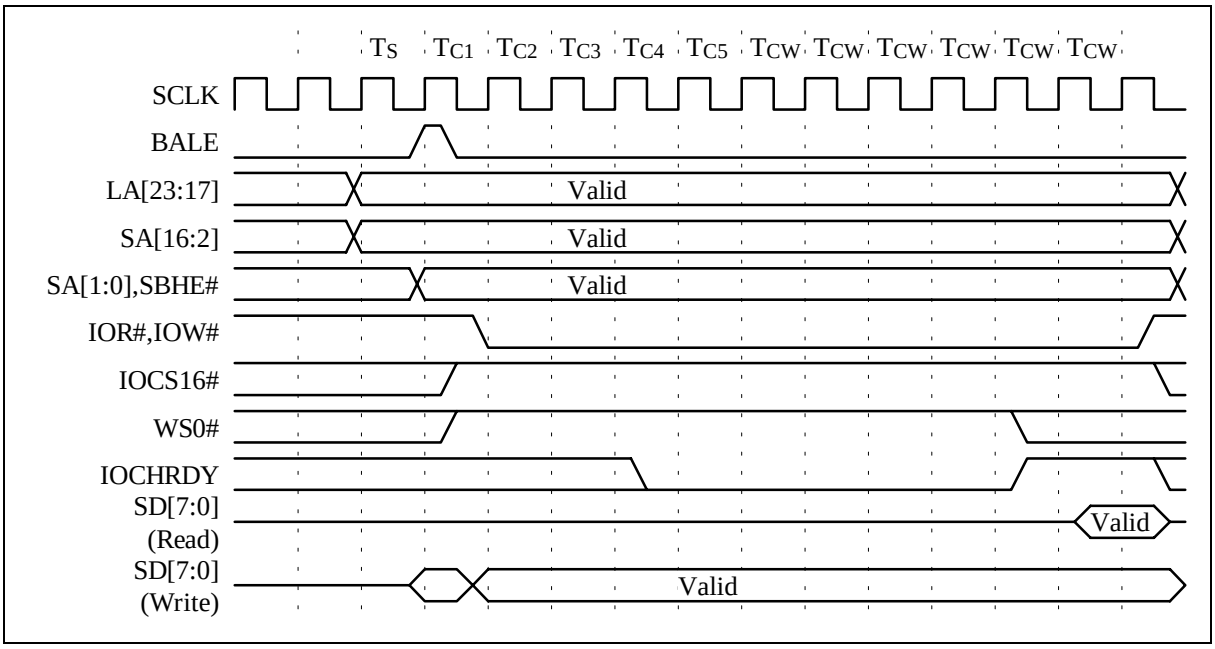


Figure 5.2.10 8-BIT ISA-Bus Read/Write Cycle with IOCHRDY Deasserted

In an 8-bit I/O transfer, the CARD-486HB/486HBL samples WS0# at the end of T_{C1}. At this time, if WS0# is low, the bus cycle ends with this cycle. SD[7:0] are only valid during this cycle. Fig. 5.2.11 is a timing chart showing the case where WS0# is active in an 8-bit I/O cycle. In a 16-bit I/O cycle, WS0# has no significance.

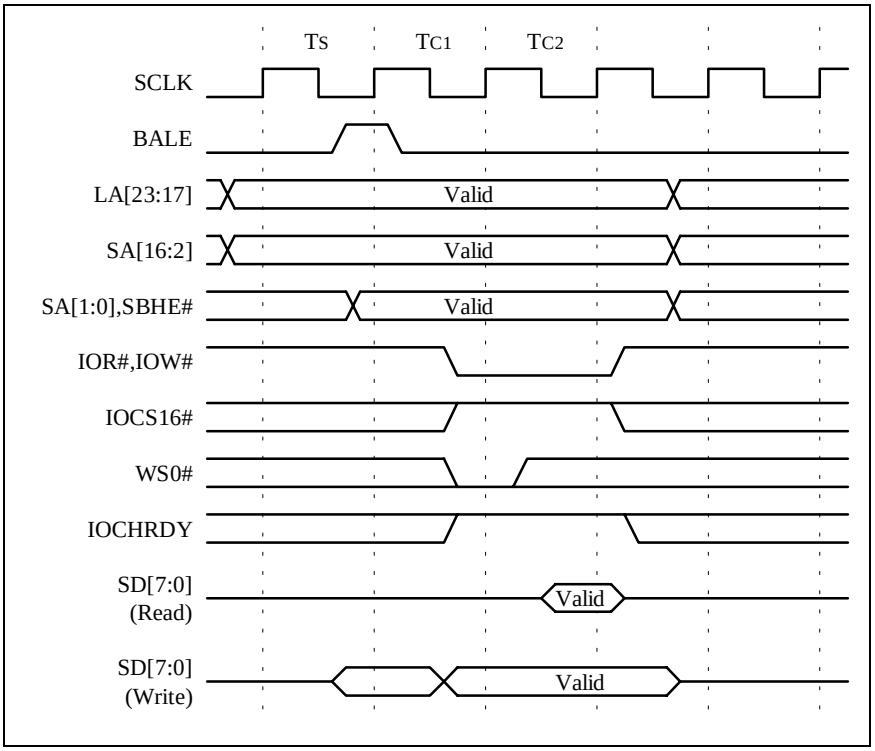


Figure 5.2.11 8-BIT ISA-Bus I/O Read/Write Cycle with WS0# Asserted

5.2.6 I/O write cycles

The I/O write cycle is the same as the I/O read cycle except for the following points.

In the I/O write cycle, the IOW# signal becomes active (low) at the falling edge of Tc1. The I/O device reads the data on the rising edge of IOW#.

In the 16-bit cycle, the timing of IOCHRDY and IOCS16# sampling is the same as in the I/O read cycle. In the 8-bit I/O cycle, IOCHRDY is sampled at the end of Tc4, and when IOCHRDY is detected to be low, a 1 SCLK cycle wait state is inserted. IOCHRDY is sampled repetitively at the end of each Tc cycle. The end of the bus cycle is 1 SCLK cycle after the cycle in which IOCHRDY is sampled as high. When this bus cycle ends, the I/O device must latch (capture) the data.

5.2.7 DMA cycles

CARD-486HB/486HBL includes two 8237A equivalent DMA controllers (DMACs) that support seven standard ISA DMA channels. These DMACs are connected in cascade fashion in a standard ISA master-slave configuration.

Fig. 5.2.12 is a timing chart of the standard DMA cycle, and Fig. 5.2.13 is a timing chart of a DMA cycle including two wait states.

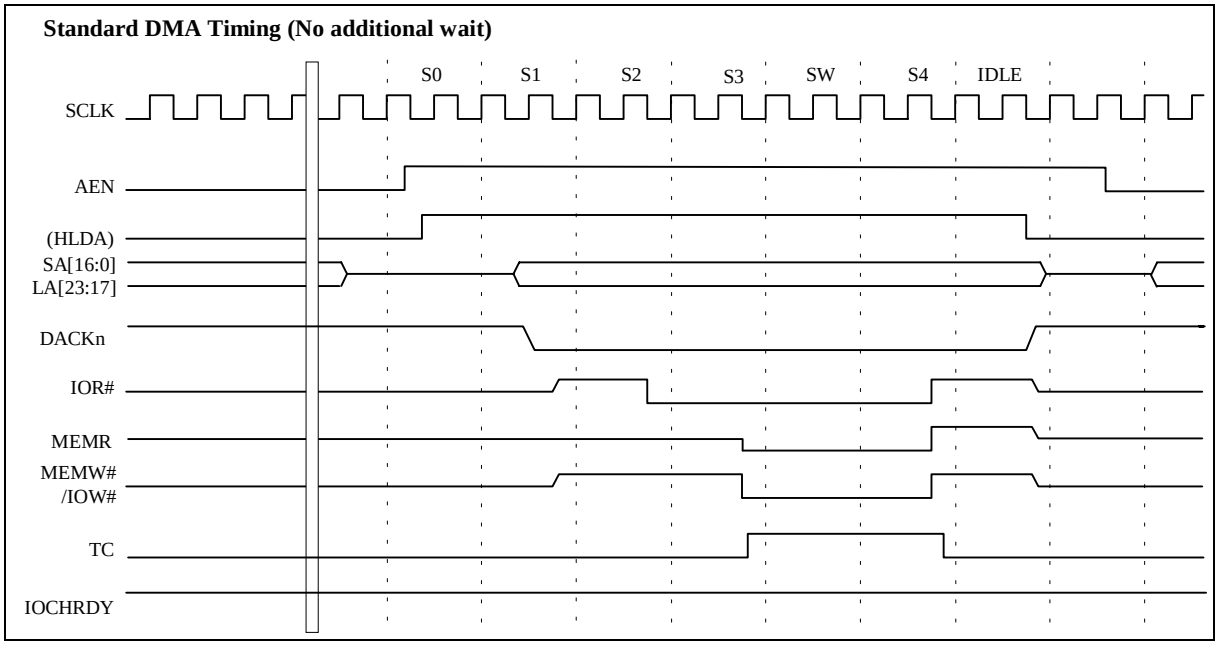


Figure 5.2.12 4-MHz DMA Cycle with 1 Wait State

DRQ[3:0] are used to request an 8-bit transfer between an 8-bit I/O device and an 8- or 16-bit memory device. Each channel transfers data in blocks of up to 64K to a memory area ranging from 0 to 16MB.

DRQ[7:5] are used for 16-bit data transfer. These signals can only be used for data transfers involving 16-bit I/O devices and 16-bit memory devices. Each channel can transfer data up to 128K in size to a system address space of 0 to 16MB.

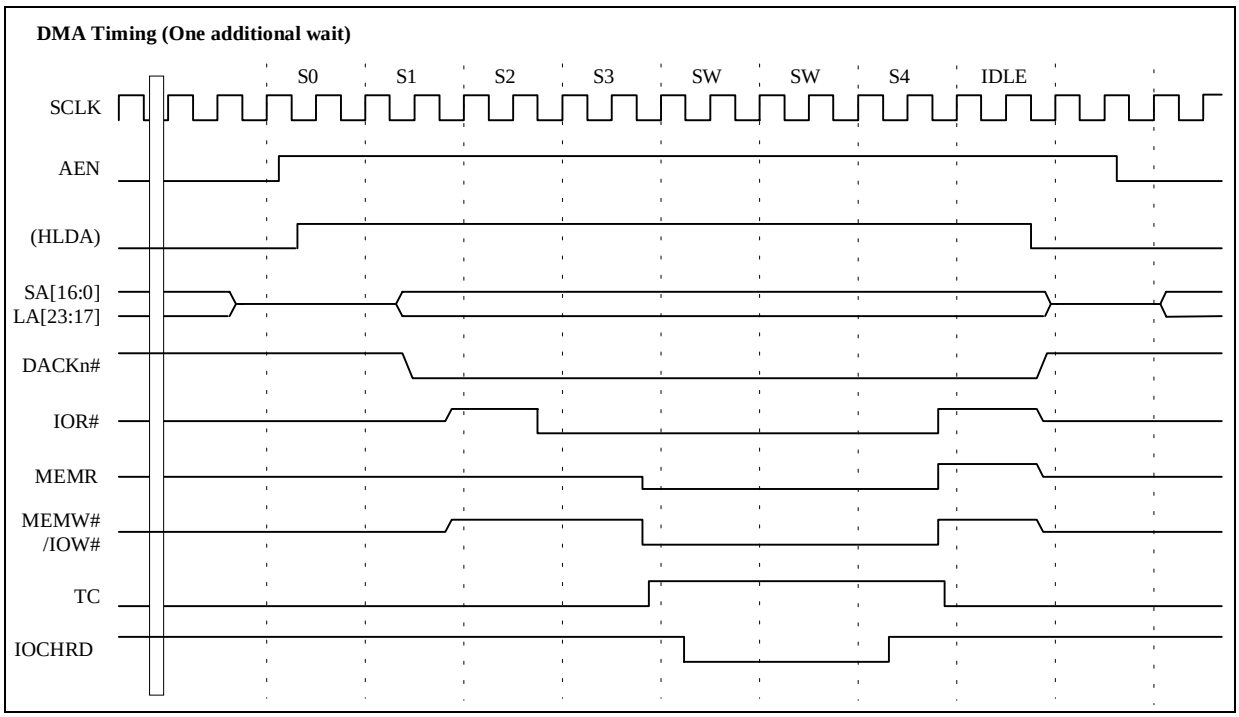


Figure 5.2.13 4-MHz DMA Cycle with 2 Wait State

The AEN signal is goes active (high) during DMA cycles. Addresses are output by the memory mapper and DMAC as follows.

	DMA Memory Address Mapper Page Resister	DMAC
8-bit transfer	A23 - A16	A15 - A0
16-bit transfer	A23 - A17	A16 - A1

5.2.8 External bus master cycles

Fig. 5.1.14 shows the timing chart for the external bus master cycle for the ISA bus. In order to enter this cycle, the bus master makes the DRQn signal active. The external bus master then waits until DACKn# becomes active; finally, in order to establish the external bus master cycle, the external bus master must make MASTER# active.

When the bus master has made MASTER# active before outputing the address and data, it must wait for one SCLK cycle. Then, in order to activate read and write commands, it must also wait at least one more SCLK. Because the memory refresh operation is not perfomed if MASTER# is active for 15us more, it is possible that the comments of memory will be lost. To prevent this from happening, the bus master must make REFRESH# active for the system and execute a refresh cycle.

When the bus master accesses a port within CARD-486HB/486HBL, the system's internal byte-swapping logic becomes effective. For read cycles for odd addresses, data is passed from SD[7:0] to SD[15:8]; for write cycles for odd addresses, data is passed from SD[15:8] to SD[7:0]. Fig.5.1.14 shows the timing chart for when the external bus master accesses an internal port without bus-swapping.

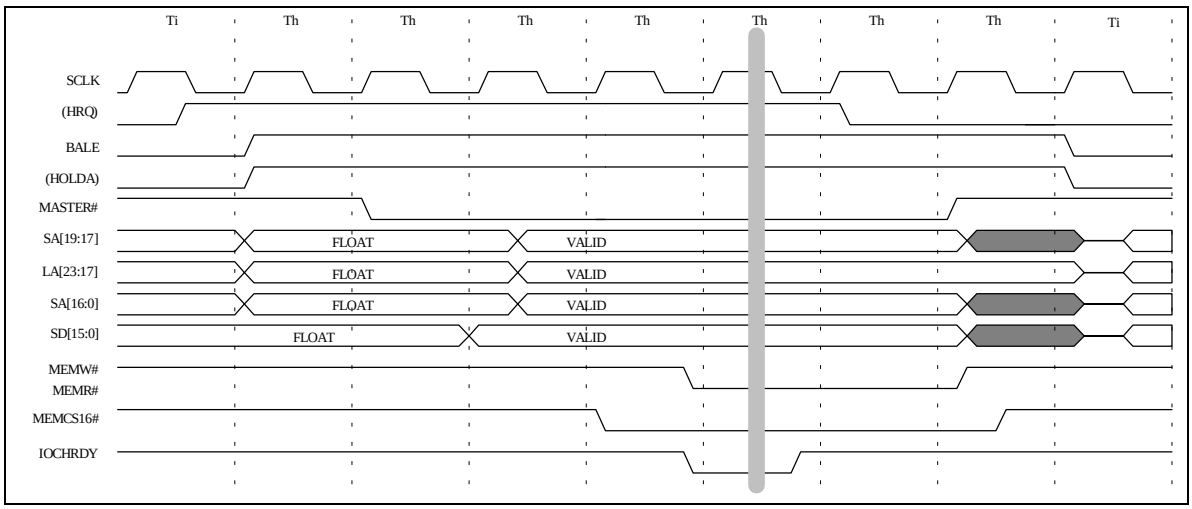


Figure 5.2.14 External Bus Master Cycle to Local Memory

In regards to memory accesses, the MEMCSI16# signal is ignored in original AT and ISA bus machines. Accesses to internal memory by an external bus master are all executed as 16-bit memory accesses.

5.2.9 Refresh cycles

When the bus master has bus control authority, the bus master begins a local memory refresh by making REF# active. Figs. 5.1.15 and 5.1.16 shows the refresh cycles generated by the bus master with and without wait states.

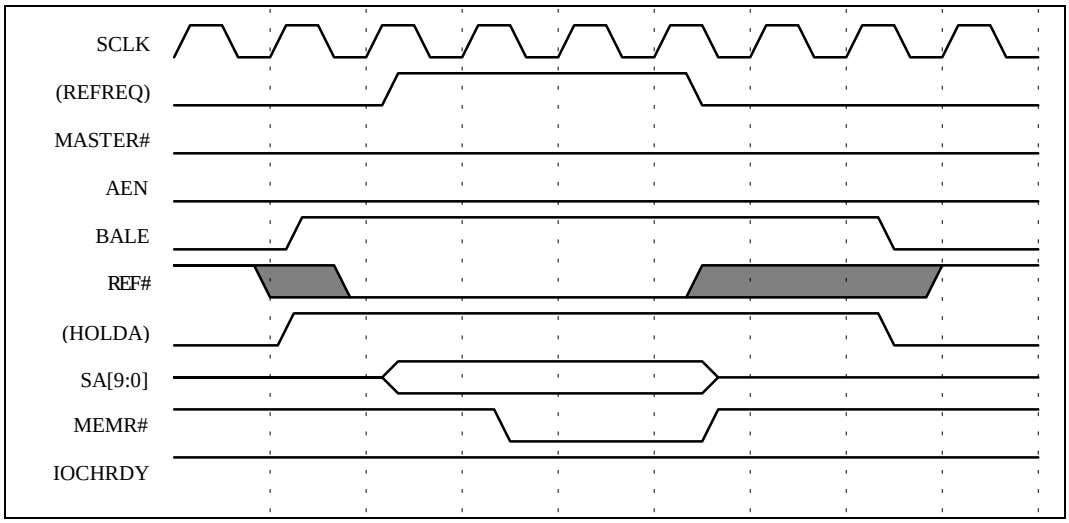


Figure 5.2.15 Bus Master Initiated Default Refresh Cycle

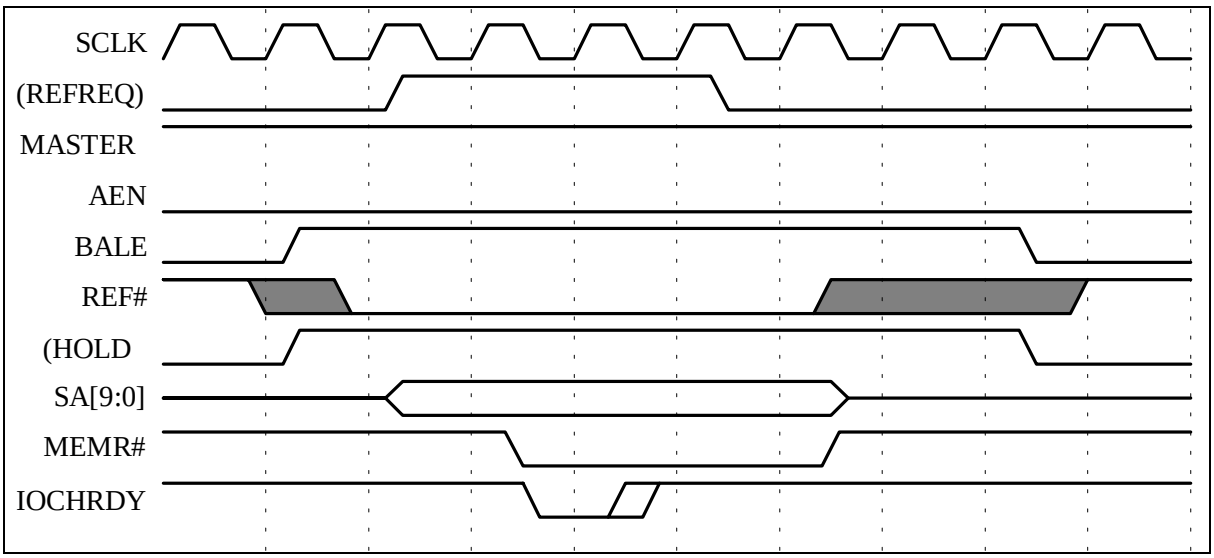


Figure 5.1.16 Bus Master Initiated Default Refresh Cycle

When MASTER# is not active, then when the 8254 (a programmable interval timer) in the system reaches the refresh timeout value, REF# is made active and a memory refresh cycle is executed. In addition, the system outputs the refresh addresses and the timing charts for the normal refresh cycle and the extended refresh cycle. To perform refresh cycles for slow memory devices, it is possible to extend the cycle by setting IOCHRDY low.

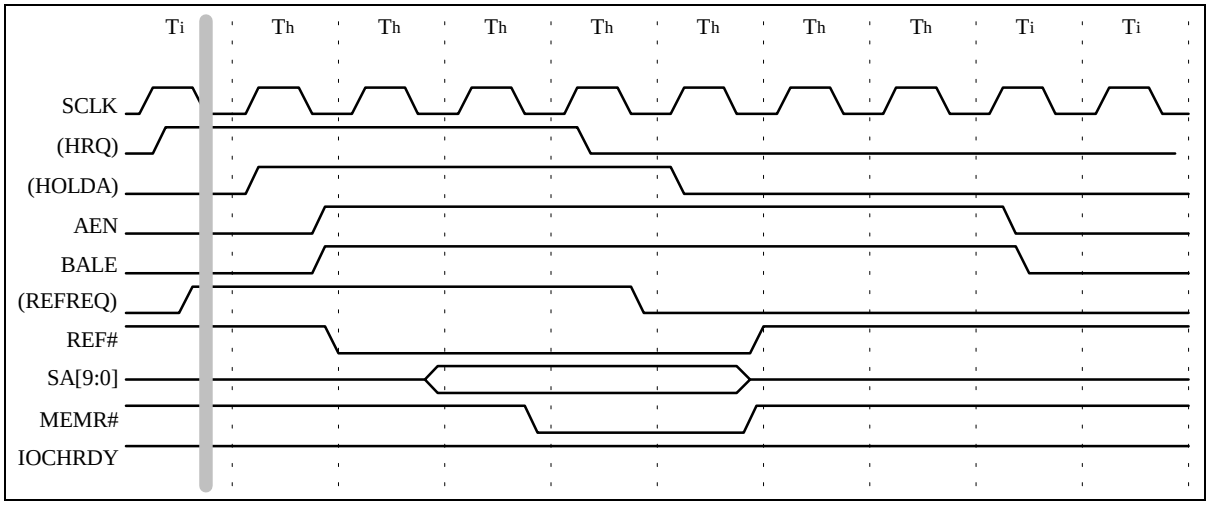


Figure 5.2.17 SYSTEM Initiated Default Refresh Cycle

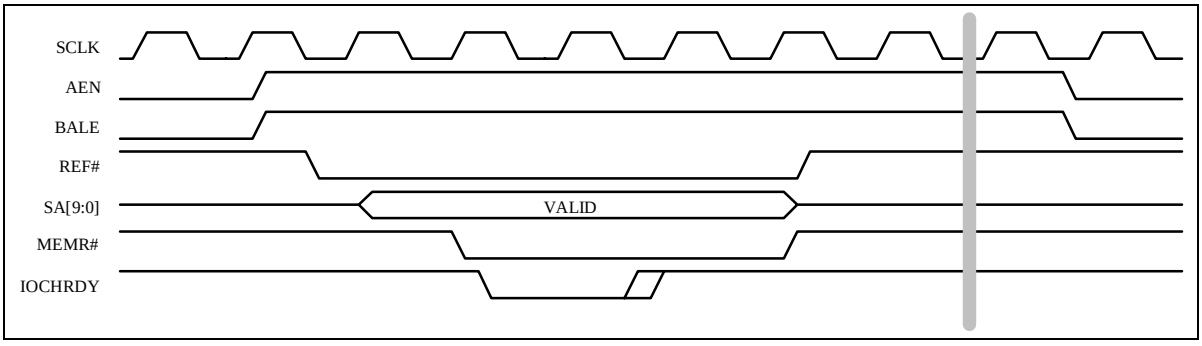


Figure 5.2.18 SYSTEM Initiated Extend Refresh Cycle

5.3 Hard Disk Bus Interface

The CARD-486HB/486HBL is provided with the necessary chip select control signals for supporting IDE (Integrated Drive Electronics) type hard disk drives. It also supports the control circuits for I/O port 3F7h for shared floppy disk and hard disk drives.

This section describes the hard disk interface and its interface signals, timing, and reference circuits.

5.3.1 Features of the hard disk interface

*ISA-compatible hard disk controller chip select signal generation
*Support for control logic for port 3F7h shared by the hard disk controller and the floppy disk controller
*Permits hard disk interface signals to be disabled

The PC AT-compatible hard disk interface addresses are located in the I/O addresses at 1F0h to 1F7h and 3F6h to 3F7h. CARD-486HB/486HBL supports HDCS0# and HDCS1# as chip select signals for these interface addresses. The system's address decording logic makes it possible to effectively utilize port space when constructing a system.

In PC AT-compatible systems, I/O address 3F7h is shared by the floppy disk and hard disk controllers. When 3F7h is read, six bits of data are returned by the hard disk controller and one bit of data is returned by the floppy disk. CARD-486HB/486HBL provides HD7 as a dedicated bus for hard disks.

In addition to the control logic for HD7, CARD-486HB/486HBL supports HDENH# and HDENL# for the control of two buffers for hard disks,. These buffer control signals simplify buffer control for a hard disk making 8-bit nad 16-bit data transfers. HDENL# is active when making an 8-bit access to a hard disk, and both HDENH# and HDENL# are active for 16-bit accesses.

5.3.2 Hard disk interface signals

Hard disk address signals

System Address(SA[2:0]).
These are the ISA bus address signals. These signals are driven by the system or by an external bus master during hard disk access. These aignals are used for register selection in the hard disk controller.

Hard disk data signals

System Data(SD[15:8],SD[6:0]).
These signals are ISA bus system data signals. If the hard disk is not able to drive the system data bus syfficiently, an external data bus buffer must not be connected to the hard disk.

Hard disk data bit (HD7)
Bit 7 of I/O address 3F7 is used for a signal from the floppy disk (DISK CHANGE). D7 from the hard disk is connected to this signal. When 3F7 is read, the data from the FDC is output to SD7, without data being transferred from HD7 to SD7. HD7 is connected to SD7 when accessing a hard disk address other than 3F7.

Hard disk control signals

Hard Disk Chip Select 0(HDCS0#)
This active low output signal is active when accessing I/O addresses 01F0h to 01F7h.

Hard Disk Chip Select 1(HDCS1#)
This active low output signal is active when accessing I/O addresses 03F6h to 03F7h.

Hard Disk buffer Enable High (HDENH#)
This active low output signal is active during 16-bit hard disk accesses.

Hard Disk buffer Enable Low (HDENL#)
This active low output signal is active during all hard disk accesses.
Hard disk data bus DIRction(HDIR)
This is the directional control signal fot he hard disk bus transceiver. Normally, this signal is driven low, but goes high during the read cycle.

I/O Chip Select 16(IOCS16#)
This active low signal is used by disks or other devices on the ISA bus to make 16-bit I/O transfer requests.
This signal is pulled up internally. When this signal is not active, an 8-bit I/O cycle is executed as the default.

Intrrupt ReQuest 14(IRQ14)
This signal is used to request interrupt servicing for the hard disk.

I/O Read(IOR#)
This is the ISA bus I/O read signal. This signal is output during the disk read cycle by the system or by an external master device.

I/O Write(IOW#)
This is the ISA bus I/O write signal. This signal is output during the hard disk write cycle by the system or by an external master device.

RESET DRiVe(RESETDRV)
This active high output signal is the reset signal used on the ISA bus. For use with IDE-type devices, this signal must be inverted. The IDE hard disk interface reset signal is active low, i.e., a reset is requested when the signal is low.

5.3.3 Hard disk bus cycles

Hard disks are accesses through the I/O read and I/O write cycles.

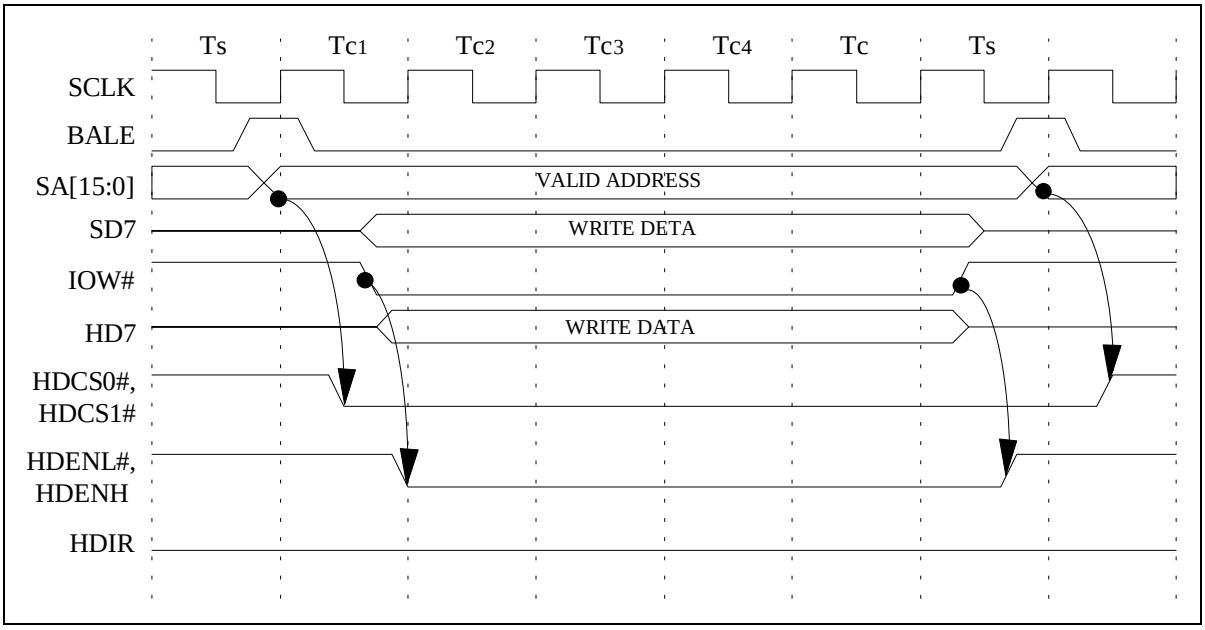


Figure 5.3.1 Hard Disk I/O Write Cycle

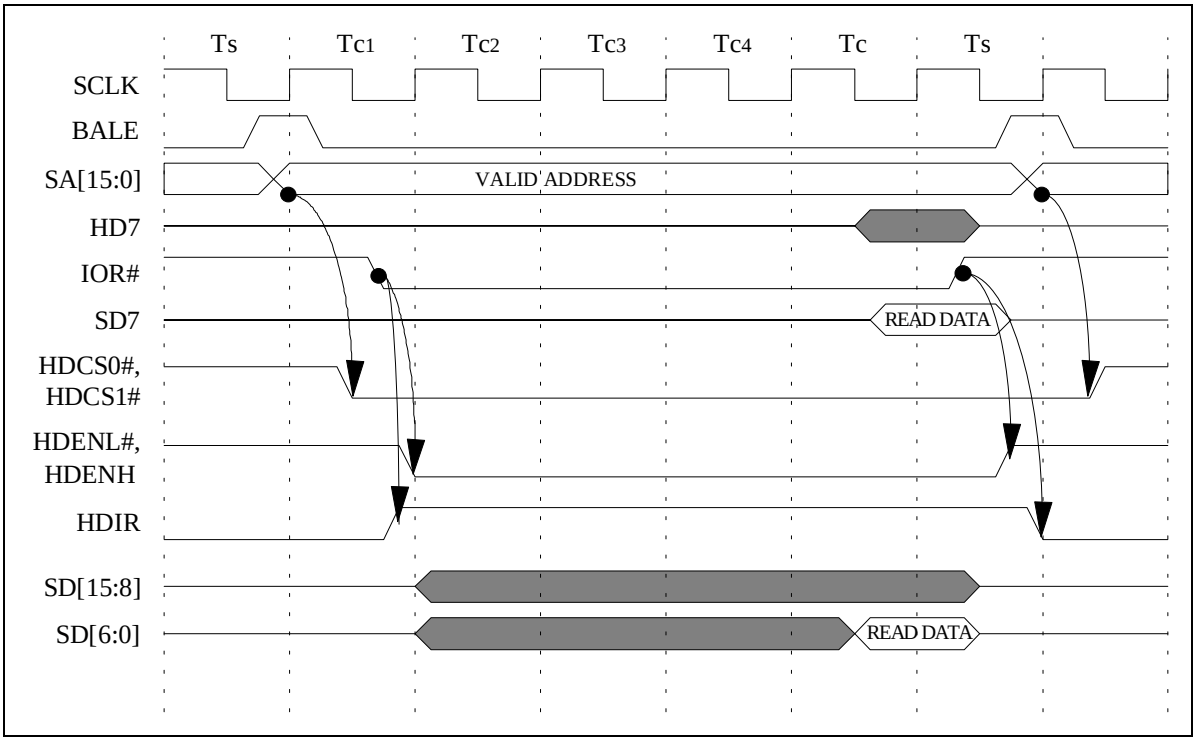


Figure 5.3.2 Hard Disk Read From I/O Address 3F7h

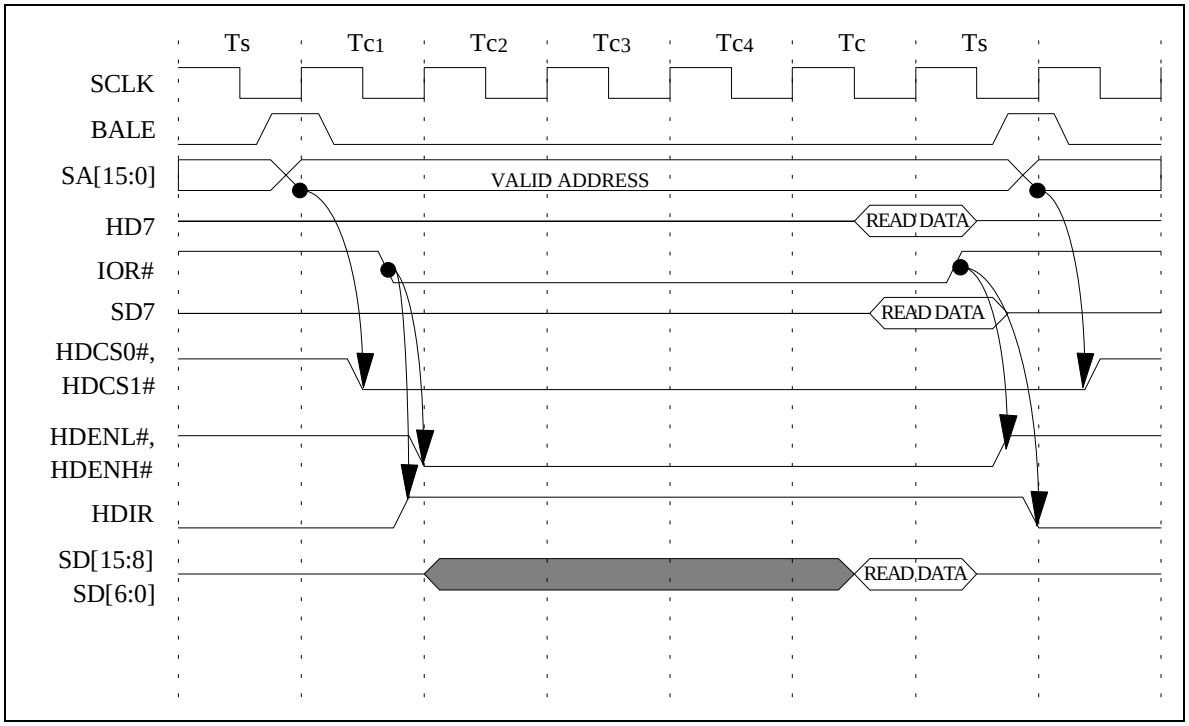


Figure 5.3.3 Hard Disk Read From I/O address 01F0h-01F7h or 03F6h

5.3.4 Hard disk hardware options

Direct IDE hard disk interface

CARD-486HB/486HBL generates the chip select signals and control signals necessary in order to directly connect an IDE-type hard disk drive. Fig.5.3.4 shows a connection diagram for IDE hard disks. This method is possible only when the load on the ISA bus is low. If this method is used, it is possible only when the load on the ISA bus is low. If this method is used, it is possible to reduce the number of external components required. In this example, only one inverter is requied, for the RESET signal. This is because the IDE hard disk reset signal is active low. If necessary, an LED that indicates when the disk is active can be connected externally.

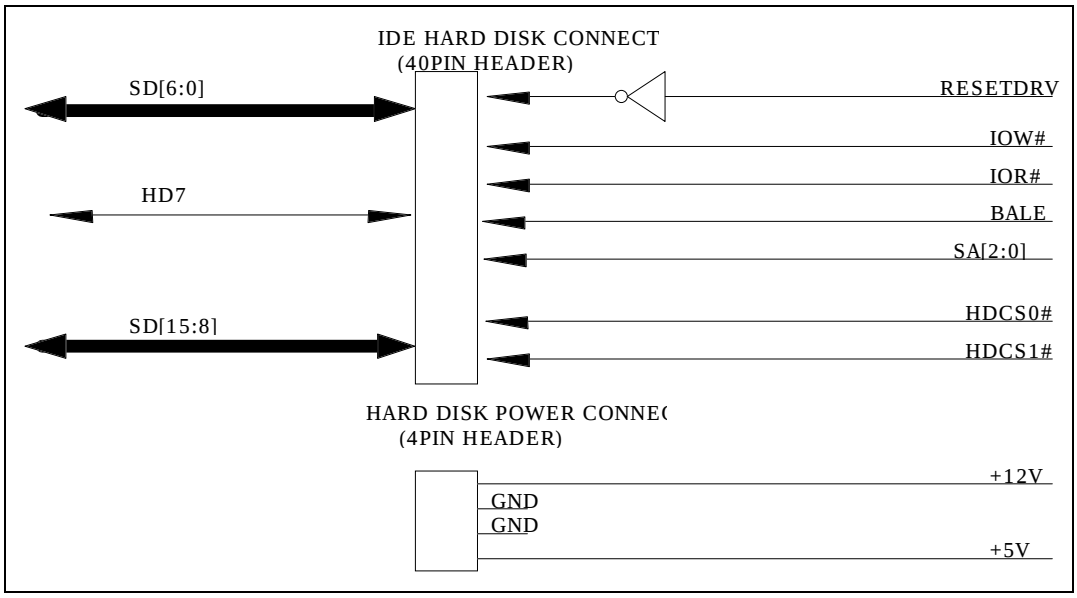


Figure 5.3.4 Direct IDE Hard Disk Interface Examples

Buffered IDE Hard Disk Interface

In systems where there is high load on the system data bus, a hard disk drive cannot drive the system data bus sufficiently. CARD-486HB/486HBL also provides signals for controlling external buffers for hard disks for just this type of situation. Fig.5.3.5 shows an example of the connection method in this case.

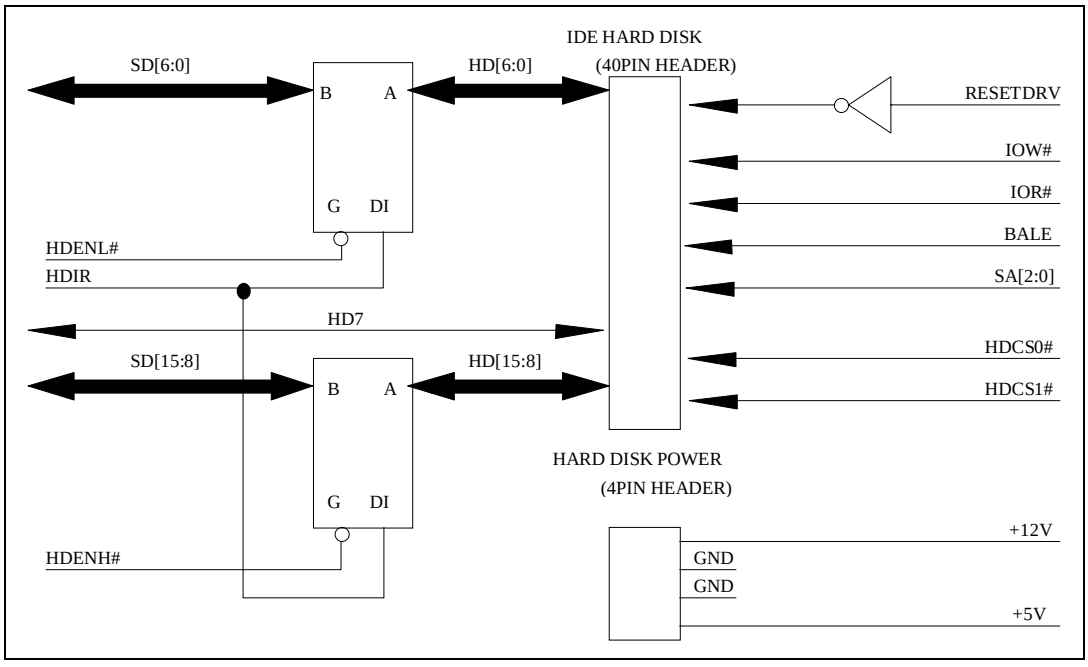


Figure 5.3.5 Buffered IDE Hard Disk Interface Examples

Hard Disk Power Shutdown

A hard disk is not always in constant use; sometimes it is primarily idle, with only ocasional accesses made in order to read or write files. A hard disk consumes a significant amount of power even when it is idle. In addtion, even when a power saving mode is implemented for multiple hard disks through software control, power consumption does not drop to zero. In this system, it is possible to completely cut off the hard disk power supply as shown in Fig.5.3.6. The power management output SMOUTz signal is used as a power interruption signal. In this case, powering down of the hard disk is controlled by the power management routine. CARD-486HB/486HBL includes hardware for detecting the device idle status. The initial setting and control of this hardware is performed by the power management routine in BIOS.

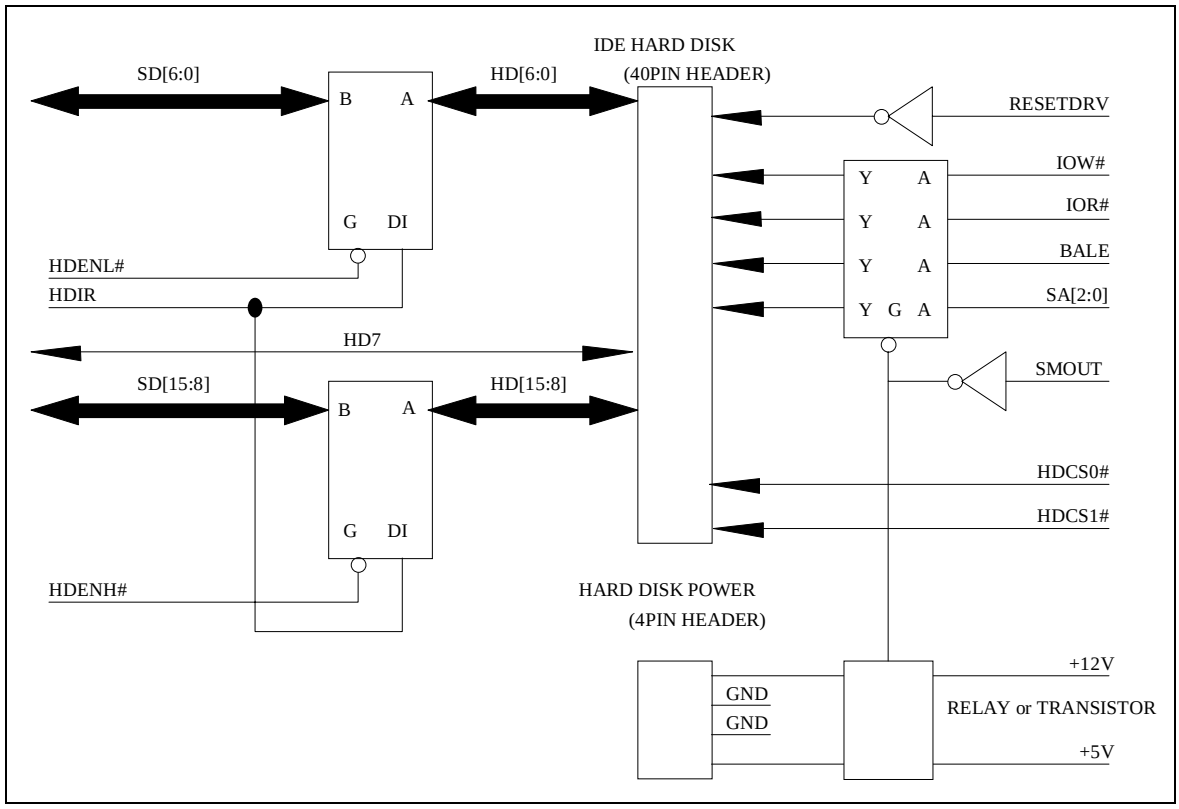


Figure 5.3.6 Bufferd IDE Hard Disk Interface Power Down Example

5.4 Serial Port Interface

Features of the serial port interface

*Support for two 16550-compatible serial port controllers
*Transfer rate can be set from 50 to 115,200bps
*Base address can be set
*Infrared communications support

5.4.1 Serial port interface signals

The serial port control and data signals are shown below.

Control signals

Data Carrier Detect (COMADCD#,COMBDCD#)
This signal indicates that a modem or data terminal detected a carrier signal.

Data Terminal Ready (COMADTR#,COMBDTR#)
This signal indicates that the main controller has completed preparations for communications with the main controller.

Data Set Ready (COMADSR#,COMBDSR#)
This signal indicates that a modem or data terminal has completed preparations for communications with the main controller.

Request to Send (COMARTS#,COMBRTS#)
This signal indicates that the controller has prepared the data to be sent and is requesting to send the data to the modem or data terminal.

Clear To Send (COMACTS#,COMBCTS#)
This signal indicates that the modem or data terminal has completed preparations to receive in response to a request to send.

Ring Indicator (COMARI#,COMBRI#)
This signal indicates that the modem or data terminal detected a telephone ring signal. In additon, in CARD-486HB this signal is also used as a wake-up signal when in the suspended state.

Data

Sriral data transmission (COMATXD,COMBTXD)
This output sends asynchronous serial data.

Serial data Receive (COMARXD,COMBRXD)
Asynchronous serial data input signal.

IrDA SIR data Receive (IRRX)
This is an IrDA SIR-1.0 data input signal for infrared communications.

IrDA SIR data Transmission (IRTX)
This is an IrDA SIR-1.0 data input signal for infrared communications.

Digital ASK data Receive (DARX)
This is a digital ASK data input signal for infrared communications.

5.4.2 Serial port functions

This serial port support full-duplex asynchronous serial transmissions. This controller's control signals are used in a protocol designed to ensure the accuracy of data transfers. Several signals are provided specifically for modem control. However, as long as certain rules are observed, those signals can also be used for communications with other devices.

The controller is provided with the following registers. In the I/O Address, "x" is 3 for COM A, and 2 for COM B, according as COM A/B is selected.

Table 5.4.1 Serial Port Resister

I/O Address	Description
xF8h WO	TX buffer when DLAB=0
xF8h RO	RX buffer when DLAB=0
xF8h RW	Divisor latch LSB when DLAB=1
xF9h RW	Divisor latch MSB when DLAB=1
xF9h RW	Interrupt enable register when DLAB=0 Bit[4-7] = 0 Bit3 : Modem status interrupt enable Bit2 : Receiver line status interrupt enable Bit1 : Transmitter holding register Bit0 : Received data available interrupt enable 1-enable, 0-disable
xFAh WO	FIFO control register
xFAh RO	Interrupt ID register Bit[3-7] = 0 Bit[2,1] Interrupt ID 0,0 Modem status 0,1 Transmitter holding register 1,0 Received data available 1,1 Receiver line status Bit0 : 0-interrupt pending
xFBh	Line control register Bit7 : DLAB 0-Receiver buffer, transmitter holding, or interrupt enable access 1-Divisor latch access Bit6 : Set Break, 1-enable Bit5 : Stick parity Bit4 : Even parity select Bit3 : Parity enable, 1-even, 0-odd Bit2 : Number of stop bit 0 : 1 stop bit, 1 : if word length is 5 bits stop bit length is 1.5 bit times if word length is 6, 7 or 8, then stop bit length is 2 bit times Bit[1-0] Bits per character 0,0 5 0,1 6 1,0 7 1,1 8
xFCh	MODEM control register Bit[5-7] : reserved Bit4 : 1-Loop back mode Bit3 : Out2 interrupt enable, 1-enable Bit2 : Out1 Active, 1-active Bit1 : Request to send active, 1-active Bit0 : Data terminal ready, 1-active

xFDh	Line status register Bit7 : 0 Bit6 : Transmitter empty Bit5 : Transmitter holding register empty Bit4 : Break interrupt Bit3 : Framing error Bit2 : Parity error Bit1 : Overrun error Bit0 : Data ready
xFEh	MODEM status register Bit7 : Data carrier detect Bit6 : Ring indicator Bit5 : Data set ready Bit4 : Clear to send Bit3 : Delta data carrier detect Bit2 : Trailing edge ring indicator Bit1 : Delta data set ready Bit0 : Delta clear to send
xFFh	Scratch register Independent data for General Data

Configuration Register settings are carried out by the BIOS, but the settings are listed here for reference. Settings can also be made for the infrared communications protocol. Read/Write operations on the Configuration Registers use I/O ports E5h and E7h.

For UART1, the I/O address and interrupt numbers can be changed by setting UART1 Configuration [UART1CFG] in the Configuration Registers.

Table 5.4.2 UART1 Configuration

Bit	1, 0	UART1 I/O Address bit 1 and 0	bit 1 bit 0 0 0 : I/O 3F8h - 3FFh 0 1 : I/O 2F8h - 2FFh 1 0 : I/O 3E8h - 3EFh 1 1 : I/O 2E8h - 2EFh
	3, 2	UART1 IRQ bit 1 and 0	bit 3 bit 2 0 0 : IRQ4 0 1 : IRQ3 1 0 : IRQ11 1 1 : IRQ10
	4	UART1 Enable	0 : Disable 1 : Enable

For UART2, the I/O address and interrupt numbers can be changed by setting UART2 Configuration [UART2CFG] in the Configuration Registers. It is also possible to select the infrared communications protocol for UART2.

Table 5.4.3 UART2 Configuration

Bit	1, 0	UART2 I/O Address bit 1 and 0	bit 1 bit 0 0 0 : I/O 3F8h - 3FFh 0 1 : I/O 2F8h - 2FFh 1 0 : I/O 3E8h - 3EFh 1 1 : I/O 2E8h - 2EFh
	3, 2	UART2 IRQ bit 1 and 0	bit 3 bit 2 0 0 : IRQ4 0 1 : IRQ3 1 0 : IRQ11 1 1 : IRQ10
	4	UART2 Enable	0 : Disable 1 : Enable
	5	UART2 IR Enable	0 : Serial Port 1 : IR Port
	6	UART2 IR Polarity	Polarity of IRTX pin 0 : Active high 1 : Active low
	7	UART2 IrDA-SIR/D-ASK	Infrared communications protocol 0 : IrDA-SIR protocol 1 : Digital ASK protocol

5.4.3 Serial port buffers

These serial port signals have the capability to directly drive TTL loads such as those used for modem signals. However, for long-distance transmissions such as those made via RS-232C or RS-422 interfaces, external buffers that satisfy the corresponding standards are necessary.

5.4.4 Infrared Communications

The CARD-486HB/486HBL incorporates an infrared communications function. Simply by connecting an external photoemitter/receiver module, infrared communications become possible. There are two communications protocols: IrDA-SIR-1.0 and Digital ASK. These are selected in the BIOS setup, and for COM B, either of IrDA-SIR-1.0 and Digital ASK can be selected. Fig. 5.4.1 shows the UART configuration.

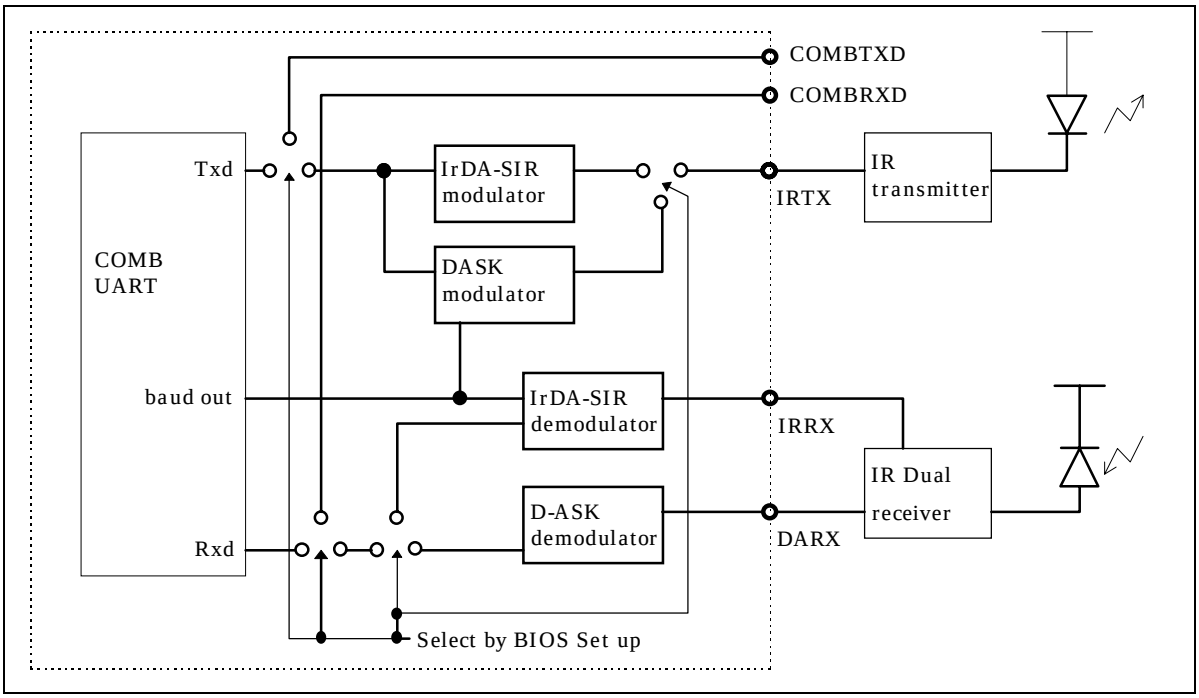


Figure 5.4.1 COMB URAT Diagram

IrDA-SIR-1.0 protocol

Modulation and demodulation in the IrDA-SIR-1.0 standard are as follows.

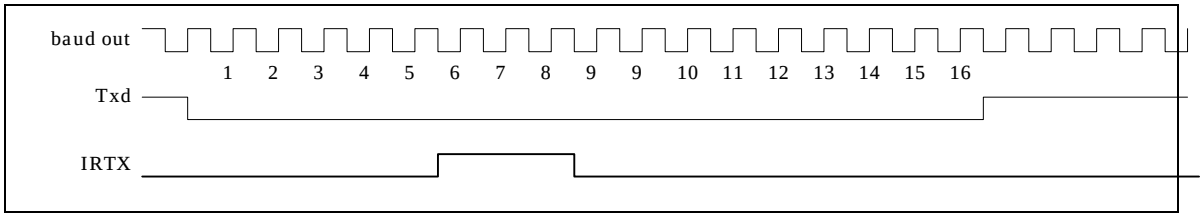


Figure 5.4.2 IrDA-SIR-1.0 protocol modulation

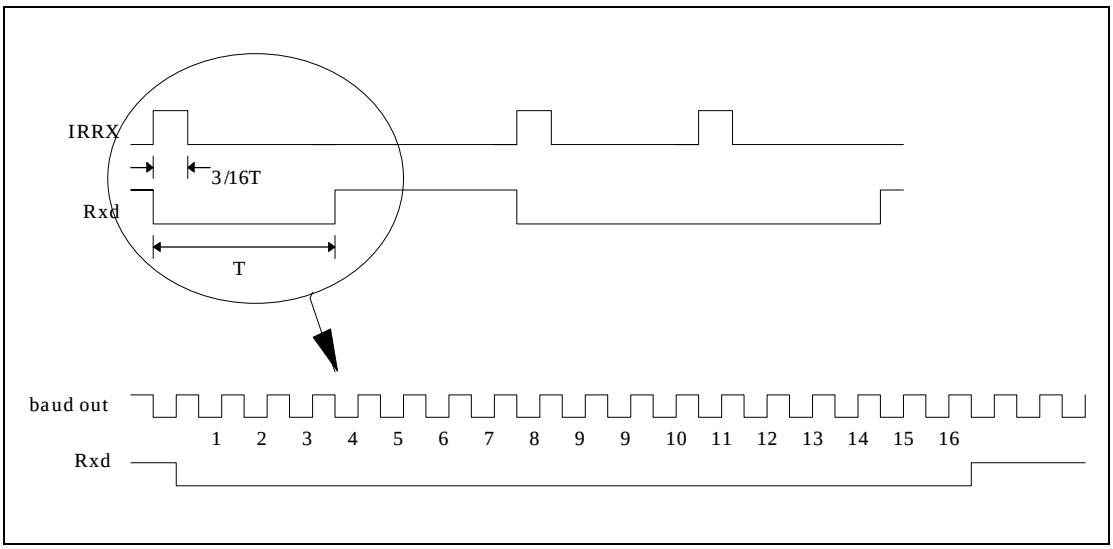


Figure 5.4.3 IrDA-SIR-1.0 protocol demodulation

Digital ASK protocol

Modulation and demodulation in the Digital ASK protocol are as follows. Wherein for the 500 kHz signal is used 1/28 division of the 14 MHz pin of this IC.

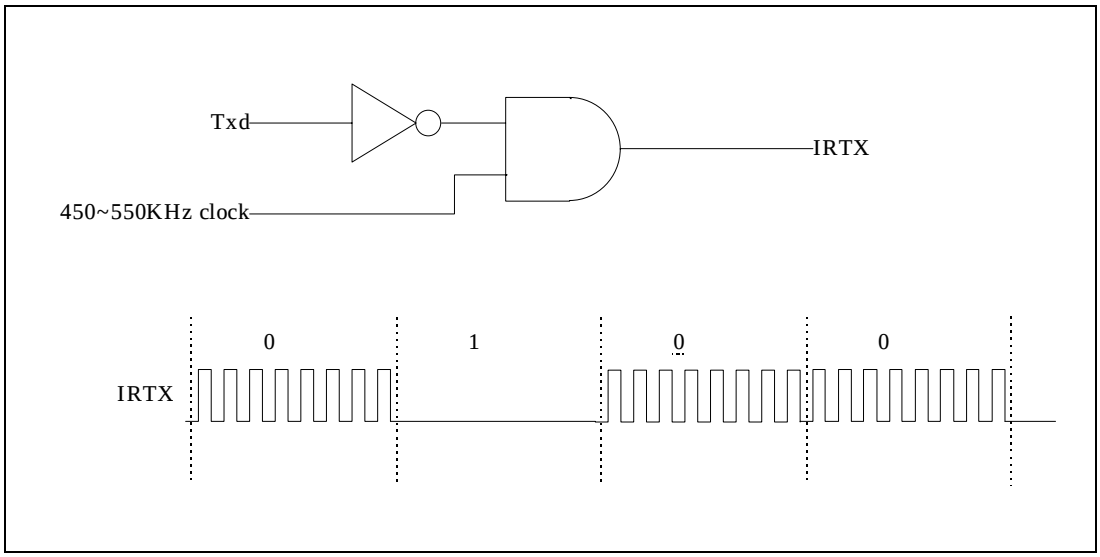


Figure 5.4.4 Digital ASK protocol modulation

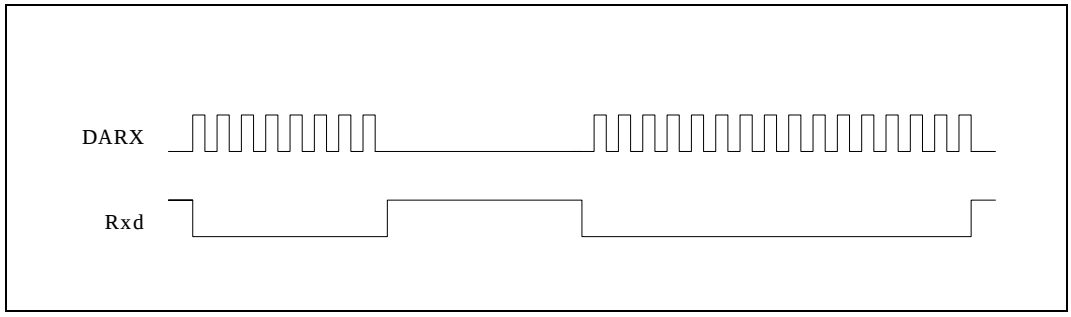


Figure 5.4.5 Digital ASK protocol demodulation

5.5 Parallel Port Interface

The following are the features of this system's parallel port interface.

*Compatible with ISA-style unidirectional parallel ports
*PS/2-style bidirectional parallel port
*No external buffers required
*High-speed parallel port support

5.5.1 Parallel port signals

Parallel port control and data signals are shown below.

Control signals

Line PrinTer STROBE(LPTSTROBE#)
Used as a data read signal for parallel peripheral devices. In high-speed parallel port mode, this signal is used to indicate the write cycle.

Line PrinTer Auto Line FeeD(LPTAFD#)
When this signal is active, the parallel printer inserts a line feed after every line. In high-speed parallel mode, this signal is used as a data strobe. This signal can also be used as a data latch signal in write cycles and as a buffer enable signal in read cycles.

Line PrinTer BUSY (LPTBUSY)
This signal indicates that the printer is not ready to accept data from the CARD-486HB/486HBL.
In high-speed parallel mode, this is used as a wait signal (WAIT#).

Line PrinTer ACKnowledge (LPTACK#)
This signal indicates that the data transmission is completed and there is a state of readiness for the next transmission. In high-speed parallel mode, this is used as an interrupt signal (Intr). This input is connected to the interrupt controller.

Line PrinTer ERROR(LPTERROR#)
This signal is used by peripheral devices to teport errors.

Line PrinTER Paper End(LPTPE#)
This signal is used to indicate that the printer has run out of paper.

Line PrinTer INITialize(LPTINIT#)
Printer initialization signal.

Line PrinTer SeLeCT IN(LPTSLCTIN#)
This signal is used to select the peripheral device currently connected to the port. In high-speed parallel port mode, this signal is used as an address strobe.

Line PrinTer SeLeCTed(LPSLCT)
This signal is used to select the peripheral device currently connected to the port. In high-speed parallel port mode, this signal is used as an address strobe.

Line PrinTer DIRection(LPTDIR)
This signal is used for directional control for external buffers.

5.5.2 Parallel port functions

The parallel port signal timing is controlled by software.

The parallel port registers are as follows. In the I/O Address, "x" is 3 for LPT1, and 2 for LPT2.

Table 5.5.1 Parallel port registers

I/O Address	Description
X78h	Parallel port data register
X79h	Parallel port status register Bit 7 : 0-Printer Busy Bit 6 : 0-Acknowledge Bit 5 : 1-Out of paper Bit 4 : 1-Printer is selected Bit 3 : 0-Error Bits [0-2] : Not Used
X7Ah	Parallel port control register Bits [6-7] : Reserved Bit 5 : direction, PS/2 mode only Bit 4 : Interrupt enable, 1-enable, 0-disable Bit 3 : Select printer, 1-select Bit 2 : Initialize printer, 0-initialize Bit 1 : Automatic line feed, 1-automatic Bit 0 : Data Strobe
X7Bh	Auto address strobe register
X7Ch	Auto data strobe register
X7Dh	Auto data strobe register
X7Eh	Auto data strobe register
X7Fh	Auto data strobe register

5.5.3 High-speed parallel mode functions

In the high-speed parallel (EPP) mode, printer initialization and selection and error signals are the same as in the normal parallel mode. LPTSLCTIN# and LPTAFD# are automatically generated as data strobe and address strobe signals to the parallel device. LPTSTROBE# is used as a signal indicating the write cycle. For details refer to the BIOS Reference Manual.

5.5.4 Parallel port buffring

The CARD-486HB/486HBL parallel port can drive a low load device without buffering, but basically it is recommended for use with an external buffer connected.

The standard setting of the CARD-486HB/486HBL is for a uni-directional parallel port. Fig. 5.5.1 is an example connection diagram, and Fig. 5.5.2 shows an example with a 74LS244 external buffer connected.

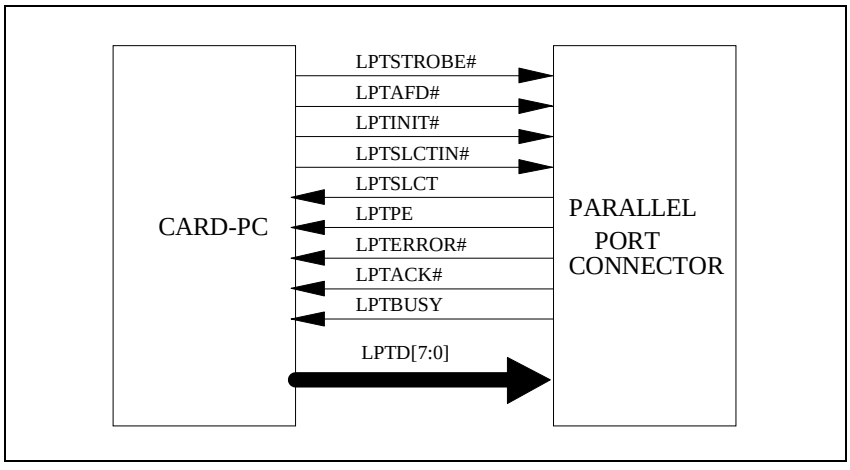


Figure 5.5.1 ISA style uni-directional parallel port interface

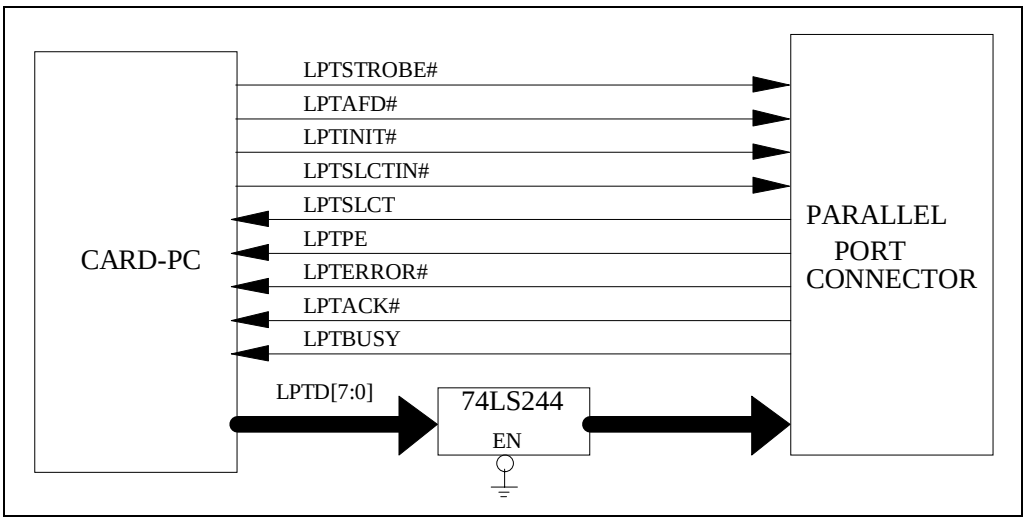


Figure 5.5.2 ISA style uni-directional parallel port interface (with buffer)

One problem with using an external buffer is that applications that require a key device for the parallel port may not operate.

When operating in PS/2-compatible mode, the port is bidirectional. The connections are illustrated in Fig.5.5.3. When using an external buffer, use an 74LS245-equivalent, and use LPTDIR# for directional control for the buffer.

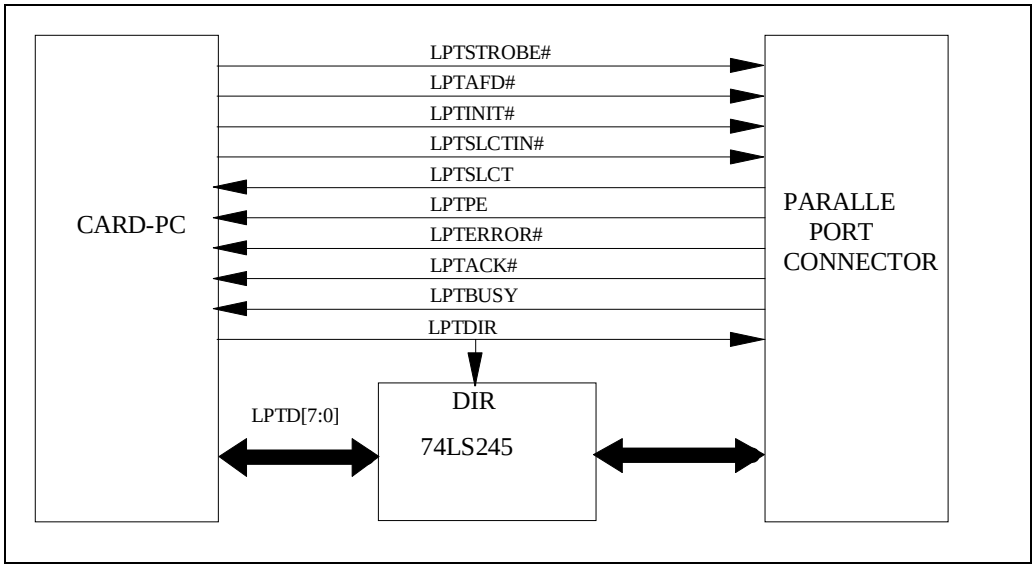


Figure 5.5.3 PS/2 style bi-directional parallel port interface

5.5.5 Pin configuration

Table 5.5.2 shows the pin assignments for ISA parallel port and high-speed parallel port mode.

Table 5.5.2 25-pin Connector Pin Assingment

Pin	Standard Mode	EPP Mode
1	STROBE#	WRITE#
2	PPD0	PPD0
3	PPD1	PPD1
4	PPD2	PPD2
5	PPD3	PPD3
6	PPD4	PPD4
7	PPD5	PPD5
8	PPD6	PPD6
9	PPD7	PPD7
10	ACK#	INTR#
11	BUSY	WAIT#
12	PE#	PE#
13	SLCT#	SLCT#
14	AFDXT#	DSTRB#
15	ERROR	ERROR
16	INIT	INIT
17	SLCTIN#	ADSTB#
18	GND	GND
19	GND	GND
20	GND	GND
21	GND	GND
22	GND	GND
23	GND	GND
24	GND	GND
25	GND	GND

5.6 Power Management

CARD-486HB/486HBL supports power management functions. The features of this system are:

*Suspend, resume function
  -Support for suspend/resume button
  -Suspend timer possible
*Support for output pins for programmable system power management
*Support for battery monitor pin

5.6.1 Power management signals

System Management OUTput (SMOUT [3:0])
These signals activate the idle state of various devices for power control. Refer to “Minimizer SMOUT Pin Assignments” in the *BIOS Reference Manual* for details of each signal.

SUSpend STATus (SUSSTAT#)
This signal indicates that CARD-486HB/486HBL is in the suspended state. This signal can also be used as a power supply control signal.

EXTernal System Management Interrupt (EXTSMI#)
This signal is used to request a system management interrupt from CARD-486H/486HBL.

Suspend Resume BuTtoN (SRBTN#)
This input signal is used to enter the suspended state and to wake up from the suspended state.

BATTery WARNing (BATTWARN#)
This input signal is used to warn when the battery's remaining capacity is low.
When this warning is issued, a warning beep is sounded by the speaker interface.

BATTery LOW (BATTLOW#)
When this signal goes active (when the battery capacity has dropped), CARD-486HB/486HBL either issues a warning or enters the suspended state.

BATTery DEAD (BATTDEAD#)
This signal indicates to the system that there is insufficient battery power to operate the system.

POWERGOOD
This signal indicates that the system power supply is normal. POWERGOOD goes active when the system power supply is within the prescribed voltage range. Timing rules are described later.

For further details on power management, refer to the BIOS reference manual.

5.6.2 Suspend and Resume Control

The CARD-486HB/486HBL supports functions to suspend the system, and thereafter to resume, that is, to return to the state immediately before the suspension. The suspend function puts all the CARD-486HB/486HBL devices in the power save mode, and maintains the system in a low power consumption state.

Depending on the operating mode of the CARD-486HB/486HBL, it is possible to switch to the suspend state automatically. It is also possible to suspend the system under the control of the suspend/resume button (SRBTN#) input, from low battery detection, or by software. For details, refer to the BIOS reference manual.

Fig. 5.6.1 is a block diagram of the suspend/resume circuit.

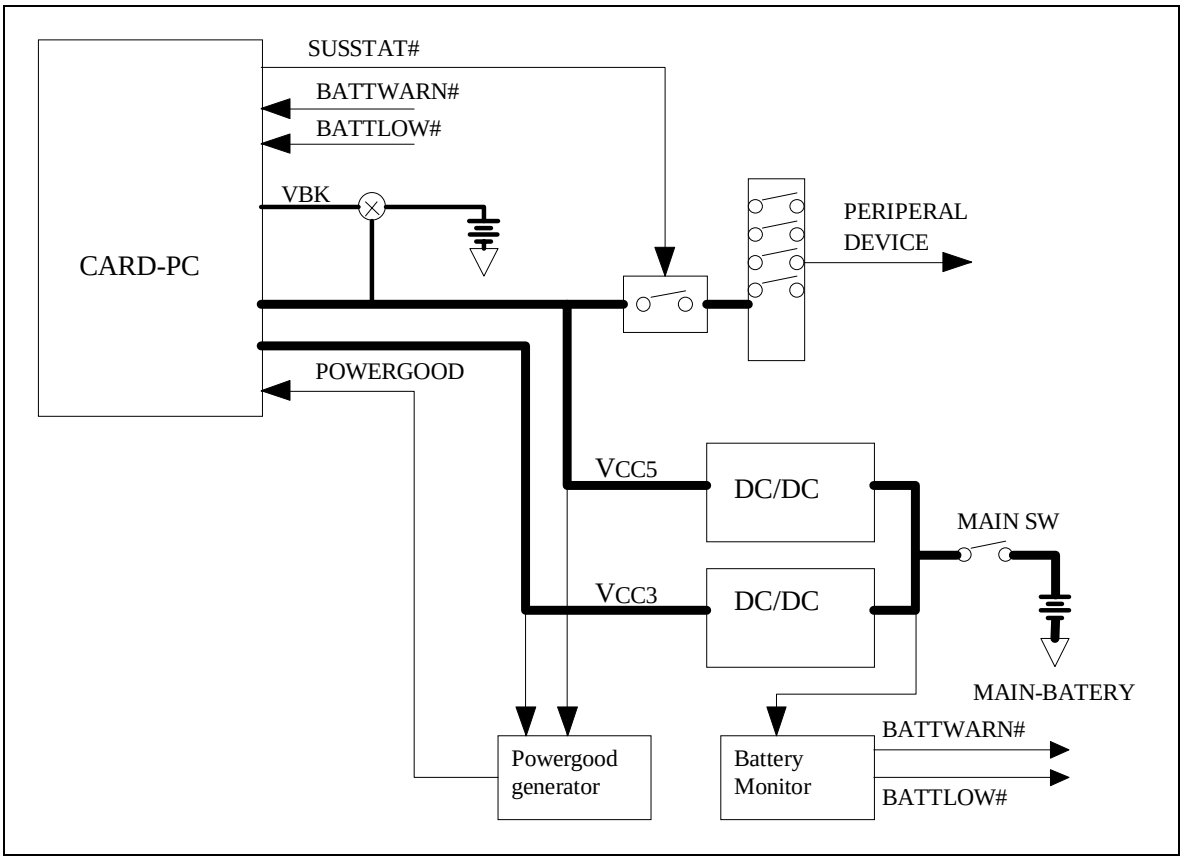


Figure 5.6.1 Suspend/Resume Block Diagram

The power supply to the CARD-486HB/486HBL is from MAIN-BATTERY. When the system is suspended, SUSSTAT# (active low signal, low in the suspend state) stops power supply to devices other than the CARD-486HB/486HBL. At this time, the CARD-486HB/486HBL is in the suspended state, and the main memory, video memory, and registers are maintained by a low capacity power supply.

The POWERGOOD signal indicates the state of the power supply (V_{CC5}, V_{CC3}), and is supplied to the CARD-486HB/486HBL. Also the BATTWARN# and BATTLOW# signals are supplied to the CARD-486HB/486HBL for system power supply monitoring. While the system is operating, if BATTLOW# becomes active, a speaker alarm is given to indicate that the battery capacity is low. When this signal is inactive the CARD-486HB/486HBL does not resume. The resume operation is started by an RTC alarm, modem ring, or SRBTN# input. When the resume state machine resumes, SUSTAT# is sent high, and RESETDRV is issued.

5.7 Keyboard Controller

The CARD-486HB/486HBL keyboard controller is emulated in software, to be function-compatible with an 8042. Its principal functions are as follows:

*AT-and PS/2-compatible standard command support
*Standard AT and PS/2 keyboard support
*PS/2-compatible mouse support

5.7.1 Signals concerning the keyboard controller

KeyBoard CLocK (KBCLK)
Clock signal for the keyboard interface

KeyBoard DATA (KBDATA)
Data signals for the keyboard interface

MouSe CLocK (MSCLK)
Clock signal for the mouse interface

MouSe DATA (MSDATA)
Data signals for the mouse interface

5.7.2 Explanation of registers and commands

The register and commands are briefly described below.

Status register 064h read only

BIT	PS/2 Compatible Mode
7	Parity Error Flag
6	General Time Out
5	Aux. Data Flag
4	Keyboard Password Unlocked
3	Command Flag
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Output buffer 060h read only
Port for outputting scan codes received by this controller from the keyboard.

Input buffer 060h write only
Port for data input to this controller.

Command register 064h write only
Port for command output to this controller. The following commands are supported:

Standard Keyboard Commands
- Set/Reset Status Indicators Command(0EDh)
- Echo Command(0EEh)
- Select Alternate Scan Code Command(0F0h)
- Read ID Command(0F2h)
- Set Typematic Rate/Delay Command(0F3h)
- Enable Command(0F4h)
- Default Disable Command(0F5h)
- Set Default Command(0F6h)
- Set Keys Command(0F7h-0FDh)
- Reset Command(0FFh)

Standard Controller Command
- Write Controller Command Byte(60h)
- Read Controller Command Byte(20h)
- Test Password Installed(0A4h)
- Load Password(0A5h)
- Enable Password(0A6h)
- Diable Auxiliary Device Interface(0A7h)
- Enable Auxiliary Device Interface(0A8h)
- Test Auxiliary Device Interface(0A9h)
- Self Test(0AAh)
- Keyboard Interface Test(0ABh)
- Disable Keyboard Interface(0ADh)
- Enable Keyboard Interface(0AEh)
- * Read Input Port(0C0h)
- * Read Output Port(0D0h)
- * Write Output Port(0D1h)
- Write Keyboard Output Buffer(0D2h)
- Write Auxiliary Output Buffer(0D3h)
- Write Auxiliary Device Command(0D4h)
- * Read Test Input Command(0E0h)
- Pulse Both Reset and Gate A20(0FCh)

* In the Read Input Port (0C0h) command, the value returned is not a physical input port value, but an emulated value.
The Read Output Port (0D0h) command also returns not a physical input port value, but an emulated value. All that can be changed by Write Output Port (0D1h) is bit 1, Gate A20 control, and other bits are ignored.
In the Read Test Input Command (0E0h) command, the value returned is not a physical Test Input Port value, but an emulated value.

5.7.3 Keyboard and mouse interfaces

Fig.5.7.1 illustrates the keyboard and mouse interfaces.

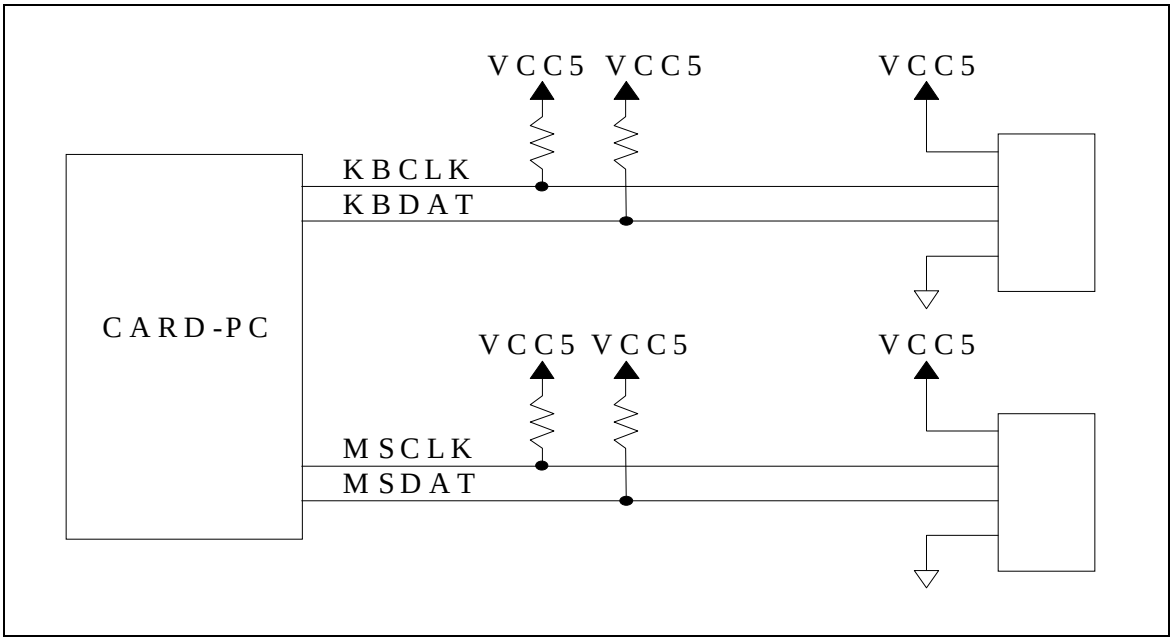


Figure 5.7.1 Mouse/Keyboard Connection Sample

Control the keyboard and mouse power supply simultaneously with the card power supply. Check the keyboard and mouse specifications before determining the external resistance value.

5.8 VGA Controller

The CARD-486HB is equipped with an Seiko Epson SPC8110 as display controller. The following are some of its features:

- Standard VGA mode support
- Simultaneous CRT and LCD display
- Suspend function support
- 256/256K color display
- Monochrome STN-LCD 64 gray level display
- Color STN-LCD support
- 256K-color TFT color LCD support
- Direct CRT and LCD connection possible

5.8.1 CRT and LCD interface signals

This system is equipped with a CRT interface and an LCD interface. The signals used in these interfaces are described below.

CRT interface signals

Horizontal SYNC (HSYNC)
Horizontal snchronization signal for the monitor

Vertical SYNC (VSYNC)
Vertical synchronization signal for the monitor

RED video (RED)
This analog output supplies current corresponding to the red pixels to be displayed.

GREEN video (GREEN)
This analog output supplies current corresponding to the green pixels to be displayed.

BLUE video (BLU)
This analog output supplies current corresponding to the blue pixels to be displayed.

LCD interface signals

Flat Panel Vertical Timing (FPVTIM)
Indicates the start of a new frame for a flat panel display.

Flat Panel Horizontal Timing (FPHTIM)
This signal advances the row shift register for an LCD panel display.

Flat Panel Blank (BLANK#)
This signal indicates the blanking interval in which data should not be displayed on a TFT LCD panel. This controls the display enable signal for a TFT LCD panel.

Flat Panel Dot Clock (FPDOTCLK)
Dot shift clock for a flat panel display.

Extended Panel Dot Clock (EXDOTCLK)
This is a special LCD panel dot clock, which is normally not used.

Flat Panel Data (LD [17:0])
Display data for a flat panel display.

Flat Panel Vcc On (FPVCCON)
This signal controls the LCD panel logic power supply, and is used together with FPVEEON. This is used to power the panel on and off.

Flat Panel Vee On (FPVEEON)
This signal controls the LCD panel drive power supply, and is used together with FPVCCON. This is used to power the panel on and off.

5.8.2 Video modes

The CRT and LCD video modes supported by this system are described below.

CRT Video Mode

Mode NO.	No. of Colors	Char.x Row	Char Cell	Screen Format	Display Mode	Hori. Freq. KHz	Verti Freq. Hz
0,1	16/256k	40x25	9x16	360x400	Text	31.5	70
2,3	16/256k	80x25	9x16	720x400	Text	31.5	70
4,5	4/256k	40x25	8x8	320x200	Graphics	31.5	70
6	2/256k	80x25	8x8	640x200	Graphics	31.5	70
7	Monochrome	80x25	9x16	720x400	Text	31.5	70
D	16/256k	40x25	8x8	320x200	Graphics	31.5	70
E	16/256k	80x25	8x14	640x200	Graphics	31.5	70
F	Monochrome	80x25	8x14	640x350	Graphics	31.5	70
10	16/256k	80x25	8x14	640x350	Graphics	31.5	70
11	2/256k	80x30	8x16	640x480	Graphics	31.5	60
12	16/256k	80x30	8x16	640x480	Graphics	31.5	60
13	256/256k	40x25	8x8	320x200	Graphics	31.5	70
100	256/256k	80x50	8x8	640x400	Graphics	31.5	70
101	256/256k	80x60	8x8	640x480	Graphics	31.5	60
102,6A	16/256k	100x75	8x8	800x600	Graphics	48	72
103	256/256k	100x75	8x8	800x600	Graphics	34	51.5
104	16/256k	128x96	8x8	1024x768	Graphics	48	60

LCD Video Mode

Mode No.	Mono. STN Number of gray scale	Color STN Number of colors	Color TFT Number of colors	Char.x Row	Char. Cell	Screen format	Display Mode
0,1	16	16/256K	16/256K	40x25	9x16	360x400	Text
2,3	16	16/256K	16/256K	80x25	9x16	720x400	Text
4,5	4	4/256K	4/256K	40x25	8x8	320x200	Graphics
6	2	2/256K	2/256K	80x25	8x8	640x200	Graphics
7	2	Mono.	Mono.	80x25	9x16	720x400	Text
D	16	16/256K	16/256K	40x25	8x8	320x200	Graphics
E	16	16/256K	16/256K	80x25	8x14	640x200	Graphics
F	2	Mono.	Mono.	80x25	8x14	640x350	Graphics
10	16	16/256K	16/256K	80x25	8x14	640x350	Graphics
11	2	2/256K	2/256K	80x30	8x16	640x480	Graphics
12	16	16/256K	16/256K	80x30	8x16	640x480	Graphics
13	64	256/256K	256/256K	40x25	8x8	320x200	Graphics
100	64	256/256K	256/256K	80x50	8x8	640x400	Graphics
101	64	256/256K	256/256K	80x60	8x8	640x480	Graphics
102,6A	64	16/256K	16/256K	100x75	8x8	800x600	Graphics
103	64	256/256K	256/256K	100x75	8x8	800x600	Graphics
104	64	16/256K	16/256K	128x96	8x8	1024x768	Graphics

5.8.3 Panel interface

A representative example of the connections between this system and a dual-scan monochrome monitor is shown below.

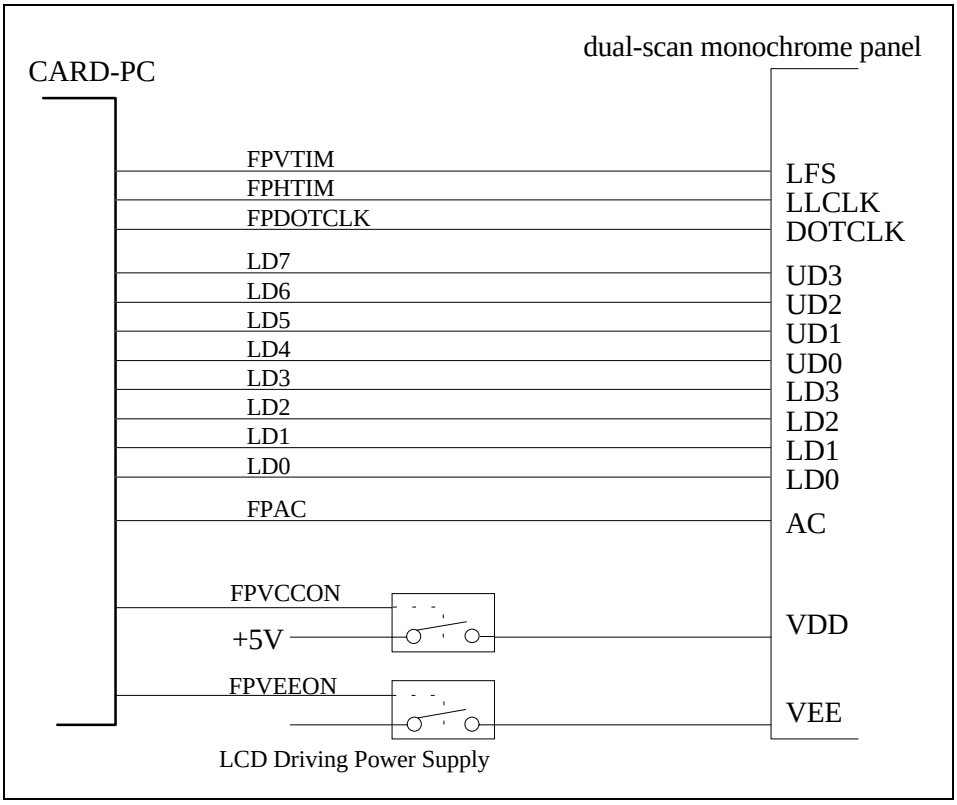


Figure 5.8.1 Dual-scan Monochrome Panel Connection Sample

The following description covers the principal panel interfaces supported by this system.

● 640 × 480 Monochrome Dual Panel (8 bit)

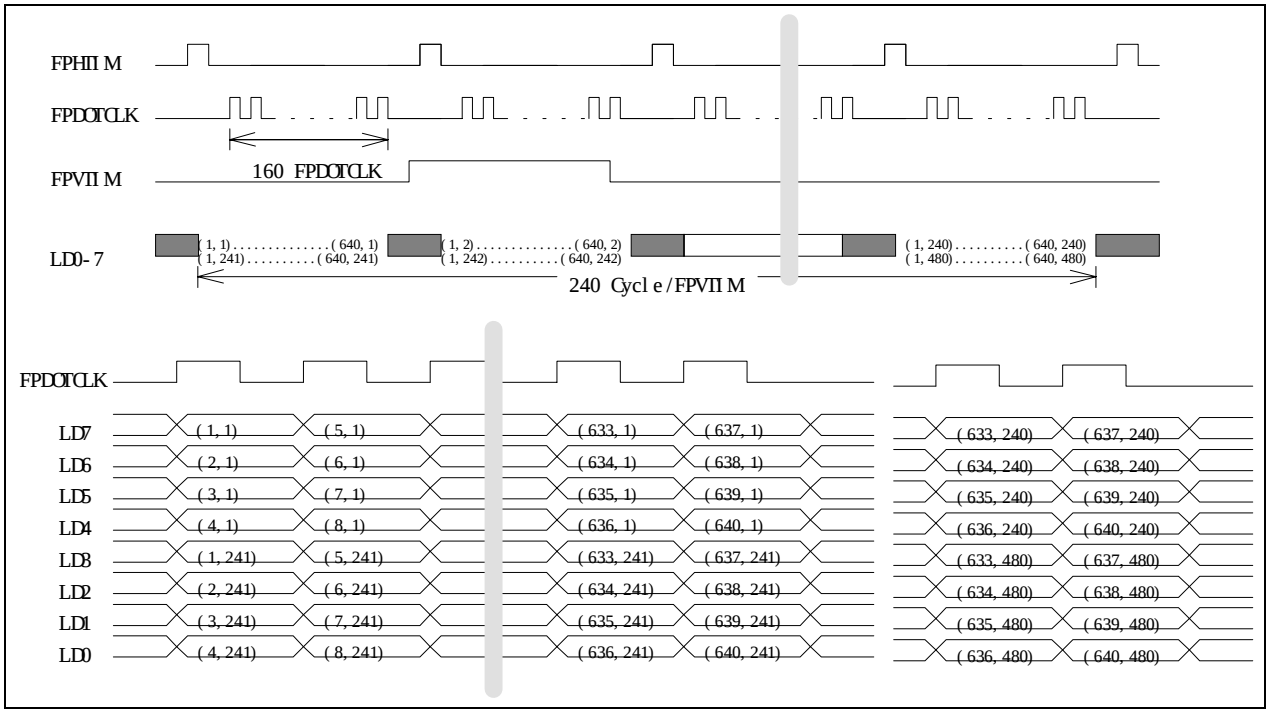


Figure 5.8.2 8 bit Monochrome Dual Panel Interface

● 640 × 480 Single Monochrome Panel (8 bit)

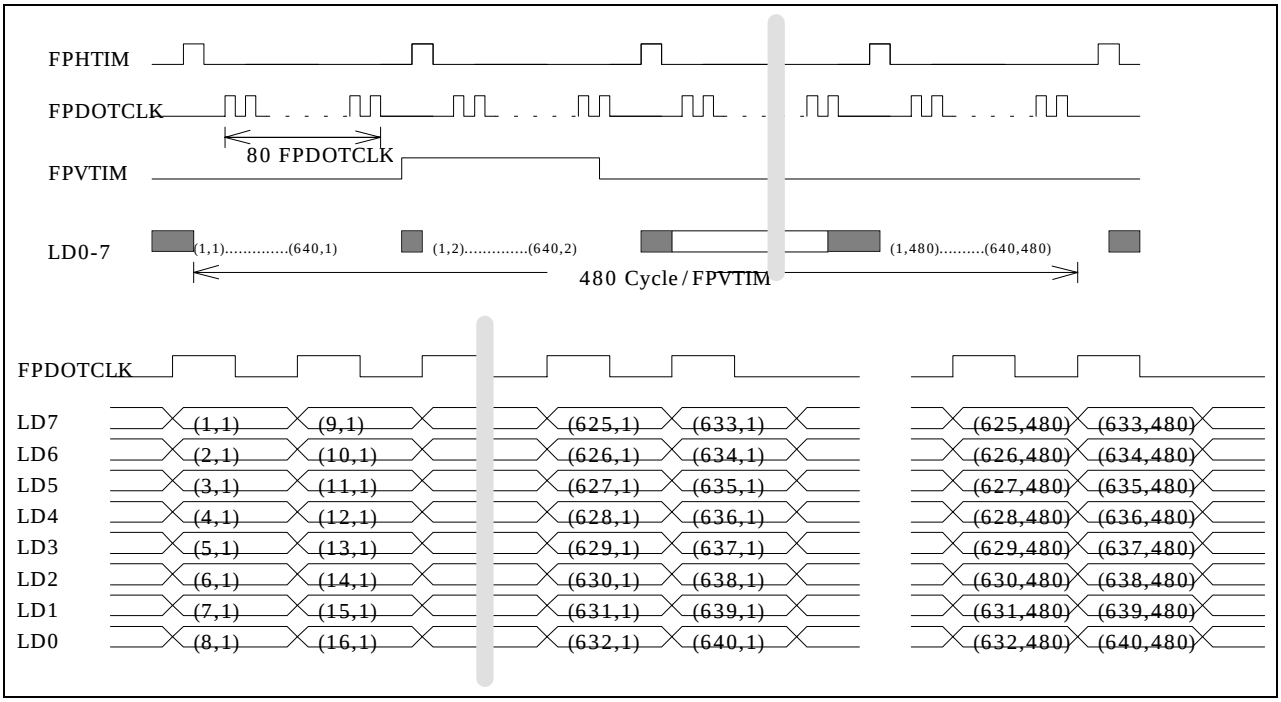


Figure 5.8.3 8 bit Monochrome Single Panel Interface

● 640 × 480 TFT color panel

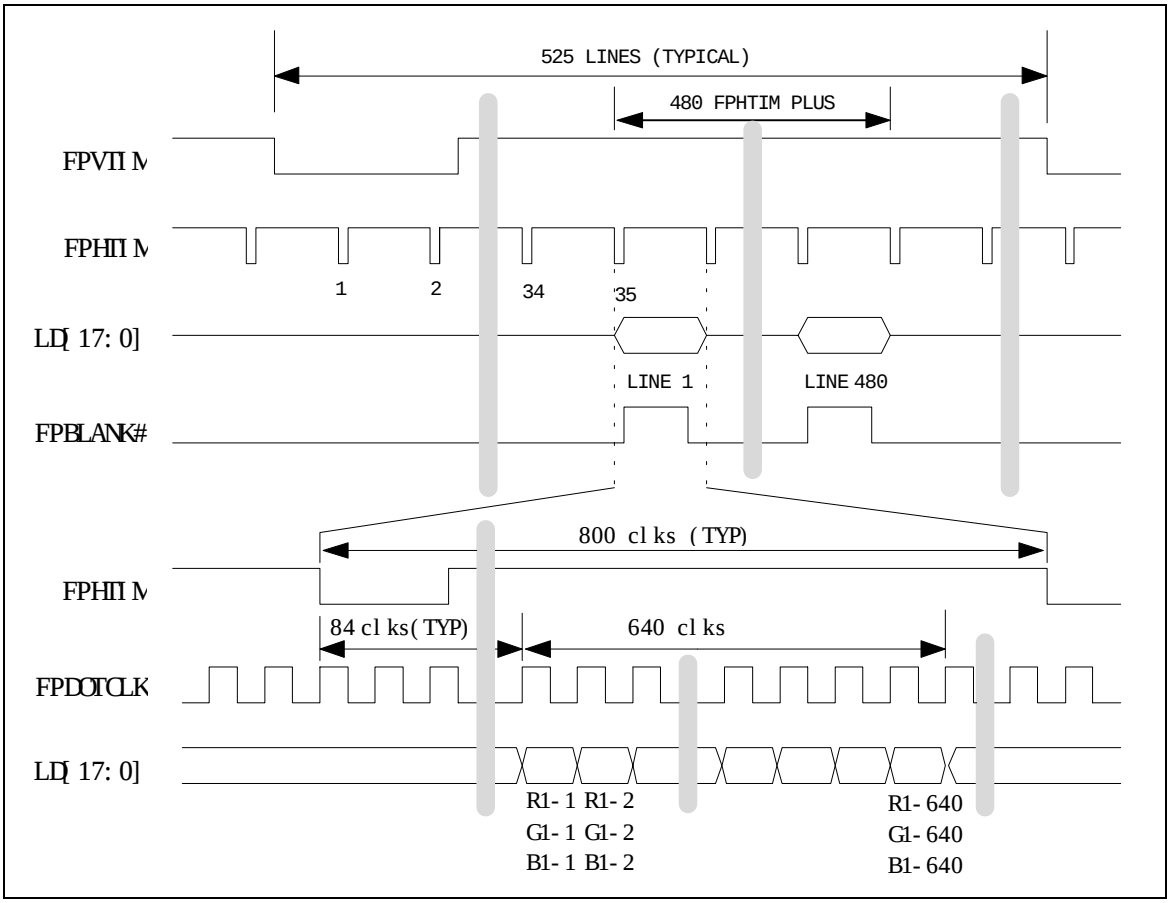


Figure 5.8.4 TFT Color Panel

The LCD panel requires special control with respect to the logic power supply, liquid crystal drive power supply, and control signals. For the CARD-486HB to meet these requirements, a ROM Adaptation Kit (RAK) can be used, and control carried out as shown in Fig. 5.8.5.

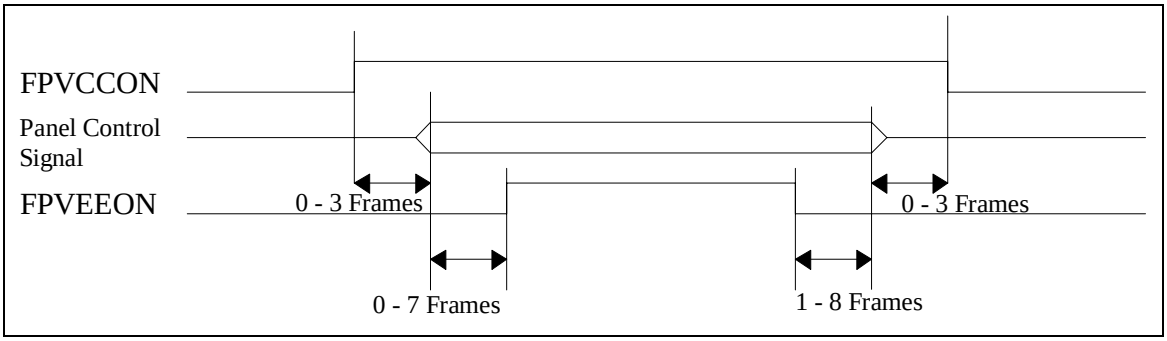


Figure 5.8.5 Panel Power Supply Control Timing

The panel connections differ according to the manufacturer of the panel and according to the panel settings. Therefore, it is necessary to check the specific connection requirements of the panel to be used.

5.9 Floppy Disk Controller

CARD-486HB is equipped with an IBM PC/AT-compatible floppy disk controller. The features of the FDD interface are:

*Permits connection with up to two drives
*Supports both 5-inch and 3.5-inch FDDs
*Supports transfer rates of 250Kbps, 300Kbps, and 500Kbps
*Built-in driver/receiver for the drives (drive current I_{OL}=38mA)
*Two-mode floppy disk drive support

5.9.1 Floppy disk control signals

DRIVE SELECT 1 (FDDS1#)
Drive 1 select signal.

DRIVE SELECT 2 (FDDS2#)
Drive 2 select signal.

MOTOR ON 1 (FDMT1#)
"Motor on" signal for drive 1.

MOTOR ON 2 (FDMT2#)
"Motor on" signal for drive 2.

STEP (FDSTEP#)
Step pulse signal that indicates the number of steps the head is to move.

DIRECTION (FDDIR)
This signal indicates the direction of a seek operation. LOW indicates the seek is towards the inner track, and HIGH indicates that the seek is towards the outer track.

SIDE (FDSIDE)
This signal selects head 0 or head 1. LOW selects head 1, HIGH selects head 0.

READ DATA (FDRD#)
Input for data read from the drive.

WRITE DATA (FDWD#)
Output for data to be written to the drive.

WRITE ENABLE (FDWE#)
This signal instructs the drive to write

WRITE PROTECT (FDWP#)
This signal from the drive indicates that the media is write-protected.

DISK CHANGE (FDDCHG#)
Disk change signal from the drive.

INDEX (FDINDEX#)
Drive index detection signal.

TRACK 0 (FDTRK0#)
This signal indicates that the head is positioned at track 0.

HIGH DENSITY SELECT (FDHIDEN)
When this signal is high it indicates high density.
According to the BIOS settings, this signal can also be used for the mode setting signal for three-mode floppy disk drive support.

5.9.2 Floppy disk interface

Floppy Disk Interface I/O Ports

I/O Address	Decription
3F2H WO	Digital output register Bit7 : Reserved Bit6 : Reserved Bit5 : Drive 2 Motor Enable Bit4 : Drive 1 Motor Enable Bit3 : Enable Diskette Interrupt and DMA Bit2 : Diskette Function Reset Bit1 : Reserved Bit0 : Drive Select 0-Drive1, 1-Drive2
3F4H	Main Status register
3F5H	Data register
3F7H WO	FDD Control Resister Bit 1 Bit 0 0 0 500 Kbps 0 1 300 Kbps 1 0 250 Kbps 1 1 reserved
3F7H RO	Digital Input Register Bit7 : Diskette Change Bits [0-6] : Hard DISK Controller

A typical connection example for a floppy disk drive is shown in Fig.5.9.1.

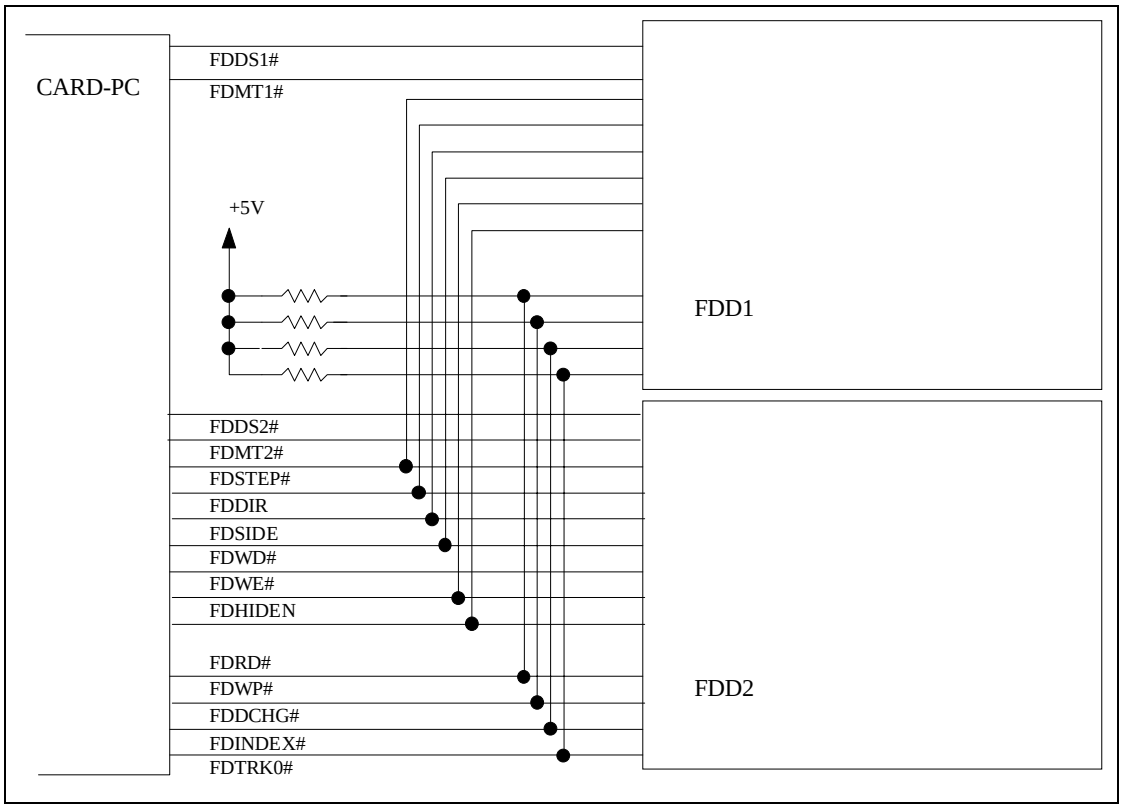


Figure 5.9.1 Floppy Disk Drive Connection Sample

Set the external resistance according to the characteristics of the floppy disk drive.

5.10 RTC and CMOS RAM Interface

CARD-486HB/486HBL has a built-in RTC (for clock and calendar functions) and CMOS RAM that can be backed up. Because this interface is provided with pins for backing up the RTC and CMOS RAM, it is necessary to supply power form a battery or other source when providing backup. When this is not used, the BIOS is used to save the contents of CMOS memory. For details, refer to the BIOS reference manual.

5.10.1 Description of Registers

CARD-486HB/486HBL is equipped with an ISA standard RTC (MC146818). The contents of the RTC can be preserved even when power is not supplied to the system, as long as power is supplied to the VBK pin.

The CMOS RAM built into the CARD-486HB/486HBL stores information required for booting the CARD-486HB/486HBL. When the CARD-486HB/486HBL is booted, expansion devices and system settings are set based on this information. Since with the standard BIOS VBK is not backed up, standard information is always used for booting. As a result, when used in a system configuration other than the standard system configuration, unless a backup power supply is connected to VBK, each time the system is booted it will be necessary to make the configuration settings. If, however, the ROM Adaptation Kit is used to change the standard BIOS settings, a backup is not required, but it will be necessary to reset the real time clock each time.

The CMOS RAM includes 128 bytes of information, including 10 bytes for second, minute, hour, day-of-the-week, day, month, and year, and 4 bytes of control data.
The address map for standard CMOS RAM is shown in the following table.

Index	Register
00H	Second
01H	Second (Alarm)
02H	Minute
03H	Minute (Alarm)
04H	Time
05H	Time (Alarm)
06H	Day of the week
07H	Day
08H	Month
09H	Year
0AH	Control Register A
0BH	Control Register B
0CH	Control Register C
0DH	Control Register D
0EH~7FH	Data Area

The RTC is accessed via the RTC index and data ports. Standard CMOS RAM is accessed via I/O ports 70H and 71H.

I/O Address	R/W	Description
0070H	R/W	CMOS RAM address port Bit 7 = NMI Mask 1- disable, 0- enable Bit 0-6 = Standard CMOS RAM INDEX
0071H	R/W	CMOS RAM data port

5.10.2 VBK

This pin is provided for backup for the real time clock, CMOS RAM, and resume state machine. When power is supplied to the CARD-486HB/486HBL (in operation), the same power supply as VCC5 is supplied. For CMOS RAM backup, it is necessary to switch to a backup power supply (lithium battery etc.) in coordination with the CARD-486HB/486HBL power off timing.

An example circuit for switching the power supply is shown in Fig.5.10.1.

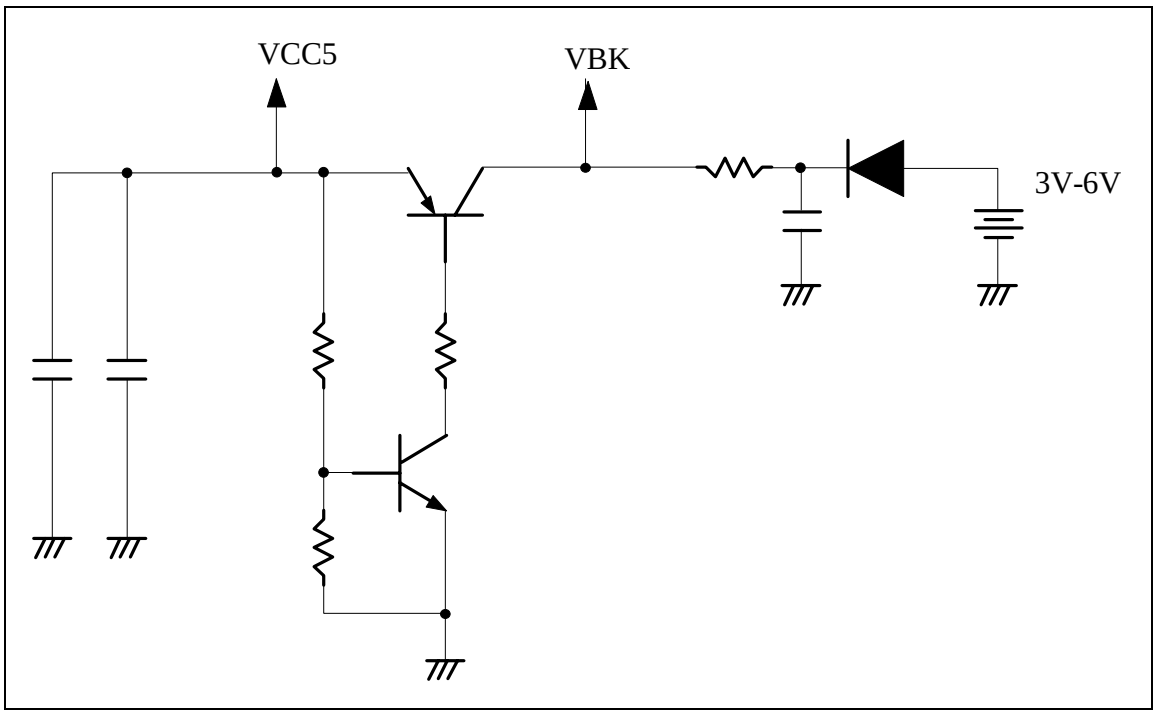


Figure 5.10.1 Example VBK Power Supply Switching Circuit

6. ENVIRONMENTAL CONDITIONS

6.1 Operating temperature (operating)

SCE8643600, SCE8643603	Ta 0 to 55°C or Tc 0 to 70°C
SCE8643605	Ta 0 to 50°C or Tc 0 to 70°C
SCE8640600, SCE8640603	Ta 0 to 65°C or Tc 0 to 70°C

Ta is specified with the supply voltage at its typical value.

For the specified position for Tc refer to Fig. 6.1.1.
The card PC operating temperature is satisfactory provided that either of the Ta or Tc specifications is met. It is not necessary to meet both specifications.

Operating temperature (suspended): Ta 0 to 70°C all models

Storage temperature: Ta -20 to 75°C all models (with no condensation)

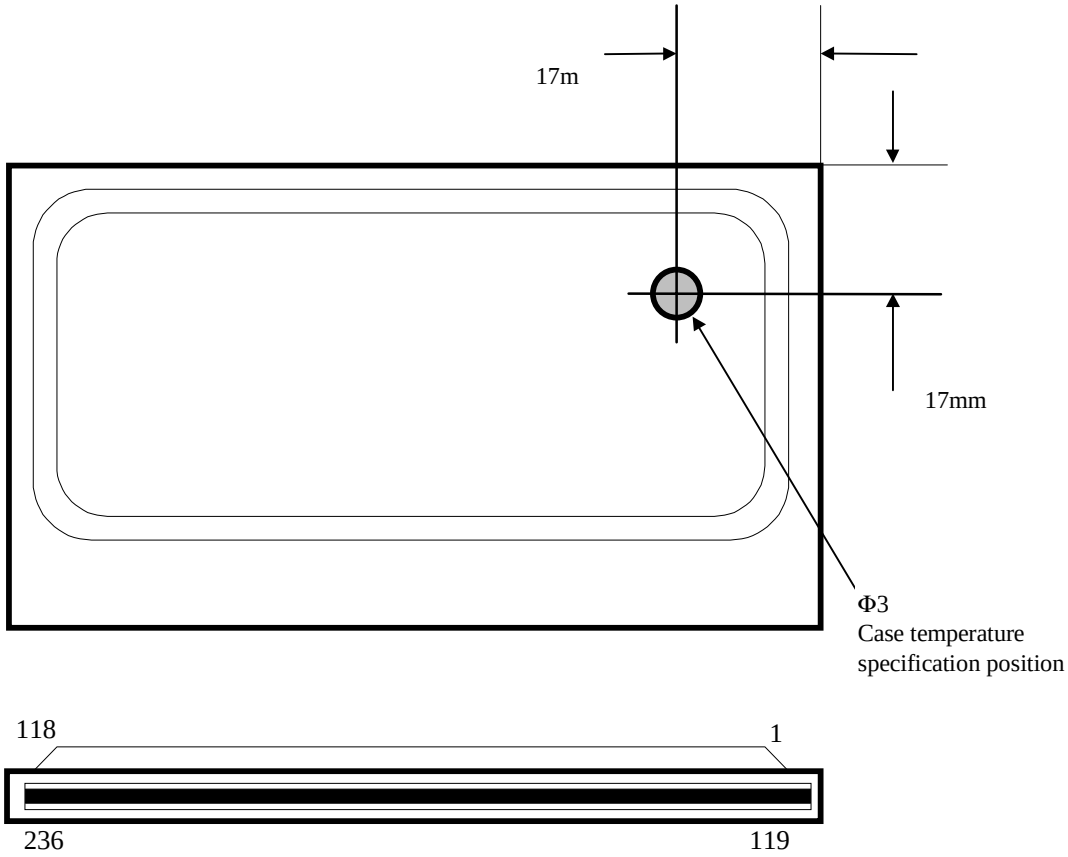


Fig. 6.1.1 Case surface temperature specification position when operating

6.2 Humidity

Storage humidity: 0% to 90% (with no condensation)

6.3 WITHSTANDING ELECTROSTATIC DISCHARGE

15kV, 100pF, 1.5kΩ (with no damage to the device)

7. MECHANICAL CHARACTERISTICS

7.1 Insertion/Removal Force

Insertion Force: No more than 98.0N (10kgf)
Removal Force: At least 9.8N (1kgf)

7.2 Bending

Apply 19.6N (2Kgf) to the unsupported end of the card while the other end is held in place. Once per side.

7.3 Dropping

From a height of 75cm on vinyl tile, twice in each of three directions

7.4 Twisting

1.23Nm (12.6kgcm), held for 5 minutes, repeated for 5 cycles

7.5 Operating Vibration

1.5G, full amplitude of 0.7mm, 10 to 55Hz, XYZ (when using the SEK6676P01 stopper)

7.6 Insertion/Removal

1000 times (using the special connector)

7.7 Load

98N (10Kgf)

8. Maximum Ratings

Item		Rating
Temperature under Bias		Ta 0 to 70°C
Storage Temperature		Ta -20 to 75°C
Supply Voltage	Vcc3	-0.3 to 4.6V
	Vcc5	-0.3 to 6V
	VBK	-0.3 to 6V
	VPGM	-0.3 to 14V
Input/Output Voltage		-0.3 to Vcc+0.5V

9. DC CHARACTERISTICS (Recommended and Nominal)

Power Source

Symbol	Parameter	Min	Max	Unit	Note
V_{CC5}	Supply Voltage	4.75	5.25	V	Indicated in the pin assignment diagram as VCC5
V_{CC3}	Supply Voltage	3.0	3.6	V	Indicated in the pin assignment diagram as VCC3
V_{BK}	Supply Voltage	2.5	---	V	In normal operation the same as VCC5
V_{PGM}	Supply Voltage	0	6.5	V	For flash reads
V_{PGM}	Supply Voltage	11.4	12.6	V	For flash writes; the power for writing must be supplied after VCC5 and VCC3 have settled. I=30mA (Max)

PWRGOOD signal

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	---	0.8	V	Refer to Fig. 9.15. Must not exceed 0.8V when backing up the RTC.
V_{IH}	Input High Voltage	4.0	V_{CC5}+0.3	V	

ISA Bus Interface Section

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=2mA	---	0.4	V	Applies to IRQ6 and DRQ2.
V_{OH}	Output High Voltage I_{OH}=-2mA	2.4	---	V	Applies to IRQ6 and DRQ2.
V_{OL}	Output Low Voltage I_{OL}=8mA	---	0.4	V	Applies to DACK0, 1, 2, 3 5, 6 and 7#, and to IRQ3, 4, 5, 7, 10, 11, and 12.
VOH	Output High Voltage I_{OH}=-8mA	2.4	---	V	Applies to DACK0, 1, 3, 5, 6 and 7#, and to IRQ3, 4, 5, 7, 10, 11, and 12.
V_{OL}	Output Low Voltage I_{OL}=12mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-12mA	2.4	---	V	
V_{OL}	I_{OH}=12mA Open Drain Output	2.4	---	V	Applies to the IOCHRDY and REF# pins.

Serial Interface

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=8mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-8mA	2.4	---	V	
V_{OL}	Output Low Voltage I_{OL}=24mA	---	0.4	V	Applies to IRTXD.
V_{OH}	Output High Voltage I_{OH}=-12mA	2.4	---	V	Applies to IRTXD.

Parallel Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=8mA		0.4	V	
V_{OH}	Output Low Voltage I_{OH}=-8mA	2.4	---	V	
V_{OL}	Output Low Voltage Open Drain Output I_{OL}=12mA		0.4	V	Applies to LPTSTROBE#, LPTAFD#, LPTINIT#, and LPTSLCTIN#.

Floppy Disk Drive Interface

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage Open Drain Output I_{OL}=38mA	---	0.4	V	

LCD Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{OL}	Output Low Voltage I_{OL}=24mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-8mA	4.0	---	V	
V_{OL}	Output Low Voltage I_{OL}=6mA	---	0.4	V	Applies to FPVCCON and FPVEEON.
V_{OH}	Output High Voltage I_{OH}=-2mA	4.0	---	V	Applies to FPVCCON and FPVEEON.

Mouse/Keyboard Interface

Symbol	Parameter	Min	Max	Unit	Note
V_{T+}	Input Low Voltage	-0.5	0.6	V	
V_{T-}	Input High Voltage	2.4	V_{CC5}+0.5	V	
V_{IH}	Input Hysteresis Voltage	0.1	---	V	
V_{OL}	Output Low Voltage Open Drain Output I_{OL}=24mA	----	0.4	V	

IDE Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=12mA	---	0.4	V	Applies to HD7, HDCS0#, and HDCS1#.
V_{OH}	Output High Voltage I_{OH}=-12mA	2.4	---	V	Applies to HD7, HDCS0#, and HDCS1#.
V_{OL}	Output Low Voltage I_{OL}=4mA	---	0.4	V	Applies to HDIR, HDENL#, and HDENH#.
V_{OH}	Output High Voltage I_{OH}=-4mA	2.4	---	V	Applies to HDIR, HDENL#, and HDENH#.

Power Management Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=8mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-8mA	2.4	---	V	

Speaker Interface
ROM Update Interface
Watchdog Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=4mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-4mA	2.4	---	V	

Current Consumption

SCE8643600 (CARD-486HB 16MHz 1Mbyte RAM) Tc=0 to 70°C

Item	Conditions	Standard			Unit
		Min.	Typ.	Max.	
Operating current consumption I_{CC3}	When operating (MS-DOS prompt) V_{CC3}=3.3V±0.3V	---	320	450	mA
Operating current consumption I_{CC5}	When operating (MS-DOS prompt) V_{CC5}=5.0V±5%	---	55	85	mA
Current in suspended state I_{CC3}	In suspended state V_{CC3}=3.3V±0.3V	---	0.4	1.2	mA
Current in suspended state I_{CC5}	In suspended state V_{CC5}=5.0V±5%	---	0.3	0.9	mA
Backup current I_{BK}	During backup V_{BK}=3.0V	---	3.0	15.0	µA

SCE8643603 (CARD-486HB 16MHz 4Mbyte RAM) Tc=0 to 70°C

Item	Conditions	Standard			Unit
		Min.	Typ.	Max.	
Operating current consumption I_{CC3}	When operating (MS-DOS prompt) V_{CC3}=3.3V±0.3V	---	320	450	mA
Operating current consumption I_{CC5}	When operating (MS-DOS prompt) V_{CC5}=5.0V±5%	---	55	85	mA
Current in suspended state I_{CC3}	In suspended state V_{CC3}=3.3V±0.3V	---	0.4	1.2	mA
Current in suspended state I_{CC5}	In suspended state V_{CC5}=5.0V±5%	---	0.3	0.9	mA
Backup current I_{BK}	During backup V_{BK} =3.0V	---	3.0	15.0	µA

SCE8643605 (CARD-486HB 33MHz 4Mbyte RAM) Tc=0 to 70°C

Item	Conditions	Standard			Unit
		Min.	Typ.	Max.	
Operating current consumption I_{CC3}	When operating (MS-DOS prompt) V_{CC3}=3.3V±0.3V	---	450	700	mA
Operating current consumption I_{CC5}	When operating (MS-DOS prompt) V_{CC5}=5.0V±5%	---	55	85	mA
Current in suspended state I_{CC3}	In suspended state V_{CC3}=3.3V±0.3V	---	0.4	1.2	mA
Current in suspended state I_{CC5}	In suspended state V_{CC5}=5.0V±5%	---	0.3	0.9	mA
Backup current I_{BK}	During backup V_{BK} =3.0V	---	3.0	15.0	µA

SCE8640600 (CARD-486HBL 16MHz 1Mbyte RAM) Tc=0 to 70°C

Item	Conditions	Standard			Unit
		Min.	Typ.	Max.	
Operating current consumption I_{CC3}	When operating (MS-DOS prompt) V_{CC3}=3.3V±0.3V	----	145	220	mA
Operating current consumption I_{CC5}	When operating (MS-DOS prompt) V_{CC5}=5.0V±5%	----	10	16	mA
Current in suspended state I_{CC3}	In suspended state V_{CC3}=3.3V±0.3V	----	0.2	0.6	mA
Current in suspended state I_{CC5}	In suspended state V_{CC5}=5.0V±5%	----	0.2	0.6	mA
Backup current I_{BK}	During backup V_{BK}=3.0V	----	3.0	15.0	µA

SCE8640603 (CARD-486HBL 16MHz 4Mbyte RAM) Tc=0 to 70°C

Item	Conditions	Standard			Unit
		Min.	Typ.	Max.	
Operating current consumption I_{CC3}	When operating (MS-DOS prompt) V_{CC3}=3.3V±0.3V	----	145	220	mA
Operating current consumption I_{CC5}	When operating (MS-DOS prompt) V_{CC5}=5.0V±5%	----	10	16	mA
Current in suspended state I_{CC3}	In suspended state V_{CC3}=3.3V±0.3V	----	0.2	0.6	mA
Current in suspended state I_{CC5}	In suspended state V_{CC5}=5.0V±5%	----	0.2	0.6	mA
Backup current I_{BK}	During backup V_{BK}=3.0V	----	3.0	15.0	µA

Pin Electrical Characteristics

This section describes the characteristics of each pin in CARD-486HB/486HBL. It also describes the pin states in the suspend state. The following table describes the meanings of the entries in the columns under the various legends.

CARD-486HBL does not have video nor FDD interface.

Characteristic	Identifier of signal
Type	Indicates the pin type I : Input pin O : Output pin O OD : Open drain output IO : Bi-directional IO OD : Input/output; open drain output POWER : Power Supply
Termination	Internal termination resistance and termination method: HOLD : Bus Hold ??PU : ??-Ω pull-up resistance ??PD : ??-Ω pull-down resistance ??ST : ??-Ω damping resistance External : External termination is required
drive	Drive current (mA) for output and bi-directional termination. Denoted I_{OL} and I_{OH} .
susp	State of this pin during the Suspend mode of Power Management This is valid in the system power management functions. Drive : Drive High or Low Drv(0) : Drive Low Drv(1) : Drive High High-Z : High impedance Active : Active Imput : Required fixed input level high or low

Signal Characteristics

Pin	Group (EASI)	Signal name	Type	Termination	drive (mA) IOL,IOH	susp
1	POWER Supply	GND	POWER	---	---	---
2		GND	POWER	---	---	---
3	LCD I/F	EXDOTCLK	O	---	24,-8	Drv(0)
4		LD6	O	---	24,-8	Drv(0)
5		LD4	O	---	24,-8	Drv(0)
6		LD2	O	---	24,-8	Drv(0)
7		LD0	O	---	24,-8	Drv(0)
8		FPVTIM	O	---	24,-8	Drv(0)
9		FPAC	O	---	24,-8	Drv(0)
10		FPVCCON	O	---	6,-2	Drv(0)
11		LD9	O	---	24,-8	Drv(0)
12		LD11	O	---	24,-8	Drv(0)
13		LD13	O	---	24,-8	Drv(0)
14		LD15	O	---	24,-8	Drv(0)
15	CRT I/F	BLUE	O	150PD	---	---
16		GREEN	O	150PD	---	---
17		RED	O	150PD	---	---
18		VSYNC	O	---	12,-4	Drv(0)
19	LCD I/F	LD17	O	---	24,-8	Drv(0)
20		RESERVE	---	---	---	---
21	MOUSE I/F	MSDATA	IO OD	External	24,-	Input
22	KEYBOARD I/F	KBDATA	IO OD	External	24,-	Input
23	FDD I/F	FDWP#	I	External	---	Input
24		FDINDEX#	I	External	---	Input
25		FDTRKO#	I	External	---	Input
26		FDWD#	O OD	External	38,-	High-Z
27	POWER Supply	VCC5	POWER	---	---	---
28		VCC5	POWER	---	---	---
29		VCC3	POWER	---	---	---
30		VCC3	POWER	---	---	---
31	FDD I/F	FDDS2#	O OD	External	38,-	Drv
32		FDMT2#	O OD	External	38,-	Drv
33		FDSIDE	O OD	External	38,-	Drv
34		FDDIR	O OD	External	38,-	Drv
35	SERIAL I/F	RESERVE	---	---	---	---
36		COMBDTR#	O	---	8,-8	High-Z
37		COMBCTS#	I	50KPU	---	Input
38		COMBRTS#	O	---	8,-8	High-Z

Pin	Group (EASI)	Signal name	Type	Termination	drive (mA) I_{OL},I_{OH}	susp
39	SERIAL I/F	COMBDSR#	I	50KPU	---	Input
40		COMADTR#	O	---	8,-8	High-Z
41		COMACTS#	I	50KPU	---	Input
42		COMARTS#	O	---	8,-8	High-Z
43		COMADSR#	I	50KPU	---	Input
44		IRRXD	I	50KPU	---	Input
45	PARALLEL I/F	LPTSTROBE#	IO OD	4.7KPU	12,-	Input/Drive
46		LPTD0	IO	50KPD	8,-8	Input/Drive
47		LPTACK#	I	60KPU	---	Input
48		LPTPE	I	20KPD	---	Input
49		LPTD1	IO	50KPD	8,-8	Input/Drive
50		LPTD2	IO	50KPD	8,-8	Input/Drive
51		LPTD3	IO	50KPD	8,-8	Input/Drive
52		LPTD5	IO	50KPD	8,-8	Input/Drive
53		LPTD7	IO	50KPD	8,-8	Input/Drive
54	IDE I/F	HDIR	O	---	8,-8	Drv(0)
55		HDENL#	O	---	8,-8	Drv(1)
56		HDCS0#	O	---	12,-12	High-Z
57	POWER MANAGEMENT I/F	SUSSTAT#	O	---	8,-8	Drv(0)
58		BATTLOW#	I	50KPU	---	---
59	POWER Supply	GND	POWER	---	---	---
60		GND	POWER	---	---	---
61	POWER MANAGEMENT I/F	BATTWARN#	I	50KPU	---	Input
62		PWRGOOD	I	---	---	---
63	SPEAKER I/F	SPKOUT	O	---	4,-4	Drv(0)
64	ROM UPDATE I/F	FLOAT#	I	25KPU	---	---
65		ROMCE0#	IO	---	4,-4	Drive
66		RESERVE	---	---	---	---
67	ISA Bus	SD7	IO	50KPU	12,-12	Input
68		SD6	IO	50KPU	12,-12	Input
69		SD5	IO	50KPU	12,-12	Input
70		SD4	IO	50KPU	12,-12	Input
71		SD3	IO	50KPU	12,-12	Input
72		SD2	IO	50KPU	12,-12	Input
73		SD1	IO	50KPU	12,-12	Input
74		SD0	IO	50KPU	12,-12	Input
75		IOCHRDY	IO OD	1KPU	12,-	Input
76		AEN	O		12,-12	Drv(0)
77		SA19	IO	HOLD	12,-12	Drive
78		SA18	IO	HOLD	12,-12	Drive

Pin	Group (EASI)	Signal name	Type	Termination	drive (mA) IOL,IOH	susp
79	ISA Bus	SA17	IO	HOLD	12,-12	Drive
80		SA16	IO	HOLD	12,-12	Drive
81		SA15	IO	HOLD	12,-12	Drive
82	POWER Supply	VCC3	POWER	---	---	---
83		VCC3	POWER	---	---	---
84		VCC5	POWER	---	---	---
85		VCC5	POWER	---	---	---
86	ISA Bus	SA14	IO	HOLD	12,-12	Drive
87		SA13	IO	HOLD	12,-12	Drive
88		SA12	IO	HOLD	12,-12	Drive
89		SA11	IO	HOLD	12,-12	Drive
90		SA10	IO	HOLD	12,-12	Drive
91		SA9	IO	HOLD	12,-12	Drive
92		SA8	IO	HOLD	12,-12	Drive
93		SA7	IO	HOLD	12,-12	Drive
94		SA6	IO	HOLD	12,-12	Drive
95		SA5	IO	HOLD	12,-12	Drive
96		SA4	IO	HOLD	12,-12	Drive
97		SA3	IO	HOLD	12,-12	Drive
98		SA2	IO	HOLD	12,-12	Drive
99		SA1	IO	HOLD	12,-12	Drive
100		SA0	IO	HOLD	12,-12	Drive
101		SBHE#	IO	HOLD	12,-12	Drive
102		LA23	IO	HOLD	12,-12	Drive
103		LA22	IO	HOLD	12,-12	Drive
104		LA21	IO	HOLD	12,-12	Drive
105		LA20	IO	HOLD	12,-12	Drive
106		LA19	IO	HOLD	12,-12	Drive
107		LA18	IO	HOLD	12,-12	Drive
108		LA17	IO	HOLD	12,-12	Drive
109		MEMR#	IO	50KPU	12,-12	Drv(1)
110		MEMW#	IO	50KPU	12,-12	Drv(1)
111		SD8	IO	50KPU	12,-12	Input
112		SD9	IO	50KPU	12,-12	Input
113		SD10	IO	50KPU	12,-12	Input
114		SD11	IO	50KPU	12,-12	Input
115	POWER MANAGEMENT I/F	SMOUT3	O	---	8,-8	Drive
116		SMOUT1	O	---	8,-8	Drive
117	POWER Supply	GND	POWER	---	---	---
118		GND	POWER	---	---	---

Pin	Group (EASI)	Signal name	Type	Termination	drive (mA) IOL,IOH	susp
119	POWER Supply	GND	POWER	---	---	---
120		GND	POWER	---	---	---
121	LCD I/F	FPDOTCLK	O	---	24,-8	Drv(0)
122		LD7	O	---	24,-8	Drv(0)
123		LD5	O	---	24,-8	Drv(0)
124		LD3	O	---	24,-8	Drv(0)
125		LD1	O	---	24,-8	Drv(0)
126		FPHTIM	O	---	24,-8	Drv(0)
127		LD8	O	---	24,-8	Drv(0)
128		FPVEEON	O	---	6,-2	Drv(0)
129		BLANK#	O	---	24,-8	Drv(0)
130		LD10	O	---	24,-8	Drv(0)
131		LD12	O	---	24,-8	Drv(0)
132		LD14	O	---	24,-8	Drv(0)
133	CRT I/F	BRTN				
134		GRTN				
135		RRTN				
136		HSYNC	O	---	12,-4	Drv(0)
137	LCD I/F	LD16	O	---	24,-8	Drv(0)
138		RESERVE	---	---	---	---
139	MOUSE I/F	MSCLK	IO OD	External	24,-	Drv(0)
140	KEYBOARD I/F	KBCLK	IO OD	External	24,-	Drv(0)
141	FDD I/F	FDRD#	I	External	---	Input
142		FDDCHG#	I	External	---	Input
143		FDWE#	O OD	External	38,-	High-Z
144		FDHIDEN	O OD	External	38,-	Drv
145	POWER Supply	VCC5	POWER	---	---	---
146		VCC5	POWER	---	---	---
147		VCC3	POWER	---	---	---
148		VCC3	POWER	---	---	---
149	FDD I/F	FDDS1#	O OD	External	38,-	Drv
150		FDMT1#	O OD	External	38,-	Drv
151		FDSTEP#	O OD	External	38,-	Drv
152		RESERVE	---	---	---	---
153	SERIAL I/F	DARXD	I	50KPU	---	Input
154		COMBRI#	I	50KPU	---	Active/Input
155		COMBRXD	I	50KPD	---	Input
156		COMBTXD	O	---	8,-8	High-Z
157		COMBDCD#	I	50KPU	---	Input
158		COMARI#	I	50KPU	---	Active/Input

Pin	Group (EASI)	Signal name	Type	Termination	drive (mA) IOL,IOH	susp
159	SERIAL I/F	COMARXD	I	50KPD	---	Input
160		COMATXD	O	---	8,-8	High-Z
161		COMADCD#	I	50KPU	---	Input
162		IRTXD	O	---	24,-12	High-Z
163	PARALLEL I/F	LPTAFD#	IO OD	4.7KPU	12,-	Input/Drive
164		LPTERROR#	I	60KPU	---	Input
165		LPTBUSY	I	20KPU	---	Input
166		LPTSLCT	I	20KPD	---	Input
167		LPTINIT#	IO OD	4.7KPU	12,-	Input/Drive
168		LPTSLCTIN#	IO OD	4.7KPU	12,-	Input/Drive
169		LPTD4	IO	50KPD	8,-8	Input/Drive
170		LPTD6	IO	50KPD	8,-8	Input/Drive
171		LPTDIR	O	---	8,-8	Drive
172	IDE I/F	HD7	IO	50KPU	12,-12	Input
173		HDENH#	O	---	8,-8	Drv(1)
174		HDCS1#	O	---	12,-12	High-Z
175	POWER MANAGEMENT I/F	VBK	POWER	---	---	---
176		EXTSMI#	I	50KPU	---	Input
177	POWER Supply	GND	POWER	---	---	---
178		GND	POWER	---	---	---
179	POWER MANAGEMENT	RESERVE	---	---	---	---
180		SRBTN#	I	50KPU	---	Active
181	WATCHDOG I/F	WDTIM#	O	---	4,-4	Drive
182	ROM UPDATE I/F	PGM	---	---	---	---
183		RESERVE	---	---	---	---
184		RESERVE	---	---	---	---
185	ISA Bus	RESETDRV	O	---	12,-12	Drv(0)
186		IOCHCK#	I	4.7KPU	---	Input
187		IRQ9	I	50KPU	---	Input
188		DRQ2	IO	50KPD	12,-2	Input/Drive
189		WS0#	I	1KPU	---	Input
190		SMEMW#	O	---	12,-12	Drv(1)
191		SMEMR#	O	---	12,-12	Drv(1)
192		IOW#	IO	50KPU	12,-12	Drv(1)
193		IOR#	IO	50KPU	12,-12	Drv(1)
194		DACK3#	O	---	8,-8	Drv(1)
195		DRQ3	I	50KPD	---	Input
196		DACK1#	O	---	8,-8	Drv(1)
197		DRQ1	I	50KPD	---	Input
198		REF#	IO OD	1.2KPU	12,-	Input
199		SCLK	O	33ST	12,-12	Drv(0)

Pin	Group (EASI)	Signal name	Type	Termination	drive (mA) IOL,IOH	susp
200	POWER Supply	VCC3	POWER	---	---	---
201		VCC3	POWER	---	---	---
202		VCC5	POWER	---	---	---
203		VCC5	POWER	---	---	---
204	ISA Bus	IRQ7	IO	50KPU	8,-8	Input/Drive
205		IRQ6	IO	50KPU	12,-2	Input/Drive
206		IRQ5	IO	50KPU	8,-8	Input/Drive
207		IRQ4	IO	50KPU	8,-8	Input/Drive
208		IRQ3	IO	50KPU	8,-8	Input/Drive
209		DACK2#	O	---	8,-8	Drv(1)
210		TC	O	---	12,-12	Drv(0)
211		BALE	O	---	12,-12	Drv(0)
212		OSC	O	33ST	8,-8	Drv(0)
213		MEMCS16#	I	1KPU	---	Input
214		IOCS16#	I	1KPU	---	Input
215		IRQ10	IO	50KPU	8,-8	Input/Drive
216		IRQ11	IO	50KPU	8,-8	Input/Drive
217		IRQ12	O	50KPU	8,-8	Drive
218		IRQ15	I	50KPU	---	Input
219		IRQ14	I	50KPU	---	Input
220		DACK0#	O	---	8,-8	Drv(1)
221		DRQ0	I	50KPD	---	Input
222		DACK5#	O	---	8,-8	Drv(1)
223		DRQ5	I	50KPD	---	Input
224		DACK6#	O	---	8,-8	Drv(1)
225		DRQ6	I	50KPD	---	Input
226		DACK7#	O	---	8,-8	Drv(1)
227		DRQ7	I	50KPD	---	Input
228		MASTER#	I	1KPU	---	Input
229		SD12	IO	50KPU	12,-12	Input
230		SD13	IO	50KPU	12,-12	Input
231		SD14	IO	50KPU	12,-12	Input
232		SD15	IO	50KPU	12,-12	Input
233	POWER MANAGEMENT I/F	SMOUT2	O	---	8,-8	Drive
234		SMOUT0	O	---	8,-8	Drive
235	POWER Supply	GND	POWER	---	---	---
236		GND	POWER	---	---	---

10. AC CHARACTERISTICS (recommended and reference values)

ISA Bus Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
	SCLK Period for 16MHz	-	125	-	ns
	SCLK Period for 33MHz	-	120	-	ns

ISA Bus Timing

Symbol	Parameter	Min.	Max.	Unit	Note
t301	BALE Active Delay from SCLK	-	25	ns	Fig.9.1
t302	BALE Inactive Delay from SCLK		25	ns	Fig.9.1
t303	LA17-23, SA2-16 Valid Delay from SCLK	-	25	ns	Fig.9.1
t304	LA17-23, SA2-16 Invalid Delay from SCLK	0	-	ns	Fig.9.1
t305	SA0-1, SBHE# Valid Delay from SCLK	-	30	ns	Fig.9.1
t306	SA0-1, SBHE# Invalid Delay from SCLK	0	-	ns	Fig.9.1
t307	Command Active Delay from SCLK (8bit Memory Read/Write, I/O Read/Write Cycle, Halt Cycle)	-	25	ns	Fig.9.1
t308	Command Inactive Delay from SCLK	5	30	ns	Fig.9.1
t309	MEMCS16# Setup to SCLK	15	-	ns	Fig.9.1
t310	MEMCS16# Hold from SCLK	15	-	ns	Fig.9.1
t311	IOCHRDY Setup to SCLK	15	-	ns	Fig.9.1
t312	IOCHRDY Hold from SCLK	15	-	ns	Fig.9.1
t313	SD0-7,SD0-15 Setup to SCLK (Read Cycle)	15		ns	Fig.9.1
t314	SD0-7,SD0-15 Hold from SCLK (Read Cycle)	5		ns	Fig.9.1
t315	SD0-7 Valid Delay from SCLK (8bit Write Cycle)	-	65	ns	Fig.9.1
t316	SD0-7, SD0-15 Invalid Delay from SCLK (Write Cycle)	0	20	ns	Fig.9.1
t317	Command Active Delay from SCLK (16bit Memory Read/Write Cycle)	-	30	ns	Fig.9.7
t318	ZEROWS# Setup to SCLK	15	-	ns	Fig.9.7
t319	ZEROWS# Hold from SCLK	15	-	ns	Fig.9.7
t320	SD0-15 Valid Delay from SCLK (16bit Write Cycle)	-	65	ns	Fig.9.7
t321	IOCS16# Setup to SCLK	15	-	ns	Fig.9.10
t322	IOCS16# Hold from SCLK	15	-	ns	Fig.9.10
t323	Command Active Delay from SCLK (SMEMR#, SMEMW#)	-	45	ns	Fig.9.2
t324	Command Inactive Delay from SCLK (SMEMR#, SMEMW#)	5	50	ns	Fig.9.2
t35	DACKx# Active Delay from SCLK	-	75	ns	Fig. 9.12
t36	DACKx# Inactive Delay from SCLK	-	75	ns	Fig. 9.12
t37	SA0-7 Valid Delay from SCLK	-	50	ns	Fig. 9.12
t38	LA17-23 Valid Delay from DACKx#	-	30	ns	Fig. 9.12
t39	IOR#/IOW#/MEMW# Active from SCLK	-	70	ns	Fig. 9.12
t40	IOR# Active Delay from SCLK	-	45	ns	Fig. 9.12
t41	MEMR# Active Delay from SCLK	-	35	ns	Fig. 9.12
t43	IOCHRDY Setup to SCLK	20	-	ns	Fig. 9.12
t44	IOR# Inactive Delay from SCLK	-	60	ns	Fig. 9.12
t45	MEMR# Inactive Delay from SCLK	-	60	ns	Fig. 9.12
t46	IOW#/MEMW# Inactive Delay from SCLK	-	60	ns	Fig. 9.12
t48	DMA address invalid from SCLK	125	-	ns	Fig. 9.12
t49	IOR# Float Delay from SCLK	-	80	ns	Fig. 9.12
t50	MEMR# Float Delay from SCLK	-	80	ns	Fig. 9.12
t51	IOW#/MEMW# Float Delay from SCLK	-	80	ns	Fig. 9.12

Symbol	Parameter	Min.	Max.	Unit	Note
t_{67}	HDCS0#/HDCS1# Active Delay from Address	-	30	ns	Fig 10.13
t_{68}	HDENL#/HDENH# Output Active Delay IOR# Active	-	30	ns	Fig 10.13
t_{69}	HDENL#/HDENH# Output Inactive Delay IOR# Inactive		45	ns	Fig 10.13
t_{70}	SD7 Read Data Valid Delay from HD7	-	30	ns	Fig 10.13
t_{71}	Address Hold from Command Inactive	40	-	ns	Fig 10.13
t_{72}	SD7 Read Data Output Float from IOR# Inactive	-	45	ns	Fig 10.13
t_{73}	IOCS16# Setup to Command	10	-	ns	Fig 10.13
t_{74}	IOCS16# Hold from Command	10	-	ns	Fig 10.13
t_{75}	HD7 Write Data Valid from IOW# Active	-	50	ns	Fig 10.14
t_{76}	SD7 Write Data Hold from IOW# Inactive	30	-	ns	Fig 10.14
t_{77}	HD7 Write Data Float from IOW# Inactive	-	45	ns	Fig 10.14
t_{78}	HD7 Write Data Hold from IOW# Inactive	20	-	ns	Fig 10.14

Power Supply Sequence

Symbol	Parameter	Min.	Max.	Unit	Note
t_{11g}	$V_{CC}3$ = 3.0V Lag from $V_{CC}5$ = 4.5V	0	-	s	Fig 10.15
t_3	POWERGOOD Turn on Delay from 3.0V of $V_{CC}3$ and 4.5V of $V_{CC}5$ when both V_{CC}s are Ramping Up	50	-	ms	Fig 10.15
t_{3a}	POWERGOOD Turn on Delay from 4.75V of $V_{CC}5$ when $V_{CC}5$ are Ramping Up	0	-	ms	Fig 10.15
t_5	POWERGOOD Inactive Setup Time to 3.0V of $V_{CC}3$ and 4.5V of $V_{CC}5$ when Both V_{CC}s are Removed	0	-	s	Fig 10.15
t_9	RESETDRV Active Hold from POWERGOOD Active	3	-	ns	Fig 10.15

Note: It is mandatory that $V_{CC}5$ $V_{CC}3$. The card can be destroyed if this requirement is not satisfied.

Grayscale Single STN 8-bit LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt_1	FPVTIM setup to FPHTIM falling edge	HDP+HDNP-10	-	Ts	Fig. 10.16
Pt_2	FPVTIM hold from FPHTIM falling edge	6	-	Ts	Fig. 10.16
Pt_3	FPHTIM period	-	HDP+HNDP	Ts	Fig. 10.16
Pt_4	FPHTIM pulse width	(LP_SEL+1)	-	Ts	Fig. 10.16
Pt_5	FPAC delay from FPHTIM falling edge	0	-	Ts	Fig. 10.16
Pt_6	FPDOTCLK falling edge to FPHTIM rising edge	(HNDP-10)	-	Ts	Fig. 10.16
Pt_7	FPDOTCLK falling edge to FPHTIM falling edge	(HNDP-7+LP_SEL)	-	Ts	Fig. 10.16
Pt_8	FPHTIM falling edge to FPDOTCLK falling edge	(15-LP_SEL)	-	Ts	Fig. 10.16
Pt_9	FPDOTCLK period	8	-	Ts	Fig. 10.16
Pt_{10}	FPDOTCLK pulse width low	4	-	Ts	Fig. 10.16
Pt_{11}	FPDOTCLK pulse width high	4		Ts	Fig. 10.16
Pt_{12}	LD[7:0] setup to FPDOTCLK falling edge	4		Ts	Fig. 10.16
Pt_{13}	LD[7:0] hold to FPDOTCLK falling edge	4		Ts	Fig. 10.16
Pt_{14}	FPHTIM falling edge to FPDOTCLK rising edge	(11-LP_SEL)	-	Ts	Fig. 10.16

note: Ts = pixel clock period = 35ns typical
HDP = horizontal display period in units of Ts = 640 typical
HNDP = horizontal non-display period in units of Ts = 112 typical
LP_SEL = 7 typical
Refer to the BIOS Reference Manual and SPC8110 Manual for details.

Grayscale Dual STN 8-bit LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt1	FPVTIM setup to FPHTIM falling edge	HDP+HDNP-10	-	Ts	Fig. 10.17
Pt2	FPVTIM hold from FPHTIM falling edge	6	-	Ts	Fig. 10.17
Pt3	FPHTIM period	-	HDP+HNDP	Ts	Fig. 10.17
Pt4	FPHTIM pulse width	(LP_SEL+1)	-	Ts	Fig. 10.17
Pt5	FPAC delay from FPHTIM falling edge	0	-	Ts	Fig. 10.17
Pt6	FPDOTCLK falling edge to FPHTIM rising edge	(HNDP-10)	-	Ts	Fig. 10.17
Pt7	FPDOTCLK falling edge to FPHTIM falling edge	(HNDP-9+LP_SEL)	-	Ts	Fig. 10.17
Pt8	FPHTIM falling edge to FPDOTCLK falling edge	(13-LP_SEL)	-	Ts	Fig. 10.17
Pt9	FPDOTCLK period	4	-	Ts	Fig. 10.17
Pt10	FPDOTCLK pulse width low	2	-	Ts	Fig. 10.17
Pt11	FPDOTCLK pulse width high	2		Ts	Fig. 10.17
Pt12	LD[7:0] setup to FPDOTCLK falling edge	2		Ts	Fig. 10.17
Pt13	LD[7:0] hold to FPDOTCLK falling edge	2		Ts	Fig. 10.17
Pt14	FPHTIM falling edge to FPDOTCLK rising edge	(11-LP_SEL)	-	Ts	Fig. 10.17

note: Ts = pixel clock period = 52ns typical
HDP = horizontal display period in units of Ts = 640 typical
HNDP = horizontal non-display period in units of Ts = 112 typical
LP_SEL = 7 typical
Refer to the BIOS Reference Manual and SPC8110 Manual for details.

Color Dual STN 16-bit LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt1	FPVTIM setup to FPHTIM falling edge	HDP+HDNP-10	-	Ts	Fig. 10.18
Pt2	FPVTIM hold from FPHTIM falling edge	6	-	Ts	Fig. 10.18
Pt3	FPHTIM period	-	HDP+HNDP	Ts	Fig. 10.18
Pt4	FPHTIM pulse width	(LP_SEL+1)	-	Ts	Fig. 10.18
Pt5	FPAC delay from FPHTIM falling edge	0	-	Ts	Fig. 10.18
Pt6	FPDOTCLK falling edge to FPHTIM rising edge	(HNDP-9)	-	Ts	Fig. 10.18
Pt7	FPDOTCLK falling edge to FPHTIM falling edge	(HNDP-8+LP_SEL)	-	Ts	Fig. 10.18
Pt8	FPHTIM falling edge to FPDOTCLK falling edge	(12-LP_SEL)	-	Ts	Fig. 10.18
Pt9	FPDOTCLK period	2	-	Ts	Fig. 10.18
Pt10	FPDOTCLK pulse width low	1	-	Ts	Fig. 10.18
Pt11	FPDOTCLK pulse width high	1		Ts	Fig. 10.18
Pt12	LD[15:0] setup to FPDOTCLK falling edge	1		Ts	Fig. 10.18
Pt13	LD[15:0] hold to FPDOTCLK falling edge	1		Ts	Fig. 10.18
Pt14	FPHTIM falling edge to FPDOTCLK rising edge	(11-LP_SEL)	-	Ts	Fig. 10.18

note: Ts = pixel clock period = 52ns typical
HDP = horizontal display period in units of Ts = 640 typical
HNDP = horizontal non-display period in units of Ts = 112 typical
LP_SEL = 7 typical
Refer to the BIOS Reference Manual and SPC8110 Manual for details.

Color TFT LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt1	FPDOTCLK period	1	-	Ts	Fig. 10.19
Pt2	FPDOTCLK pulse width high	0.5	-	Ts	Fig. 10.19
Pt3	FPDOTCLK pulse width low	0.5	-	Ts	Fig. 10.19
Pt4	DATA setup to FPDOTCLK falling edge	0.5	-	Ts	Fig. 10.19
Pt5	DATA hold from FPDOTCLK falling edge	0.5	-	Ts	Fig. 10.19
Pt6	FPHTIM cycle time	-	805	Ts	Fig. 10.19
Pt7	FPHTIM pulse width low	-	96	Ts	Fig. 10.19
Pt8	FPVTIM cycle time	-	525	lines	Fig. 10.19
Pt9	FPVTIM pulse width low	-	2	lines	Fig. 10.19
Pt10	horizontal display period	-	640	Ts	Fig. 10.19
Pt11	FPHTIM setup to FPDOTCLK falling edge	0.5	-	Ts	Fig. 10.19
Pt12	FPVTIM falling edge to FPHTIM falling edge phase difference	1	-	Ts	Fig. 10.19
Pt13	FPBLANK# to FPDOTCLK falling edge setup time	0.5	-	Ts	Fig. 10.19
Pt14	FPBLANK# width	-	640	Ts	Fig. 10.19
Pt15	FPHTIM sampled low (by FPDOTCLK) to FPBLANK# rising edge	-	144	Ts	Fig. 10.19
Pt16	FPBLANK# falling edge to FPHTIM falling edge	-	16	Ts	Fig. 10.19
Pt17	FPBLANK# hold from FPDOTCLK falling edge	0.5	-	Ts	Fig. 10.19

note: Ts = pixel clock period = 52ns typical
Refer to the BIOS Reference Manual and SPC8110 Manual for details.

Timing Chart

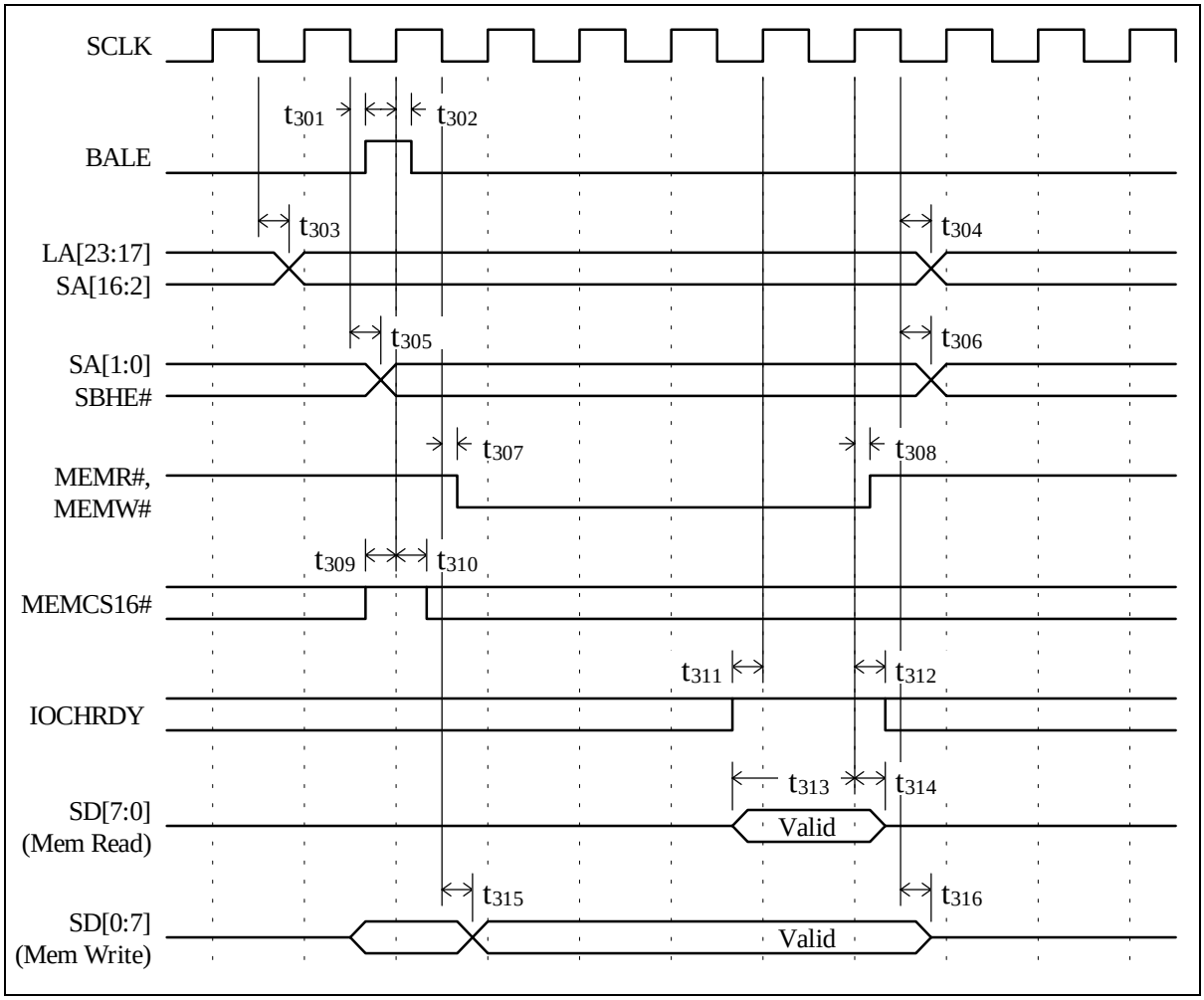


Figure 10.1 ISA Bus 8-Bit Memory Read/Write Standard ISA Bus Cycle (6 SCLKs)

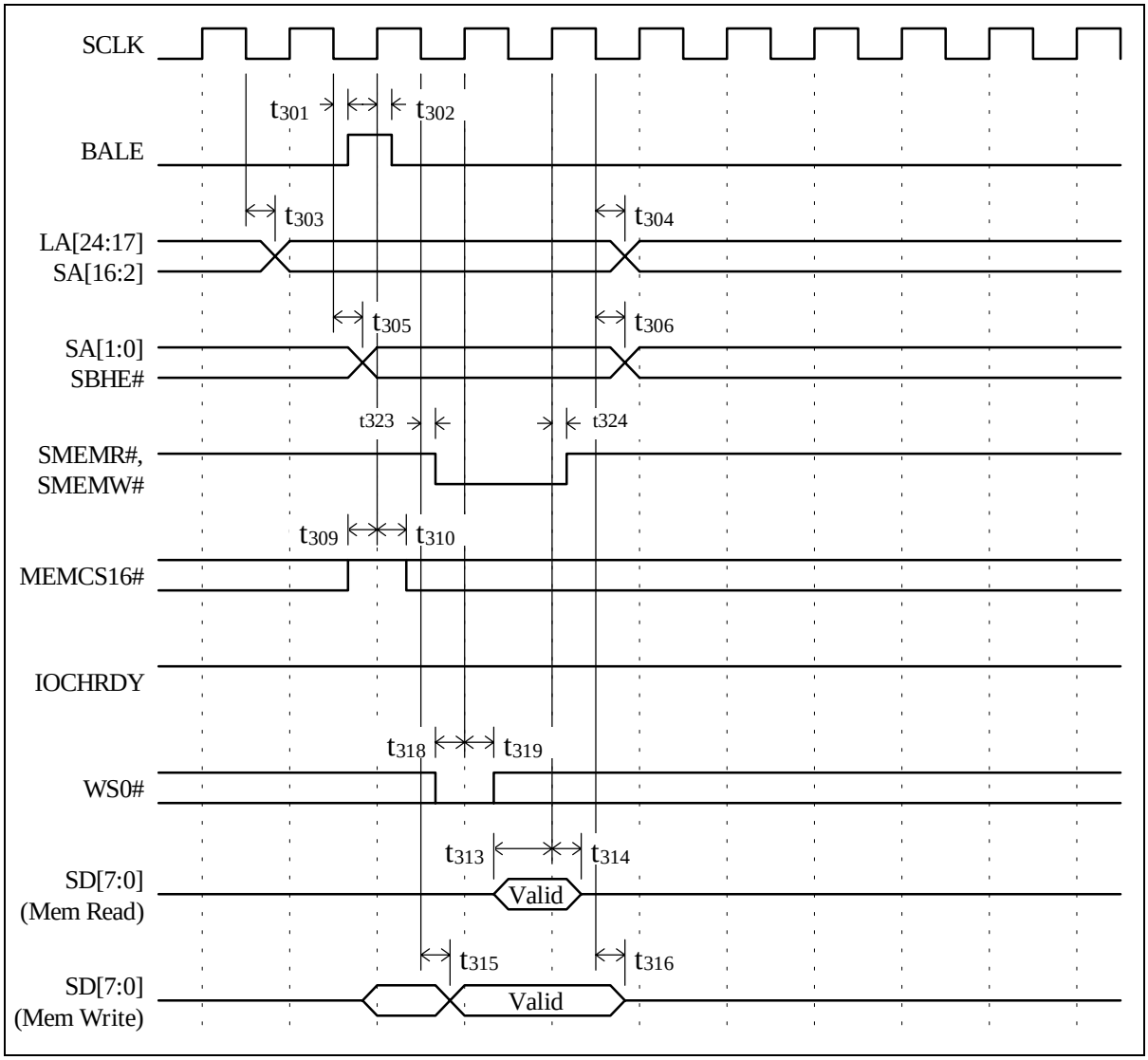


Figure 10.2 ISA Bus 8-Bit Memory Read/Write with ZEROWS# Asserted (3 SCLKs)

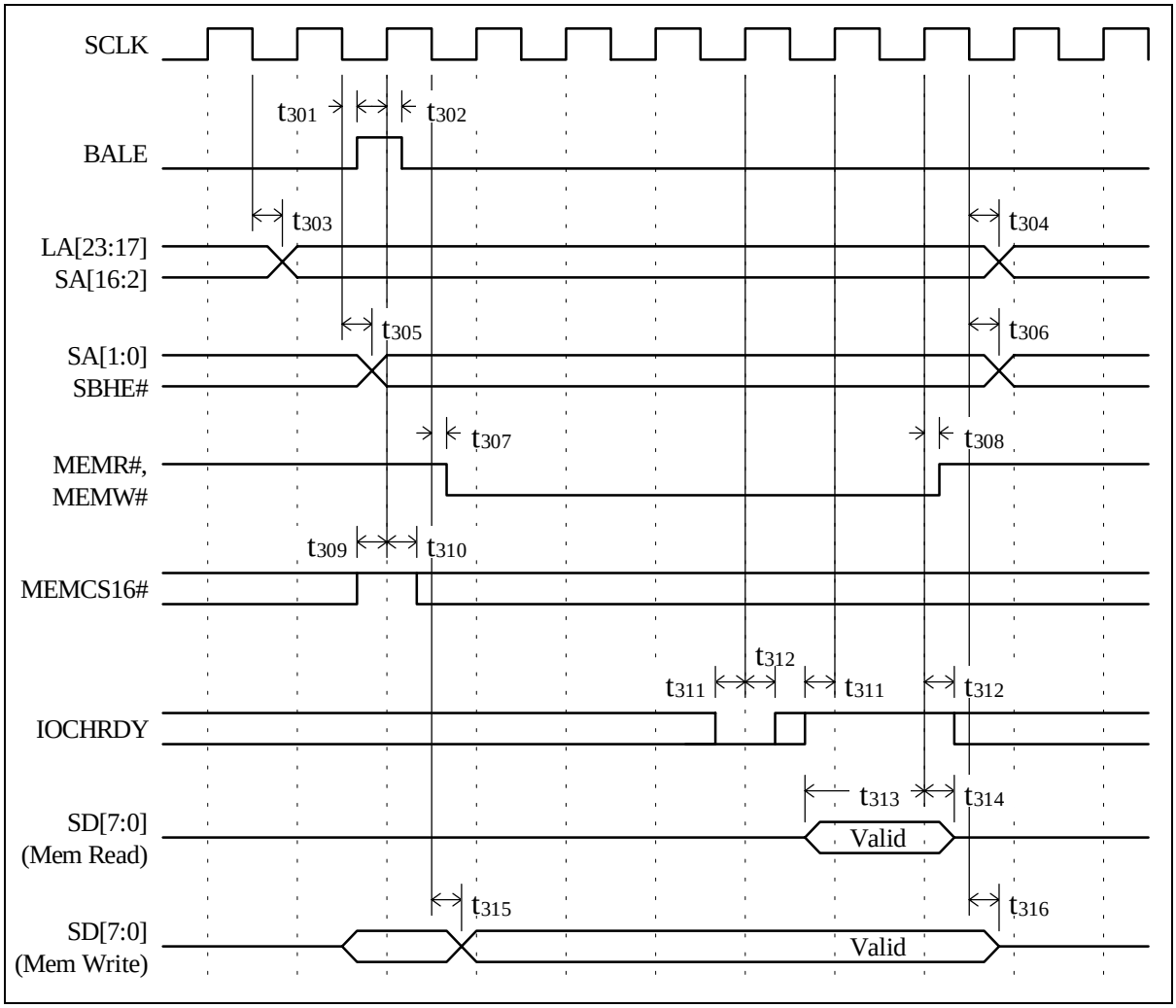


Figure 10.3 ISA Bus 8-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait State)

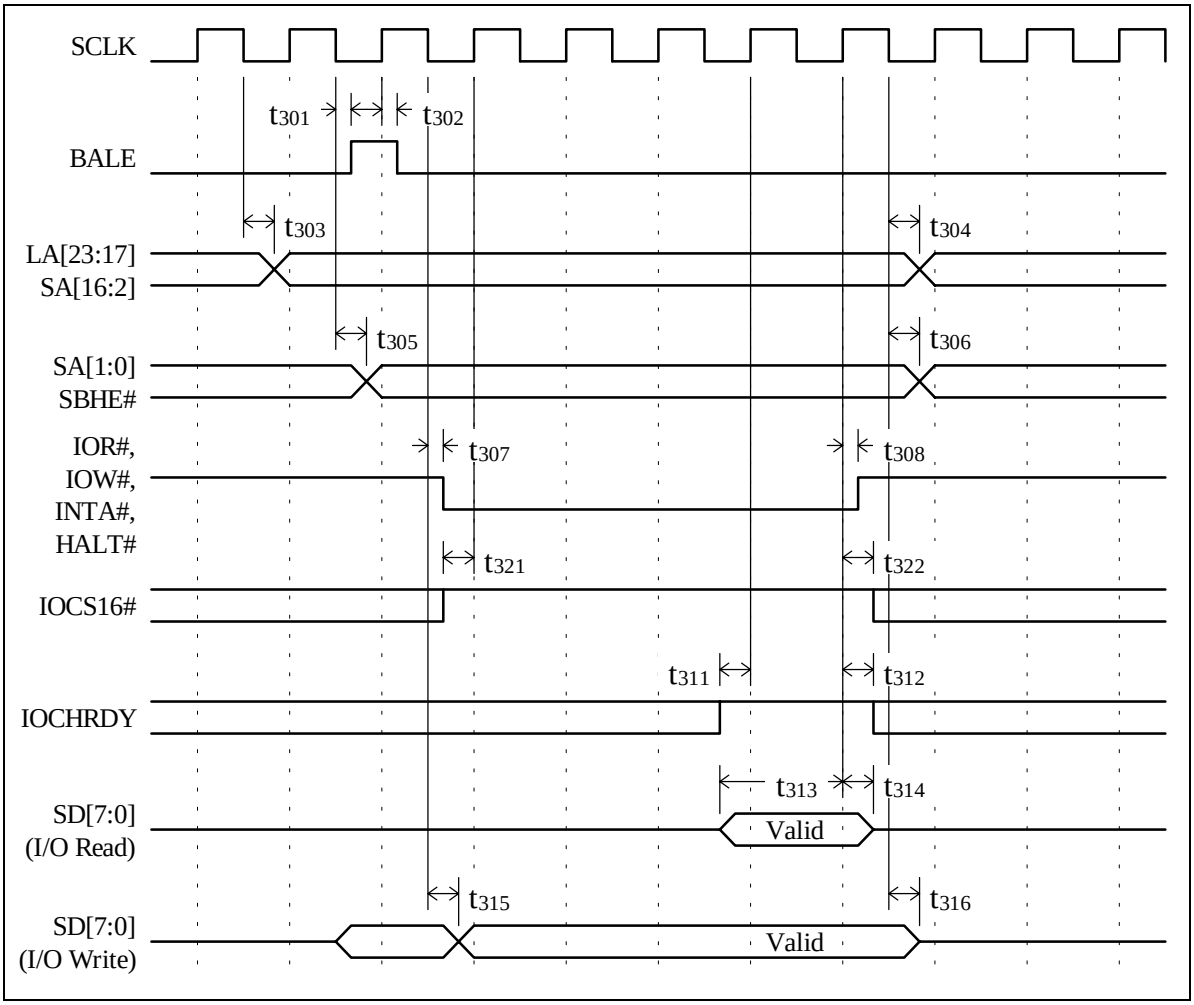


Figure10.4 ISA Bus 8-Bit I/O Read/Write Standard ISA Bus Cycle (6 SCLKs)

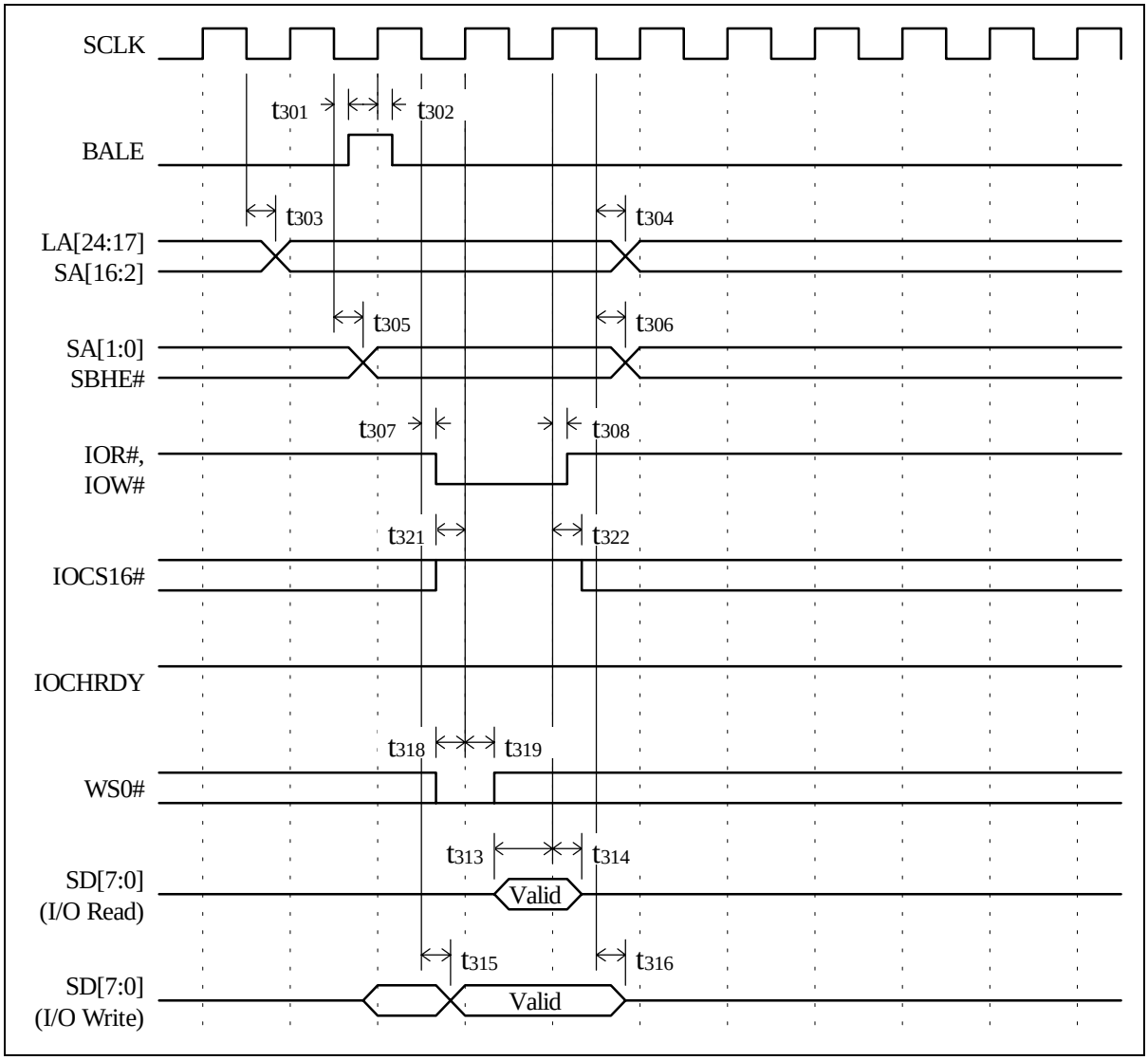


Figure 10.5 ISA Bus 8-Bit I/O Read/Write with ZEROWS# Asserted (3 SCLKs)

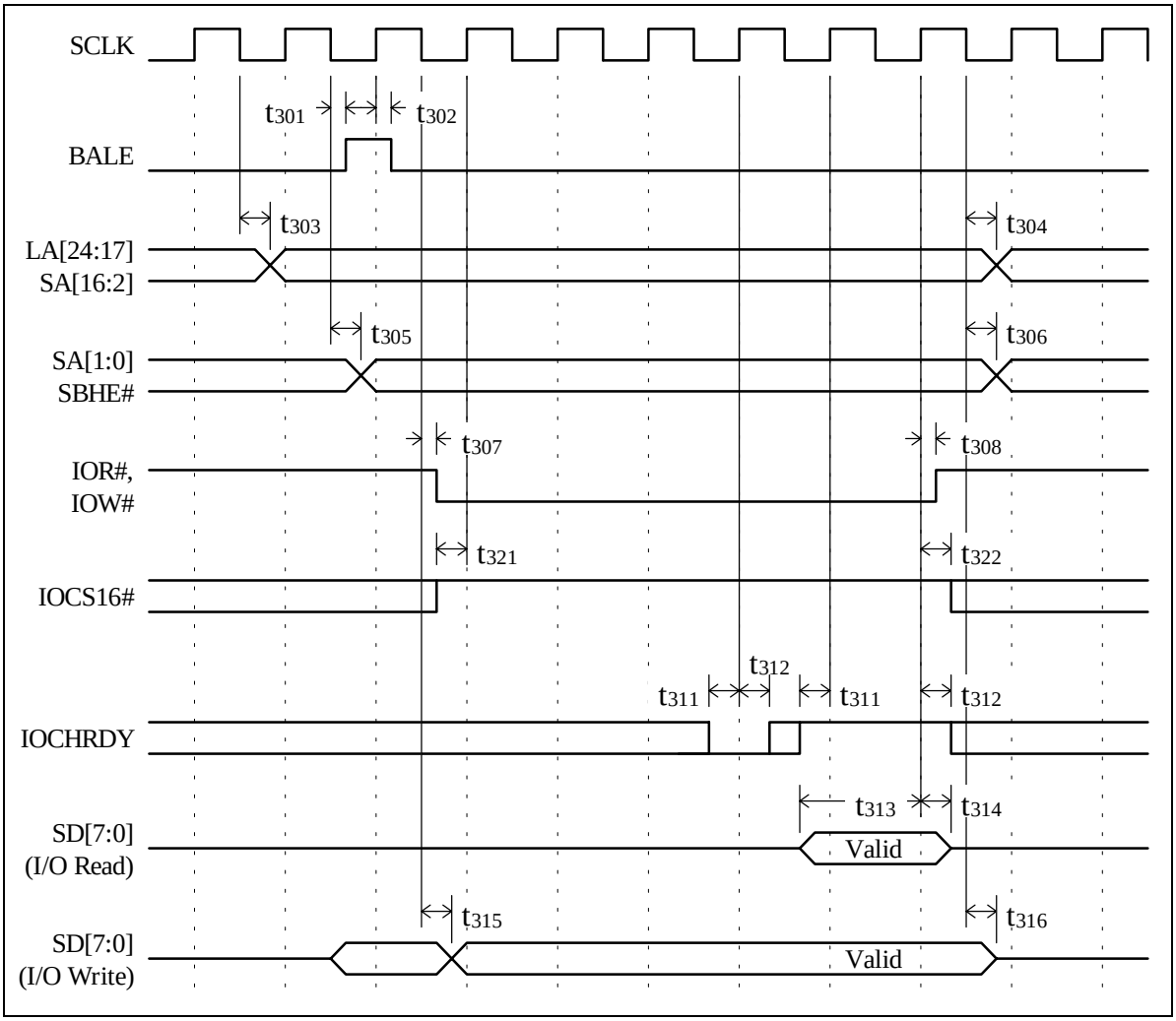


Figure 10.6 ISA Bus 8-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

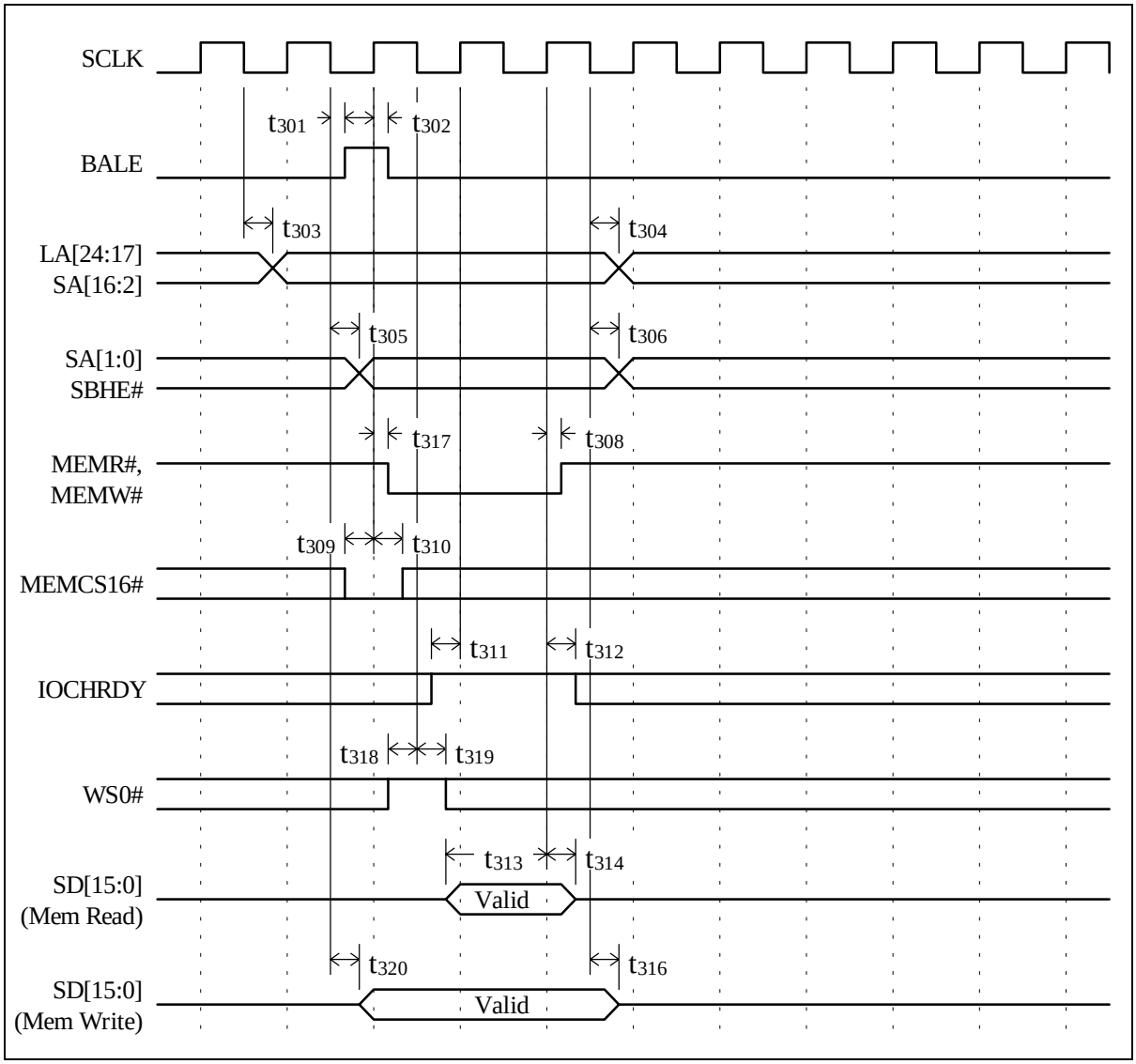


Figure 10.7 ISA Bus 16-Bit Memory Read/Write Standard Bus Cycles (3 SCLKs)

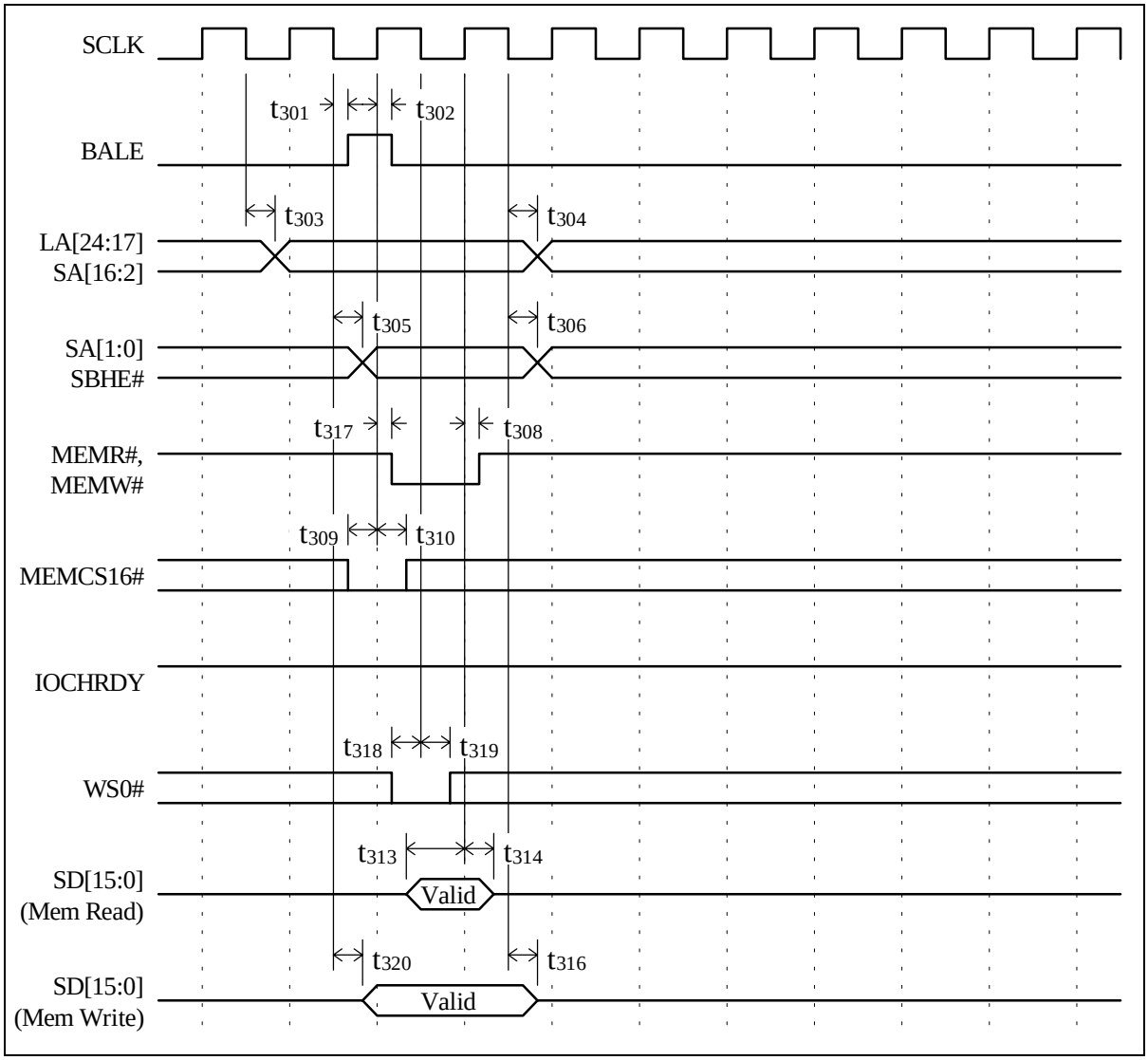


Figure 10.8 ISA Bus 16-Bit Memory Read/Write with ZEROWS# Asserted

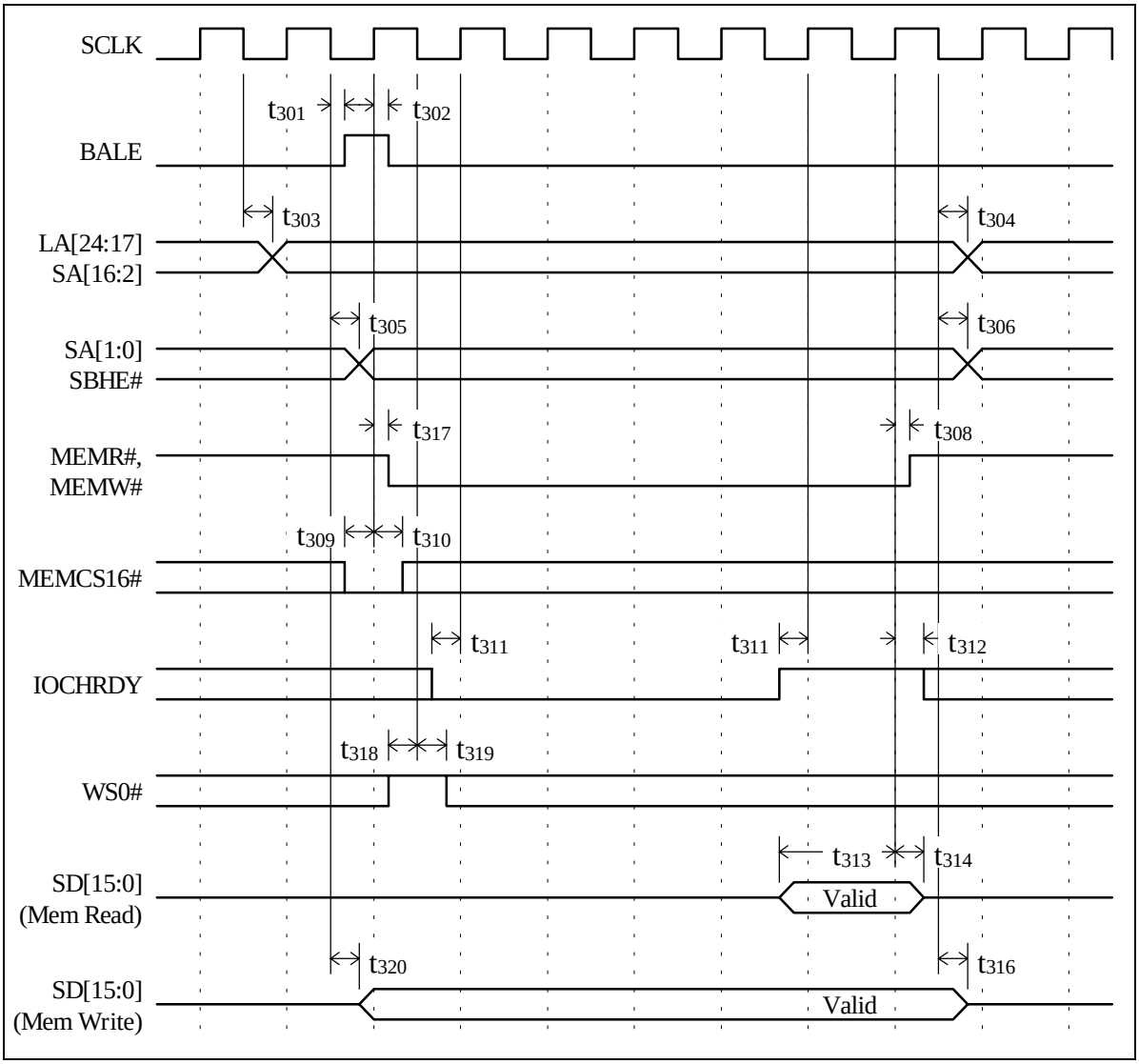


Figure 10.9 ISA Bus 16-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

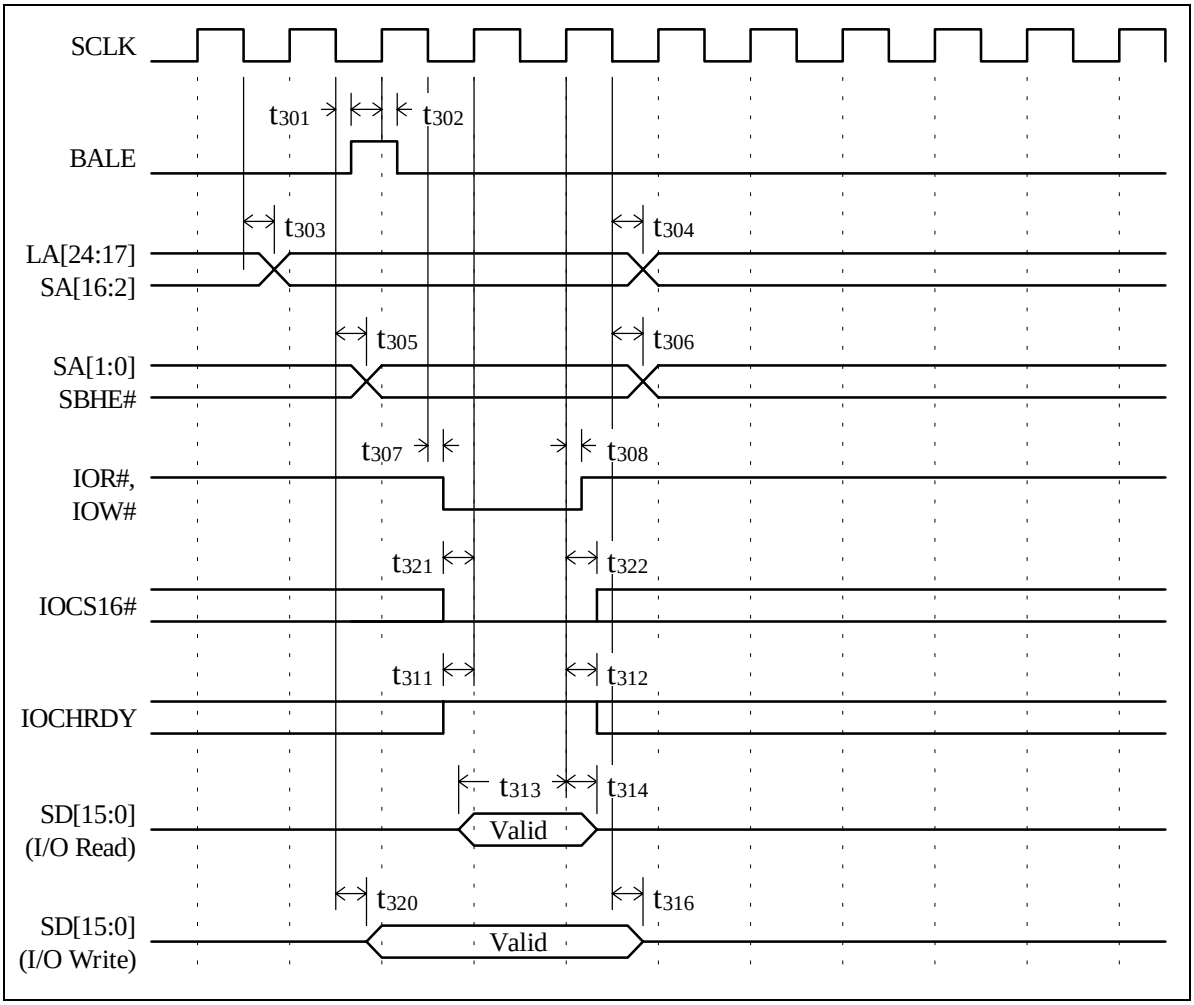


Figure 10.10 ISA Bus 16-Bit I/O Read/Write Standard ISA Bus Cycle (3 SCLKs)

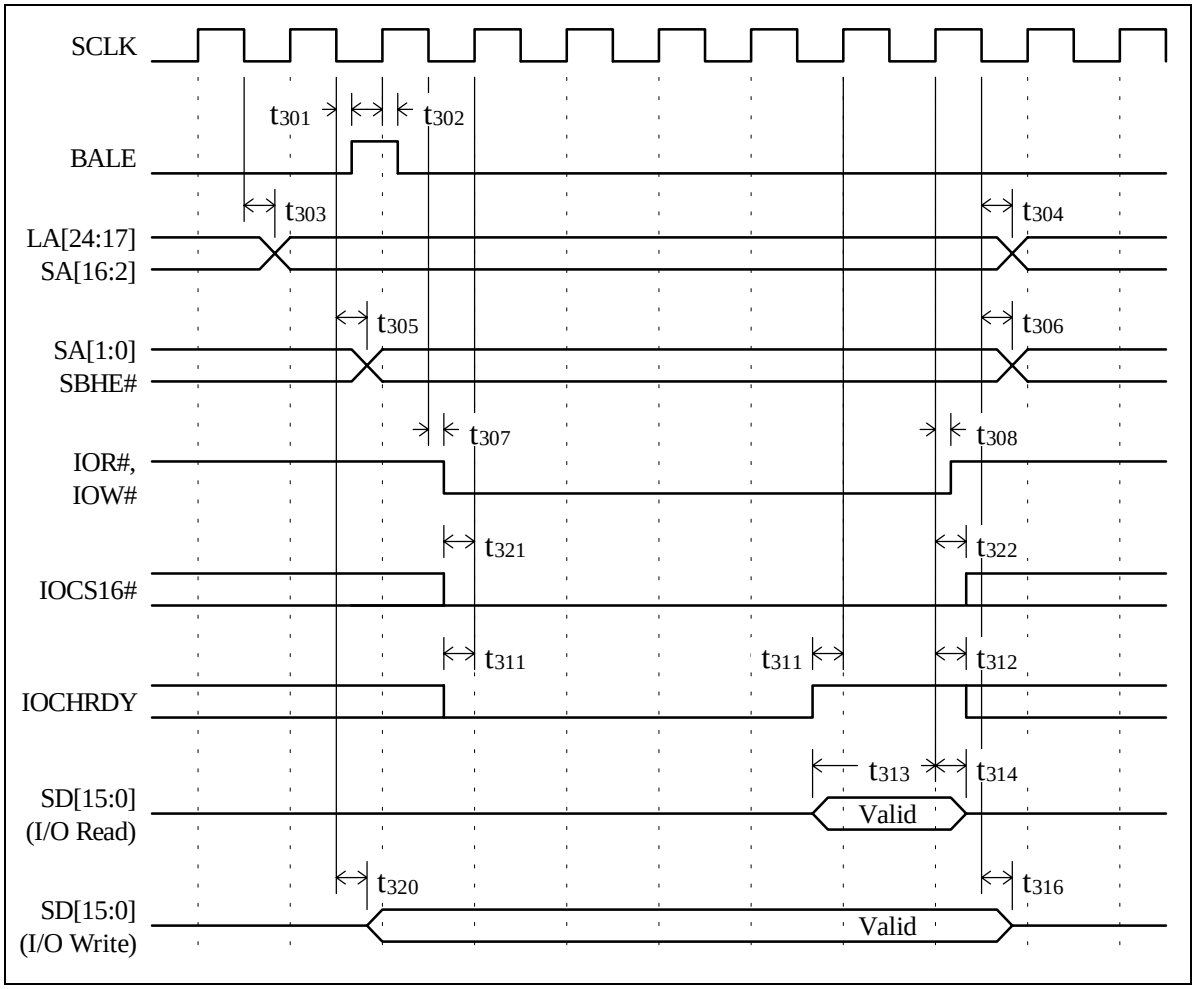


Figure 10.11 ISA Bus 16-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

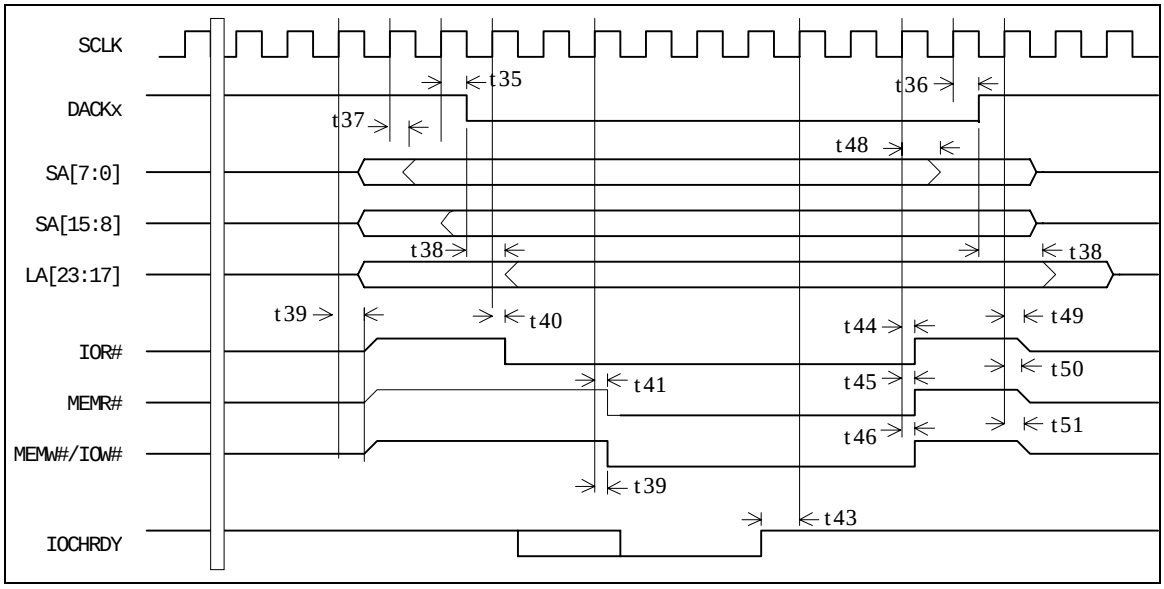


Figure 10.12 DMA Memory Read Timings (4 MHz)

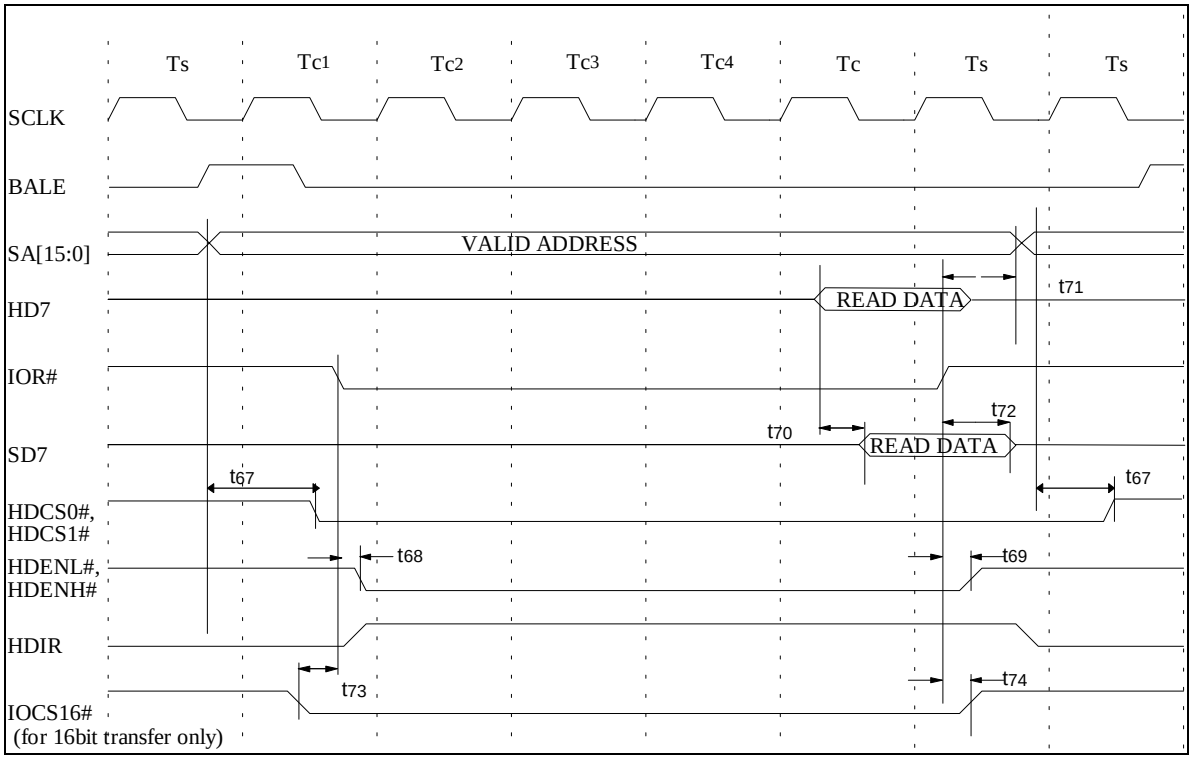


Figure 10.13 Bus Master Refresh Cycle Timings

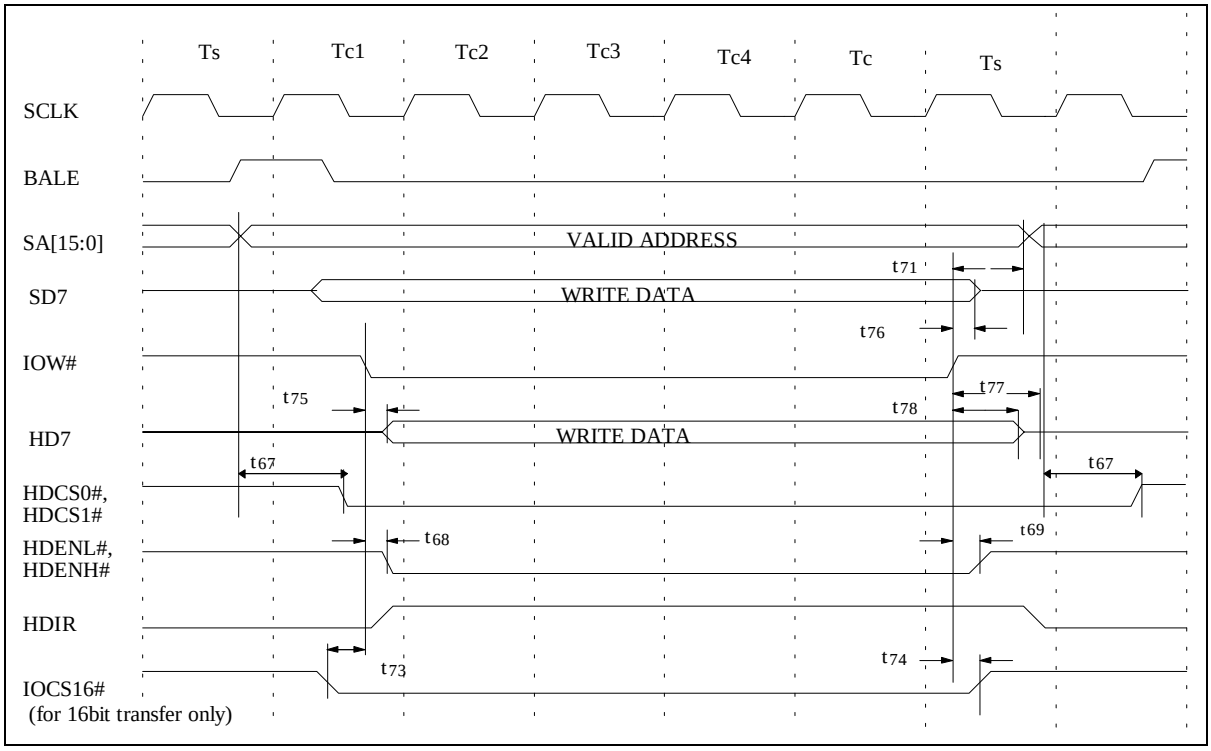


Figure 10.14 I.D.E Hard Disk Control Signals (I/O Write Timings)

Power-Up Sequence

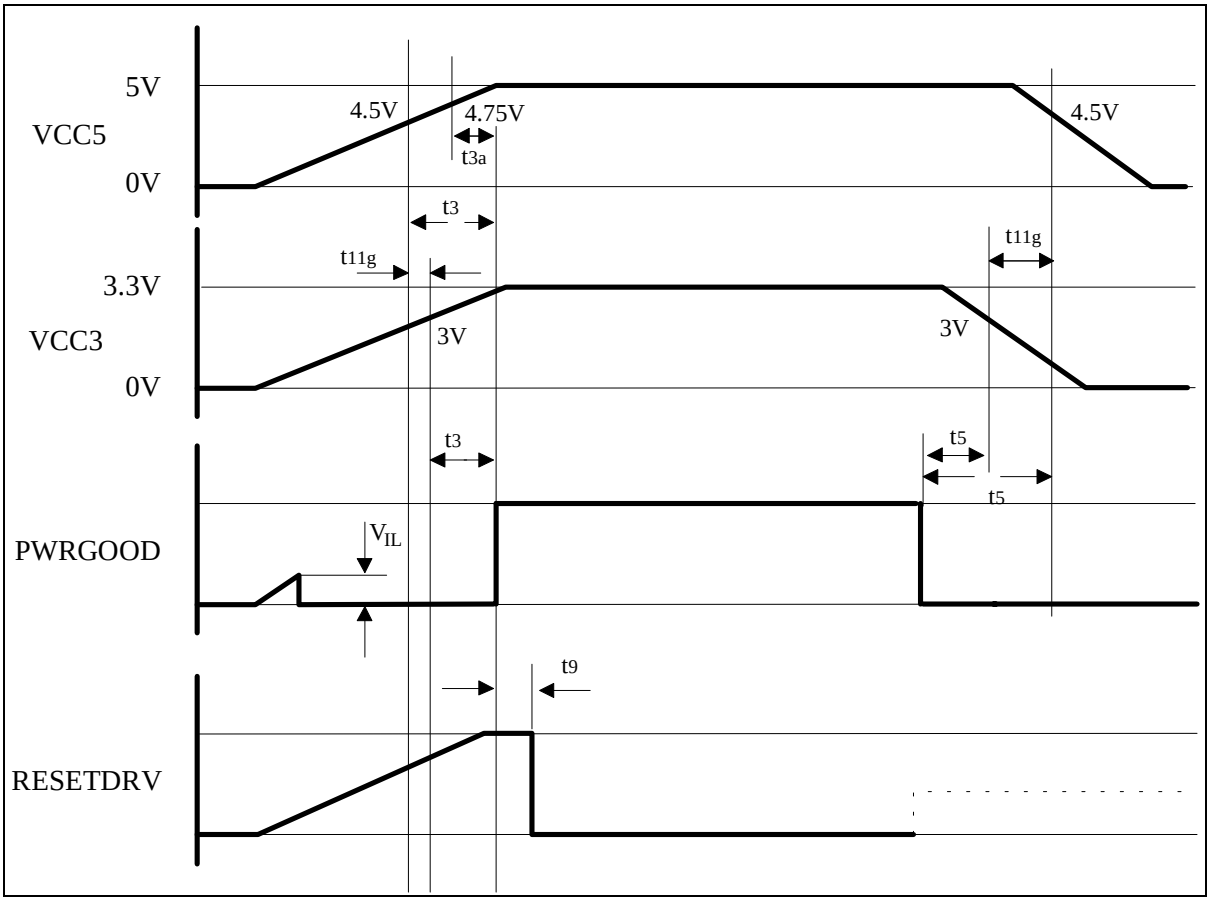


Figure 10.15. Power-Up Sequence

LCD Interface

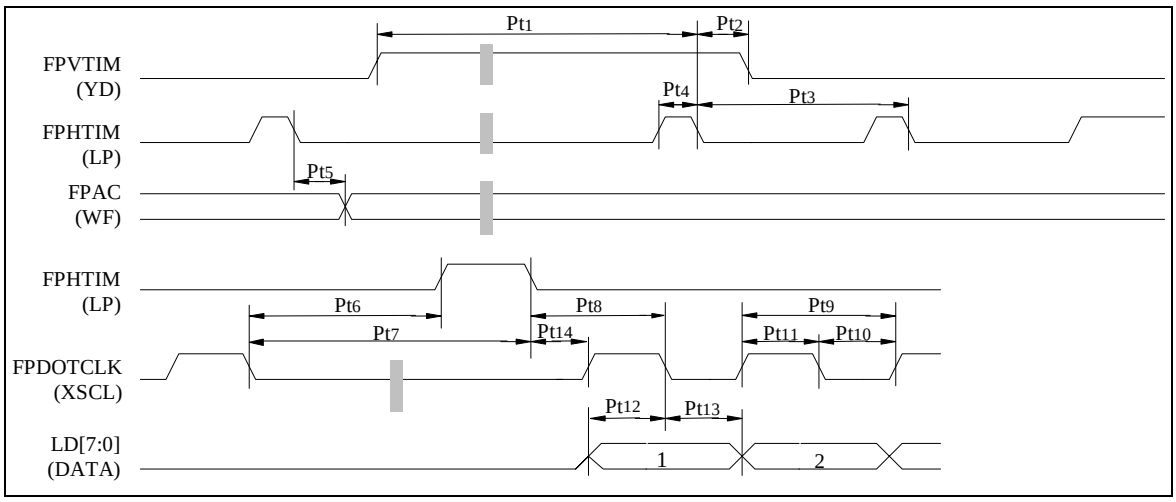


Figure 10.16. Grayscale Single STN 8-bit LCD Interface

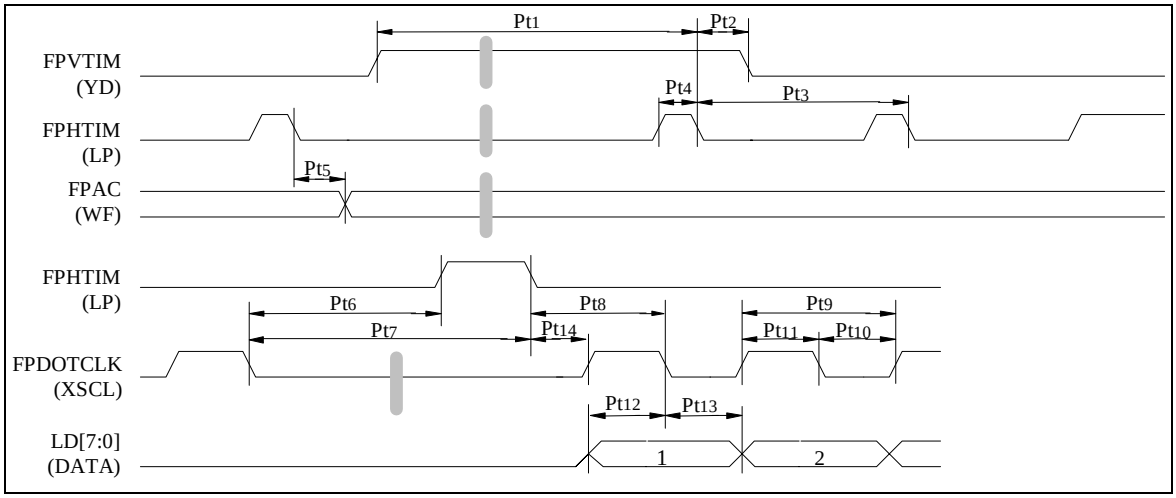


Figure 10.17. Grayscale Dual STN 8-bit LCD Interface

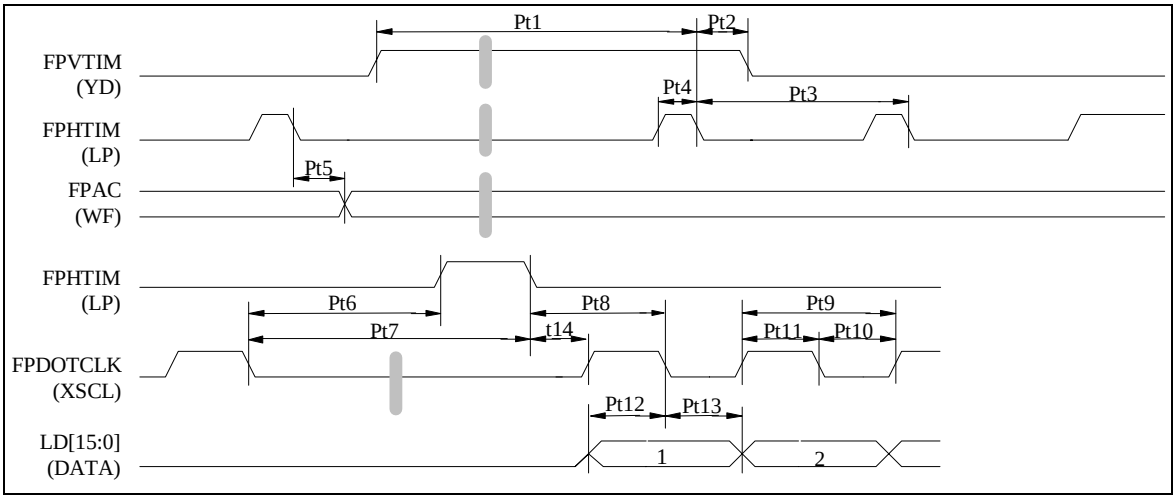


Figure 10.18. Color Dual STN 16-bit LCD Interface

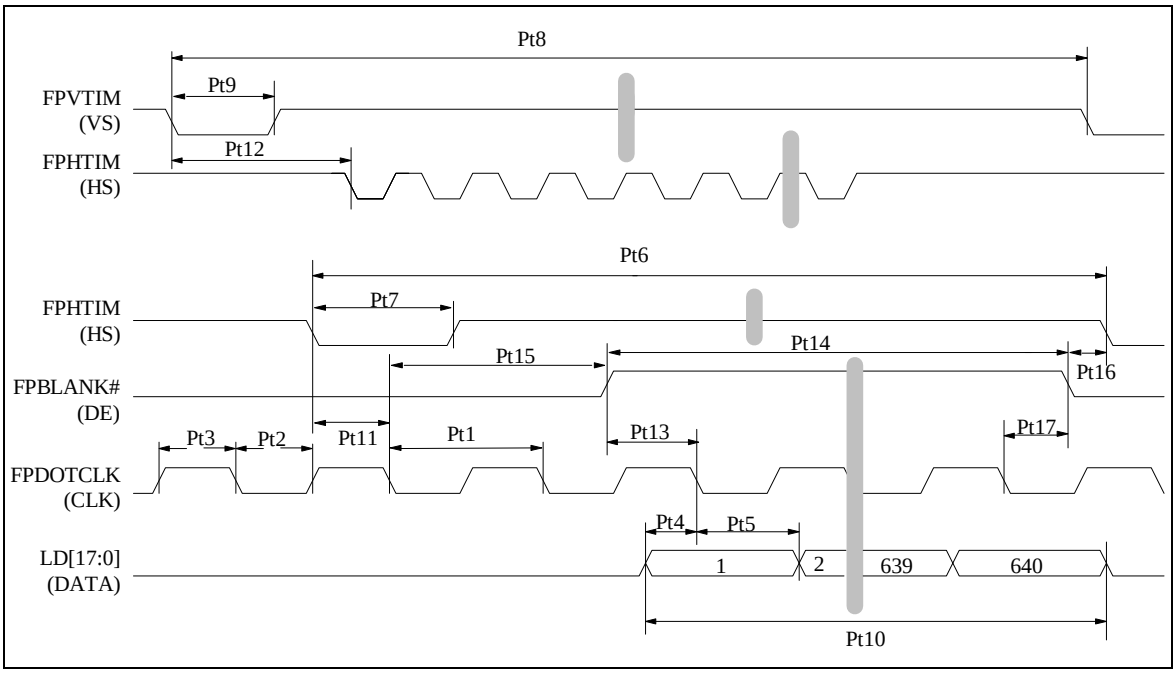


Figure 10.19. Color TFT LCD Interface

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CARD-486HB/HBL
Hardware Manual

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