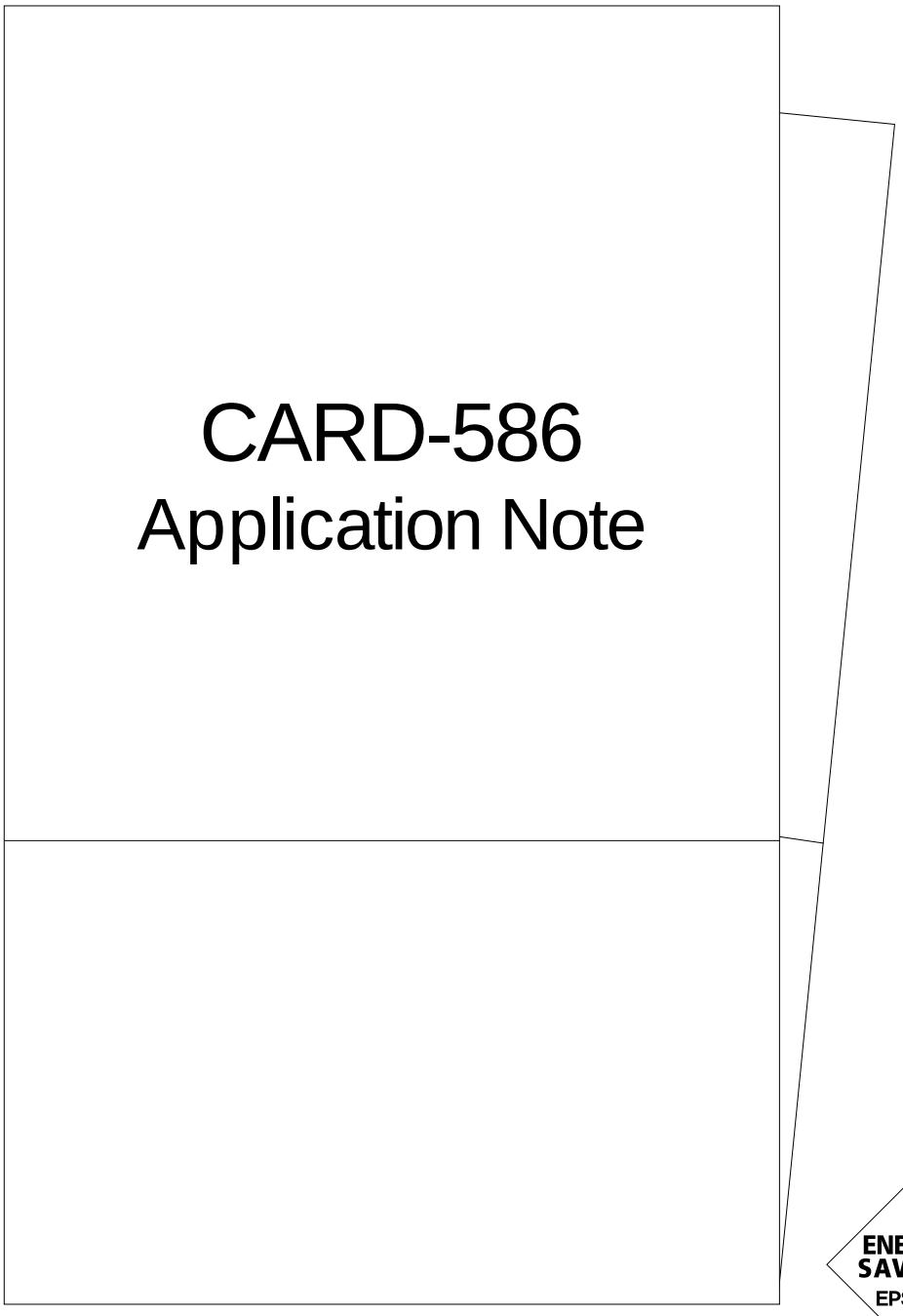
MF1123-02

EPSON

CARD-586
Application Note



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Contents

1. EASI Specifications

Credit card-sized PC boards employing 236-pin interface connectors are all referred to here as card-sized PC. The EASI (Embedded All-In-One System Interface) specifications aim to standardize, among sponsors in the EASI Group, location and naming of the 236-pin connector on card-sized PCs. The SCE86437 series (referred to as CARD-586 hereafter) is a product which conforms to the EASI specifications.

With the EASI specifications, pins are grouped in blocks according to their functions. This leads to easy design work even if the customer exchanges and uses different card-sized PCs. Also, use of chipset in card-sized PCs enables incompatibility among card-sized PCs to limit to blocks only. For this reason, be sure to check the specifications of each card-sized PC when they will be used together with CARD-586. In addition, be sure to design the block section so that cabling between the connector pin and device can be changed freely.

Table 1-1 summarizes the EASI pin block types and pin numbers.

Table 1-1 EASI Pin Block

Pin Block	Number of Pins	Pin No.	
Power	28	#1, #2, #2730 #59, #60, #8285 #117, #118	#119, #120, #145148 #177, #178, #200203 #235, #236
LCD interface	28	#314, #19, #20	#121132, #137, #138
CRT interface	8	#1518	#133136
Mouse interface	2	#21	#139
Keyboard interface	2	#22	#140
FDD interface	18	#2326, #3135	#141144, #149153
Serial interface	18	#3644	#154162
Parallel interface	18	#4553	#163171
IDE interface	6	#5456	#172174
Power management	12	#57, #58, #61, #62, #115, #116	#175, #176, #179, #180 #233, #234
Speaker interface	2	#63	#181
ROM update interface	6	#6466	#182184
ISA bus	88	#6781, #86114	#185199, #204232

*1 : Depending on the combination of the LCD panel and card-sized PC, the handling of synchronous signal and data signal may be different.
*2 : #152 (FDMSEL) is not supported.
*3 : Handling of #153 (DARX), #44 (IRRX), and #162 (IRTX) may be different.
*4 : Handling of #171 (LPTDIR) may be different.
*5 : Handling of pins other than #57 (SUSSTAT#), #58 (BATLOW#), #62 (POWERGOOD), #175 (V_{BK}) and #176 (EXTSMI#) may be different.
*6 : Handling of #181 (WDTIM#) may be different.
*7 : Handling may be different depending on the card-sized PC. Card-sized PCs manufactured by Seiko Epson (referred to as CARD-PC in this manual) are compatible with each other.

2. Video Interface

CARD-586 has a built-in video controller (SPC8100, manufactured by Seiko Epson) which is compatible with IBM PC/AT. In terms of display device, it can drive a CRT, a LCD, or both at the same time. These display methods are referred to as CRT display, LCD display, and simultaneous display. CARD-586's BIOS controls switching of video signal output. The main difference between the CRT interface and the LCD interface is that the former is an analog output whereas the latter is a digital (TTL) output.

2.1 CRT Interface

As shown below, CARD-586 and the CRT connectors are only connected by the 8 signals.

Figure 2-1 CRT Interface

2.2 LCD Interface

The LCD interface of CARD-586 can be connected to the following liquid display panels:

- QVGA compliant (320×240) single panel STN monochrome liquid display panel. Bus configuration is 4×1.
- VGA compliant (640×480) single panel STN monochrome liquid display panel. Bus configuration is 8×1.
- VGA compliant (640×480) dual panel STN monochrome liquid display panel. Bus configuration is 4×2.
- VGA compliant (640×480) dual panel STN color liquid display panel. Bus configuration is 8×2.
- SVGA compliant (800×600) single panel STN monochrome liquid display panel. Bus configuration is 4×1.
- SVGA compliant (800×600) dual panel STN monochrome liquid display panel. Bus configuration is 4×2.
- SVGA compliant (800×600) dual panel STN color liquid display panel. Bus configuration is 8×2.
- VGA compliant (640×480) TFT color liquid display panel. Color configuration is 3×3, 4×3, 6×3 bits.
- SVGA compliant (800×600) TFT color liquid display panel. Color configuration is 6×3 bits.

Also, CARD-586 can control power to the LCD while operating. By having the power ON/OFF circuitry installed outside, CARD-586 can make use of its signal to supply or disconnect power to the LCD in a simple way. The sequence is shown in figure 2-2. A connection example is shown in figure 2-3.

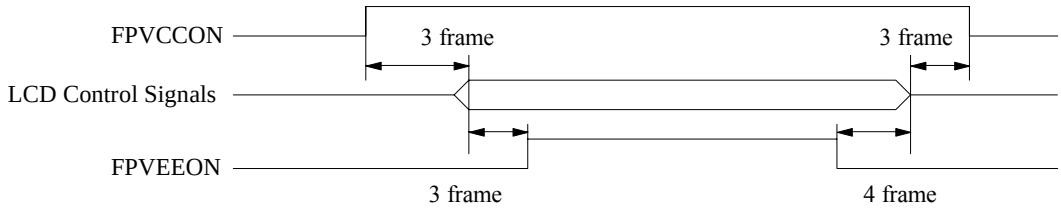


Figure 2-2 Panel Power Supply Sequence

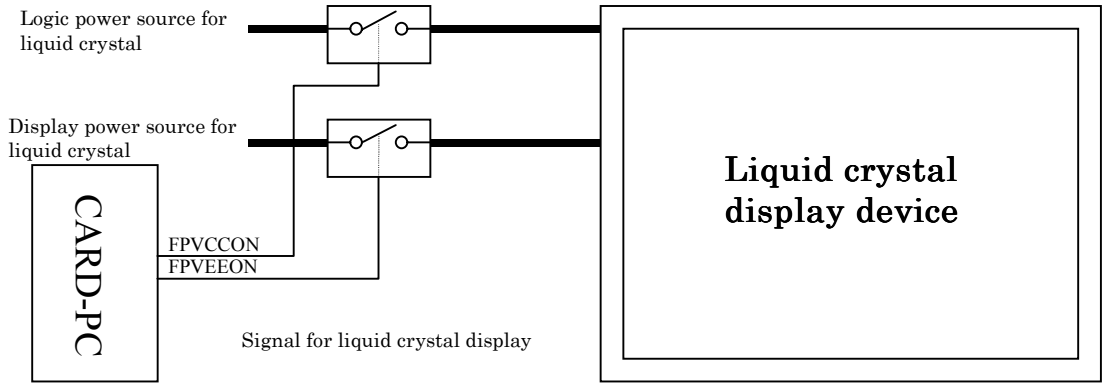


Figure 2-3 Connection Example

The following is an overview of LCD panels supported by the controller built into CARD-586. However, color STN single scan LCD is not supported.

- Monochrome STN single scan LCD

Resolution can be 320×240 dots or 640×480 dots. Supported data transmission are 4 bits and 8 bits. For LCD data signals, LC0 to LD7 are used. A maximum of 64-greyscale display is possible.

- Monochrome STN dual scan LCD

Resolution can be 640×480 dots and 800×600 dots. Supported data transmission is 4 bits. For LCD data signals, LC0 to LD7 are used. A maximum of 64-greyscale display is possible.

- Color STN dual scan LCD

Resolution can be 640×480 dots and 800×600 dots. Supported data transmission is 8 bits. For LCD data signals, LC0 to LD15 are used. Display of 256 colors is possible.

- Color (3×3, 4×3, 6×3 bits) TFT LCD

Resolution can be 640×480 dots and 800×600 dots. Supported display color are 3×3 bits (512 colors), 4×3 bits (4096 colors) and 6×3 bits (262144 colors). For LCD data signals, LC0 to LD17 are used. Also, TFT panel using DE signal for horizontal synchronization is supported. As horizontal synchronization signal, FPHTIM is connected to the Hsync pin, and FPBLANK is connected to the DE pin. However, TFT basing start time on horizontal synchronization signal and special FPDOTCLK number is not supported.

Because the video interface setting is performed at the BIOS, RAK must be used to change the BIOS according to the panel for use. For connection information on typical LCDs, please refer to the separate "CARD-PC Technical Information." However, because this information is constantly updated, please see our home page or contact our sales personnel for the latest information. Also, see the "Appendix 2. Control Methods for Different LCDs" for explanation on control methods of different LCDs.

When shipped, CARD-586 is set to have value for the Seiko Epson EG9013 is used as the default for the 640×480 dot monochrome STN single scan LCD setting.

2.3 Simultaneous CRT and LCD Display

The following LCD specification is required to enable simultaneous display on both LCD and CRT. If this specification is not met, then the simultaneous display on CRT cannot be done.

Table 2-1 Display Frequency

	Color VGA TFT	Monochrome STN Dual Scan	Monochrome STN Single Scan	Color STN Dual
Clock frequency (MHz)	25.175	6.294	3.147	12.587
Frame frequency (Hz)	60	120	60	120

In principle, SVGA panel does not allow for simultaneous display, regardless of the video mode.

2.4 Panel Parameter Setup Method

The BIOS's panel parameters can be set using RAK. The necessary parameters are stored in the file with the BPX file extension; just use RAK to perform the setup. For connection information on each LCD, please refer to the separate "CARD-PC Technical Information." However, because this information is constantly updated, please see our home page or contact our sales personnel for the latest information.

3. Keyboard and Mouse Interface

See figure 3-1 for an example on connection between CARD-586 and keyboard/mouse. Because KBCLK, KBDATA, MSCLK, and MSDATA are bi-directional signals of the open drain output, external pull-up resistance of CARD-586 is required.

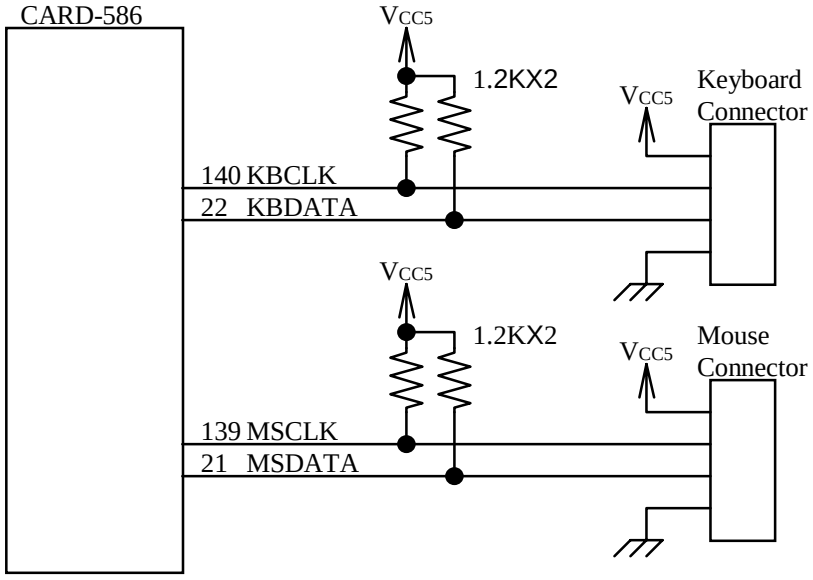


Figure 3-1 Keyboard and Mouse Interface

Also, if user-created hardware is to connect to the keyboard/mouse interface of CARD-586, then the PS/2 interface specification must be met. For reference purpose, a brief PS/2 interface hardware specification is included here as below. For details on the AC timing of CARD-586, please refer to CARD-586's hardware manual.

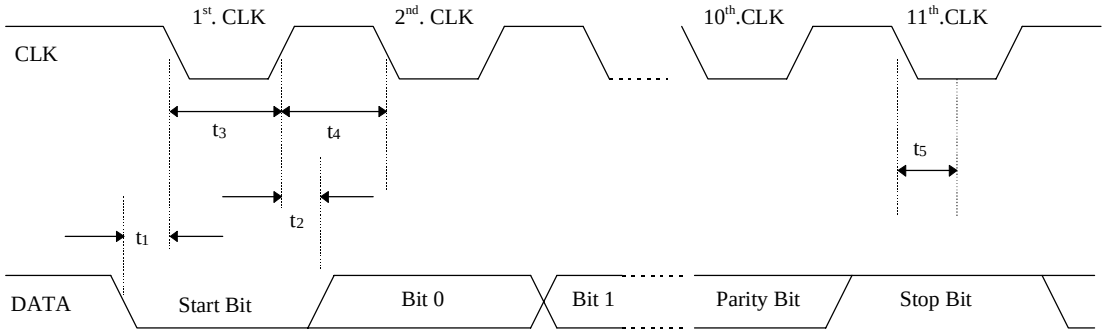


Figure 3-2 PS/2 Interface AC Timing During Reception (Reference)

Symbol	Parameter	Min.	Max.
t_1	DATA=LOW setup time for CLK shutdown	5	25
t_2	Duration from CLK startup to when DATA is confirmed	5	t_4-5
t_3	CLK's LOW pulse width	30	50
t_4	CLK's HIGH pulse width	30	50
t_5	Time delay for 11th. CLK shutdown when transmission is prohibited	0	50

Unit:μs

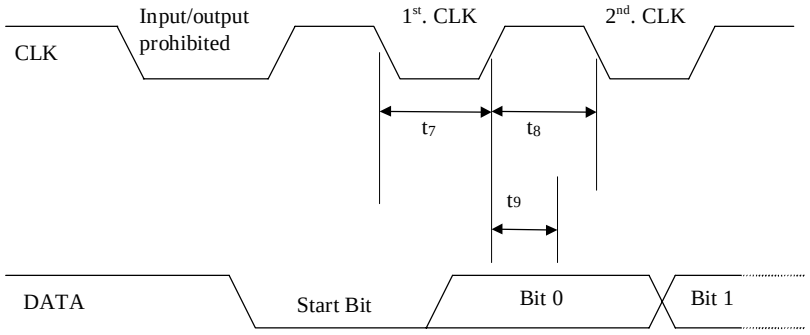


Figure 3-3 PS/2 Interface AC Timing During Transmission (Reference)

Symbol	Parameter	Min.	Max.
t_7	CLK's LOW pulse width	30	50
t_8	CLK's HIGH pulse width	30	50
t_9	Time range for device's DATA loading on CLK's startup	5	25

(Unit:μs)

4. FDD Interface

CARD-586 supports the following types of floppy disk drives, with a maximum connection of 2 drives.

Table 4-1 Supported FDD

FDD	Transmission Rate	Rotation Rate	FD	Unformatted	Formatted
5inch FDD	250Kbps	300rpm	2DS	500KB	360KB
5inch FDD	300Kbps	360rpm	2DS	500KB	360KB
	500Kbps	360rpm	2HD	1.6MB	1.2MB
3.5inch FDD	250Kbps	300rpm	2DD	1MB	720KB
	500Kbps	300rpm	2HD	2MB	1.44MB

Figure 4-1 shows an example of connection between CARD-586 and FDD. Because FDWP#, FDRD#, FDINDEX#, FDDCHG#, and FDTRK0# are output at the open collector from the FDD, external pull-up resistance at CARD-586 is required. For other signals, even though they are also output at the open collector from CARD-586, they do not need to be handled in the same way because there is already pull-up resistance inside the FDD usually.

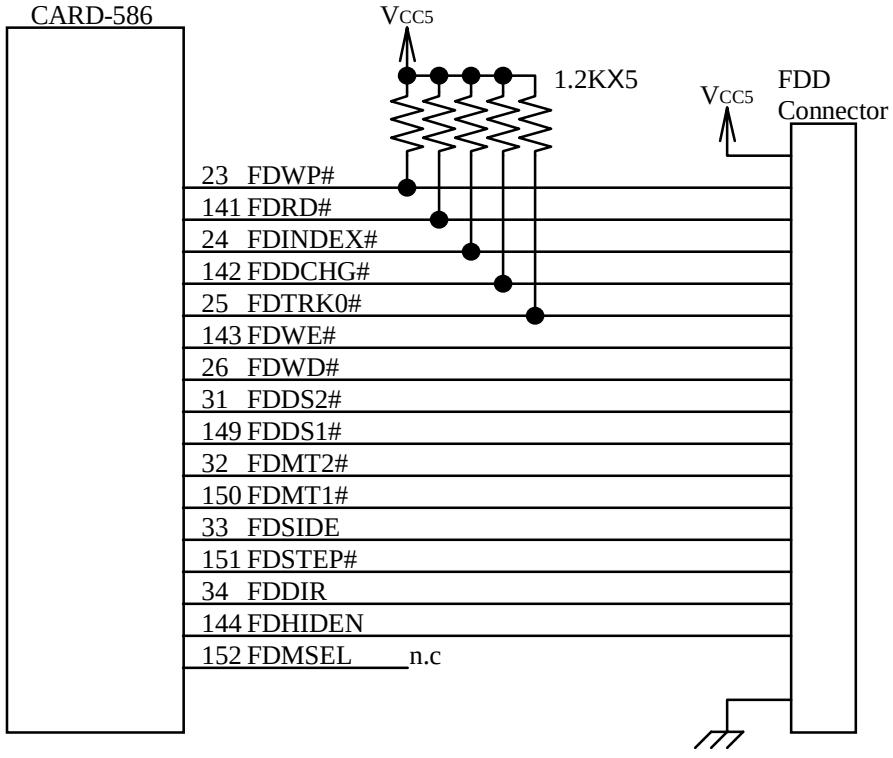


Figure 4-1 FDD Interface

CARD-PC does not support 3-mode FDD. To enable 3-mode FDD support, a separate FDD controller must be connected to the ISA bus. For details please contact us.

5. Serial Port Interface

5.1 RS-232C Interface

CARD-586 uses a 16550-compatible serial controller, with clock speed input at 1.8432MHz. This allows transmission from 50bps to 56000 bps (with an Tolerance of 2.86% for use up to 57600bps).
CARD-586's serial port interface can drive the TTL device directly, but long distance transfer via devices such as RS-232 requires driver/receiver IC that meets the standard specification. Figure 5-1 is a circuitry example using the NEC's RS-232C driver/receiver µPD4724. This IC converts TTL level signals and RS-232C compliant signals of CARD-586. Also, by having SMOUT0,1 of CARD-586 connected to STBY# of µPD4724, when CARD-586's serial port is in standby mode or suspend mode, the IC can also be set to the standby mode. However, to return from the standby mode via serial port interrupt or to resume via RI# signal, the driver/receiver ID must always be set to ON (STBY# = HIGH).

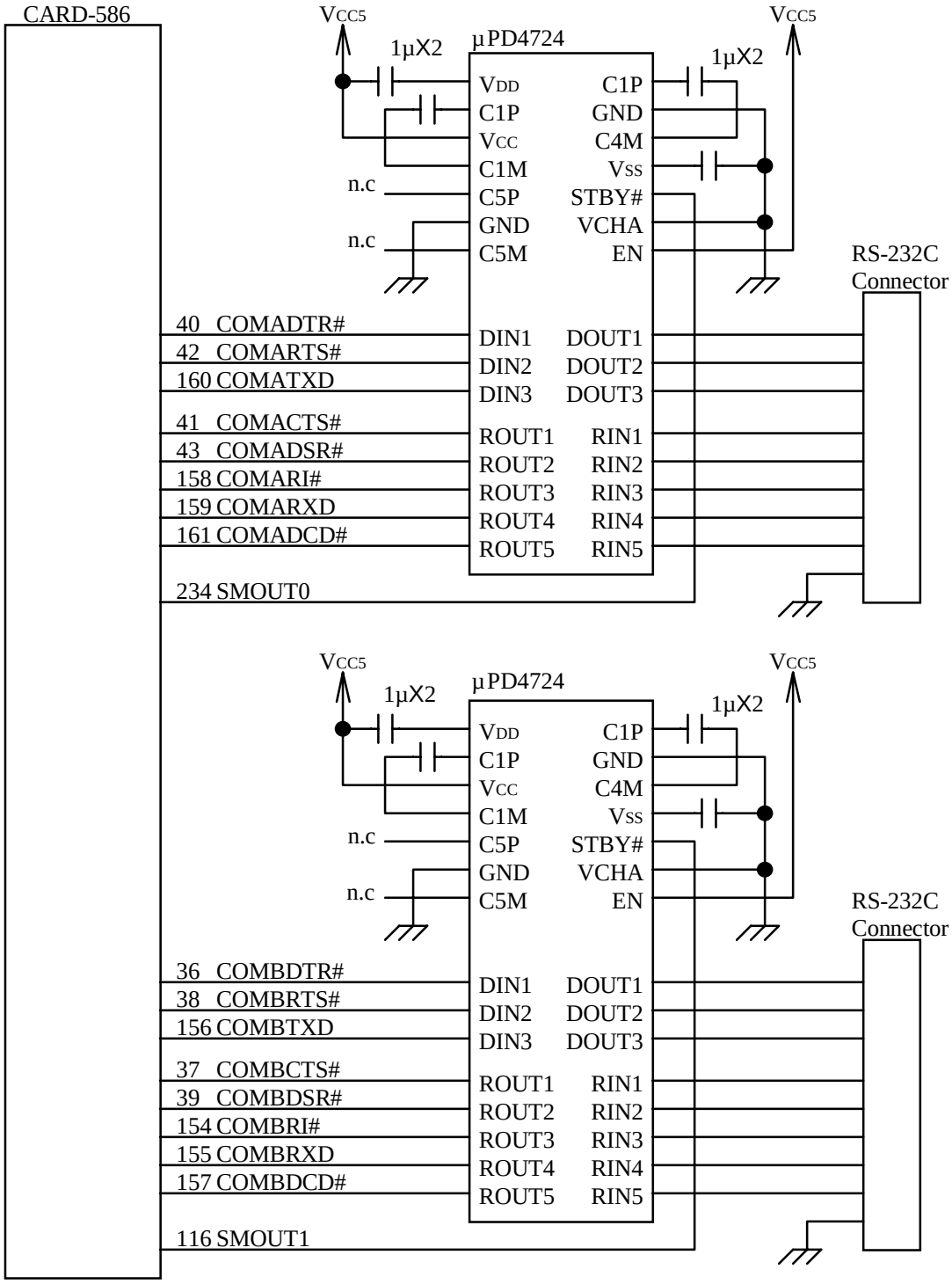


Figure 5-1 RS-232C Interface

5.2 Infrared Communication

CARD-586 supports both IrDA 1.0 and ASK protocols for infrared communication. Because these protocols make use of the internal serial controller of CARD-586, the COMB serial port cannot be used during infrared communication. Selection of IrDA, ASK or COMB can be done during CARD-586 setup using RAK. Figure 5-2 is a circuitry example on using TFDS3000 from TEMIC for infrared communication. TFDS300 is a light module with built-in light emission and light reception capability for infrared communication.

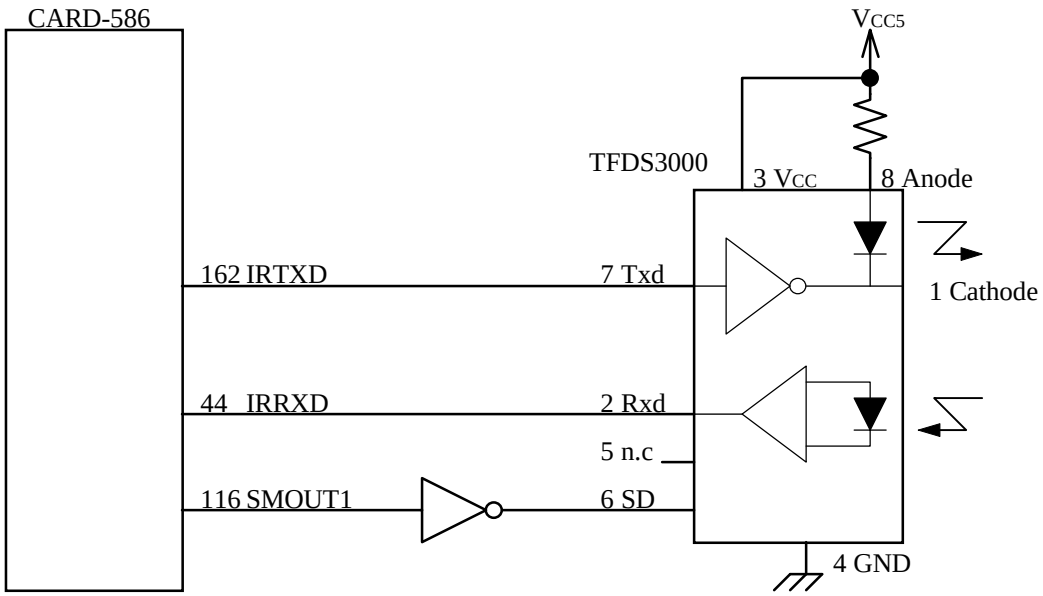


Figure 5-2 IrDA Interface

If the IrDA light module supplies power to the LED for a long time, the LED may become damaged. For this reason, be sure to protect the light source module input by adding, for example, the differentiating circuit. Polarity of the IRTXD of CARD-586 is as follows:

1. Default (reset)
   IRTXD is in the OFF state of the 3-State.
2. During transmission
   IRTXD sends data at active high. Be sure to design in a way so that the LED lights when IRTXD is HIGH.

While it is possible to have IRTXD become active low during transmission, change at the BIOS is required.

6. Parallel Port Interface

Figure 6-1 is a circuitry example on bi-directional parallel port. In this example, the data signal is stored in the buffer; however, it does not need to be stored in the buffer and CARD-586 and the parallel port connector can be directly connected.

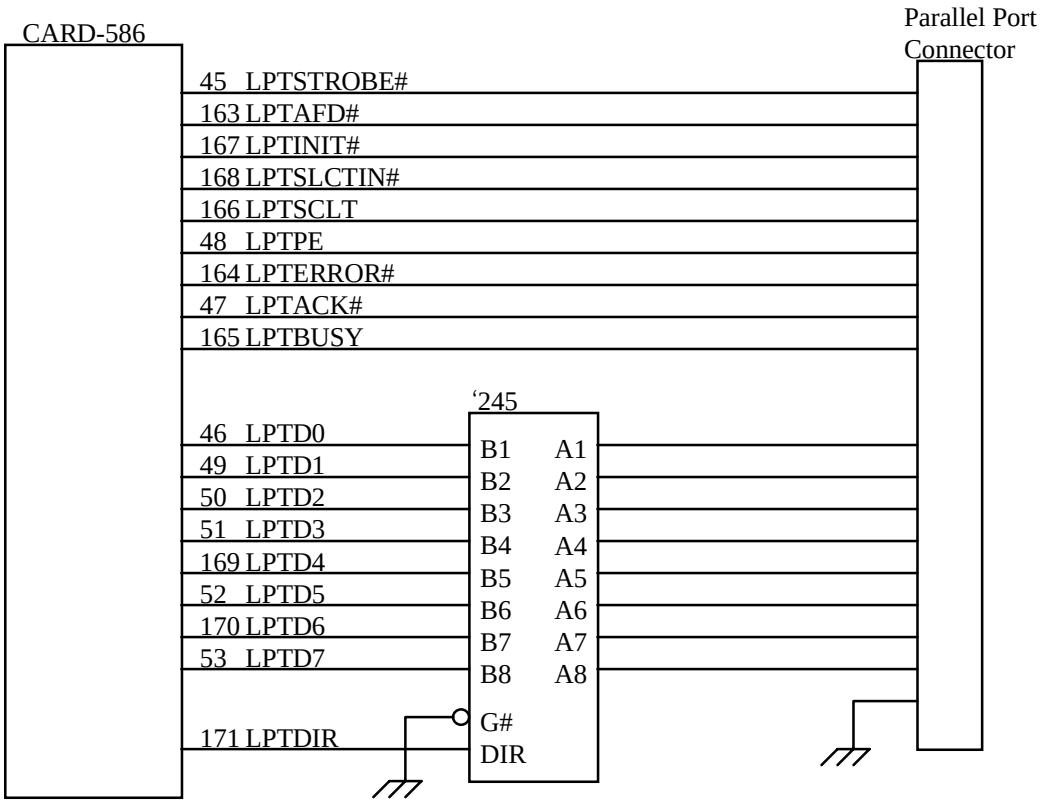


Figure 6-1 Parallel Port Interface

To add pull-up/pull-down resistance at the signal for handling the static electricity problem, align the resistance in the same direction as the internal design of CARD-586, as shown in table 6-1. (Please add the pull-up resistance to the pull-up signal, and pull-down resistance to the pull-down signal.)

Table 6-1 Parallel Port Pull-up/Pull-down Resistance

Signal Name	Resistance
LPTSTROBE#	Pull-up resistance
LPTAFD#	Pull-up resistance
LPTINIT#	Pull-up resistance
LPTSLCTIN#	Pull-up resistance
LPTSLCT	Pull-down resistance
LPTPE	Pull-down resistance
LPTERROR	Pull-up resistance
LPTACK#	Pull-up resistance
LPTBUSY	Pull-up resistance
LPTD0..7	Pull-down resistance

Because input and output configuration of the parallel port is determined by the CMOS device, if it is used without buffer, then depending on how it is used, problem may occur as a result of the inflow of electric current.

Table 6-2 Electric Current Inflow to Parallel Port

Problem	Power of CARD-586	Power of Device
1. No problem	ON	ON
2. Electric current flows to the parallel port of CARD-586.	OFF	ON
3. Electric current flows from CARD-586 to device.	ON	OFF
4. No problem	OFF	OFF

Table 6-2 shows how electric current flows when CARD-586 is ON and the device is OFF (or when CARD-586 is OFF and the device is ON). This causes excessive current to flow to the input protection diode or the parasite diode when there is input or output at the CMOS device, causing the CMOS device to latch up, or to become damaged in the worst case. For example, when power of a device such as a printer is ON, if it is connected to CARD-586 (which is OFF), immediately after power to CARD-586 is supplied, enough current may flow to cause the device to latch up. Therefore, try to avoid cases 2 and 3 in table 6-2.

7. HDD Interface

7.1 HDD Interface of CARD-586

CARD-586's BIOS can support up to four large-capacity HDDs (2 primary ports + 2 secondary ports). However, CARD-586's hardware can support only primary ports. If three or more HDD interfaces are required, a separate secondary port must be installed externally. The standard specifications of secondary ports are as follows:

Table 7-1 Secondary HDD Port Standard Specifications

I/O Port

Address	Register Name
170h	Data Register
171h	Error Register
172h	Sector Count
173h	Sector Number
174h	Cylinder High
175h	Cylinder Low
176h	SDH Register
177h	Status Register
376h	SDH Register
377h	Status Register

Hardware interrupt: IRQ15

Please contact us for detailed example on the circuitry, etc.

7.2 Buffered HDD Interface

HDD interface data bus /SA0..2/IOW#/IOR#/IOCS16# can be used by devices on other ISA buses. For this reason, the signal load becomes heavy so that not only the IDE HDD but also other devices and CARD-586 itself may not function normally. Also, if it is connected to the IDE HDD via a cable, then it may be affected by the noise. Normally, try to insert a buffer between CARD-586 and the IDE HDD, as shown in figure 7-1.

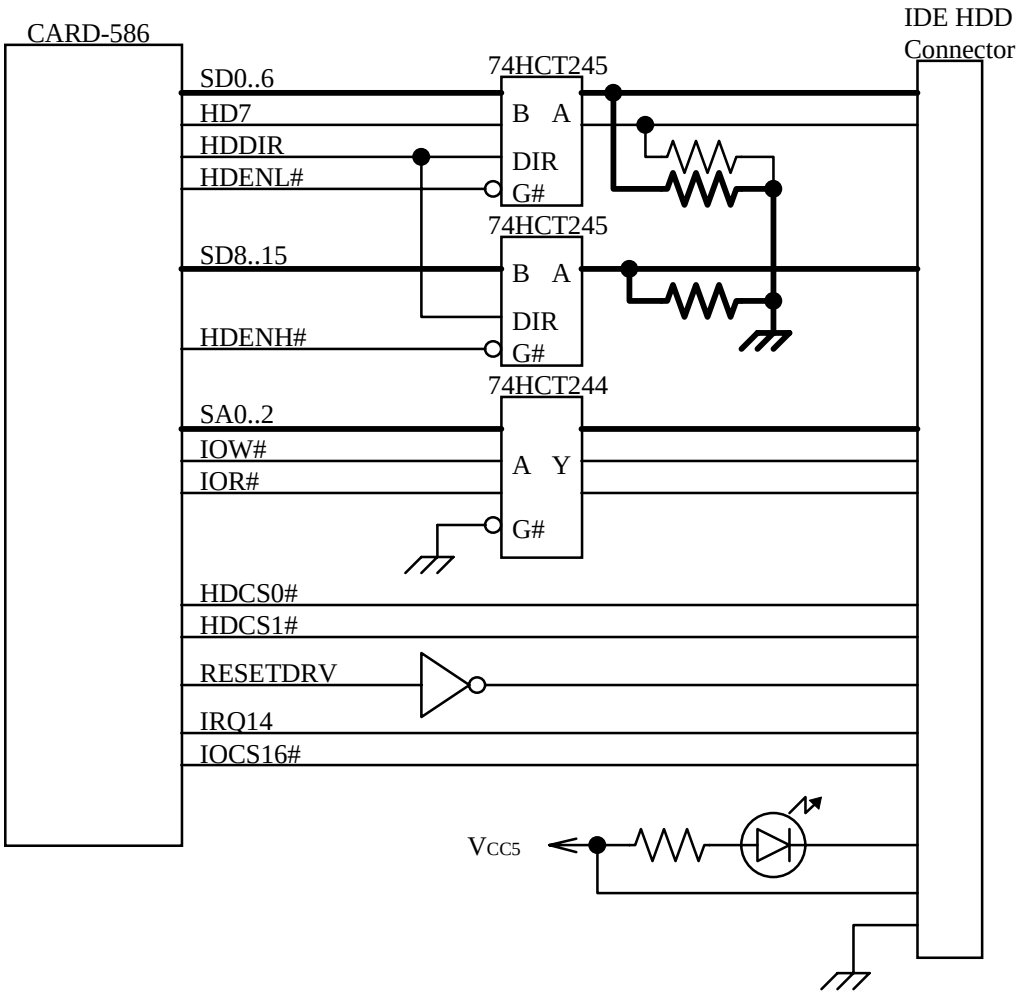


Figure 7-1 Buffered IDE HDD Interface

7.3 Direct HDD Interface

When signals are not shared with other devices and cable noise influence is small, then CARD-586, as shown in figure 7-2, can be connected directly to the IDE HDD, because the IDE HDD of chipselect can generate the required signal.

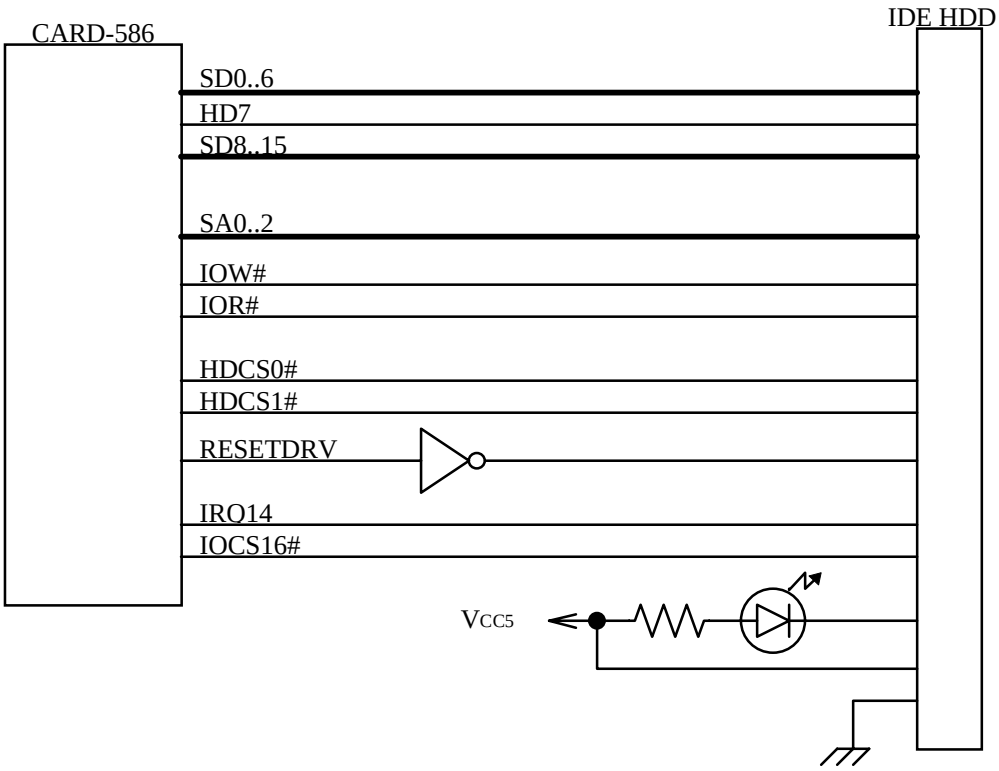


Figure 7-2 Direct IDE HDD Interface

7.4 HDD Power Down

When HDD is not used often other than occasional access for file read or write, it is mostly in its idle state. However, this idle state can still consume significant amount of electric power. On the other hand, for hard disk with software-controlled power-saving mode, the power consumption is actually not zero. CARD-586 has a circuitry built externally to it, as shown in figure 7-3, which can completely turn off power to the hard disk.

The external circuitry of CARD-586 makes use of SMOUT2 to control the ON/OFF of power to HDD. With the standard BIOS setting, when HDD's idle state is detected, SMOUT2 will be set to "Low". SMOUT2 returns to "High" when HDD is accessed.

When power to HDD is turned off, HDD must be completely cut off electrically from other devices including CARD-586. If it is not cut off from a device, then this device will not function normally. For this reason, a buffer must be built into HDD and the buffer must be controlled properly. While CARD-586 can control the chip select signals (HDCS0# and HDCS1#) and data buffer's control signals (HDENH# and HDENL#), other signals must be controlled by the external control circuitry of CARD-586. Also, circuitry for generating reset signal is also required, because when the power to HDD is ON, if HDD is not reset (power-on reset) it will not function normally.

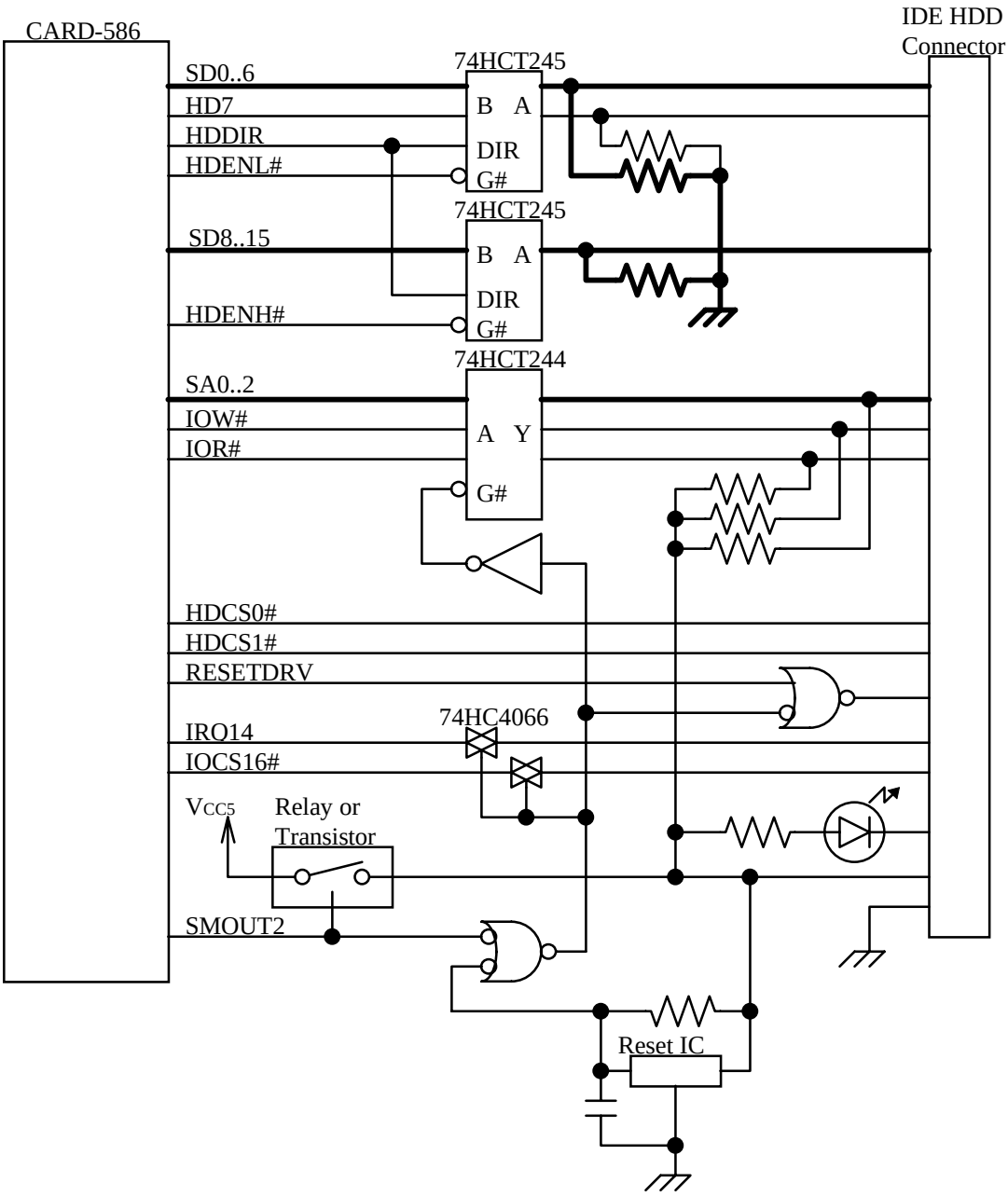


Figure 7-3 IDE HDD Interface with Power Down Control

8. ISA Bus Interface

8.1.1 Expansion of I/O Device

8.1.2 I/O Address

The I/O space of CARD-586 is 1KB (000h-3FFh), same as IBM PC/AT. The internal I/O device of CARD-586 can decode just the 10 bits of address SA0 to SA9. Also, as 000h-0FFh is used internally by CARD-586, this space cannot be used on the ISA bus. Similarly, 100h-3FFh also contains address used internally by CARD-586. When adding features on the ISA bus, be careful not to use I/O addresses already being used internally by CARD-586.

The following table lists I/O addresses used internally by CARD-586, as well as I/O addresses that can be used on the ISA bus.

Table 8-1 I/O Address

Address	Usage
000h - 0FFh	Cannot be used by ISA bus as already being used internally by CARD-586
100h - 16Fh	Can be used by ISA bus.
170h - 178h	Used by secondary HDD (note 1).
179h - 1EFh	Can be used by ISA bus.
1F0h - 1F8h	Used by HDD. (note 2)
1F9h - 277h	Can be used by ISA bus.
278h - 27Fh	Used by the parallel port. (note 3)
280h - 2E7h	Can be used by ISA bus.
2E8h - 2Efh	Used by the serial port. (note 4)
2F0h - 2F7h	Can be used by ISA bus.
2F8h - 2FFh	Used by the serial port. (note 4)
300h - 377h	Can be used by ISA bus
378h - 37Fh	Used by the parallel port. (note 3)
380h - 3Afh	Can be used by ISA bus
3B0h - 3DFh	Used by VGA. (note 2)
3E0h - 3E7h	Can be used by ISA bus.
3E8h - 3Efh	Used by the serial port. (note 4)
3F0h - 3F7h	Used by FDC. (note 2)
3F8h - 3FFh	Used by the serial port. (note 4)

(note 1) If no secondary HDD interface is on the ISA bus, then the I/O address can be used on the ISA bus.

(note 2) When these features are not used, then the I/O address can be used on the ISA bus.

(note 3) Because CARD-586 has only one parallel controller, one out of the two areas can be used on the ISA bus. If no parallel port is used, then all of the two areas can be used on the ISA bus.

(note 4) Because CARD-586 has only two serial controllers, at least two out of the four areas can be used on the ISA bus. If no serial port is used, then by disabling the internal serial port of CARD-586 , all of the four areas can be used on the ISA bus.

8.1.3 Decoding I/O Address

The internal I/O address of CARD-586 is decoded on the 10 bits (000h - 3FFh) of Sa0 to SA9, similar to IBM PC/AT. Therefore, be careful as I/O address above 400h is duplicated at 000h-3FFh. For example, if 0400h-040Fh on the ISA bus is set for the I/O device (full decode of SA0 to SA15), when 400h-40Fh is accessed, this will cause conflict with the internal DMA register of CARD-586 (000h - 00Fh) and CARD-586 will not function normally. For this reason, when mapping fully decoded I/O device to I/O space above 400h, be careful to select an I/O address so that the lower 10 bits of the address will not overlap with the internal I/O device of CARD-586.

During DMA transfer at CARD-586, when DMA is transferred from the memory to the I/O, the memory address is output to the address bus (SA0-19, LA16-23), and both IOW# and MEMR# become active at the same time. On the other hand, when DMA is transferred from the I/O to the memory, the memory address is output to the address bus, and both IOR# and MEMW# become active at the same time. This means that during DMA transfer, regardless of whether there is address in relation to the memory or not, IOR# or IOW# become active, Therefore, the I/O device must be designed in a way so that it will not function even when the address for the DMA transfer matches the address being used by itself. To make this possible, AEN can be used. AEN becomes HIGH during DMA transfer. Usually, be sure to design in a way that when AEN is HIGH, the I/O device will prohibit address decode.

The following is a simple example. The I/O device in this example uses the 100h I/O address.

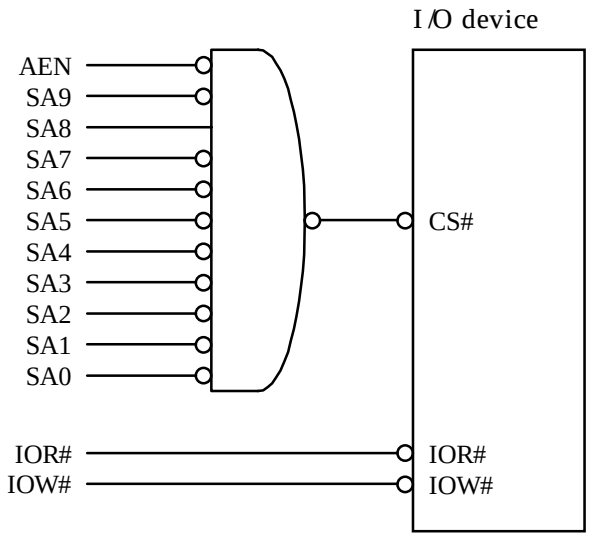


Figure 8-1 I/O Device Connection Example

8.2 Memory Device Expansion

The ISA bus provides 16MB of memory space. SMEMR#/SMEMW# become active only when memory is accessed in the 0-1MByte range by the memory control signal used for XT bus (with memory space of 1MB). MEMR#/MEMW# become valid in all of the memory range of the ISA space by the memory control signal used for the AT bus (with memory space of 16MB). However, similar to the I/O address, the memory address used by the internal DRAM or flash ROM of CARD-586 cannot be used on the ISA bus. Also, when the DRAM installed in CARD-586 is accessed, SMEMR#/SMEMW#MEMR#/MEMW# on the ISA bus do not become active. Table 8-2 indicates the memory map of CARD-586 with standard BIOS.

Table 8-2 CARD-586 Memory Map

Address	Mapped Device	
000000h - 09FFFFh	DRAM	
0A0000h - 0BFFFFh	VGA	(note 5)
0C0000h - 0C7FFFh	DRAM(VGA BIOS)	(note 5)
0C8000h - 0CFFFFh	ISA	(note 6)
0D0000h - 0D7FFFh	ISA	(note 6)
0D8000h - 0DFFFFh	ISA	(note 6)
0E0000h - 0E7FFFh	ISA	(note 6)
0E8000h - 0EFFFFh	ISA	(note 6)
0F0000h - 0FFFFFh	DRAM(BIOS)	
100000h - FBFFFFh	DRAM	
FC0000h - FEFFFFh	DRAM or flash ROM	(note 7)
FF0000h - FFFFFFh	DRAM or flash ROM	(note 7)
1000000h - 1FFFFFFh	DRAM or none	(note 8)
2000000h - 2FFFFFFh	DRAM or none	(note 8)

(note 5) ISA bus can be used when the internal VGA of CARD-586 is not used.
(note 6) See the "10. User Program" section.
(note 7) Depending on the internal flash ROM setting of CARD-586 at RAK
(note 8) Depending on the internal DRAM capacity of CARD-586

8.3 8/16-bit Device

The I/O memory data bus on the ISA bus can either be 8- or 16-bit. If the cycle target is 8-bit device, CARD-586 sends data using SD0-7; if the cycle target is 16-bit device, then CARD-586 sends data using SD0-15. Therefore, when the cycle target is a 16-bit device, the device needs to drive MEMCS16# or IOCS16# to become active, and inform CARD-586 that the target is a 16-bit device. Because MEMCS16#/IOCS16# is a signal that can be "Wired Or", it must be driven at the open collector. As they are pulled up internally at CARD-586, they are inactive normally (when "Low" is not driven). Because of this reason, an 8-bit device does not need to drive MEMCS16#/IOCS16# to become inactive.

8.3.1 16-bit Memory Device

For memory devices holding 16-bit data, they must keep MEMCS16 active until termination of t_S, as shown in figure 8-2. Because CARD-586 latches MEMCS16 upon termination of t_S, it has no meaning in other periods.

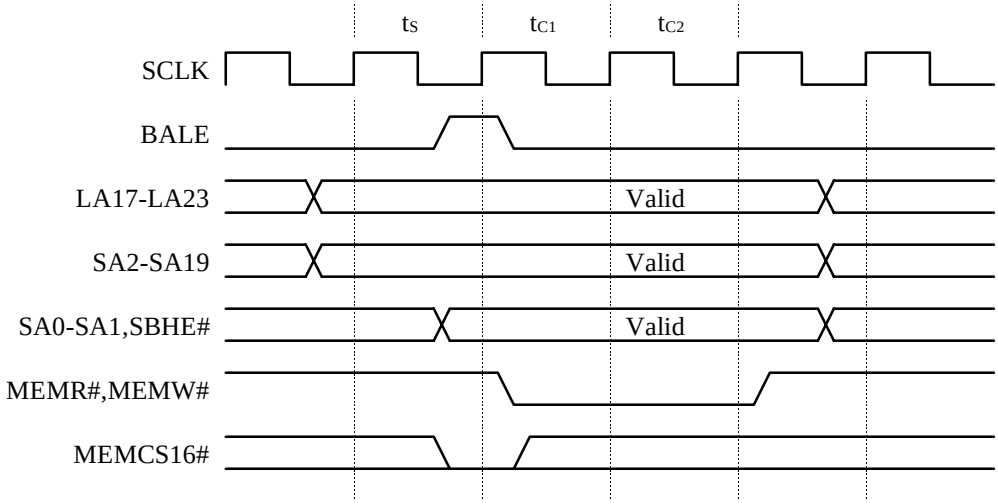


Figure 8-2 MEMCS16# Timing

Figure 8-3 indicates a MEMCS16# generation circuitry example. In this example, the memory device using memory address A00000h-BFFFFFh to decode the address and drive MEMCS16 by the open collector.

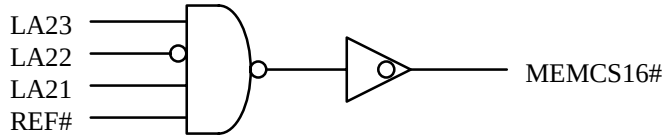


Figure 8-3 MEMCS16# Example(1)

While MEMCS16# is also used in determining whether the memory is 8- or 16-bit during DMA transfer, it does not cause any problem in circuitry such as the one indicated in figure 8-3.

Figure 8-4 indicates use of memory address 0D0000h-0DFFFFh.

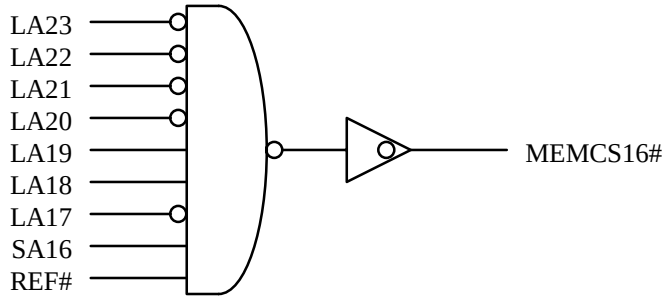


Figure 8-4 MEMCS16# Example(2)

In this case also, the address is decoded and MEMCS16 becomes active at the open collector.; however, pay attention to the location in the address code where SA16 is used. For CARD-586, both SA2-SA19 and LA17-LA23 output valid values at the same timing. This timing is sufficient for decoding the address and driving MEMCS16# (duration from when the address becomes valid to termination of t_S).

On IBM PC/ATs (same for CARD-386/486 using Intel SL chipset), SA2-SA19 becomes valid at the same timing as SA0, SA1, and SBHE#, as indicated in figure 8-2. Because of this reason, the duration from when the address (in this example SA16) becomes valid to termination of t_S (time required to decode the address) becomes shorter, and the system cannot correctly latch the value of MEMCS16#, thus possibly causing incorrect operation. However, most of the recent PCs have specifications same as CARD-586 so that both SA and LA can be output at the same timing, thus causing no problem. Future release of CARD-PCs will continue to use this specification. This means there is no need to latch at BALE when generating MEMCS16# or decoding memory address (generating memory's chip select signal).

8.3.2 16-bit I/O Device

Figure 8-5 indicates the timing of IOCS16#. Because IOCS16# is not latched by CARD-586, there is no need to keep it active during the period from TC1 termination to end of the cycle.

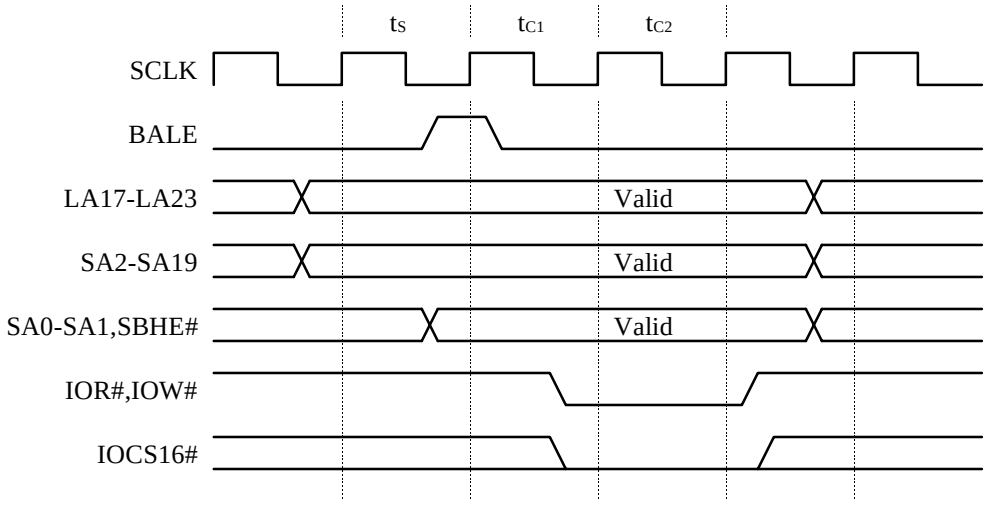


Figure 8-5 IOCS16# Timing

The IOCS16# generation decodes the address and drives IOCS16# by the open collector.

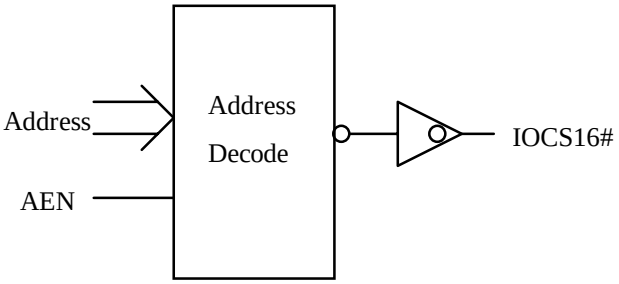


Figure 8-6 IOCS16# Example

8.4 IRQ and DRQ

Be sure to pay attention to the following when using IRQ and DRQ available on CARD-586.
The FDD interface built into CARD-586 makes use of IRQ6 and DRQ2. As indicated in the block diagram in figure 8-7, the IRQ/DRQ from the internal FDD controller and IRQ/DRQ from ISA are "Wired Or". Therefore, when using the internal FDD interface, make sure IRQ6 and DRQ2 on the ISA bus are not connected or are at high impedance.

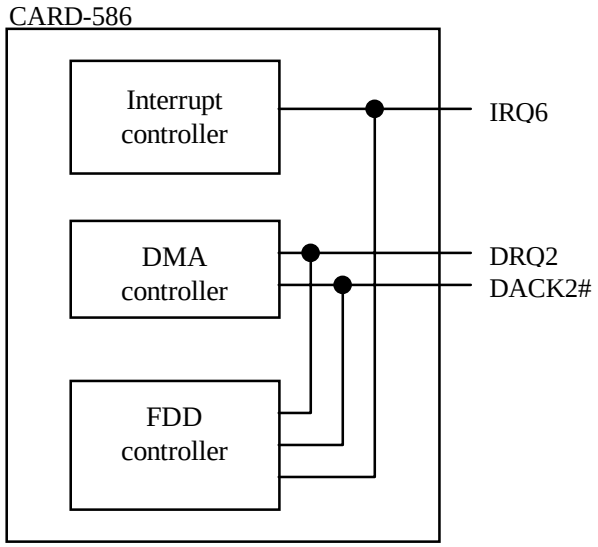


Figure 8-7 IRQ6/DRQ2 Block Diagram

In the same way, the serial interface uses some of IRQ3, 4, 10 and 11 (IRQ3, 4 by default), and the parallel interface uses either IRQ5 or 7 (by default IRQ7). The choice of IRQ for these interfaces can be changed from the CARD-586 setup or using RAK.

On the other hand, IRQ12 is used for the mouse interface. On CARD-586, IRQ12 cannot be used on the ISA bus.

8.5 ISA Data Buses

To determine existence of option board, some applications may write to the I/O port followed by immediate read of the port. These types of applications expect data on the data bus to change at FFh when there is no I/O port. This is not a problem when there is I/O port. However, when there is no I/O port but
there is data written on the data bus and kept until the next bus cycle, the application may incorrectly interpret that an I/O port exists even though there is none. To avoid this kind of problem, be sure to pull up the data bus.

8.6 Bus Clock (SCLK)

The ISA bus operates according to the bus clock (SCLK). However, CARD-586 splits cycle CPUCLK and generates SCLK. CARD-586 has SCLK = 33 / 4 = 8.25 MHz. Because CPUCLK is generated by PLL, there is some Tolerance. This means SCLK itself also contains Tolerance. Because of this reason, SCLK cannot be used at clocks requiring precision. Instead, a combination of SCLK and non-synchronous OSC (14.31818MHz), or addition of vibrator at the local is recommended.
Also, because the ISA bus timing is also affected by SCLK, be sure to allow margin in design for operation where SCLK can vary between 6.78MHz and 10MHz.

9. Power Management

9.1 System Management OUT (SMOUT)

The standard BIOS in CARD-586 comes with SMOUT0-2 to control power of the following devices:

SMOUT0 Controls COMA.
Because SMOUT0 becomes Low when COMA is in the standby state or when CARD-586 is in suspend mode, RS-232C driver/receiver IC can be turned to standby.

SMOUT1 Controls COMB.
Because SMOUT1 becomes Low when COMB is in the standby state or when CARD-586 is in suspend mode, RS-232C driver/receiver IC can be turned to standby.

SMOUT2 Controls HDD.
Because SMOUT2 becomes Low when HDD is in the standby state or when CARD-586 is in the suspend mode, power to HDD can be turned OFF. HDD uses many signals which are also shared by the ISA bus. When power to HDD is turned OFF, if the shared signals are not put into isolation, this will cause incorrect operation. So pay attention to this problem.

SMOUT3 is used for switching voltage of power source PGM which is used for flash ROM update.

9.2 Battery Monitor Signals

CARD-586 provides two pins, BATWARN# and BATLOW#, for battery warning of battery-driven systems. When these signals become active, CARD-586's standard BIOS will perform the following operations. (These operations can be disabled at CARD-586 setup.)

BATWARN#
This input signal is for low battery warning. When this signal becomes active, the speaker interface sounds low battery warning beeps.

BATLOW#
While BATWARN# sounds the beeps as low battery warning, BATLOW# handles the next phase. When the battery continues to drop to a stage where the system can no longer work, this signal will become active, causing CARD-586 to enter the suspend mode.

9.3 EXTSMI#

By turning EXISMI# to become active, it is possible to perform CPU interrupt and run any required program regardless of the application or operating system. Since this program belongs to the system, CARD-586's standard BIOS does not support it. Therefore, this program must be newly created in order to use EXTSMI#.

9.4 Suspend Mode

CARD-586 supports suspend mode. In this model, the CPU enters the standby state, and uses very little electric current consumption to keep data in memory and registers alive. When CARD-586's standard BIOS (with suspend mode enabled at setup) detects the RBTN# pin's shutdown edge of RBTN#, it enters the suspend mode. When resume is performed, it exits the suspend mode and CARD-586 returns to where it was before the suspend mode. There are three ways to perform a resume, as follows:

1. When SRBTN# pin's shutdown edge is detected
2. When COMARI# and COMBRI# pins' shutdown edges are detected
3. At the time specified by setup

Tables 13-2 to 13-10 indicate the states of CARD-586 pins in suspend mode with standard settings of the BIOS. Depending on shapes of pins and how the pins external to CARD-586 are handled, the electric current consumption of CARD-586 may increase. In order to avoid increase of electric current consumption, take notes of the following cautions.

1. When pull-up resistance is added to the pin driving CARD-586 to Low, electric current will flow to the resistance and electric current consumption will increase. In section "13 Pin Handling," table 13-1 has the description "Pin driving Low regardless of whether CARD-586 itself has pull-up resistance or not," but when CARD-586 itself drives the Low, then the pull-up resistance is detached and so no electric current will flow to the pull-up resistance.
2. When pull-down resistance is added to the pin driving CARD-586 to High, electric current will flow to the resistance and electric current consumption will increase. In section "13 Pin Handling," table 13-1 has the description "Pin driving High regardless of whether CARD-586 itself has pull-down resistance or not," but when CARD-586 itself drives the High, then the pull-down resistance is detached and so no electric current will flow to the pull-down resistance.
3. When Low is input to a pin with pull-up resistance, electric current will flow to the pull-up resistance and the electric current consumption will increase.
4. When High is input to a pin with pull-down resistance, electric current will flow to the pull-down resistance and the electric current consumption will increase.
5. For input pins with no pull-up/pull-down resistance, be sure to check the level. Avoid state where input is floating.

6. When outputting OFF of 3-State from CARD-586, if it is connected to the CMOS device with the power still ON, check that the device is input at the pull-up/pull-down resistance.

7. For only the devices connected to pin in the following cases, they can be done with the power off during the suspend mode.

   Output pins with 3-State is OFF
   Pins driving Low
   Input pins with pull-down resistance
   Input-output pins with pull-down resistance and in input state

   For pins in other states, electric current flows to the pull-up/pull-down resistance or input is floating, so that power to the device cannot be turned off. To turn it off, a buffer must be added between CARD-586 and the device. (See the "7.4 HDD Power Down" for more information.)

10. User Program

CARD-586 comes with 256KB of built-in flash ROM for storing BIOS/SETUP, etc. More than half of the flash ROM space is empty and is available for the user to store programs and data. Programs can be copied to and then executed from the DRAM area between 0A0000 and 0EFFFFh. Because the memory area for storing copy of a program is modified so as to map the DRAM, this area can no longer be used on the ISA bus.

For explanation on storing programs in the flash ROM, please refer to "CARD-PC ROM Adaptation Kit for DBIOS Manual."

11. Others

11.1 Generic Timer Output (Watchdog Timer)

CARD-586 comes with a generic timer which can be used as a watchdog timer. This timer uses channel 1 of the extended timer 8254 with base clock of 8KHz. Its OUT1 is output as it is to the WDTIM# pin of CARD-586.

The method of using the watchdog timer on CARD-586 is as follows:

1. Set up timer.
2. Application software resets timer before it times out, then restarts.
3. If the software crashes, etc. so that the timer cannot be reset before the timeout, then WDTIM# will become active.

CARD-586 provides the following BIOS functions for using the watchdog timer:

- Get watchdog timer status.
- Get protected mode interface routine address.
- Set, start, and reset timer.

(For details, please refer to "BIOS Reference Manual".)

Usually WDTIM# is High, but becomes Low when there is a timeout. When a timeout occurs, how this will be handled depends on the external circuitry of CARD-586. Usually the following circuitry are used.

1. Connect WDTIM# to the IRQ pin. When timeout occurs, an interrupt is performed at the CPU.

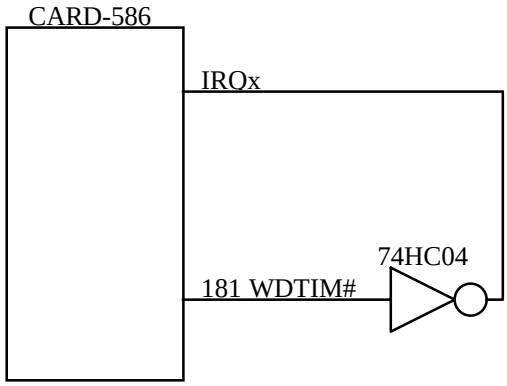


Figure 11-1 Interrupt at WDTIM#

2. Connect WDTIM# to the IOCHCK# pin. When a timeout occurs, add NMI to the CPU.

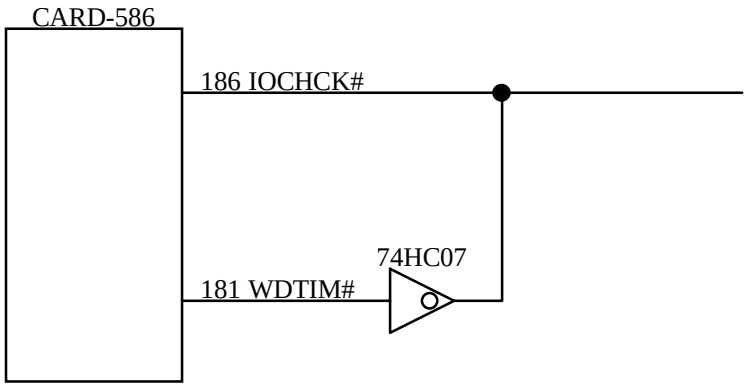


Figure 11-2 NMI with WDTIM#

3. Connect WDTIM# to the EXTSMI# pin. When a timeout occurs, add SMI to the CPU.

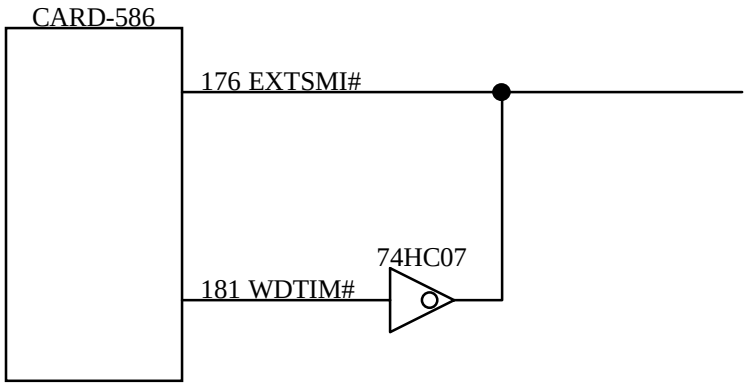


Figure 11-3 SMI with WDTIM#

4. Connect WDTIM# to the POWERGOOD pin. When a timeout occurs, reset CARD-586.

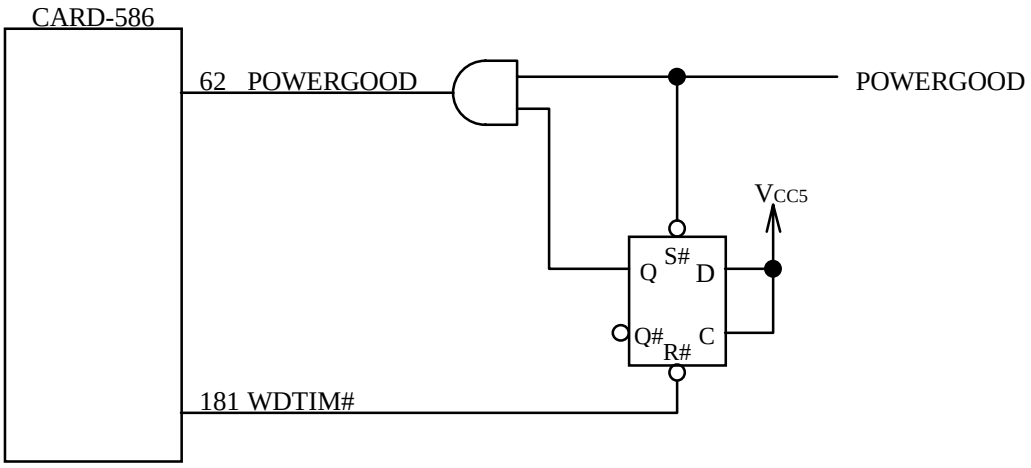


Figure 11-4 Reset with WDTIM#

This diagram is only a conceptual diagram. When the system is backing up the internal CMOS-RAM of CARD-586 using the battery, glitch may occur at the power good and the CMOS-RAM contents may become damaged. So be aware of this problem. For details, please see 11.2/11.2.1/11.3/11.4.

To use interrupt, NMI, and SMI, their respective routine must be created.

11.2 Flash ROM Update

When necessary, the BIOS flash ROM (256KB) inside CARD-586 can be updated using one of the following two methods:

1. Update the flash ROM with CARD-586 still embedded in a machine.
2. Use the ROM writer for CARD-PC.

11.2.1 Flash ROM Update Circuit

To update the flash ROM with CARD-586 still embedded in a machine. the PGM pin must be supplied with +12V electric power. Make sure to keep the level to 0-5V for normal operation. A special program is required to write data to the flash ROM. The flash ROM update program from Epson, WFLASH.EXE, allows easy update of the ROM contents. If WFLASH.EXE is used, the circuitry as indicated in figure 11-5 is required.

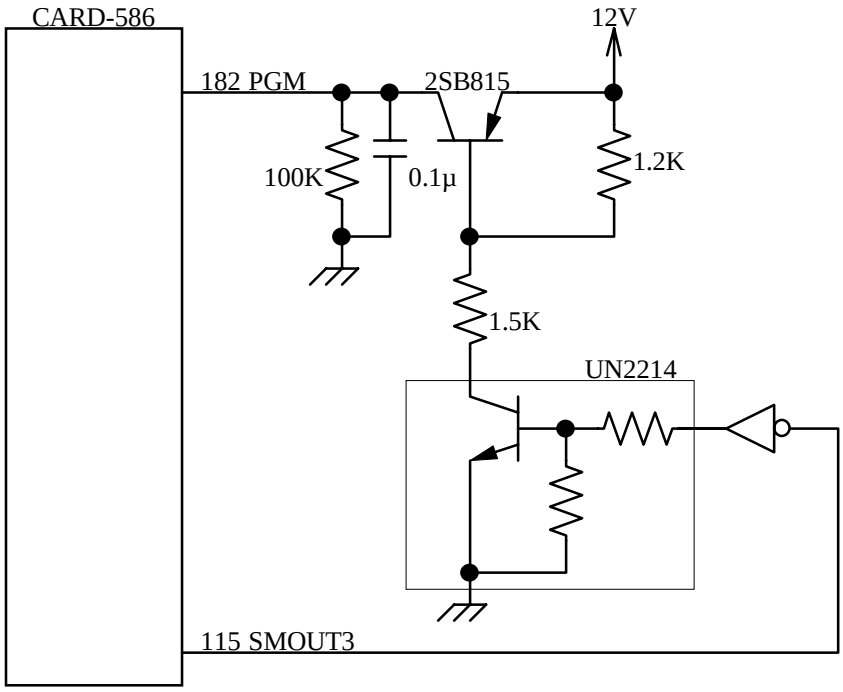


Figure 11-5 Flash ROM Update Circuit

11.2.2 ROM Writer for CARD-PC

For information on the ROM writer for CARD-PC, please refer to the manual of the ROM writer for CARD-PC.

The FLOAT# and ROMCE0# pins are required only when using the ROM writer for CARD-PC. For normal operation, make sure they are unconnected.

11.3 Backup of RTC and CMOS RAM

Even when the system power is OFF, data in the RTC and CMOS RAM inside CARD-586 can be kept with the use of external backup power.

11.3.1 Backup Power Supply

V_{BK} is a power pin for backup of RTC (Real Time Clock) and CMOS RAM. When power (V_{CC5}, V_{CC3}) is supplied to CARD-586 (ON), the same power as V_{CC5} is supplied to the V_{BK} pin; when power is not supplied to CARD-586 (OFF), power is supplied from the backup power (lithium battery, etc.). Figure 11-6 indicates a sample circuitry for power switching.

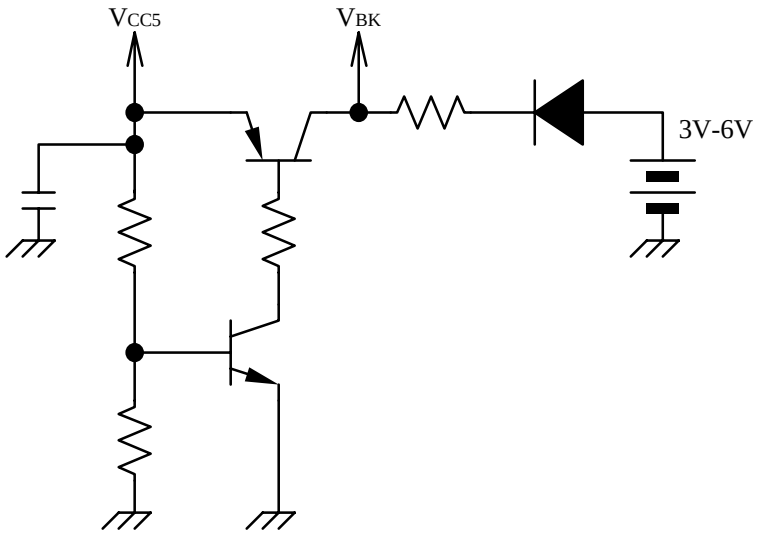


Figure 11-6 Sample Power Switching Circuit (1)

If backup of RTC and CMOS RAM is not required, be sure to supply the same power as V_{CC5} of CARD-586 to the V_{BK} pin. The default BIOS settings of CARD-586 assume backup of the RTC and CMOS RAM, therefore if no backup is required, the BIOS must be changed by using RAK.

11.3.2 Precautions on Systems for Backing Up RTC/CMOS RAM

If problems such as complete absence of backup power supplied at the system for backing up RTC and CMOS RAM, CARD-586's BIOS will perform tasks to circumvent the problem. In this case (using RAK), note the following points.

When backing up the RTC/CMOS RAM of CARD-PC, voltage of the backup power should be maintained at 2.5V or above at the CARD-PC. Therefore, be sure to keep the voltage at this level during the backup period. If backup power falls below 2.5V, the RTC contents (time, etc.) and CMOS RAM contents (setup information, etc.) will be damaged.

The RTC controller of CARD-PC has a bit to indicate "No backup power was supplied while the power was OFF." (CMOS RAM index 0Dh. For details refer to "BIOS Reference Manual".) This happens in the following cases:

- CARD-PC is disconnected from the system.
- Backup battery is completely discharged (with almost 0V).
- Backup battery is disconnected, or reconnected after being disconnected.

CARD-586's BIOS can examine this bit in the RTC controller as well as the RTC/CMOS RAM contents (Checksum, for example. However, date/time information cannot be obtained unless they have abnormal values.), and then correct the RTC/CMOS RAM data. This selection and the BIOS setup can be performed at RAK. By default, if "No backup power is supplied" is detected, or the RTC/CMOS RAM content is damaged (checksum error or date/time error is detected), the preset default CMOS value will be loaded.

When the default CMOS value is loaded, the setup information will change and may affect the system operation. To handle this, CARD-586's BIOS provides a bit to indicate that the default CMOS value has been loaded.

[CMOS RAM Index 0Eh**]**
bit 1 1: Default CMOS is loaded
0: Default CMOS is not loaded

This bit is not cleared (=0) until CARD-586's setup program starts. Therefore, the system can include a program (as one of its first tasks to carry out) to check this bit and perform any necessary operation to avoid the problem due to change of the setup information.

11.4 Power (V_{CC5}/V_{CC3}) and POWERGOOD

In figure 11-1, the diagram indicates the V_{CC5}/V_{CC3}/POWERGOOD sequence when the power is ON/OFF. For timing other than those indicated in the diagram, make sure $V_{CC5} \geq V_{CC3}$ is always true. When the power is on, if CARD-586 is not reset, then it cannot start to function normally. Therefore, POWERGOOD needs to be input according to the timing indicated in the diagram.

On the other hand, POWERGOOD is also used for isolation of RTC and CMOS inside CARD-586 from other circuitries. Because of this, if POWERGOOD is High before V_{BK} switches from the lithium battery to V_{CC5}, the RTC/CMOS RAM content may become damaged. Therefore, be careful not to have POWERGOOD exceed 0.8V when power is switched from the lithium battery to V_{BK}.

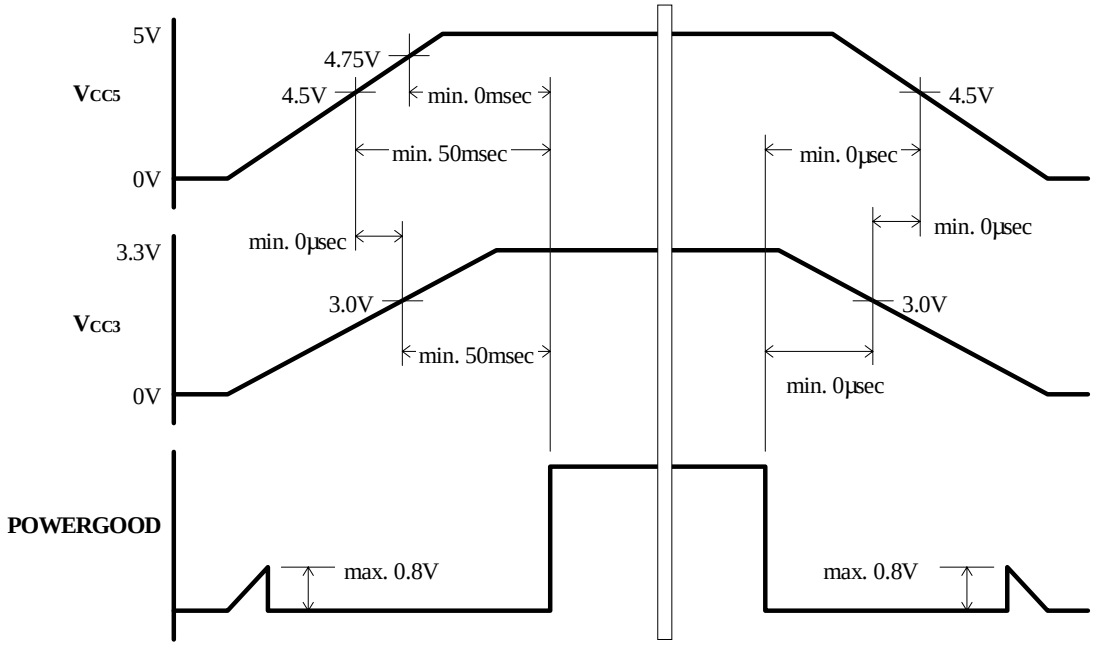


Figure 11-7 Power-up/Power-down Sequence

[Reference] ●Battery V_{CC} switching and POWERGOOD signal emission circuitry
The MAX703 from MAXIM enables easy design of battery/V_{CC} switching and POWERGOOD signal emission circuitry. Figure 11-8 is a circuitry for reference.

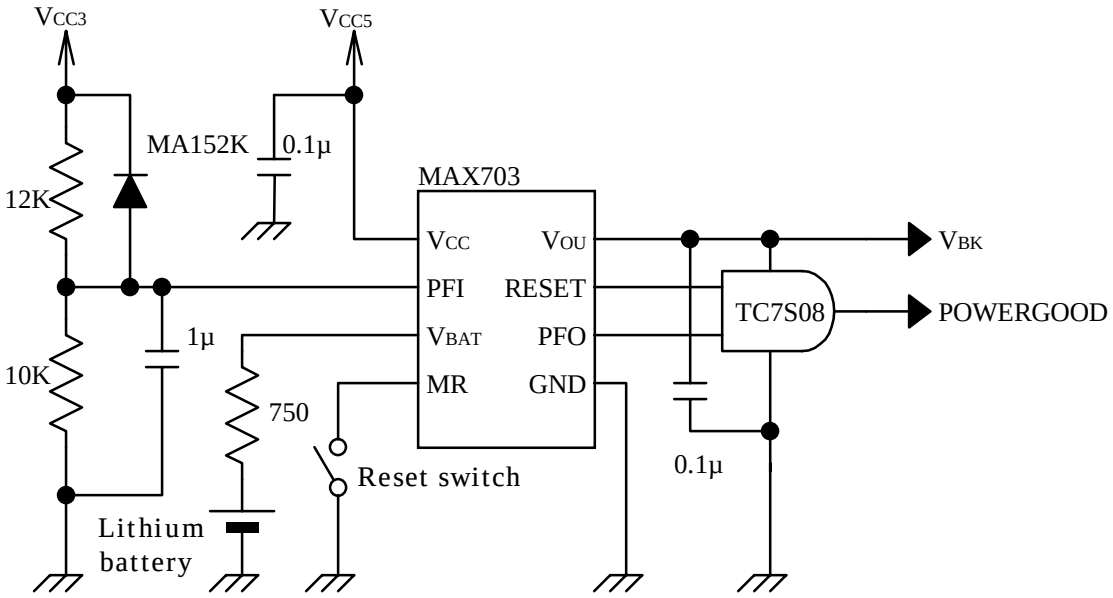


Figure 11-8 Power Source Switching Sample Circuit (2)

At the above circuitry configuration, if the watchdog timer is used, be sure not to connect the WDTIM# signal directly to the MR pin. The MR pin is pulled up at VOU inside MAX703 (simulated). If the WDTIME# signal is directly connected to the pin, then when the power is OFF (V_{CC5}=V_{CC3}=0V), leak current will flow from V_{BK} to the WDTIM# signal, causing the battery life of the lithium battery to shorten drastically. In this case, when the power is OFF, the WDTIM# signal and the MR pin should be completely separated with use of, for example, 4066. (See figure 11-9 on the MR and WDTIM# separation sample circuitry.)

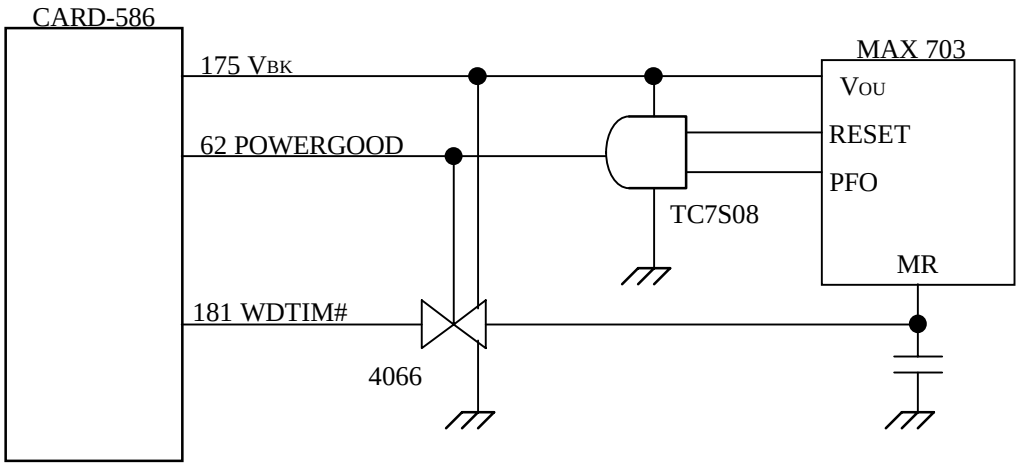


Figure 11-9 MR and WDTIM# Separation Sample Circuit

12. Matters to be Noted in Use of CARD-PC

12.1 Power Supply and Grounding

12.1.1 Power Connection

Because CARD-586 is a machine which contains high speed CPU and peripheral circuitry, when it operates, it causes vigorous change in electric current consumption. To ensure stable CARD-586 operation and display quality, try as much as possible to use low impedance when connecting CARD-586 power pin (V_{CC5}, V_{CC3}) and ground pin to the power circuitry.
When selecting power circuitry, use electric capacity appropriate to the application and make sure instant power supply can be secured. Also, precaution should be take to handle noise problem and reduce high frequency noise or low frequency noise.

12.1.2 Power Cord Cabling

When handling power cord cabling and ground cabling external to CARD-586, try as much as possible to use power plain/ground plain and lower the cabling inductance. If plain connection is really not possible, try to use as thick as possible cabling and pay detailed attention to reducing noise.

12.1.3 Capacitor Inserting

For stable operation of CARD-586, be sure to insert a condenser between the power source and the ground.

Between V_{CC3}-GND	47470µF (Two 47µF parallel connections recommended) Insert near V_{CC3} (Pin No.82,83,200,201). In addition, insertion near V_{CC3} (Pin No.2930147148) also recommended.
Between V_{CC5}-GND	10100µF (47µF recommended)

As the best value varies depending on the system and application in use, be sure to check and select the appropriate values. For condensers, use organic semiconductor aluminum solid electrolyte capacitors, etc. which have low impedance and good temperature characteristics. In addition, installation of condensers with excellent high frequency characteristics at 0.010.47µF at the above mentioned condenser, parallel, and near the pin are recommended.

In particular, if CARD-586/33MHz is used, then be sure to install these condensers.

12.2 Matters to be Noted in Designing of Printed Circuit Board

(1) If the CARD-PC address and data bus have many cablings, and they change simultaneously, the signal's energy will become more and when the cabling coil around and around this may affect other signals. Therefore, it is necessary to usually insert dumping resistance at the address and data bus to smooth off the wave form, or increase the distance from other signals.

(2) For reset, clock and other control line, bus noise may heavily overlap due to cross talk, etc. If there is fear of noise overlapping, the following remedies, for example, can be tried.

1. For signal such as clock whose delay would cause system problem, the guard pattern etc. can be used to reduce influence from other signals, or the distance from other signals can be increased.
2. For signals such as reset signal which has margin in timing, integrated circuit etc. can be used to remove the noise.

(3) Usually, CMOS output buffer has output impedance ranging from several to tens of ohms. However, cables on the printed board has impedance over 100 ohms and so the output buffer and the cable do not match in impedance. As a result, depending on the shape of the board's pattern, influence from reflection, etc. may occur to cause distortion in the wave form. Therefore, it is necessary to check each wave form and, if necessary, add dumping resistance or terminator resistance to correct the problem.

(4) When BIOS data is transferred from CARD-PC's internal flash memory to the shadow area of CARD-PC's internal RAM, the bus will change more vigorously than usual. Therefore, perform BIOS data transfer to the shadow area immediately after the card's power is turned on or at the end of its setup. When checking for existence of bus noise influence, be sure also to check the case when data is transferred from FLASH to RAM.

12.3 Connection of CARD-PC Frame

The CARD-PC frame and CARD-PC signal ground are connected at one spot near the EASI connector inside CARD-PC. Because of the EMC characteristic, it may be better for the frame to be connected to the signal ground at only one spot near the EASI pin, or the frame be connected closest to the mother board's ground; however, it all depends on the system configuration. Therefore, when designing the board, be sure to design it in a way that all of the two methods can be handled, then chose a method after evaluation.

12.4 Accuracy of RTC

Precision of the CARD-PC's RTC falls roughly within ±100ppm (±8.6sec/day). If the system requires more accurate clock function, be sure to connect RTC via external installation.

The precision of RTC is determined by the vibration frequency of the quartz for the RTC. At room temperature, the vibration frequency of the quartz has Tolerance, and the vibration frequency varies according to change in temperature. The frequency Tolerance at room temperature is roughly ±50ppm. The relationship between the temperature and the frequency can be shown in a secondary curve. The frequency is highest when the temperature is around 25°C, then the frequency drops as temperature changes. When the temperature reaches the maximum limit of the operating temperature of CARD-PC (in other words at CARD-PC's internal temperature of 70°C), the frequency is approximately 70 ppm lower than at room temperature. Also, at close to 0°C, the frequency is approximately 20 ppm lower than at room temperature. In conclusion, the RTC's precision is by and large about roughly ±100ppm.

Usually, heat from CARD-PC itself will cause the temperature to rise, and so generally speaking RTC tend to be late. When it is left at room temperature with the power OFF, the Tolerance is smaller than when it is operating.

13. Pin Termination

The following tables indicate characteristics of the pins and how pins are handled when they are not used.

Table 13-1 Name of Tables and Meaning of Symbols

Pin No.	Pin number
Signal Name	Name of pin
Type	Indicates input/output type of the pin while in operation. I : Input O : Output IO : Input/output IO OD : Input/output with output being in open drain OD : Output of open drain
Term	Indicates whether the pin has pull-up/pull-down resistance inside CARD-586, or whether it has the bus hold circuitry. xxKPU : Has xxKΩ of pull-up resistance. xxKPD : Has xxKΩ of pull-down resistance. HOLD : Has bus hold circuitry. The resistance values are only average values. While the pull-up/pull-down resistance in CARD-386 and CARD-486 could be detached when in the suspend mode, they cannot be detached in CARD-586.
Drive	Indicates the pin's drive ability. I_{OL} : Input electric current capable of keeping the Low level I_{OH} : Output electric current capable of keeping the High level
Suspend	Indicates state of the pin when CARD-586 is in the suspend mode. Input : While this brings no influence to CARD-586 operation, input should be confirmed upfront. For pins with pull-up/pull-down resistance or bus hold circuitry inside CARD-586, this will confirm the input. Active : Becomes input. This pin will affect CARD-586 operation. Drive : Drives High or Low. Drive (H) : Drives High. Drive (L) : Drives Low. 3-State : 3-State is OFF. These states assume the standard BIOS of CARD-586 is used.
Handling of Connector When Not Used	Indicates how the pin will be handled when its functions are not used. For pins where input level must be confirmed upfront, handling external to CARD-586 is required. n.c : Regard it as unconnected Pull-up : Be sure to add pull-up resistance.

Table 13-2 VGA Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
3	EXDOTCLK	O	---	24,8	Drive (L)	n.c
4	LD6	O	---	24,8	Drive (L)	n.c
5	LD4	O	---	24,8	Drive (L)	n.c
6	LD2	O	---	24,8	Drive (L)	n.c
7	LD0	O	---	24,8	Drive (L)	n.c
8	FPVTIM	O	---	24,8	Drive (L)	n.c
9	FPAC	O	---	24,8	Drive (L)	n.c
10	FPVCCON	O	---	6,2	Drive (L)	n.c
11	LD9	O	---	24,8	Drive (L)	n.c
12	LD11	O	---	24,8	Drive (L)	n.c
13	LD13	O	---	24,8	Drive (L)	n.c
14	LD15	O	---	24,8	Drive (L)	n.c
15	BLUE	O	150PD	-	0V	n.c
16	GREEN	O	150PD	-	0V	n.c
17	RED	O	150PD	-	0V	n.c
18	VSYNC	O	---	12,4	Drive (L)	n.c
19	LD17	O	---	24,8	Drive (L)	n.c
121	FPDOTCLK	O	---	24,8	Drive (L)	n.c
122	LD7	O	---	24,8	Drive (L)	n.c
123	LD5	O	---	24,8	Drive (L)	n.c
124	LD3	O	---	24,8	Drive (L)	n.c
125	LD1	O	---	24,8	Drive (L)	n.c
126	FPHTIM	O	---	24,8	Drive (L)	n.c
127	LD8	O	---	24,8	Drive (L)	n.c
128	FPVEEON	O	---	6,2	Drive (L)	n.c
129	FPBLANK#	O	---	24,8	Drive (L)	n.c
130	LD10	O	---	24,8	Drive (L)	n.c
131	LD12	O	---	24,8	Drive (L)	n.c
132	LD14	O	---	24,8	Drive (L)	n.c
133	BRTN	--	---	-	-	n.c
134	GRTN	--	---	-	-	n.c
135	RRTN	--	---	-	-	n.c
136	HSYNC	O	---	12,4	Drive (L)	n.c
137	LD16	O	---	24,8	Drive (L)	n.c

Table 13-3 Keyboard and Mouse Interfaces

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
21	MSDATA	IO OD	---	24,-	Input	Pull-up
139	MSCLK	IO OD	---	24,-	Input	Pull-up
22	KBDATA	IO OD	---	24,-	Input	Pull-up
140	KBCLK	IO OD	---	24,-	Input	Pull-up

Table 13-4 Floppy Disk Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
23	FDWP#	I	---	-	Input	Pull-up
24	FDINDEX#	I	---	-	Input	Pull-up
25	FDTRK0#	I	---	-	Input	Pull-up
26	FDWD#	OD	---	38,-	DRV	n.c
31	FDDS2#	OD	---	38,-	DRV	n.c
32	FDMT2#	OD	---	38,-	DRV	n.c
33	FDSIDE	OD	---	38,-	DRV	n.c
34	FDDIR	OD	---	38,-	DRV	n.c
141	FDRD#	I	---	-	Input	Pull-up
142	FDDCHG#	I	---	-	Input	Pull-up
143	FDWE#	OD	---	38,-	DRV	n.c
144	HDHIDEN	OD	---	38,-	DRV	n.c
149	FDDS1#	OD	---	38,-	DRV	n.c
150	FDMT1#	OD	---	38,-	DRV	n.c
151	FDSTEP#	OD	---	38,-	DRV	n.c

Table 13-5 Serial Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
36	COMBDTR#	O	---	8,8	3-State	n.c
37	COMBCTS#	I	50KPU	-	Input	n.c
38	COMBRTS#	O	---	8,8	3-State	n.c
39	COMBDSR#	I	50KPU	-	Input	n.c
154	COMBRI#	I	50KPU	-	Input/ Active	n.c
155	COMBRXD	I	50KPD	-	Input	n.c
156	COMBTXD	O	---	8,8	3-State	n.c
157	COMBDCD#	I	50KPU	-	Input	n.c
40	COMADTR#	O	---	8,8	3-State	n.c
41	COMACTS#	I	50KPU	-	Input	n.c
42	COMARTS#	O	---	8,8	3-State	n.c
43	COMADSR#	I	50KPU	-	Input	n.c
158	COMARI#	I	50KPU	-	Input/ Active	n.c
159	COMARXD	I	50KPD	-	Input	n.c
160	COMATXD	O	---	8,8	3-State	n.c
161	COMADCD#	I	50KPU	-	Input	n.c
162	IRTXD	O	---	24,12	3-State	n.c
44	IRRXD	I	50KPU	-	Input	n.c
153	DARXD	I	50KPU	-	Input	n.c

- When resume by modem link is enabled, COMARI# or COMBRI# will become active and so CARD-586 will be resumed.

Table 13-6 Parallel Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
45	LPTSTROBE#	IO OD	4.7KPU	12,-	Input	n.c
46	LPTD0	IO	50KPD	8,8	Input/ Drive	n.c
47	LPTACK#	I	60KPU	-	Input	n.c
48	LPTPE	I	20KPD	-	Input	n.c
49	LPTD1	IO	50KPD	8,8	Input/ Drive	n.c
50	LPTD2	IO	50KPD	8,8	Input/ Drive	n.c
51	LPTD3	IO	50KPD	8,8	Input/ Drive	n.c
52	LPTD5	IO	50KPD	8,8	Input/ Drive	n.c
53	LPTD7	IO	50KPD	8,8	Input/ Drive	n.c
163	LPTAFD#	IO OD	4.7KPU	12,-	Input	n.c
164	LPTERROR#	I	60KPU	-	Input	n.c
165	LPTBUSY	I	20KPU	-	Input	n.c
166	LPTSLCT	I	20KPD	-	Input	n.c
167	LPTINIT#	IO OD	4.7KPU	12,-	Input	n.c
168	LPTSLCTIN#	IO OD	4.7KPU	12,-	Input	n.c
169	LPTD4	IO	50KPD	8,8	Input/ Drive	n.c
170	LPTD6	IO	50KPD	8,8	Input/ Drive	n.c
171	LPTDIR	O	---	8,8	Drive	n.c

Table 13-7 HDD Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
54	HDDIR	O	---	8,8	Drive (L)	n.c
55	HDENL#	O	---	8,8	Drive (H)	n.c
56	HDCS0#	O	---	12,12	High-Z	n.c
172	HD7	IO	50KPU	12,12	Input	n.c
173	HDENH#	O	---	8,8	Drive (H)	n.c
174	HDCS1#	O	---	12,12	High-Z	n.c

Table 13-8 ISA Bus Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
67	SD7	IO	50KPU	12,12	Input	n.c
68	SD6	IO	50KPU	12,12	Input	n.c
69	SD5	IO	50KPU	12,12	Input	n.c
70	SD4	IO	50KPU	12,12	Input	n.c
71	SD3	IO	50KPU	12,12	Input	n.c
72	SD2	IO	50KPU	12,12	Input	n.c
73	SD1	IO	50KPU	12,12	Input	n.c
74	SD0	IO	50KPU	12,12	Input	n.c
75	IOCHRDY	IO OD	1KPU	12,-	Input	n.c
76	AEN	O	---	12,12	Drive (L)	n.c
77	SA19	O	HOLD	12,12	Drive	n.c
78	SA18	O	HOLD	12,12	Drive	n.c
79	SA17	O	HOLD	12,12	Drive	n.c
80	SA16	IO	HOLD	12,12	Drive	n.c
81	SA15	IO	HOLD	12,12	Drive	n.c
86	SA14	IO	HOLD	12,12	Drive	n.c
87	SA13	IO	HOLD	12,12	Drive	n.c
88	SA12	IO	HOLD	12,12	Drive	n.c
89	SA11	IO	HOLD	12,12	Drive	n.c
90	SA10	IO	HOLD	12,12	Drive	n.c
91	SA9	IO	HOLD	12,12	Drive	n.c
92	SA8	IO	HOLD	12,12	Drive	n.c
93	SA7	IO	HOLD	12,12	Drive	n.c
94	SA6	IO	HOLD	12,12	Drive	n.c
95	SA5	IO	HOLD	12,12	Drive	n.c
96	SA4	IO	HOLD	12,12	Drive	n.c
97	SA3	IO	HOLD	12,12	Drive	n.c
98	SA2	IO	HOLD	12,12	Drive	n.c
99	SA1	IO	HOLD	12,12	Drive	n.c
100	SA0	IO	HOLD	12,12	Drive	n.c
101	SBHE#	IO	HOLD	12,12	Drive	n.c
102	LA23	IO	HOLD	12,12	Drive	n.c
103	LA22	IO	HOLD	12,12	Drive	n.c
104	LA21	IO	HOLD	12,12	Drive	n.c
105	LA20	IO	HOLD	12,12	Drive	n.c
106	LA19	IO	HOLD	12,12	Drive	n.c
107	LA18	IO	HOLD	12,12	Drive	n.c
108	LA17	IO	HOLD	12,12	Drive	n.c
109	MEMR#	IO	50KPU	12,12	Drive (H)	n.c

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
110	MEMW#	IO	50KPU	12,12	Drive (H)	n.c
111	SD8	IO	50KPU	12,12	Input	n.c
112	SD9	IO	50KPU	12,12	Input	n.c
113	SD10	IO	50KPU	12,12	Input	n.c
114	SD11	IO	50KPU	12,12	Input	n.c
185	RESETDRV	O	---	12,12	Drive (L)	n.c
186	IOCHCK#	I	4.7KPU	-	Input	n.c
187	IRQ9	I	50KPU	-	Input	n.c
188	DRQ2	IO	50KPD	12,2	Input/ Drive	n.c
189	WS0#	I	1KPU	-	Input	n.c
190	SMEMW#	O	---	12,12	Drive (H)	n.c
191	SMEMR#	O	---	12,12	Drive (H)	n.c
192	IOW#	IO	50KPU	12,12	Drive (H)	n.c
193	IOR#	IO	50KPU	12,12,	Drive (H)	n.c
194	DACK3#	O	---	8,8	Drive (H)	n.c
195	DRQ3	I	50KPD	-	Input	n.c
196	DACK1#	O	---	8,8	Drive (H)	n.c
197	DRQ1	I	50KPD	-	Input	n.c
198	REF#	IO OD	1.2KPU	12,-	3-State	n.c
199	SCLK	O	---	12,12,	Drive (L)	n.c
204	IRQ7	IO	50KPU	8,8	Input/ Drive	n.c
205	IRQ6	IO	50KPU	12,2	Input/ Drive	n.c
206	IRQ5	IO	50KPU	8,8	Input/ Drive	n.c
207	IRQ4	IO	50KPU	8,8	Input/ Drive	n.c
208	IRQ3	IO	50KPU	8,8	Input/ Drive	n.c
209	DACK2#	O	---	8,8	Drive (H)	n.c
210	TC	O	---	12,12	Drive (L)	n.c
211	BALE	O	---	12,12	Drive (L)	n.c
212	OSC	O	---	8,8	Drive	n.c
213	MEMCS16#	I	1KPU	-	Input	n.c
214	IOCS16#	I	1KPU	-	Input	n.c
215	IRQ10	IO	50KPU	8,8	Input/ Drive	n.c
216	IRQ11	IO	50KPU	8,8	Input/ Drive	n.c
217	IRQ12	IO	50KPU	8,8	Input/ Drive	n.c
218	IRQ15	I	50KPU	-	Input	n.c

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
219	IRQ14	I	50KPU	-	Input	n.c
220	DACK0#	O	---	8,8	Drive (H)	n.c
221	DRQ0	I	50KPD	-	Input	n.c
222	DACK5#	O	---	8,8	Drive (H)	n.c
223	DRQ5	I	50KPD	-	Input	n.c
224	DACK6#	O	---	8,8	Drive (H)	n.c
225	DRQ6	I	50KPD	-	Input	n.c
226	DACK7#	O	---	8,8	Drive (H)	n.c
227	DRQ7	I	50KPD	-	Input	n.c
228	MASTER#	I	1KPU	-	Input	n.c
229	SD12	IO	50KPU	12,12	Input	n.c
230	SD13	IO	50KPU	12,12	Input	n.c
231	SD14	IO	50KPU	12,12	Input	n.c
232	SD15	IO	50KPU	12,12	Input	n.c

Table 13-9 Power Management

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
57	SUSSTAT#	O	---	8,8	Drive (L)	n.c
58	BATLOW#	I	50KPU	---	Active	n.c
61	BATWRN#	I	50KPU	---	Input	n.c
176	EXTSMI#	I	50KPU	---	Input	n.c
180	SRBTN#	I	50KPU	---	Active	n.c
115	SMOUT3	O	---	8,8	Drive (H)	n.c
116	SMOUT1	O	---	8,8	Drive (L)	n.c
233	SMOUT2	O	---	8,8	Drive (L)	n.c
234	SMOUT0	O	---	8,8	Drive (L)	n.c

- When BATLOW# becomes active, CARD-586 cannot be resumed.

Table 13-10 Others

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Handling of Connector When Not Used
62	POWERGOOD	I	---	---	Active	Must be used.
63	SPKOUT	O	---	4,4	Drive (L)	n.c
181	WDTIM#	O	---	4,4	Drive	n.c
64	FLOAT#	I	25KPU	-	Active	n.c
65	ROMCE0#	IO	---	4,4	Drive (H)	n.c
175	V_{BK}	---	---	---	---	See explanation below
182	PGM	---	---	---	---	See explanation below

- FLOAT# and ROMCE0# are pins required when the ROM writer is used to update flash ROM contents of CARD-586. For normal use regard them as not connected.
- When POWERGOOD becomes inactive, CARD-586 will be reset.
- V_{BK} pin cannot be regarded as unused. If the backup circuitry is not required, be sure to connect V_{CC5}.
- With regard to the PGM pin, be sure to check its level when it is unused. (Refer to the hardware manual for more information.)

- RESERVE connectors (20, 35, 66, 138, 152, 179, 183, 184,)

RESERVE pins are reserved for use for other functions in the future; therefore, be sure to regard all of them as unconnected.

14. Mounting and Fixture

14.1 Mounting Procedure

Figure 14-1 indicates the dimensional diagram when the receiving connector is installed. Figure 14-2 indicates the board holes diagram. Figure 14-3 indicates the pin number diagram.

- Connectors on card receiving side
  - Regarding the board for installation of the connectors on the receiving end, be sure to limit the thickness of the board to within 1.6mm.
  - Use screws to secure the connectors on the receiving end.
    (Use M2.5×8 hexagonal nut screws.)
  - When CARD-586 is installed, it becomes higher than the height of the connector. Therefore, make sure to have 9mm or more of clearance (height when actually installed).

- Fall-off prevention

  CARD-586 may fall off from the connector as a result of vibration or shock. To prevent this problem to happen, SEK6676P01 is recommended. SEK6676P01 is a card stopper with good heat radiation effect and the ability to prevent CARD-586 from detaching from the pins. Use the screws which are used to secure the connectors to tighten the card stopper. To install the card stopper, change the screw for securing the connector to M 2.5×14 and first secure the connector. Then install the "]" shape rubber (which comes with the card stopper) to the two locations on CARD-586. From its top, while pressing CARD-586 along the direction of the connector by using the card stopper, tighten the nuts.

  The M1.2 screws (3 pieces) which come with the card stopper are for inserting into the female screw locations on the card stopper. The prevention purpose can be achieved even if these screws are not used. However, use of the screws give added prevention effect. If these screws are to be used, be sure to tighten the screws until resistance is felt.

Please see the figure below if the stopper is to be used. Please take the distance from CARD-586 to the stopper position (A) as 0.5±0.2mm.

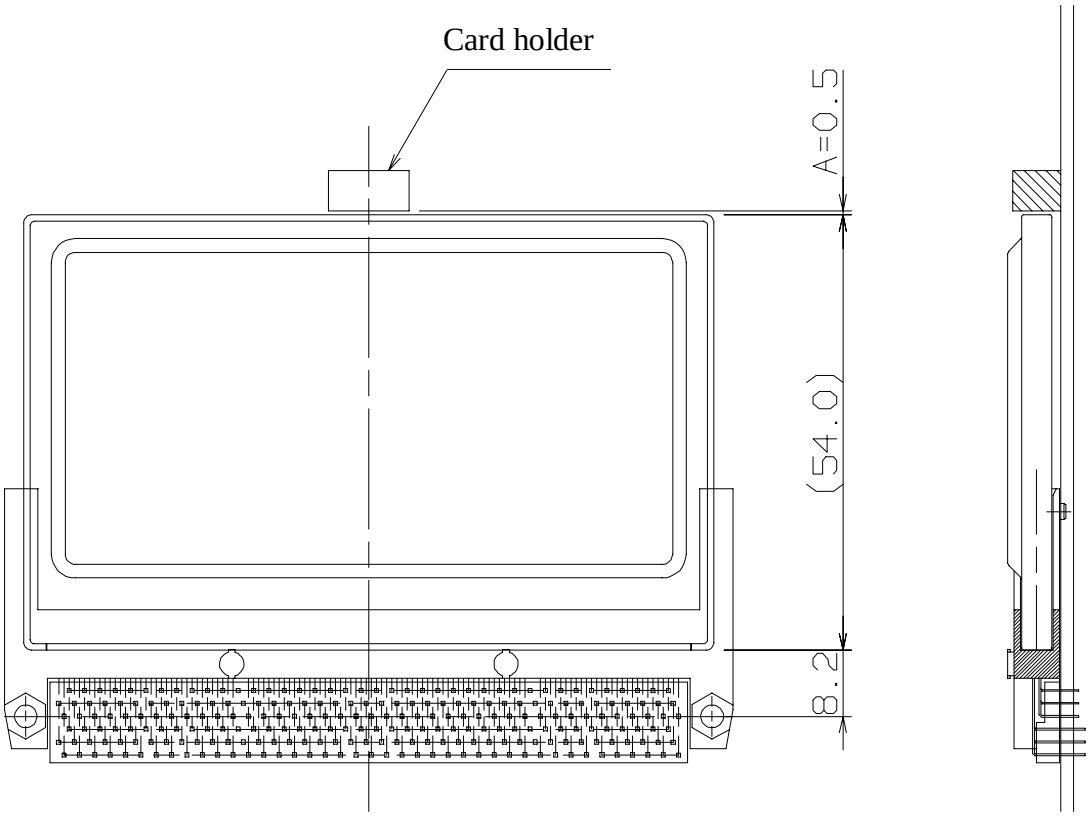


Figure 14-1 Dimension for Card Holder

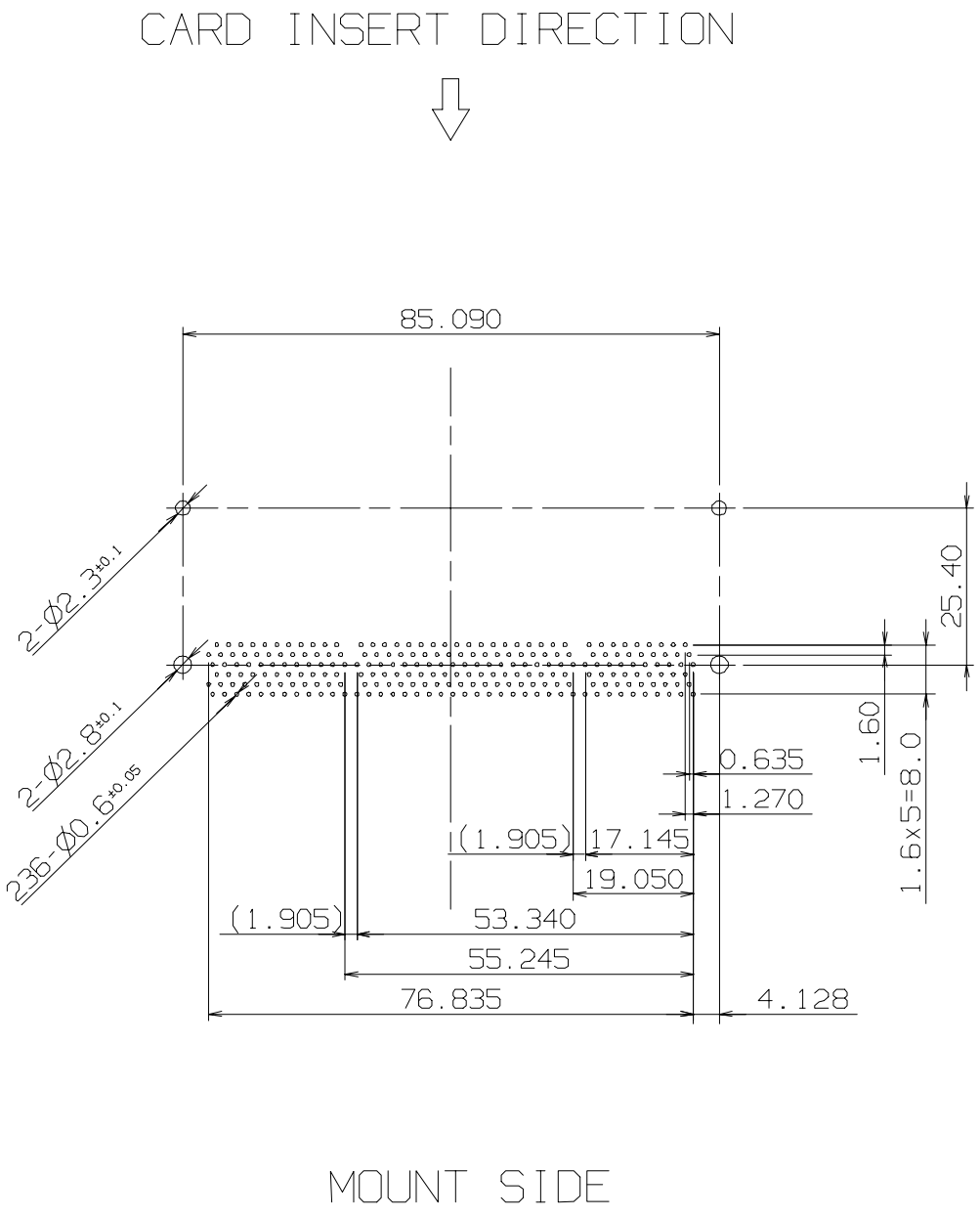


Figure 14-2 Dimension for Board Holes

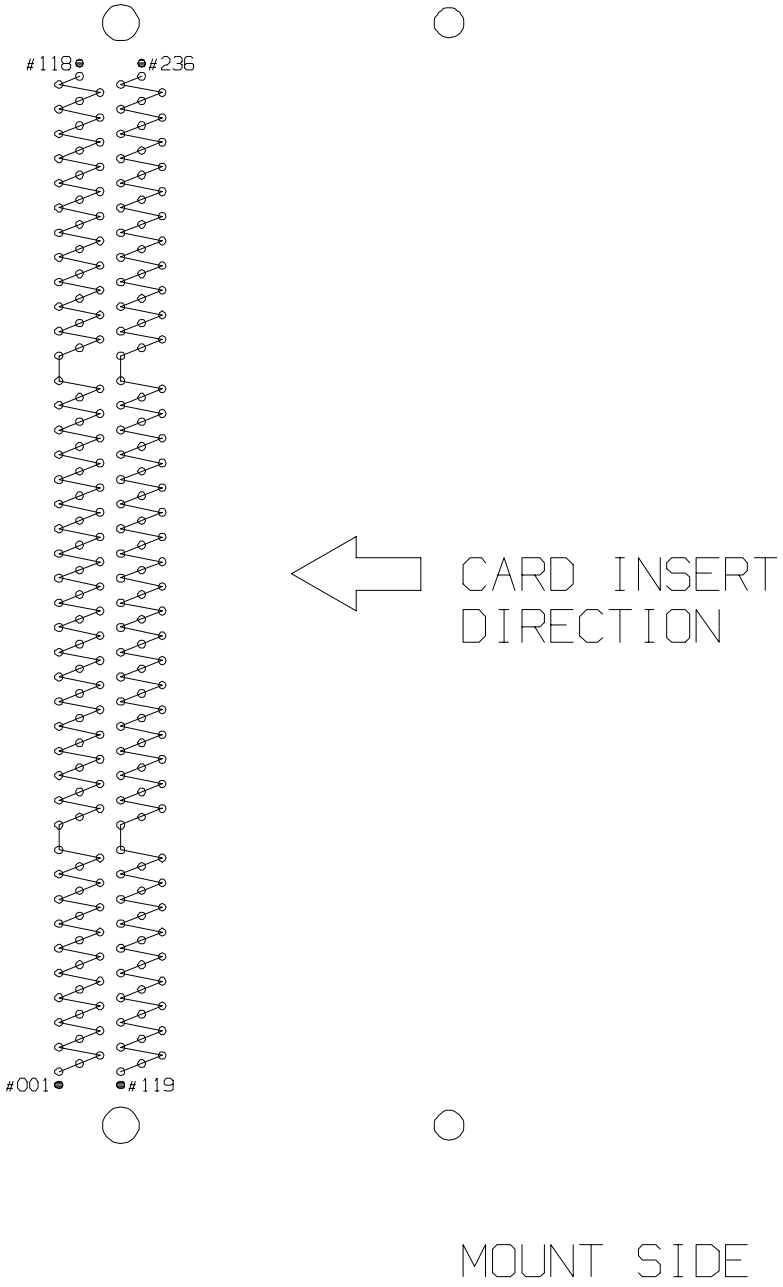


Figure 14-3 Pin Number

14.2 Card Socket and Card Stopper

Two types of pins are available, one with the ejector and the other one without the ejector.

Table 14-1 Connectors/Card Stopper List

Model Number	Specification
SEK6669P01	236PIN with no ejector
SEK6669P02	236PIN with ejector Note 1
SEK6675P01	Card stopper Note 2
SEK6676P01	Card stopper for heat radiation Note 3
SEK6677P01 SEK6678P01	Stand off pin Note 4

(Note 1) For SEK6669P02, due to card height limit, CARD-586 cannot be used.

(Note 2) For SEK6675P01, due to stopper shape and heat radiation capability, CARD-586 cannot be used.

(Note 3) SEK6676P01 has increased heat radiation capability designed for use with CARD-586.

(Note 4) It can also be used with CARD-486HB.

(Note 5) The stand-off connector consists of two pieces: SEK6677P01 connects to the board and SEK6678P01 is used to maintain CARD-PC. At present, the heat radiation stopper for use together with the stand-off connector is not included. Should this need arise, please contact us for assistance.

14.3 Cautions on Mounting CARD-586

CARD-586 emits heat when it is operating and can become very hot. It may affect its surrounding devices or it may be affected by the surrounding devices. Therefore, please bear in mind this issue when doing the design work.
The temperature specification of CARD-586 while it is operating is below 70°C at the case surface. The spot for temperature measurement is indicated in figure 14.-4.
When using the card stopper (SEK6676P01), take consideration of its surrounding components. Figure 14-6 indicates the horizontal dimensions with the card stopper installed.

(Unit: mm)

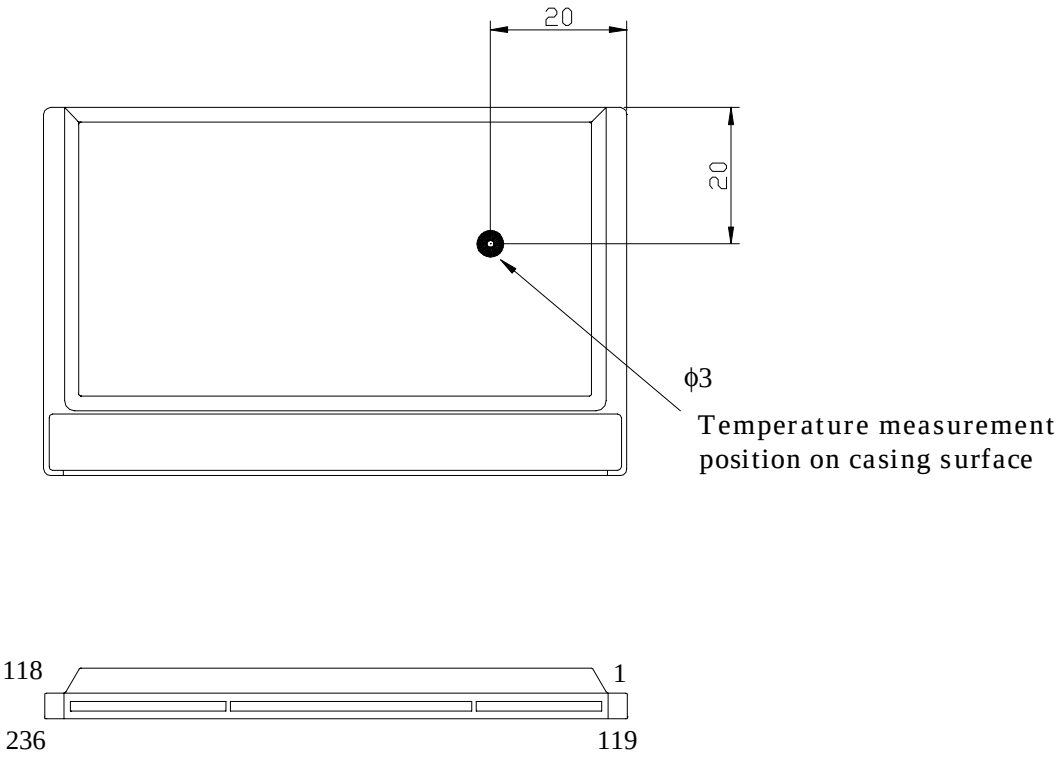


Figure 14-4 Position on Case Surface for Temperature Measurement

(Unit mm)

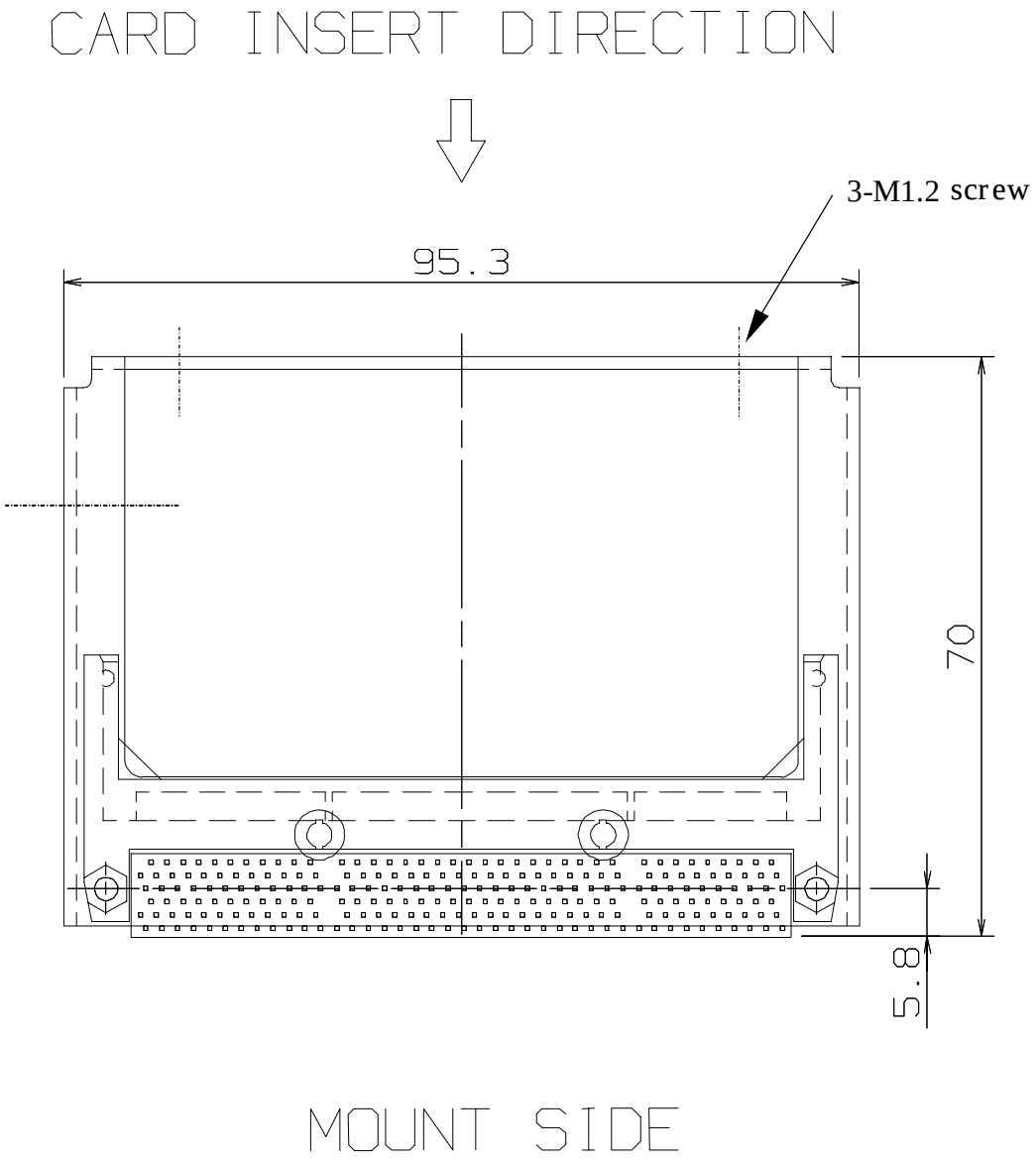


Figure 14-5 Horizontal Dimension When Card Stopper (SEK6676P01) is Mounted

Appendix 1. Temperature Measurement Sample Data

1.1 Measurement System Configurations

Board	SEK0630B$_{0C}$
HDD	Viper 170 (Integral)
FDD	No
Monitor	MF-5015A (Iiyama Denki
Key board	RT6672T JP (NMB TECHNOROGY INC.)
Case	PAC-100 (ACQUIRE)
Recorder	MODEL 3081 (YOKOGAWA)
Operating State	DOS prompt display
Supply Voltage	+5.00V
	+12.0V
	+3.30V±2% (featured with internal 3-terminal regulator)

1.2 Measurement Conditions

The ambient temperature (Ta) and CARD-586's surface temperature (Tc) are measured under the following conditions:

- Casing is completely shielded from external environment.
- No fan is used to stir up the air inside the casing. (Used in natural state)
  Place CARDPRESSO vertically inside the 230mm × 400mm ×175mm casing.
  Add heat radiation stopper to CARD-586.
- Install CARD-586 to CARDPRESSO, then measure the ambient temperature (Ta) at the surface temperature measurement point as well as at a location 20 mm from the point.

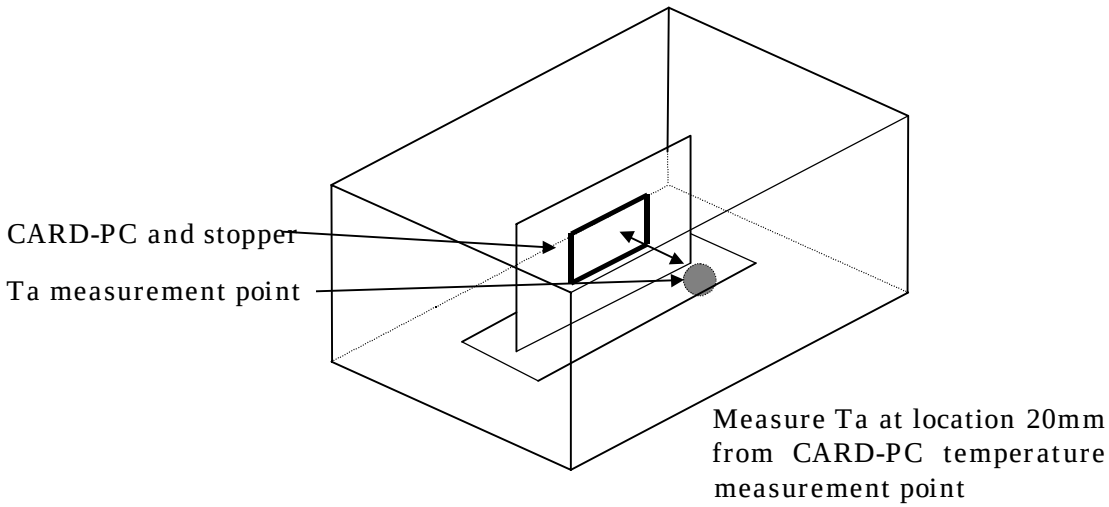
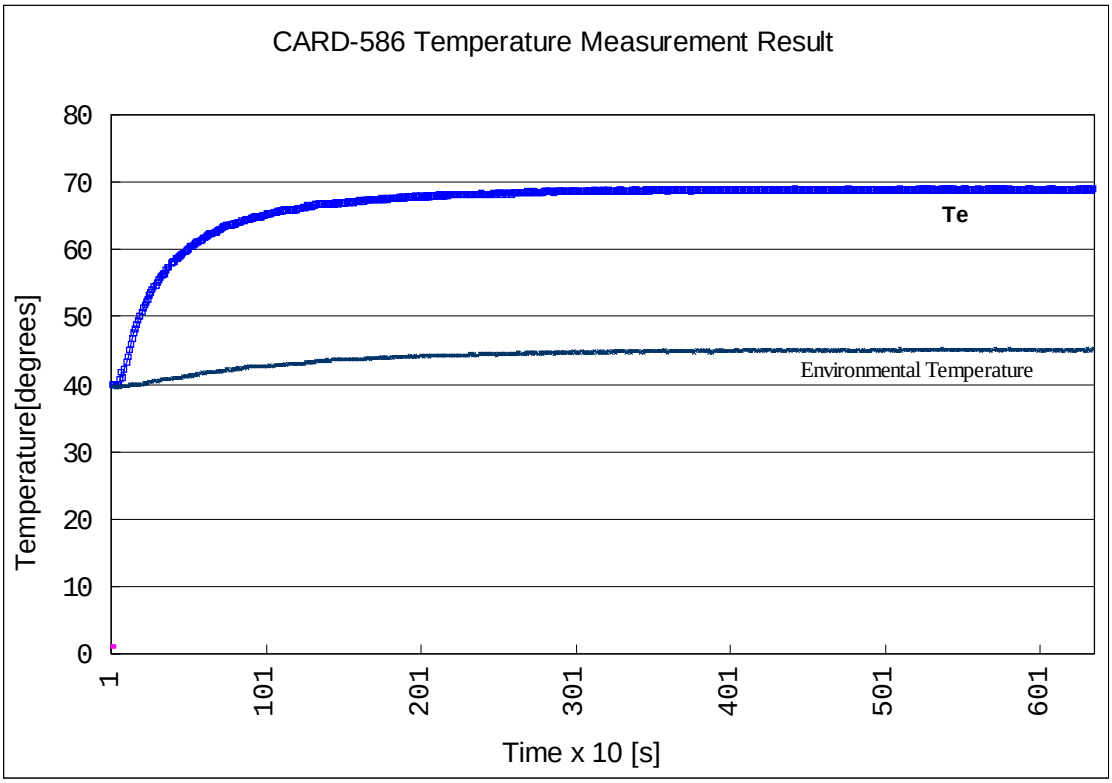


Figure Appendix 1-1 CARD-586 Surface Temperature Measurement Data

1.3 Measurement Results

The following graph indicates the surface temperature measurement data of CARD-586.



Graph Appendix 1-1 CARD-586 Surface Temperature Measurement Data

Table Appendix 1-1 Temperature Data at Balanced State

	Ta	Tcase	T
CARD-586 (32MB)	45.0°C	68.8°C	23.8°C

Because the electric current consumption does not depend on the DRAM size, the above measurement data can be used independent of the size of the memory. However, use the data as a reference only.

1.4 Cautions

This measured values are only a reference values. When designing the system, be sure to measure the temperatures of CARD-586 and other devices inside the system during actual operation, and make sure they meet the operating temperature specifications.

Appendix 2. Controls for Different LCD Types

In this manual, LCDs are classified according to the general display methods. The following briefly describes the control method for each type of LCD. For connection information on using LCD with CARD-586, please refer to the separate document "CARD-PC Technical Information." Because this information is constantly updated, please contact us for the latest information

2.1 STN LCDs

Depending on the maker, LCDs which have picture quality improved on STN are also available, by the names NTN, FTN, and DSTN. However, their interfaces are identical to STN. They are all referred to as STN for discussion to follow below.

STN LCD display can be monochrome or color. Many color STNs are monochrome STN with added RGB color filter. For VGA display, color STNs have three times of the number of pixels than the monochrome STNs.

8-bit monochrome STNs send pixels equivalent to the data width in one clock. That means 8 pixels of data of a LCD can be sent in one clock. On the other hand, an 8-bit color STN can send only 8/3 pixels of data of a LCD (RGBRGB totaling 8 bits) in one clock. Because of this reason, their data arrays are not compatible and so signal output for color STN cannot be display correctly on monochrome STN, or signal output for monochrome STN cannot be displayed correctly on color LCD.

By theory, STN LCD operation requires positive or negative driving power. While LCDs with small number of pixels (such as calculator display LCD) can operate at 5V or 12V of driving power, STN LCDs for PC generally require from +20V to 40V or from -15V to -35V of driving power. Also, many LCDs require a certain sequence of ON/OFF between the driving power and the logic signal. For this reason, a separate power ON/OFF control circuitry must be prepared.

In addition, depending on the data width that can be used for each transfer, STNs also classified according to the number. Here, the bit number as used in data transfer width is different from the bit number as used in color TFT.

2.1.1STN Single Scan LCDs

On this type of LCDs, display data with size of the data bus width is sent line by line from left to right. Data width can be 4 or 8 bits, but in general data on the left side of the screen seems to be standardized with the MSB of the data bus. (See table appendix 2-1.)

Table Appendix 2-1

Relationship between 8-bit Single Scan STN Data and Screen, Using VGA as Example

→		← 8 bits per each width (data bus width)					
1.1	1.2	1.3	1.4	1.5	----------	1.79	1.80
2.1	2.2	2.3	2.4	2.5	----------	2.79	2.80
3.1	3.2	3.3	3.4	3.5	----------	3.79	3.80
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
479.1	479.2	479.3	479.4	479.5	----------	479.79	479.80
480.1	480.2	480.3	480.4	480.5	----------	480.79	480.80

Data transfer sequence is 1.1/1.2/1.3/.../1.79/1.80/2.1/2.2/.../480.79/480.80

The clock (referred to as dot clock hereafter) required for data transfer must be input externally. FPDOTCLK of CARD-586 serves this purpose. Also, the synchronous signal FPVTIM on the upper end of the screen as well as the synchronous signal FPHTIM on the left end of the screen are required, therefore there are 3 input signals in addition to the data.

2.1.2 STN Dual-Scan Monochrome LCDs

In this type of LCDs, the screen is split into the two areas, upper and lower areas, with display data for each area sent by each line. The data bus width can be 4 bits × 2 or 8 bits × 2. The data composition is same as the STN single scan, apparently with MSB standardized on the left and LSB on the right in general. (See table appendix 2-2.)

Table Appendix 2-2
Relationship Between 4-bit × 2 Dual-Scan STN Data and Screen, Using VGA as Example

→		← 4 bits per each width (data bus width)				
U1.1	U1.2	U1.3	U1.4	----------	U1.159	U1.160
U2.1	U2.2	U2.3	U2.4	----------	U2.159	U2.160
⋮	⋮	⋮	⋮	⋮	⋮	⋮
U239.1	U239.2	U239.3	U239.3	----------	U239.159	U239.160
U240.1	U240.2	U240.3	U240.3	----------	U240.159	U240.160
L1.1	L1.2	L1.3	L1.4	----------	L1.159	L1.160
L2.1	L2.2	L2.3	L2.4	----------	L2.159	L2.160
⋮	⋮	⋮	⋮	⋮	⋮	⋮
L239.1	L239.2	L239.3	L239.4	----------	L239.159	L239.160
L240.1	L240.2	L240.3	L240.4	----------	L240.159	L240.160

Data consists of the following sets of data which are sent simultaneously.

Data for upper area of screen: U1.1/U1.2/.../U1.159/U1.160/U2.1/U2.2/.../U240.159/U240.160
Data for lower area of screen: L1.1/L1.2/.../L1.159/L1.160/L2.1/L2.2/.../L240.159/L240.160

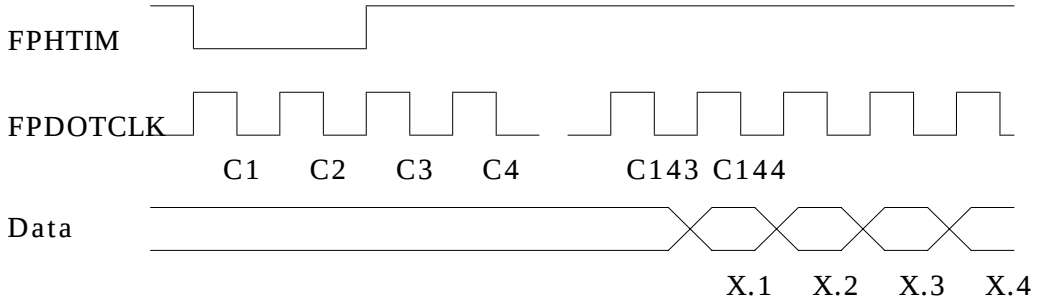
Depending on the LCD, input of signal for start position of lower area of screen display may be required, and clocks with different timing for the upper and lower areas may also be required. Except for this type of special products, most dual scan STNs are same as single scan STNs. This means the three signals, namely dot clock (FPDOTCLK), synchronous signal indicating the upper end of screen (FPVTIM), and synchronous signal indicating the left end of screen (FPHTIM), are required in addition to the data signal.

2.2 TFT LCDs

2.2.1TFT having a timing of screen display data by counting FPDOTCLKs

CARD-586 does not support this type of TFTs.
They generally fall into two groups: one that displays screen data using the FPHTIM shutdown to 144 FPDOTCLK timing (described as C144 type in this manual), and the other one using the FPHTIM startup to 104 FPDOTCLK timing (described as C104 type in this manual).

AC timing of C144 type of TFT



AC timing of C104 type of TFT

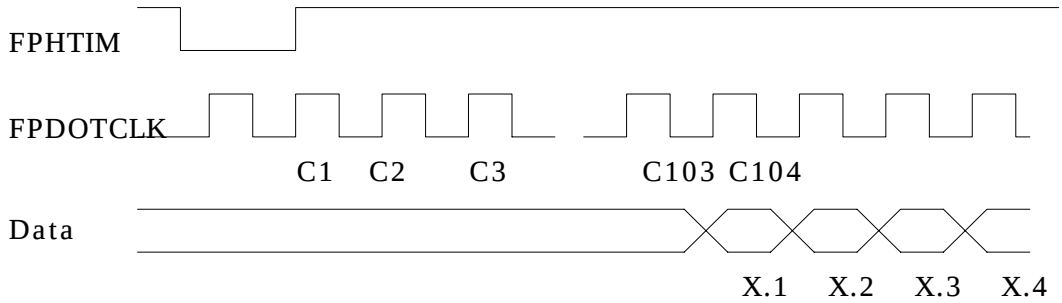


Figure Appendix 2-1 TFT AC Timing

2.2.2TFT using sync signals in the timing of screen display data

This type of TFTs use synchronous signal (DE) input externally to determine the screen display data timing (described as DE type in this manual). Depending on the model, some may use the synchronous signal to determine the display position in both the upper and lower areas on the screen. Display may be possible with parameter change on CARD-586. For details, please refer to "CARD-PC Technical Information."

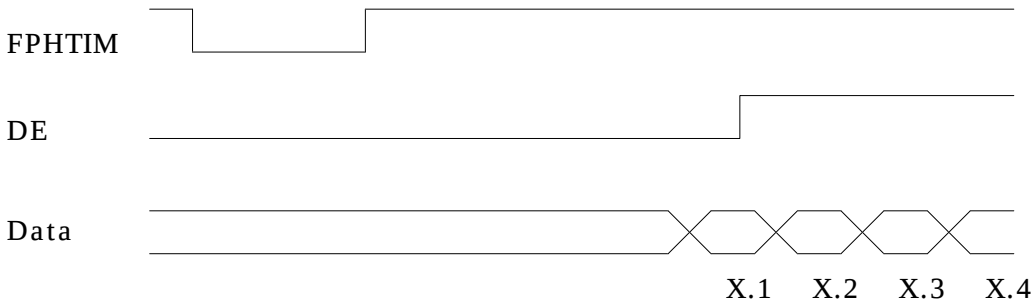


Figure Appendix 2-2 DE-type TFT AC Timing

2.2.3TFT supporting the selection of the above two functions

This type of LCDs use a setup pin to select whether the display position should be fixed to an internal value or should use external synchronous signal. At present, this type is widely available. CARD-586 provides external synchronous signal.

Also, depending on the number of data signal, TFTs may allow maximum number of color pixels of 512 colors (3 bits each), 4096 colors (4 bits per color), and 260,000 colors (6 bits per color). CARD-586 can connect to all of these color TFTs.

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