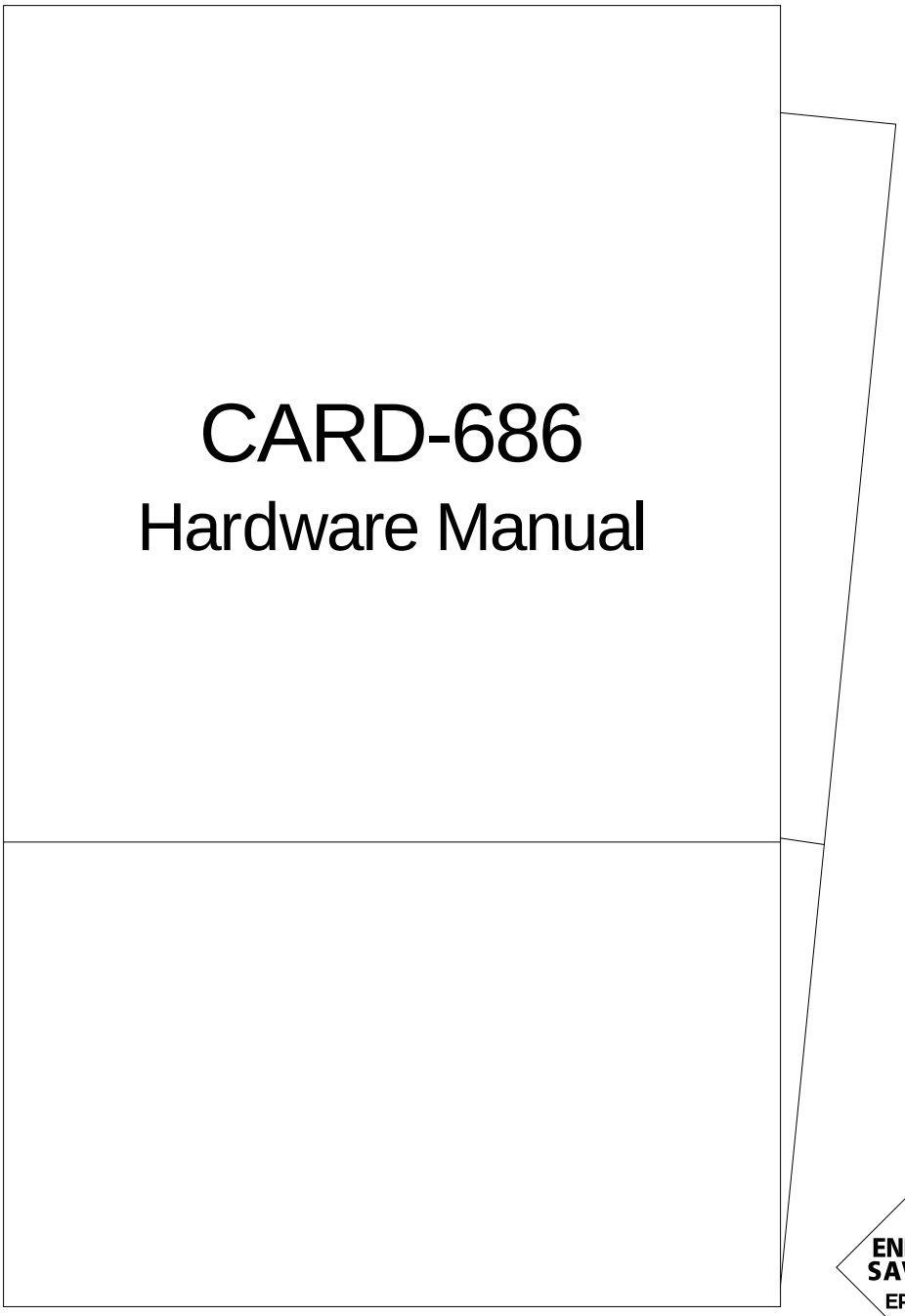
MF1162-04

EPSON

CARD-686

Hardware Manual



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Contents

1.1 BASIC SPECIFICATIONS

SCE86638 Series (CARD-686) consolidates the main board blocks of the ISA architecture into a credit card sized card. The configuration is described below.

CPU

AMD-K6-2 (manufactured by AMD Corp.)

I/O block

ISP0016 (manufactured by Seiko Epson Corp.)
SPC8221 (manufactured by Seiko Epson Corp.)
- Interrupt controllers (82C59A equivalent. ×2)
- Programmable timers (82C54 equivalent. ×2)
- DMA controllers (82C37A A equivalent. ×2)
- Memory mapper (74LS612 equivalent.)
- Parallel I/O port
- Serial I/O ports (16C550 equivalent. ×2)
- Real-time clock (146818 equivalent.)
- IDE interface
  - Support for large-capacity IDE HDD (8.4 GB)

Memory block

- DRAM 32 or 64 MB
- Flash ROM (for BIOS) 256 KB

Keyboard Interface block

8042 Software emulation
- PS/2 Style Keyboard
- PS/2 Style Mouse

Video block

SPC8110 (manufactured by Seiko Epson Corp.)
- CRT
- STN mono/color (single/dual panel)
- TFT color
- VRAM 1 MB

FDC block

SPC2052 (manufactured by Seiko Epson Corp.)
- Equivalent to µPD765.
- Drive : Support two units.
- Transfer rate : 250Kbps, 300Kbps, 500 Kbps

CARD-686 Model List

Model No	CPU Clock	DRAM
SCE8663802	233 MHz	32 MB
SCE8663803	233 MHz	64 MB

CAUTION

1) The surface of the CARD-686 becomes very hot during and immediately after use. To prevent accidental burns, avoid touching it.

   Observe the following precautions
   - Warn service personnel and other people who might come in contact with the CARD-686 that the card becomes hot.
   - If appropriate, after installing the CARD-686, attach a label to it warning that it is hot.
   - If appropriate, place a cover over the CARD-686 to prevent people from coming in contact with it accidentally.

2) Due to structural constraints, the CARD-686 emits more radiation noise that the CARD-586. Accordingly, appropriate measures must be taken to counter EMI in the customer's system.

3) Due to structural constraints of the CARD-686, measures must be implemented to counter static electrical noise in the customer's system.

4) Never touch the CARD-686's terminal contacts with your hands or metallic objects.

5) Never bend or drop the CARD-686 or subject it to mechanical shock.

6) Avoid exposure to heat, moisture, and direct sunlight.

7) Never insert or remove the CARD-686 while the power is on.

8) Unauthorized reproduction or modification of the BIOS is prohibited.

9) When designing products that incorporate the CARD-686, please refer to the application notes.

1.2 Block Diagram

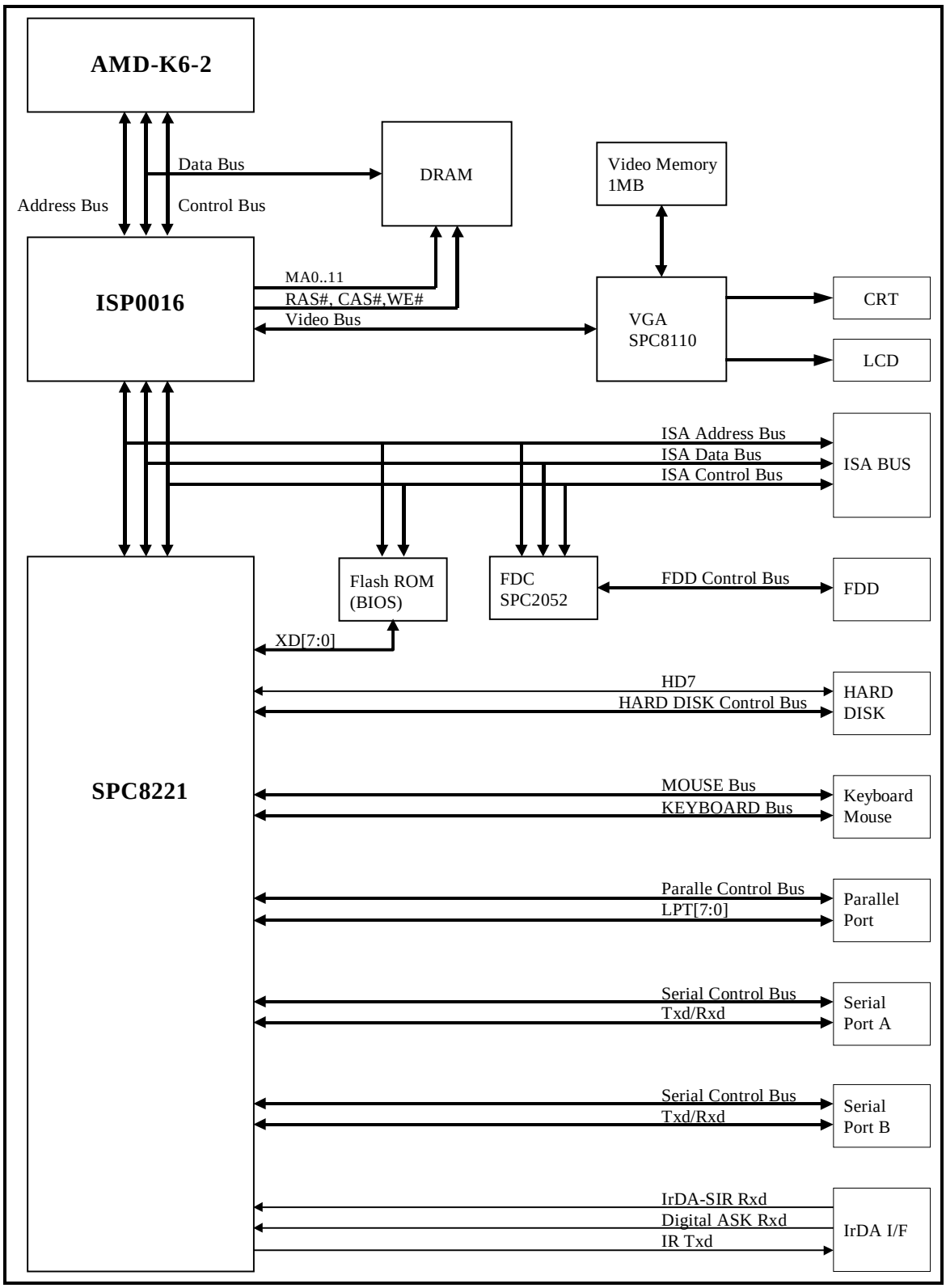

Figure 1-1 CARD-686 Block Diagram

2. PHISYCAL SPECIFICATIONS

2.1 Dimensions

85.4mm × 54.0mm × 16.75mm

2.2 Weight

91(g)

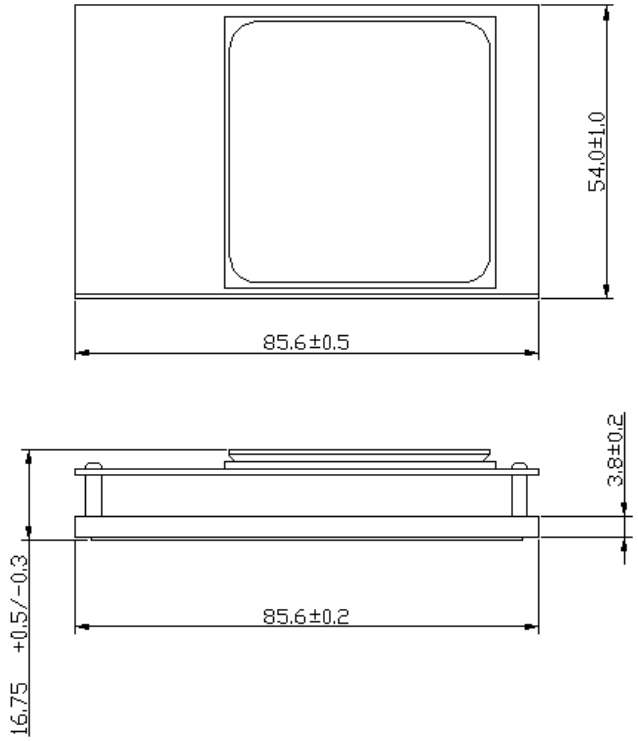

Figure 2-1 CARD-686 Dimensions

2.3 Installation Method

The card socket side connector SEK6669P$_{01}$ (without ejector) can be used.

Note: SEK6669P$_{02}$ (with ejector) cannot be used.

- Thickness of board to which socket side connector is fitted should not exceed 1.6mm.
- Socket side connector fixing should be done with screws.
  (Screws M2.5 × 8 hexagonal nuts)

3. PIN CONFIGURATION

CARD-686 Pin Configuration

1	GND	119	GND
2	GND	120	GND
3	EXDOTCLK	121	FPDOTCLK
4	LD6	122	LD7
5	LD4	123	LD5
6	LD2	124	LD3
7	LD0	125	LD1
8	FPVTIM	126	FPHTIM
9	FPAC	127	LD8
10	FPVCCON	128	FPVEEON
11	LD9	129	FPBLANK#
12	LD11	130	LD10
13	LD13	131	LD12
14	LD15	132	LD14
15	BLUE	133	BRTN
16	GREEN	134	GRTN
17	RED	135	RRTN
18	VSYNC	136	HSYNC
19	LD17	137	LD16
20	RESERVE	138	RESERVE
21	MSDATA	139	MSCLK
22	KBDATA	140	KBCLK
23	FDWP#	141	FDRD#
24	FDINDEX#	142	FDDCHG#
25	FDTRK0#	143	FDWE#
26	FDWD#	144	FDHIDEN
27	VCC5	145	VCC5
28	VCC5	146	VCC5
29	VCC3	147	VCC3
30	VCC3	148	VCC3
31	FDDS2#	149	FDDS1#
32	FDMT2#	150	FDMT1#
33	FDSIDE	151	FDSTEP#
34	FDDIR	152	RESERVE
35	RESERVE	153	DARX
36	COMBDTR#	154	COMBRI#
37	COMBCTS#	155	COMBRXD
38	COMBRTS#	156	COMBTXD
39	COMBDSR#	157	COMBDCD#
40	COMADTR#	158	COMARI#

41	COMACTS#	159	COMARXD
42	COMARTS#	160	COMATXD
43	COMADSR#	161	COMADCD#
44	IRRX	162	IRTX
45	LPTSTROBE#	163	LPTAFD#
46	LPTD0	164	LPTERROR#
47	LPTACK#	165	LPTBUSY
48	LPTPE	166	LPTSLCT
49	LPTD1	167	LPTINIT#
50	LPTD2	168	LPTSLCTIN#
51	LPTD3	169	LPTD4
52	LPTD5	170	LPTD6
53	LPTD7	171	LPTDIR
54	HDIR	172	HD7
55	HDENL#	173	HDENH#
56	HDCS0#	174	HDCS1#
57	SUSSTAT#	175	VBK
58	BATLOW#	176	EXTSMI#
59	GND	177	GND
60	GND	178	GND
61	BATWRN#	179	RESERVE
62	POWERGOOD	180	SRBTN#
63	SPKOUT	181	WDTIM#
64	FLOAT#	182	PGM
65	ROMCE0#	183	RESERVE
66	RESERVE	184	RESERVE
67	SD7	185	RESETDRV
68	SD6	186	IOCHCK#
69	SD5	187	IRQ9
70	SD4	188	DRQ2
71	SD3	189	WS0#
72	SD2	190	SMEMW#
73	SD1	191	SMEMR#
74	SD0	192	IOW#
75	IOCHRDY	193	IOR#
76	AEN	194	DACK3#
77	SA19	195	DRQ3
78	SA18	196	DACK1#
79	SA17	197	DRQ1
80	SA16	198	REF#

81	SA15	199	SCLK
82	VCC3	200	VCC3
83	VCC3	201	VCC3
84	VCC5	202	VCC5
85	VCC5	203	VCC5
86	SA14	204	IRQ7
87	SA13	205	IRQ6
88	SA12	206	IRQ5
89	SA11	207	IRQ4
90	SA10	208	IRQ3
91	SA9	209	DACK2#
92	SA8	210	TC
93	SA7	211	BALE
94	SA6	212	OSC
95	SA5	213	MEMCS16#
96	SA4	214	IOCS16#
97	SA3	215	IRQ10
98	SA2	216	IRQ11
99	SA1	217	IRQ12
100	SA0	218	IRQ15
101	SBHE#	219	IRQ14
102	LA23	220	DACK0#
103	LA22	221	DRQ0
104	LA21	222	DACK5#
105	LA20	223	DRQ5
106	LA19	224	DACK6#
107	LA18	225	DRQ6
108	LA17	226	DACK7#
109	MEMR#	227	DRQ7
110	MEMW#	228	MASTER#
111	SD8	229	SD12
112	SD9	230	SD13
113	SD10	231	SD14
114	SD11	232	SD15
115	SMOUT3	233	SMOUT2
116	SMOUT1	234	SMOUT0
117	GND	235	GND
118	GND	236	GND

4. PIN FUNCTIONS

The functions are described below for each of the interfaces.
The abbreviations in the “Type” column have the following meanings:

I: Input pin
O: Output pin
O OD: Output pin, open-drain output
IO: Input /output pin
IO OD: Input / output pin, open-drain output

4.1 ISA Bus

Pin Name	Type	Functions
SA[19:17] SA[16:0]	O IO	System Address Bus SA19-SA0 of the bus
LA[23:17]	IO	Latchable Address Bus LA23-LA17 of the bus
SBHE#	IO	System Byte High Enable Active Low This signal indicates that SD[15:8] is effective.
SD[15:0]	IO	System Data Bus 16-bit data bus
IOR#	IO	I/O Read Active Low This signal requests an I/O device on the bus to output data to SD[15:8] or SD[7:0].
IOW#	IO	I/O Write Active Low This signal requests an I/O device on the bus to accept the data at SD[15:8] or SD[7:0].
IOCS16#	I	I/O Chip select 16 Active Low This signal lets the I/O device on the bus indicate the CARD-686 that 16-bit transfer is possible by the current I/O cycle.
MEMR#	IO	Memory read Active Low This signal requests a memory device on the bus to output data to SD[15:8] or SD[7:0].
MEMW#	IO	Memory write Active Low This signals request the memory device on the bus to accept data at SD[15:8] or SD[7:0].
SMEMW#	O	System memory write Active Low This signal is active when a memory write cycle is started for the 0 to1MB memory space on the bus.
SMEMR#	O	System memory read Active Low This signal is active when a memory read cycle is started for the in the 0 to 1MB memory space on the bus.

Pin Name	Type	Functions
MEMCS16#	I	Memory chip select 16 Active Low This signal lets the memory device on the bus indicate the CARD-686 that 16-bit transfer is possible by the current memory.
AEN	O	Address enable This signal indicates that the current cycle is a DMA cycle or a refresh cycle.
DRQ[7:5,3,1,0] DRQ2	I IO	DMA request Active High These signals request the CARD-686 for DMA transfer. DRQ2 becomes an output signal when the internal FDD interface is enabled and becomes an input signal when it is disabled .
DACK[7:5,3:0]#	O	DMA acknowledge Active Low These signals indicate the DMA channel, which requested for a DMA transfer, that the request was accepted.
TC	O	Terminal count Active High In a DMA transfer, this signal indicates the end of the DMA transfer..
REF#	IO OD	Refresh Active Low When this signal is active, it indicates that the cycle is a refresh cycle.
MASTER#	I	Master Active Low The bus master on this bus make this active in order to acquire the control authority of the bus. Before making this signal active, the bus master must make DRQn# active and must receive DACKn#.
SCLK	O	System clock This is the basic 8.33-MHz ISA clock. This signal is not output when POWERGOOD is inactive. Note: The SCLK frequency varies with the CPU and the CPU clock of the CARD-PC.
OSC	O	Oscillator 14.3 MHz 50% duty clock output. This signal is not synchronized with the system clock.
IOCHCK#	I	I/O channel check Active Low This signal informs the CARD-686 that a parity error or unrecoverable error has occurred in the memory or the I/O device on the bus. When this signal becomes active, NMI occurs to the CPU.

Pin Name	Type	Functions
IOCHRDY	IO OD	I/O channel ready Active High This signal terminates the bus cycle. When the memory or the I/O device on the bus wants to extend the bus cycle, it can extend the cycle by setting this signal to low immediately after detecting an effective address and command. The CARD-686 continues the bus cycle until this signal becomes high. When the DMA or the bus master is transferred to the internal DRAM of the CARD-686, the CARD-686 makes IOCHRDY inactive to extend the bus.
WS0#	I	Zero wait state Active Low Make this signal active in order to terminate the bus cycle without any wait states.
RESETDRV	O	Reset drive Active High System initialization signal. Initialize devices on the bus by using this signal.
BALE	O	Buffered address enable Active High This signal indicates that SA[19:0] and LA[23:17] have become effective and the CPU cycle has started. During the DMA and refresh cycle, this signal becomes high. Note: In case of the standard IBM-PC/AT, LA[23:17] becomes effective only at the beginning of the CPU cycle and devices on the bus need latch LA[23:17] by BALE. But the CARD-686 keep outputting effective addresses to LA[23:17] until the end of the cycle.
IRQ[15,14,9] IRQ12 IRQ[11,10,7:3]	I O IO	Interrupt request Active High These signals request the CARD-686 for interruption.. Since being used by the mouse interface, IRQ12 cannot be used on the bus. When being used by the serial interface inside the CARD-686, IRQ[11,10,4,3] become outputs. When being not used, they become inputs and can be used on the bus. When being used by the parallel interface inside the CARD-686, IRQ[7,5] becomes outputs. When being not used, they become inputs and can be used on the bus. When being used by the FDD interface inside the CARD-686, IRQ6 become an output. When being not used, it becomes an input and used on the bus.

4.2 LCD Interface

Pin Name	Type	Functions
LD[17:0]	O	Display data for flat panel display. Flat panel display data.
FPVTIM	O	Vertical display timing signal for a flat panel display. This signal indicates the display start timing of a screen for the flat panel.
FPHTIM	O	Horizontal display timing signal for a flat panel display. This signal gives the timing for the start of a scan line.
FPDOTCLK	O	Data shift clock signal for a flat panel display. This signal provides the shift clock for the display data.
EXDOTCLK	O	Specify Flat Panel Data Shift Clock(normally not used).
FPVCCON	O	Flat panel display power supply control signal. This signal turns on the logic power supply of the flat panel.
FPVEEON	O	Flat panel display power supply control signal. This signal turns on bias power of the flat panel.
FPAC	O	Liquid Crystal AC signal. This signal can be used when the simple matrix display monochrome panel requires an alternation.
FPBLANK#	O	Flat panel data blank signal. This signal indicates the period that no data is displayed on the TFT panel. This signal is generally connected to the display enable (DE) of the TFT panel.

4.3 CRT Interface

Pin Name	Type	Functions
VSYNC	O	Vertical display timing. This signal provides the vertical sync signal for a CRT.
HSYNC	O	Horizontal Display Timing. This signal provides the horizontal sync signal for a CRT.
RED	O	Analog Color signal.
RRTN	---	Red return signal.
GREEN	O	Color signal.
GRTN	---	Green return signal.
BLUE	O	Analog Color signal.
BRTN	---	Blue return signal.

4.4 IDE Interface

Pin Name	Type	Functions
HDCS0#	O	Hard disk chip select 0 Active Low 1F0H~1F7H select signal.
HDCS1#	O	Hard disk chip select 1 Active Low 3F6H~3F7H select signal.
HDENH#	O	Hard disk buffer enable high Active Low This signal is active during all 16-bit accesses to the disk, and can be used for buffer control of data bits DATA8-15 of the IDE drive interface.
HDENL#	O	Hard disk buffer enable low Active Low This signal is active during all disk cycles, and can be used for buffer control of data bits DATA0-7 of the IDE drive interface.
HD7	IO	Hard disk bit 7 Bit 7 of the data bus in the hard disk interface.
HDIR	O	Hard disk bus data direction Output for direction control of hard disk data buffer. This signal is high during read cycle.

4.5 FDD Interface

Pin Name	Type	Functions
FDDS1#	O OD	Drive select 1 Active Low Used as a select signal for drive 1.
FDDS2#	O OD	Drive select 2 Active Low Used as a select signal for drive 2.
FDMT1#	O OD	Motor on 1 Active Low Used as a motor on signal for drive 1.
FDMT2#	O OD	Motor on 2 Active Low Used as a Motor on signal for drive 2.
FDSTEP#	O OD	Step Active Low Stepping pulses signal indicating the number of steps the head must move.
FDDIR	O OD	Direction This signal indicates the seek direction. When low it indicates inward movement, and when high outward movement.
FDSIDE	O OD	Side Head selection signal. When low it selects head 1, and when high head 0.
FDRD#	I	Read data Data input read from drive.

Pin Name	Type	Functions
FDWD#	O OD	Write data Data input written to drive.
FDWE#	O OD	Write enable Active Low This signal controls writing to the drive.
FDWP#	I	Write Protect Active Low This signal from the drive indicates that the disk in the drive is write-protected.
FDDCHG#	I	Disk change Active Low This signal from the drive indicates that the disk has been removed from the drive.
FDINDEX#	I	Index Active Low This is the index detection signal from the drive.
FDTRK0#	I	Track 0 Active Low This signal is used to notify the system that the head has detection track 0.
FDHIDEN	O OD	High density select Active High When high, this signal indicates high density.

4.6 Keyboard Interface

Pin Name	Type	Functions
KBCLK	IO OD	Keyboard clock Clock signal for a PS/2-style keyboard interface.
KBDATA	IO OD	Keyboard data Data signal for a PS/2-style keyboard interface.

4.7 Mouse Interface

Pin Name	Type	Functions
MSCLK	IO OD	Mouse clock Clock signal for a PS/2-style mouse interface.
MSDATA	IO OD	Mouse data Data signal for a PS/2-style mouse interface.

4.8 Parallel Interface

Pin Name	Type	Functions
LPTSTROBE#	IO OD	Line printer strobe Active Low This signal is used as strobe for a peripheral on the parallel interface to read the data. In the high-speed parallel port mode this signal is used to indicate a write cycle.

Pin Name	Type	Functions
LPTAFD#	IO OD	Line printer auto feed Active Low When this signal is active, a parallel printer inserts a line feed after every line. This signal can be used as a data latch signal during write cycles and as a buffer enable signal during read cycle.
LPTBUSY	I	Line printer busy Active High This signal indicates that the printer is not able to accept data from the CARD-686.
LPTACK#	I	Line printer acknowledge Active Low This signal indicates that data transfer has been completed and also to prepare for the next transfer.
LPTERROR#	I	Line printer error Active Low This signal notifies the system of error in peripheral devices.
LPTPE	I	Line printer paper end Active High This signal notifies the system that the printer is out of paper.
LPTINIT#	IO OD	Line printer initialize Active Low Initialization signal for the printer.
LPTSLCTIN#	IO OD	Line printer select In Active Low This signal selects the peripheral device connected to the parallel port. It also serves as the address strobe in high-speed parallel port mode.
LPTSLCT	I	Line printer selected Active High Used to select the perip heral device currently connected to the port. In high-speed parallel port mode, this signal is used as an address strobe.
LPTDIR	O	Line printer direction This signal controls the buffer direction of LPTD[7:0]. When being set to low, this signal indicates an output, and when set to high, it indicates an input. This signal outputs “low” at all times in the ISA mode.
LPTD[7:0]	IO	Line printer data bus A data bus between the CARD-686 and a printer. This signal output only in the ISA mode and becomes a bit-directional signal in the PS/2 mode.

4.9 Serial Interface

Pin Name	Type	Functions
COMADCD# COMBDCD#	I	Data carrier detect Active Low This signal indicates that the modem or data terminal has detected the carrier.
COMADTR# COMBDTR#	O	Data terminal ready Active Low This signal indicates that the controller is ready for data transmission with respect to the modem or data terminal.

Pin Name	Type	Functions
COMADSR# COMBDSR#	I	Data set ready Active Low This signal indicates that the modem or data terminal is ready for data transmission with respect to the controller.
COMARTS# COMBRTS#	O	Request to send Active Low This signal indicates that controller has transmission data ready, and indicates a request to transmit data with respect to the modem or data terminal.
COMACTS# COMBCTS#	I	Clear to send Active Low This input signal indicates that the modem or the data terminal has become ready to receive or the CARD-686's request to send.
COMARI# COMBRI#	I	Ring indicator Active Low This signal indicates that the modem or data terminal has detected a telephone ringing signal. Alternatively, this signal can be used in the CARD-686 as a wake-up signal from the suspend state.
COMATXD COMBTXD	O	Serial data transmission This output is the asynchronous serial data.
COMARXD COMBRXD	I	Serial data receive This input is the asynchronous serial data.
IRTX	O	Ir data Transmission Transmission data for infrared communications.
IRRX	I	IrDA-SIR format data receive An input terminal of IrDA-SIR format receive data
DARX	I	Digital ASK data receive An input terminal of Digital ASK format receive data.

4.10 Power Management

Pin Name	Type	Functions
BATLOW#	I	Battery low Active Low This input signal indicates the CARD-686 that the battery is dead. When this signal becomes active, a system management interrupt (SMI) is executed.
BATWRN#	I	Battery warning Active Low This signal is used to indicate a battery capacity warning to the system.
SUSSTAT#	O	Suspend status Active Low This signal indicates that the system is in the suspended state.
SRBTN#	I	Suspend resume button Active Low This signal is a suspend and resume request signal with respect to the system.

Pin Name	Type	Functions
EXTSMI#	I	External system management interrupt Active Low A system management interrupt is input from an external device.
SMOUT[3:0]	O	System management out These signals can be used for standby control of local devices (hard disk, serial driver/receiver) on the output terminals for local standby control.
POWERGOOD	I	Power good Active High This signal indicates that the power supply is normal. When this signal become low, the CARD-686 is reset.

4.11 BIOS ROM Update Interfaces

Pin Name	Type	Functions
FLOAT#	---	Signal to write Flash ROM (BIOS)
PGM	---	Power supply to write Flash ROM (BIOS)
ROMCE0#	---	Signal to write Flash ROM (BIOS)

4.12 Speaker Interfaces

Pin Name	Type	Functions
SPKOUT	O	Speaker Out This can be used as a digital output for speaker.
WDTIM#	O	Watchdog Timer Out Active Low Watchdog Timer output.

4.13 Power Supply

Pin Name	Type	Functions
V_{CC3}	---	System Power 3.15 V to 3.6 V Power supply for internal circuits
V_{CC5}	---	System Power 5.0 V ± 5 % Power supply for external interfaces
V_{BK}	---	Backup power supply for real time clock When V_{CC5} is supplied, the same voltage as V_{CC5}. When V_{CC5} is not supplied, a backup voltage should be applied.
GND	---	System ground

5. DATAILED DESCRIPTION OF FUNCTIONS

5.1 System Overview

CARD-686 has a system configuration based on the ISA architecture. This section provides an overview of the system memory configuration and basic I/O.

5.1.1 Memory map

The memory map of the CARD-686 (DRAM 32MB) becomes as shown in Figure 5-1. The CARD-686 retains the memory area of 4GB, and the lower 16MB is released for the ISA bus. When a memory is the CARD-686 is accessed even in this range, the address is not output to the ISA bus.
Figures 5-1 and 5-2 show the memory maps of DRAM 32MB and 64MB respectively. These memory maps are available when the standard BIOS of the CARD-686 is used. When the BIOS is changed, the memory maps change.

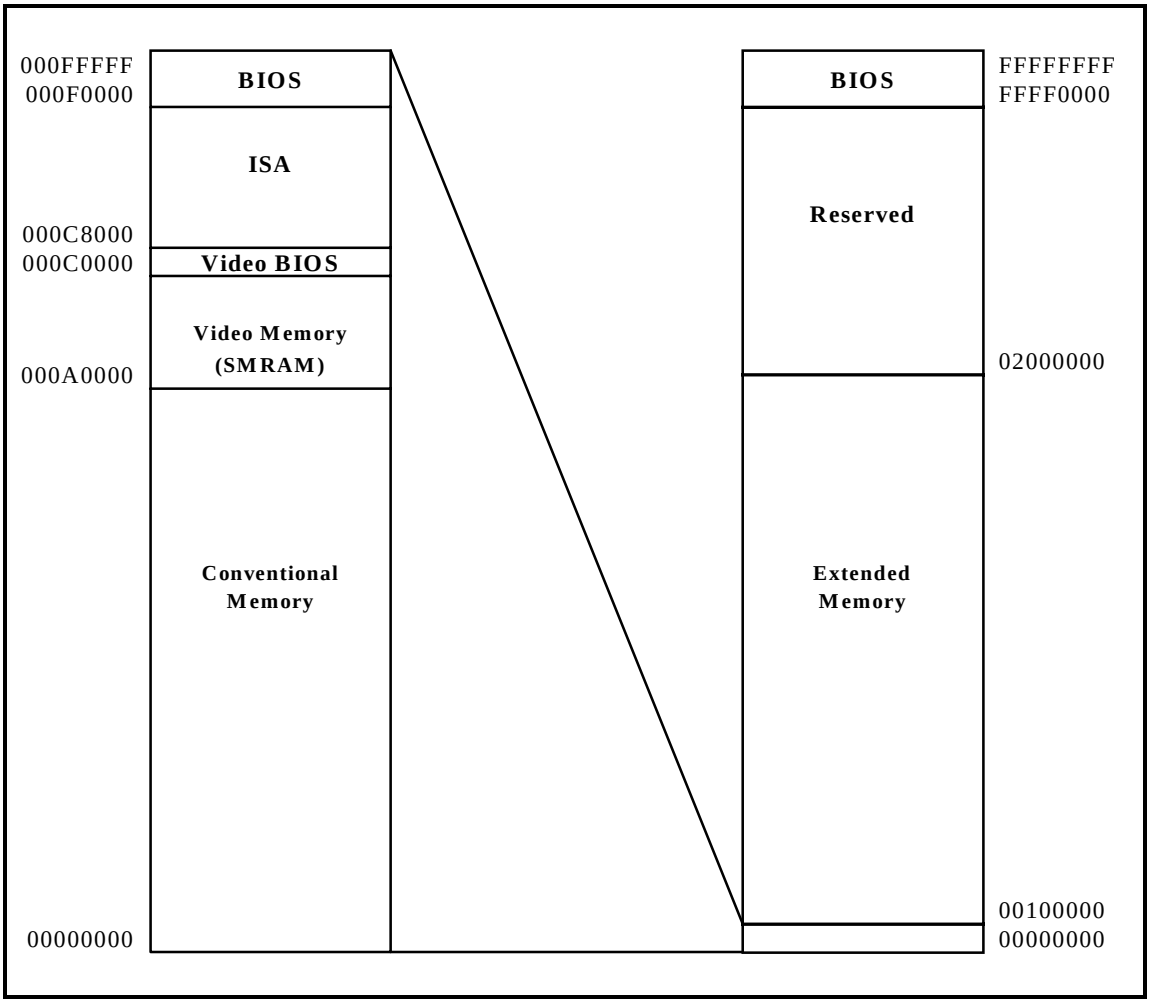

Figure 5-1 Memory Map (DRAM 32MB

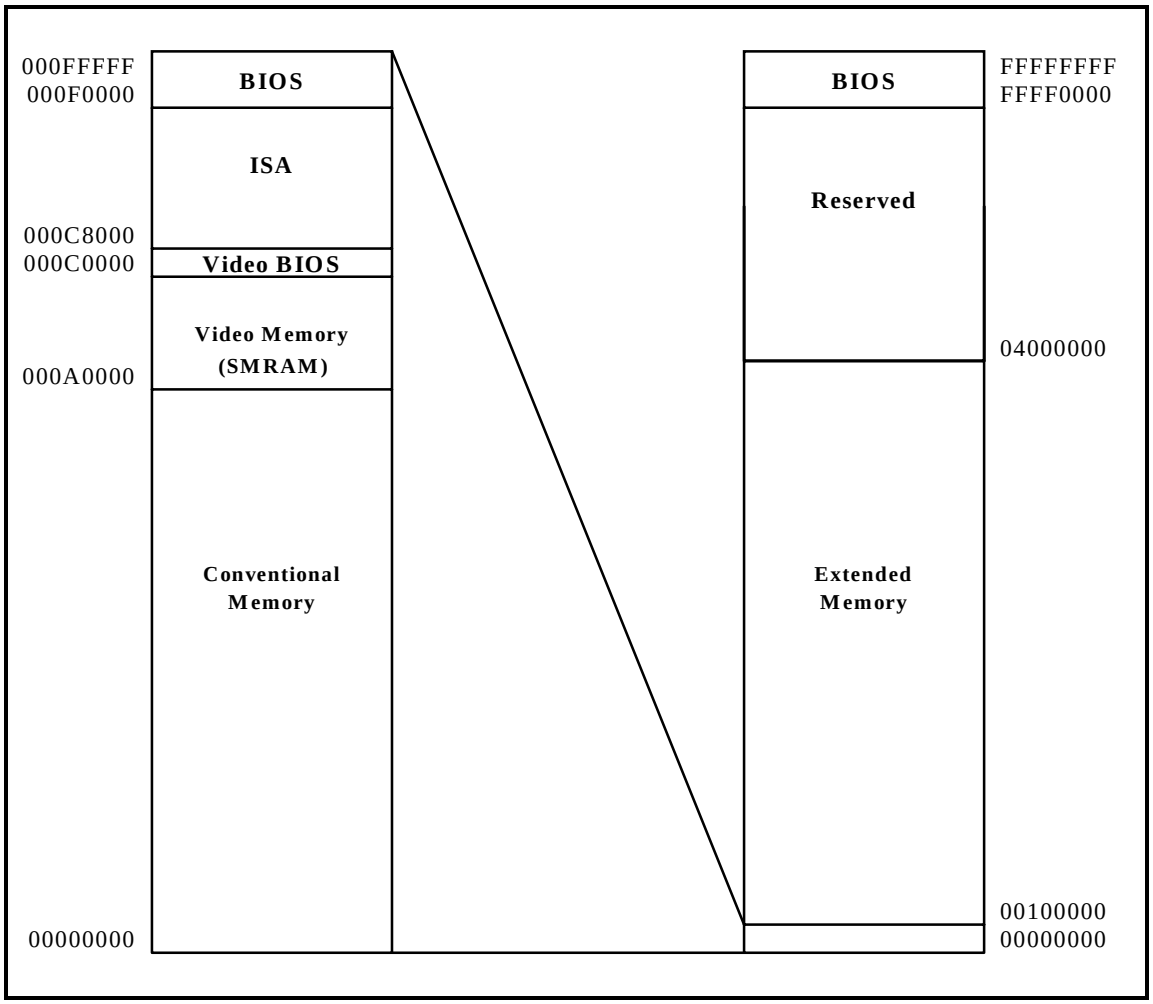

Figure 5-2 Memory Map (DRAM 64MB

5.1.2 DMA controllers

The CARD-686 has two DMA controllers (equivalent to the 82C37A). The DMA channels in this system are shown in Table 5-1 and Table 5-2.

Table 5-1 DMA controllers 1

Channel No.	Device allocated
CH0	Device on the ISA bus are usable.
CH1	Device on the ISA bus are usable.
CH2	Floppy disk.
CH3	Device on the ISA bus are usable.

Table 5-2 DMA controllers 2

Channel No.	Device allocated
CH4	Cascade connection to controller 1
CH5	Device on the ISA bus are usable.
CH6	Device on the ISA bus are usable.
CH7	Device on the ISA bus are usable.

Controller 1, which includes channels 0 to 3, is used for 8-bit data transfers. Between 8-bit I/O and 8-bit memory or 16-bit memory, transfer is possible in 8-bit units up to block of 64KB.

Controller 2, which includes channels 4 to 7, is used principally for 16-bit data transfers, and since channel 4 is connected in cascade to controller 1 it is not available to the ISA bus. Channels 5 to 7 are available to the ISA bus, and can be used for 16-bit data transfers. In this case, between 16-bit I/O and memory, transfer is possible in 16-bit units up to a block of 128KB.

The I/O addresses for the page registers used to support each DMA channel during DMA transfers are shown in T

able 5-3. The DMA controllers have only 16-bit addressing capability, are these page registers are used to make up for this.

Table 5-3 Page Register Addresses

Page Register	I/O Address
DMA channel 0	0087h
DMA channel 1	0083h
DMA channel 2	0081h
DMA channel 3	0082h
DMA channel 5	008Bh
DMA channel 6	0089h
DMA channel 7	008Ah
REFRESH	008Fh

Information relating to transfer timing is contained in the chapter on the ISA bus interface.

5.1.3 System interrupts and interrupt controller

CARD-686 interrupt types are shown below.

Table 5-4 Cause of interrupt on CARD-686

Level	Function
SMI	External system management interrupt Power management functions, keyboard emulation
NMI	Parity error or IOCHCK#
IRQ	Interrupts from the Interrupt Controller

IRQ interrupts are caused by the two interrupt controllers (equivalent to 82C59) mounted on the CARD-686. Cause of interrupt on the interrupt controller are as follows:

Table 5-5 Interrupt Controller Interrupt Assignments

Controller 1	Controller 2	Device
IRQ0		Timer Out 0
IRQ1		Keyboard
IRQ2		Cascade connection to controller 2
	IRQ8	Real time clock
	IRQ9	Usable on ISA bus
	IRQ10	Serial port (Note)
	IRQ11	Serial port (Note)
	IRQ12	Mouse
	IRQ13	Co-Processor
	IRQ14	HDD
	IRQ15	Usable on ISA bus
IRQ3		Serial port 2 (Note)
IRQ4		Serial port 1 (Note)
IRQ5		Parallel port 2 (Note)
IRQ6		FDD
IRQ7		Parallel port 1 (Note)

Note:
The CARD-686 has two built-in serial ports and one built-in parallel port. Interrupt of these serial ports is selected from IRQ3,410,11 and the one of the parallel port is selected from IRQ5,7. Interrupt for which the built-in serial ports and parallel port are not used can be used on the ISA bus.
When the FDD or the HDD is not used, IRQ6,14 can be used on the ISA bus.

5.1.4 Timer counters

The CARD-686 incorporates two 8254 equivalent timer-counters. Each has three independent timers. The following describes the applications of each and the inputs.

Table 5-6 Setting of Timer 1

Channel 0 System Timer	GATE 0	Fixed at "On"
	CLK IN 0	1.19 MHz
	CLK OUT 0	Connected to IRQ0 on Interrupt Controller 1
Channel 1 Refresh Request	GATE 1	Fixed at "On"
	CLK IN 1	1.19MHz
	CLK OUT 1	Refresh request
Channel 2 Speaker Interface	GATE 2	Controlled by I/O Port 61h
	CLK IN 2	1.19MHz
	CLK OUT 2	Used to drive the speaker interface

Table 5-7 Setting of Timer 2

Channel 0 SMI Request	GATE 0	Fixed at "On"
	CLK IN 0	32KHz
	CLK OUT 0	SMI request
Channel 1 General Purpose Timer Output (Watchdog Timer)	GATE 1	Fixed at "On"
	CLK IN 1	4KHz
	CLK OUT 1	Watchdog timer output
Channel 2 Alarm for Power Management Alarm	GATE 2	Controlled by the configuration register
	CLK IN 2	1.19MHz
	CLK OUT 2	Used to drive the speaker interface

For the detail of the timer counter, refer to the Seiko Epson's Technical Manual for Falconer Chip Set.

5.1.5 Real-time clock and CMOS RAM

The CARD-686 has a real time clock which provides clock and calendar functions and CMOS RAM used to hold system configuration information. The real time clock is compatible with a 146818.

Power must be supplied constantly to the V_{BK} pin in order to maintain the operation of the real time clock and the contents of CMOS RAM. When switching between the system power supply and the backup power supply, care is required to ensure that data is not lost. Care must be paid to the power supply sequence for the CARD-686.

5.1.6 I/O MAP

The I/O addresses from 000h to 0FFh are assigned to the system board (basic I/O). Although the addresses from 100h to 3FFh are available for the I/O channels, because CARD-686 already has built in I/O, use the following table as a reference when expanding.

I/O Address	Register Name		Function
000h-01Fh	00h RW	DMA Channel 0 Base and Current Address	DMA Controller 1 82C37A equivalent.
	01h RW	DMA Channel 0 Base and Current Word	
	02h RW	DMA Channel 1 Base and Current Address	
	03h RW	DMA Channel 1 Base and Current Word	
	04h RW	DMA Channel 2 Base and Current Address	
	05h RW	DMA Channel 2 Base and Current Word	
	06h RW	DMA Channel 3 Base and Current Address	
	07h RW	DMA Channel 3 Base and Current Word	
	08h WO	Command Resister	
	08h RO	Status Register	
	09h WO	Request Register	
	0Ah WO	Single-Mask Register	
	0Bh WO	Mode Register	
	0Ch WO	Clear Byte Pointer	
	0Dh RO	Master Clear	
	0Dh WO	Temporary Register	
	0Eh WO	Clear Mask Register	
	0Fh WO	Write all Mask Register	
020h-03Fh	20h WO	Initialization Control Word ICW1	Interrupt controller 1 82C59A equivalent.
	20h WO	Operation Control Word OCW2	
	20h WO	Operation Control Word OCW3	
	20h RO	Interrupt Service Resister	
	20h RO	Interrupt Request Resister	
	21h WO	Initialization Control Word ICW2	
	21h WO	Initialization Control Word ICW3	
	21h WO	Initialization Control Word ICW4	
	21h RW	Operation Control Word OCW1	
	21h RW	Interrupt Mask Resister	
040h-04Fh	40h RW	Channel 0 Count	Timer Counter 1 8254 equivalent.
	41h RW	Channel 1 Count	
	42h RW	Channel 2 Count	
	43h RW	Command Register	
048h-04Fh	48h RW	Channel 0 Count	Timer Counter 2 8254 equivalent.
	49h RW	Channel 1 Count	
	4Ah RW	Channel 2 Count	
	4Bh RW	Command Register	
050h-057h		Timer Counter 1 duplicated	
058h-05Fh		Timer Counter 2 duplicated	

I/O Address	Register Name		Function
060h-06Fh	60h R	Keyboard controller Data Input Buffer	Keyboard Controller
	60h W	Keyboard controller Data Output Buffer	
	61h RW	Port B	
	64h WO	Keyboard controller Command Register	Keyboard Controller
	64h RO	Keyboard Controller Status Register	
070h-07Fh	70h WO	RTC/CMOS RAM Address Port and NMI Mask	RTC/CMOS RAM
	71h RW	RTC/CMOS RAM Data port	
080h-09Fh	80h RW	Reserved	DMA Memory Address Mapper Page Register
	81h RW	Channel 2	
	82h RW	Channel 3	
	83h RW	Channel 1	
	84h RW	Reserved	
	85h RW	Reserved	
	86h RW	Reserved	
	87h RW	Channel 0	
	88h RW	Reserved	
	89h RW	Channel 6	
	8Ah RW	Channel 7	
	8Bh RW	Channel 5	
	8Ch RW	Reserved	
	8Dh RW	Reserved	
	8Eh RW	Reserved	
	8Fh RW	Refresh	
0A0h-0BFh	A0h WO	Initialization Control Word ICW1	Interrupt Controller 2 82C59A equivalent.
	A0h WO	Operation Control Word OCW2	
	A0h WO	Operation Control Word OCW3	
	A0h RO	Interrupt Service Resister	
	A0h RO	Interrupt Request Resister	
	A1h WO	Initialization Control Word ICW2	
	A1h WO	Initialization Control Word ICW3	
	A1h WO	Initialization Control Word ICW4	
	A1h RW	Operation Control Word OCW1	
	A1h RW	Interrupt Mask Resister	
0C0h-0DFh	C0h RW	DMA Channel 4 Base and Current Address	DMA Controller 2 82C37A equivalent.
	C2h RW	DMA Channel 4 Base and Current Word	
	C4h RW	DMA Channel 5 Base and Current Address	
	C6h RW	DMA Channel 5 Base and Current Word	
	C8h RW	DMA Channel 6 Base and Current Address	
	CAh RW	DMA Channel 6 Base and Current Word	
	CCh RW	DMA Channel 7 Base and Current Address	
	CEh RW	DMA Channel 7 Base and Current Word	
	D0h W0	Command Register	
	D0h RO	Status Register	
	D2h WO	Request Register	
	D4h WO	Mask Register	
	D6h WO	Mode Register	
	D8h WO	Clear Byte Pointer	

I/O Address	Register Name		Function
	DAh RO	Master Clear	
	DAh WO	Temporary Register	
	DCh WO	Clear Mask Register	
	DEh WO	Write all Mask Register	
0E0h-0EFh	E5h RW	CARD-686 Configuration Resister (Index)	
	E7h RW	CARD-686 Configuration Resister (Data)	
0F0h-0FFh	F0h WO	Mathematical Co-processor Resister	
100h-1EFh			Can be used on the ISA bus.
1F0h-1F7h	1F0h RW	Data Register	Hard Disk Controller
	1F1h RO	Error Register	
	1F2h RW	Sector Count	
	1F3h RW	Sector Number	
	1F4h RW	Cylinder HIGH	
	1F5h RW	Cylinder LOW	
	1F6h RW	SDH Register	
	1F7h RO	Status Register	
	1F7h WO	Command Register	
1F8h-277h			Can be used on the ISA bus.
278h-27Fh	278h RW	LPT2 Data Port	Parallel Port 2
	279h RO	LPT2 Status Port	
	27Ah RW	LPT2 Control	
	27Bh RW	Automatic Address Strobe Register	
	27Ch RW	Automatic Data Strobe Register	
	27Dh RW	Automatic Data Strobe Register	
	27Eh RW	Automatic Data Strobe Register	
	27Fh RW	Automatic Data Strobe Register	
280h-2F7h			Can be used on the ISA bus.
2F8h-2FFh	2F8h RO	Receiver Buffer	Serial Port 2
	2F8h WO	Transmit Holding Buffer	
	2F8h RW	Divider Latch Least Significant Byte	
	2F9h RW	Divider Latch Most Significant Byte	
	2F9h RW	Interrupt Enable Register	
	2Fah RO	Interrupt Register	
	2FBh RW	Line Controller Register	
	2FCh RW	MODEM Control Register	
	2FDh RO	Status Register	
	2Feh RO	MODEM Status Register	
	2FFh RW	Scratch Register	
300h-377h			Can be used on the ISA bus.
378h-37Fh	378h RW	LPT1 Data Port	Parallel Port 1
	379h RO	LPT1 Status Port	
	37Ah RW	LPT1 Control	
	37Bh RW	Automatic Address Strobe Register	
	37Ch RW	Automatic Data Strobe Register	
	37Dh RW	Automatic Data Strobe Register	
	37Eh RW	Automatic Data Strobe Register	
	37Fh RW	Automatic Data Strobe Register	

I/O Address	Register Name		Function
380h-3B3h			Can be used on the ISA bus.
3B4h-3BAh	3B4h RW	CRT Controller Index	VGA Controller (monochrome)
	3B5h RW	CRT Controller Data	
	3Bah W	Feature Control	
	3Bah R	Input Status Register	
3BBh-3BFh			Can be used on the ISA bus.
3C0h-3CFh	3C0h W	Attribute Controller Index/Data	VGA Controller
	3C1h R	Attribute Controller Index/Data	
	3C2h W	Miscellaneous Output	
	3C2h R	Input Status Register	
	3C3h RW	VGA Enable	
	3C4h RW	Sequencer Index	
	3C5h RW	Sequencer Data	
	3C6h RW	Video DAC Pixel Mask, Hidden DAC Register	
3C0h-3CFh	3C7h W	Pixel Address Read Mode	VGA Controller
	3C7h R	DAC Status	
	3C8h RW	Pixel Mask Write Mode	
	3C9h RW	Pixel Data	
	3CAh R	Future Control Readback	
	3CCh R	Miscellaneous Output Readback	
	3CEh RW	Graphics Controller Index	
	3CFh RW	Graphics Controller Data	
3D0h-3DFh	3D4h RW	CRT Controller Index	VGA Controller (color)
	3D5h RW	CRT Controller Data	
	3DAh W	Feature Control	
	3DAh R	Input Status Register	
3E0h-3F1h			Can be used on the ISA bus.
3F2h	3F2h WO	Digital Output Register	Floppy Disk Controller
3F3h			Can be used on the ISA bus.
3F4h-3F7h	3F4h RW	Main Status Register	Floppy Disk Controller
	3F5h RW	Data Register	
	3F6h RO	Reserved for IDE	
	3F7h RO	Digital Input Resister	
	3F7h WO	Diskette Control Register (Shared with Hard Disk Controller)	
3F8h-3FFh	3F8h RO	Receiver Buffer	Serial Port 1
	3F8h WO	Transmit holding Buffer	
	3F8h RW	Divider Latch Least Significant Byte	
	3F9h RW	Divider Latch Most Significant Byte	
	3F9h RW	Interrupt Enable Register	
	3FAh RO	Interrupt ID Register	
	3FBh RW	Line Control Register	
	3FCh RW	MODEM Control Register	
	3FDh RO	Status Register	
	3FEh RO	MODEM Status Register	
	3FFh RW	Scratch Register	

5.2 ISA Bus Interface

The CARD-686 is equipped with the Industry Standard Architecture (ISA) bus structure, a worldwide standard architecture for personal computer systems.

5.2.1 ISA Bus signals

The ISA bus consists of the following signals

Address Bus Signals

System Address bus (SA[19:0])
These signals are used to indicate memory and I/O device address on the bus. Specific memory and I/O device addresses are output on this bus. These addresses are latched within the CARD-686, and are enabled during the bus cycle. Also, when the Bus Mastering function is used, it is performed by driving the bus from a device on the I/O channel.

Latchable Address bus (LA[23:17])
These signals are used to indicate memory device addresses on the bus. They are used together with the system address signals, and make it possible to access up to 16MB of memory on the bus.

System Byte High Enable (SBHE#)
When active, this signal (which is active low) indicates transmission of the most significant 8 bits (SD[15:8]) on the system data bus.

Data Bus

System Data bus (SD[15:0])
This 16-bit data bus is used in the transmission of data between memory on the bus and the CPU and I/O devices.

I/O Control Signals

I/O Read (IOR#)
This signal gives an I/O device permission to drive data on the bus.

I/O Write (IOW#)
This signal instructs an I/O device to accept data from the bus.

I/O Chip Select 16 (IOCS16#)
This input is a signal that indicates to the CARD-686 that the data transfer on the bus is a 16-bit I/O transfer. The default for 16-bit I/O transfer is one wait cycle. When not driven low, the default transfers a 4-wait 8-bit I/O cycle.

Memory Control Signals

Memory Read (MEMR#)
This signal gives a memory device permission to drive data on the bus.

Memory Write (MEMW#)
This signal instructs an I/O device to accept data from the bus.

System Memory Write (SMEMW#)
This signal is active when a memory write cycle is started for the 0-1MB memory space on the bus.

System Memory Read (SMEMR#)
This signal is active when a memory read cycle is started for the 0-1MB memory space on the bus.

Memory Chip Select 16 (MEMCS16#)
This signal indicates a 16-bit memory transfer to the CARD-686. When this signal is not active, the default memory bus cycle, a 4-wait 8-bit cycle, is used.

DMA Control Signals

Address Enable (AEN)
When this signal is active, it indicates that the cycle is the DMA cycle or the refresh cycle.

DMA Request (DRQ[7:5,3:0])
DMA data transfer request signal sent to the CARD-686.

DMA Acknowledge (DACK[7:5,3:0])
This signal indicates that control of the bus was released to the DMA channel on which DMA transfer was requested.

Terminal Count (TC)
In the DMA transfer cycle, this signal indicates completion of the DMA channel transfer.

Refresh Control Signal

Refresh (REF#)
When this signal is active, it indicates that the bus refresh cycle has either been requested or is in progress.

External Master Control Signal

Master (MASTER#)
The external bus master makes this signal active in order to acquire the control authority of the bus. Before the external bus master makes this signal active, however, it must first make DRQn# active and then receive DACKn#.

Clock Signals

System Clock (SCLK)
This is the basic 8.33 MHz clock signal.

The SCLK frequency varies with the CPU and CPU clock of the CARD-PC.

Oscillator (OSC)
This is a 14.31818 MHz clock output. This signal is not synchronized to the system clock.

Other ISA Bus Signals

I/O Channel Check (IOCHCK#)
This signal alerts the CARD-686 when a parity error occurs in memory or an I/O device on the bus, or when an unrecoverable error occurs. This signal generates an NMI for the system.

I/O Channel Ready (IOCHRDY)
This signal terminates the bus cycle. If memory on ISA bus or an I/O device on the bus wants to extend the bus cycle, it can extend the cycle by searching for an effective address and command and then setting this signal low. Until this signal goes high, the CARD-686 will continue to insert waits in the cycle.

Zero Wait State (WS0#)
Make this signal initializes the system when the power is turned on. Initialize devices on the bus by using this signal. This signal is active for 50ms.

Reset Drive (RESETDRV)
When the power is turned on, devices on the ISA bus are initialized using this signal.

Buffered Address Latch Enable (BALE)
This signal indicates that SA[19:0] and LA[23:17] are enabled and the CPU cycle or DMA cycle has started. In the DMA cycle, this signal remains high throughout the cycle.

Interrupt Request(IRQ[15,14,12:9,7:3])
These signals are active high and are used as interrupt request signals. These signals are input asynchronously.

5.2.2 ISA bus cycle

The ISA bus supports the following types of bus cycles:

- ∗Memory read
- ∗Memory write
- ∗I/O read
- ∗I/O write
- ∗DMA
- ∗Refresh
- ∗External bus master

5.2.3 Memory read/write cycles

Figure 5-3 shows the basic timing of the 16-bit memory read/write cycle in the ISA bus cycle. Figure 5-4 shows the 8-bit memory read/write cycle. In both the 8- and 16-bit cycles, the system address lines SA[19:0] become valid within one system clock cycle previous to MEMR# becoming active. In the first bus cycle Ts, the system address becomes the valid address, and when the SCLK signal falls BALE becomes active. SA[19:2] are latched by the time of the Ts cycle within the CARD-686, and output.

The CARD-686 latches read data at the end of the last Tc cycle of the memory read cycle. Also, the CARD-686 outputs valid write data from the fall of the Ts cycle to the next fall of the last Tc cycle of the memory write cycle.

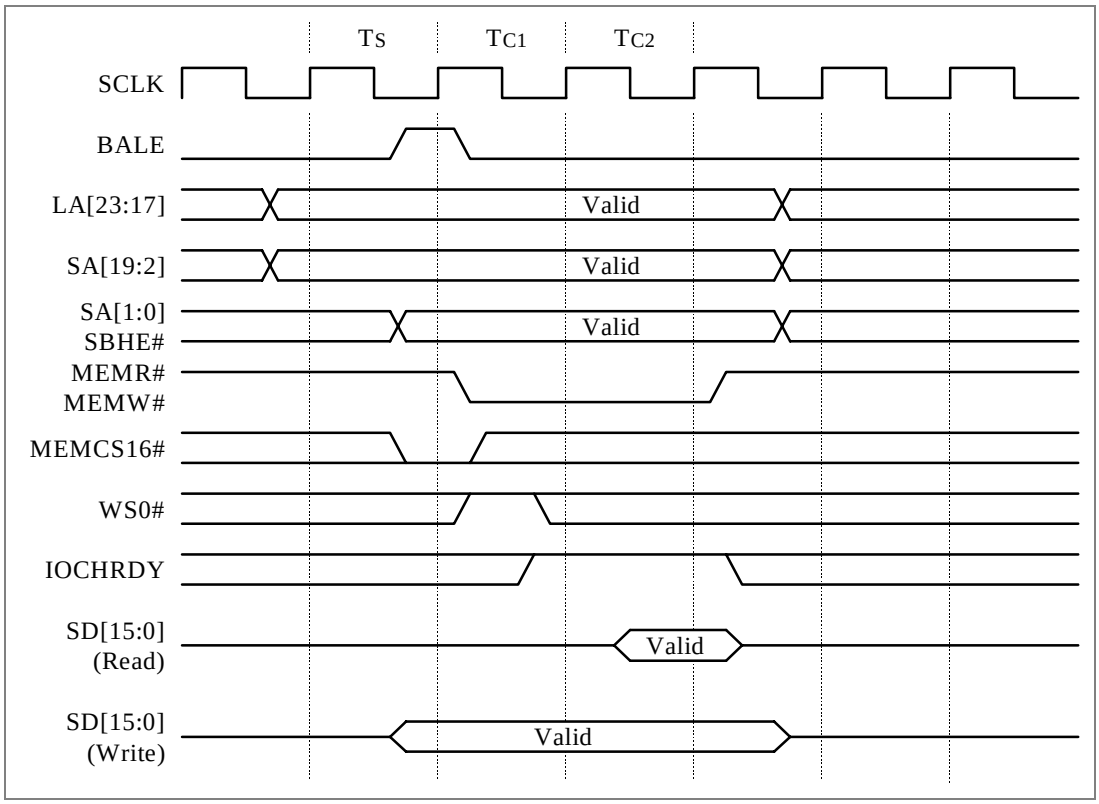

Figure 5-3 16bit ISA-Bus Memory Read/Write Cycle

16-bit memory transfers are carried out by an external device making MEMCS16# active. LA[23:17] become valid not later than the Tx cycle. MEMR# becomes valid following the SCLK falling edge in T_{C1}. In the 16-bit memory cycle, MEMR# becomes active in the first half of T_{C1}, and in the 8-bit memory cycle, MEMR# becomes active in the second half. In a 16-bit memory transfer, IOCHRDY is sampled for the last time 1 SYSCLK pulse before the end of the cycle. If at this time it is low, a 1 SYSCLK pulse wait is inserted. Thereafter, at the end of each of the Tc [cycles], it is sampled, and a 1 SYSCLK pulse wait is inserted. When IOCHRDY has become inactive, the cycle ends at the end of the next SYSCLK pulse.

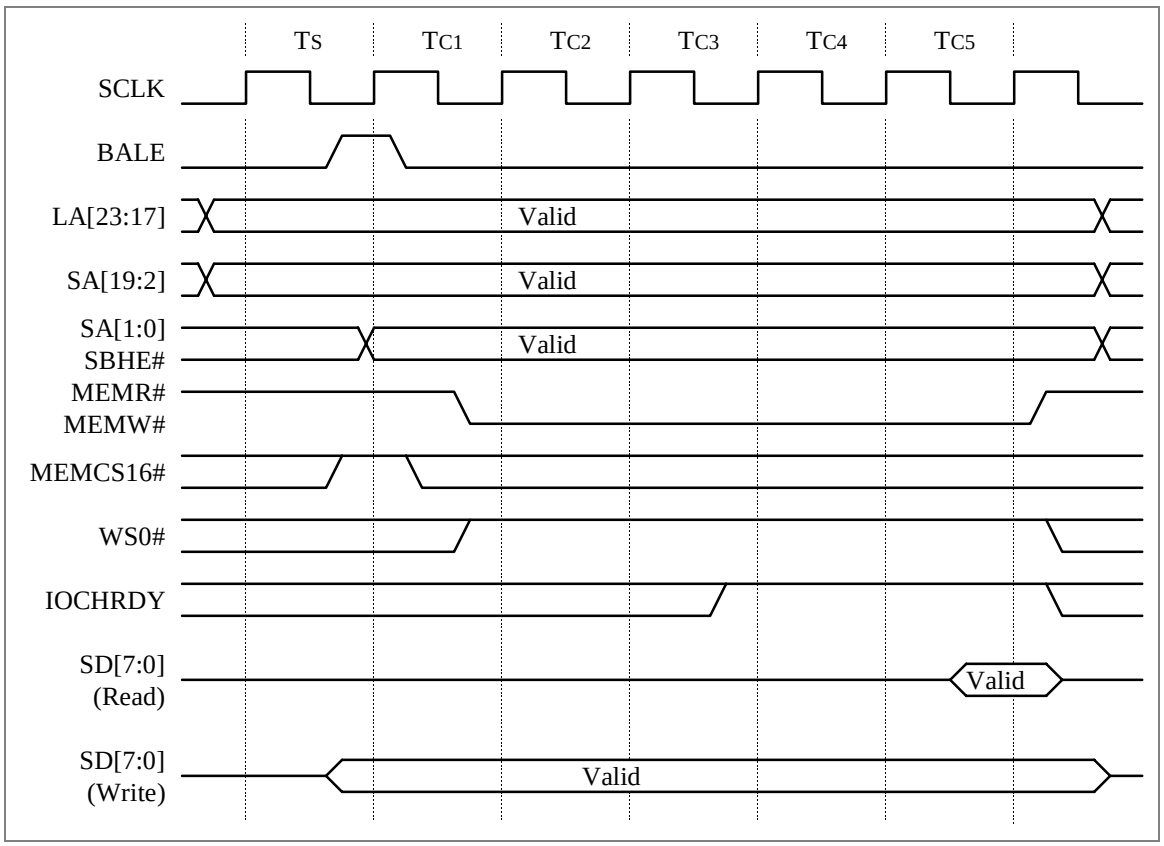

Figure 5-4 8bit ISA-Bus Memory Read/Write Cycle

In an 8-bit memory transfer, MEMCS16# is inactive. The CARD-686 samples this signal at the end of the Ts cycle, and if this signal is high, before sampling IOCHRDY, a 3-SCLK wait state is inserted. IOCHRDY is sampled at the end of T_{C5}, and if low, a 1 SCLK wait state is inserted. Thereafter, at the end of each of the Tc cycles, it is checked, and after IOCHRDY high is detected, after 1 SCLK cycle termination occurs. Figure 5-6 is a timing chart showing the 8-bit ISA memory cycle when IOCHRDY is inactive.

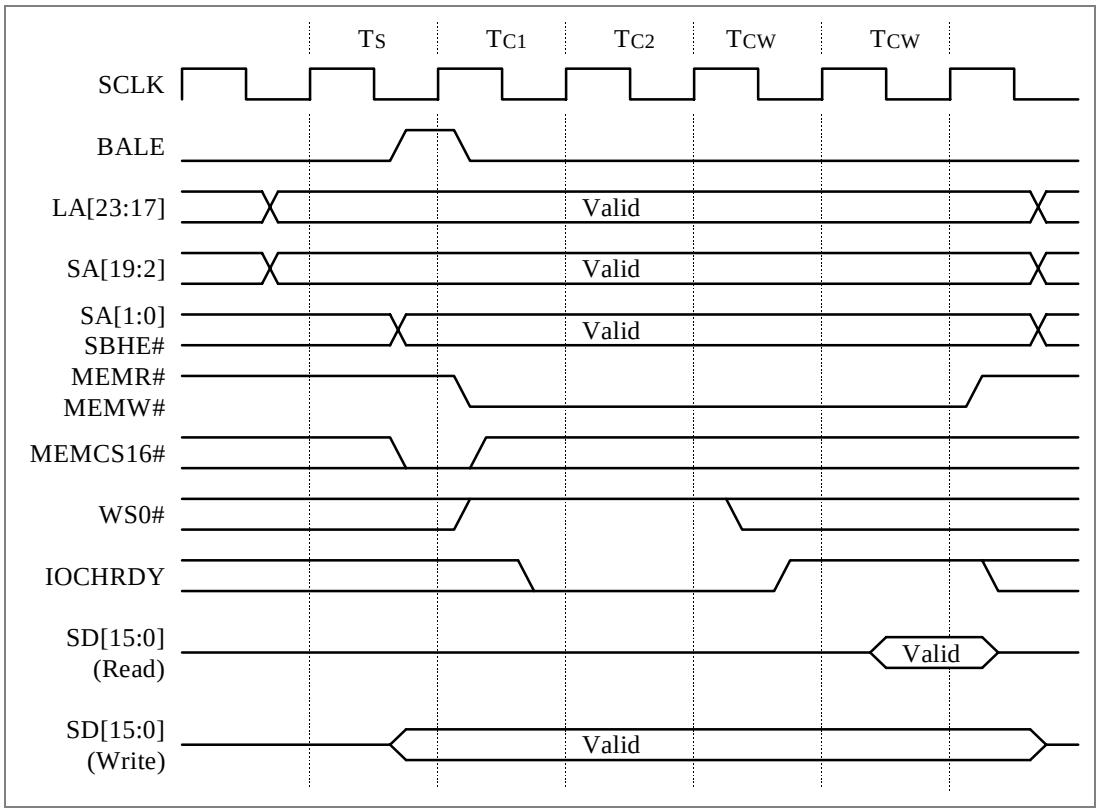

Figure 5-5 16bit ISA-Bus Memory Read/Write Cycle with IOCHRDY Deasserted

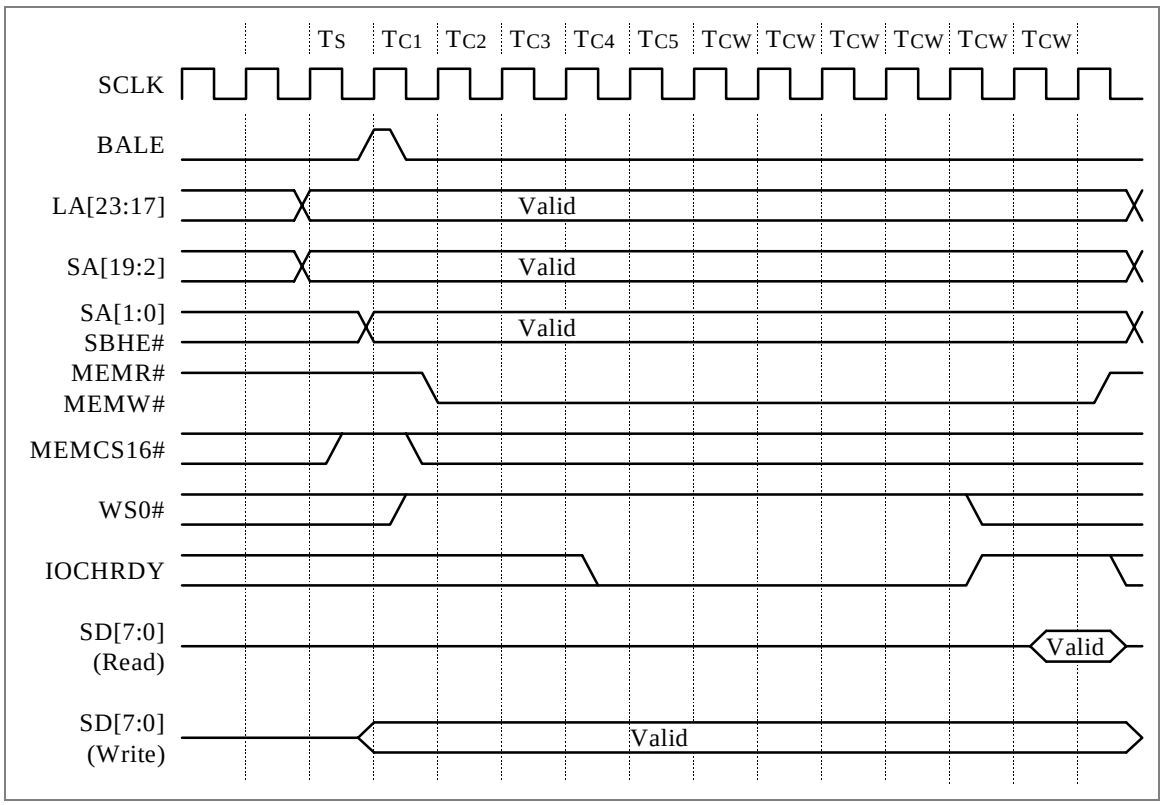

Figure 5-6 8bit ISA-Bus Memory Read/Write Cycle with IOCHRDY Deasserted

In a 16-bit memory transfer, WS0# is sampled at the falling edge of T_{C1}, and if it is found to be low, this cycle ends here.

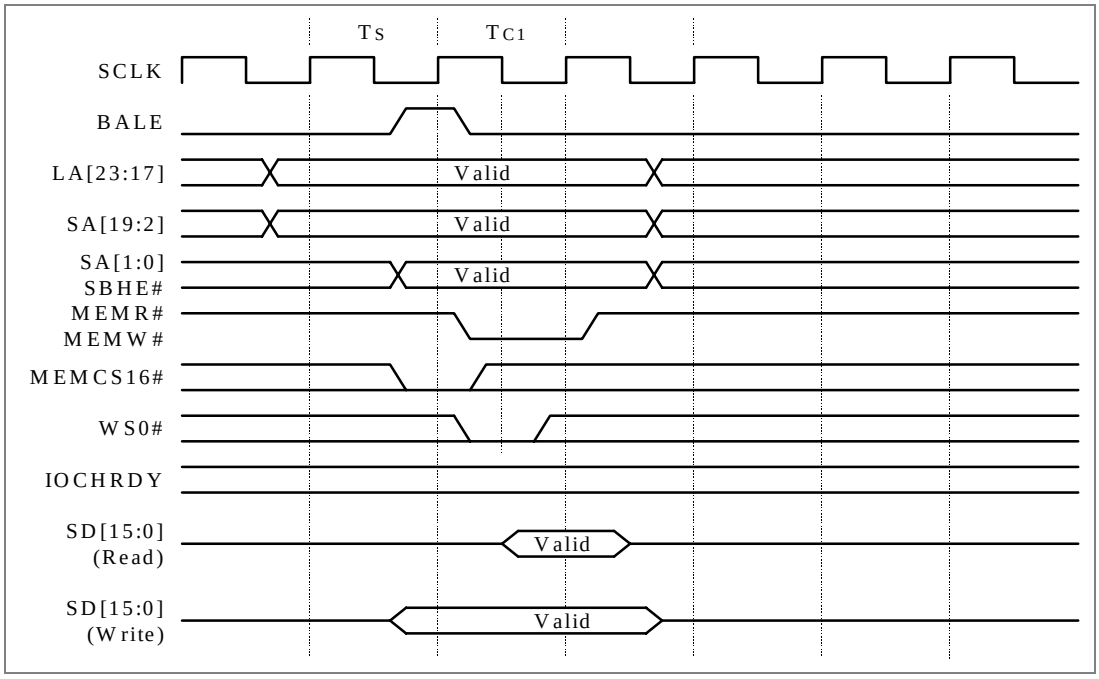

Figure 5-7 16bit ISA-Bus Memory Read/Write Cycle with WS0# Asserted

In a 8-bit memory transfer, WS0# is sampled at the end of T_{C1}. At this time, if WS0# is active, the bus cycle ends with this cycle (T_{C2}). Figure 5-8 is a timing chart showing the case where WS0# is used.

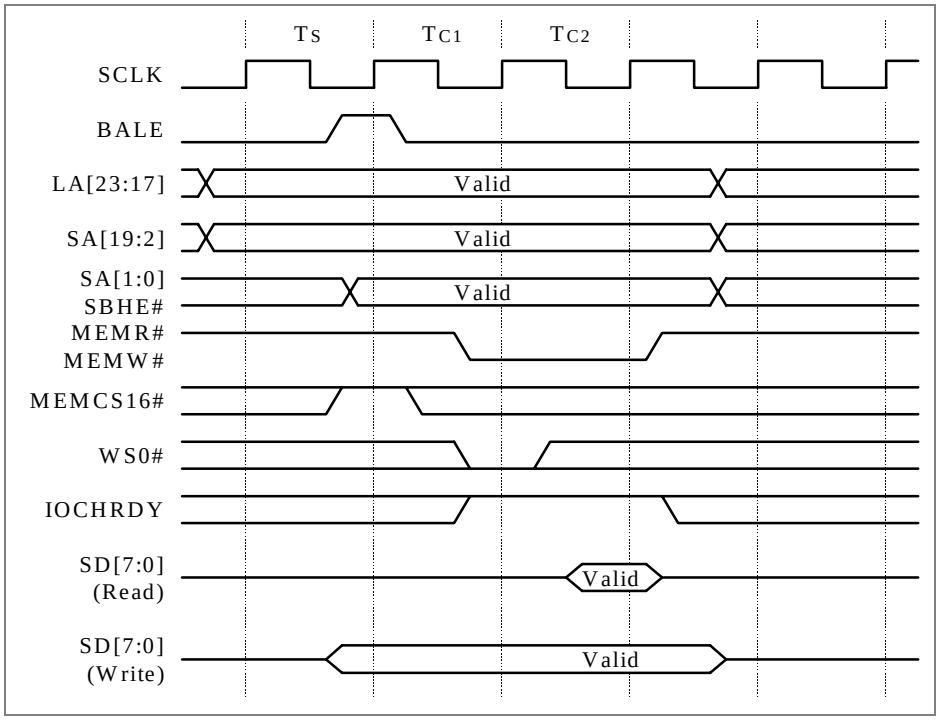

Figure 5-8 8bit ISA-Bus Memory Read/Write Cycle with WS0# Asserted

5.2.4 I/O read/write cycles

Figure 5-9 shows the basic timing for the ISA 16-bit I/O read/write cycle. Figure 5-10 shows the basic timing for the ISA 8-bit I/O read/write cycle. IOCS16#, which corresponds to MEMCS16# in the memory cycle, distinguishes between 16-bit I/O transfers and 8-bit I/O transfers. MEMCS16# is latched at the end of Ts, but IOCS16# is not latched. As a result, assurance from T_{C1} to the end of the cycle is required.

In the 16-bit memory cycle MEMR# and MEMW# become active from the beginning of T_{C1}, but in the 16-bit I/O cycle IOR# and IOW# become active in the second half of T_{C1}.

In the 16-bit I/O cycle WS0# is ignored. As a result, the 16-bit I/O cycle cannot be shorter than 3 SYSCLK cycles.

Just like in the memory cycle, the CARD-686 latches read data at the end of the last Tc cycle of the I/O read cycle and outputs valid write data from the fall of the Ts cycle to the next fall of the last Tc cycle of the I/O write cycle.

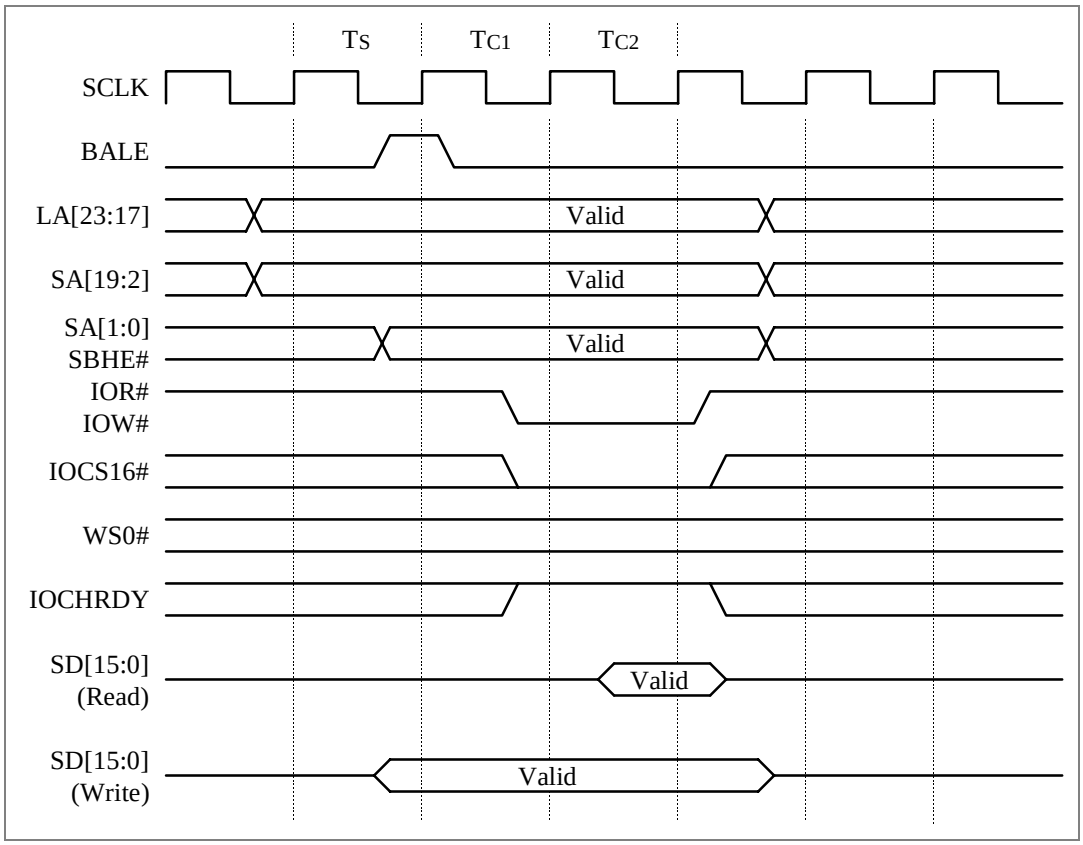

Figure 5-9 16bit ISA-Bus I/O Read/Write Cycle

In a 16-bit transfer, IOCS16# must be driven low by an external device on the ISA bus. IOCS16# is sampled at the end of T_{C1}. Moreover, LA[23:17] are, according to the CPU specification, always low in an I/O read/write cycle. At the falling edge of T_{C1}, IOR# is driven low, and at the end of the cycle the data is latched.

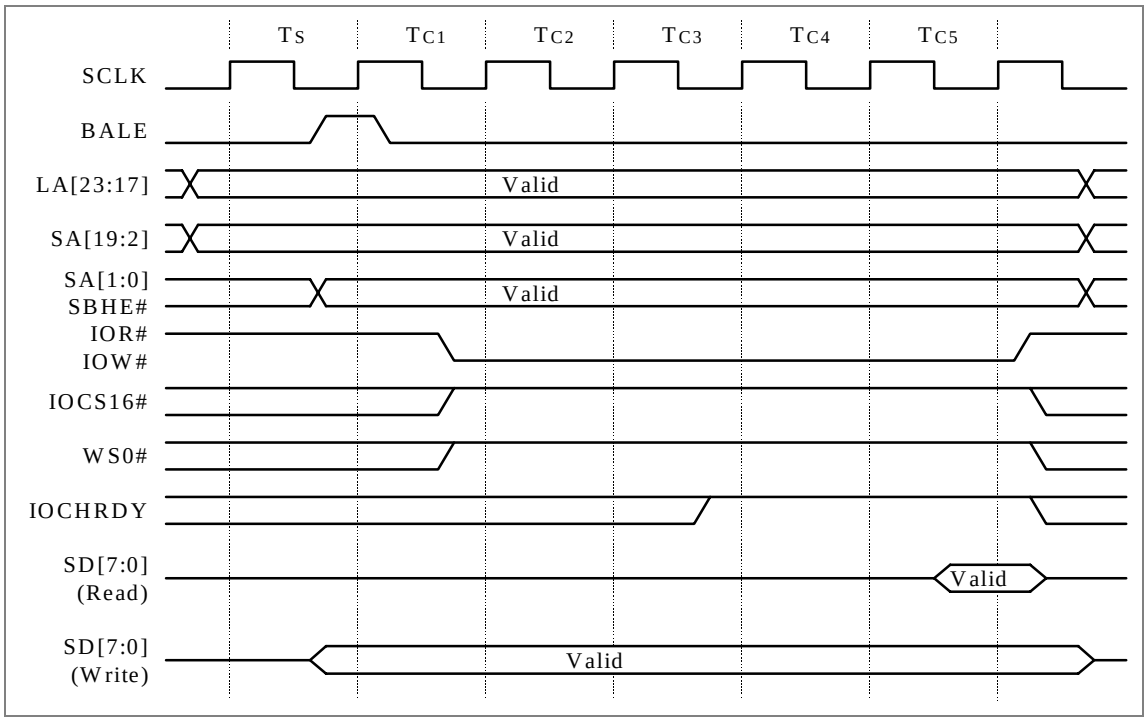

Figure 5-10 8bit ISA-Bus I/O Read/Write Cycle

In a 16-bit I/O transfer, IOCHRDY is sampled at the end of T_{C1}. If at this time IOCHRDY is found to be low, a 1 SCLK wait state is inserted, and it is sampled again at the beginning of the next cycle. If IOCHRDY is found to be high, this bus cycle ends after 1 SCLK cycle.

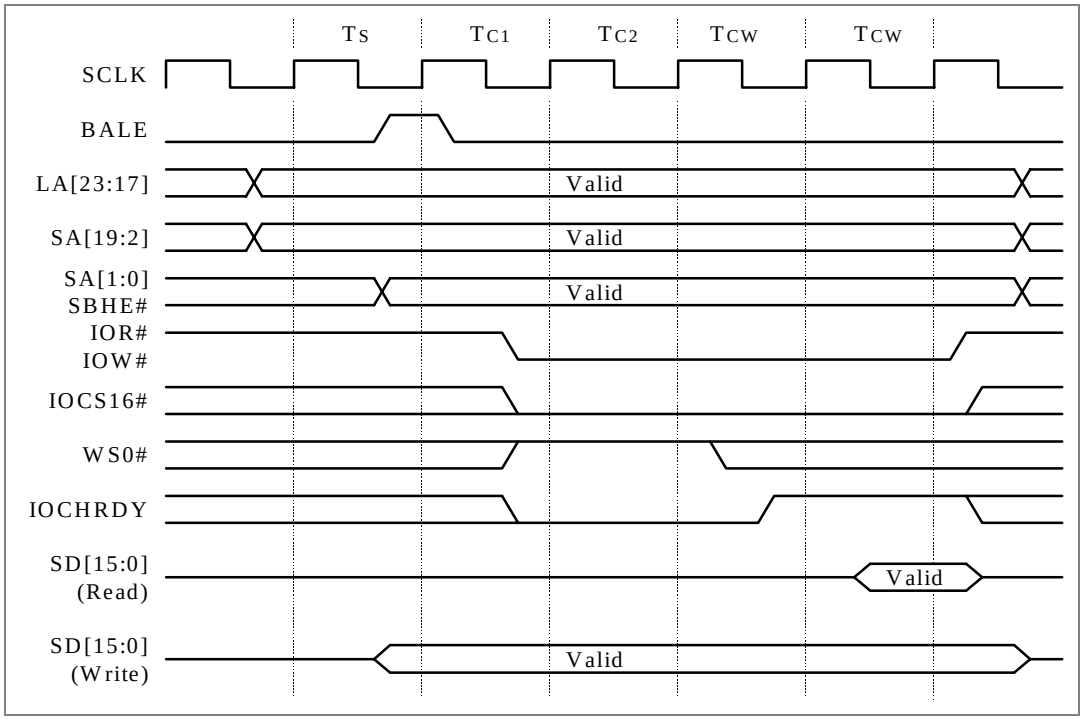

Figure 5-11 16bit ISA-Bus I/O Read/Write Cycle with IOCHRDY Deasserted

An 8-bit I/O device data transfer is carried out when IOCS16# is inactive. The CARD-686 samples this signal at the end of the Ts cycle, and if this signal is high, before sampling IOCHRDY, a 3-SCLK wait state is inserted. IOCHRDY is sampled at the end of T_{C4}, and until it is detected to be high, is sampled repetitively at the end of [each] Tc cycle. The bus cycle ends 1 SCLK cycle after IOCHRDY high is detected.

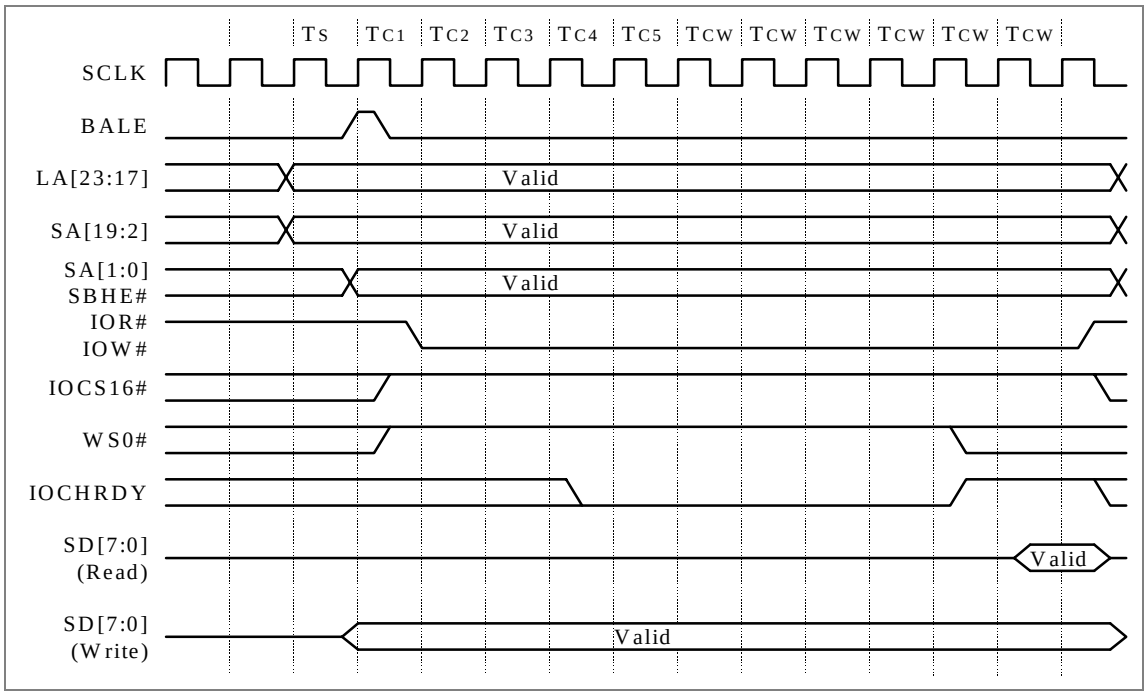

Figure 5-12 8bit ISA-Bus I/O Read/Write Cycle with IOCHRDY Deasserted

In an 8-bit I/O transfer, the CARD-686 samples WS0# at the end of T_{C1}. At this time, if WS0# is low, the bus cycle ends with this cycle. SD[7:0] are only valid during this cycle. Figure 5-13 is a timing chart showing the case where WS0# is active in an 8-bit I/O cycle. In a 16-bit I/O cycle, WS0# has no significance.

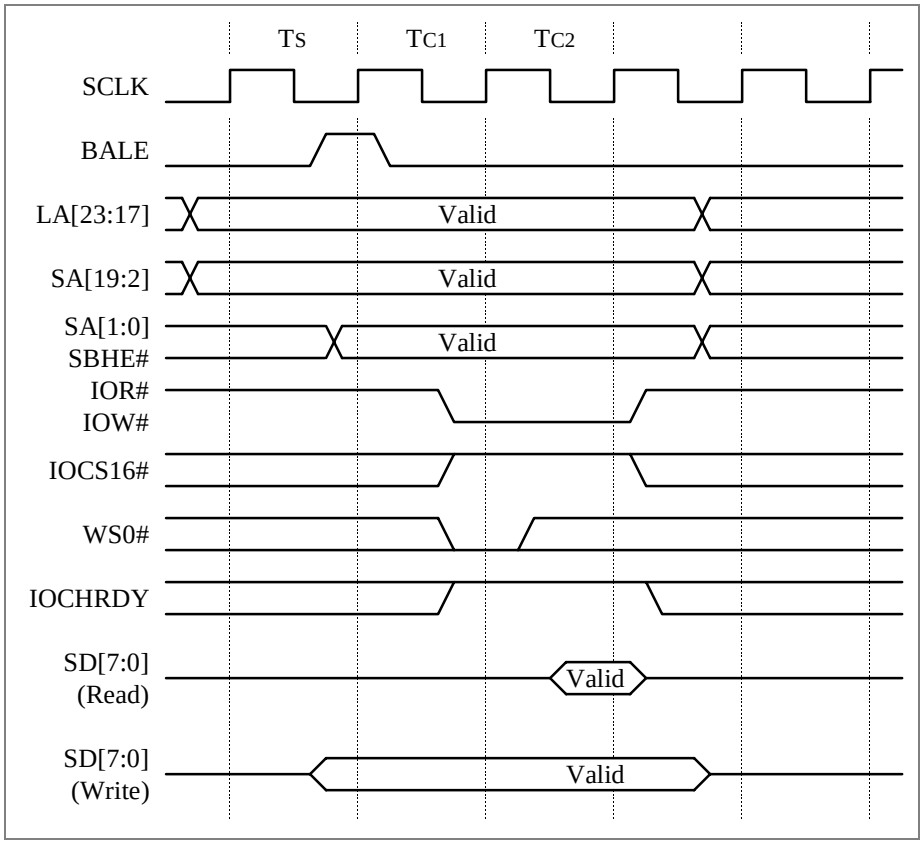

Figure 5-13 8bit ISA-Bus I/O Read/Write WS0# Asserted

5.2.5 DMA cycle

The CARD-686 contains two 8237A-equivalent DMA controllers (DMAC) to support the standard ISA DMA channels. These DMACs are configured with cascade connection as master/slave.

Figure 5-14 is a timing chart of the standard DMA cycle.

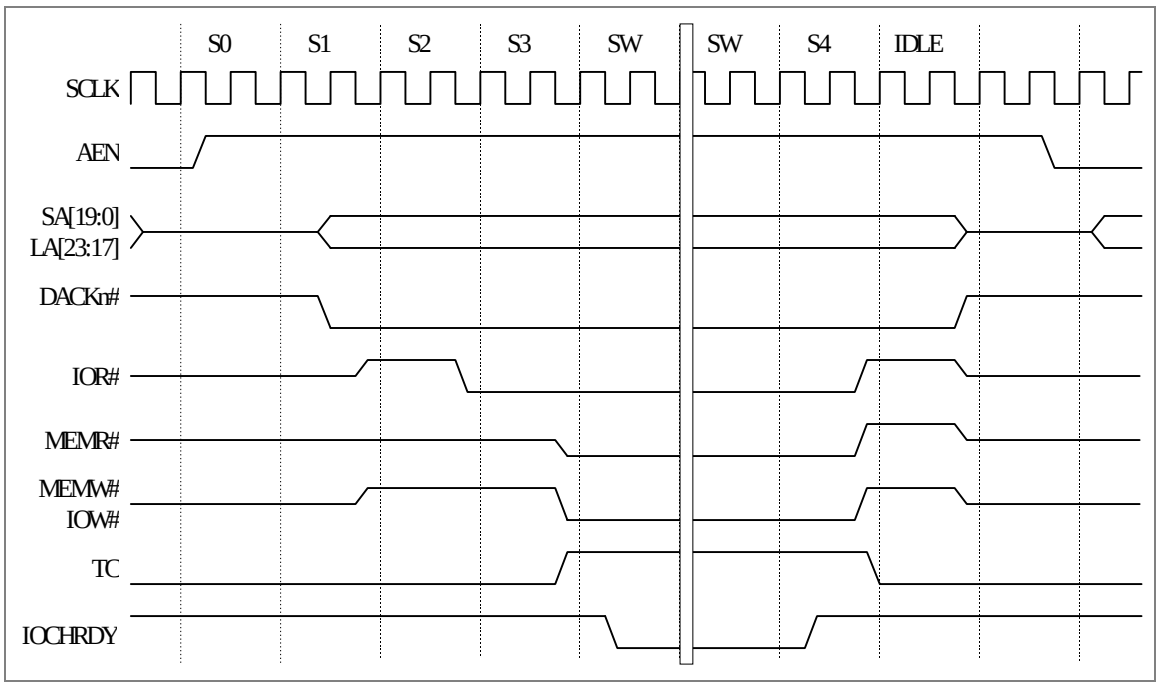

Figure 5-14 DMA Cycle with Wait State

DRQ[3:0] are used to request an 8-bit transfer between an 8-bit I/O device and an 8- or 16-bit memory device. Each channel transfers data in blocks of up to 64KB to a memory area ranging from 0 to 16MB.

DRQ[7:5] are used for 16-bit data transfer. These signals can only be used for data transfers involving 16-bit I/O devices and 16-bit memory devices. Each channel can transfer data up to 128KB in size to a system address space of 0 to 16MB.

The signals AEN and BALE become active (HIGH) during the DMA cycle. Memory addresses are output as follows from the memory mapper (by setting the DMA Memory Address Mapper Page Resister) and the DMAC:

Table 5-8 DMA Address Generation

	DMA Memory Address Mapper Page Resister	DMAC	
8 bits transfer	LA23~LA17, SA16	SA15~SA0	Reversed signal of SA0 is generated to SBHE#.
16 bit transfer	LA23~LA17	SA16~SA1	LOW is generated to SA0 and SBHE#.

5.2.6 External bus master cycle

Figure 5-15 shows the timing chart for the external bus master cycle for the ISA bus. In order to enter this cycle, the bus master makes the DRQn signal active. The external bus master then waits until DACKn# becomes active; finally, in order to establish the external bus master cycle, the external bus master must make MASTER# active.

After having made MASTER# active, the external bus master must output addresses (LA[23:17], SA[16:0], SBHE#) and data when one SCLK cycle comes. Also, read and write commands have to wait for another one SCLK cycle or more. The external bus master has not to output addresses to SA[19:17]. The LA[19:17] value is output to SA[19:17] from the CARD-686.
If MASTER# is held low for more than 15µsec., the memory on the ISA is not refreshed and the memory contents may be lost. To avoid this, it is necessary for the external bus master to make REF# active for the CARD-686 and to execute a refresh cycle.

When the external bus master accesses the memory or the I/O as well, the byte-swapping logic inside the CARD-686 works. So, when writing odd addresses, the external bus master outputs the data to SD[15:8], and when writing even addresses, it outputs the data to SD[7:0]. When reading odd addresses, the external bus master receives the data from SD[15:8], and when reading even addresses, it receives the data from SD[7:0]. Figure 5-15 shows the access timing from the external bus master to the internal DRAM of the CARD-686.

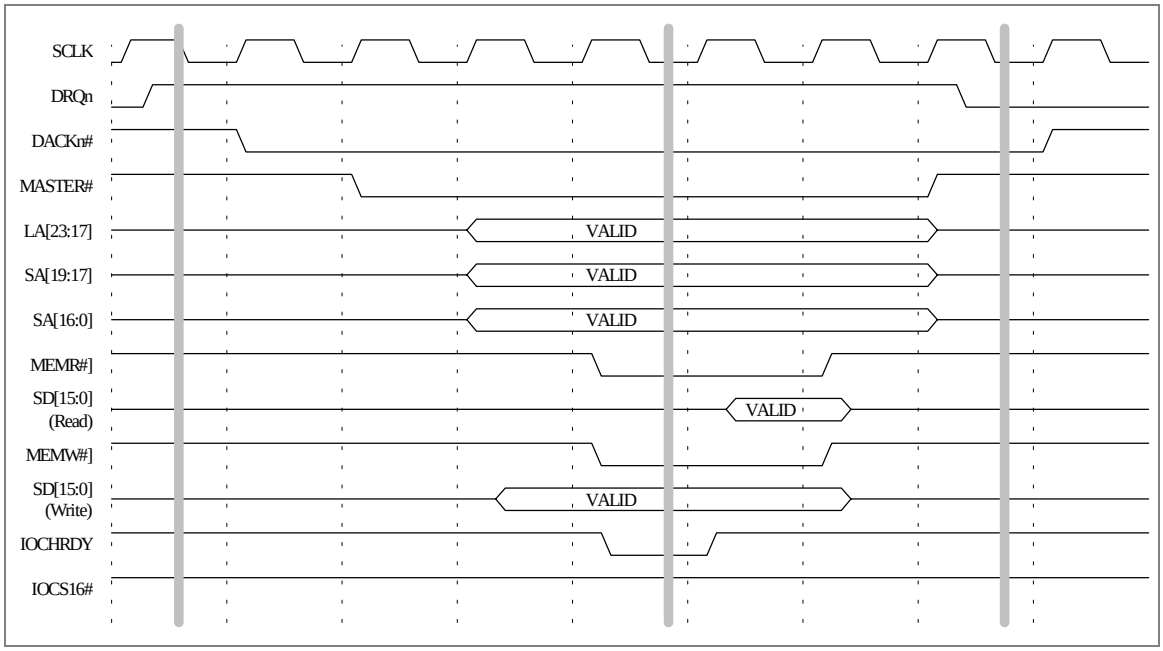

Figure 5-15 External Bus Master Cycle to Local Memory

When the external bus master accesses the internal DRAM, MEMCS16# does not become active as shown in Figure 5-15. Each time accessing the internal DRAM, the external bus master has to access the 16-bit memory.

5.2.7 External bus mastering precautions

The CARD-686 has a built-in write-back cache. When the DMA or the external bus master accesses the DRAM, the bus controller, ISP0016, of the CARD-686 operates as follows:

<1> ISP0016 checks from the address from the DMAC or the external bus master if it has hit the cache modified line.

<2> When ISP0016 has hit it, ISP0016 makes the CPU execute a write-back cycle and writes the cache data in the DRAM.

<3> When ISP0016 has not hit it or after the end of the write-back cycle, ISP0016 reads and writes the DRAM data.

In the meantime, ISP0016 makes IOCHRDY inactive and inserts a wait to the DMAC or the external bus master. (Even when the controller has not hit the modified line, it is necessary to check if it has hit, and a wait is inserted.) Therefore, such external bus master to which IOCHRDY cannot insert a wait does not work normally on the CARD-686.

Since the CARD-486D4 cache is of a write-through type, a wait cannot be inserted like to the CARD-686 when the DMA or the external bus master accesses the DRAM.

5.2.8 Refresh cycle

When the built-in 8254 (Programmable interval timer) shows refresh time-out values, the CARD-686 makes REF# active and execute the memory refresh cycle. In the refresh cycle, the CARD-686 outputs refresh addresses (12 bits) the MEMR# signal on the ISA bus. Figures 5-16 and 5-17 generally show the timing charts of the refresh cycle and the extended refresh cycle. To refresh slow memory devices, make IOCHRDY low to extend the cycle.

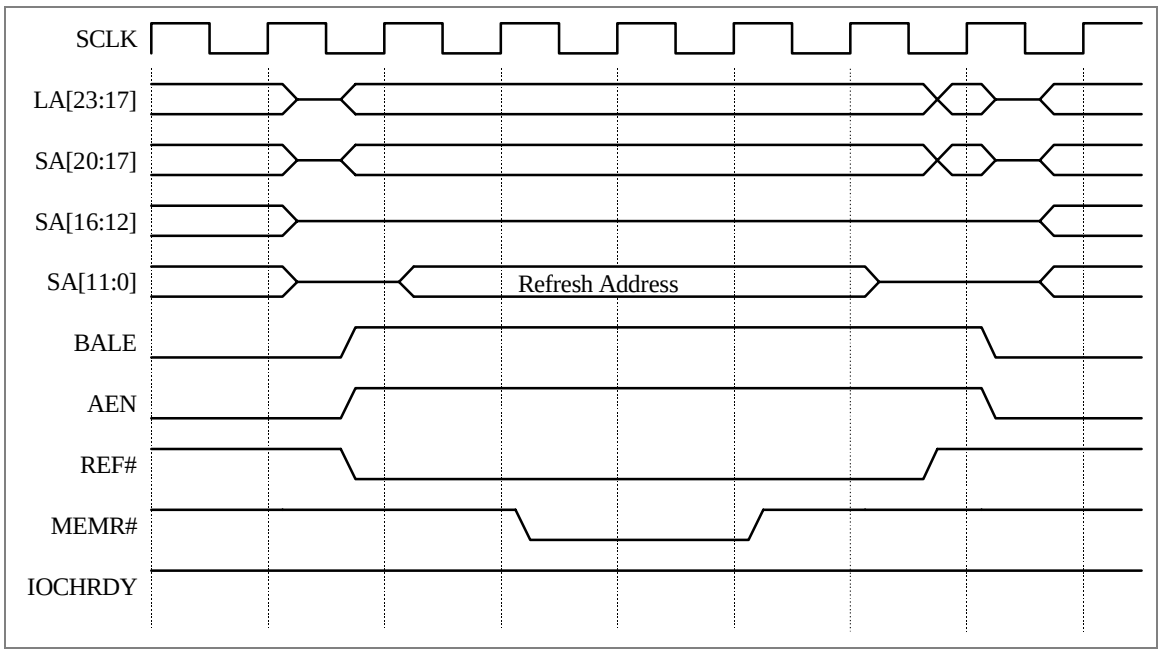

Figure 5-16 CARD-686 Initiated Default Refresh Cycle

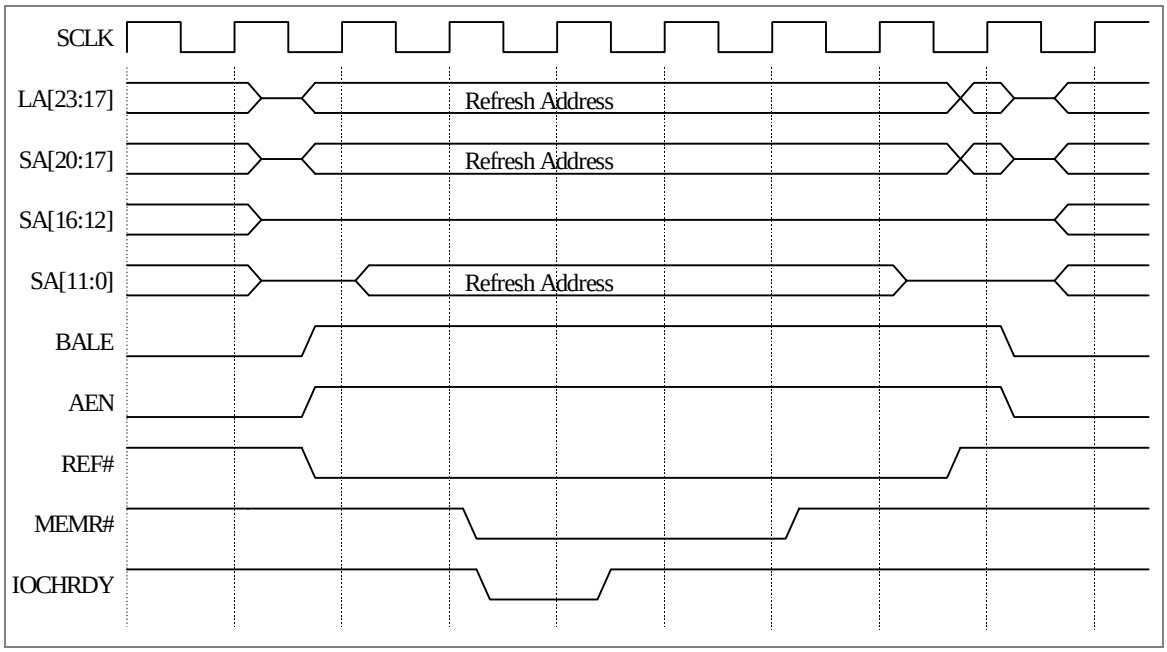

Figure 5-17 CARD-686 Initiated Extend Refresh Cycle

When the bus master has the bus control authority, the CARD-686 does not execute the refresh cycle even when 8254 shows refresh time-out values. If REF# is made active, the bus master can execute the refresh cycle. At the time, the CARD-686 generates refresh addresses and MEMR#.

Figures 5-18 and 5-19 show refresh cycles which are generated by the bus master with or without wait state.

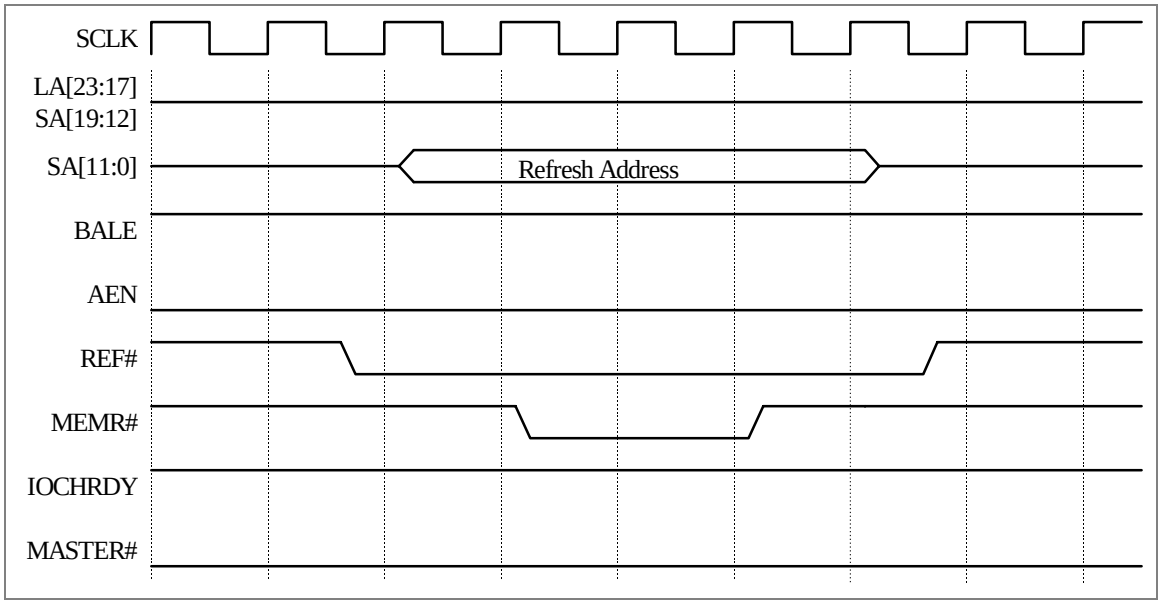

Figure 5-18 Bus Master Initiated Default Refresh Cycle

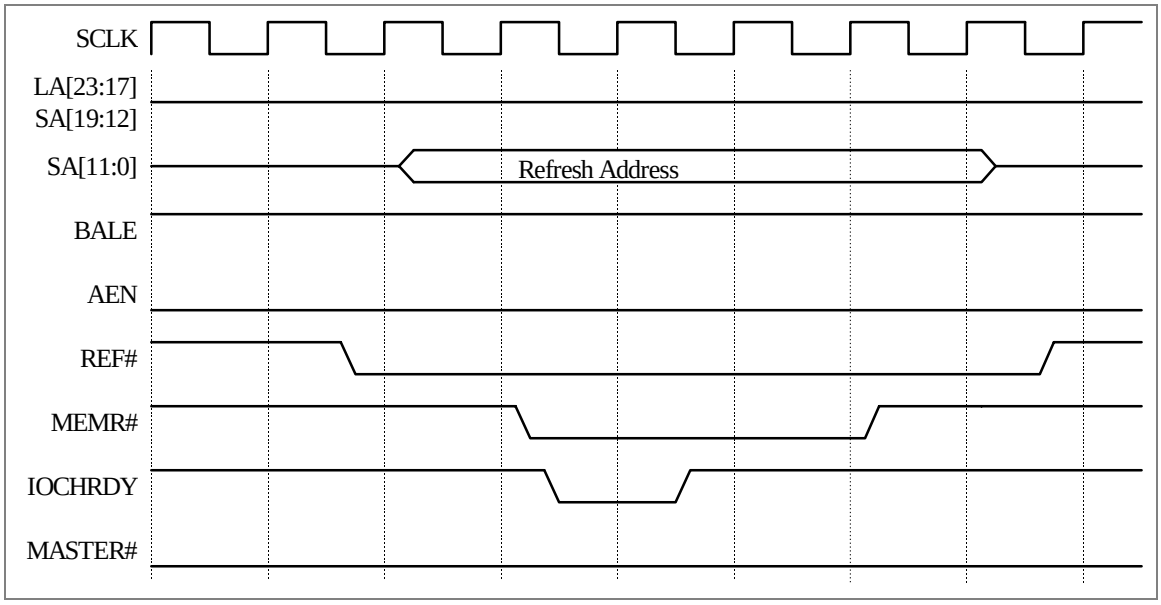

Figure 5-19 Bus Master Initiated Extended Refresh Cycle

5.3 Hard Disk Bus Interface

The CARD-686 is provided with the necessary chip select control signals for supporting IDE (Integrated Drive Electronics) type hard disk drives. It also supports the control circuits for I/O port 3F7h for shared floppy disk and hard disk drives.

This section describes the hard disk interface and its interface signals, timing, and reference circuits.

5.3.1 Features of the hard disk interface

∗ISA-compatible hard disk controller chip select signal generation
∗Support for control logic for port 3F7h shared by the hard disk controller and the floppy disk controller
∗Permits hard disk interface signals to be disabled

The PC AT-compatible hard disk interface addresses are located in the I/O addresses at 1F0h to 1F7h and 3F6h to 3F7h. CARD-686 supports HDCS0# and HDCS1# as chip select signals for these interface addresses.

In the PC/AT compatible system, I/O address 3F7h is shared by the floppy disk and hard disk controllers. Reading 3F7h results in reading 7 bits data (bits 0 to 6) from the hard disk controller and 1 bit data (bit 7) from the floppy disk controller. HD7 is prepared on the CARD-686 as a special bus for the hard disk.

In addition to the control logic for HD7, CARD-686 supports HDENH# and HDENL# for the control of two buffers for hard disks,. These buffer control signals simplify buffer control for a hard disk making 8-bit and 16-bit data transfers. HDENL# is active when making an 8-bit access to a hard disk, and both HDENH# and HDENL# are active for 16-bit accesses.

5.3.2 Hard Disk Interface Signals

Hard Disk Address Signals

System Address Bus (SA[2:0])
Right most 3 bits of the ISA address bus. While the hard disk is being accessed, the signal is driven by the CARD-686 or external bus master. It is used for selecting the address resister on the hard disk.

Hard Disk Data Signals

System Data Bus (SD[15:8], SD[6:0])
These signals are ISA bus system data signals.

Hard Disk Data bit 7 (HD7)
This signal is multiplexed with system data bit 7. The reason is I/O address 3F7h is shared by the floppy disk and the hard disk; as a result, hard disk data bit 7 must be multiplexed with internal bus data bit 7. In this system, the fact that I/O address 3F7h is currently being read is output to SD7 from the internal data bus. HD7 and SD7 are connected in this system in regards to accesses of I/O addresses for other hard disks.

Hard Disk Control Signals

Hard Disk Chip Select 0 (HDCS0#)
This active low output signal is active when accessing I/O addresses 01F0h to 01F7h.

Hard Disk Chip Select 1 (HDCS1#)
This active low output signal is active when accessing I/O addresses 3F6h to 3F7h.

Hard Disk Buffer Enable High (HDENH#)
This active low output signal is active during 16-bit hard disk accesses.

Hard Disk Buffer Enable Low (HDENL#)
This active low output signal is active during all hard disk accesses.

Hard Disk Data Bus Direction (HDIR)
This is the directional control signal for the hard disk bus transceiver. Normally, this signal is driven low, but goes high during the read cycle.

I/O Chip Select 16 (IOCS16#)
This active low signal is used by disks or other devices on the ISA bus to make 16-bit I/O transfer requests.

Interrupt Request 14 (IRQ14)
This signal is used to request interrupt servicing for the hard disk.

I/O Read (IOR#)
This is the ISA bus I/O read signal. This signal is output during the disk read cycle by the CARD-686 or by an external master device.

I/O Write (IOW#)
This is the ISA bus I/O write signal. This signal is output during the hard disk write cycle by the CARD-686 or by an external master device.

Reset Drive (RESETDRV)
This active high output signal is the reset signal used on the ISA bus. For use with IDE-type devices, this signal must be inverted.

5.3.3 Hard disk bus cycles

Hard disks are accesses through the I/O read and I/O write cycles.

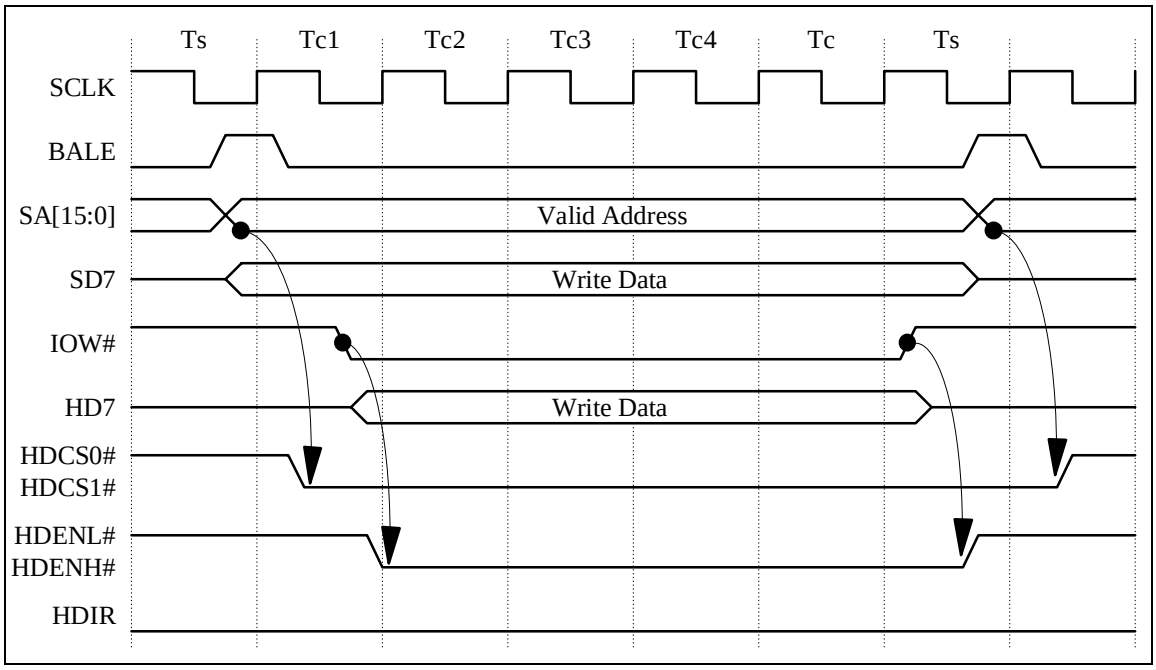

Figure 5-20 Hard Disk I/O Write Cycle

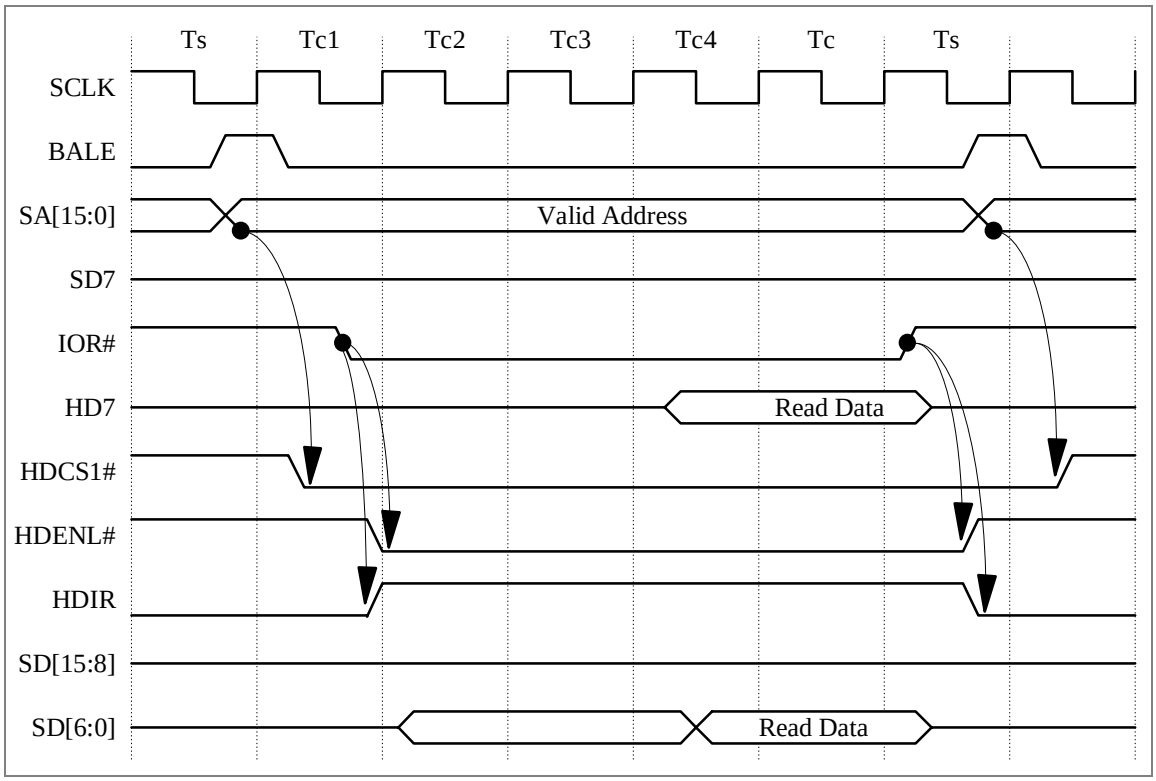

Figure 5-21 Hard Disk Read from I/O Address 3F7H

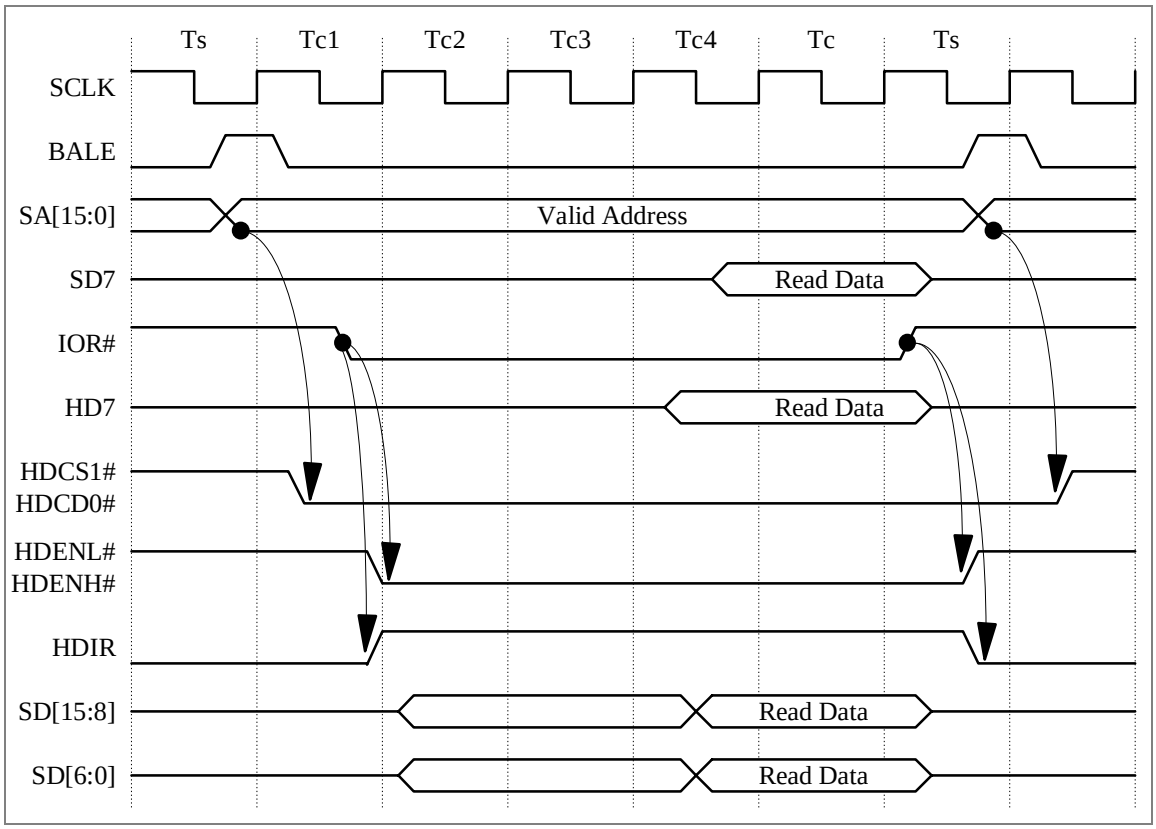

Figure 5-22 Hard Disk Read from I/O Address 01F0H01F7H or 03F6H

5.3.4 Hard disk hardware option

Buffered Hard Disk Interface

Figure 5-23 shows an example of connection of the CARD-686 and an IDE hard disk. The data buffer 74HCT245 is connected between the data SD[15:8, 6:0] and HD7 on the ISA bus and a had disk data bus. These buffers are controlled by HDENL#, HDENH# and HDDIR. SA[2:0], IOR# and IOW# are connected to the hard disk through 74HCT244. Since being connected to other devices on the ISA bus, it is recommended that the ISA data bus, SA[2:0], IOR# and IOW# are connected to the hard disk through the buffer. The RESET signal is connected to the hard disk through the inverter because the reset signal of the IDE hard disk is low active. The LDE which indicates that the disk is active is installed outside if necessary.

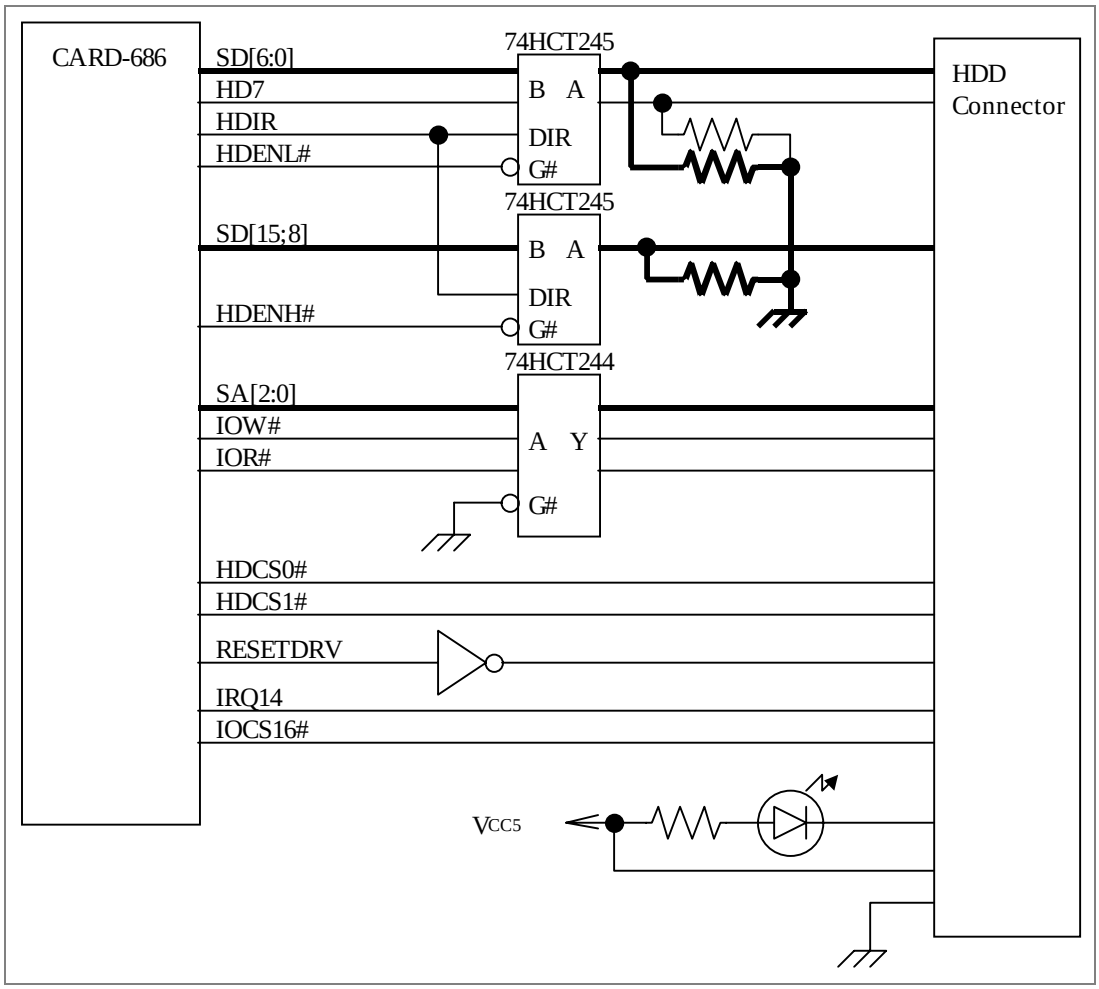

Figure 5-23 Buffered IDE Hard Disk Interface Examples

Hard Disk Power Shutdown

The hard disk is not used all the times and is idle in most cases and is accessed sometimes for reading and writing files. The hard disk consumes considerable power even in the idle state. The power consumption of even a hard disk which saves power as controlled by a software is not 0. The CARD-686 can cut off the power to the hard disk completely as shown in Figure 5-24. To cut off the power, the output signal SMOUT2 for power management is used. In this case, the power to the hard disk is controlled in the power management routine of the BIOS. The CARD-686 contains a hardware to detect idle states of devices, and the hardware is initialized and controlled in the power management routine of the BIOS.

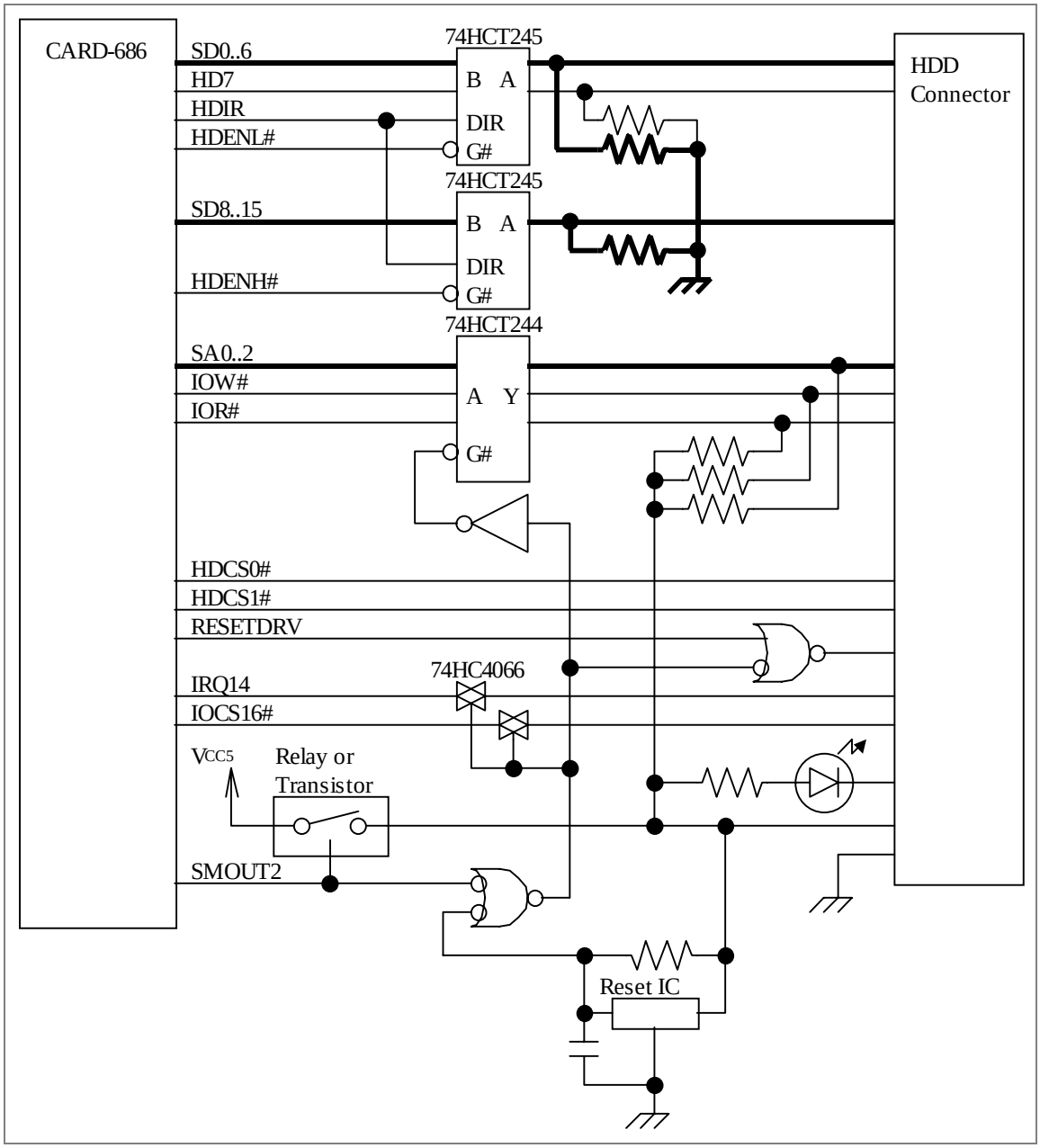

Figure 5-24 Buffered IDE Hard Disk Interface Examples Power Down

Direct IDE Hard Disk Interface

The CARD-686 can directly be connected to the IDE hard disk. (Figure 5-25). But this method is applicable only when the ISA bus is lightly loaded. This method can reduce the number of parts installed outside.

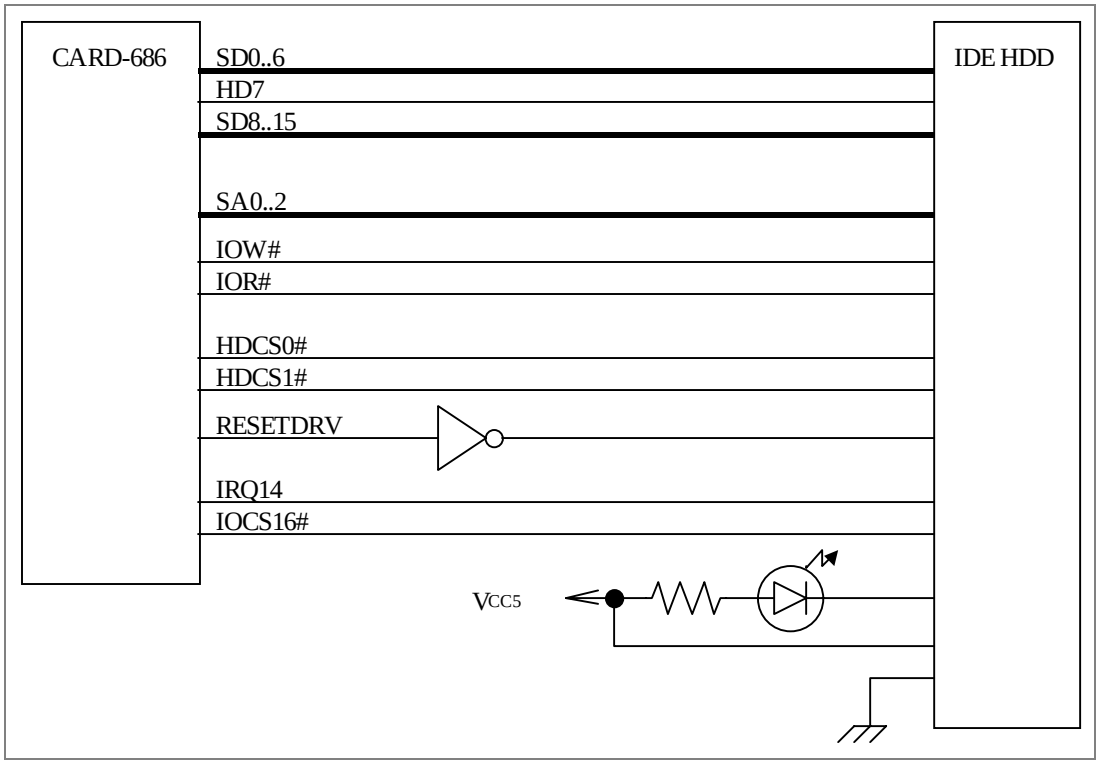

Figure 5-25 Direct IDE Hard Disk Interface Examples

5.4 Serial Port Interface

Features of the serial port interface

∗Support for two NS16C450-compatible serial port controllers
∗Transfer rate can be set from 50 to 56,000bps
∗Base address can be set
∗Infrared communications support

5.4.1 Serial port interface signals

The serial port control and data signals are shown below.

Control Signals

Data Carrier Detect (COMADCD#, COMBDCD#)
This signal indicates that the modem or data set has detected a carrier.

Data Terminal Ready (COMADTR#, COMBDTR#)
This signal indicates that the main controller has completed preparations for communicatio with the main controller.

Data Set Ready (COMADSR#, COMBDSR#)
This signal indicates that a modem or data terminal has completed preparations for communications with the main controller.

Request To Send (COMARTS#, COMBRTS#)
This signal indicates that the controller has prepared the data to be sent and is requesting to send the data to the modem or data terminal.

Clear To Send (COMACTS#, COMBCTS#)
This signal indicates that the modem or data terminal has completed preparations to receive in response to a request to send.

Ring Indicator(COMARI#, COMBRI#)
This signal indicates that the modem or data terminal detected a telephone ring signal. In addition, in CARD-686 this signal is also used as a wake-up signal when in the suspended state.

Data

Serial data Transmission (COMATXD, COMBTXD)
This output sends asynchronous serial data.

Serial data Receive (COMARXD, COMBRXD)
Asynchronous serial data input signal.

IrDA SIR data Transmission (IRTX)
This is an IrDA SIR-1.0/Digital ASK data output signal for infrared communications.

IrDA SIR data Receive (IRRX)
This is an IrDA SIR-1.0 data input signal for infrared communications.

Digital ASK data Receive (DARX)
This is a digital ASK data input signal for infrared communications.

5.4.2 Serial port functions

This serial port support full-duplex asynchronous serial transmissions. This controller's control signals are used in a protocol designed to ensure the accuracy of data transfers. Several signals are provided specifically for modem control. However, as long as certain rules are observed, those signals can also be used for communications with other devices.

"x" of I/O addresses is 3 for COM A and 2 for COM B

Table 5-9 Serial Port Registers

I/O Address	Description
xF8h WO	TX buffer when DLAB=0
xF8h RO	RX buffer when DLAB=0
xF8h RW	Divisor latch LSB when DLAB=1
xF9h RW	Divisor latch MSB when DLAB=1
xF9h RW	Interrupt enable register when DLAB=0 Bit[4-7] = 0 Bit3 : Modem status interrupt enable Bit2 : Receiver line status interrupt enable Bit1 : Transmitter holding register Bit0 : Received data available interrupt enable 1-enable, 0-disable
xFAh RO	Interrupt ID register Bit[3-7] = 0 Bit[2,1] Interrupt ID 0,0 : Modem status 0,1 : Transmitter holding register 1,0 : Received data available 1,1 : Receiver line status Bit0 : 0-interrupt pending
xFBh	Line control register Bit7 : DLAB 0 : Receiver buffer, transmitter holding, or interrupt enable access 1 : Divisor latch access Bit6 : Set Break, 1-enable Bit5 : Stick parity Bit4 : Even parity select Bit3 : Parity enable, 1-even, 0-odd Bit2 : Number of stop bit 0 : 1 stop bit, 1 : if word length is 5 bits stop bit length is 1.5 bit, if word length is 6, 7 or 8, then stop bit length is 2 bit.
xFBh	Line control register Bit[1-0] Bits per character (Word length) 0,0 : 5 0,1 : 6 1,0 : 7 1,1 : 8

xFCh	MODEM control register Bit[5-7] : reserved Bit4 : 1-Loop back mode Bit3 : Out2 interrupt enable, 1-enable Bit2 : Out1 Active, 1-active Bit1 : Request to send active, 1-active Bit0 : Data terminal ready, 1-active
xFDh	Line status register Bit7 : 0 Bit6 : Transmitter empty Bit5 : Transmitter holding register empty Bit4 : Break interrupt Bit3 : Framing error Bit2 : Parity error Bit1 : Overrun error Bit0 : Data ready
xFEh	MODEM status register Bit7 : Data carrier detect Bit6 : Ring indicator Bit5 : Data set ready Bit4 : Clear to send Bit3 : Delta data carrier detect Bit2 : Trailing edge ring indicator Bit1 : Delta data set ready Bit0 : Delta clear to send
xFFh	Scratch register Independent data for General Data

Configuration Register settings are carried out by the BIOS, but the settings are listed here for reference. Settings can also be made for the infrared communications protocol. Read/Write operations on the Configuration Registers use I/O ports E5h and E7h. For the detail, refer to the Seiko Epson's manual of Falconer Chip Set.

For UART1, the I/O address and interrupt numbers can be changed by setting UART1 Configuration [UART1CFG] in the Configuration Registers.

Table 5-10 UART1 Configuration

bit	Function	Description
1,0	UART1 I/O Address bit 1,0	bit1 bit0 0 0 : I/O 3F8h~3FFh 0 1 : I/O 2F8h~2FFh 1 0 : I/O 3E8h~3EFh 1 1 : I/O 2E8h~2EFh
3,2	UART1 IRQ bit 1,0	bit3 bit2 0 0 : IRQ4 0 1 : IRQ3 1 0 : IRQ11 1 1 : IRQ10
4	UART1 Enable	0 : Disable 1 : Enable

For UART2, the I/O address and interrupt numbers can be changed by setting UART2 Configuration [UART2CFG] in the Configuration Registers. It is also possible to select the infrared communications protocol for UART2.

Table 5-11 UART2 Configuration

bit	Function	Description
1,0	UART2 I/O Address bit 1,0	bit1 bit0 0 0 : I/O 3F8h~3FFh 0 1 : I/O 2F8h~2FFh 1 0 : I/O 3E8h~3EFh 1 1 : I/O 2E8h~2EFh
3,2	UART2 IRQ bit 1,0	bit3 bit2 0 0 : IRQ4 0 1 : IRQ3 1 0 : IRQ11 1 1 : IRQ10
4	UART2 Enable	0 : Disable 1 : Enable
5	UART2 IR Enable	0 : Serial Port 1 : IR Port
6	UART2 IR Polarity	IRTX Pin Polarity 0 : Active High 1 : Active Low
7	UART2 IrDA-SIR/ Digital-ASK	Infrared comm. system selection 0 : IrDA-SIR system 1 : Digital-ASK system

5.4.3 Serial port buffers

These serial port signals have the capability to directly drive TTL loads such as those used for modem signals. However, for long-distance transmissions such as those made via RS-232C or RS-422 interfaces, external buffers that satisfy the corresponding standards are necessary.

5.4.4 Infrared Communications

The CARD-686 incorporates an infrared communications function. Simply by connecting an external photoemitter / receiver module, infrared communications become possible. There are two communications protocols: IrDA-SIR-1.0 and Digital ASK. These are selected in the BIOS setup, and for COM B, either of IrDA-SIR-1.0 and Digital ASK can be selected. Figure 5-26 shows the UART configuration.

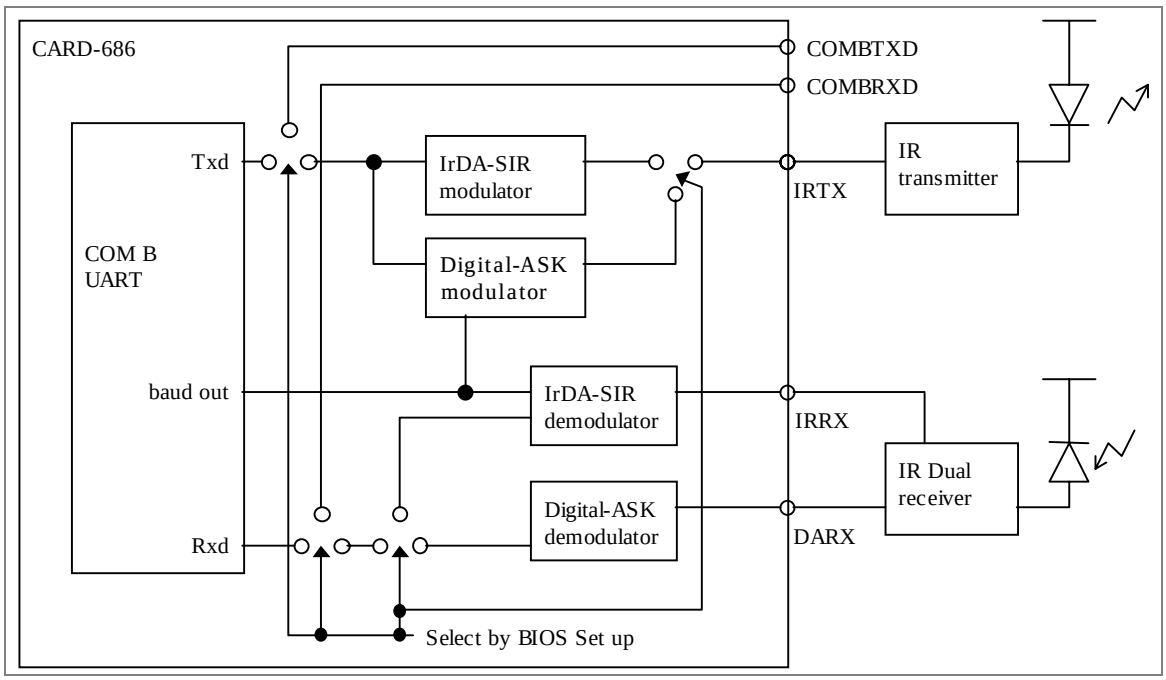

Figure 5-26 COM B UART Diagram

IrDA-SIR-1.0 protocol

Modulation and demodulation in the IrDA-SIR-1.0 standard are as follows.

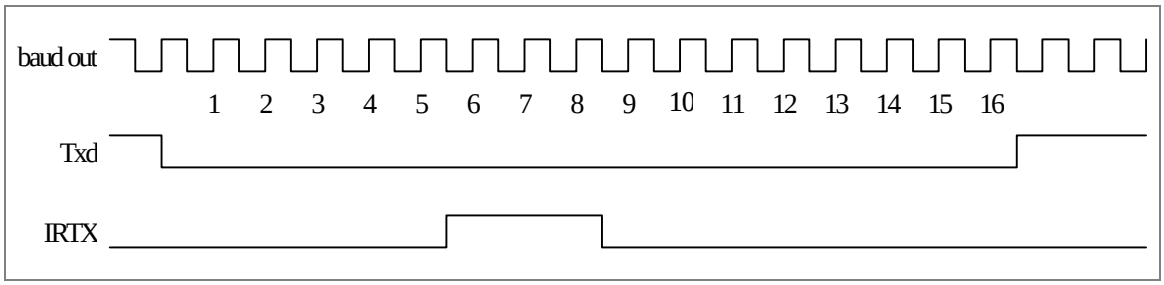

Figure 5-27 IrDA-SIR-1.0 protocol modulation

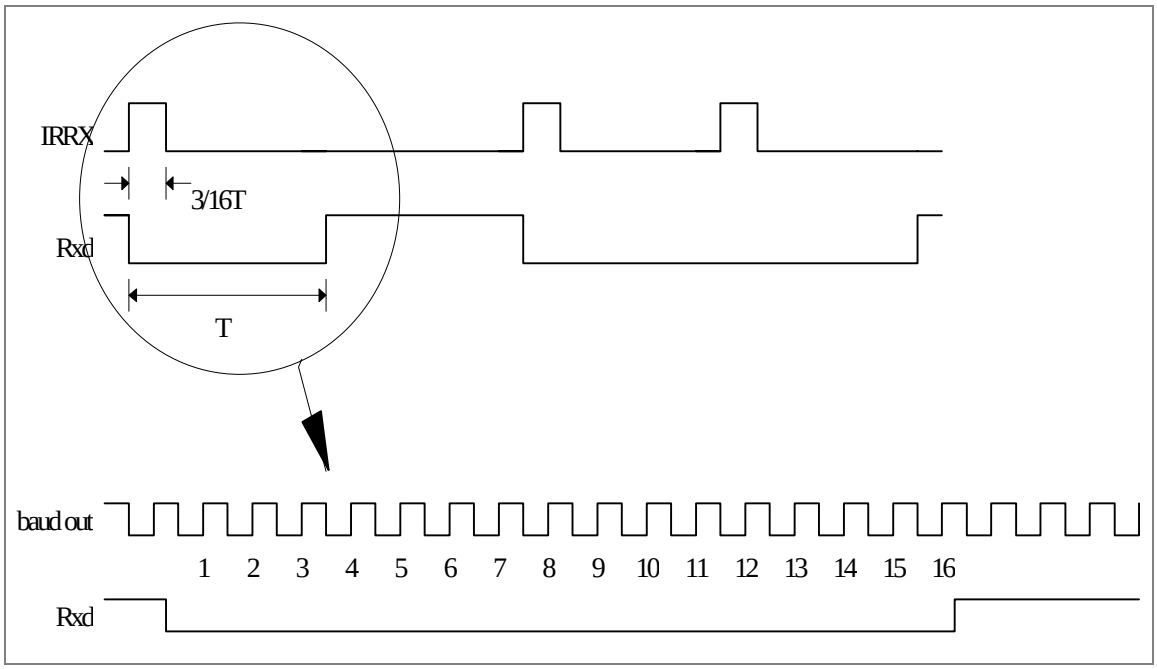

Figure 5-28 IrDA-SIR-1.0 protocol demodulation

Digital ASK protocol

Modulation and demodulation in the Digital ASK protocol are as follows.

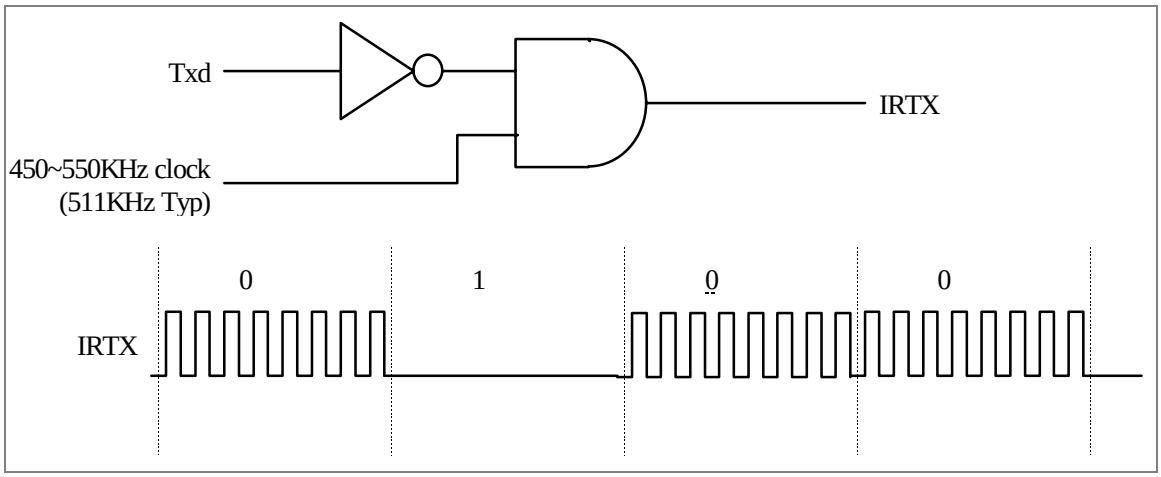

Figure 5-29 Digital-ASK Digital ASK protocol modulation

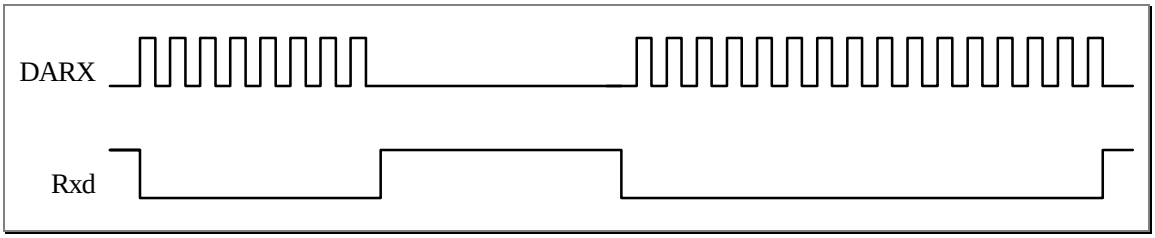

Figure 5-30 Digital-ASK protocol demodulation

5.5 Parallel Port Interface

The following are the features of CARD-686's parallel port interface.

∗Compatible with ISA-style unidirectional parallel ports
∗Supports two ports, LPT1 and LPT2.
∗PS/2-style bidirectional parallel port
∗High-speed parallel port support

5.5.1 Parallel Port Signals

Parallel port control and data signals are shown below.

Control Signals

Line Printer STROBE (LPTSTROBE#)
Used as a data read signal for parallel peripheral devices. In high-speed parallel port mode, this signal is used to indicate the write cycle.

Line Printer Auto Line Feed (LPTAFD#)
When this signal is active, the parallel printer inserts a line feed after every line. In high-speed parallel mode, this signal is used as a data strobe (DS TB#) . This signal can also be used as a data latch signal in write cycles and as a buffer enable signal in read cycles.

Line Printer Busy (LPTBUSY)
This signal indicates that the printer is not ready to accept data from the CARD-686.
In high- speed parallel mode, this is used as a wait signal (WAIT#).

Line Printer Acknowledge (LPTACK#)
This signal indicates that the data transmission is completed and there is a state of readiness for the next transmission. In high-speed parallel mode, this is used as an interrupt signal (INTR#). This input is connected to the interrupt controller.

Line Printer Error (LPTERROR#)
This signal is used by peripheral devices to report errors.

Line Printer Paper End (LPTPE)
This signal is used to indicate that the printer has run out of paper.

Line Printer Initialize (LPTINIT#)
Printer initialization signal.

Line Printer Select In (LPTSLCTIN#)
This signal is used to select the peripheral device currently connected to the port. In high-speed parallel port mode, this signal is used as an address strobe.

Line Printer Selected (LPTSLCT)
This signal is used to select the peripheral device currently connected to the port. In high-speed parallel port mode, this signal is used as an address strobe.

Line Printer Direction (LPTDIR)
This signal is used for directional control for external buffers.

Data Signals

Line Printer Data (LPTD[7:0])

This is a data bus between the CARD-686 and a printer.
This signal is only output in the ISA mode and becomes a bi-directional one in the PS/2 mode.

5.5.2 Parallel port operation

The parallel port signal timing is controlled by software.
The parallel port registers are as follows. In the I/O Address, "x" is 3 for LPT1, and 2 for LPT2.

Table 5-12 Parallel Port Registers

I/O Address	Description
x78h	Parallel Port Data Register
x79h	Parallel Port Status Register Bit7 : 0-Printer Busy BIt6 : 0-Acknowledge Bit5 : 1-Out of paper Bit4 : 1-Printer is selected Bit3 : 0-Error Bits[0-2] : Not Used
x7Ah	Parallel Port Control Register Bits[6-7] Reserved Bit5 : Direction (PS/2 mode only) 1-Read, 0-Write Bit4 : Interrupt enable 1-Enable, 0-Disable Bit3 : Select printer 1-Select Bit2 : Initialize printer 0-Initialize Bit1 : Automatic line feed 1-Automatic Bit0 : Data Strobe
x7Bh	Auto Address Strobe Register
x7Ch	Auto Data Strobe Register
x7Dh	Auto Data Strobe Register
x7Eh	Auto Data Strobe Register
x7Fh	Auto Data Strobe Register

5.5.3 High-speed parallel mode operation

In the high-speed parallel (EPP) mode, printer initialization and selection and error signals are the same as in the normal parallel mode. LPTSLCTIN# and LPTAFD# are automatically generated as data strobe and address strobe signals to the parallel device. LPTSTROBE# is used as a signal indicating the write cycle. For details refer to the BIOS Manual.

5.5.4 Parallel port buffering

The CARD-686 parallel port can drive a low load device without buffering, but basically it is recommended for use with an external buffer connected.
The standard setting of the CARD-686 is for a uni-directional parallel port. Figure 5-31 is an example connection diagram.

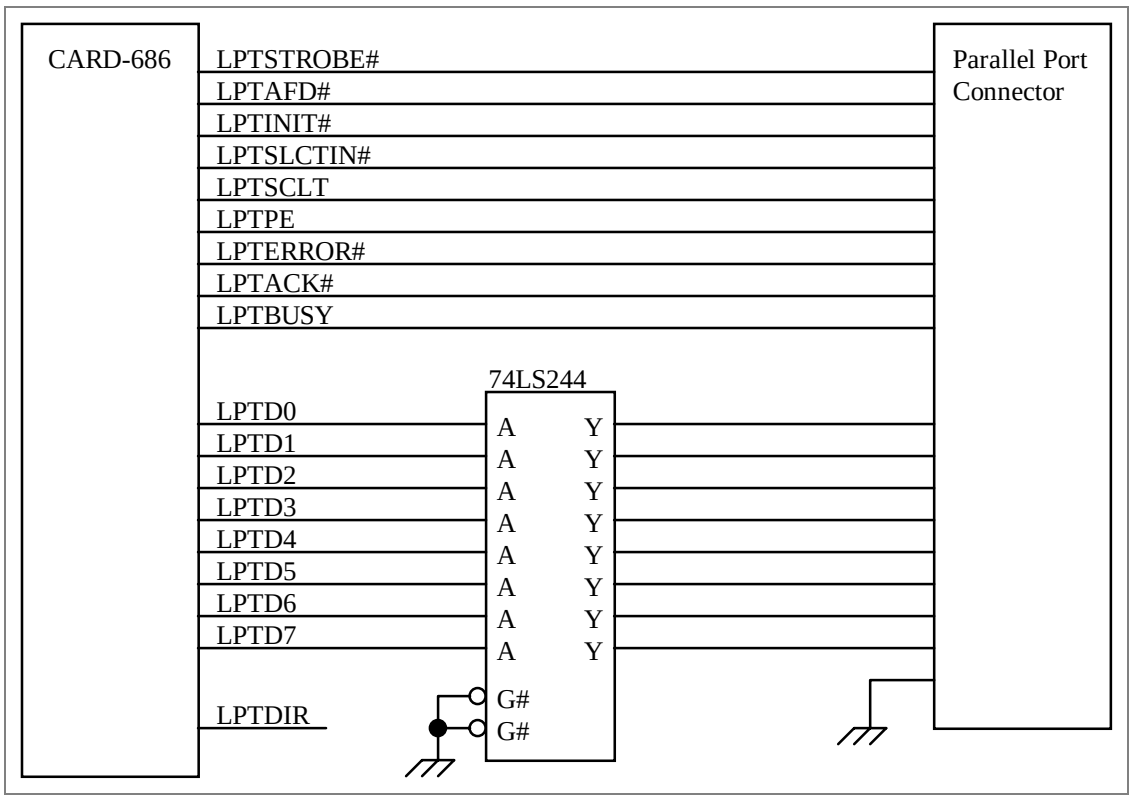

Figure 5-31 ISA Style Unidirectional Parallel Port Interface (with Buffer)

One problem with using an external buffer is that applications that require a key device for the parallel port may not operate.

When operating in PS/2-compatible mode, the port is bi-directional. The connections are illustrated in Figure 5-32. When using an external buffer, use an 74LS245-equivalent, and use LPTDIR# for directional control for the buffer.

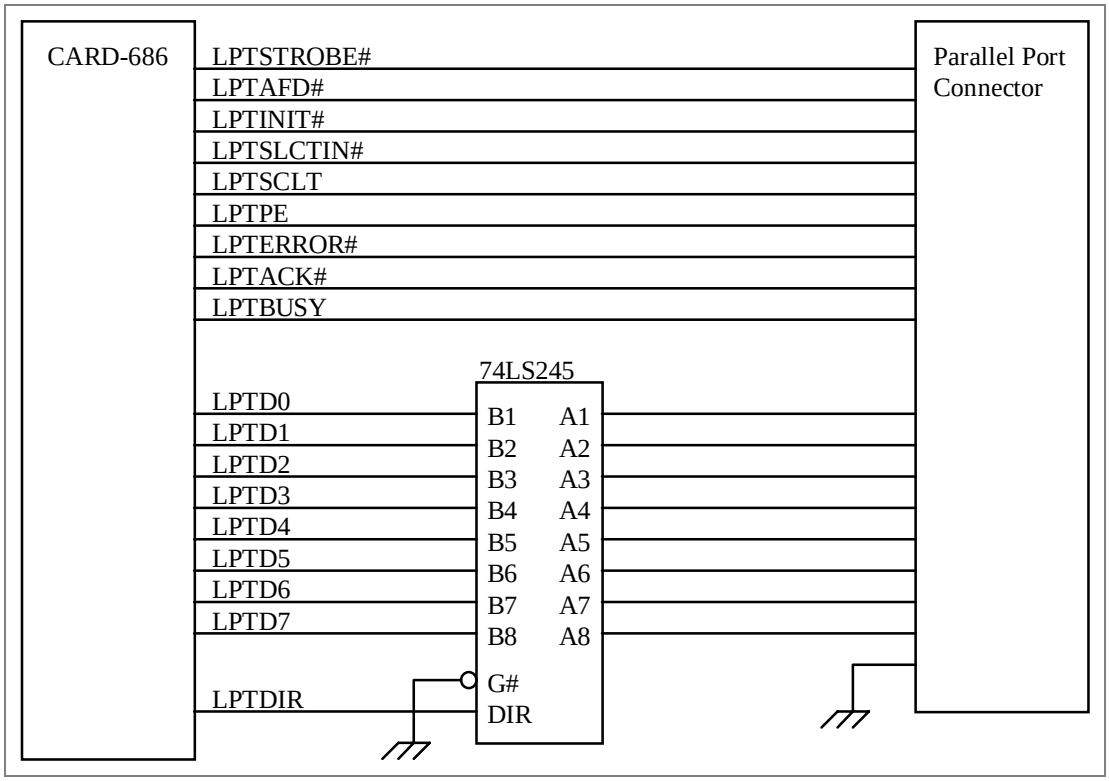

Figure 5-32 PS/2 style bi-directional parallel port interface

Figure 5-33 shows a sample of the circuit without employing the buffer.

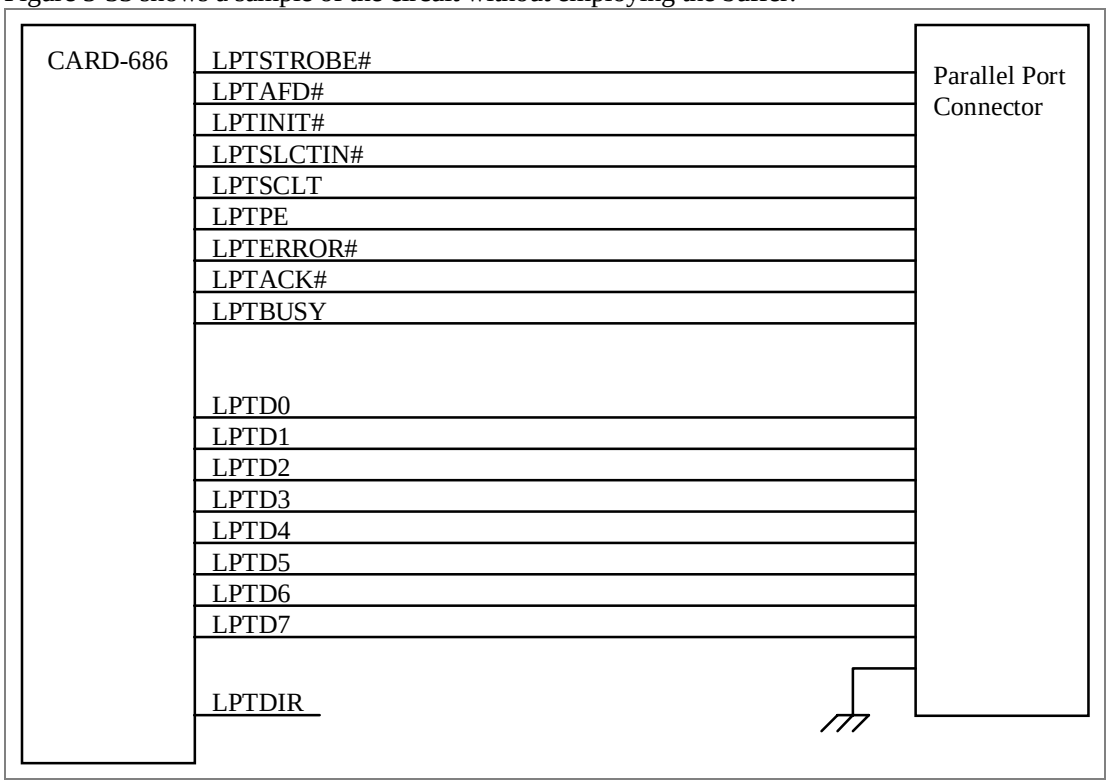

Figure 5-33 ISA Style Simplex Parallel Port Interface

5.5.5 Pin configuration

Table 5-13 shows the pin assignments for ISA parallel port (Standard Mode) and high-speed parallel port mode (EPP Mode).

Table 5-13 25-Pin Connector Pin Assignment

Pin	Standard Mode	EPP Mode	CARD-686
1	STROBE#	WRITE#	LPTSTROBE#
2	PPD0	PPD0	LPTD0
3	PPD1	PPD1	LPTD1
4	PPD2	PPD2	LPTD2
5	PPD3	PPD3	LPTD3
6	PPD4	PPD4	LPTD4
7	PPD5	PPD5	LPTD5
8	PPD6	PPD6	LPTD6
9	PPD7	PPD7	LPTD7
10	ACK#	INTR#	LPTACK#
11	BUSY	WAIT#	LPTBUSY
12	PE	PE	LPTPE
13	SLCT	SLCT	LPTSLCT
14	AFDXT#	DSTRB#	LPTAFD#
15	ERROR#	ERROR#	LPTERROR#
16	INIT#	INIT#	LPTINIT#
17	SLCTIN#	ADSTB#	LPTSLCTIN#
18	GND	GND	
19	GND	GND	
20	GND	GND	
21	GND	GND	
22	GND	GND	
23	GND	GND	
24	GND	GND	
25	GND	GND	

5.6 Power Management

CARD-686 supports power management functions. The features of this system are:

∗Suspend, resume function
∗Support for suspend/resume button
∗Suspend timer possible
∗Support for output pins for programmable system power management
∗Support for battery monitor pin

5.6.1 Power management signals

System Management Output (SMOUT[3:0])
These signals activate the idle state of various devices for power control.

Suspend Status (SUSSTAT#)
This signal indicates that CARD-686 is in the suspended state. This signal can also be used as a power supply control signal.

External System Management (EXTSMI#)
This signal is used to request a system management interrupt from CARD-686.

Suspend Resume Button (SRBTN#)
This input signal is used to enter the suspended state and to wake up from the suspended state.

Battery Warning (BATWARN#)
This input signal is used to warn when the battery's remaining capacity is low.
When this warning is issued, a warning beep is sounded by the speaker interface.

Battery Low (BATLOW#)
When this signal goes active (when the battery capacity has dropped), CARD-686 either issues a warning or enters the suspended state.

POWERGOOD (POWERGOOD)
This signal indicates that the system power supply is normal. It is necessary to make this signal active when the system supply voltage is within the specified range. For the timing rule, see the Chapter of "AC Characteristic."

For further details on power management, refer to the BIOS Manual.

5.6.2 Suspend and resume control

The CARD-686 supports functions to suspend the system, and thereafter to resume, that is, to return to the state immediately before the suspension. The suspend function puts all the CARD-686 devices in the power save mode, and maintains the system in a low power consumption state.

When detecting a fall edge of the terminal SRBTN#, the CARD-686 gets into the suspended state. Also, it gets into the suspended state when detecting a low battery (when BATLOW# becomes active) or according to suspend request of a software.

If resumed, the CARD-686 will return to the state just before the suspension.
The following three resuming methods are available:

1. When a fall edge of the terminal SRBTN# is detected.
2. When a fall edge of the terminal COMARI# or COMBRI# is detected.
3. When a set time has come.

When BATLOW# is active even after the CARD-686 gets into any of the above states, however, the CARD-686 does not resume.

For the details of suspend/resume, refer to the BIOS Manual.

Figure 5-34 shows the block diagram of the suspend/resume circuit.

The MAIN-BATTERY supplies power to the CARD-686. When the system gets into the suspended state, the system stops supplying power to other than the CARD-686. At the time, the CARD-686 gets into the suspended state and the contents of the DRAM, the video memory and the registers are maintained by little power. The signal POWERGOOD indicates the states of the power supplies (V_{CC5} and V_{CC3}) and is input to the CARD-686. Also, the signal BATWARN# and BATLOW# are input to the CARD-686 for monitoring the system power supply. When BATLOW# becomes active while the system is operating, the system warns through the speaker that the battery capacity has become low. When this signal is inactive, the CARD-686 does not resume. It starts resuming when the RTC alarm, modem ring and SRBTN# signals are input. When the CARD-686 resumes, SUSSTAT# returns to HIGH.

Figure 5-34 is a block diagram of the suspend/resume circuit.

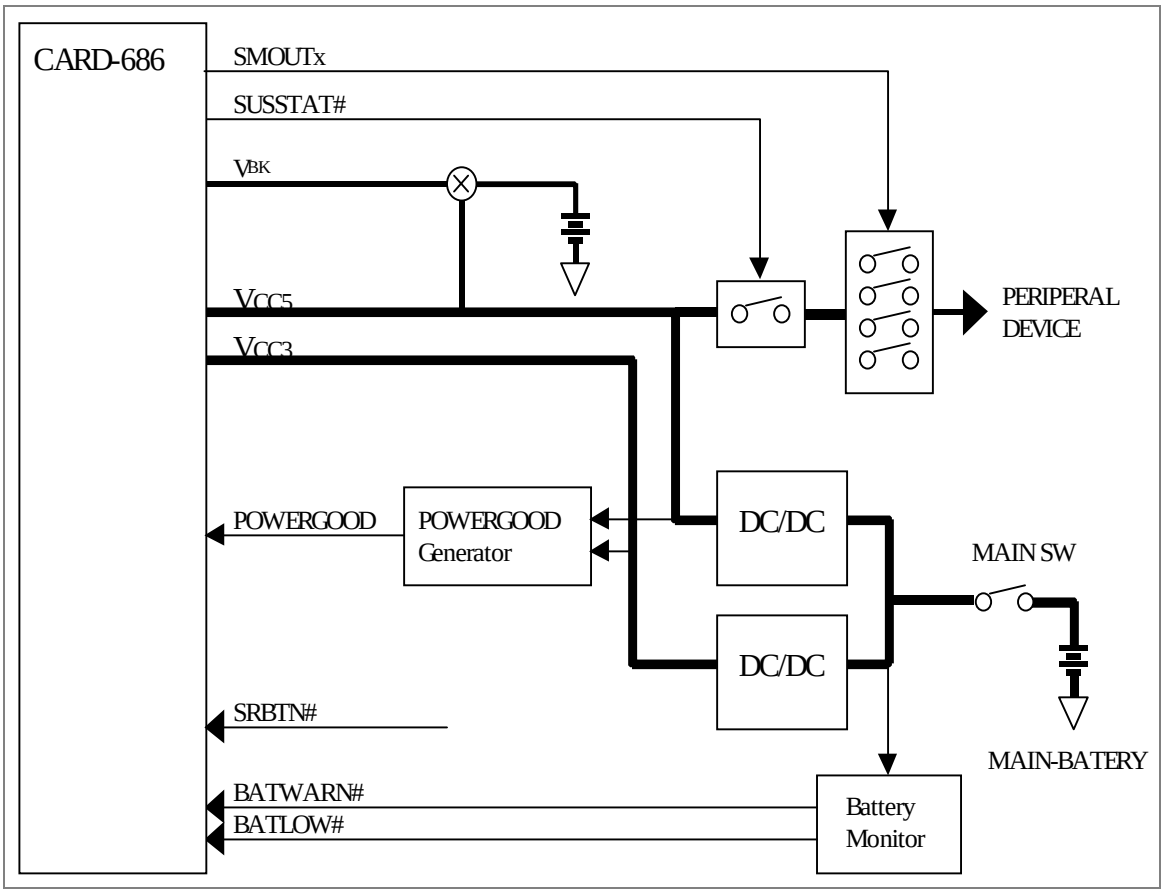

Figure 5-33 Suspend/Resume Block Diagram

5.6.3 SMOUT

The CARD-686 controls devices as follows using signals SMOUT0 to 3:

SMOUT0 Controls COM A.
Since SMOUT0 becomes low when COM A is in the standby state or when the CARD-686 is in the suspended state, it can bring the Driver/Receiver IC of the RS-232C to the standby state.

SMOUT1 Controls COM B.
Since SMOUT1 becomes low when COM B is in the standby state or when the CARD-686 is in the suspended state, it can bring the Driver/Receiver IC of the RS-232C to the standby state.

SMOUT2 Controls HDD.
When the CARD-686 brings the HDD to the standby state or is suspended, SMOUT2 becomes Low. The CARD-686 can turn off the power of the HDD using SMOUT2.
Lots of signals are commonly used for the HDD and the ISA bus. Keep it in mind that, if these signals are not isolated when the power supply of the HDD is turned off, the CARD-686 will malfunction.

SMOUT3 SMOUT3 is used to change the voltage of the power supply (PGM) for updating the Flash ROM (BIOS).

These signals are for the standard BIOS of the CARD-686. If the BIOS is changed, the CARD-686 can also control other devices. These SMOUTs can be used as general purpose output ports instead of for power control.

5.7 Keyboard Controller

The CARD-686 keyboard controller is emulated in software, to be function-compatible with an 8042. Its principal functions are as follows:

∗AT-and PS/2-compatible standard command support
∗Standard AT and PS/2 keyboard support
∗PS/2-compatible mouse support

5.7.1 Keyboard controller signals

Keyboard Clock (KBCLK)
Clock signal for the keyboard interface

Keyboard Data (KBDATA)
Data signals for the keyboard interface

Mouse Clock (MSCLK)
Clock signal for the mouse interface

Mouse Data (MSDATA)
Data signals for the mouse interface

5.7.2 Explanation of registers and commands

The register and commands are briefly described below.

Status Register 064h (Read Only)
This register shows the status of the keyboard controller.

Table 5-14 Status Register

Bit	
7	Parity Error Flag
6	General Time Out
5	Aux. Data Flag
4	Keyboard Password Unlocked
3	Command Flag
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Output Buffer 060h (Read Only)
Port for outputting scan codes received by this controller from the keyboard.

Input Buffer 060h (Write Only)
Port for data input to this controller.

Command Register 064h (Write Only)

Port for command output to this controller. The following commands are supported:

Standard Keyboard Commands

Set/Reset Status Indicators Command	(EDh)
Echo Command	(EEh)
Select Alternate Scan Code Command	(F0h)
Read ID Command	(F2h)
Set Typematic Rate/Delay Command	(F3h)
Enable Command	(F4h)
Default Disable Command	(F5h)
Set Default Command	(F6h)
Set Keys Command	(F7h-FDh)
Reset Command	(FFh)

Standard Controller Command

Write Controller Command Byte	(60h)
Read Controller Command Byte	(20h)
Test Password Installed	(A4h)
Load Password	(A5h)
Enable Password	(A6h)
Disable Auxiliary Device Interface	(A7h)
Enable Auxiliary Device Interface	(A8h)
Test Auxiliary Device Interface	(A9h)
Self Test	(AAh)
Keyboard Interface Test	(ABh)
Disable Keyboard Interface	(ADh)
Enable Keyboard Interface	(AEh)
* Read Input Port	(C0h)
* Read Output Port	(D0h)
* Write Output Port	(D1h)
Write Keyboard Output Buffer	(D2h)
Write Auxiliary Output Buffer	(D3h)
Write Auxiliary Device Command	(D4h)
* Read Test Input Command	(E0h)
Pulse System Reset	(FEh)

*In the Read Input Port (0C0h) command, the value returned is not a physical input port value, but an emulated value. The Read Output Port (0D0h) command also returns not a physical input port value, but an emulated value. All that can be changed by Write Output Port (0D1h) is bit 1, Gate A20 control, and other bits are ignored. In the Read Test Input Command (0E0h) command, the value returned is not a physical Test Input Port value, but an emulated value.

5.7.3 Keyboard and mouse interface

Figure 5-35 illustrates the keyboard and mouse interfaces.

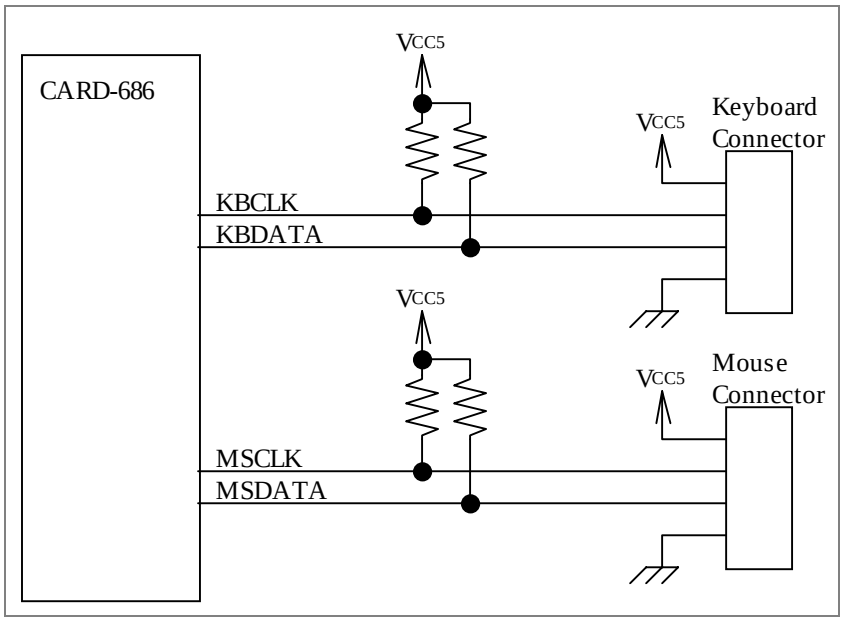

Figure 5-34shows the keyboard and mouse interface.

Check the keyboard and mouse specifications before determining the external resistance value.

5.8 VGA Controller

The CARD-686 is equipped with an Seiko Epson SPC8110 as display controller.
The following are some of its features:

∗Standard VGA mode support
∗Simultaneous CRT and LCD display
∗Suspend function support
∗256/256K color display
∗Monochrome STN-LCD 64 gray level display
∗Color STN-LCD support
∗256K-color TFT color LCD support
∗Direct CRT and LCD connection possible

For the video mode supported by the CARD-686, refer to the BIOS Manual.

5.8.1 CRT and LCD interface signals

CARD-686 is equipped with a CRT interface and an LCD interface.
The signals used in these interfaces are described below.

CRT interface signals

HORIZONTAL SYNC (HSYNC)
Horizontal synchronization signal for the monitor

VERTICAL SYNC (VSYNC)
Vertical synchronization signal for the monitor

RED VIDEO (RED)
This analog output supplies current corresponding to the red pixels to be displayed.

GREEN VIDEO (GREEN)
This analog output supplies current corresponding to the green pixels to be displayed.

BLUE VIDEO (BLUE)
This analog output supplies current corresponding to the blue pixels to be displayed.

LCD interface signals

Flat Panel Vertical Timing (FPVTIM)
Indicates the start of a new frame for a flat panel display.

Flat Panel Horizontal Timing (FPHTIM)
This signal advances the row shift register for an LCD panel display.

Flat Panel Blank (FPBLANK#)
This signal indicates the blanking interval in which data should not be displayed on a TFT LCD panel. This controls the display enable signal for a TFT LCD panel.

Flat Panel Dot Clock (FPDOTCLK)
Dot shift clock for a flat panel display.

Extend Panel Dot Clock (EXDOTCLK)
This is a special LCD panel dot clock, which is normally not used.

Flat Panel Data (LD[17:0])
Display data for a flat panel display.

Flat Panel V_{CC} On (FPVCCON)
This signal controls the LCD panel logic power supply, and is used together with FPVEEON. This is used to power the panel on and off.

Flat Panel V_{EE} On (FPVEEON)
This signal controls the LCD panel drive power supply, and is used together with FPVCCON. This is used to power the panel on and off.

5.8.2 Panel interface

A representative example of the connections between CARD-686 and a dual-scan monochrome monitor is shown below.

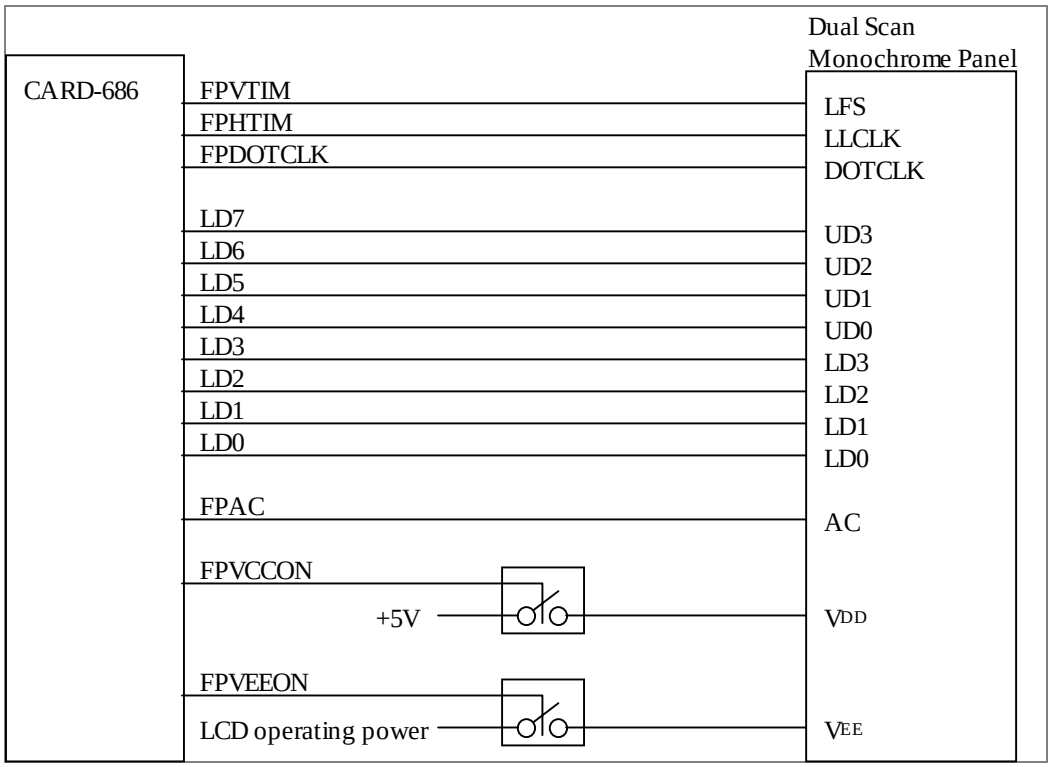

Figure 5-36 Dual-scan Monochrome Panel Connection Sample

The following description covers the principal panel interfaces supported by CARD-686.

● 640x480 Monochrome Dual Panel (8 bit)

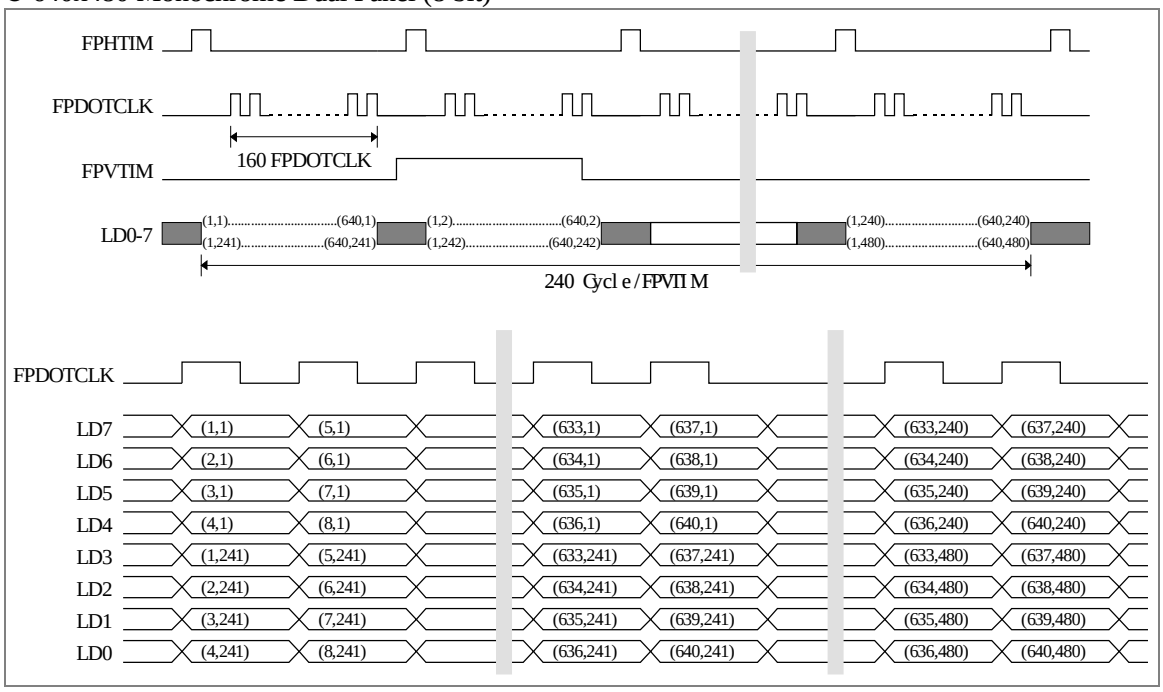

Figure 5-35 8 bit Monochrome Dual Panel Interface

● 640x480 Single Monochrome Panel (8 bit)

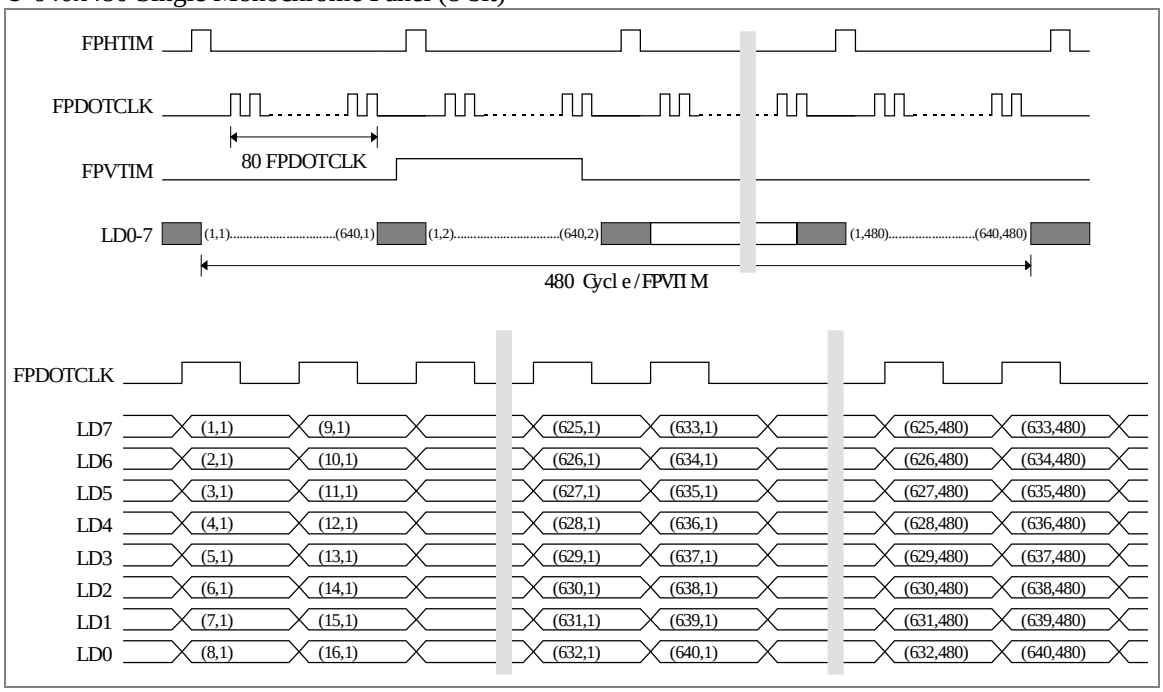

Figure 5-36 8 bit Monochrome Single Panel Interface

●640×480 TFT color panel

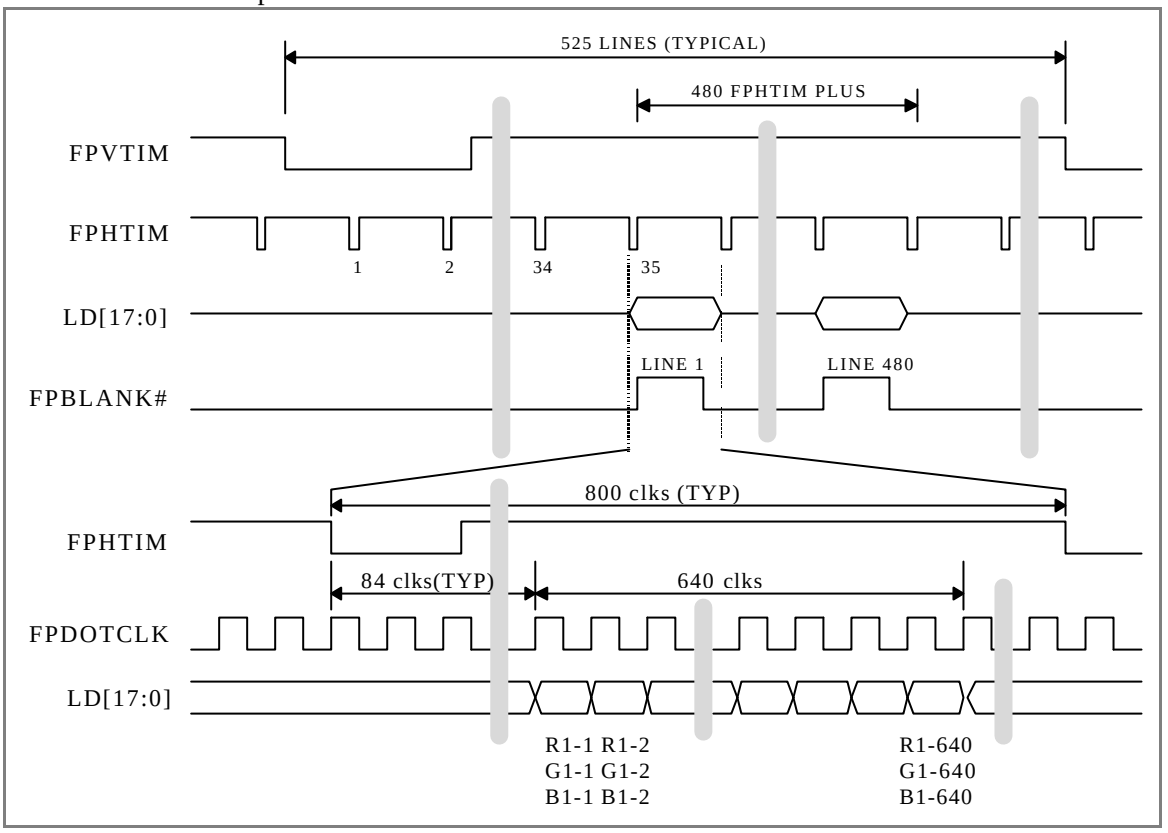

Figure 5-37 TFT Panel Interface

The LCD panel requires special control with respect to the logic power supply, liquid crystal drive power supply, and control signals. The CARD-686 to meet these requirements controls these signals as shown in Figure 5-38.

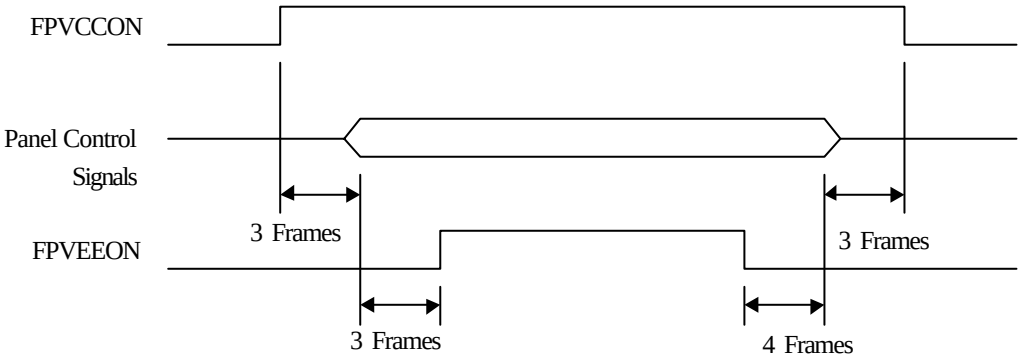

Figure 5-38 Panel Power Control Timing

The panel connections differ according to the manufacturer of the panel and according to the panel settings. Therefore, it is necessary to check the specific connection requirements of the panel to be used.

5.9 Floppy Disk Controller

CARD-686 is equipped with an IBM PC/AT-compatible floppy disk controller.
The features of the FDD interface are:

∗Permits connection with up to two drives
∗Supports both 5-inch and 3.5-inch FDDs
∗Supports transfer rates of 250Kbps, 300Kbps, and 500Kbps
∗Built-in driver/receiver for the drives (drive current I_{OL}=38mA)

5.9.1 Floppy disk control signals

DRIVE SELECT 1 (FDDS1#)
Drive 1 select signal.

DRIVE SELECT 2 (FDDS2#)
Drive 2 select signal.

MOTOR ON 1 (FDMT1#)
"Motor on" signal for drive 1.

MOTOR ON 2 (FDMT2#)
"Motor on" signal for drive 2.

STEP (FDSTEP#)
Step pulse signal that indicates the number of steps the head is to move.

DIRECTION (FDDIR)
This signal indicates the direction of a seek operation. LOW indicates the seek is towards the inner track, and HIGH indicates that the seek is towards the outer track.

SIDE (FDSIDE)
This signal selects head 0 or head 1. LOW selects head 1, HIGH selects head 0.

READ DATA (FDRD#)
Input for data read from the drive.

WRITE DATA (FDWD#)
Output for data to be written to the drive.

WRITE ENABLE (FDWE#)
This signal instructs the drive to write

WRITE PROTECT (FDWP#)
This signal from the drive indicates that the media is write-protected.

DISK CHANGE (FDDCHG#)
Disk change signal from the drive.

INDEX (FDINDEX#)
Drive index detection signal.

TRACK 0 (FDTRK0#)
This signal indicates that the head is positioned at track 0.

HIGH DENSITY SELECT (FDHIDEN)
When this signal is high it indicates high density.

5.9.2 Floppy disk interface

Floppy Disk Interface I/O Ports

Table 5-15 FDC I/O Port

I/O Address	Description
3F2h WO	Digital output Register Bit7 : Reserved Bit6 : Reserved Bit5 : Drive 2 Motor Enable Bit4 : Drive 1 Motor Enable Bit3 Enable Diskette Interrupt and DMA Bit2 : Diskette Function Reset Bit1 : Reserved Bit0 : Drive Select 0-Drive1, 1-Drive2
3F4h	FDC Main Status Register
3F5h	FDC Data Register
3F7h WO	FDD Control Register Bit 1 Bit 0 0 0 500 Kbps 0 1 300 Kbps 1 0 250 Kbps 1 1 reserved
3F7h RO	Digital Input Register Bit7 : Diskette Change Bits[0-6] : Hard Disk Controller

A typical connection example for a floppy disk drive is shown in Figure 5-41.

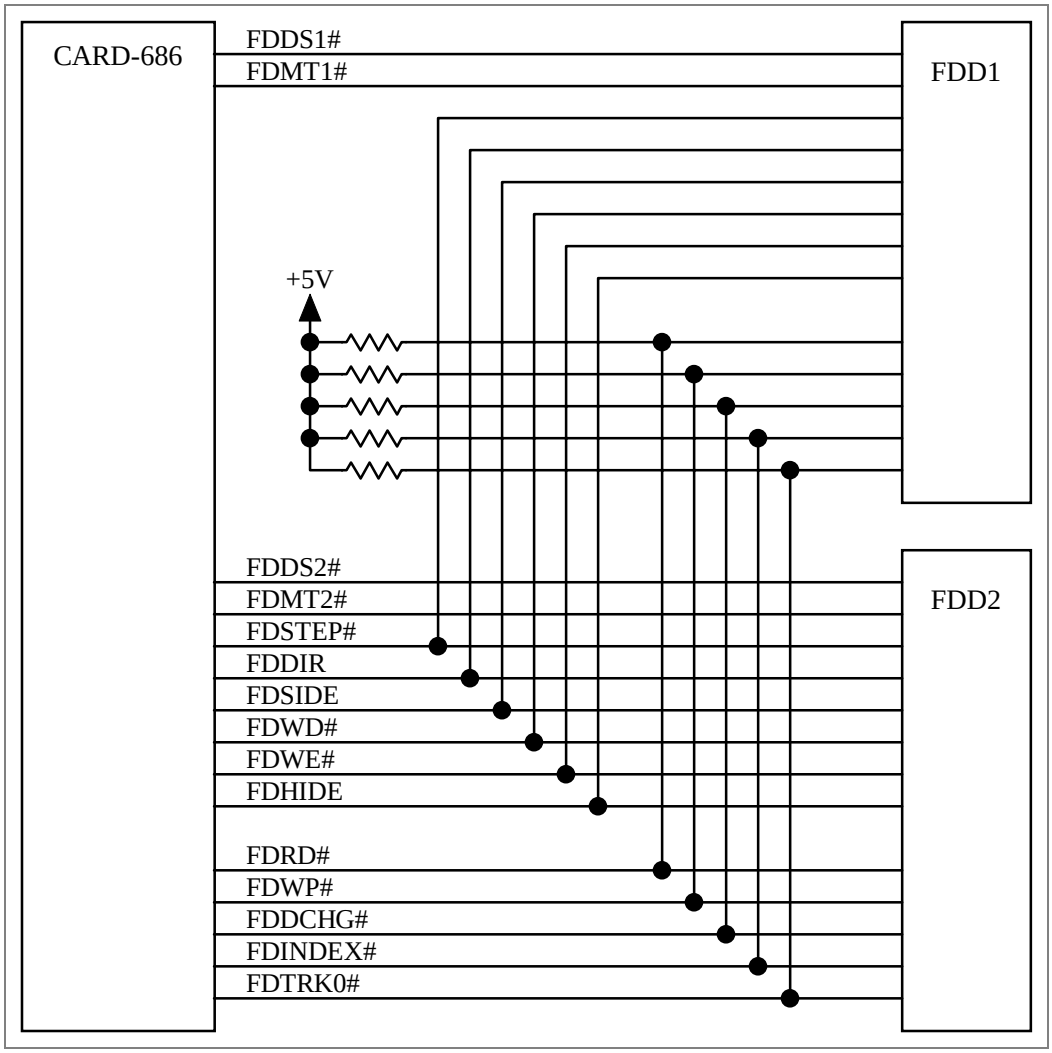

Figure 5-39 Floppy Disk Drive Connection Sample

Set the external resistance according to the characteristics of the floppy disk drive.

5.10 RTC/CMOS RAM

CARD-686 has a built-in RTC (for clock and calendar functions) and CMOS RAM that can be backed up. Because this interface (V_{BK}) is provided with pins for backing up the RTC and CMOS RAM, it is necessary to supply power form a battery or other source when providing backup. When this is not used, the BIOS is used to save the contents of CMOS memory. For details, refer to the BIOS Manual.

5.10.1 Register description

CARD-686 is equipped with an ISA standard RTC (MC146818). The contents of the RTC can be preserved even when power is not supplied to the system, as long as power is supplied to the V_{BK} pin.

The CMOS RAM built into the CARD-686 stores information required for booting the CARD-686. When the CARD-686 is booted, expansion devices and system settings are set based on this information. Since with the standard BIOS V_{BK} is not backed up, standard information is always used for booting. As a result, when used in a system configuration other than the standard system configuration, unless a backup power supply is connected to V_{BK}, each time the system is booted it will be necessary to make the configuration settings. If, however, the ROM Adaptation Kit is used to change the standard BIOS settings, a backup is not required, but it will be necessary to reset the real time clock each time.

The CMOS RAM includes 128 bytes of information, including 10 bytes for second, minute, hour, day-of-the-week, day, month, and year, and 4 bytes of control data.
The address map for standard CMOS RAM is shown in the following table.

Table 5-16 RTC/CMOS RAM Register

Index	Register
00h	seconds
01h	seconds (alarm)
02h	minutes
03h	minutes (alarm)
04h	hours
05h	hours (alarm)
06h	day of week
07h	day
08h	month
09h	year
0Ah	Control Register A
0Bh	Control Register B
0Ch	Control Register C
0Dh	Control Register D
0Eh-7Fh	Data Area

The RTC and the CMOS RAM are accessed through the Index port (I/O Address 70h) and the Data port (I/O Address 71h).

Table 5-17 RTC/CMOS RAM I/O Port

I/O Address	R/W	Description
0070h	RO	RTC/CMOS RAM Index port Bit 7 = NMI Mask 1- NMI Disable, 0- NMI Enable Bit 0-6 = RTC/CMOS RAM Index
0071h	R/W	RTC/CMOS RAM Data port

5.10.2 About V_{BK}

This pin is provided for backup for the real time clock, CMOS RAM. When power is supplied to the CARD-686 (in operation), the same power supply as V_{CC5} is supplied. For CMOS RAM backup, it is necessary to switch to a backup power supply (lithium battery etc.) in coordination with the CARD-686 power off timing.

An example circuit for switching the power supply is shown in Figure 5-42.

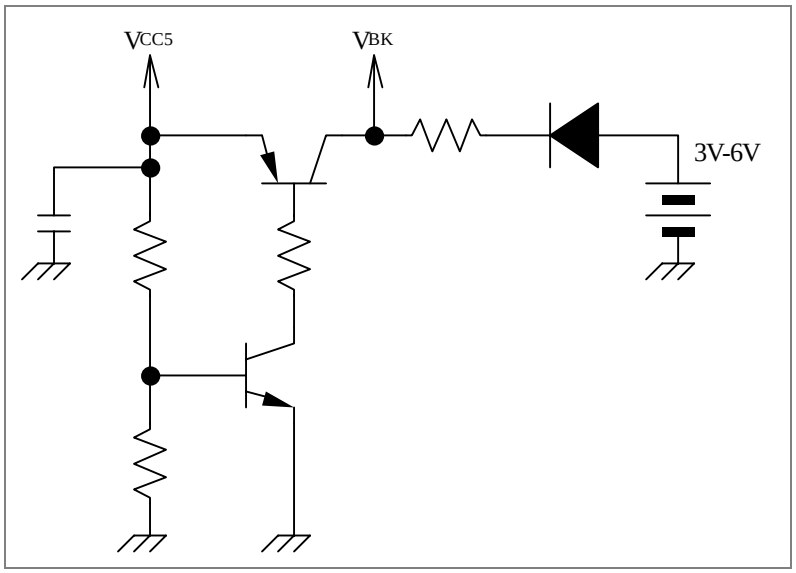

Figure 5-40 Example V_{BK} Power Supply Switching Circuit

5.10.3 POWERGOOD

POWERGOOD is also used to separate the RTC and the CMOS RAM electrically from other circuits. So, if POWERGOOD becomes "HIGH" before V_{BK} is switched from the backup power supply to V_{CC5}, the contents of the RTC and the CMOS RAM may be destroyed. When V_{BK} is powered from the backup power supply, keep POWERGOOD below 0.8V.

5.11 Output of General Purpose Timer (Watchdog Timer)

A general purpose timer which can be used as watchdog timer is readily available for the CARD-686. This timer used Channel 1 of the extension timer 8254 with the standard clock of 4KHz, and OUT1 is output to the WDTIM# terminal of the CARD-686.

The watchdog timer is used as follows on the CARD-686:

1. For setting timers.
2. For resetting timers before time-out of an application software and for re-starting them.
3. If timers are not reset and come to time-out due to runaway of software, WDTIM# will become active.

Since using the watchdog time in this way, the CARD-686 has the following BIOS functions:

To get into the watchdog timer state.
To acquire protect mode interface routine address.
To set and start or reset timers.
(For the details, refer to the BIOS Manual.)

The WDTIM# state is "HIGH" in general and become "low" at a time-out. The measures to be taken in case of time-out depend on the external circuit of the CARD-686.

6. ENVIRONMENTAL REQUIREMENTS

6.1 Temperature

Operating (during use)	Tc = 0~85°C	
Storage	Ta = -20~85°C	(non-condensating)

Tc: Case Temperature (see Figure 6-1)
Ta: Ambient Temperature

6.2 Humidity

Storage	0~90%	(non-condensating)

6.3 Electrostatic Breakdown Immunity

15 kV at 100 pF, 1.5 kΩ(sustainable without damage)

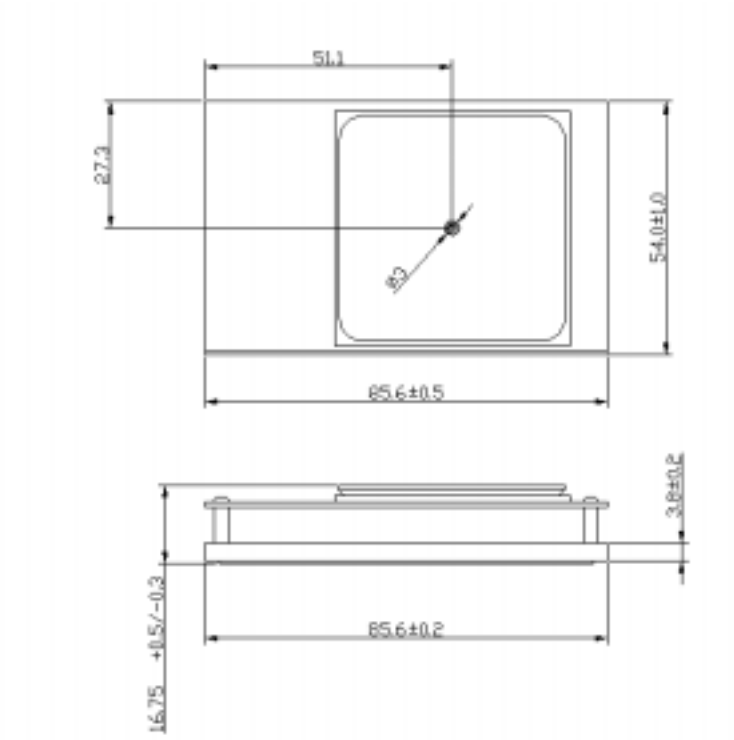

Figure 6-1 Operating Case Temperature Measurement Point (center of case surface K6-2)

7. MECHANICAL CHARACTERISTICS

7.1 Insertion and Removal Force

Insertion Force	98.0 N or less	(10 kg or less)
Removal Force	9.8 N or more	(1 kg or more)

7.2 Insertions and Removals

1000 operations (using dedicated connector)

8. DC CHARACTERISTICS (RECOMMENDED AND NOMINAL)

Power Section

Symbol	Parameter	Min.	Max.	Unit	Note
V_{CC5}	Supply Voltage	4.75	5.25	V	Indicated in the pin assignment diagram as V_{CC5}
V_{CC3}	Supply Voltage	3.15	3.6	V	Indicated in the pin assignment diagram as V_{CC3}
V_{BK}	Supply Voltage	2.5	---	V	When the RTC is backed up. In normal operation the same as V_{CC5}
V_{PGM}	Supply Voltage	0	6.5	V	When FLASH ROM (BIOS) is read
		11.4	12.6	V	When FLASH ROM (BIOS) is written. Supply power to VPGM after V_{CC5} and V_{CC3} is fixed. I=30mA (Max)

POWERGOOD Signal

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	---	0.8	V	When the RTC is backed up, the voltage shall not exceed 0.8V.
V_{IH}	Input High Voltage	4.0	V_{CC5}+0.3	V	

ISA Bus Interface Section

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=12mA	---	0.4	V	Applies to IRQ6, DRQ2.
V_{OH}	Output High Voltage I_{OH}=-2mA	4.0	---	V	Applies to IRQ6, DRQ2.
V_{OL}	Output Low Voltage I_{OL}=8mA	---	0.4	V	Applies to DACK0#, 1#, 3#, 5#, 6#, 7# and IRQ3, 4, 5, 7, 10, 11, 12.
V_{OH}	Output High Voltage I_{OH}=-8mA	2.4	---	V	Applies to DACK0#, 1#, 3#, 5#, 6#, 7# and IRQ3, 4, 5, 7, 10, 11, 12.
V_{OL}	Output Low Voltage I_{OL}=12mA	---	0.4	V	
V_{OH}	Output Low Voltage I_{OH}=2mA	2.4		V	Applies to SD[15:0], LA[23:17], SA[19:0], SBHE#, BALE, AEN, MEMR#, MEMW#, IOR#, IOW# and RESETDRV.
V_{OH}	Output High Voltage I_{OH}=-12mA	2.4	---	V	
V_{OL}	Output Low Voltage I_{OL}=12mA Open Drain Output		0.4	V	Applied to IOCHRDY pin and REF#.

Serial Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=8mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-8mA	2.4	---	V	
V_{OL}	Output Low Voltage I_{OL}=24mA	---	0.4	V	Applies to IRTXD pin
V_{OH}	Output High Voltage I_{OH}=-12mA	2.4	---	V	Applies to IRTXD pin

Parallel Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=8mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-8mA	2.4	---	V	
V_{OL}	Output Low Voltage I_{OL}=12mA Open Drain Output	---	0.4	V	Applies to LPTSTROBE#, LPTAFD#, LPTINIT#, LPTSLCTIN#

Floppy Disk Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=38mA Open Drain Output	---	0.4	V	

LCD Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{OL}	Output Low Voltage I_{OL}=24mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-8mA	4.0	---	V	
V_{OL}	Output Low Voltage I_{OL}=6mA	---	0.4	V	Applies to FPVCCON and FPVEEON.
V_{OH}	Output High Voltage I_{OH}=-2mA	4.0	---	V	Applies to FPVCCON and FPVEEON.

Mouse and Keyboard Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.6	V	
V_{IH}	Input High Voltage	2.4	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=24mA Open drain output	---	0.4	V	

IDE Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=12mA	---	0.4	V	Applies to HD7, HDCS0# and HDCS1#.
V_{OH}	Output High Voltage I_{OH}=-12mA	2.4	---	V	Applies to HD7, HDCS0# and HDCS1#.
V_{OL}	Output Low Voltage I_{OL}=4mA	---	0.4	V	Applies to HDIR, HDENL# and HDENH#.
V_{OH}	Output High Voltage I_{OH}=-4mA	2.4	---	V	Applies to HDIR, HDENL# and HDENH#.

Power Management Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.6	V	
V_{IH}	Input High Voltage	2.4	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=8mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-8mA	2.4	---	V	

Speaker Interface
OM Update Interface
Watchdog Timer Interface

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC5}+0.3	V	
V_{OL}	Output Low Voltage I_{OL}=4mA	---	0.4	V	
V_{OH}	Output High Voltage I_{OH}=-4mA	2.4	---	V	

Current Consumption

SCE8663802 (32MB DRAM) Tc=0 to 85°C

Item	Condition	Specification			Unit
		Min.	Typ.	Max.	
Operating current consumption I_{CC3}	When operating (MS-DOS prompt) V_{CC3}=3.15V to 3.6V	----	430	650	mA
Operating current consumption I_{CC5}	When operating (MS-DOS prompt) V_{CC5}=5V±5%	----	1250	2000	mA
Current in suspended state I_{CC3}	In suspended state V_{CC3}=3.15V to 3.6V	----	70	150	mA
Current in suspended state I_{CC5}	In suspended state V_{CC5}=5V±5%	----	40	100	mA
Backup current I_{BK}	During backup V_{BK}=3.0V	----	3	15	µA

SCE8663803 (64MB DRAM) Tc=0 to 85°C

Item	Condition	Specification			Unit
		Min.	Typ.	Max.	
Operating Current I_{CC3}	Operating(MS-DOS prompt) V_{CC3}=3.15V to 3.6V	----	430	650	mA
Operating Current I_{CC5}	Operating(MS-DOS prompt) V_{CC5}=5V±5%	----	1250	2000	mA
Suspend Current I_{CC3}	During Suspend V_{CC3}=3.15V to 3.6V	----	72	150	mA
Suspend Current I_{CC5}	During Suspend V_{CC5}=5V±5%	----	40	100	mA
Backup Current I_{BK}	During Backup V_{BK}=3.0V	----	3	15	µA

9. PIN ELECTRICAL CHARACTERISTICS

This section describes the characteristics of each pin in CARD-686.
The following table describes the meanings of the entries in the columns under the various legends.

Type	Indicates the pin type I : Input O : V_{CC5}-level output O3 : V_{CC3}-level output (5V maximum) O OD : V_{CC5}-level open drain output O3 OD : V_{CC3}-level open drain output (5V maximum) IO : V_{CC5}-level output, bi-directional IO3 : V_{CC3}-level output, bi-directional (5V maximum) IO3/5 : mixed V_{CC3}/V_{CC5}-level bi-directional (max. V_{CC5} level input) IO OD : V_{CC5}-level bi-directional, open drain output IO3 OD : V_{CC3}-level bi-directional, open drain output (max. V_{CC5} level input) POWER : Power supply
Termination	Internal termination resistance and termination method: HOLD : With bus holder ??PU : ??-Ω pull-up resistance (to V_{CC5}) ??PD : ?? Ω Pull-down resistance. ??ST : Through ??Q damping resistance External : External termination is required
Drive rive	Drive current (mA) for output and bi-directional termination. Denoted I_{OL} and I_{OH} .
Suspend	Indicates pin state during Suspend mode. This is valid in the system power management functions. Drive : "HIGH" or "LOW" is output. Drv (0) : "LOW" is output. Drv (1) : “HIGH” is output High-Z : High-impedance Active : Input status. These terminals affect operations of the CARD-686. Input : Enter "HIGH" or "LOW" external to the CARD-686 to determine the input level. However, this operation is not necessary when the bus holder, pull-up resistor or pull-down resistor is provided Input (1) : : "HIGH" need be input

Signal Characteristics

Pin	Group (EASI)	Signal name	Type	Termination	Drive (mA) Iol, Ioh	Suspend
1	Power Supply	GND	POWER	---	---	---
2		GND	POWER	---	---	---
3	LCD I/F	EXDOTCLK	O	---	24, -8	Drv (0)
4		LD6	O	---	24, -8	Drv (0)
5		LD4	O	---	24, -8	Drv (0)
6		LD2	O	---	24, -8	Drv (0)
7		LD0	O	---	24, -8	Drv (0)
8		FPVTIM	O	---	24, -8	Drv (0)
9		FPAC	O	---	24, -8	Drv (0)
10		FPVCCON	O	---	6, -2	Drv (0)
11		LD9	O	---	24, -8	Drv (0)
12		LD11	O	---	24, -8	Drv (0)
13		LD13	O	---	24, -8	Drv (0)
14		LD15	O	---	24, -8	Drv (0)
15	CRT I/F	BLUE	O	150PD	---	---
16		GREEN	O	150PD	---	---
17		RED	O	150PD	---	---
18		VSYNC	O	---	12, -4	Drv (0)
19	LCD I/F	LD17	O	---	24, -8	Drv (0)
20		RESERVE	---	---	---	---
21	Mouse I/F	MSDATA	IO OD	External	24,-	Input
22	Keyboard I/F	KBDATA	IO OD	External	24,-	Input
23	FDD I/F	FDWP#	I	External	---	Input
24		FDINDEX#	I	External	---	Input
25		FDTRK0#	I	External	---	Input
26		FDWD#	O OD	External	38,-	High-Z
27	Power Supply	V_{CC5}	POWER	---	---	---
28		V_{CC5}	POWER	---	---	---
29		V_{CC3}	POWER	---	---	---
30		V_{CC3}	POWER	---	---	---
31	FDD I/F	FDDS2#	O OD	External	38,-	High-Z
32		FDMT2#	O OD	External	38,-	High-Z
33		FDSIDE	O OD	External	38,-	High-Z
34		FDDIR	O OD	External	38,-	High-Z
35	Serial I/F	RESERVE	---	---	---	---
36		COMBDTR#	O	---	8, -8	High-Z
37		COMBCTS#	I	50KPU	---	Input
38		COMBRTS#	O	---	8, -8	High-Z
39		COMBDSR#	I	50KPU	---	Input
40		COMADTR#	O	---	8, -8	High-Z
41		COMACTS#	I	50KPU	---	Input
42		COMADTR#	O	---	8, -8	High-Z
43		COMACTS#	I	50KPU	---	Input
44		IRRXD	I	50KPU	---	Input
45	Parallel I/F	LPTSTROBE#	IO OD	4.7KPU	12,-	Input
46		LPTD0	IO	50KPD	8, -8	Input or Drive
47		LPTACK#	I	47KPU	---	Input

Pin	Group (EASI)	Signal name	Type	Termination	Drive (mA) Iol, Ioh	Suspend
48	Parallel I/F	LPTPE	I	47KPD	---	Input
49		LPTD1	IO	50KPD	8, -8	Input or Drive
50		LPTD2	IO	50KPD	8, -8	Input or Drive
51		LPTD3	IO	50KPD	8, -8	Input or Drive
52		LPTD5	IO	50KPD	8, -8	Input or Drive
53		LPTD7	IO	50KPD	8, -8	Input or Drive
54	IDE I/F	HDIR	O	---	8, -8	Drv (0)
55		HDENL#	O	---	8, -8	Drv (1)
56		HDCS0#	O	---	12, -12	High-Z
57	Power	SUSSTAT#	O	---	8, -8	Drv (0)
58	Management I/F	BATLOW#	I	10KPU	---	Active
59	Power Supply	GND	POWER	---	---	---
60		GND	POWER	---	---	---
61	Power	BATWARN#	I	10KPU	---	Input
62	Management I/F	POWERGOOD	I	---	---	Input(1)
63	Speaker I/F	SPKOUT	O	---	4, -4	Drv (0)
64	BIOS ROM	FLOAT#	I	10KPU	---	Input(1)
65	Update I/F	ROMCE0#	O3	---	4, -4	Drive
66		RESERVE		---	---	---
67	ISA Bus	SD7	IO3/5	47KPU	12, -2	Input
68		SD6	IO3/5	47KPU	12, -2	Input
69		SD5	IO3/5	47KPU	12, -2	Input
70		SD4	IO3/5	47KPU	12, -2	Input
71		SD3	IO3/5	47KPU	12, -2	Input
72		SD2	IO3/5	47KPU	12, -2	Input
73		SD1	IO3/5	47KPU	12, -2	Input
74		SD0	IO3/5	47KPU	12, -2	Input
75		IOCHRDY	IO3OD	1KPU	12,-	Input
76		AEN	O3	22ST	12, -2	Drv (0)
77		SA19	IO3/5	HOLD	12, -2	Drive
78		SA18	IO3/5	HOLD	12, -2	Drive
79		SA17	IO3/5	HOLD	12, -2	Drive
80		SA16	IO3/5	HOLD	12, -2	Drive
81		SA15	IO3/5	HOLD	12, -2	Drive
82	Power Supply	V_{CC3}	POWER	---	---	---
83		V_{CC3}	POWER	---	---	---
84		V_{CC5}	POWER	---	---	---
85		V_{CC5}	POWER	---	---	---
86	ISA Bus	SA14	IO3/5	HOLD	12, -2	Drive
87		SA13	IO3/5	HOLD	12, -2	Drive
88		SA12	IO3/5	HOLD	12, -2	Drive
89		SA11	IO3/5	HOLD	12, -2	Drive
90		SA10	IO3/5	HOLD	12, -2	Drive
91		SA9	IO3/5	HOLD	12, -2	Drive
92		SA8	IO3/5	HOLD	12, -2	Drive
93		SA7	IO3/5	HOLD	12, -2	Drive
94		SA6	IO3/5	HOLD	12, -2	Drive
95		SA5	IO3/5	HOLD	12, -2	Drive
96		SA4	IO3/5	HOLD	12, -2	Drive

Pin	Group (EASI)	Signal name	Type	Termination	Drive (mA) Iol, Ioh	Suspend
97	ISA Bus	SA3	IO3/5	HOLD	12, -2	Drive
98		SA2	IO3/5	HOLD	12, -2	Drive
99		SA1	IO3/5	HOLD	12, -2	Drive
100		SA0	IO3/5	HOLD	12, -2	Drive
101		SBHE#	IO3	47KPU	12, -2	Drive
102		LA23	IO3/5	HOLD	12, -2	Drive
103		LA22	IO3/5	HOLD	12, -2	Drive
104		LA21	IO3/5	HOLD	12, -2	Drive
105		LA20	IO3/5	HOLD	12, -2	Drive
106		LA19	IO3/5	HOLD	12, -2	Drive
107		LA18	IO3/5	HOLD	12, -2	Drive
108		LA17	IO3/5	HOLD	12, -2	Drive
109		MEMR#	IO3/5	47KPU	12, -2	Drv (1)
110		MEMW#	IO3/5	47KPU	12, -2	Drv (1)
111		SD8	IO3/5	47KPU	12, -2	Input
112		SD9	IO3/5	47KPU	12, -2	Input
113		SD10	IO3/5	47KPU	12, -2	Input
114		SD11	IO3/5	47KPU	12, -2	Input
115	Power	SMOUT3	O	---	8, -8	Drive
116	Management I/F	SMOUT1	O	---	8, -8	Drive
117	Power Supply	GND	POWER	---	---	---
118		GND	POWER	---	---	---
119		GND	POWER	---	---	---
120		GND	POWER	---	---	---
121	LCD I/F	FPDOTCLK	O	---	24, -8	Drv (0)
122		LD7	O	---	24, -8	Drv (0)
123		LD5	O	---	24, -8	Drv (0)
124		LD3	O	---	24, -8	Drv (0)
125		LD1	O	---	24, -8	Drv (0)
126		FPHTIM	O	---	24, -8	Drv (0)
127		LD8	O	---	24, -8	Drv (0)
128		FPVEEON	O	---	6, -2	Drv (0)
129		FPBLANK#	O	---	24, -8	Drv (0)
130		LD10	O	---	24, -8	Drv (0)
131		LD12	O	---	24, -8	Drv (0)
132		LD14	O	---	24, -8	Drv (0)
133	CRT I/F	BRTN				
134		GRTN				
135		RRTN				
136		HSYNC	O	---	12, -4	Drv (0)
137	LCD I/F	LD16	O	---	24, -8	Drv (0)
138		RESERVE	---	---	---	---
139	Mouse I/F	MSCLK	IO OD	External	24,-	Drv (0)
140	Keyboard I/F	KBCLK	IO OD	External	24,-	Drv (0)
141	FDD I/F	FDRD#	I	External	---	Input
142		FDDCHG#	I	External	---	Input
143		FDWE#	O OD	External	38,-	High-Z
144		FDHIDEN	O OD	External	38,-	High-Z
145	Power Supply	V_{CC5}	POWER	---	---	---

Pin	Group (EASI)	Signal name	Type	Termination	Drive (mA) Iol, Ioh	Suspend
146	Power Supply	V_{CC5}	POWER	---	---	---
147		V_{CC3}	POWER	---	---	---
148		V_{CC3}	POWER	---	---	---
149	FDD I/F	FDDS1#	O OD	External	38,-	High-Z
150		FDMT1#	O OD	External	38,-	High-Z
151		FDSTEP#	O OD	External	38,-	High-Z
152		RESERVE	---	---	---	---
153	Serial I/F	DARXD	I	50KPU	---	Input
154		COMBRI#	I	50KPU	---	Active or Input
155		COMBRXD	I	50KPD	---	Input
156		COMBTXD	O	---	8, -8	High-Z
157		COMBDCD#	I	50KPU	---	Input
158		COMARI#	I	50KPU	---	Active or Input
159		COMARXD	I	50KPD	---	Input
160		COMATXD	O	---	8, -8	High-Z
161		COMADCD#	I	50KPU	---	Input
162		IRTXD	O	---	24, -12	High-Z
163	Parallel I/F	LPTAFD#	IO OD	4.7KPU	12,-	Input
164		LPTERROR#	I	47KPU	---	Input
165		LPTBUSY	I	47KPU	---	Input
166		LPTSLCT	I	47KPD	---	Input
167		LPTINIT#	IO OD	4.7KPU	12,-	Input
168		LPTSLCTIN#	IO OD	4.7KPU	12,-	Input
169		LPTD4	IO	50KPD	8, -8	Input or Drive
170		LPTD6	IO	50KPD	8, -8	Input or Drive
171		LPTDIR	O	---	8, -8	Drive
172	IDE I/F	HD7	IO	50KPU	12, -12	Input
173		HDENH#	O	---	8, -8	Drv(1)
174		HDCS1#	O	---	12, -12	High-Z
175	Power	V_{BK}	POWER	---	---	---
176	Management I/F	EXTSMI#	I	10KPU	---	Input
177	Power Supply	GND	POWER	---	---	---
178		GND	POWER	---	---	---
179	Power	RESERVE	---	---	---	---
180	Management I/F	SRBTN#	I	10KPU	---	Active
181	Watchdog I/F	WDTIM#	O	---	4, -4	Drive
182	BIOS ROM	PGM	POWER	---	---	---
183	Update I/F	RESERVE	---	---	---	---
184		RESERVE	---	---	---	---
185	ISA Bus	RESETDRV	O3	22ST	12, -2	Drv(0)
186		IOCHCK#	I	4.7KPU	---	Input
187		IRQ9	I	50KPU	---	Input
188		DRQ2	IO	50KPD	12, -2	Input or Drive
189		WS0#	I	1KPU	---	Input
190		SMEMW#	O	---	12, -12	Drv (1)
191		SMEMR#	O	---	12, -12	Drv (1)
192		IOW#	IO3/5	47KPU	12, -2	Drv (1)
193		IOR#	IO3/5	47KPU	12, -2	Drv (1)
194		DACK3#	O	---	8, -8	Drv (1)

Pin	Group (EASI)	Signal name	Type	Termination	Drive (mA) Iol, Ioh	Suspend
195	ISA Bus	DRQ3	I	50KPD	---	Input
196		DACK1#	O	---	8, -8	Drv (1)
197		DRQ1	I	50KPD	---	Input
198		REF#	IO3 OD	1KPU	12,-	Input
199		SCLK	O3	33ST	12, -2	Drv (0)
200	Power Supply	V_{CC3}	POWER	---	---	---
201		V_{CC3}	POWER	---	---	---
202		V_{CC5}	POWER	---	---	---
203		V_{CC5}	POWER	---	---	---
204	ISA Bus	IRQ7	IO	50KPU	8, -8	Input or Drive
205		IRQ6	IO	50KPU	12, -2	Input or Drive
206		IRQ5	IO	50KPU	8, -8	Input or Drive
207		IRQ4	IO	50KPU	8, -8	Input or Drive
208		IRQ3	IO	50KPU	8, -8	Input or Drive
209		DACK2#	O	---	8, -8	Drv (1)
210		TC	O	---	12, -12	Drv (0)
211		BALE	O3	---	12, -2	Drv (0)
212		OSC	O	33ST	8, -8	Drv (0)
213		MEMCS16#	I	1KPU	---	Input
214		IOCS16#	I	1KPU	---	Input
215		IRQ10	IO	50KPU	8, -8	Input or Drive
216		IRQ11	IO	50KPU	8, -8	Input or Drive
217		IRQ12	O	50KPU	8, -8	Drive
218		IRQ15	I	50KPU	---	Input
219		IRQ14	I	50KPU	---	Input
220		DACK0#	O	---	8, -8	Drv (1)
221		DRQ0	I	50KPD	---	Input
222		DACK5#	O	---	8, -8	Drv (1)
223		DRQ5	I	50KPD	---	Input
224		DACK6#	O	---	8, -8	Drv (1)
225		DRQ6	I	50KPD	---	Input
226		DACK7#	O	---	8, -8	Drv (1)
227		DRQ7	I	50KPD	---	Input
228		MASTER#	I	1KPU	---	Input
229		SD12	IO3/5	47KPU	12, -2	Input
230		SD13	IO3/5	47KPU	12, -2	Input
231		SD14	IO3/5	47KPU	12, -2	Input
232		SD15	IO3/5	47KPU	12, -2	Input
233	Power	SMOUT2	O	---	8, -8	Drive
234	Management I/F	SMOUT0	O	---	8, -8	Drive
235	Power Supply	GND	POWER	---	---	---
236		GND	POWER	---	---	---

10. AC CHARACTERISTICS (RECOMMENDED AND REFERENCE VALUES)

ISA Bus Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
	SCLK Period	-	120	-	ns

ISA Bus Timing

Symbol	Parameter	Min.	Max.	Unit	Note
t301	BALE Active Delay from SCLK	-	25	ns	Figure 10-1
t302	BALE Inactive Delay From SCLK		25	ns	Figure 10-1
t303	LA[23:17], SA[16:2] Valid Delay from SCLK	-	65	ns	Figure 10-1
t304	LA[23:17], SA[16:2] Invalid Delay from SCLK	0	-	ns	Figure 10-1
t305	SA[1:0], SBHE# Valid Delay from SCLK	-	30	ns	Figure 10-1
t306	SA[1:0], SBHE# Invalid Delay from SCLK	0	-	ns	Figure 10-1
t307	Command Active Delay from SCLK (8bit Memory Read/Write, I/O Read/Write Cycle)	-	25	ns	Figure 10-1
t308	Command Inactive Delay from SCLK	5	30	ns	Figure 10-1
t309	MEMCS16# Setup to SCLK	15	-	ns	Figure 10-1
t310	MEMCS16# Hold from SCLK	15	-	ns	Figure 10-1
t311	IOCHRDY Setup to SCLK	15	-	ns	Figure 10-1
t312	IOCHRDY Hold from SCLK	15	-	ns	Figure 10-1
t313	SD[15:0] Setup to SCLK (Read Cycle)	15		ns	Figure 10-1
t314	SD[15:0] Hold from SCLK (Read Cycle)	5		ns	Figure 10-1
t315	SD[15:0] Valid Delay from SCLK (Write Cycle)	-	65	ns	Figure 10-1
t316	SD[15:0] Invalid Delay from SCLK (Write Cycle)	0	20	ns	Figure 10-1
t317	Command Active Delay from SCLK (16bit Memory Read/Write Cycle)	-	30	ns	Figure 10-7
t318	WS0# Setup to SCLK	15	-	ns	Figure 10-2
t319	WS0# Hold from SCLK	15	-	ns	Figure 10-2
t320	IOCS16# Setup to SCLK	15	-	ns	Figure 10-4
t321	IOCS16# Hold from SCLK	15	-	ns	Figure 10-4
t322	Command Active Delay from SCLK (SMEMR#/SMEMW#)	-	45	ns	Figure 10-2
t323	Command Inactive Delay from SCLK (SMEMR#/SMEMW#)	5	50	ns	Figure 10-2

DMA Timing

Symbol	Parameter	Min.	Max.	Unit	Note
t_{35}	DACKx# Active Delay from SCLK	-	75	ns	Figure 10-12
t_{36}	DACKx# Inactive Delay from SCLK	-	75	ns	Figure 10-12
t_{37}	SA[7:0] Valid Delay from SCLK	-	50	ns	Figure 10-12
t_{38}	LA[23:17] Valid Delay from DACKx#	-	90	ns	Figure 10-12
t_{39}	IOR#/IOW#/MEMW# Active from SCLK	-	70	ns	Figure 10-12
t_{40}	IOR# Active Delay from SCLK	-	45	ns	Figure 10-12
t_{41}	MEMW# Active Delay from SCLK	-	35	ns	Figure 10-12
t_{43}	IOCHRDY Setup to SCLK	20	-	ns	Figure 10-12
t_{44}	IOR# Inactive Delay from SCLK	-	60	ns	Figure 10-12
t_{45}	MEMR# Inactive Delay from SCLK	-	60	ns	Figure 10-12
t_{46}	IOW#/MEMW# Inactive Delay from SCLK	-	60	ns	Figure 10-12
t_{48}	DMA address invalid from SCLK	125	-	ns	Figure 10-12
t_{49}	IOR# Float Delay from SCLK	-	80	ns	Figure 10-12
t_{50}	MEMR# Float Delay from SCLK	-	80	ns	Figure 10-12
t_{51}	IOW#/MEMW# Float Delay from SCLK	-	80	ns	Figure 10-12

IDE Interface Timing

Symbol	Parameter	Min.	Max.	Unit	Note
t_{67}	HDCS0#/HDCS1# Active Delay from Address	-	30	ns	Figure 10-13
t_{68}	HDENL#/HDENH# Output Active Delay IOR# Active	-	30	ns	Figure 10-13
t_{69}	HDENL#/HDENH# Output Inactive Delay IOR# Inactive		45	ns	Figure 10-13
t_{70}	SD7 Read Data Valid Delay from HD7	-	30	ns	Figure 10-13
t_{71}	Address Input Hold from Command Inactive	40	-	ns	Figure 10-13
t_{72}	SD7 Read Data Output Float from IOR# Inactive	-	45	ns	Figure 10-13
t_{73}	IOCS16# Setup to Command	10	-	ns	Figure 10-13
t_{74}	IOCS16# Hold from Command	10	-	ns	Figure 10-13
t_{75}	HD7 Write Data Valid from IOW# Active	-	50	ns	Figure 10-14
t_{76}	SD7 Write Data Hold from IOW# Inactive	30	-	ns	Figure 10-14
t_{77}	HD7 Write Data Float from IOW# Inactive	-	45	ns	Figure 10-14
t_{78}	HD7 Write Data Hold from IOW# Inactive	20	-	ns	Figure 10-14

Power Supply Sequencing

Symbol	Parameter	Min.	Max.	Unit	Note
t_{11g}	V_{CC3} = 3.0v Lag fromV_{CC5} = 4.5v	0	-	µs	Figure 10-15
t_3	POWERGOOD Turn on Delay from 3.0v of V_{CC3} and 4.5v of V_{CC5} when both V_{CC}s are Ramping Up	50	-	ms	Figure 10-15
t_{3a}	POWERGOOD Turn on Delay from 4.75v of V_{CC5} when V_{CC5} are Ramping Up	0	-	ms	Figure 10-15
t_5	POWERGOOD Inactive Setup Time to 3.0v of V_{CC3} and 4.5v of V_{CC5} when Both V_{CC}s are Removed	0	-	µs	Figure 10-15
t_9	RESETDRV Active Hold from POWERGOOD Active	1	-	ms	Figure 10-15

note: $V_{CC5} \geq V_{CC3}$ must always be satisfied to avoid damaging the CARD-686.

Monochrome Single STN 8bit LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt_1	FPVTIM Setup to FPHTIM Falling edge	HDP+ HDNP-10	-	Ts	Figure 10-16
Pt_2	FPVTIM Hold from FPHTIM Falling edge	6	-	Ts	Figure 10-16
Pt_3	FPHTIM Period	-	HDP+ HNDP	Ts	Figure 10-16
Pt_4	FPHTIM Pulse Width	LP_SEL +1	-	Ts	Figure 10-16
Pt_5	FPAC Delay from FPHTIM Falling edge	0	-	Ts	Figure 10-16
Pt_6	FPDOTCLK Falling edge to FPHTIM Rising edge	HNDP-10	-	Ts	Figure 10-16
Pt_7	FPDOTCLK Falling edge to FPHTIM Falling edge	HNDP-7+ LP_SEL	-	Ts	Figure 10-16
Pt_8	FPHTIM Falling edge to FPDOTCLK Falling edge	15-LP_SEL	-	Ts	Figure 10-16
Pt_9	FPDOTCLK Period	8	-	Ts	Figure 10-16
Pt_{10}	FPDOTCLK Pulse Width Low	4	-	Ts	Figure 10-16
Pt_{11}	FPDOTCLK Pulse Width High	4		Ts	Figure 10-16
Pt_{12}	LD[7:0] Setup to FPDOTCLK Falling edge	4		Ts	Figure 10-16
Pt_{13}	LD[7:0] Hold to FPDOTCLK Falling edge	4		Ts	Figure 10-16
Pt_{14}	FPHTIM Falling edge to FPDOTCLK Rising edge	11-LP_SEL	-	Ts	Figure 10-16

note: Ts = pixel clock period = 35ns typical
HDP = horizontal display period in units of Ts = 640 typical
HNDP = horizontal non-display period in units of Ts = 112 typical
LP_SEL= 7 typical
Refer to the BIOS Manual and SPC8110 Manual for details.

Monochrome Dual STN 8bit LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt_1	FPVTIM Setup to FPHTIM Falling edge	HDP+ HDNP-10	-	Ts	Figure 10-17
Pt_2	FPVTIM Hold from FPHTIM Falling edge	6	-	Ts	Figure 10-17
Pt_3	FPHTIM Period	-	HDP+ HNDP	Ts	Figure 10-17
Pt_4	FPHTIM Pulse Width	LP_SEL+1	-	Ts	Figure 10-17
Pt_5	FPAC Delay from FPHTIM Falling edge	0	-	Ts	Figure 10-17
Pt_6	FPDOTCLK Falling edge to FPHTIM Rising edge	HNDP-10	-	Ts	Figure 10-17
Pt_7	FPDOTCLK Falling edge to FPHTIM Falling edge	HNDP-9+ LP_SEL	-	Ts	Figure 10-17
Pt_8	FPHTIM Falling edge to FPDOTCLK Falling edge	13-LP_SEL	-	Ts	Figure 10-17
Pt_9	FPDOTCLK Period	4	-	Ts	Figure 10-17
Pt_{10}	FPDOTCLK Pulse Width Low	2	-	Ts	Figure 10-17
Pt_{11}	FPDOTCLK Pulse Width High	2		Ts	Figure 10-17
Pt_{12}	LD[7:0] Setup to FPDOTCLK Falling edge	2		Ts	Figure 10-17
Pt_{13}	LD[7:0] Hold to FPDOTCLK Falling edge	2		Ts	Figure 10-17
Pt_{14}	FPHTIM Falling edge to FPDOTCLK Rising edge	11-LP_SEL	-	Ts	Figure 10-17

note: Ts = pixel clock period = 52ns typical
HDP = horizontal display period in units of Ts = 640 typical
HNDP = horizontal non-display period in units of Ts = 112 typical
LP_SEL= 7 typical
Refer to the BIOS Manual and SPC8110 Manual for details.

Color Dual STN 16bit LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt_1	FPVTIM Setup to FPHTIM Falling edge	HDP+ HDNP-10	-	Ts	Figure 10-18
Pt_2	FPVTIM Hold from FPHTIM Falling edge	6	-	Ts	Figure 10-18
Pt_3	FPHTIM Period	-	HDP+ HNDP	Ts	Figure 10-18
Pt_4	FPHTIM Pulse Width	LP_SEL+1	-	Ts	Figure 10-18
Pt_5	FPAC Delay from FPHTIM Falling edge	0	-	Ts	Figure 10-18
Pt_6	FPDOTCLK Falling edge to FPHTIM Rising edge	HNDP-9	-	Ts	Figure 10-18
Pt_7	FPDOTCLK Falling edge to FPHTIM Falling edge	HNDP-8+ LP_SEL	-	Ts	Figure 10-18
Pt_8	FPHTIM Falling edge to FPDOTCLK Falling edge	12-LP_SEL	-	Ts	Figure 10-18
Pt_9	FPDOTCLK Period	2	-	Ts	Figure 10-18
Pt_{10}	FPDOTCLK Pulse Width Low	1	-	Ts	Figure 10-18
Pt_{11}	FPDOTCLK Pulse Width High	1		Ts	Figure 10-18
Pt_{12}	LD[15:0] Setup to FPDOTCLK Falling edge	1		Ts	Figure 10-18
Pt_{13}	LD[15:0] Hold to FPDOTCLK Falling edge	1		Ts	Figure 10-18
Pt_{14}	FPHTIM Falling edge to FPDOTCLK Rising edge	11-LP_SEL	-	Ts	Figure 10-18

note: Ts = pixel clock period = 52ns typical
HDP = horizontal display period in units of Ts = 640 typical
HNDP = horizontal non-display period in units of Ts = 112 typical
LP_SEL= 7 typical
Refer to the BIOS Manual and SPC8110 Manual for details.

Color TFT LCD Interface

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt_1	FPDOTCLK Period	1	-	Ts	Figure 10-19
Pt_2	FPDOTCLK Pulse Width High	0.5	-	Ts	Figure 10-19
Pt_3	FPDOTCLK Pulse Width Low	0.5	-	Ts	Figure 10-19
Pt_4	DATA Setup to FPDOTCLK Falling edge	0.5	-	Ts	Figure 10-19
Pt_5	DATA Hold from FPDOTCLK Falling edge	0.5	-	Ts	Figure 10-19
Pt_6	FPHTIM Cycle time	-	805	Ts	Figure 10-19
Pt_7	FPHTIM Pulse Width Low	-	96	Ts	Figure 10-19
Pt_8	FPVTIM Cycle time	-	525	lines	Figure 10-19
Pt_9	FPVTIM Pulse Width Low	-	2	lines	Figure 10-19
Pt_{10}	Horizontal Display Period	-	640	Ts	Figure 10-19
Pt_{11}	FPHTIM Setup to FPDOTCLK Falling edge	0.5	-	Ts	Figure 10-19
Pt_{12}	FPVTIM Falling edge to FPHTIM Falling edge Phase Difference	1	-	Ts	Figure 10-19
Pt_{13}	FPBLANK# to FPDOTCLK Falling edge Setup time	0.5	-	Ts	Figure 10-19
Pt_{14}	FPBLANK# Width	-	640	Ts	Figure 10-19

Symbol	Parameter	Min.	Typ.	Unit	Note
Pt_{15}	FPHTIM Sampled Low (by FPDOTCLK) to FPBLANK# Rising edge	-	144	Ts	Figure 10-19
Pt_{16}	FPBLANK# Falling edge to FPHTIM Falling edge	-	16	Ts	Figure 10-19
Pt_{17}	FPBLANK# Hold from FPDOTCLK Falling edge	0.5	-	Ts	Figure 10-19

note: Ts = pixel clock period = 40ns typical
Refer to the BIOS Manual and SPC8110 Manual for details.

10.1 Timing Charts

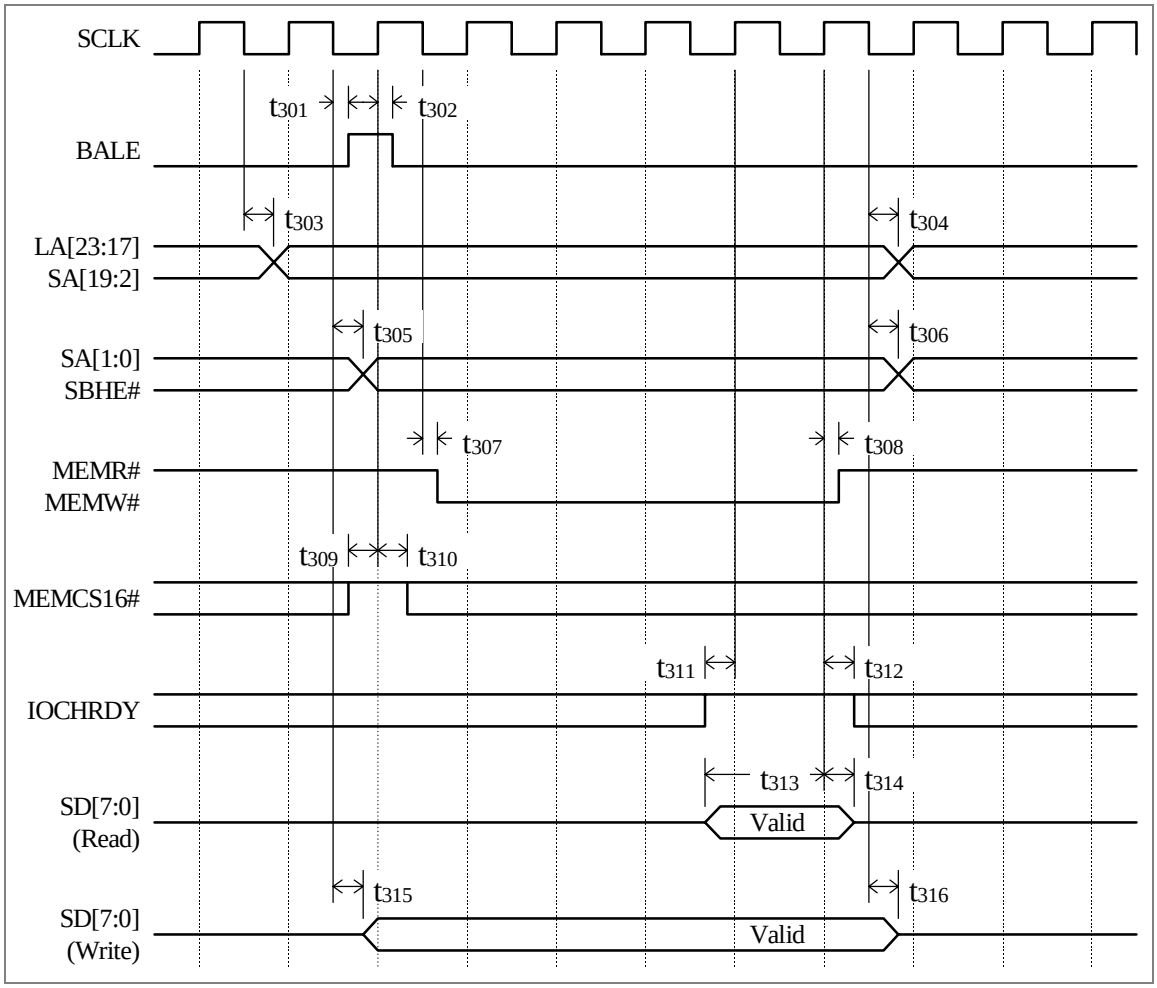

Figure 10-1 ISA Bus 8-Bit Memory Read/Write Standard ISA Bus Cycle (6 SCLKs)

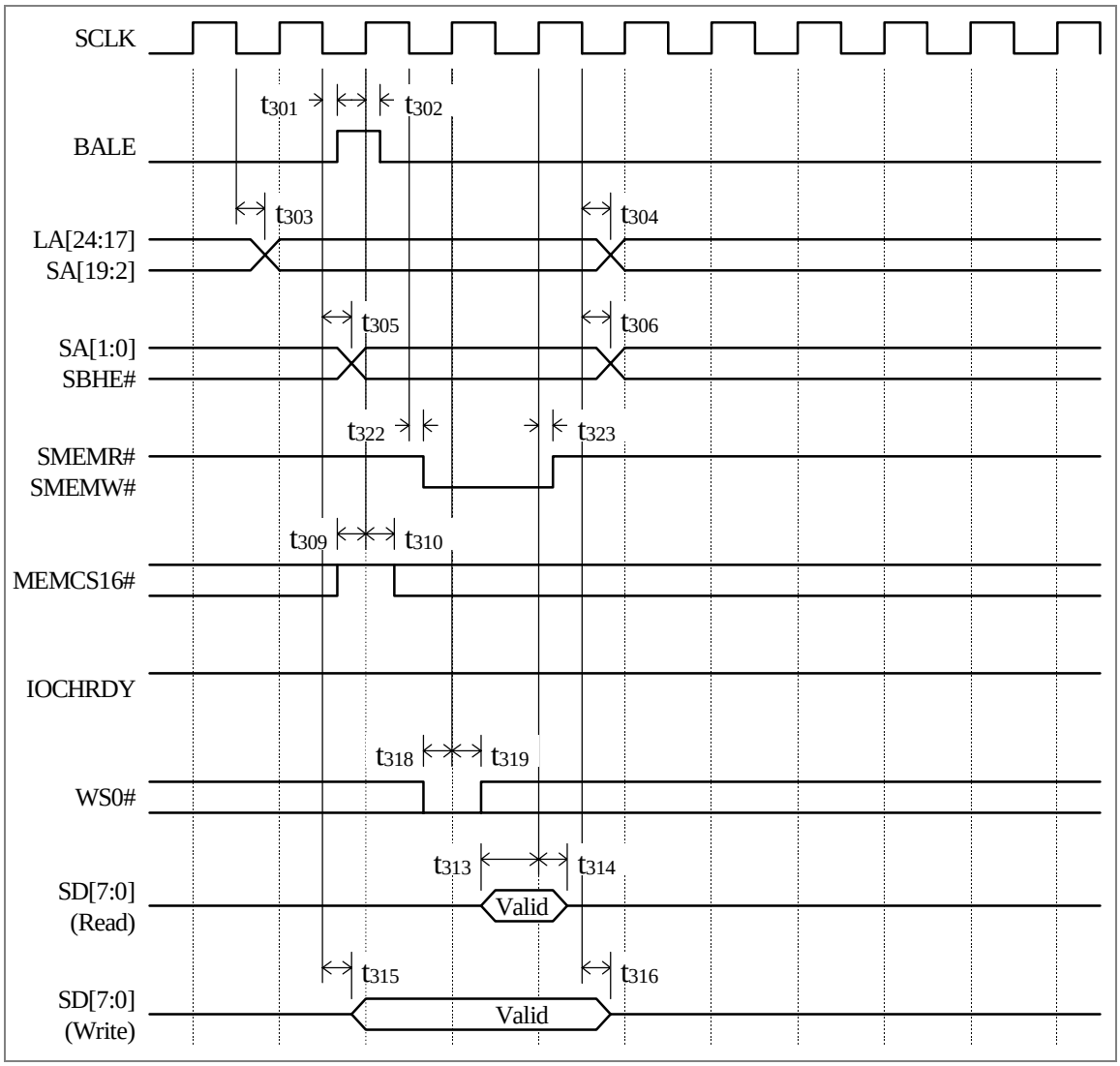

Figure 10-2 ISA Bus 8-Bit Memory Read/Write with WS0# Asserted (3 SCLKs)

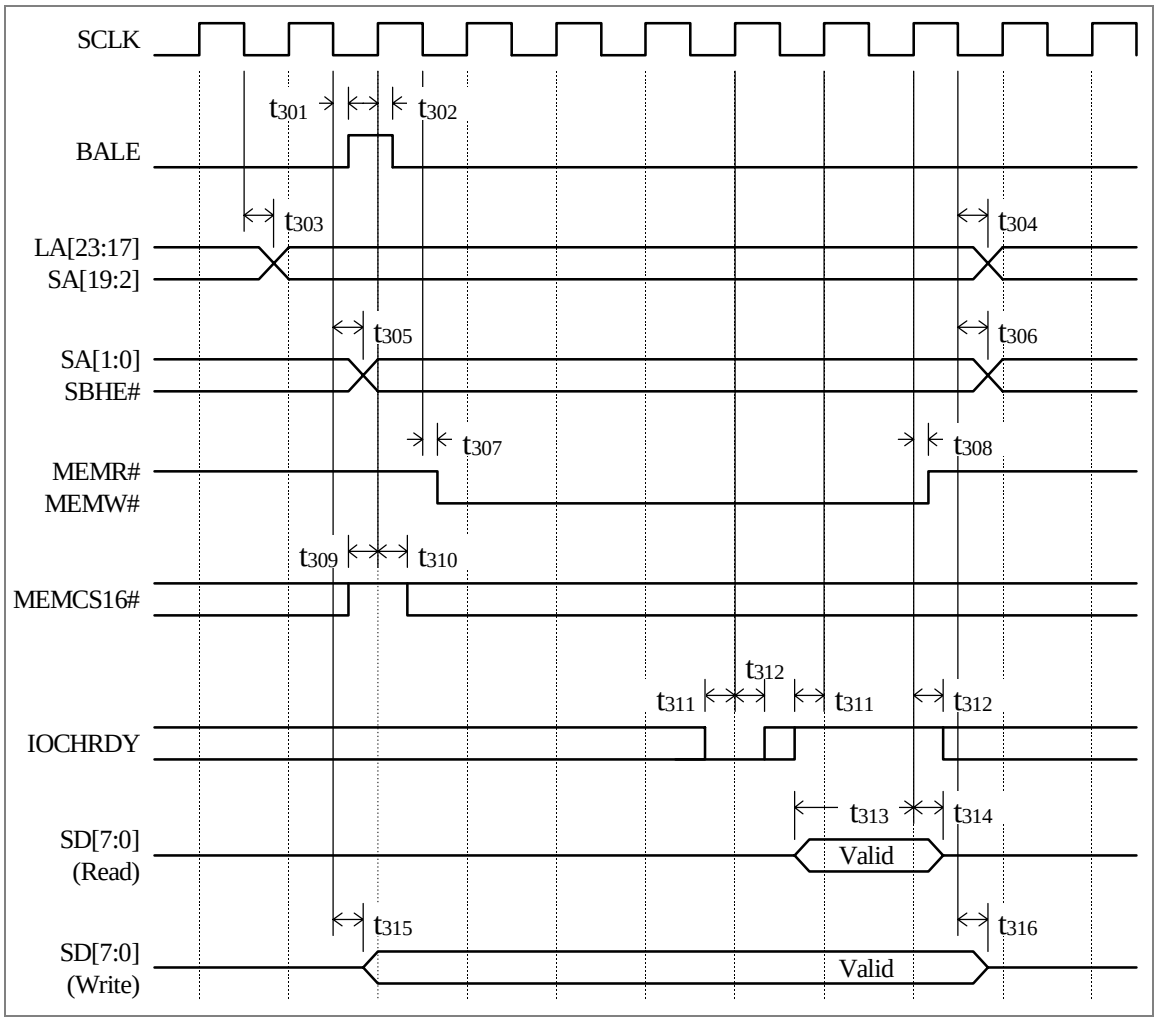

Figure 10-3 ISA Bus 8-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait State)

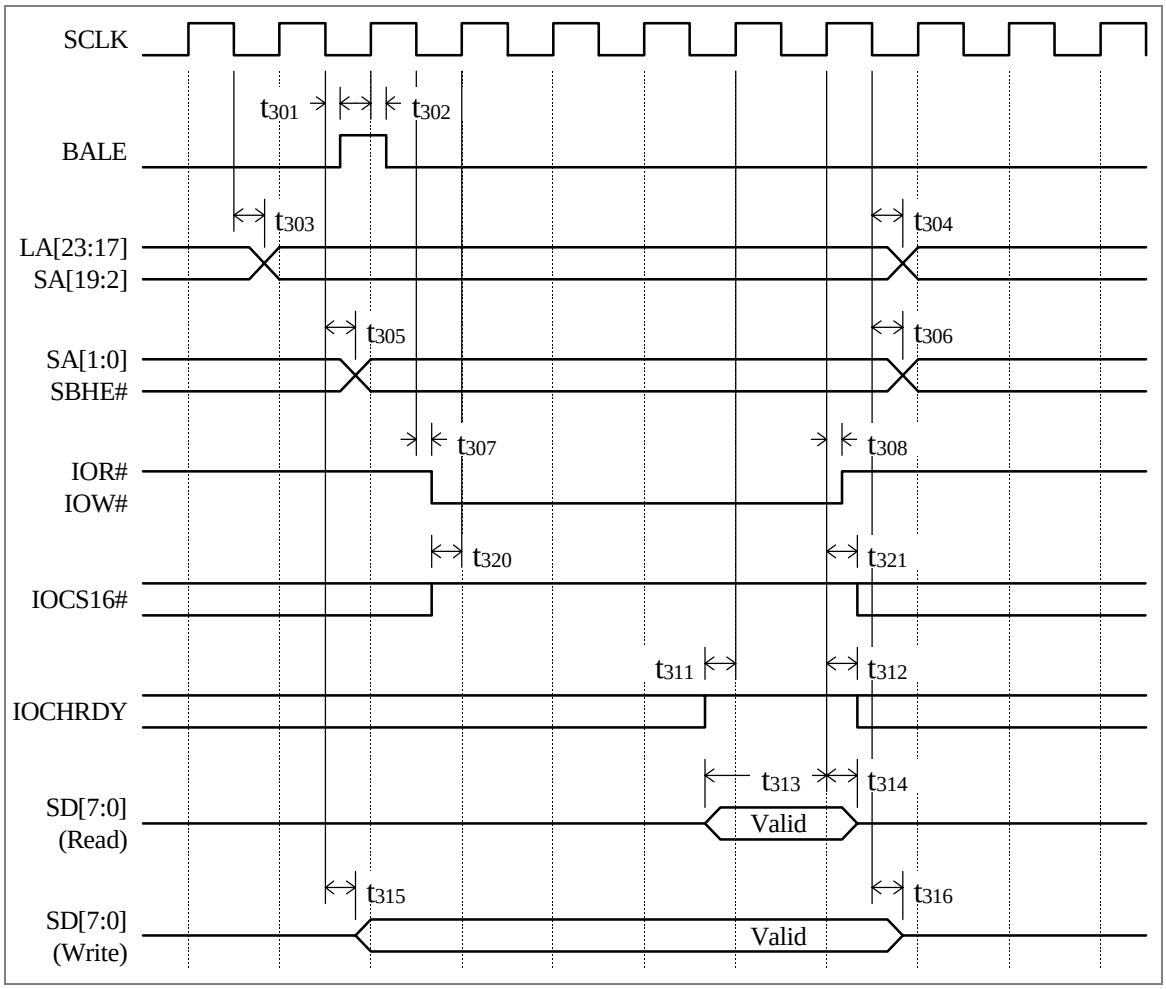

Figure 10-4 ISA Bus 8-Bit I/O Read/Write Standard ISA Bus Cycle (6 SCLKs)

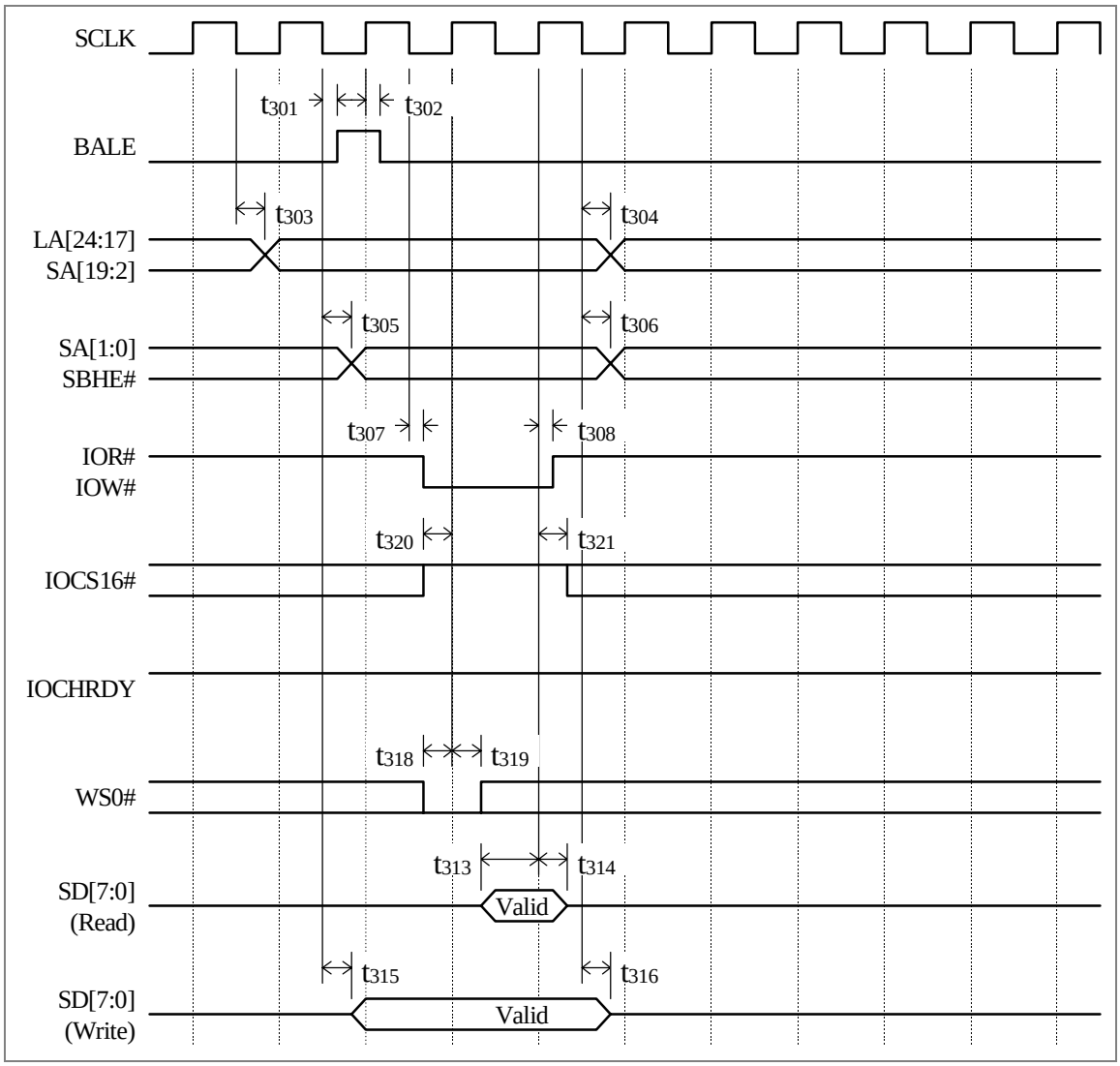

Figure 10-5 ISA Bus 8-Bit I/O Read/Write with WS0# Asserted (3 SCLKs)

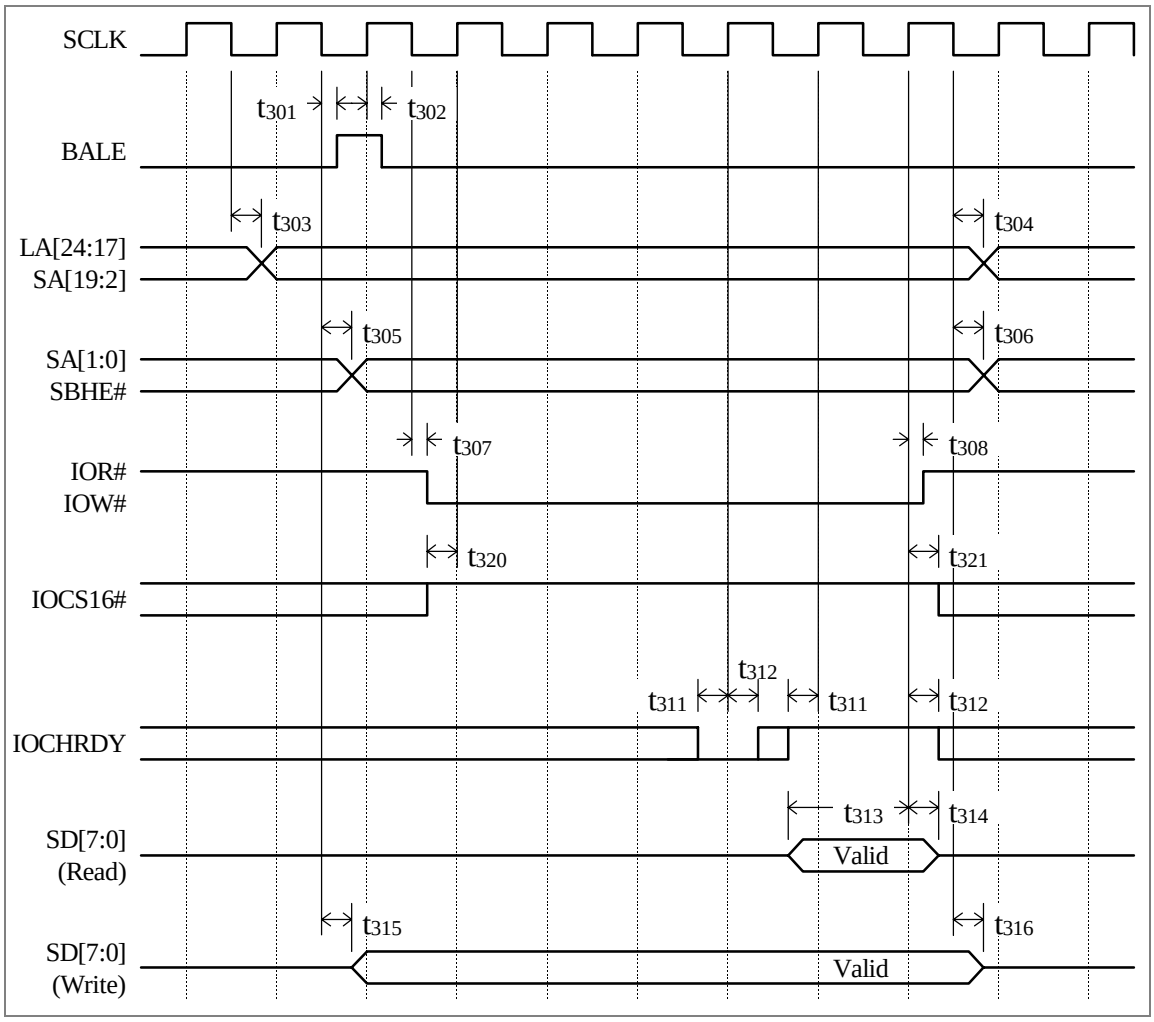

Figure 10-6 ISA Bus 8-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

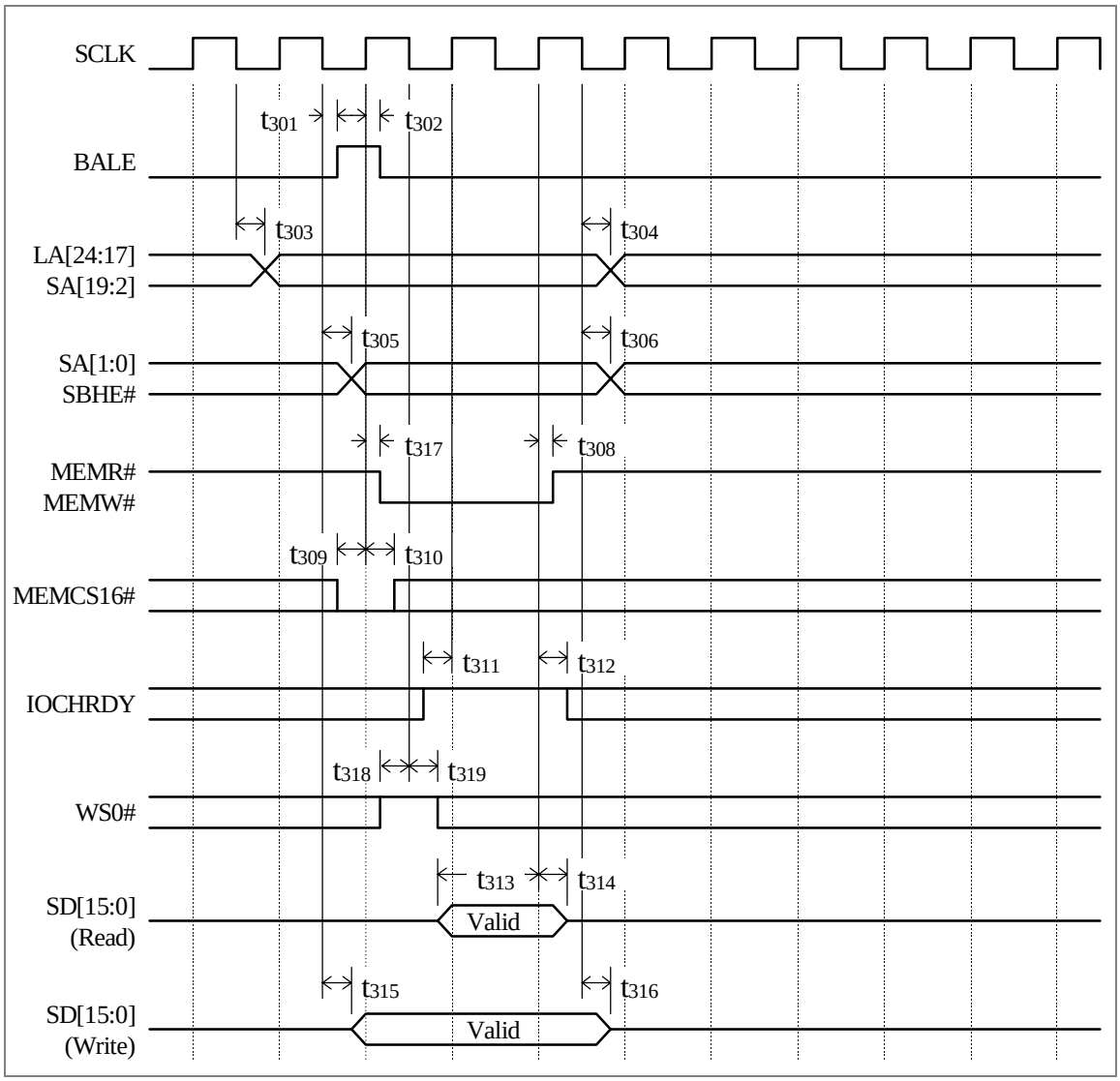

Figure 10-7 ISA Bus 16-Bit Memory Read/Write Standard Bus Cycles (3 SCLKs)

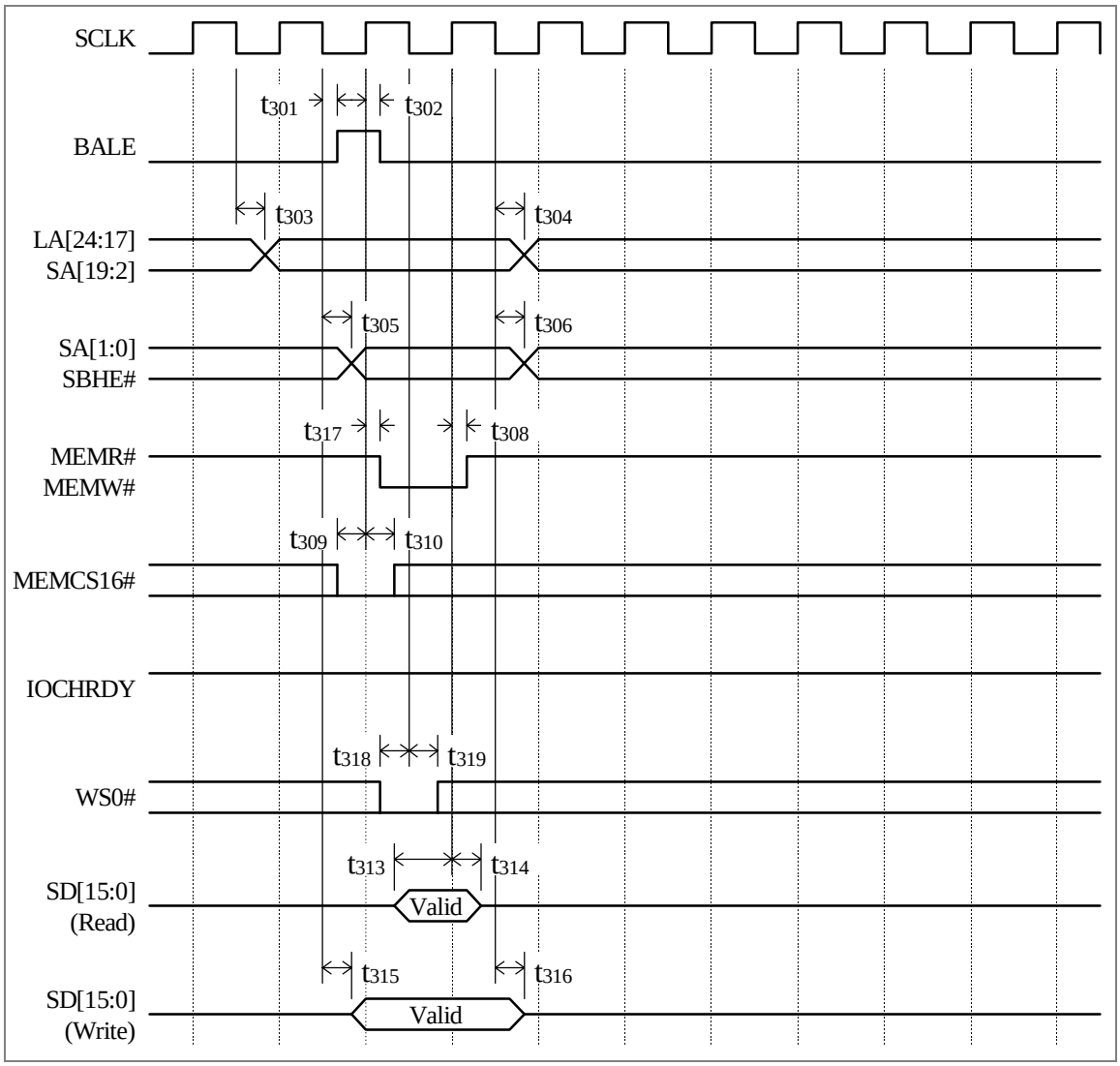

Figure 10-8 ISA Bus 16-Bit Memory Read/Write with WS0# Asserted

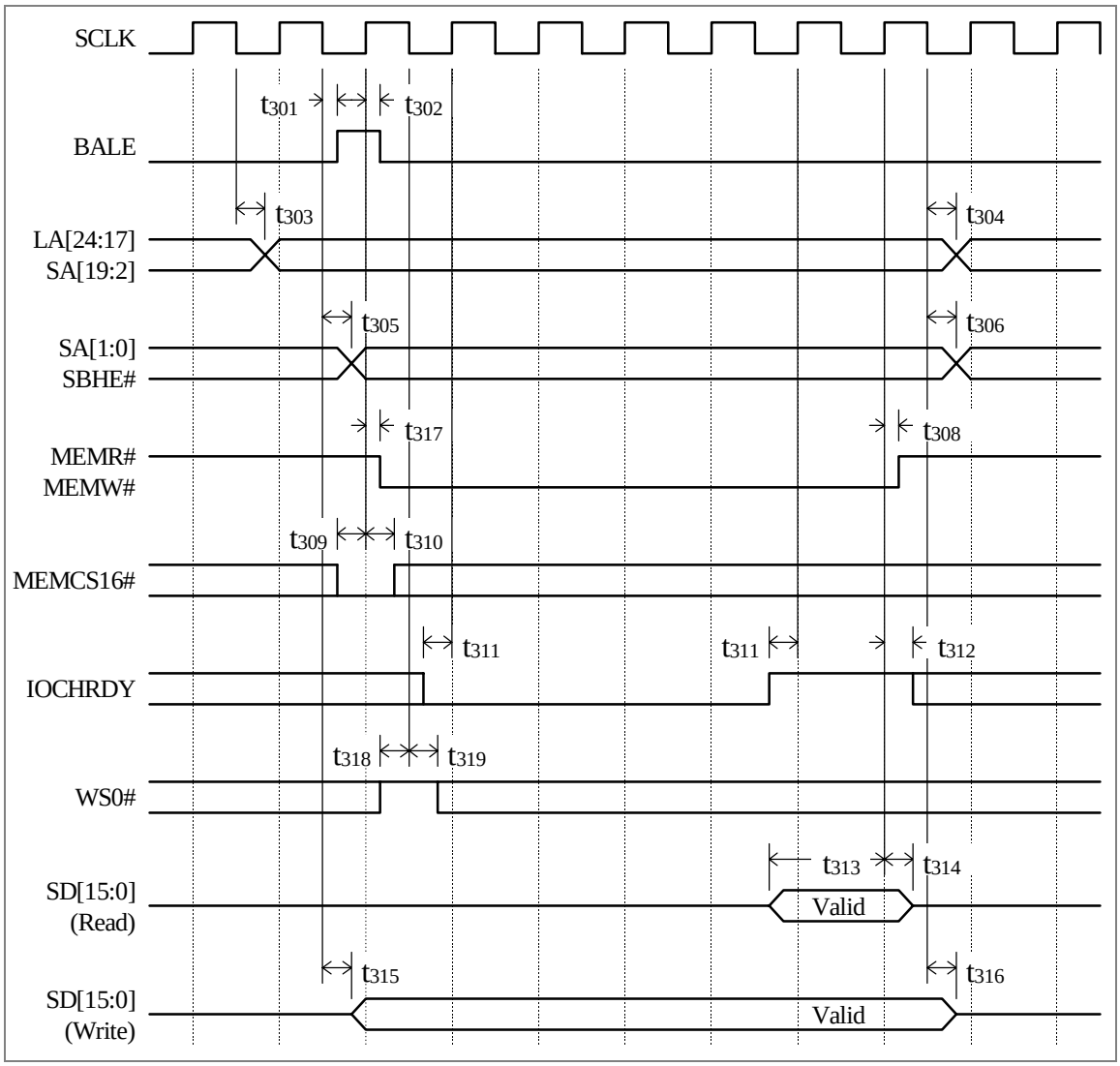

Figure 10-9 ISA Bus 16-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

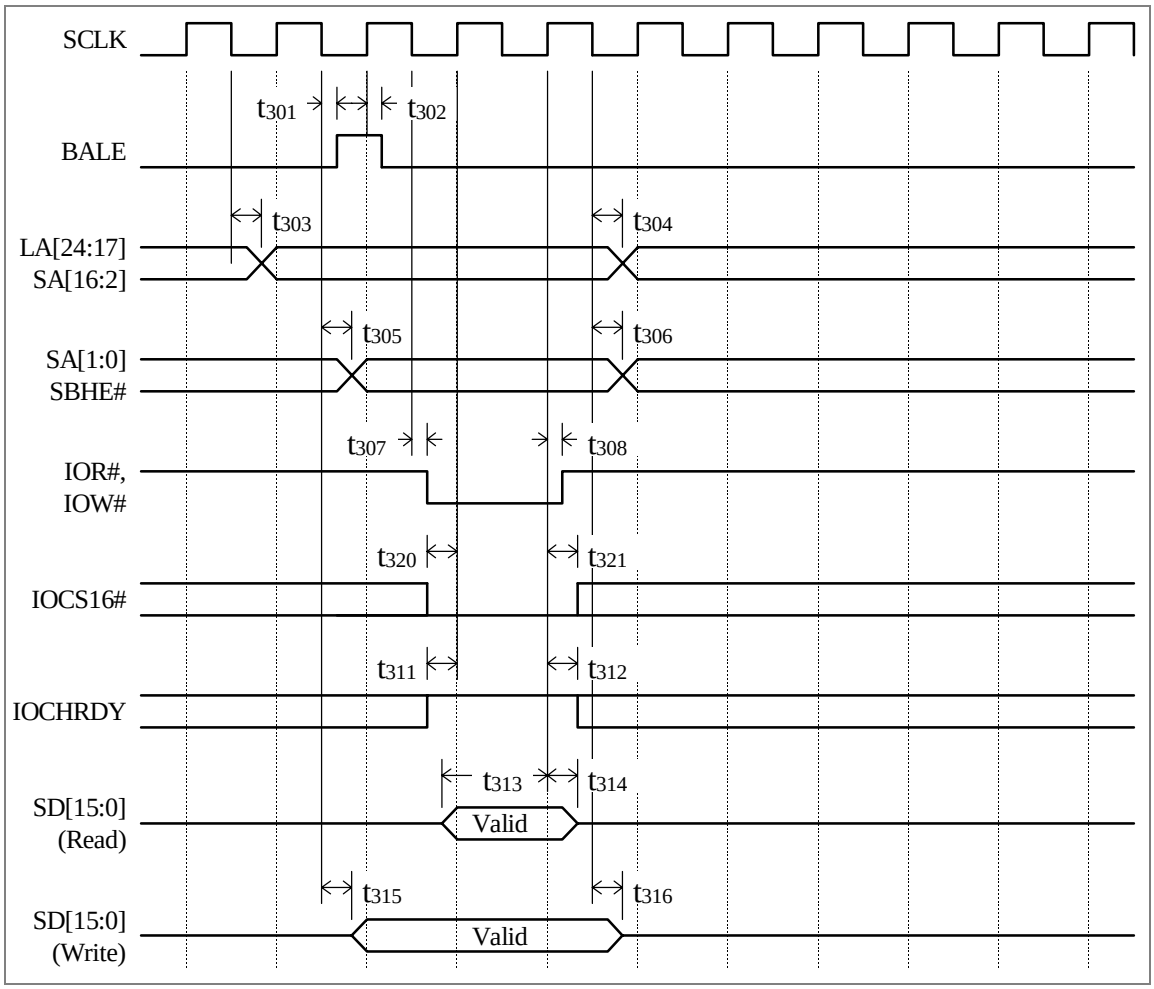

Figure 10-10 ISA Bus 16-Bit I/O Read/Write Standard ISA Bus Cycle (3 SCLKs)

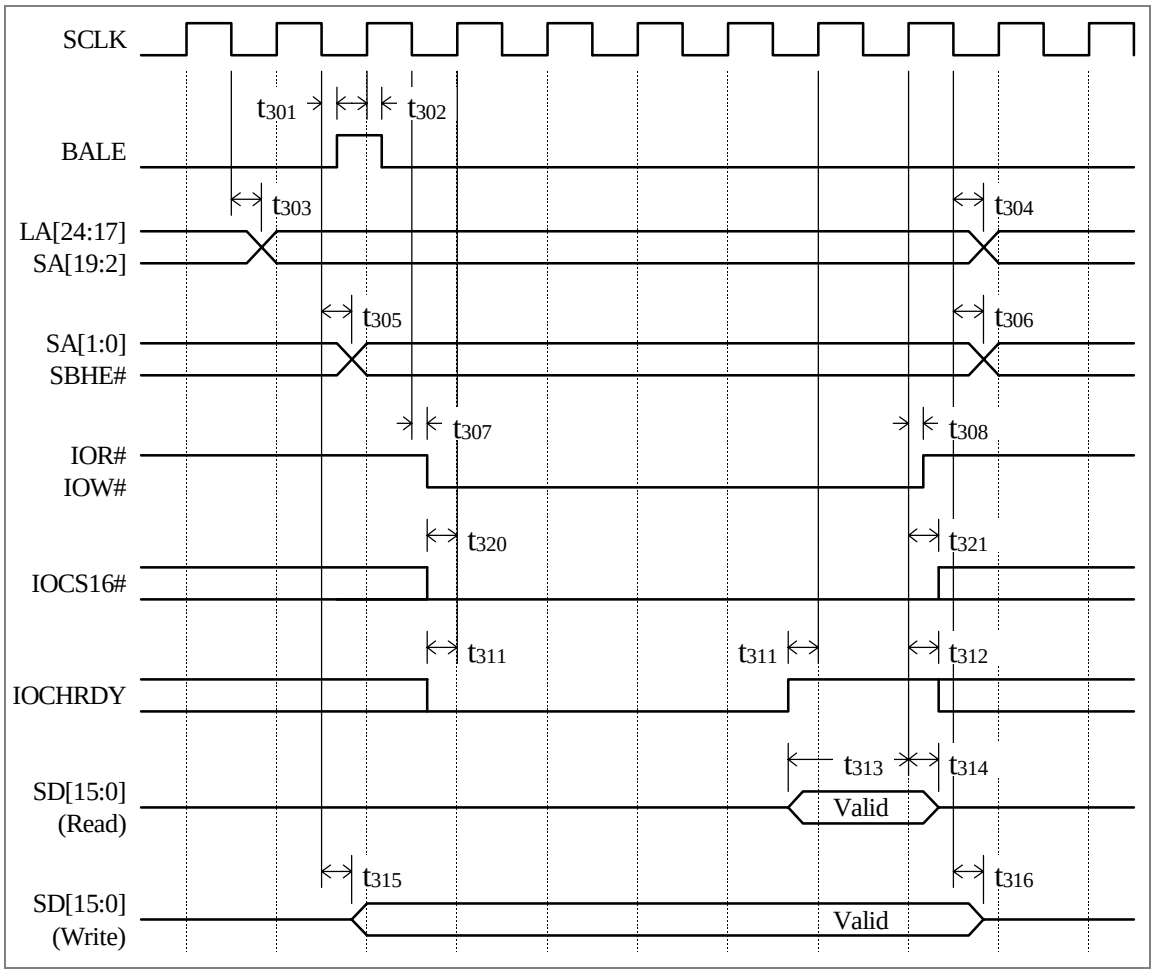

Figure 10-11 ISA Bus 16-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

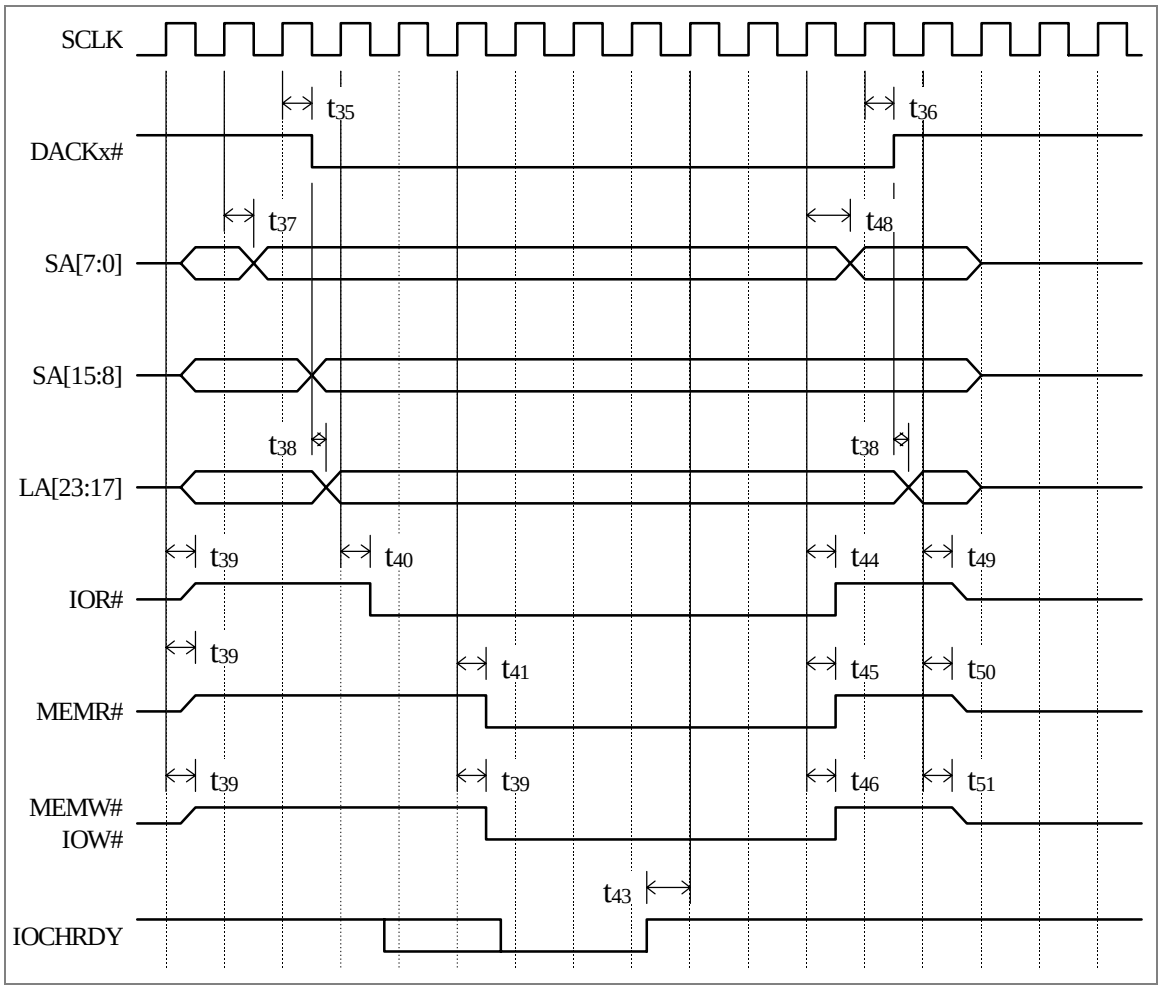

Figure 10-12 DMA Timing

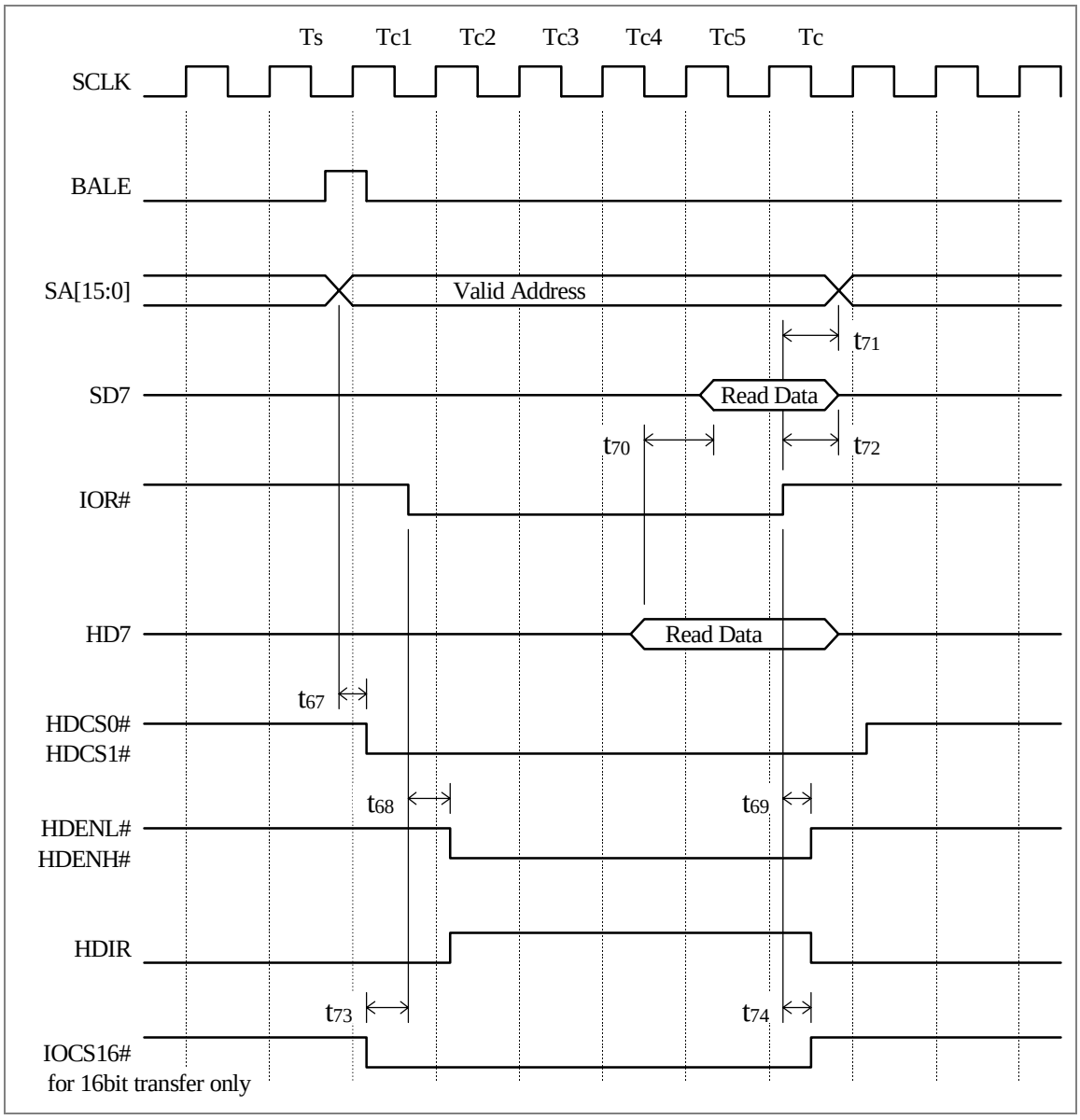

Figure 10-13 IDE Hard Disk Control Signal (I/O Read Timing)

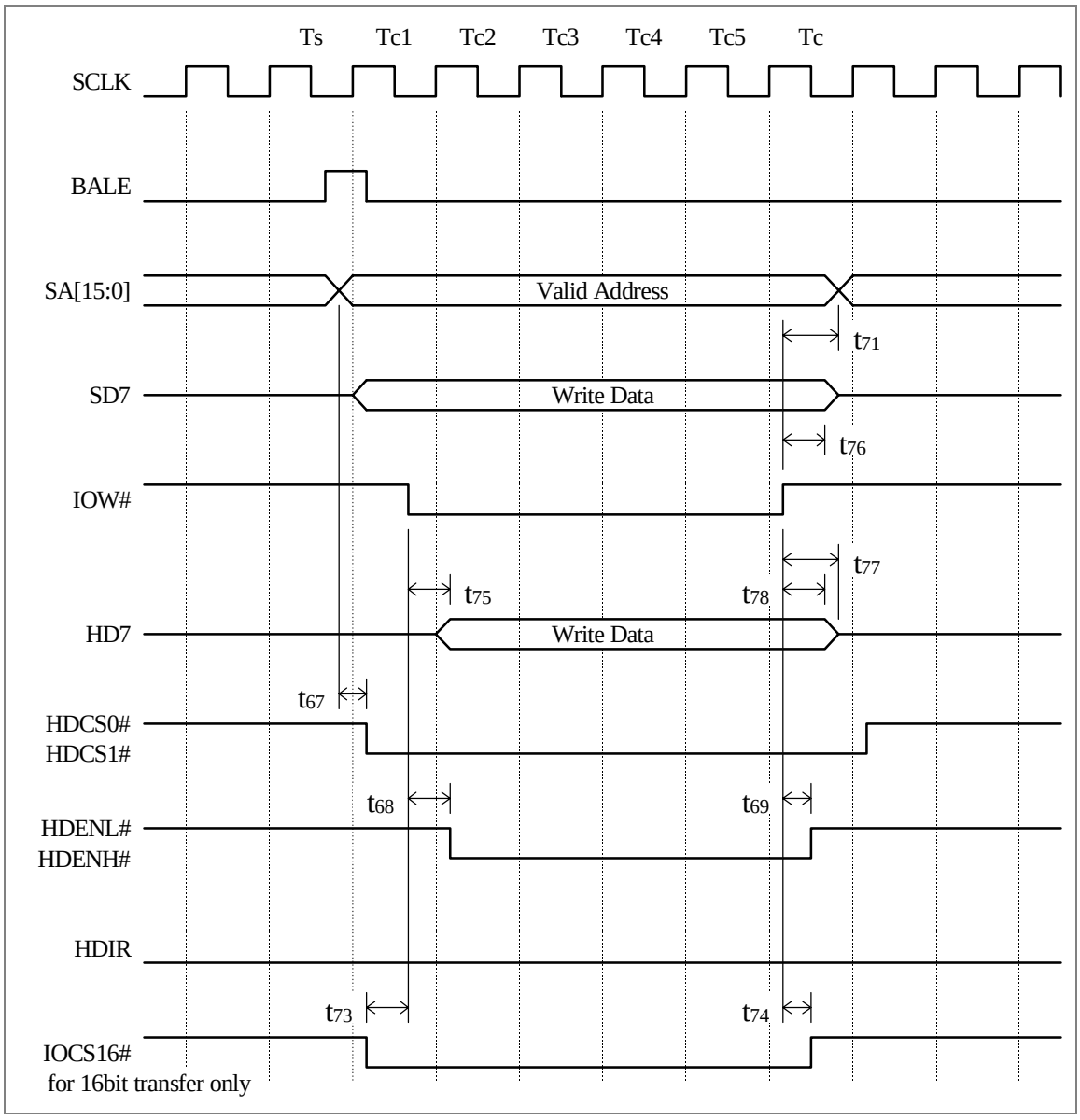

Figure 10-14 IDE Hard Disk Control Signals (I/O Write Timings)

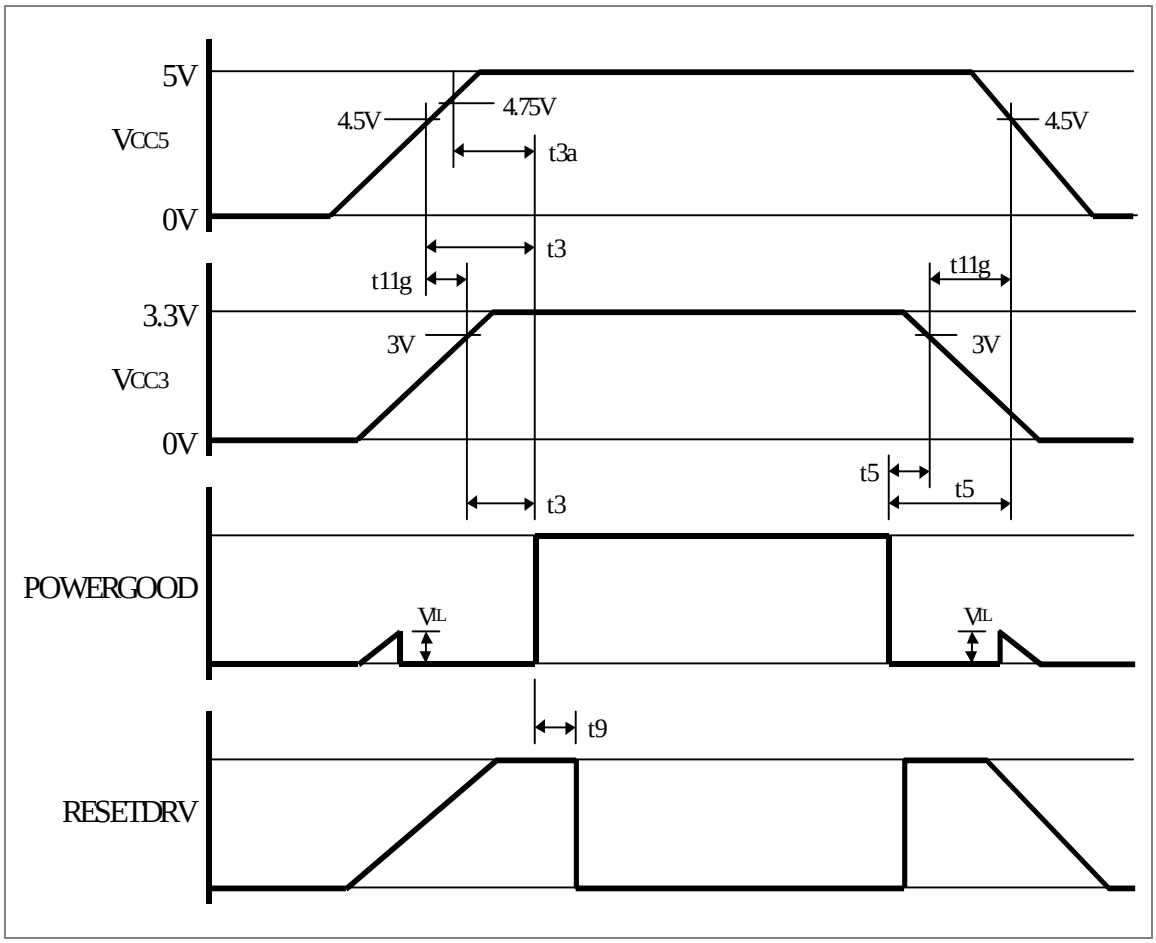

Figure 10-15 Power Supply Sequencing

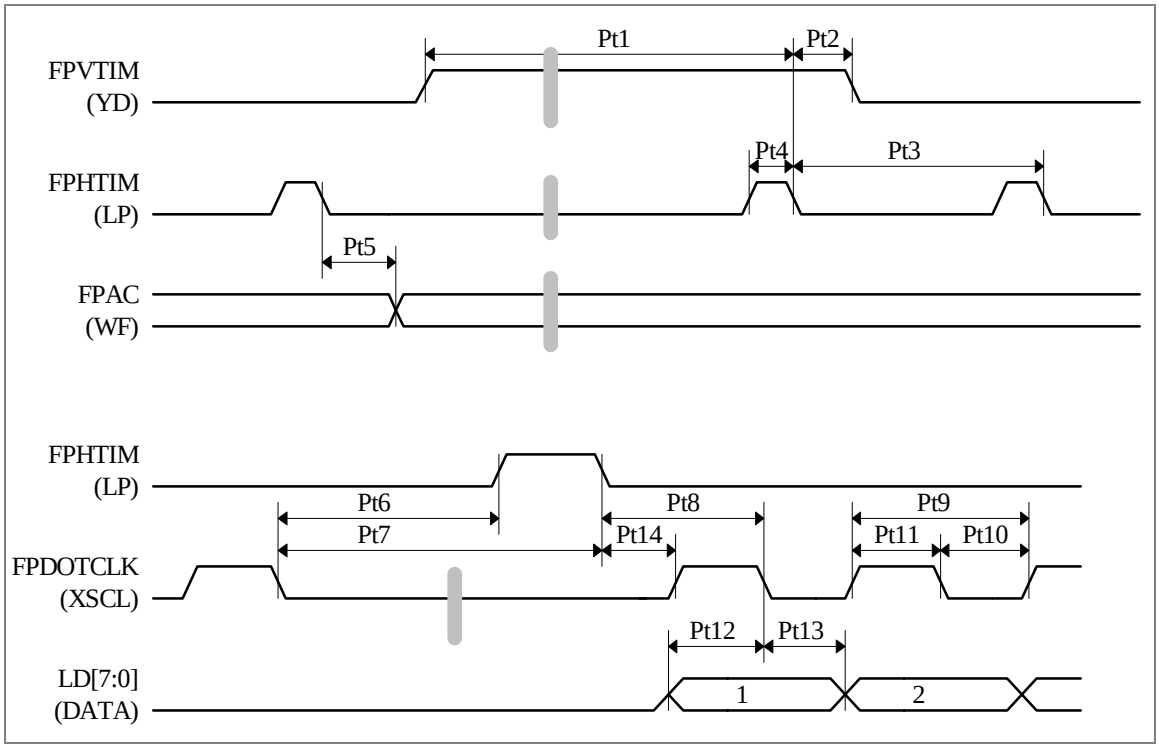

Figure 10-16 Monochrome Single STN 8bit LCD Interface

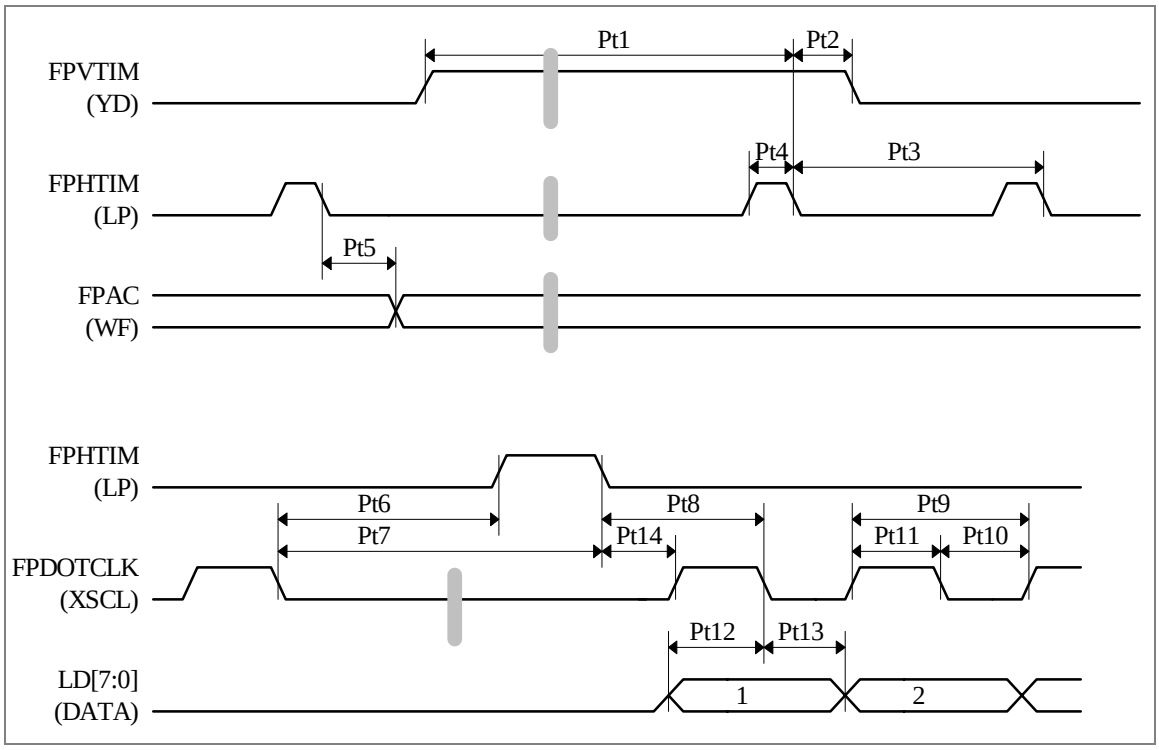

Figure 10-17 Monochrome Dual STN 8bit LCD Interface

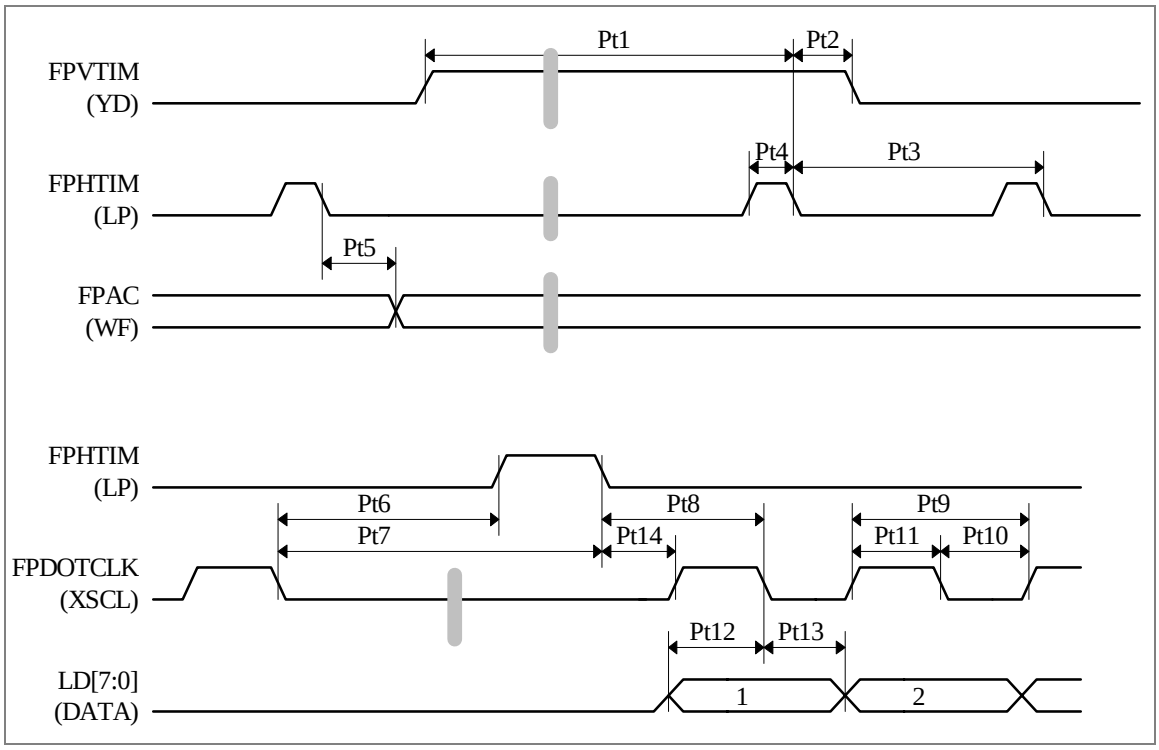

Figure 10-18 Color Dual STN 16bit LCD Interface

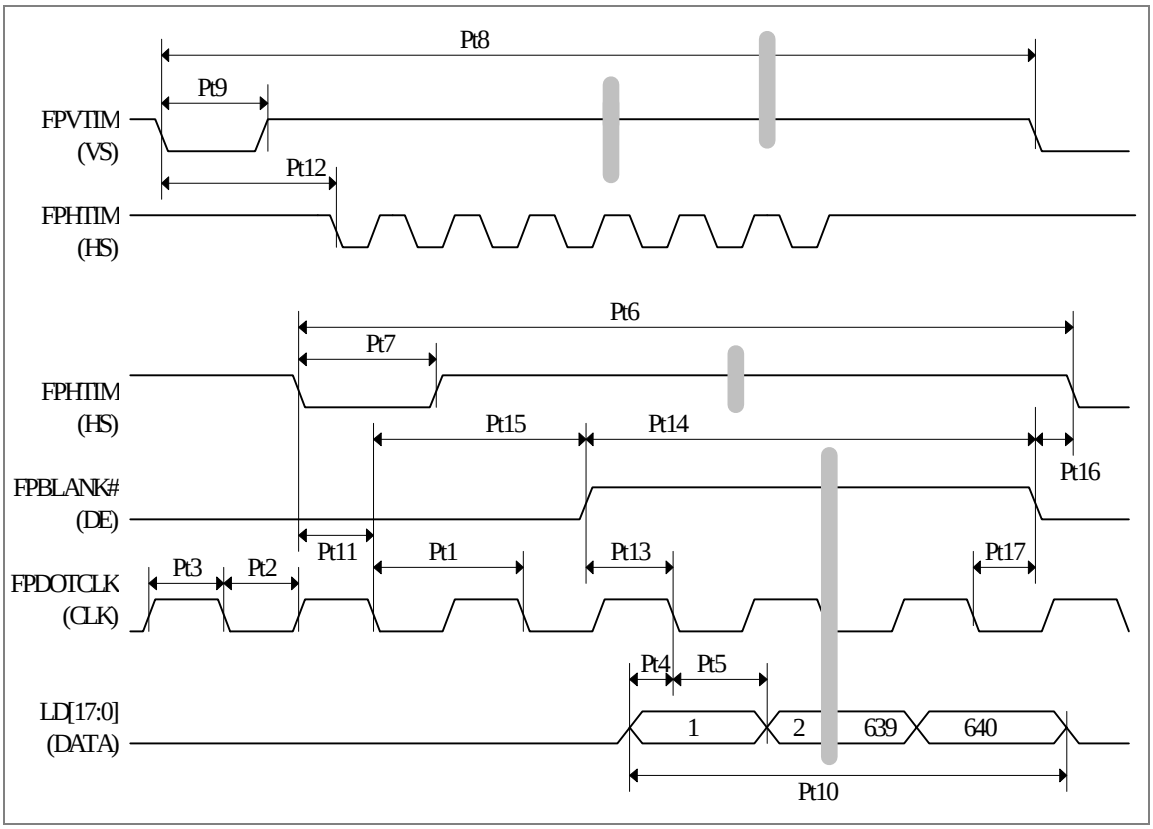

Figure 10-19 Color TFT LCD Interface

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CARD-686
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First issue March,1999
Printed February, 2000 in Japan Ⓟ A