MF1202-01a

EPSON

CARD-E09A

Evaluation Kit Hardware Manual (English)

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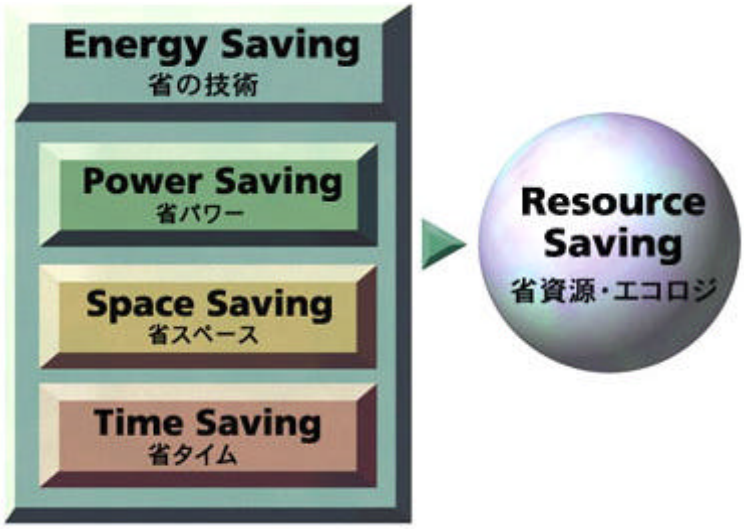

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CARD-E09A Evaluation Kit Hardware Manual (English)

- **CARD-E09A Evaluation Board(SCE88J1B01) Hardware Manual**
- **ISH Board (SCE88J2B01) Hardware Manual**

CARD-E09A

Evaluation Kit Hardware Manual (English)

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CARD-E09A

Evaluation Board
(SCE88J1B01)

Hardware Manual

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1.CAUTIONS

(1) Make sure that JP2 pin 2 and JP2 pin 3 are connected on the CARD-E09A evaluation board (Evaluation board, thereafter) before mounting CARD-E09A.

(2) If the system startup PROM is NOT present on the CN15 socket, leave JP1 pins open.

2.OUTLINE

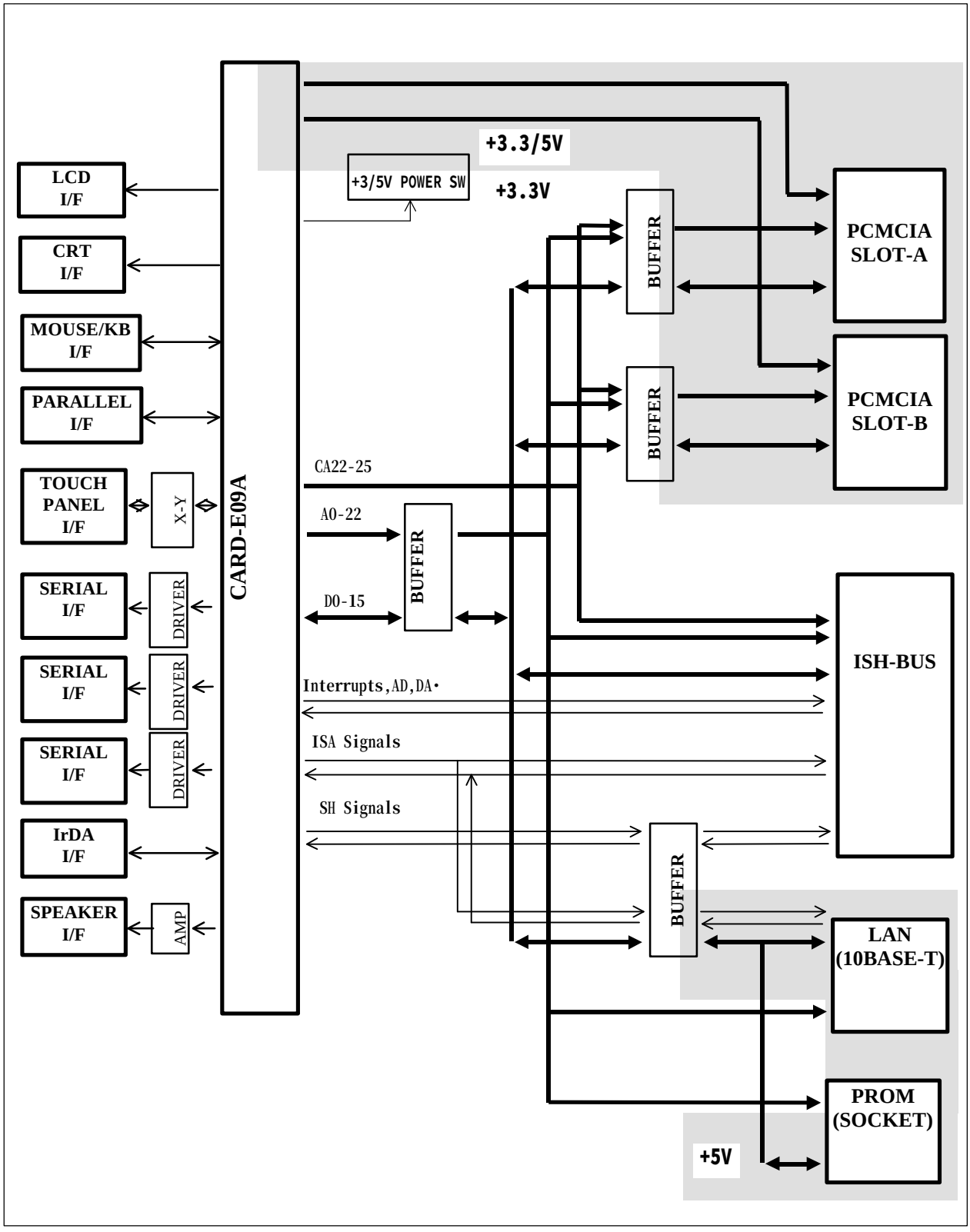
Evaluation board contains the standard connectors, power circuit, Ethernet circuit (10BASE-T) and others required to connect peripheral units for functional evaluation of an SCE8700C Series Card-PC (called the CARD-E09A) that uses the SH7709A (SH3).

Note: The connecter of CARD-E09A is different from the EASI connector.

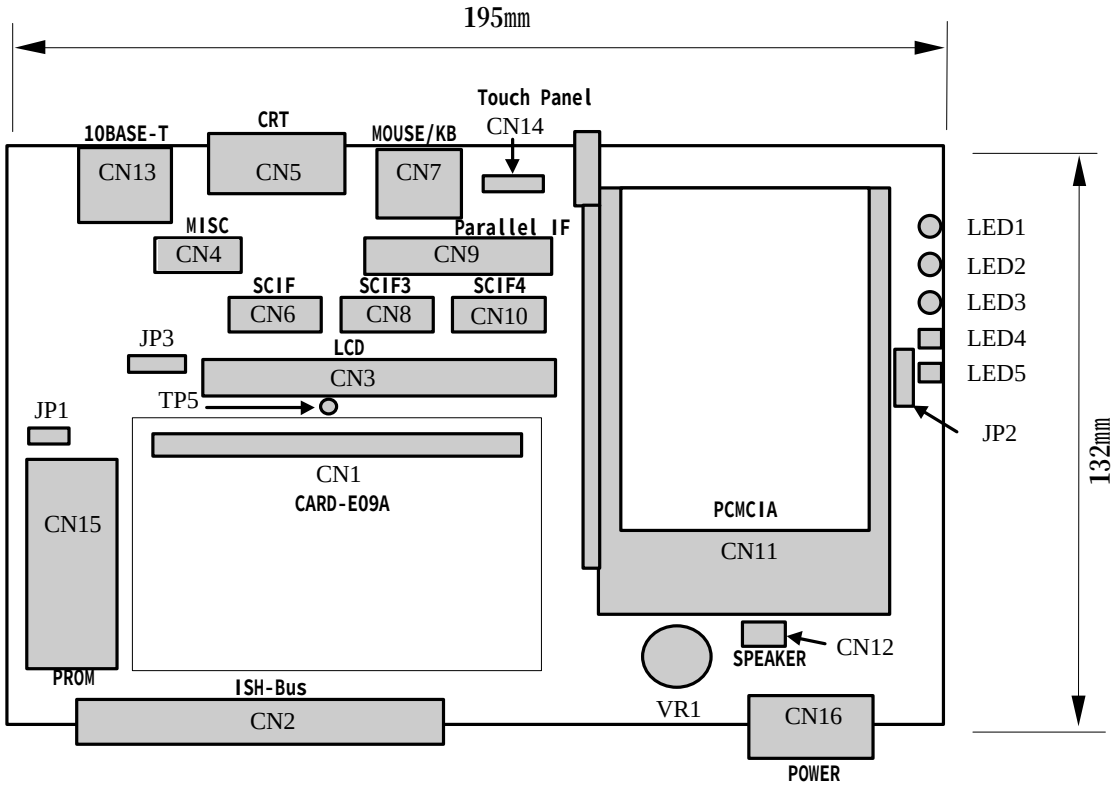
2.1.Features

- A 240-pin connector for CARD-E09A
- Dual PCMCIA slots
- ISH extension bus (SH-bus, ISA-bus and others)
- A 50-pin connector for LCD
- A 15-pin D-sub connector for CRT display
- A Mini-DIN connector for PS/2 mouse or keyboard
- A connector of Parallel port interface
- A connector of Dual-channel serial port interface (the 16550-compatible RS-232C interface)
- A connector of Single-channel serial port interface (SH3 built-in serial channel interface with FIFO, RS-232C interface)
- A connector of Single-channel serial port interface for IrDA 1.0
- A connector of Single-channel serial port interface (SH3 built-in without FIFO)
- A connector of Ethernet (10BASE-T) interface
- Touch panel interface
- Speaker connector(s)
- A PROM socket
- A Backup battery pack

2.2.Block Diagram



2.3.Appearance and Connector Layout



CN17**(Battery)**is mounted on the back.

3.PIN ASSIGNMENT

Refer to the table below for cross reference of power supply signal name.

CARD-E09A Evaluation Board	CARD-E09A	DC Voltage
P3V	V_{CC}	+3.3V
P5V	-	+5.0V

The following symbols are used in the "Type" column of each pin.

I ····· Input
O ····· Output
O OD ····· Output (Open drain output)
Tri ····· Output (Tri-state output)
I/O ····· Input/output
POWER …… Power or ground (GND)
Analog I/O …… Analog input/output
Analog O …… Analog output

3.1.CARD-E09A Connectors

The 240-pin CN1 connector is used for CARD-E09A attachment. For its function details, see the "CARD-E09A Hardware Manual."

Connector: Molex 53481-2409

CN1 : SH-Card?Connector			
Pin	Signal Name	Type	Function
1	GND	POWER	
2	BCD1#	O	PCMCIA slot-B signal
3	BCE1#	I	PCMCIA slot-B signal
4	BCE2#	I	PCMCIA slot-B signal
5	BOE#	I	PCMCIA slot-B signal
6	SLOT_B_V_{CC}	POWER	PCMCIA slot-B V_{CC} power
7	BVS1	O	PCMCIA slot-B signal
8	BIORD#	I	PCMCIA slot-B signal
9	BIOWR#	I	PCMCIA slot-B signal
10	BWE#	I	PCMCIA slot-B signal
11	BRDY_IRQ#	O	PCMCIA slot-B signal
12	BVS2	O	PCMCIA slot-B signal
13	BRESET	I	PCMCIA slot-B signal
14	BWAIT#	O	PCMCIA slot-B signal
15	V_{CC}	POWER	+3.3V (P3V) power
16	BREG#	I	PCMCIA slot-B signal
17	BBVD2_SPKR	O	PCMCIA slot-B signal
18	BBVD1_STSCHG#	O	PCMCIA slot-B signal

19	BWP_IOIS16#	O	PCMCIA slot-B signal
20	GND	POWER	Ground
21	BCD2#	O	PCMCIA slot-B signal
22	BADRENA#	I	PCMCIA slot-B signal
23	BDATAENA#	I	PCMCIA slot-B signal
24	BVPPPGM	I	PCMCIA slot-B VPP control signal
25	BVPPVCC	I	PCMCIA slot-B VPP control signal
26	BVCC5#	I	PCMCIA slot-B VCC control signal
27	BVCC3#	I	PCMCIA slot-B VCC control signal
28	KBCLK	I/O	Keyboard clock
29	KBDATA	I/O	Keyboard data
30	MSCLK	I/O	Mouse clock
31	MSDATA	I/O	Mouse data
32	RESETDRV	I	ISA-bus signal
33	IOCHRDY	O	ISA-bus signal
34	IOW#	I	ISA-bus signal
35	IOR#	I	ISA-bus signal
36	MEMCS16#	O	ISA-bus signal
37	SBHE#	I	ISA-bus signal
38	IOCS16#	O	ISA-bus signal
39	MEMR#	I	ISA-bus signal
40	MEMW#	I	ISA-bus signal
41	GND	POWER	
42	ISADATAENA#	I	ISA-bus data enable signal
43	RI4#	O	FIFO serial (16550-compatible) interface 4
44	DTR4#	I	FIFO serial (16550-compatible) interface 4
45	V_{CORE}	POWER	CPU core logic power
46	V_{CORE}	POWER	CPU core logic power
47	CTS4#	O	FIFO serial (16550-compatible) interface 4
48	TXD4	I	FIFO serial (16550-compatible) interface 4
49	RTS4#	I	FIFO serial (16550-compatible) interface 4
50	RXD4	O	FIFO serial (16550-compatible) interface 4
51	DSR4#	O	FIFO serial (16550-compatible) interface 4
52	DCD4#	O	FIFO serial (16550-compatible) interface 4
53	RI3#	O	FIFO serial (16550-compatible) interface 3
54	DTR3#	I	FIFO serial (16550-compatible) interface 3
55	CTS3#	O	FIFO serial (16550-compatible) interface 3
56	TXD3	I	FIFO serial (16550-compatible) interface 3
57	RTS3#	I	FIFO serial (16550-compatible) interface 3
58	RXD3	O	FIFO serial (16550-compatible) interface 3
59	DSR3#	O	FIFO serial (16550-compatible) interface 3
60	DCD3#	O	FIFO serial (16550-compatible) interface 3
61	GND	POWER	
62	CKIO	I	SH-bus signal (clock)
63	TCLK	O	
64	RESETP#	O	Reset signal (Power-ON reset)
65	RESETM#	O	Reset signal (Manual reset)
66	WAIT#	O	SH-bus signal
67	CS2#	I	SH-bus signal
68	CS0#	I	ROM control signal
69	RD/WR#	I	SH-bus signal
70	WE1#	I	SH-bus signal
71	WE0#	I	SH-bus signal
72	RD#	I	SH-bus signal

73	BS#	I	SH-bus signal
74	A25	I	Address bus
75	A24	I	Address bus
76	A23	I	Address bus
77	V_{CC}	POWER	+3.3V (P3V) power
78	A22	I	Address bus
79	A21	I	Address bus
80	A20	I	Address bus
81	A19	I	Address bus
82	GND	POWER	
83	A18	I	Address bus
84	A17	I	Address bus
85	A16	I	Address bus
86	A15	I	Address bus
87	A14	I	Address bus
88	A13	I	Address bus
89	A12	I	Address bus
90	A11	I	Address bus
91	A10	I	Address bus
92	A9	I	Address bus
93	A8	I	Address bus
94	A7	I	Address bus
95	A6	I	Address bus
96	A5	I	Address bus
97	A4	I	Address bus
98	A3	I	Address bus
99	A2	I	Address bus
100	A1	I	Address bus
101	GND	POWER	
102	A0	I	Address bus
103	D15	I/O	Data bus
104	D14	I/O	Data bus
105	D13	I/O	Data bus
106	V_{CC}	POWER	+3.3V (P3V) power
107	D12	I/O	Data bus
108	D11	I/O	Data bus
109	D10	I/O	Data bus
110	D9	I/O	Data bus
111	D8	I/O	Data bus
112	D7	I/O	Data bus
113	D6	I/O	Data bus
114	D5	I/O	Data bus
115	D4	I/O	Data bus
116	D3	I/O	Data bus
117	D2	I/O	Data bus
118	D1	I/O	Data bus
119	D0	I/O	Data bus
120	GND	POWER	
121	GND	POWER	
122	ACD1#	O	PCMCIA slot-A signal
123	ACE1#	I	PCMCIA slot-A signal
124	ACE2#	I	PCMCIA slot-A signal
125	AOE#	I	PCMCIA slot-A signal
126	SLOT_A_V_{CC}	POWER	PCMCIA slot-A V_{CC} power

127	AVS1	O	PCMCIA slot-A signal
128	AIORD#	I	PCMCIA slot-A signal
129	AIOWR#	I	PCMCIA slot-A signal
130	AWE#	I	PCMCIA slot-A signal
131	ARDY_IRQ#	O	PCMCIA slot-A signal
132	AVS2	O	PCMCIA slot-A signal
133	ARESET	I	PCMCIA slot-A signal
134	AWAIT#	O	PCMCIA slot-A signal
135	V_{CC}	POWER	+3.3V (P3V) power
136	AREG#	I	PCMCIA slot-A signal
137	ABVD2_SPKR	O	PCMCIA slot-A signal
138	ABVD1_STSCHG#	O	PCMCIA slot-A signal
139	AWP_IOIS16#	O	PCMCIA slot-A signal
140	GND	POWER	GND
141	ACD2#	O	PCMCIA slot-A signal
142	AADRENA#	I	PCMCIA slot-A signal
143	ADATAENA#	I	PCMCIA slot-A signal
144	AVPPPGM	I	PCMCIA slot-A VPP control signal
145	AVPPVCC	I	PCMCIA slot-A VPP control signal
146	AVCC5#	I	PCMCIA slot-A VCC control signal
147	AVCC3#	I	PCMCIA slot-A VCC control signal
148	CA25	I	Address bus
149	CA24	I	Address bus
150	CA23	I	Address bus
151	SLCT	O	Parallel IF signal
152	PE	O	Parallel IF signal
153	BUSY	O	Parallel IF signal
154	ACK#	O	Parallel IF signal
155	LPTD7	I/O	Parallel IF data
156	LPTD6	I/O	Parallel IF data
157	LPTD5	I/O	Parallel IF data
158	LPTD4	I/O	Parallel IF data
159	LPTD3	I/O	Parallel IF data
160	SLCTIN#	I/O	Parallel IF signal
161	GND	POWER	
162	LPTD2	I/O	Parallel IF data
163	INIT#	I/O	Parallel IF signal
164	LPTD1	I/O	Parallel IF data
165	V_{CORE}	POWER	CPU core logic power
166	V_{BK}	POWER	RTC backup power
167	ERROR#	O	Parallel IF signal
168	LPTD0	I/O	Parallel IF data
169	AFD#	I/O	Parallel IF signal
170	STROBE#	I/O	Parallel IF signal
171	STANDBY#	I	Standby (suspend) status signal
172	ROMDIS#	O	CARD-E09A internal ROM disable signal
173	RESERVE	-	-
174	EXTCLKI	O	Display controller external clock input
175	RESERVE	-	-
176	CA22	I	Address bus
177	TXD0	I	Serial IF 0
178	SCK0	I	Serial IF 0
179	RXD0	O	Serial IF 0
180	AN4	O	A/D converter port 4

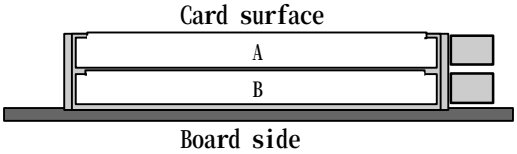
181	GND	POWER	
182	AN5	O	A/D converter port 5
183	DA1	I	A/D converter port 1
184	DA0	I	A/D converter port 0
185	TXD1	I	IrDA serial IF
186	RXD1	O	IrDA serial IF
187	TXD2	I	FIFO serial IF 2
188	RXD2	O	FIFO serial IF 2
189	RTS2#	I	FIFO serial IF 2
190	CTS2#	O	FIFO serial IF 2
191	PWOFF#	I	Power-OFF enable signal
192	SRBTN#	O	Suspend/Resume button signal
193	FPVCCON	I	LCD signal
194	PTC7/PINT7	I/O	I/O port/interrupt 7
195	PTC6/PINT6	I/O	I/O port/interrupt 7
196	PTC5/PINT5	I/O	I/O port/interrupt 7
197	V_{CC}	POWER	+3.3V (P3V) Power
198	PTC4/PINT4	I/O	I/O port/interrupt 4
199	PTC3/PINT3	I/O	I/O port/interrupt 3
200	PTC2/PINT2	I/O	I/O port/interrupt 2
201	PTC1/PINT1	I/O	I/O port/interrupt 1
202	GND	POWER	
203	DACK0#	I	DMA control signal
204	DREQ0#	O	DMA control signal
205	DACK1#	I	DMA control signal
206	DREQ1#	O	DMA control signal
207	NMI	O	Interrupt request signal
208	IRQ1	O	Interrupt request signal
209	IRQ2	O	Interrupt request signal
210	IRQ3	O	Interrupt request signal
211	IRQ4	O	Interrupt request signal
212	VSYNC	I	CRT signal
213	HSYNC	I	CRT signal
214	B	I	CRT signal
215	G	I	CRT signal
216	R	I	CRT signal
217	FPDAT15	I	LCD signal (data)
218	FPDAT14	I	LCD signal (data)
219	FPDAT13	I	LCD signal (data)
220	FPDAT12	I	LCD signal (data)
221	GND	POWER	
222	FPDAT11	I	LCD signal (data)
223	FPDAT10	I	LCD signal (data)
224	FPDAT9	I	LCD signal (data)
225	FPDAT8	I	LCD signal (data)
226	V_{CC}	POWER	+3.3V (P3V)
227	FPDAT7	I	LCD signal (data)
228	FPDAT6	I	LCD signal (data)
229	FPDAT5	I	LCD signal (data)
230	FPDAT4	I	LCD signal (data)
231	FPDAT3	I	LCD signal (data)
232	FPDAT2	I	LCD signal (data)
233	FPDAT1	I	LCD signal (data)
234	FPDAT0	I	LCD signal (data)

235	DOTCLK	I	LCD signal
236	MOD	I	LCD signal
237	FPVEEON	I	LCD signal
238	LINE	I	LCD signal
239	FRAME	I	LCD signal
240	GND	POWER	

3.2.PCMCIA Slots

Connector CN11 is a dual-slot PCMCIA interface. A type-II PC-card can be inserted into slot B, and a type-III PC-card can be inserted into slot A.

Slot A is a top connector. Slot B is a bottom connector as shown below.



Connectors

Header: 92140-040 (Slot B) or 92140-045 (Slot A)

Ejector: 95079-02CA (Slot B) or 95079-00CA (Slot A)

(Both made by BERG Corp.)

CN11 : PCMCIA Connector			
Pin	Signal Name	I/O	Function
1	GND	POWER	
2	A_D3	I/O	Slot-A data
3	A_D4	I/O	Slot-A data
4	A_D5	I/O	Slot-A data
5	A_D6	I/O	Slot-A data
6	A_D7	I/O	Slot-A data
7	ACE1#	I	Slot-A card enable signal
8	A_A10	O	Slot-A address
9	AOE#	O	Slot-A output enable signal
10	A_A11	O	Slot-A address
11	A_A9	O	Slot-A address
12	A_A8	O	Slot-A address
13	A_A13	O	Slot-A address
14	A_A14	O	Slot-A address
15	AWE1#	O	Slot-A write enable signal
16	ARDY_IRQ#	I	Slot-A ready/interrupt request signal
17	SLOT_A_V_{CC}	POWER	Slot-A VCC power
18	A_V_{PP1}	POWER	Slot-A VPP power
19	A_A16	O	Slot-A address
20	A_A15	O	Slot-A address
21	A_A12	O	Slot-A address
22	A_A7	O	Slot-A address
23	A_A6	O	Slot-A address
24	A_A5	O	Slot-A address
25	A_A4	O	Slot-A address
26	A_A3	O	Slot-A address
27	A_A2	O	Slot-A address
28	A_A1	O	Slot-A address
29	A_A0	O	Slot-A address
30	A_D0	I/O	Slot-A data

31	A_D1	I/O	Slot-A data
32	A_D2	I/O	Slot-A data
33	AWP_IOIS16#	I	Slot-A write protect (16-bit I/O signal)
34	GND	POWER	
35	GND	POWER	
36	ACD1#	I	Slot-A card detect signal
37	A_D11	I/O	Slot-A data
38	A_D12	I/O	Slot-A data
39	A_D13	I/O	Slot-A data
40	A_D14	I/O	Slot-A data
41	A_D15	I/O	Slot-A data
42	ACE2#	O	Slot-A card enable signal
43	AVS1	I	Slot-A voltage sense signal
44	AIORD#	O	Slot-A I/O read signal
45	AIOWR#	O	Slot-A I/O write signal
46	A_A17	O	Slot-A address
47	A_A18	O	Slot-A address
48	A_A19	O	Slot-A address
49	A_A20	O	Slot-A address
50	A_A21	O	Slot-A address
51	SLOT_A_V_{CC}	POWER	Slot-A I/O V_{CC} power
52	A_V_{PP2}	POWER	Slot-A I/O V_{PP} power
53	A_A22	O	Slot-A address
54	A_A23	O	Slot-A address
55	A_A24	O	Slot-A address
56	A_A25	O	Slot-A address
57	AVS2	I	Slot-A voltage sense signal
58	ARESET	O	Slot-A card reset signal
59	AWAIT#	I	Slot-A wait signal
60	NC	-	
61	AREG#	Tri	Slot-A register select signal
62	ABVD2_SPKR	I	Slot-A battery voltage sense/speaker signal
63	ABVD1_STSCHG#	I	Slot-A battery voltage sense/status change signal
64	A_D8	I/O	Slot-A data
65	A_D9	I/O	Slot-A data
66	A_D10	I/O	Slot-A data
67	ACD2#	I	Slot-A card detect signal
68	GND	POWER	
69	GND	POWER	
70	B_D3	I/O	Slot-B data
71	B_D4	I/O	Slot-B data
72	B_D5	I/O	Slot-B data
73	B_D6	I/O	Slot-B data
74	B_D7	I/O	Slot-B data
75	BCE1#	I	Slot-B card enable signal
76	B_A10	O	Slot-B address
77	BOE#	O	Slot-B output enable signal
78	B_A11	O	Slot-B address
79	B_A9	O	Slot-B address
80	B_A8	O	Slot-B address
81	B_A13	O	Slot-B address
82	B_A14	O	Slot-B address
83	BWE1#	O	lot-B write enable signal
84	BRDY_IRQ#	I	Slot-B ready/interrupt request signal

85	SLOT_B_V_{CC}	POWER	Slot-B V_{CC} power
86	B_V_{PP1}	POWER	Slot-B V_{PP} power
87	B_A16	O	Slot-B address
88	B_A15	O	Slot-B address
89	B_A12	O	Slot-B address
90	B_A7	O	Slot-B address
91	B_A6	O	Slot-B address
92	B_A5	O	Slot-B address
93	B_A4	O	Slot-B address
94	B_A3	O	Slot-B address
95	B_A2	O	Slot-B address
96	B_A1	O	Slot-B address
97	B_A0	O	Slot-B address
98	B_D0	I/O	Slot-B data
99	B_D1	I/O	Slot-B data
100	B_D2	I/O	Slot-B data
101	BWP_IOIS16#	I	Slot-B write protect I/O (16-bit I/O signal)
102	GND	POWER	
103	GND	POWER	
104	BCD1#	I	Slot-B card detect signal
105	B_D11	I/O	Slot-B data
106	B_D12	I/O	Slot-B data
107	B_D13	I/O	Slot-B data
108	B_D14	I/O	Slot-B data
109	B_D15	I/O	Slot-B data
110	BCE2#	O	Slot-B card enable signal
111	BVS1	I	Slot-B voltage sense signal
112	BIORD#	O	Slot-B I/O read signal
113	BIOWR#	O	Slot-B I/O write signal
114	B_A17	O	Slot-B address
115	B_A18	O	Slot-B address
116	B_A19	O	Slot-B address
117	B_A20	O	Slot-B address
118	B_A21	O	Slot-B address
119	SLOT_B_V_{CC}	POWER	Slot-B V_{CC} power
120	B_V_{PP2}	POWER	Slot-B V_{PP} power
121	B_A22	O	Slot-B address
122	B_A23	O	Slot-B address
123	B_A24	O	Slot-B address
124	B_A25	O	Slot-B address
125	BVS2	I	Slot-B voltage sense signal
126	BRESET	O	Slot-B card reset signal
127	BWAIT#	I	Slot-B wait signal
128	NC	-	
129	BREG#	Tri	Slot-B register select signal
130	BBVD2_SPKR	I	Slot-B battery voltage sense/speaker signal
131	BBVD1_STSCHG#	I	Slot-B battery voltage sense/status change signal
132	B_D8	I/O	Slot-B data
133	B_D9	I/O	Slot-B data
134	B_D10	I/O	Slot-B data
135	BCD2#	I	Slot-B card detect signal
136	GND	POWER	

3.3.ISH Extension Bus

Connector CN2 is a 100-pin extension bus which has SH-bus signals, ISA-bus signals and others. See the memory maps for their areas and addresses.

Connector: TX15-100P-LT-MH1 (JAE)

CN2 : ISH-bus Connector			
Pin	Signal Name	I/O	Function
1	GND	POWER	
2	RESETDRV	O	ISA-bus signal
3	IOCHRDY	I	ISA-bus signal
4	IOW#	O	ISA-bus signal
5	IOR#	O	ISA-bus signal
6	MEMCS16#	I	ISA-bus signal
7	SBHE#	O	ISA-bus signal
8	IOCS16#	I	ISA-bus signal
9	MEMR#	O	ISA-bus signal
10	MEMW#	O	ISA-bus signal
11	ISADATAENA#	O	ISA data enable signal
12	CKIO	O	SH-bus signal (clock)
13	TCLK	I	SH-bus signal (clock)
14	RESETP#	I	SH-bus signal (clock)
15	RESETM#	I	SH-bus signal (clock)
16	WAIT#	I	ISA-bus signal
17	CS2#	O	ISA-bus signal
18	RD/WR#	O	ISA-bus signal
19	WE1#	O	ISA-bus signal
20	WE0#	O	ISA-bus signal
21	RD#	O	ISA-bus signal
22	BS#	O	ISA-bus signal
23	GND	POWER	-
24	BA25	O	Address
25	BA24	O	Address
26	BA23	O	Address
27	BA22	O	Address
28	BA21	O	Address
29	BA20	O	Address
30	BA19	O	Address
31	BA18	O	Address
32	BA17	O	Address
33	BA16	O	Address
34	BA15	O	Address
35	BA14	O	Address
36	BA13	O	Address
37	BA12	O	Address
38	BA11	O	Address
39	BA10	O	Address
40	BA9	O	Address
41	BA8	O	Address
42	BA7	O	Address
43	BA6	O	Address
44	BA5	O	Address
45	BA4	O	Address

46	BA3	O	Address
47	BA2	O	Address
48	BA1	O	Address
49	BA0	O	Address
50	GND	POWER	-
51	GND	POWER	-
52	RESERVE	-	-
53	RESERVE	-	-
54	DA1	O	D/A conversion 1
55	RESERVE	-	-
56	STANDBY#	O	Standby signal
57	RESERVE	-	-
58	PWOFF#	O	Power-OFF signal
59	SRBTN#	I	Suspend/resume button signal
60	PTC7/PINT7	I/O	Port-C signal
61	PTC6/PINT6	I/O	Port-C signal
62	PTC5/PINT5	I/O	Port-C signal
63	PTC4/PINT4	I/O	Port-C signal
64	PTC3/PINT3	I/O	Port-C signal
65	PTC2/PINT2	I/O	Port-C signal
66	PTC1/PINT1	I/O	Port-C signal
67	FPVCCON	O	LCD signal
68	DACK0#	I/O	DMA signal
69	DREQ0#	I	DMA signal
70	DACK1#	I/O	DMA signal
71	DREQ1#	I	DMA signal
72	NMI	I	Interrupt request
73	GND	POWER	-
74	P5V	POWER	+5V power
75	P5V	POWER	+5V power
76	P5V	POWER	+5V power
77	P3V	POWER	+3.3V power
78	P3V	POWER	+3.3V power
79	P3V	POWER	+3.3V power
80	IRQ1	I	Interrupt request
81	IRQ2	I	Interrupt request
82	IRQ3	I	Interrupt request
83	IRQ4	I	Interrupt request
84	BD15	I/O	Data
85	BD14	I/O	Data
86	BD13	I/O	Data
87	BD12	I/O	Data
88	BD11	I/O	Data
89	BD10	I/O	Data
90	BD9	I/O	Data
91	BD8	I/O	Data
92	BD7	I/O	Data
93	BD6	I/O	Data
94	BD5	I/O	Data
95	BD4	I/O	Data
96	BD3	I/O	Data
97	BD2	I/O	Data
98	BD1	I/O	Data
99	BD0	I/O	Data
100	GND	POWER	-

3.4.LCD Connector

Connector CN3 is a 50-pin, header for LCD interface.

Connector: PS-50PE-D4T1-B1 (JAE)

CN3 : LCD I/F Connector			
Pin	Signal Name	Type	Function
1	V_{CC}	POWER	+3.3V or +5V power (*1)
2	GND	POWER	-
3	FRAME	O	Frame pulse signal
4	GND	POWER	-
5	LINE	O	Line pulse signal
6	GND	POWER	-
7	DOTCLK	O	Dot clock (shift clock)
8	GND	POWER	-
9	V_{CC}	POWER	+3.3V or +5V power (*1)
10	FPDAT8	O	Display data
11	FPDAT7	O	Display data
12	FPDAT6	O	Display data
13	FPDAT5	O	Display data
14	FPDAT4	O	Display data
15	V_{CC}	POWER	+3.3V or +5V power (*1)
16	GND	POWER	-
17	FPDAT3	O	Display data
18	FPDAT2	O	Display data
19	FPDAT1	O	Display data
20	FPDAT0	O	Display data
21	V_{CC}	POWER	+3.3V or +5V power (*1)
22	GND	POWER	-
23	FPVEEON	O	LCD power control signal
24	FPVCCON	O	LCD power control signal
25	MOD	O	Multi-purpose signal (*2)
26	MOD	O	Multi-purpose signal (*2)
27	GND	POWER	-
28	P12V	POWER	+12V power
29	P12V	POWER	+12V power
30	P12V	POWER	+12V power
31	GND	POWER	-
32	MOD	O	Multi-purpose signal (*2)
33	FPDAT9	O	Display data
34	FPDAT10	O	Display data
35	FPDAT11	O	Display data
36	V_{CC}	POWER	+3.3V or +5V power (*1)
37	GND	POWER	-
38	FPDAT12	O	Display data
39	FPDAT13	O	Display data
40	FPDAT14	O	Display data
41	FPDAT15	O	Display data
42	V_{CC}	POWER	+3.3V or +5V power (*1)
43	GND	POWER	-
44	GND	POWER	-
45	GND	POWER	-
46	RESERVE	-	NC
47	FPVEEON	O	LCD power control signal

48	RESERVE	-	NC
49	RESERVE	-	NC
50	RESERVE	-	NC

*1 +3.3VDC or +5VDC can be applied to V_{CC} pins, which is determined by JP3 setting.

JP3	Pins 1 and 2 connected	+3.3V (default)
	Pins 2 and 3 connected	+5V

*2 The MOD signals of pins 25, 26 and 32 are set to MOD signals, dot clocks, or display enable signals by setup of SED1355 display controller used in on the CARD-E09A. For these function details, see the SED1355 manual.

3.5.CRT Display Connector

Connector CN5 is a 15-pin, D-sub CRT display interface (IF).

Connector: 17HE-B13150-74HC1 (DDK)

CN5 : CRT Connector			
Pin	Signal Name	Type	Function
1	R	Analog O	RED
2	G	Analog O	GREEN
3	B	Analog O	BLUE
4	NC	-	-
5	GND	POWER	-
6	GND	POWER	-
7	GND	POWER	-
8	GND	POWER	-
9	NC	-	-
10	GND	POWER	-
11	NC	-	-
12	NC	-	-
13	HSYNC	O	Horizontal sync signal
14	VSYNC	O	Vertical sync signal
15	NC	-	-

3.6.Mouse and Keyboard Interface

Connector CN7 is a PS2 type mouse and keyboard interface. This connector allows direct connection of a PS2 mouse or a keyboard. A special branch connector is necessary to connect a keyboard and a mouse at the same time.

Connector: TCS7927-56-401 (Hoshiden)

CN7 : KB/MS Connector			
Pin	Signal Name	Type	Function
1	MSDATA	I/O	Mouse data
2	KBDATA	I/O	Keyboard data
3	GND	POWER	-
4	P5V	POWER	+5V power
5	MSCLK	I/O	Mouse clock
6	KBCLK	I/O	Keyboard clock

3.7.Parallel Port Interface

Connector CN9 is 26-pin header of a parallel port interface.

Connector: PS-26PE-D4T1-B1 (JAE)

CN9 : Parallel Connector			
Pin	Signal Name	Type	Function
1	STROBE#	I/O	Strobe signal
2	AFD#	I/O	Auto Feed signal
3	PD0	I	Data
4	ERROR#	I/O	Error signal
5	PD1	I/O	
6	INIT#	I/O	Initialize signal
7	PD2	I/O	Data
8	SLCTIN#	I/O	Select In signal
9	PD3	I/O	Data
10	GND	POWER	-
11	PD4	I/O	Data
12	GND	POWER	-
13	PD5	I/O	Data
14	GND	POWER	-
15	PD6	I/O	Data
16	GND	POWER	-
17	PD7	I/O	Data
18	GND	POWER	-
19	ACK#	I	Acknowledge signal
20	GND	POWER	-
21	BUSY	I	Busy signal
22	GND	POWER	-
23	PE	I	Paper End signal
24	GND	POWER	-
25	SLCT	I	Select signal
26	NC	-	-

3.8.Serial Port Interface

Connectors CN6, CN8 and CN10 are serial port interfaces with a 10-pin, header.

Connector CN6 is a serial port interface with FIFO from SH3. Connectors CN8 and CN10 are 16550-compatible serial port interface. They are connected via the RS-232C driver/receiver.

Connector: PS-10PE-D4T1-B1 (JAE)

CN6 : SCIF Connector			
Pin	Signal Name	Type	Function
1	NC	-	-
2	RESERVED	-	-
3	RXD2	I	Receive data
4	RTS2#	O	Request to send signal
5	TXD2	O	Transmit data
6	CTS2#	I	Clear to send data
7	RESERVED	-	-
8	NC	-	-
9	GND	POWER	-
10	NC	-	-

CN8 : SCIF3 Connector			
Pin	Signal Name	Type	Function
1	DCD3#	I	Data carrier detect signal
2	DSR3#	I	Data set ready signal
3	RXD3	I	Receive data
4	RTS3#	O	Request to send signal
5	TXD3	O	Transmit data
6	CTS3#	I	Clear to send signal
7	DTR3#	O	Data terminal ready signal
8	RI3#	I	Ring indicator signal
9	GND	POWER	-
10	NC	-	-

CN10 : SCIF4 Connector			
Pin	Signal Name	Type	Function
1	DCD4#	I	Data carrier detect signal
2	DSR4#	I	Data set ready signal
3	RXD4	I	Receive data
4	RTS4#	O	Request to send signal
5	TXD4	O	Transmit data
6	CTS4#	I	Clear to send signal
7	DTR4#	O	Data terminal ready signal
8	RI4#	I	Ring indicator signal
9	GND	POWER	-
10	NC	-	-

3.9.Miscellaneous Interface

Connector CN4 is a 10-pin herder with the following functions.

- Serial port interface from SH3 with no FIFO, and no driver/receiver.
- Serial port interface for IrDA 1.0; pins 7 and 8
- Power Off signal; pin 10
- +5V and +3.3V powers; pins 2 and 3

Connector: PS-10PE-D4T1-PN1

CN4 : MISC Connector			
Pin	Signal Name	Type	Function
1	NC	-	-
2	P5V	POWER	+5V power
3	P3V	POWER	+3.3V power
4	TXD0	O	Transmit data
5	SCK0	I/O	Serial clock
6	RXD0	I	Receive data
7	TXD1	O	Transmit data for IrDA 1.0
8	RXD1	I	Receive data for IrDA 1.0
9	GND	POWER	Ground
10	PSOFF	OD	Power control signal (Low for power On, High Z for power Off)

3.10.10BASE-T Interface

Connector CN13 is a 10BASE-T interface.

Connector: 290A-88-30-335 (Mitsumi)

CN13 : LAN Connector			
Pin	Signal Name	Type	Function
1	TDP	O	Transmit data (Positive)
2	TDM	O	Transmit data (Negative)
3	RDP	I	Receive data (Positive)
4	NC	-	-
5	NC	-	-
6	RDM	I	Receive data (Negative)
7	NC	-	-
8	NC	-	-

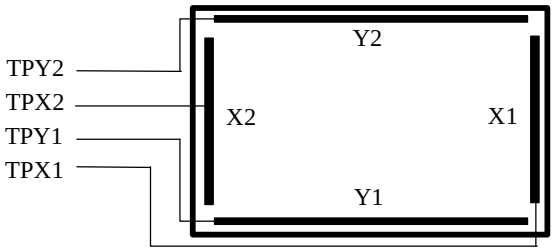
3.11.Touch Panel Connector

Connector CN14 is a 4-pin touch panel interface. It supports a four-wire, resistance membrane touch panel.

Connector: FFC-4CM1 (Honda)

CN14 : Touch Panel Connector			
Pin	Signal Name	Type	Function
1	TPX1	Analog I/O	
2	TPY1	Analog I/O	
3	TPX2	Analog I/O	
4	TPY2	Analog I/O	

Touch panel connection diagram.



Use the PTC4-2, AN5-4 and IRQ2 in the CARD-E09A.

State	CARD-E09A signals					
	PTC4 /PINT4 output value	PTC3 /PINT3 output value	PTC2 /PINT2 output value	AN5	AN4	IRQ2
Reads X	0	0	0		X-Read	
Reads Y	1	1	0	Y-Read		
waiting for interrupt	1	0	1			interrupt occurs at PEN DOWN
PEN UP/DOWN detection	1	0	1	Read		

3.12.Speaker Connectors

Connector CN12 is a dual-pin speaker connector. Terminal DA0 of D/A converter output of CARD-E09A is used.

Connector: 173981-2 (AMP)

CN12 : Speaker Connector			
Pin	Signal Name	Type	Function
1	SPEAKER+	Analog O	Speaker (Positive)
2	SPEAKER-	Analog O	Speaker (Negative)

3.13.PROM Socket

Connector CN15 is a 40-pin DIP PROM socket (with 5V power). It can be used if JP1 is connected. The PROMs having the 1M-bit (64K by 16 bits), 2M-bit (128K by 16 bits), and 4M-bit (256K by 16 bits) JEDEC standard pin assignment can be used.

CN15 : PROM Socket			
Pin	Signal Name	Type	Function
1	V_{PP}	-	(Connected to V_{SS} on the board)
2	CE#	O	Chip enable
3	I/O 15	I	Data
4	I/O 14	I	Data
5	I/O 13	I	Data
6	I/O 12	I	Data
7	I/O 11	I	Data
8	I/O 10	I	Data
9	I/O 9	I	Data
10	I/O 8	I	Data
11	V_{SS}	POWER	Ground
12	I/O 7	I	Data
13	I/O 6	I	Data
14	I/O 5	I	Data
15	I/O 4	I	Data
16	I/O 3	I	Data
17	I/O 2	I	Data
18	I/O 1	I	Data
19	I/O 0	I	Data
20	OE#	O	Output enable
21	A0	O	Address
22	A1	O	Address
23	A2	O	Address
24	A3	O	Address
25	A4	O	Address
26	A5	O	Address
27	A6	O	Address
28	A7	O	Address
29	A8	O	Address
30	V_{SS}	POWER	Ground
31	A9	O	Address
32	A10	O	Address
33	A11	O	Address
34	A12	O	Address
35	A13	O	Address
36	A14	O	Address
37	A15	O	Address
38	A16	O	Address
39	A17	O	Address
40	V_{CC}	POWER	+5V power

3.14.Backup Battery

CN17 is a backup battery holder, and a CR2032 manganese dioxide lithium battery can be used.

Battery holder: HL32-A2 (Sony)

CN17 : Battery Holder			
Pin	Signal Name	Type	Function
1	+	POWER	Battery positive terminal
2	-	POWER	Battery negative terminal

Battery used: CR2032 (3V, 220 mAh)

3.15.LEDS

LED4 and LED5 are power status indicator LEDs.

- Green LED4 lights when the power turns on.
- Orange LED5 lights when the power is ready to off. (*)

* LED5 switching is meaningful only when the PWOFF# signal (pin 191 of card) is controlled by a software.

3.16.Suspend/Resume Switch

The SW2 push button switch is used for suspend or resume request (or power-off ready request).

3.17.Manual Reset Switch

The SW3 push button switch is used for manual function reset. (When the SW3 switch is pressed, the RESETM# signal is set to Low.)

3.18.Power-On Reset Switch

The SW1 push button switch is used for power-on reset. (When the SW1 switch is pressed, the RESETP# signal is set to Low.)

3.19.Power Input Connector

CN16 is a 4-pin, power input connector. Although the +5V and +12V power inputs are available, this Evaluation board can operate with the +5V power only in the following cases.

- The card inserted into the PCMCIA slot does not use the +12V power.
- The LCD panel does not use the +12V power.

Connector: 178454-1 (AMP)

CN16 : Power Connector			
Pin	Signal Name	Type	Function
1	P12V	POWER	+12V power
2	GND	POWER	
3	GND	POWER	
4	P5V	POWER	+5V power

3.20.External Clock Input for Display Controller

The CARD-E09A has the reference clock select function for SED1355 display controller. Although the SED1355 usually operates at 33 MHz, the External Clock Input mode can be selected if the reference clock needs to be adjusted for the LCD connected.

To select the External Clock Input mode, enter clocks into TP5 (through hole terminal) of the board. TP5 is connected to the EXTCLKI signal (pin 174) of CN1. Additional software setup is required. For details, see the manual of SH-CARD Windows CE2.11 Development Kit.

4.JUMPER SETTINGS

The board has three jumper connectors (JP1, JP2 and JP3).

JP1: Boot ROM selection

Short	System starts with the PROM mounted on CN15. (Default)
Open	System starts with the internal ROM of CARD-E09A. The PROM at CN15 is ignored.

The JP1 is connected when delivered. Open it if you do not have a PROM.

JP2: V_{CORE} selection

Pins 1 and 2 shorted	V_{CORE}=3.3Vis set
Pins 2 and 3 shorted	V_{CORE}=1.9V (Default) **Caution: Use this setup for CARD-E09A.**

JP3: LCD V_{CC} (CN3, pin 1, 9, 15 and 21) selection

Pins 1 and 2 shorted	V_{CC}=3.3V
Pins 2 and 3 shorted	V_{CC}=5V

5.POWER SUPPLY SPECIFICATION

The following provides the power supply specifications of the board.

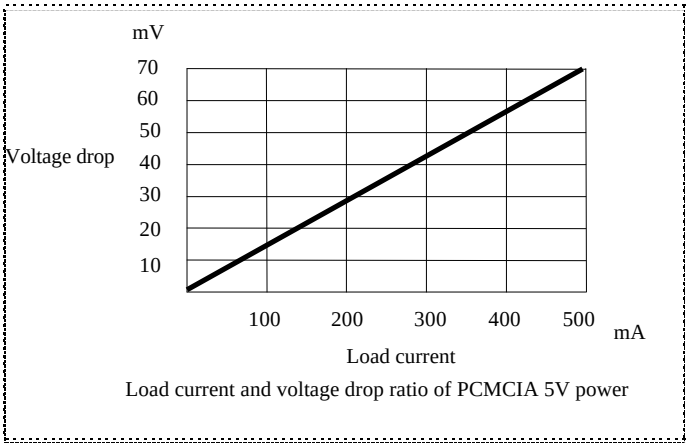
Power supply	Name on board	Input voltage at CN16 and tolerance
+5V	P5V	+5.0V +/-5% (Note1)
+12V	P12V	+12.0V (Note 2)

Power supply	Name on board	Supply voltage and accuracy
+3.3V	P3V	+3.3V ±0.1V
CPU core power supply	V_{CORE}	+1.9V ±0.1V
RTC backup power supply	V_{BK}	+2.0V to +3.6V (V_{BK} =< P3V)

The +5V power is converted by on board power circuit and supplied to the +3.3V and CPU core power circuits. Also, the lithium battery and +3.3V powers are switched and supplied to the RTC backup power circuit.

Note 1. The board has the 5V devices with +/-5% voltage tolerance. However, the following points should be considered.

When the +5V power is supplied to the PCMCIA slot, the voltage may drop due to the resistance of PCMCIA power switch circuit as follows. Check the power supply specifications of the PC card and its load current before use.

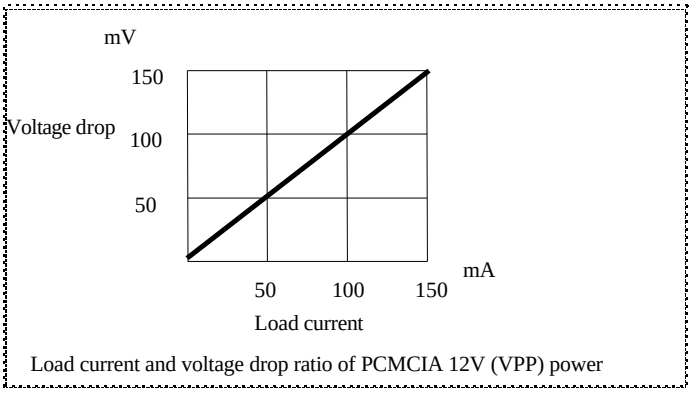


Load current and voltage drop ratio of PCMCIA 5V power

Note 2. Consider the following two points and use the +12V power having the required accuracy.

(a) Follow the accuracy of load circuit to be connected to the +12V power supply of LCD panel IF (CN3).

(b) Similar to the +5V power supply, the +12V voltage may drop at PCMCIA slot due to the resistance of power switching circuit. Check the power supply specifications and load current of the PC card before its use.

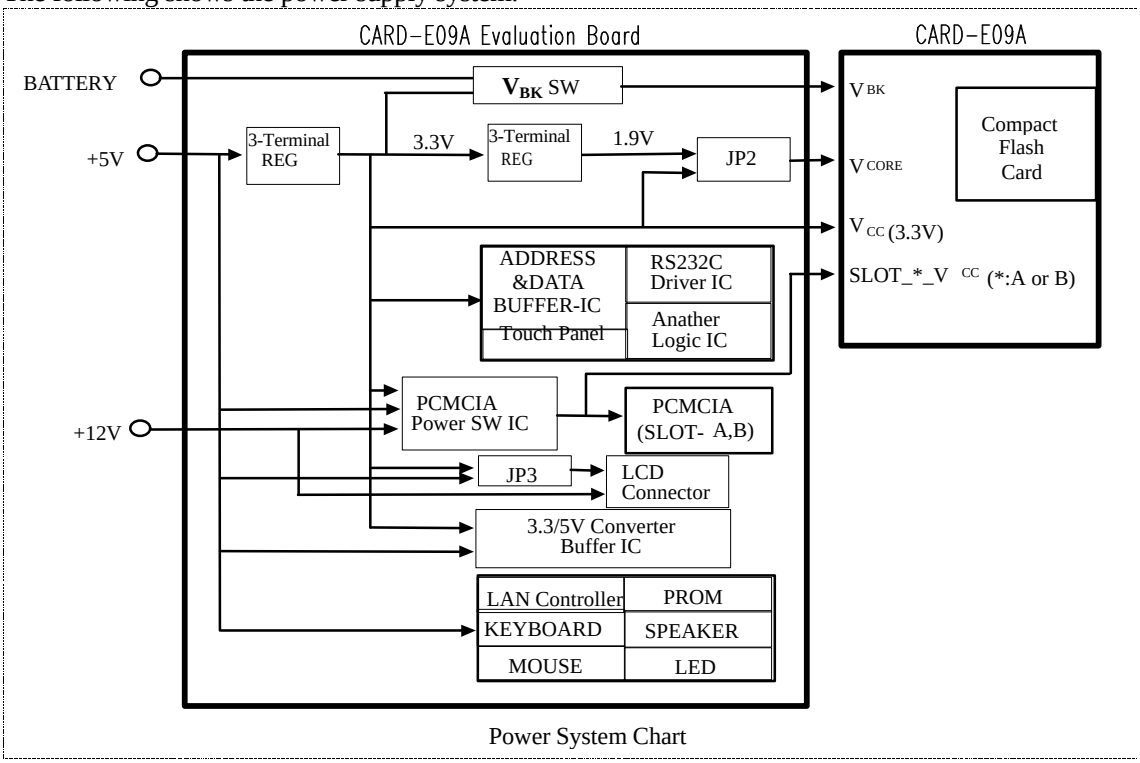


Load current and voltage drop ratio of PCMCIA 12V (VPP) power

6.CURRENT CONSUMPTION

6.1.Power System Chart

The following shows the power supply system.



Power System Chart

6.2.Current Consumption (Reference)

The following provides the reference current consumption of CARD-E09A. Supply the power to connector CN16 according to your application. For current consumption of the CARD-E09A and Compact Flash Card, see the respective manuals.

		5V (Converted) Power Supply	12V Power Supply
CARD-E09A Evaluation Board (excluding CARD-E09A)	Keyboard	100mA typ	
	PROM	30mA typ	
	Others (3.3V system)	80mA typ	
	Others (5V system)	80mA typ	
	PCMCIA SLOT-A	120mA max	60mA max **(*1)**
	PCMCIA SLOT-B	120mA max	60mA max **(*1)**
	LCD I/F VCC	100mA max	100mA max **(*1)**
	Power for ISH expansion bus	500mA max **(*2)**	

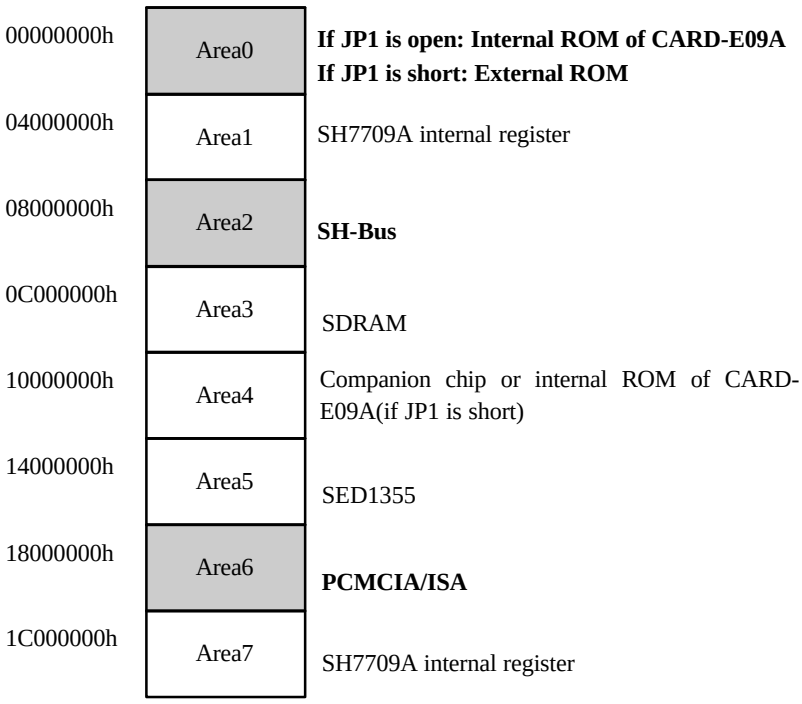
*1 Not required if the card and LCD do not use the +12V power.

*2 Maximum value available on the ISH expansion bus, including the current consumption of devices of 16-bit LED current on the ISH board and those mounted in the universal area.

7.MEMORY MAP

7.1.SH7709A Memory Map

The following provides the standard SH7709A memory map of EPROM, PCMCIA, ISA-bus and SH-bus areas. For details, see the "CARD-E09A Hardware Manual."



Area 0

The system operation starts from area 0 after reset.

If JP1 is open, the internal flash ROM of CARD-E09A is used as area 0. If JP1 is short, the PROM mounted on CN15 can be used as area 0.

In later case, the internal ROM of CARD-E09A is seen as area 4.

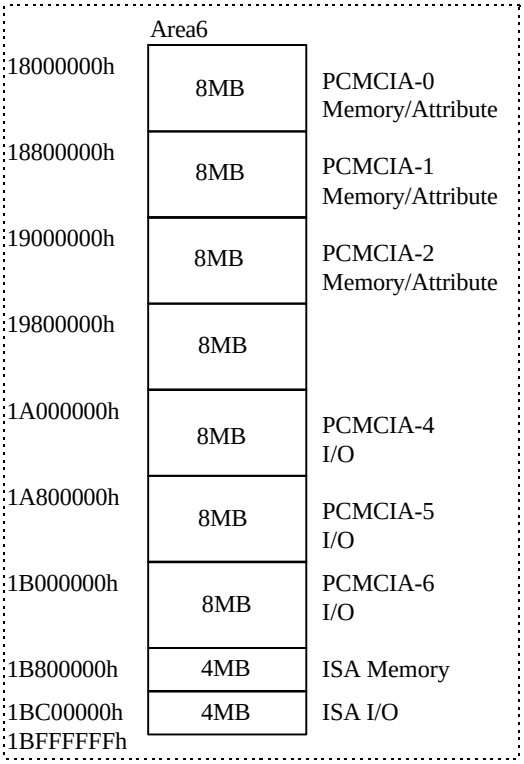
Area 2

Area 2 can be used through the ISH expansion bus of CN2.

The chip select signal of area 2 is CS#2. Addresses BA0 to BA25 of ISH expansion bus are used. Data of BD0 to BD15 of ISH expansion bus are used together with ISA-bus.

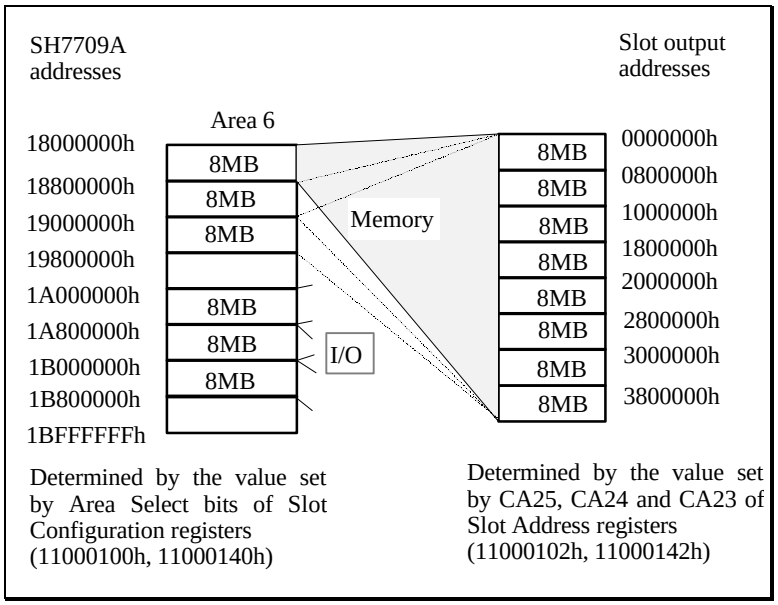
Area 6

The following addresses are assigned inside of area 6.



7.2.PCMCIA Slot Addresses

Upper address bits (A23, A24 and A25) of PCMCIA slot A and slot B are determined by "Slot Address Register" of CARD-E09A. Refer to "CARD-E09A Hardware Manual" in detail.



Item	Effective address	Explanation
PCMCIA slot address	A0 to A25	A23, A24 and A25 are determined by "Slot Address Register A" and "Slot Address Register B".

7.3.ISH-Bus and ISA-Bus of ISH Expansion Bus

7.3.1.SH-bus

Signals of area 2 of SH7709A are directly connected to ISH expansion bus.

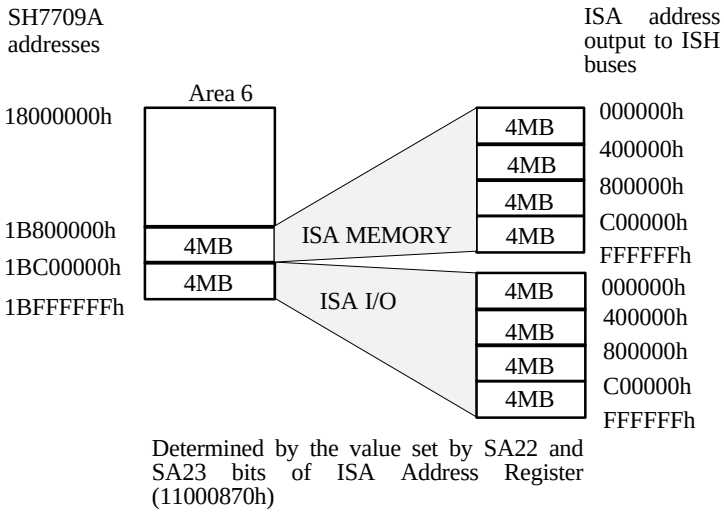
Item	Effective address	Explanation
SH-bus of ISH expansion bus	BA0 to BA25	-

7.3.2.ISA-bus

The SH7709A addresses are mapped as shown above. Upper address bits output to the ISA-bus are determined by "ISA Address Register" of CARD-E09A. For details, refer to the "CARD-E09A Hardware Manual."

Item	Effective address	Explanation
ISA-bus address of ISH expansion bus	BA0 to BA23	BA22 and BA23 are determined by "ISA Address Register."

The following provides the relationship between ISA memory map and addresses.



ISA-bus Areas of LAN Controller

The following shows the LAN controller areas on ISA-bus, and they are determined by population of resistor R30, R31, R32 and R33. (High-order 2 bits of address are used for BA22 or BA23 selection.)

The LAN area of BA22=0 and BA23=0 is set when delivered.

Signal	Address value	R30	R32	R31	R33
BA23	**0**	**OPEN**	Mounted	-	-
	1	Mounted	**OPEN**	-	-
BA22	**0**	-	-	**OPEN**	Mounted
	1	-	-	Mounted	**OPEN**

Summary table

The following provides a relationship between SH and ISA-bus of ISH expansion bus.

Signal	SH-bus	ISA-bus
A25	A	-
A24	A	-
A23	A	A
A22	A	A
A21-0	A	A
D15-D0	A	A
CKIO, BS#, RD#, RD/WR#, WE0#, WE1#, WAIT#, CS2#	A	-
SBHE#, IOR#, IOW#, IOCS16#, MEMR#, MEMW#, MEMCS16#, IOCHRDY, RESETDRV, ISADATAENA#	-	A

A: available

7.4.U1, U2, U6 and U7 Functions

U1, U2, U6, and U7 ICs on this board control data and addresses. U2 shown in he reference circuit diagram for this board includes other functions than 3.3 to 5-volt and 5 to 3.5-volt conversion. When you want to see the details of this section, see the separate reference circuit diagram covering the U2 functions.

8.LAN FUNCTIONS

8.1.Outline

Evaluation board uses the REALTEK's RTL8019AS Ethernet controller that meets the IEEE 802.3 Standards and is compatible to NE2000 series. The controller has the following features.

- 16K-byte SRAM buffer (included in RTL8019AS)
- 10BASE-T interface

RTL8019AS is connected to the ISA-bus on the CARD-E09A (refer to the chapter describing the memory map)

8.2.Internal Registers

The RTL8019AS has two types of registers: the NE2000-compatible and RTL8019AS unique registers, and the plug-and-play (called "PnP") registers. As this board has no PnP setup, the PnP register description is omitted.

8.3.NE2000-Compatible and RTL8019AS Unique Registers

The following lists the registers compatible to NE2000 series and those unique to the RTL8019AS controller. The registers shown in boldface are unique to the RTL8019AS, are others are compatible to the NE2000.

Registers are accessed through page mapping, and any of four total pages can be accessed by setup of bits 6 and 7 (PS1 and PS0) of CR register. During access, bits 6 and 7 of CR register must be set. Then, data can be written or read via the appropriate I/O port.

PAGE=0 （PS1=0, PS0=0）

Index	Read	Write
00h	Command register (CR)	Command register (CR)
01h	Current Local DMA address 0 (CLDA0)	Page Start register (PSTART)
02h	Current Local DMA address 1 (CLDA1)	Page Stop register (PSTOP)
03h	Boundary pointer (BNDR)	Boundary pointer (BNRY)
04h	Transmit Status register (TSR)	Transmit Page Start address (TPSR)
05h	Number of Collisions register (NCR)	Transmit Byte Count register 0 (TBCR0)
06h	FIF0	Transmit Byte Count register 1 (TBCR1)
07h	Interrrupt Status register (ISR)	Interrrupt Status register (ISR)
08h	Current Remote DMA address 0 (CRDA0)	Remote Start Address register 0 (RSAR0)
09h	Current Remote DMA address 1 (CRDA1)	Remote Start Address register 1 (RSAR1)
0Ah	**8019ID0**	Remote Byte Count register 0 (RBCR0)
0Bh	**8019ID1**	Remote Byte Count register 1 (RBCR1)
0Ch	Receive Status register (RSR)	Receive Configuration resister (RCR)
0Dh	Tally counter 0 (CNTR0)	Transmit Configuration resister (TCR)
0Eh	Tally counter 1 (CNTR1)	Data Configuration resister (DCR)
0Fh	Tally counter 2 (CNTR2)	Interrupt Mask register (IMR)
10-17	Remote DMA Port	
18-1F	Reset Port	

PAGE=1 （PS1=0, PS0=1）

Index	Read	Write
00h	Command register (CR)	Command register (CR)
01h	Physical Address register 0 (PAR0)	Physical Address register 0 (PAR0)
02h	Physical Address register 1 (PAR1)	Physical Address register 1 (PAR1)
03h	Physical Address register 2 (PAR2)	Physical Address register 2 (PAR2)
04h	Physical Address register 3 (PAR3)	Physical Address register 3 (PAR3)
05h	Physical Address register 4 (PAR4)	Physical Address register 4 (PAR4)
06h	Physical Address register 5 (PAR5)	Physical Address register 5 (PAR5)
07h	Current Page register (CURR)	Current Page register (CURR)
08h	Multicast Address register 0 (MAR0)	Multicast Address register 0 (MAR0)
09h	Multicast Address register 1 (MAR1)	Multicast Address register 1 (MAR1)
0Ah	Multicast Address register 2 (MAR2)	Multicast Address register 2 (MAR2)
0Bh	Multicast Address register 3 (MAR3)	Multicast Address register 3 (MAR3)
0Ch	Multicast Address register 4 (MAR4)	Multicast Address register 4 (MAR4)
0Dh	Multicast Address register 5 (MAR5)	Multicast Address register 5 (MAR5)
0Eh	Multicast Address register 6 (MAR6)	Multicast Address register 6 (MAR6)
0Fh	Multicast Address register 7 (MAR7)	Multicast Address register 7 (MAR7)
10-17	Remote DMA Port	
18-1F	Reset Port	

PAGE=2 （PS1=1, PS0=0）

Index	Read	Write
00h	Command register (CR)	Command register (CR)
01h	Page Start register (PSTART)	-Read only-
02h	Page Stop register (PSTOP)	-Read only-
03h	-Reserved-	-Read only-
04h	Transmit Page Start address (TPSR)	-Read only-
05h	-Reserved-	-Read only-
06h	-Reserved-	-Read only-
07h	-Reserved-	-Read only-
08h	-Reserved-	-Read only-
09h	-Reserved-	-Read only-
0Ah	-Reserved-	-Read only-
0Bh	-Reserved-	-Read only-
0Ch	Receive Configuration resister (RCR)	-Read only-
0Dh	Transmit Configuration resister (TCR)	-Read only-
0Eh	Data Configuration resister (DCR)	-Read only-
0Fh	Interrupt Mask register (IMR)	-Read only-
10-17	Remote DMA Port	
18-1F	Reset Port	

PAGE=3 （PS1=1, PS0=1）

Index	Read	Write
00h	Command register (CR)	Command register (CR)
01h	**9346CR**	**9346CR**
02h	**BPAGE**	**BPAGE**
03h	**CONFIG0**	-Reserved-
04h	**CONFIG1**	**CONFIG1**
05h	**CONFIG2**	**CONFIG2**
06h	**CONFIG3**	**CONFIG3**
07h	-Reserved-	**TEST**
08h	**CSNSAV**	-Reserved-
09h	-Reserved-	**HLTCLK**
0Ah	-Reserved-	-Reserved-
0Bh	**INTR**	-Reserved-
0Ch	-Reserved-	**FMWP**
0Dh	**CONFIG4**	-Reserved-
0Eh	-Reserved-	-Reserved-
0Fh	-Reserved-	-Reserved-
10-17	Remote DMA Port	
18-1F	Reset Port	

8.3.1.NE2000-Compatible Registers

Command register (CR) (00h; R/W type)

Used for register page selection, enabling or disabling of remote DMA operations, and command issue.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Explanation</th></tr>
<tr><td>7,6</td><td>PS1,PS0</td><td>Page Select:
<table>
<tr><th>PS1</th><th>PS0</th><th>Register page</th><th>Explanation</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>NE2000 compatible</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>NE2000 compatible</td></tr>
<tr><td>1</td><td>0</td><td>2</td><td>NE2000 compatible</td></tr>
<tr><td>1</td><td>1</td><td>3</td><td>Unique to RTL8019AS</td></tr>
</table></td></tr>
<tr><td>5 to 3</td><td>RD2 to RD0</td><td>Remote DMA Command:
<table>
<tr><th>RD2</th><th>RD1</th><th>RD0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Not allowed</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Remote Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Remote Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Transmits packets.</td></tr>
<tr><td>1</td><td>*</td><td>*</td><td>Aborts or completes remote DMA.</td></tr>
</table></td></tr>
<tr><td>2</td><td>TXP</td><td>Transmit Packet bit:
This bit must always be set for packet transfer. When packet transfer is completed or aborted, this bit is internally reset. Nothing occurs when zeros (0s) are written.</td></tr>
<tr><td>1</td><td>STA</td><td>Start bit:
This bit does not affect on system control. A value written in this bit can be read only. (It is set to zero (0) during power-up.)</td></tr>
<tr><td>0</td><td>STP</td><td>Stop bit:
This bit is the STOP command. When set, no packets are sent or received at all. (It is set to one (1) during power-up.)
<table>
<tr><th>STA</th><th>STP</th><th>Function</th></tr>
<tr><td>1</td><td>0</td><td>Start command</td></tr>
<tr><td>0</td><td>1</td><td>Stop command</td></tr>
</table></td></tr>
</table>

Interrupt Status register (ISR) (07h; Page 0; R/W type)

This register indicates the status of Network Interface controller (NIC), and it is used to determine an interrupt cause. It is cleared when each bit is set to 1. Also, the register must be cleared after power-up.

Bit	Symbol	Explanation
7	RST	Reset Status: This bit is set when the NIC is reset, and cleared when the Start command is issued for CR. Also, the bit is set when the receive buffer is overflowed, and cleared when one or more packets are read from the buffer.
6	RDC	Remote DMA Complete: Set when remote DMA has completed.
5	CNT	Counter Overflow: Set when the MSB is set on one or more Network Tally counters.
4	OVW	Overwrite Warning: Set when the Receive buffer is exhausted.
3	TXE	Transmit Error: Set if packet transfer is not completed due to excessive collision.
2	RXE	Receive Error: Set when a packet having one or more following errors is received. - CRC error - Frame alignment error - Packet missing
1	PTX	Packet Transmitted: This bit shows that packets have been transmitted without errors.
0	PRX	Packet Received: This bit shows that packets have been received without errors.

Interrupt Mask register (IMR) (0Fh; Page 0; W type) (0Fh; Page 2; R type)

All bits correspond to the bits of ISR register. They are all zeros (0s) during power-up. An interrupt is enabled when its bit is set.

Bit	Symbol	Explanation
7	—	—
6	RDCE	DMA Complete Interrupt Enable:
5	CNTE	Counter Overflow Interrupt Enabel:
4	OVWE	Overwrite Warning Interrupt Enabel:
3	TXEE	Transmit Error Interrupt Enable:
2	RXEE	Receive Error Interrupt Enable:
1	PTXE	Packet Transmitted Interrupt Enable:
0	PRXE	Packet Received Interrupt Enable:

Data Configuration register (DCR) (0Eh; Page 0; W type) (0Eh; Page 2; R type)

Bit	Symbol	Explanation
7	—	Always 1
6,5	FT1,FT0	FIFO Threshold Select: FIFO Threshold Select bits 1 and 0
4	ARM	Auto Initialize Remote: 0: Does not execute the transmit command. 1: Executes the transmit command.
3	LS	Loopback Select: 0: Select the Loopback mode. Bits 1 and 2 of TCR must also be set to allow loopback operations. 1: Selects the normal operation mode.
2	LAS	Long Address Select: This bit must be set to zero (0). This NIC supports the dual 16-bit DMA mode only. (It is set to 1 during power-up.)
1	BOS	Byte Order Select: 0: Sets the MS byte in MD15 to 8, and LS byte in MD7 to 0. (32xxx, 80x86) 1: Sets the MS byte in MD7 to 0, and LS byte in MD15 to 8. (680x0)
0	WTS	Word Transfer Select: 0: Selects the byte-width DMA transfer. 1: Selects the word-width DMA transfer.

Transmit Configuration register (TCR) (0Dh; Page 0; W type) (0Dh; Page 2; R type)

Bit	Symbol	Explanation
7	—	Always 1
6	—	Always 1
5	—	Always 1
4	OFST	Collision Offset Enable bit
3	ATD	Auto Transmit Disable: 0: Normal operation 1: Disables the transmitter when it receives a multicast address hashed to bit 62, and enables the transmitter when it receives a multicast address hashed to bit 63.
2,1	LB1,LB0	Encoded Loopback Control:
0	CRC	Inhibit CRC:

	LB1	LB0	Explanation
Mode0	0	0	Normal operation
Mode1	0	1	Internal loopback
Mode2	1	0	External loopback
Mode3	1	1	External loopback

Setup		CRC logic operation	
CRC bit	MODE	CRC Generator	CRC Checker
0	Normal	Enabled	Disableld
1	Normal	Disabled	Enabled
0	Loopback	Enabled	Disabled
1	Loopback	Disabled	Enabled

Transmit Status register (TSR) (04h; Page 0; R type)

This register shows the packet transmission status.

Bit	Symbol	Explanation
7	OWC	Out of Window Collision: This bit is set when a collision is detected after slot time (51.2 microseconds). Similar to the usual collision, packets are rescheduled and transmitted.
6	CDH	CD Heartbeat: The NIC must start the Collision signal (CD Heartbeat signal) within the first 6.4 microseconds of the interframe gap following the transmission. This bit is set if the transceiver cannot transmit this signal.
5	—	Always 0
4	CRS	Carrier Sense Lost: This bit is set if a carrier is lost during packet transmission.
3	ABT	Transmit Aborted: This bit shows that packet transmission is aborted due to excessive collision.
2	COL	Transmit Collided: This bit shows that packet transmission is collided to another station of network.
1	—	Always 1
0	PTX	Packet Transmitted: This bit shows that packet transmission has completed without errors.

Receive Configuration register (RCR) (0Ch; Page 0; W type) (0Ch; Page 2; R type)

Bit	Symbol	Explanation
7	—	Always 1
6	—	Always 1
5	MON	When the Monitor Mode bit is set, the receive packets are checked for their addresses, CRC and frame alignment. But they are not buffered in memory. Otherwise, the packets are buffered in memory.
4	PRO	Promiscuous Physical: If PRO=1, all packets have physical addresses are accepted. If PRO=0, packets are accepted if their physical node address matches the station address set by PAR0 to PAR5.
3	AM	Accept Multicast: If AM=1, the packets having the multicast destination addresses are accepted. If AM=0, the packets having the multicast destination addresses are rejected.
2	AB	Accept Broadcast: If AB=1, the packets having the broadcast destination addresses are accepted. If AB=0, the packets having the broadcast destination addresses are rejected.
1	AR	Accept Runt Packets: If AR=1, the packets shorter than 64 bytes are accepted. If AR=0, the packets shorter than 64 bytes are rejected.
0	SEP	Save Errored Packets: If SEP=1, a packet having a receive error is accepted. If SEP=0, a packet having a receive error is rejected.

Receive Status register (RSR) (0Ch; Page 0; R type)

Bit	Symbol	Explanation
7	DFR	Deferring: This bit is set when a carrier or collision is detected.
6	DIS	Receive Disable: This bit is set when the NIC enters the Monitor mode, and the receiver is disabled. This bit is reset when the Monitor mode is ended and the receiver is enabled.
5	PHY	Physical/Multicast Address: The PHY bit is set when the receive packet has a multicast or broadcast destination address. It is reset when the receive packet has a physical destination address.
4	MPA	Missed Packet: This bit is set when a packet is rejected by the NIC due to insufficient receive buffer or Monitor mode selected. The CNTR2 tally counter is incremented.
3	—	Always 0
2	FAE	Frame Alignment Error: This bit shows that the input packet does not end on the byte boundary or its CRC does not match the last byte boundary. The CNTR0 tally counter is incremented.
1	CRC	CRC Error: This bit shows that the receive packet has a CRC error. This bit is also set during FAE error. The CNTR1 tally counter is incremented.
0	PRX	Packet Received Intact: This bit shows that the packets have been received without errors.

Current Local DMA registers 0 and 1 (CLDA0 and 1) (01h and 02h; Page 0; R type)

The current local DMA address can be obtained from these two registers.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLDA1	A15	A14	A13	A12	A11	A10	A9	A8
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLDA0	A7	A6	A5	A4	A3	A2	A1	A0

Page Start register (PSTART) (01h; Page 0; W type) (01h; Page 2; R type)

This register sets the Start Page address of receive buffers.

Page Stop register (PSTOP) (02h; Page 0; W type) (02h; Page 2; R type)

This register sets the Stop Page address of receive buffers.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSTART/ PSTOP	A15	A14	A13	A12	A11	A10	A9	A8

Boundary register (BNRY) (03h; Page 0; R/W type)

This register is used to prevent an overwrite of receive buffers. It is usually used as a pointer to the Receive Buffer page that the host has recently read.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BNRY	A15	A14	A13	A12	A11	A10	A9	A8

Transmit Page Start register (TPSR) (04h; Page 0; W type)

This register sets the Start Page address of packets transmitted.

	Bit 7	Bit 6	Bit5	Bit 4	Bit3	Bit2	Bit 1	Bit 0
TPSR	A15	A14	A13	A12	A11	A10	A9	A8

Transmit Byte Count registers 0 and 1 (TBCR0 and 1) (05h and 06h; Page 0; W type)

The transmit packet length (in bytes) is set in these two registers.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit0
TBCR1	TBC15	TBC14	TBC13	TBC12	TBC11	TBC10	TBC9	TBC8
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBCR0	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0

Number of Collisions register (NCR) (05h; Page 0; R type)

This register stores the number of collision times occurring during packet transmission.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NCR	0	0	0	0	NC3	NC2	NC1	NC0

First-In, First-Out register (FIFO) (06h; Page 0; R type)

The FIFO contents after loopback can be checked by use of this register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO	D7	D6	D5	D4	D3	D2	D1	D0

Current Remote DMA Address registers 0 and 1 (CRDA0 and 1) (08h and 09h; Page 0; R type)

Current address of remote DMA is stored in these two registers.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRDA1	A15	A14	A13	A12	A11	A10	A9	A8
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRDA0	A7	A6	A5	A4	A3	A2	A1	A0

Remote Start Address registers 0 and 1 (RSAR0 and 1) (08h and 09h; Page 0; W type)

The Start address of remote DMA is set in these two registers.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSAR1	A15	A14	A13	A12	A11	A10	A9	A8
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSAR0	A7	A6	A5	A4	A3	A2	A1	A0

Remote Byte Count registers 0 and 1 (RBCR0 and 1) (0Ah and 0Bh; Page 0; W type)

The data byte count of remote DMA is set in these two registers.

	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBCR1	RBC15	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBCR0	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0

Frame Alignment Error Tally Counter register (CNTR0) (0Dh; Page 0; R type)

	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNTR0	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

CRC Error Tally Counter register (CNTR1) (0Eh; Page 0; R type)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNTR1	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

Missed Packet Tally Counter register (CNTR2) (0Fh; Page 0; R type)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNTR2	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0

Physical Address registers (PAR0 to PAR5) (01h to 06h; Page 1; R/W type)

The Ethernet node addresses are set in these registers. They are compared with the destination address of input packets, and used for packet acceptance or rejection.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Current Page register (CURR) (07h; Page 1; R/W type)

This register points to the page address of the first receive buffer page to be used for packet reception.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CURR	A15	A14	A13	A12	A11	A10	A9	A8

Multicast Address registers (MAR0 to 7) (08h to 0Fh; Page 1; R/W type)

These registers provide the filtering bits of multicast addresses to be hashed by the CRC logic.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MAR0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MAR1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MAR2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MAR3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MAR4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MAR5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MAR6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MAR7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

8.3.2.Registers Unique to RTL8019AS

As introduced above, the registers unique to RTL8019AS are used in Page 0 and Page 3 as follows.

Page 0: An ID of the 8019AS can be read.

INDEX	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	**8019ID0**	R	0	1	0	1	0	0	0	0
0Bh	**8019ID1**	R	0	1	1	1	0	0	0	0

The following explains the contents of unique registers used in Page 3.

9346CR Register （01h ）

<table>
<tr><th>Bit</th><th>Symbol</th><th>TYPE</th><th>Explanation</th></tr>
<tr><td>7-6</td><td>EEM1-0</td><td>R/W</td><td>Selects an RTL8019AS operation mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Normal operation mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (DP8390-compatible)</td></tr>
<tr><td>0</td><td>1</td><td>Auto Load:
When this mode is selected, the RTL8019AS loads the 93C46 contents similar to the time when the RSTDRV is activated. (The load time is 2 msec.)
When data load is completed, it operation is automatically returned to the normal mode (EEM1=EEM0=0). The CR register is reset to 21h.</td></tr>
<tr><td>1</td><td>0</td><td>93C46 Programming:
In this mode, both local and remote DMA operations are disabled. The 93C46 can be accessed directly by use of bits 3 to 1 that reflect each status of EECS, EESK, EEDI, and EEDO pins.</td></tr>
<tr><td>1</td><td>1</td><td>Config Register Write Enable:
This mode must be selected to write data in CONFIG1 to 3 registers of Page 3.</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>-</td><td>-</td><td>Not used</td></tr>
<tr><td>3</td><td>EECS</td><td>R/W</td><td rowspan="4">Reflect each status of EECS, EESK, EEDI, and EEDO pins in the Auto Load mode or 93C46 Programming mode.</td></tr>
<tr><td>2</td><td>EESK</td><td>R/W</td></tr>
<tr><td>1</td><td>EEDI</td><td>R/W</td></tr>
<tr><td>0</td><td>EEDO</td><td>R</td></tr>
</table>

BPAGE register （ 02h ）

This register selects a BROM page that is read by the host. However, this Evaluation board does not support the BROM and this register is not used.

CONFIG0 register （ 03h ）

Bit	Symbol	TYPE	Explanation
7and6	VERID	R/W	Controller (RTL8019AS) version ID Bit7 / Bit6 / Mode 0 / 0 / Initial value is 0. Write-enabled if EEM1=EEM0=1 of 9346CR register.
5	AUI	R	1: If 10Base5 mode is selected or if AUI (pin 64) is set to high 0: Others It is always zero (0) on this board.
4	PNPJP	R	Indicates the JP status of pin 66. It is zero (0) on this board.
3	JP	R	Indicates the JP status of pin 65. It is zero (0) (not jumpered) on this board.
2	BNC	R	It is set to one (1) when the 10BASE2 mode is selected and the following is satisfied. (1) PL1=PL0=0 (Auto Detect mode) and the Link test has failed. (2) PL1=PL0=1 (10BASE2 mode)
1and0	-	R	Always zero (0)

CONFIG1 register （ 04h ）

<table>
<tr><th>Bit</th><th>Symbol</th><th>TYPE</th><th>Explanation</th></tr>
<tr><td>7</td><td>IRQEN</td><td>R/W</td><td>It is the IRQS2_0 status control.
1 = It goes high when interrupt request is issued, and goes low when the request is not present.
0 = Turns on the tri-state output.
Initial value of this bit is 9346CR. When the register EEM1 = EEM0 = 1, overwrite is enabled.</td></tr>
<tr><td>6to4</td><td>IRQS2-0</td><td>R</td><td>IRQ select: It is used for selecting which of INT 7 - 0 of RTL8019AS to be used. Outputs not selected are forced to tri-state.
When specified from setting on EEPROM, this board selects INT0. This output is connected to IRQ1 on the CARD-E09A.
<table>
<tr><th>IRQS2</th><th>IRQS1</th><th>IRQS0</th><th>Interrupt line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>INT0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>INT1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>INT2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>INT3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>INT4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>INT5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>INT6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>INT7</td></tr>
</table></td></tr>
<tr><td>3to0</td><td>I0S3-0</td><td>R</td><td>It is used for selecting base address of I/O (see Note).
When specified from setting on EEPROM, this board selects 300h.
<table>
<tr><th>IOS3</th><th>IOS2</th><th>IOS1</th><th>IOS0</th><th>I/O base address</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>300h</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>320h</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>340h</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>360h</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>380h</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3A0h</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>3C0h</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>3E0h</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>200h</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>220h</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>240h</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>260h</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>280h</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>2A0h</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>2C0h</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>2E0h</td></tr>
</table></td></tr>
</table>

NOTE: The RTL8019A is connected to the ISA-bus of CARD-E09A. When the I/O base is set to 300 (hex), the bit configuration on this board is, in practice, as shown below.

- Both bits 4 and 5 of ISA Address Register of CARD-E09A are set to 0.
- The address gained access is 1BC0030h of Area-6.

CONFIG2 register （ 05h ）

<table>
<tr><th>Bit</th><th>Symbol</th><th>TYPE</th><th>Explanation</th></tr>
<tr><td>7and6</td><td>PL1-0</td><td>R/W</td><td>Selects a network media type.
<table>
<tr><th>PL1</th><th>PL0</th><th>Media type</th></tr>
<tr><td>0</td><td>0</td><td>TP/CX auto-detect
(10baseT link test is enabled.)</td></tr>
<tr><td>0</td><td>1</td><td>10BaseT with link test disabled</td></tr>
<tr><td>1</td><td>0</td><td>10Base5</td></tr>
<tr><td>1</td><td>1</td><td>10Base2</td></tr>
</table></td></tr>
<tr><td>5</td><td>BSELB</td><td>R/W</td><td>When this bit is set to 1, the BROM is disabled regardless of BS4 to 0 setup. Initial value is 0, and it is write-enabled if EEM1=EEM0=1 of 9346CR register.</td></tr>
<tr><td>4 to 0</td><td>BS4-0</td><td>R</td><td>Sets the BROM size and memory base address.
<u>This board does not support the BROM.</u>
<table>
<tr><th>BS4</th><th>BS3</th><th>BS2</th><th>BS1</th><th>BS0</th><th>BROM Base & Size</th></tr>
<tr><td>0</td><td>0</td><td>*</td><td>*</td><td>*</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>C000h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>C800h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>D000h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>D800h, 32K</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>C000h, 64K</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>D000h, 64K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C000h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C400h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>C800h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>CC00h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>D000h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>D400h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>D800h, 16K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>DC00h, 16K</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>C000h, Page</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>C400h, Page</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>C800h, Page</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>CC00h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>D000h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>D400h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>D800h, Page</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>DC00h, Page</td></tr>
</table>
<table>
<tr><th>BROM Size</th><th>BA14</th><th>BA15</th></tr>
<tr><td>16K</td><td>High</td><td>High</td></tr>
<tr><td>32K</td><td>SA14</td><td>High</td></tr>
<tr><td>64K</td><td>SA14</td><td>SA15</td></tr>
</table></td></tr>
</table>

CONFIG3 register （ 06h ）

<table>
<tr><th>Bit</th><th>Symbol</th><th>TYPE</th><th>Explanation</th></tr>
<tr><td>7</td><td>PNP</td><td>R</td><td>When this bit is set to 1, the RTL8019AS is operating in the PNP mode. This bit is set when the PNP pin is high or when the PNP bit of 93C46 is set in Jumper-less mode. It can be ignored in the Jumper mode.</td></tr>
<tr><td>6</td><td>FUDUP</td><td>R</td><td>When this bit is set, the RTL8019AS is set to the full-duplex mode that allows simultaneous transmission and reception on the twisted-pair link to the full-duplex Ethernet switching hub.</td></tr>
<tr><td>5and4</td><td>LEDS1-0</td><td>R</td><td>Selects an output of LED2 to 0.
<table>
<tr><th>LEDS0</th><th>LED0 Pin</th></tr>
<tr><td>0</td><td>LED_COL</td></tr>
<tr><td>1</td><td>LED_LINK</td></tr>
</table>
<table>
<tr><th>LEDS1</th><th>LED1 Pin</th><th>LED2 Pin</th></tr>
<tr><td>0</td><td>LED_RX</td><td>LED_TX</td></tr>
<tr><td>1</td><td>LED_CRS</td><td>MCSB</td></tr>
</table></td></tr>
<tr><td>3</td><td>-</td><td>-</td><td>Reserved. Value 1 must not be written.</td></tr>
<tr><td>2</td><td>SLEEP</td><td>R/W</td><td>Selects the Sleep mode as follows.
1: Sleep mode
0: Normal mode
Initial value is 0, and it is write-enabled if EEM1=EEM0=1 of 9346CR register.</td></tr>
<tr><td>1</td><td>PWRDN</td><td>R/W</td><td>Selects the Power Down mode as follows.
1: Power Down mode
0: Normal mode
The initial value is obtained from the 93C46, and it is write-enabled if EEM1=EEM0=1 of 9346CR register.
There are two types of Power Down mode, depending on the HLTCKL register setup.
(1) Mode 1: Power down with clock operation
(2) Mode 2: Power down with stopped clock
In both mode types, the serial network interface and transceiver of RTL8019AS are turned off. All network operations are ignored. Also, all LED signals (except for LEDBNC) are set to high. In Mode 2, the internal clock of RTL8019AS is stopped. Usually, the registers (except for HLTCLK) cannot be accessed in this mode.</td></tr>
<tr><td>0</td><td>ACTIVEB</td><td>R</td><td>This is an inverse of bit 0 of PnP Activate register (index 30h).
When the RTL8019AS is deactivated, an I/O access to group-1 registers (except for BROM memory read and HLTCLK registers) is ignored. The HLTCLK register and PnP logic are operated in the normal way.</td></tr>
</table>

TEST register （07h）

Bit	Symbol	TYPE	Explanation
7 to 0	-	-	Reserved. Write-inhibited.

CSNSAV register （08h; R type）

(This register is used to backup the CSN assigned to the PnP CSN register.)

HLTCLK register （09h; W type）

Bit	Symbol	TYPE	Explanation
7 to 0	HLT7-0	W	Halt Clock register: This is an only register that the controller can access to during inactive. Data writing is invalid except for Power Down mode.

Write value	Power Down mode
52h	Mode 1: Power down with clock operation
48h	Mode 2: Power down with stopped clock
Others	Ignored

INTR register （0Bh; R type）

The ISA-bus status of INT7 to 0 pins is reflected.

FMWP register （0Ch; W type）

Bit	Symbol	TYPE	Explanation
7 to 0		W	Flash Memory Write Protect: Meaningless as this board does not use flash memory. It is write-enabled if EEM1=EEM0=1 of 9346CR register. Data can be written into the flash memory by two times of continuous data writing (57h and 58h). If a value other than 57h and 58h is written, the write sequence is aborted and memory is write-protected.

CONFIG4 register （0Dh; R type）

Bit	Symbol	TYPE	Explanation
7 to 1	-	-	Reserved.
0	IOMS	R	1: Uses SA15 to SA0 for I/O address decoding by NE2000 register. (I/O address full decoding) 0: Uses SA9 to SA0 for I/O address decoding by NE2000 register.

8.4.RTL8019AS Configuration Setup Mode

The RTL8019AS supports three configuration modes by jumper setup, RT jumperless setup, and PnP setup. This Evaluation board uses the RT jumperless setup mode by the hardware setup as shown at the bottom of the table. Pin 65 is set to low, pin 66 is set to low, and PNP bit of EEPROM (93C46) is set to 0 (not equal to PNP) to select the RT jumperless setup mode.

JP pin (pin 65)	PNP pin (pin 66)	PNP bit of 93C46	Configuration mode
High	*	*	Jumper mode
Low	High	*	PnP mode
Low	*	1	PnP mode
Low	**Low**	**0**	**RT jumperless mode**

The resource configuration information of RTL8019AS (such as I/O base address and interrupt request lines) is stored in CONFIG3 to 0 registers of Page 3 as explained above. The initial value of these registers depend on the EEPROM contents in RT jumperless mode. It is loaded from the EEPROM when the Auto Load command is executed or when the hardware reset signal is issued to the RTL8019AS.

If the value is modified after startup, it is held in the CONFIG3 to 0 registers and used. However, the new configuration value is lost when the Auto Load command is executed, the hardware reset is issued to the RTL8019AS, or the power supply is turned off.

The initial value cannot be changed on this board as its modification means the modification of EEPROM contents.

8.5.Initial Value of Configuration Registers

The following lists the initial values of CONFIG1 to 4 registers that are set when the Auto Load command is executed or when the hardware reset signal is generated.
The value of "Before loaded" is the value that has been loaded from the EEPROM.
The value of "93C46" storage value" is the value that is contained in the EEPROM and loaded when triggered.
The value in shaded area is the bit to be set initially regardless of EEPROM contents.

CONFIG1

Bit	7	6	5	4	3	2	1	0
Name	IRQEN	IRQS2	IRQS1	IRQS0	IOS3	IOS2	IOS1	IOS0
Before loaded	1	-	-	-	-	-	-	-
93C46 storage value	0	0	0	0	0	0	0	0
Initial value	1	0	0	0	0	0	0	0

CONFIG2

Bit	7	6	5	4	3	2	1	0
Name	PL1	PL0	BSELB	BS4	BS3	BS2	BS1	BS0
Before loaded	-	-	0	-	-	-	-	-
93C46 storage value	0	1	0	0	0	0	0	0
Initial value	0	0	0	0	0	0	0	0

CONFIG3

Bit	7	6	5	4	3	2	1	0
Name	PNP	FUDUP	LEDS1	LEDS0	-	SLEEP	PWRDN	ACTIVEB
Before loaded	0	-	-	-	-	0	-	0
93C46 storage value	0	1	0	0	0	0	0	0
Initial value	0	1	0	0	0	0	0	0

CONFIG4

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	IOMS
Before loaded	-	-	-	-	-	-	-	-
93C46 storage value	0	0	0	0	0	0	0	1
Initial value	0	0	0	0	0	0	0	1

9.TERMINAL CHARACTERISTICS

9.1.CARD-E09A Connectors

"Termination-1" gives the termination specifications of CARD-E09A. The value in parentheses are valid if SLOT_A_V_{CC} or SLOT_B_V_{CC} is 5V.

"Termination-2" gives the termination specifications of this board.

I/O type and termination

Signal Name	Type	Termination-1 (SH Card)	Termination-2 (Board)
ACD1#, ACD2#, AVS1, AVS2, BCD1#, BCD2#, BVS1, BVS2	O	100KPU	-
ARDY_IRQ#, AWAIT#, ABVD2_SPKR, ABVD1_STSCHG#, AWP_IOIS16#, BRDY_IRQ#, BWAIT#, BBVD2_SPKR, BBVD1_STSCHG#, BWP_IOIS16#,	O	100K(60K)PU	-
ACE1#, ACE2#, AOE#, AIORD#, AIOWR#, AWE#, ARESET, AREG#, BCE1#, BCE2#, BOE#, BIORD#, BIOWR#, BWE#, BRESET, BREG#	I (Tri)	-	-
AADRENA#, ADATAENA#, AVPPPGM, AVPPVCC, AVCC5#, AVCC3#, BADRENA#, BDATAENA#, BVPPPGM, BVPPVCC, BVCC5#, BVCC3#,	I	-	-
DREQ0#, DREQ1#	O	100KPU	-
DACK0#, DACK1#	I	-	-
RESETDRV, IOW#, IOR#, SBHE#, MEMR#, MEMW#, ISADATAENA#	I	-	-
IOCHRDY, MEMCS16#, IOCS16#,	O	-	1.2KPU
TXD0, SCK0	I	-	-
RXD0	O	100KPU	-
TXD1	I	-	-
RXD1	O	100KPU	-
TXD2, RTS2#	I	Active PU	-
RXD2,CTS2#	O	100KPU	-
TXD3, TXD4, DTR3#, DTR4#, RTS3#, RTS4#	I	-	-
RXD3, RXD4, DSR3#, DSR4#, CTS3#, CTS4#, DCD3#, DCD4#, RI3#, RI4#	O	50KPU	-
IRQ1-4	O	60KPU	-
NMI	O	100KPU	-
SRBTN#	O	60KPU	1.2KPU
STANDBY#, PWOFF#	I	-	-
CKIO, CS0#, CS2#, RD/WR#, WE1#, WE0#, RD#, BS#	I	-	-
WAIT#	O	4.7KPU	-
ROMDIS#	O	50KPU	-
TCLK	O	100KPU	-
RESETP#, RESETM#	O	-	1.2KPU

DA0, DA1	I	-	-
PTC7/PINT7-PTC1/PINT1	I/O	60KPU	-
LINE, FRAME, DOTCLK, MOD, FPVCCON, FPVEEON, FPDAT0-15	I	-	-
VSYNC, HSYNC, LINE	I	-	-
B,G,R	I	150PD	-
EXTCLKI	O	100KPU	-
KBCLK, KBDATA, MSCLK, MSDATA	I/O D	-	1.2 KPU (5V)
SLCT, PE, BUSY, ACK#, ERROR#	O	-	10KPU (5V)
SLCTIN#, INIT#, AFD#, STROBE#, LPTD7-0	I/O	-	10KPU (5V)
A25-22	I	HOLD	-
A21-0	I	-	-
CA25-22	I	-	-
D15-8	I/O	100KPU	-
D7-0	I/O	HOLD	-

9.2.PCMCIA Slot

The following provides the signal characteristics when the CARD-E09A is inserted into CN1 socket. The values in parentheses of "Termination" column are valid when SLOT_A_V_{CC} or SLOT_B_V_{CC} is 5V.

Termination and Output

Signal Name	Type	Termination 3.3V(5V)	Drive(mA) 3.3V/5V I_{OL}	I_{OH}	Output voltage(V) V_{OL} [max]	V_{OH} [min]
A_D0-15	I/O	100K(60K)PD	2/3	-2/-3	0.4	SLOT_A_V_{CC}-0.4
B_D0-15	I/O	100K(60K)PD	2/3	-2/-3	0.4	SLOT_B_V_{CC}-0.4
ACE1#, ACE2#, AOE#, AWE1#, AIORD#, AIOWR#, ARESET	O	100KPU	2/3	-2/-3	0.4	SLOT_A_V_{CC}-0.4
BCE1#,BCE2#, BOE#, BWE1#, BIORD#, BIOWR#, BRESET	O	100KPU	2/3	-2/-3	0.4	SLOT_B_V_{CC}-0.4
A_A0-25	O		2/3	-2/-3	0.4	SLOT_A_V_{CC}-0.4
B_A0-25	O		2/3	-2/-3	0.4	SLOT_B_V_{CC}-0.4
AREG#	Tri		2/3	-2/-3	0.4	SLOT_A_V_{CC}-0.4
BREG#	Tri		2/3	-2/-3	0.4	SLOT_B_V_{CC}-0.4
ARDY_IRQ#, AWP_IOIS16#, AWAIT#, ABVD2_SPKR, ABVD1_STSCHG#, BRDY_IRQ#, BWP_IOIS16#, BWAIT#, BBVD2_SPKR, BBVD1_STSCHG#	I	100K(60K)PU				
ACD1#, ACD2#, AVS1, AVS2, BCD1#, BCD2#, BVS1, BVS2	I	100KPU				

Input

Signal Name	Type	Input Low(V) V_{IL} [min]	V_{IL} [max]	Input High(V) V_{IH} [min]	V_{IH} [max]
A_D0-15	I/O	GND	0.8/1.0	2.0/3.5	SLOT_A_V_{CC}
B_D0-15	I/O	GND	0.8/1.0	2.0/3.5	SLOT_B_V_{CC}
ARDY_IRQ#, AWP_IOIS16#, AWAIT#, ABVD2_SPKR, ABVD1_STSCHG#,	I	GND	0.8/0.8	2.0/2.0	SLOT_A_V_{CC}
BRDY_IRQ#, BWP_IOIS16#, BWAIT#, BBVD2_SPKR, BBVD1_STSCHG#	I	GND	0.8/0.8	2.0/2.0	SLOT_B_V_{CC}
ACD1#, ACD2#, AVS1, AVS2, BCD1#, BCD2#, BVS1,2	I	GND	0.6	2.4	V_{CC}

9.3.ISH Expansion Bus

Termination and Output

Signal Name	Type	Termination	Drive(mA) I_{OL}	Drive(mA) I_{OH}	Output Voltage(V) V_{OL} [max]	Output Voltage(V) V_{OH} [min]
RESETDRV, IOW#, IOR#, SBHE#, MEMR#, MEMW#, STANDBY#	O	-	6	-6	0.4	P3V-0.4
ISADATAENA#	O	-	2	-2	0.4	P3V-0.4
CKIO, CS2#, RD/WR#, WE1#, WE0#, RD#, BS#	O	-	2	-2	0.4	P3V-0.4
PWOFF# DACK0#, DACK1#	O	-	1.6	-0.2	0.55	2.4
FPVCCON	O	60KPU	1.6	-0.2	0.55	2.4
DA1	O	-	-	-	-	-
BA25-22	O	-	6	-6	0.4	P3V-0.4
BA21-0	O	-	2	-2	0.4	P3V-0.4
BD15-0	I/O	100KPD	2	-2	0.4	P3V-0.4
PTC7/PINT7 -PTC1/PINT1	I/O	60KPU	1.6	-0.2	0.55	2.4
IOCHRDY, MEMCS16#, IOCS16#, RESETP#, RESETM#, NMI	I	1.2KPU				
TCLK, WAIT#, SRBTN#, DREQ0#, DREQ1#	I	100KPU				
IRQ1-4	I	60KPU				

Input

Signal Name	Type	Input Low(V) V_{IL} [min]	Input Low(V) V_{IL} [max]	Input High(V) V_{IH} [min]	Input High(V) V_{IH} [max]
IOCHRDY, MEMCS16#, IOCS16#	I	GND	0.8	2.0	5.5
TCLK, WAIT#, SRBTN#, DREQ0#, DREQ1#	I	-0.3	P3Vx0.2	2.0	P3V+0.3
RESETP# **(**Cautions**),** RESETM#, NMI	I	-0.3	P3Vx0.1	P3Vx0.9	P3V+0.3
IRQ1-4	I	-0.3	0.5	P3V-0.5	P3V+0.3
PTC7/PINT7-PTC1/PINT1	I/O	-0.3	P3Vx0.2	2.0	P3V+0.3
BD15-0	I/O	GND	0.8	2.0	P3V

Cautions: The RESET# signal must not exceed 0.5V if the RTC is backed up when the system power supply is off. (This rule must also be used during transient of power on/off switching.)

9.4.LCD Connector

Output

Signal Name	Type	Drive(mA)		Output voltage(V)	
		I_{OL}	I_{OH}	V_{OL} [max]	V_{OH} [min]
FRAME, LINE, DOTCLK, MOD, FPDAT15-0	O	6	-6	0.3	P3V-0.3
FPVEEON	O	2	-2	0.3	P3V-0.3
FPVCCON	O	1.6	-0.2	0.55	2.4

9.5.CRT Connector

Termination and output

Signal Name	Type	Termination	Drive(mA)		Output voltage(V)	
			I_{OL}	I_{OH}	V_{OL} [max]	V_{OH} [min]
R, G, B	Analog Out	150ΩPD	-	-	-	-
HSYNC, VSYNC	O	-	6	-6	0.3	P3V-0.3

9.6.Mouse and Keyboard Connectors

Termination and output

Signal Name	Type	Termination	Drive(mA)		Output voltage(V)	
			I_{OL}	I_{OH}	V_{OL} [max]	V_{OH} [max]
MSDATA, KBDATA, MSCLK, KBCLK	I/OD	1.2KPU[5V]	12	-	0.4	-

Input

Signal Name	Type	Input Low(V)		Input High(V)	
		V_{IL} [min]	V_{IL} [max]	V_{IH} [min]	V_{IH} [max]
MSDATA, KBDATA, MSCLK, KBCLK	I/OD	GND	0.8	2.0	5.5

9.7.Parallel IF

Termination and output

Signal Name	Type	Termination	Drive(mA)		Output voltage(V)	
			I_{OL}	I_{OH}	V_{OL} [max]	V_{OH} [min]
STROBE#, AFD#, INIT#, SLCTIN#	I/OD	10KPU[5V]	12	-	0.4	-
ERROR#, ACK#, BUSY, PE, SLCT	I	10KPU[5V]	-	-	-	-
PD0-7	I/OD	10KPU[5V]	6	-	0.4	-

Input

Signal Name	Type	Input Low(V)		Input High(V)	
		V_{IL} [min]	V_{IL} [max]	V_{IH} [min]	V_{IH} [max]
STROBE#, AFD3, INIT#, SLCTIN#	I/OD	GND	0.8	2.0	5.5
ERROR#, ACK#, BUSY, PE, SLCT	I	GND	0.8	2.0	5.5
PD0-7	I/OD	GND	0.8	2.0	5.5

9.8.Serial IF

Termination and output

Signal Name	Type	Termination	Input Low(V)		Input High(V)	
			V_{IL} [min]	V_{IL} [max]	V_{IH} [min]	V_{IH} [max]
RXD2, CTS2#	I	5.5KPD	-30	0.8	2.0	30
RTS2#, TXD2	O	-	-	-	-	-

Termination and output

Signal Name	Type	Termination	Input Low(V)		Input High(V)	
			V_{IL} [min]	V_{IL} [max]	V_{IH} [min]	V_{IH} [max]
DCD3#, DCD4#, DSR3#, DSR4#, RXD3, RXD4 CTS3#, CTS4# RI3#, RI4#	I	5.5KPD	-30	0.8	2.0	30
RTS3#, RTS4# TXD3, TXD4 DTR3#, DTR4#	O	-	-	-	-	-

9.9.Miscellaneous(Serial and IrDA)IF

Output

Signal Name	Type	Drive(mA)		Output voltage(V)	
		I_{OL}	I_{OH}	V_{OL} [max]	V_{OH} [min]
TXD0, SCK0, TXD1	O	1.6	-0.2	0.55	2.4
PSOFF	OD	10	-	0.3	-

Input

Signal Name	Type	Input Low(V)		Input High(V)	
		V_{IL} [min]	V_{IL} [max]	V_{IH} [min]	V_{IH} [max]
RXD0,1	I	0.3	P3Vx0.2	2.0	P3V+0.3

9.10.10BASE-T Connector

Signal Name	Type
TDP	O
TDM	O
RDP	I
NC	-
NC	-
RDM	I
NC	-
NC	-

9.11.Touch Panel Connector

Signal Name	Type
TPX1	Analog I/O
TPY1	Analog I/O
TPX2	Analog I/O
TPY2	Analog I/O

9.12.Speaker Connector

Signal Name	Type
SPEAKER+	Analog Out
SPEAKER-	Analog Out

9.13.EPROM Socket

Termination and output

Signal Name	Type	Termination	Drive(mA)		Output voltage(V)	
			I_{OL}	I_{OH}	V_{OL} [max]	V_{OH} [min]
CE#, OE3, A17-0	O	-	2	-2	0.4	P3V-0.4
I/O 15 -0	I	60KPD	-	-	-	-

Input

Signal Name	Type	Input Low(V)		Input High(V)	
		V_{IL} [min]	V_{IL} [max]	V_{IH} [min]	V_{IH} [max]
I/O 15 -0	I	GND	1.0	3.5	P5V

9.14.Backup Battery

Backup voltage(V)	
V_{IN}(Min)	V_{IN}(Max)
2.6	3.6

9.15.Power Input

Signal name	Voltage
P12V	+12V
GND	
GND	
P5V	+5V

10.CARD-E09A MOUNTING PROCEDURE

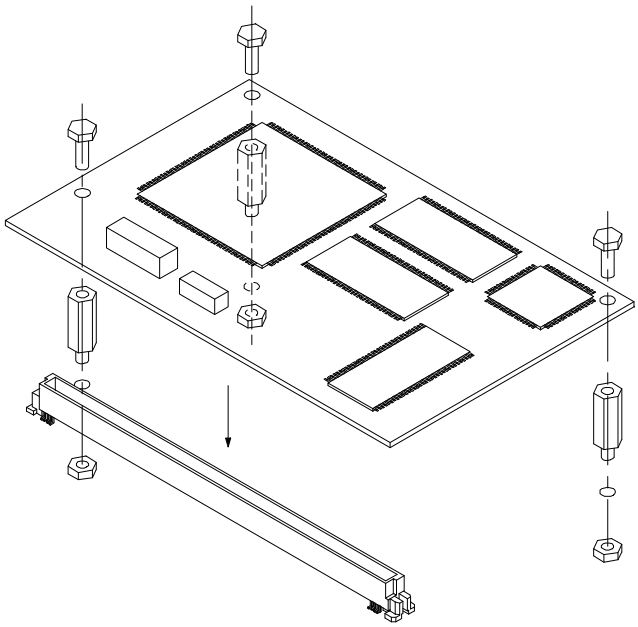
Tools required:

- Three M2 hex keys (7 mm long)
- Three M2 nuts
- Three M2 screws

(1) Insert three hex keys into three board holes, and tighten them using three nuts.

(2) Securely insert the CARD-E09A board into the CN1 socket as shown.

(3) Tighten three screws to fix the board (onto three keys).



12.LIST OF CONNECTORS

No.	Location	Connector model	Manufacturer	Connector applicable
CN1	SH-CARD	53481-2409	MOLEX	-
CN2	ISH-BUS	TX15-100P-LT-MH1	JAE	TX14-100R-LT-MH1
CN3	LCD	PS-50PE-D4T1-B1	JAE	PS-50SM-D4P1-1C
CN4	MISC	PS-10PE-D4T1-PN1	JAE	PS-10SM-D4P1-1C
CN5	CRT	17HE-B13150-74HC1	DDK	-
CN6,8,10	SERIAL	PS-10PE-D4T1-B1	JAE	PS-10SM-D4P1-1C
CN7	MOUSE/KB	TCS-7927-56-401	HOSHIDEN	-
CN9	PARALLEL	PS-26PE-D4T1-B1	JAE	PS-26SM-D4P1-1C
CN11	PCMCIA LOWER HEADER	92140-040	BERG	-
	PCMCIA UPPER HEADER	92140-045	BERG	-
	PCMCIA LOWER EJECTOR	95079-02CA	BERG	-
	PCMCIA UPPER EJECTOR	95079-00CA	BERG	-
CN12	SPEAKER	173981-2	AMP	179228-2 (Housing) 179518-1 (Contact)
CN13	10BASE-T	290A-88-30-335	MITSUMI	-
CN14	TOUCH PANEL	FFC-4CM1	HONDA	HKP-4FS01 (Housing) HKP-F113 (Contact)
CN16	POWER	178454-1	AMP	1-480424-0 (Housing) 170148-1 (Contact)

Manufacturer's name (abbreviation) details

MOLEX	Molex Inc.
JAE	Japan Aviation Electronics Industry, Ltd.
DDK	Daiichi Denshi Kogyo Corp.
HOSHIDEN	Hoshiden Corp.
BERG	Berg Electronics, Japan Corp.
AMP	AMP Inc.
MITSUMI	Mitsumi Electric and Machinery Corp.
HONDA	Honda Communication Industry Corp.

ISH Board
(SCE88J2B01)

Hardware Manual

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1.OVERVIEW

The ISH Board is an evaluation board to be connected to the ISH expansion bus connector (CN2) on the CARD-E09A Evaluation Board.
See "CARD-E09A Evaluation Board Hardware Manual" also.
The ISH Board has the following functions and can be used for evaluation of CARD-E09A.

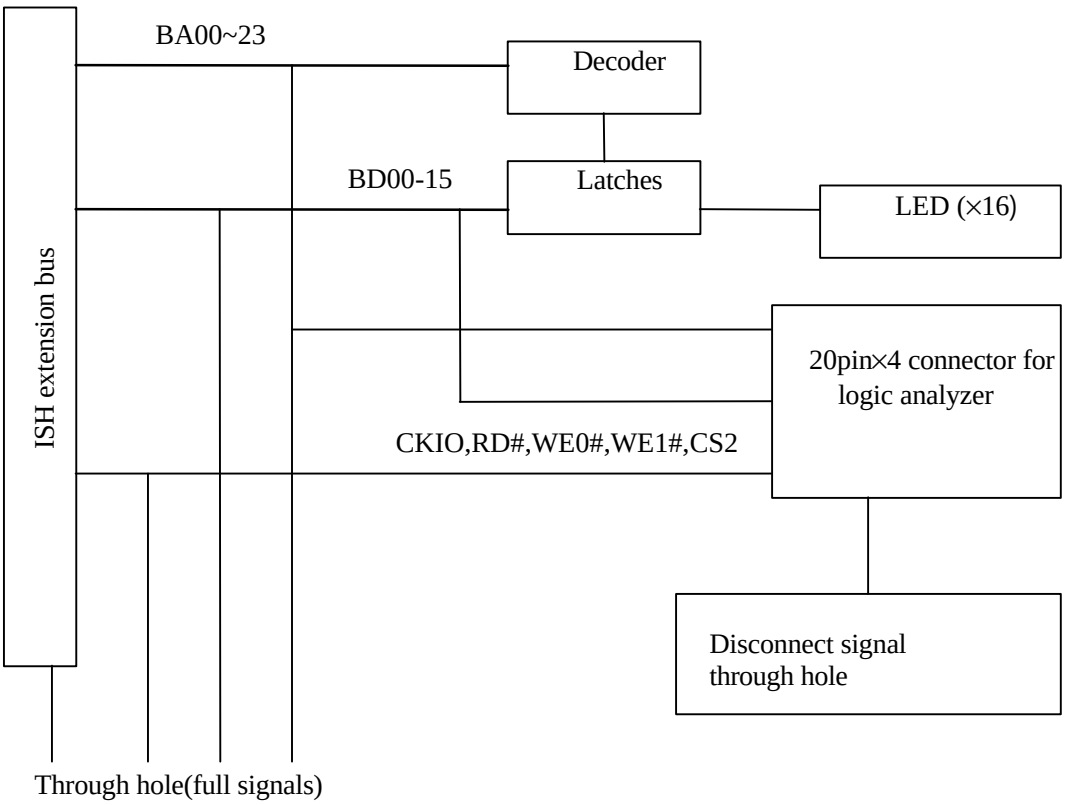
- Through-holes which output signals from the ISH expansion bus
  All signals from the ISH expansion bus are output to the board.
  Can be used for signal verification and signal output.

- LEDs for debugging
  16-bit LEDs are available for debugging.
  The LEDs come on and go off corresponding to status of 80h and 81h data bits of the I/O port.

- Logic analyzer connector
  Connector for connecting the logic analyzer is mounted.

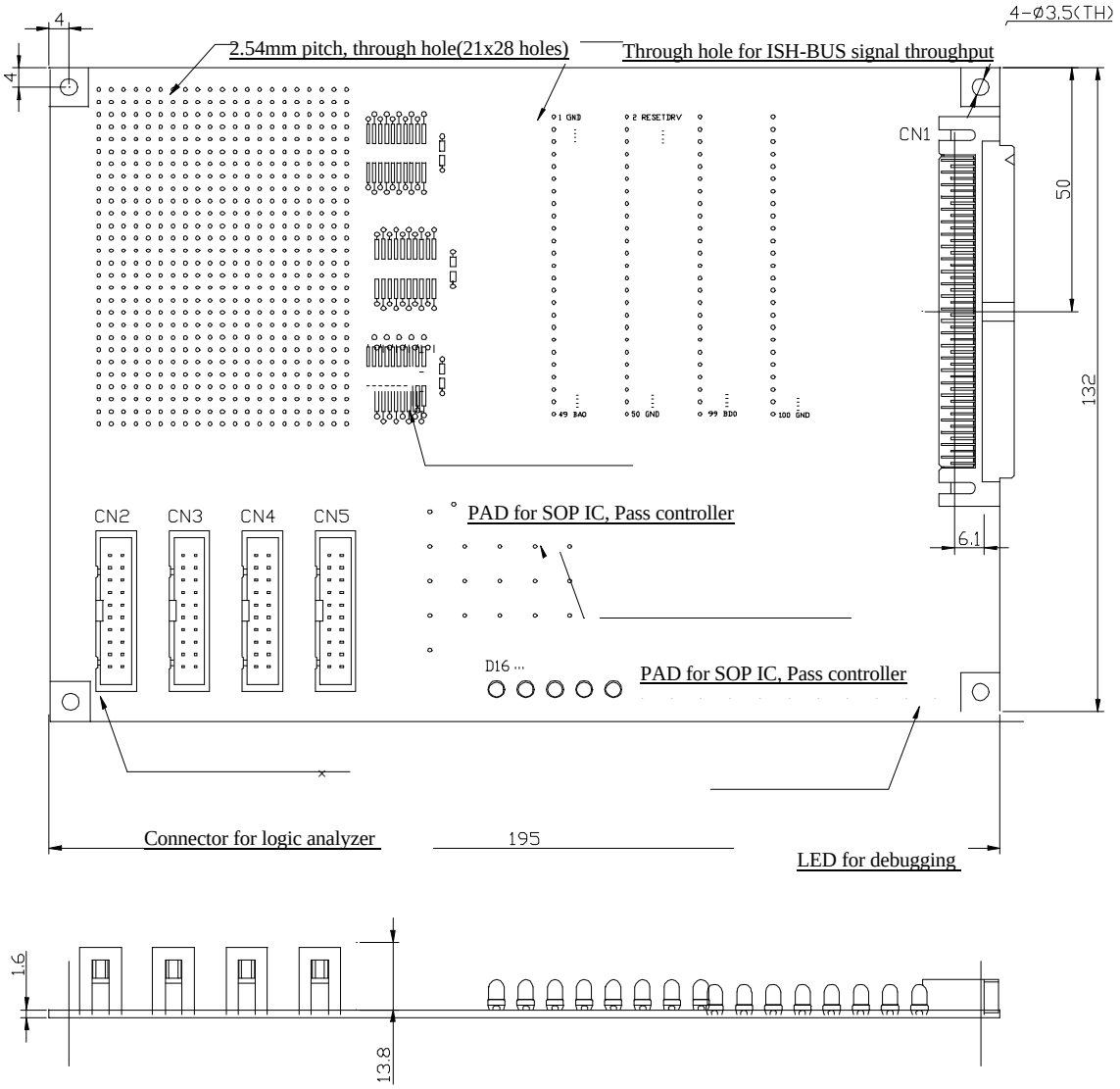
- Universal board
  Universal board is mounted.
  The board contains 2.54-mm pitch through-holes and SOP IC pads on which IC can be added for evaluation.

2.BLOCK DIAGRAM



3.BOARD EXTERNAL VIEW

- Board dimensions: 195×132 mm (same as the CARD-E09A Evaluation Board)



4.FUNCTION DESCRIPTION

Relationship between the power signal name indications and voltages are as follows.

ISH Board	CARD-E09A Evaluation Board	CARD-E09A	Voltage
P3V	P3V	V_{CC}	+3.3V
P5V	P5V	-	+5.0V

4.1.ISH Expansion Bus Connector

CN1 is a 100-pin connector. It is used for connecting with the ISH expansion bus on the CARD-E09A Evaluation Board.
All the signals from the ISH expansion bus are output to the ISH expansion bus output through-holes located in the center of the board.
For detailed information on signal types and functions, which are the same as CN2 on the CARD-E09A Evaluation Board, see "CARD-E09A Evaluation Board Hardware Manual".

Connector: TX14-100R-LT-MH1 (JAE)

CN1 : ISH-BUS Connector			
Pin	Signal Name	Pin	Signal Name
1	GND	51	GND
2	RESETDRV	52	RESERVE
3	IOCHRDY	53	RESERVE
4	IOW#	54	DA1
5	IOR#	55	RESERVE
6	MEMCS16#	56	STANDBY#
7	SBHE#	57	RESERVE
8	IOCS16#	58	PWOFF#
9	MEMR#	59	SRBTN#
10	MEMW#	60	PTC7/PINT7
11	ISADATAENA#	61	PTC6/PINT6
12	CKIO	62	PTC5/PINT5
13	TCLK	63	PTC4/PINT4
14	RESETP#	64	PTC3/PINT3
15	RESETM#	65	PTC2/PINT2
16	WAIT#	66	PTC1/PINT1
17	CS2#	67	FPVCCON
18	RD/WR#	68	DACK0#
19	WE1#	69	DREQ0#
20	WE0#	70	DACK1#
21	RD#	71	DREQ1#
22	BS#	72	NMI
23	GND	73	GND
24	BA25	74	P5V
25	BA24	75	P5V
26	BA23	76	P5V
27	BA22	77	P3V
28	BA21	78	P3V
29	BA20	79	P3V
30	BA19	80	IRQ1

30	BA19	80	IRQ1
31	BA18	81	IRQ2
32	BA17	82	IRQ3
33	BA16	83	IRQ4
34	BA15	84	BD15
35	BA14	85	BD14
36	BA13	86	BD13
37	BA12	87	BD12
38	BA11	88	BD11
39	BA10	89	BD10
40	BA9	90	BD9
41	BA8	91	BD8
42	BA7	92	BD7
43	BA6	93	BD6
44	BA5	94	BD5
45	BA4	95	BD4
46	BA3	96	BD3
47	BA2	97	BD2
48	BA1	98	BD1
49	BA0	99	BD0
50	GND	100	GND

4.2.Logic Analyzer Connector

CN2, 3, 4 and 5 are connectors for connecting the logic analyzer of the 20-pin box type pin header. Each signal is connected to the signal having the same name as in CN1.
Among these connectors, CN3 and CN5 have signals connected only to the through-hole located close to CN5, thereby allowing additional signal connection when necessary. The signals CS0#, 3#, 4#, 5# and BD16 to 31 correspond to such signals. The signal names do not have any special meanings; they are only for convenience. (For these signals, the columns are shaded, and the Remarks columns are marked with asterisk.)
Connector: J3592-6002FL (3M)

CN2 : Logic analyzer connector 1		
Pin	Signal Name	Remarks
1	NC	
2	NC	
3	CKIO	
4	BA15	
5	BA14	
6	BA13	
7	BA12	
8	BA11	
9	BA10	
10	BA9	
11	BA8	
12	BA7	
13	BA6	
14	BA5	
15	BA4	
16	BA3	
17	BA2	

18	BA1	
19	BA0	
20	GND	

CN3 : Logic analyzer connector 2		
Pin	Signal Name	Remarks
1	NC	
2	NC	
3	RD#	
4	BA25	
5	BA24	
6	BA23	
7	BA22	
8	BA21	
9	BA20	
10	BA19	
11	BA18	
12	BA17	
13	BA16	
14	CS0#	*
15	CS2#	
16	CS3#	*
17	CS4#	*
18	CS5#	*
19	CS6#	*
20	GND	

CN4 : Logic analyzer connector 3		
Pin	Signal Name	Remarks
1	NC	
2	NC	
3	WE0#	
4	BD15	
5	BD14	
6	BD13	
7	BD12	
8	BD11	
9	BD10	
10	BD9	
11	BD8	
12	BD7	
13	BD6	
14	BD5	
15	BD4	
16	BD3	
17	BD2	
18	BD1	
19	BD0	
20	GND	

CN5 : Logic analyzer connector 4		
Pin	Signal Name	Remarks
1	NC	
2	NC	
3	WE1#	
4	BD31	*
5	BD30	*
6	BD29	*
7	BD28	*
8	BD27	*
9	BD26	*
10	BD25	*
11	BD24	*
12	BD23	*
13	BD22	*
14	BD21	*
15	BD20	*
16	BD19	*
17	BD18	*
18	BD17	*
19	BD16	*
20	GND	

4.3.LED for Debugging

D1 to 16 are LEDs for debugging.
On CARD-E09A, when data are written to the ISA bus I/O addresses 80h and 81h, the data are latched and the LED corresponding to each data bit comes on/goes off.
The LED comes on when the data bit indicates "1" and goes off when the data bit indicates "0".
The addresses BA0 to BA23 are decorded.
The 80h corresponds to BD0 to 7, and the 81h corresponds to BD8 to 15.

When BD00="1" → D1 comes on.
When BD15="1"→ D16 comes on.

4.4.Universal Board

The universal board is equipped with 2.54-mm pitch through-holes and three sets of 20-pin SOP IC pad. The IC pads are equipped with pads for pass-controller and are connected to P3V (Note) and grounded.

(Note) Although the silk indication on the board is "VCC", the IC pads are connected to P3V.

5.ELECTRICAL SPECIFICATIONS

The circuit of LEDs for debugging operates with P3V power supply. The electrical specifications of this circuit are as follows:

GND=0V

Item		Min.	Max.	Unit
Circuit power supply voltage	V_{CC}	3.0	3.6	V
Input voltage of each signal (BA0 to 23, BD0 to 15, SBHE#, IOW#)	V_{IH}	2.0	-	V
	V_{IL}	-	0.8	V

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CARD-E09A
Evaluation Kit Hardware Manual
(English)