EPSON

CARD-E09A

Application Note

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

NOTICE

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

1. Introduction

This document is an Application Note to be used for reference when designing systems using the CARD-E09A. Use it in conjunction with the "CARD-E09A Hardware Manual," "SED1355F0A Technical Manual," the "Evaluation Board Hardware Manual" supplied with the CARD-E09A evaluation kit (SCE88J0X01), and the "Windows CE Development Kit Instruction Manual" supplied with the CARD-E09A Windows CE Development Kit (SCE88J3X01).

This document assumes incorporation into an operating system created using the Windows CE Development Kit provided by Epson for the CARD-E09A. Therefore, if a different operating system is used, additional software, such as device drivers, and additional hardware, such as extra circuits on the motherboard on which the CARD-E09A is mounted may be required.

2. Video Interface

The CARD-E09A includes LCD controller (SED1355, Seiko Epson) with internal RAM DAC. For the video memory 2MB (1M × 16 bits, 60 ns) of EDO-RAM is connected. In terms of display device, it can drive a CRT, a LCD, or both at the same time. Video signal output switching can be specified in STARTUP.DAT (described below). The STARTUP.DAT setting not only switches between CRT and LCD panel, but can also set the panel parameters so that various LCD panels can be connected. The main difference between the CRT interface and the LCD interface is that the former is an analog output whereas the latter is a digital (TTL) output. For details, see "SED1355F0A Technical Manual."

2.1. CRT Interface

In Section 13.2.1.2, "Reference Circuit Diagrams," Sheet 5 "Video, Keyboard/Mouse, Parallel Interface" shows a reference circuit diagram. Only eight signal lines are required to connect the CARD-E09A to the CRT interface connector.

2.2. LCD Interface

The LCD interface of CARD-E09A can be connected to the following liquid display panels:

Interface types

- 4-bit single monochrome passive LCD panel (bus configuration: 4 × 1)
- 8-bit single monochrome passive LCD panel (bus configuration: 8 × 1)
- 4-bit single color passive LCD panel (bus configuration: 4 × 1)
- 8-bit single color passive LCD panel (bus configuration: 8 × 1)
- 16-bit single color passive LCD panel (bus configuration: 16 × 1)
- 8-bit dual monochrome passive LCD panel (bus configuration: 4 × 2)
- 8-bit dual color passive LCD panel (bus configuration: 4 × 2)
- 16-bit dual color passive LCD panel (bus configuration: 8 × 2)
- 9-bit TFT color LCD panel (color configuration: R, G, B × 3)
- 12-bit TFT color LCD panel (color configuration: R, G, B × 4)
- 16-bit TFT color LCD panel (color configuration: R × 5, G × 6, B × 5)

Display sizes and colors

The panel parameter settings (see 2.3.2.) principally allow the following display sizes and colors. Although the size can be adjusted to a size other than the following, the maximum size is SVGA.

- QVGA (320 × 240), maximum 16 bpp (65,536 colors)
- VGA (640 × 480), maximum 16 bpp (65,536 colors)
- SVGA (800 × 600), maximum 8 bpp (256 colors)

2.3. LCD Connection

This describes the LCD panel connection and notes thereon. When connecting an LCD panel, follow the procedure given in this section for checking. The following is an outline.
Step 1: Check the signal and power line connections: see Section 2.3.1.
Step 2: Check the panel parameter settings: see Section 2.3.2.
Step 3: Amend the STARTUP.DAT settings as required: see Section 2.3.3.

2.3.1. Signal and Power Line Connections

2.3.1.1. Signal Lines

2.3.1.1.1. LCD interface

Tables 2-1 to 2-3 show the connections between the CARD-E09A and the LCD panel. Refer to this together with Table 5-9, "Interface Connector Assignment" in the "SED1355F0A Technical Manual." In the following table, FPFRAME is the frame pulse, FPLINE is the line pulse, and FPSHIFT is the shift clock pulse; MOD is the bias signal for a passive panel, and the display enable signal for a TFT panel. Note that the actual names may vary from panel to panel.

Table 2-1 Signal connector assignment (monochrome passive panel)

CARD-E09A		Monochrome passive panel		
		Single		Dual
Connector name	Pin number	4-bit	8-bit	8-bit
FRAME	239	FPFRAME		
LINE	238	FPLINE		
DOTCLK	235	FPSHIFT		
MOD	236	MOD		
FPDAT0	234	–	D0	LD0
FPDAT1	233	–	D1	LD1
FPDAT2	232	–	D2	LD2
FPDAT3	231	–	D3	LD3
FPDAT4	230	D0	D4	UD0
FPDAT5	229	D1	D5	UD1
FPDAT6	228	D2	D6	UD2
FPDAT7	227	D3	D7	UD3
FPDAT8	225	–	–	–
FPDAT9	224	–	–	–
FPDAT10	223	–	–	–
FPDAT11	222	–	–	–
FPDAT12	220	–	–	–
FPDAT13	219	–	–	–
FPDAT14	218	–	–	–
FPDAT15	217	–	–	–

Table 2-2 Signal connector assignment (color passive panel)

CARD-E09A		Color passive panel					
		Single	Single format 1	Single format 2	Single	Dual	
Connector name	Pin number	4-bit	8-bit	8-bit	16-bit	8-bit	16-bit
FRAME	239	FPFRAME					
LINE	238	FPLINE					
DOTCLK	235	FPSHIFT					
MOD	236	MOD	FPSHIFT2	MOD			
FPDAT0	234	–	D0	D0	D0	LD0	LD0
FPDAT1	233	–	D1	D1	D1	LD1	LD1
FPDAT2	232	–	D2	D2	D2	LD2	LD2
FPDAT3	231	–	D3	D3	D3	LD3	LD3
FPDAT4	230	D0	D4	D4	D4	UD0	UD0
FPDAT5	229	D1	D5	D5	D5	UD1	UD1
FPDAT6	228	D2	D6	D6	D6	UD2	UD2
FPDAT7	227	D3	D7	D7	D7	UD3	UD3
FPDAT8	225	–	–	–	D8	–	LD4
FPDAT9	224	–	–	–	D9	–	LD5
FPDAT10	223	–	–	–	D10	–	LD6
FPDAT11	222	–	–	–	D11	–	LD7
FPDAT12	220	–	–	–	D12	–	UD4
FPDAT13	219	–	–	–	D13	–	UD5
FPDAT14	218	–	–	–	D14	–	UD6
FPDAT15	217	–	–	–	D15	–	UD7

Table 2-3 Signal connector assignment (color TFT panel)

CARD-E09A		Color TFT panel		
Connector name	Pin number	9-bit	12-bit	18-bit
FRAME	239	FPFRAME		
LINE	238	FPLINE		
DOTCLK	235	FPSHIFT		
MOD	236	DRDY		
FPDAT0	234	R2	R3	R5
FPDAT1	233	R1	R2	R4
FPDAT2	232	R0	R1	R3
FPDAT3	231	G2	G3	G5
FPDAT4	230	G1	G2	G4
FPDAT5	229	G0	G1	G3
FPDAT6	228	B2	B3	B5
FPDAT7	227	B1	B2	B4
FPDAT8	225	B0	B1	B3
FPDAT9	224	–	R0	R2
FPDAT10	223	–	–	R1
FPDAT11	222	–	G0	G2
FPDAT12	220	–	–	G1
FPDAT13	219	–	–	G0
FPDAT14	218	–	B0	B2
FPDAT15	217	–	–	B1

Notes
1) Unused data lines on the CARD-E09A are driven at low level.
2) For single color passive panels, format 1 and 2 have different data formats. See "SED1355F0A Technical Manual."

2.3.1.1.2. External Clock Input Mode

The default setting of the SED1355 LCD controller built into the CARD-E09A (referred to as "internal clock mode") is to operate synchronized to the system clock CKIO (33.2 MHz). The dot clock signal (DOTCLK) for the LCD panel is also generated by frequency division of CKIO, so depending on the LCD panel it may not be possible to meet the dot clock signal specification. The dot clock signal in internal clock mode is shown in Table 2-4 and the dot clock signal for typical LCD panels is shown in Table 2-5. The clock divisor is determined by the setting of SED1355 REG[19h].

Notes

DOTCLK is different from the CARD-E09A internal display reference clock signal (PCLK) for each pixel. The setting of SED1355 REG[19h] only affects PCLK, and therefore when determining DOTCLK, it is essential to check Table 2-10 "Relation between DOTCLK and PCLK," and Table 2-11 "Restrictions on PCLK settings" in Section 2.3.2, "Panel parameter settings." Table 2-4 shows the relationship for a TFT panel or the like, when DOTCLK = PCLK.

Table 2-4 Dot clock signal in internal clock mode (when DOTCLK = PCLK)

Frequency divisor	DOTCLK [MHz]
CKIO/1	33.2
CKIO/2	16.6
CKIO/3	11.1
CKIO/4	8.3

Table 2-5 Dot clock signal for standard LCD panel (typical frequency)

	Color VGA TFT	Color VGA STN (Dual Scan)	Mono VGA STN (Dual Scan)	Mono VGA STN (Single Scan)
DOTCLK [MHz]	25.175	12.587	6.294	3.147

Table 2-5 shows only typical frequency for the dot clock, but in general an LCD panel has minimum, reference, and maximum values stipulated for the dot clock signal. For any of the frequency divisors shown in Table 2-4, if the specification range cannot be satisfied, or if it is necessary to make fine adjustments to the dot clock signal to optimize the display performance, this cannot be supported in internal clock mode.

The above problems can be solved by operating in external clock input mode. In external clock input mode, for the SED1355 reference clock signal, CKIO is replaced by an external input to the CARD-E09A. The following procedure is required for setting external clock input mode.

Step 1) Connect the external clock circuit to the CARD-E09A.
To pin 174, "EXTCLKI" of the CARD-E09A interface connector, connect the most appropriate external clock source for LCD panel. Note the following points when selecting the external clock frequency and designing the circuit.

1) The input voltage rating and AC characteristics rating must be strictly observed.
   $V_{IL} = V_{CC} \times 0.3$ Max., $V_{IH} = V_{CC} \times 0.7$ Min., $V_{CC} = 3.3V$
   For the AC characteristics, refer to Chapter 8, "AC Characteristics" in the "CARD-E09A Hardware Manual."

2) Maximum frequency which can be set = 33.2 MHz
   This is based on the specification of the 2 MB EDO-RAM used in the CARD-E09A. If a clock source exceeding this frequency is connected, the display quality cannot be guaranteed.

3) Select as high a frequency as possible.
   The clock source connected to "EXTCLKI" is used as the reference clock signal for SED1355 operation. To get the optimal performance, select as high a frequency as possible. Table 2-6 shows examples.

Table 2-6 Examples of external clock source

	Color VGA TFT	Color VGA STN (Dual Scan) #1	Mono VGA STN (Dual Scan) #2	Mono VGA STN (Single Scan) #3
External clock source [MHz]	25.175	25.175	25.175	25.175
Divisor	1	2	1	1
PCLK [MHz]	25.175	12.587	25.175	25.175
DOTCLK [MHz]	25.175	12.587	6.294	3.147

#1) If the minimum rating of the dot clock signal specification for the LCD panel is 11.1 MHz or below, in internal clock mode a divisor of 3 can be set. In the external clock input mode, the SED1355 reference clock signal is 25.175 MHz, while in the internal clock mode it is 33.2 MHz, and therefore the internal clock mode gives better performance.

#2) This is the example in which DOTCLK = PCLK/4. If the maximum rating of the dot clock signal specification of the LCD panel is 8.3 MHz or above, in internal clock mode a divisor of 1 can be set. As in Note #1, the internal clock mode gives better performance.

#3) This is the example in which DOTCLK = PCLK/8. If the maximum rating of the dot clock signal specification of the LCD panel is 4.2 MHz or above, in internal clock mode a divisor of 1 can be set. As in Note #1, the internal clock mode gives better performance.

Step 2) Set STARTUP.DAT to external clock input mode.

The change to the external clock input mode occurs based on the STARTUP.DAT settings in the power-on sequence.

In the CARD-E09A, the SH7709A Port E register bit 2 is connected to the switchover selector for the SED1355 reference clock signal. When the external clock input mode is set, it is necessary first to edit STARTUP.DAT. For details, see Section 2.3.3, "STARTUP.DAT Settings."

2.3.1.2. Power Sequence

FPVCCON and FPVEEON signals are prepared for the LCD panel power control. By merely adding a power on/off circuit, the LCD panel can be powered on and off easily. An overview of the power sequence is shown in Fig. 2-1. In this figure, the power on/off timing and the suspend/resume timing are shown together. This should be seen together with Section 7.4, "Power Sequence" of the "SED1355F0A Technical Manual." Note that in the "SED1355F0A Technical Manual," FPVEEON is shown as LCDPWR. Again, FPVCCON is not an SED1355 function, but is added with the CARD-E09A specification.

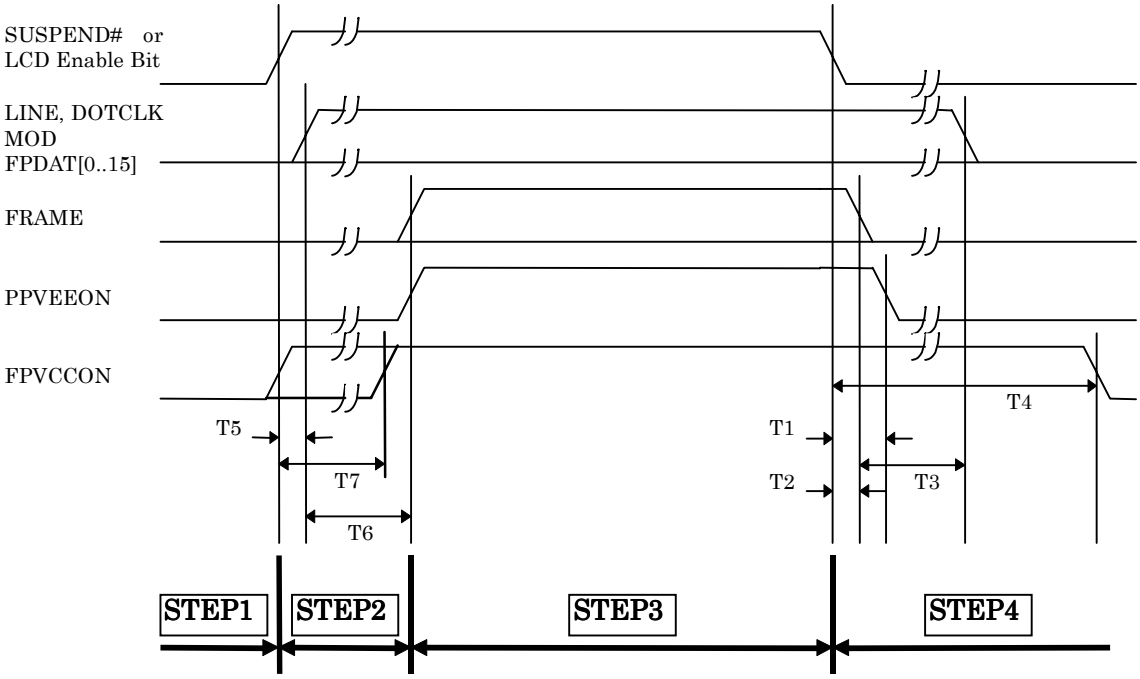


Fig. 2-1 Overview of Power Sequence

[Fig. 2-1]

Symbol	Item	Min.	Max.	Units
T1	"SUSPEND# Bit" enable, or "LCD Enable Bit" disable to FPVEEON off	-	2 Frame + Dotclk	ns
T2	"SUSPEND# Bit" enable or "LCD Enable Bit" disable to FRAME inactive	-	1	Frame
T3	FRAME inactive to LINE, DOTCLK, MOD, and FPDAT[0..15] inactive	128	-	Frame
T4	"SUSPEND# Bit" enable or "LCD Enable Bit" disable to FPVCCON off	10 (Setting can be changed in STARTUP.DAT)	-	ms
T5	"SUSPEND# Bit" disable or "LCD Enable Bit" enable to LINE, DOTCLK, MOD, FPDAT[0..15] active	-	1 Frame + 8 Dotclk	ns
T6	LINE, DOTCLK, MOD, FPDAT[0..15] active to FRAME active, and FPVEEON on	128	-	Frame
T7	"SUSPEND# Bit" disable or "LCD Enable Bit" enable to FPVCCON on (Timing can be set in STARTUP.DAT, and in a resume is fixed at 0 frame)	0 (This value is fixed in a resume)	127	Frame

1) In the figure above, "LCD Enable Bit" indicates REG[0Dh] Bit 0 (LCD Enable).
2) "SUSPEND# Bit" indicates the SH7709A Port E register Bit 7 (in the CARD-E09A, assigned to control of SUSPEND#). The output of this port is connected internally to the CARD-E09A to the SUSPEND# pin of the SED1355. SED1355 REG[1Ah] Bit 0 (Software SUSPEND Mode) is not used.
3) For the FPVCCON on timing setting, see Section 2.3.3, "STARTUP.DAT settings."

A summary of the power sequence is now described. In the system power on/off sequence, NKLOADS.BIN (part of the loader), in the suspend/resume sequence, Windows CE HAL, respectively sets the SED1355 and SH7709A registers based on the STARTUP.DAT settings. The user simply has to make settings in STARTUP.DAT, and the following power sequence requirements can be met. Read this in conjunction with Section 2.3.3, "STARTUP.DAT settings."

<<STEP1>>

Power on sequence preparations are made.

For the sequence after system power on
After a system power on, NKLOADS.BIN (part of the loader) makes the initial settings based on the settings in STARTUP.DAT.

1) The SH7709A Port E register Bit 2 (assigned to SED1355 reference clock signal switching control in CARD-E09A) is set, and a check made of whether the internal clock mode or external clock input mode is selected.
2) SED1355 registers are set.
3) First SED1355 REG[23h] Bit 7 (Display FIFO Disable) is set to 1, (display inhibit mode), and next SED1355 REG[0Dh] Bit 0 (LCD Enable) is set to 1 for the LCD power on sequence.

For a resume
Previously, before the suspend, the settings in 1) and 2) above have been carried out, and the display inhibit mode setting completed. At that time, to speed up the suspend/resume display power on sequence, the display area is set to a minimum. The setting size is as follows. In this state, NKLOADS.BIN carries out the next step, A).

- HDP (horizontal display period) = 8 pixels
- HNDP (horizontal non-display period) = 32 pixels
- VDP (vertical display period) = 1 line
- VNDP (vertical non-display period) = 1 line

A) Windows CE HAL sets the SUSPEND# Bit to 1 (Disable).

<<STEP2>>

This is the power on sequence.

Sequence after a system power on
4) The SH7709A Port D register Bit 1 (assigned to FPVCCON control in CARD-E09A) is set, and FPVCCON is turned on. The on timing "T7" can be adjusted by a STARTUP.DAT setting.
5) After time T5, LINE, DOTCLK, MOD, and FPDAT[0..15] are active, and further after time T6, FRAME and FPVEEON are active. (Since FRAME operation timing is delayed by time T6 with respect to other signals, in order to prevent a broken-up display when the vertical sync cannot be obtained, the display inhibit mode is set.)
6) After 128 Frames (T6) from 3), the display inhibit mode is ended.

The following is an example of the calculation of T5, T6, and T7.
For settings of DOTCLK = 25.175 MHz, HDP = 640 pixels, HNDP = 160 pixels, VDP = 480 lines, VNDP = 45 lines, then T5, T6, and T7 are obtained as follows.

T5 = 1 (Frame) + 8 (Dotclk) = 1 × ((HDP + HNDP) × (VDP + VNDP) + 8) × (1 / 25.175 MHz)
= ((640 + 160) × (480 + 45) + 8) × (1/25.175 MHz)
= 16.683 ms Max.
T6 = 128 (Frame) = 128 × (HDP + HNDP) × (VDP + VNDP) × (1/25.175 MHz)
= 128 × (640 + 160) × (480 + 45) × (1/25.175 MHz)
= 2.135 s Min.
T7 = 127 (Frame) Max. = 127 × (HDP + HNDP) × (VDP + VNDP) × (1/25.175 MHz)
= 127 × (640 + 160) × (480 + 45) × (1/25.175 MHz)
= 2.118 s Max. (for minimum setting, 0 Frame = 0 ns Min.)

Note:
When the connected LCD panel has a specified time from logic power on until the signal lines are driven not exceeding "T5 + T6", a buffer IC must be inserted in all signal lines, and the power on sequence controlled. See Section 2.3.4, "Design Notes."

For a resume
B) FPVCCON is turned on. T7 = 0 Frame fixed.
C) After time T5, LINE, DOTCLK, MOD, FPDAT[0..15] are active, and further after time T6, FRAME and FPVEEON are active.
D) After 128 Frames (T6) from A), based on STARTUP.DAT, the proper display size is set, after which the display inhibit mode is ended.

The following is an example of the calculation of T5, T6, and T7 when DOTCLK = 25.175 MHz
The display size is the minimum setting (HDP = 8 pixels, HNDP = 32 pixels, VDP = 1 line, VNDP = 1 line).

T5 = 1 (Frame) + 8 (Dotclk) = 1 × ((HDP + HNDP) × (VDP + VNDP) + 8) × (1 / 25.175 MHz)
= ((8 + 32) × (1 + 1) + 8) × (1/25.175 MHz)
= 3.495 μs Max.
T6 = 128 (Frame) = 128 × (HDP + HNDP) × (VDP + VNDP) × (1/25.175 MHz)
= 128 × (8 + 32) × (1 + 1) × (1/25.175 MHz)
= 406.752 μs Min.
T7 = 0 s Min. (fixed)

<STEP3>

This is the display mode. When ending the display mode, the preparations must be made in advance.

Sequence before a system power off

7) After setting the display inhibit mode, to speed up the power off sequence, the display size is set to the minimum. The display size is as follows.
   - HDP (horizontal display period) = 8 pixels
   - HNDP (horizontal non-display period) = 32 pixels
   - VDP (vertical display period) = 1 line
   - VNDP (vertical non-display period) = 1 line

8) SED1355 REG[0Dh] Bit 0 (LCD Enable) is set to 0, and the LCD is set to the power off sequence.

Sequence before a suspend

Read this in combination with Section 9.3, "LCD Power Off Sequence" in the "CARD-E09A Windows CE Development Kit Instruction Manual" supplied with the CARD-E09A Windows CE Development Kit.

E) Same as 7).
F) Windows CE HAL sets SUSPEND# Bit to 0 (Enable).

<STEP 4>

This is the power off sequence.

For a system power off sequence

9) After time T1, FPVEEON goes off, after time T2, FRAME, and then after time T3, LINE, DOTCLK, MOD, and FPDAT[0..15] are inactive.
10) After time T4, FPVCCON goes off.

For a suspend

G) Same as 9).
H) Same as 10).

The following is an example of the calculation of T1, T2, T3, and T4 when DOTCLK = 25.175 MHz. The display size is the minimum setting
(HDP = 8 pixels, HNDP = 32 pixels, VDP = 1 line, VNDP = 1 line).

T1 = 2 (Frame) + 8 (Dotclk) = 2 × ((HDP + HNDP) × (VDP + VNDP) + 8) × (1 / 25.175 MHz)
= (2 × (8 + 32) × (1 + 1) + 8) × (1/25.175 MHz)
= 6.673 µs Max.
T2 = 1 (Frame) = 1 × (HDP + HNDP) × (VDP + VNDP) × (1/25.175 MHz)
= (8 + 32) × (1 + 1) × (1/25.175 MHz)
= 3.177 µs Max.
T3 = 128 (Frame) = 128 × (HDP + HNDP) × (VDP + VNDP) × (1/25.175 MHz)
= 128 × (8 + 32) × (1 + 1) × (1/25.175 MHz)
= 406.752 µs Min.
T4 = 10 ms Min. (No dependency on DOTCLK)

The specification of time T4 is given in Section 7.4, "Power Sequence" of the "SED1355F0A Technical Manual" as 130 Frames minimum, but in CARD-E09A, to improve the suspend/resume and power off sequence response, HDP/HNDP, and VDP/VNDP are minimized, and it is fixed at 10 ms minimum. This value is generated using the SH7709A internal timer function, and therefore in the external clock input mode does not depend on the external clock source or DOTCLK frequency. However, with a very low frequency external clock source, if 130 Frames exceeds 10 ms, it is necessary to change the STARTUP.DAT settings, and specify a larger time. For the method of changing the specified time, see Section 2.3.3, "STARTUP.DAT Settings." The reference criterion is as follows.

- T4 = 130 (Frames) = 130 × (HDP + HNDP) × (VDP + VNDP) × (1/DOTCLK) < 10 ms
  HDP = 8, HNDP = 32, VDP = 1, VNDP = 1
  If the above relation cannot be satisfied, then the setting for time T4 must be changed in STARTUP.DAT.

As described above, the LCD panel power sequence can be controlled by FPVCCON and FPVEEON. Also, the signal line power on timing is determined by the HDP, HNDP, VDP, VNDP, and DOTCLK as set in the SED1355 registers.

Fig. 2-2 shows an example of connections. In this example of connections, signals for the liquid crystal display are directly connected between the CARD-E09A and the liquid crystal display device, but depending on the LCD panel, the DC characteristics of the signal lines may not match those of the CARD-E09A, or there may be strict requirements for the power on/off sequence. In such cases, a buffer IC must be inserted, or other measures taken so that the LCD panel specification is met.

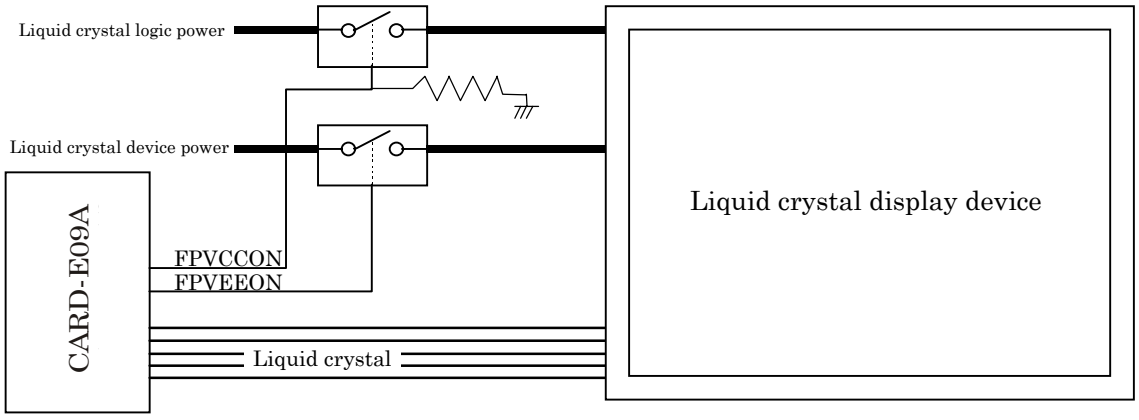


Fig. 2-2 Example connections

2.3.2. Panel Parameter Setup Method

Note the following points when setting SED1355 registers. Checking the display of the parameters which have been set can be done with the quick debugger supplied with the "CARD-E09A evaluation kit (SCE88J0X01)." For directions for using the quick debugger, see Chapter 12, "Quick Debugger" in the "CARD-E09A Windows CE Development Kit Instruction Manual" supplied with the CARD-E09A Windows CE Development Kit.
The parameters checked here are reflected in STARTUP.DAT. Read this in combination with the "SED1355F0A Technical Manual."

2.3.2.1. SED1355 Register Settings

The registers which require setting are REG[01h] to REG[23h]. Except in special cases, such as direct setting from a look-up table (LUT), other registers do not require setting in STARTUP.DAT.

Fixed setting parameters

Registers with values have to set according to the CARD-E09A hardware specification are described below. When making settings in STARTUP.DAT, always use this setting.

Table 2-7 Preset register values

Index	Bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
01h	N/A	0	1	1	N/A	0	N/A	0
1Ah	R/O	N/A	N/A	N/A	0	0	1	0
22h	Rsv	0	1	0	0	1	Rsv	rsv
23h	Any	0	0	Any	Any	Any	Any	Any

N/A: Not applicable (Set to 0 in STARTUP.DAT.)
Rsv: Reserved (Set to 0 in STARTUP.DAT.)
Any: Set to any value. (See Table 2-8.)

Basic settings

Set registers shown in Table 2-8 so that they meet with the LCD panel specification. When checking the settings, read this in combination with Chapter 8, "Registers" and the timing charts for each LCD panel shown in Section 7.5, "Display Interface" in the "SED1355F0A Technical Manual."

Table 2-8 Registers which have to be set

Index	Name	Note
02h	Panel type setting	-
03h	MOD rate setting	This is significant for a passive panel. Default "00h": Toggle for each frame Values other than "00h": Specify line number to toggle
04h	Horizontal display width (HDP) setting	-
05h	Horizontal non-display period (HNDP) setting	Set larger than "REG[06h] + REG[07h]".
06h	Line start position setting	Specify the delay from the start of HNDP until a rising edge or a falling edge where LINE goes active (included in HNDP).
07h	LINE polarity/pulse width setting	The pulse width (included in HNDP) is automatically generated in the case of a passive panel, and thus has no effect.
08h, 09h	Vertical display period (VDP) setting	-
0Ah	Vertical non-display period (VNDP) setting	Set larger than "REG[0Bh] + REG[0Ch]".
0Bh	FRAME start position setting	Specify the delay from the start of VNDP until a rising edge or a falling edge where FRAME goes active (included in VNDP). This is automatically generated in the case of a passive panel, and thus has no effect.
0Ch	FRAME polarity /pulse width setting	The pulse width (included in VNDP) is automatically generated in the case of a passive panel, and thus has no effect.
0Dh	Display mode setting	#1)
0Eh to 12h	Screen 1 setting	#2) When the screen is not divided, the settings are: [0Eh]=FFh, [0Fh]=03h, [10h] to [12h]=00h.
13h to 15h	Screen 2 setting	#2) When screen 2 is not used, set to all 00h (in the quick debugger set to 08h to drive screen 2).
16h, 17h	Memory address offset setting	#2) #3)
18h	Panning setting	When the panning function is not used, set to 00h.
19h	Dot clock signal setting	#4)
1Bh	Half-frame buffer setting	When using dual panel, set to Enable.
23h	Display FIFO setting	#5) Normally set to 00h. With MCLK=PCLK (see #4) in following cases, set to 1Bh - for 16/15 bpp setting - for 16/8 bpp setting in portrait mode

#1) For the hardware portrait mode (Bit 7) see Section 2.3.2.2. When operating with an OS created using Epson's "CARD-E09A Windows CE Development Kit," there are restrictions on the bpp selection (bits 4, 3, 2). The device driver only supports 8 bpp and 16 bpp modes. If another mode is set, the display quality under Windows CE cannot be guaranteed. For the CRT/LCD simultaneous display setting (bits 6, 5), see Section 2.3.2.3. For details of setting the CRT Enable (Bit 1) and LCD Enable (Bit 0) in STARTUP.DAT, see Section 2.3.3.

#2) For details, see Chapter 10, "Display Configuration" of the "SED1355F0A Technical Manual." Note that the Windows CE device driver does not support a two-screen drive. Again, in the hardware portrait mode, the settings of REG[10h] to REG[15h] are different. See Section 2.3.2.2.

#3) Table 2-9 illustrates example settings of the memory address offset. For hardware portrait mode see Section 2.3.2.2. The settings are different. Note that in the quick debugger LCD command, setting and entering HDP (REG[04h]), automatically displays the settings of REG[16h] and [17h].

Table 2-9 Example settings of memory address offset

HDP	Offset Address	16/15BPP	8BPP	4BPP	2BPP	1BPP
640 pixels	Number of words of data required for one line display	640	320	160	80	40
	REG[16h] setting value	80h	40h	A0h	50h	28h
	REG[17h] setting value	02h	01h	00h	00h	00h
320 pixels	Number of words of data required for one line display	320	160	80	40	20
	REG[16h] setting value	40h	A0h	50h	28h	14h
	REG[17h] setting value	01h	00h	00h	00h	00h

Note:
The number of pixels that can be represented by 1 byte is 1/2 pixel (2 bytes per 1 pixel) for 16/15 bpp, 1 pixel for 8 bpp, 2 pixels for 4 bpp, 4 pixels for 2 bpp, and 8 pixels for 1 bpp.

#4) In this register, the frequency of MCLK (memory clock) and PCLK (pixel clock) is set based on the source frequency (CKIO or external clock input source). MCLK is the video memory (EDO-RAM) reference clock signal. To minimize the current consumption during EDO-RAM access, make the setting (bit 2 = 0) so that MCLK is equal to the source frequency.
PCLK is a once-per-pixel display reference clock signal. It is not connected to the CARD-E09A interface internally. The relation between DOTCLK and PCLK is shown in Table 2-10.
Table 2-11 shows restrictions when setting PCLK. Read this in combination with Section 2.3.1.1.2, "External Clock Input Mode."

Table 2-10 Relation between DOTCLK and PCLK

LCD panel types	DOTCLK
4-bit single monochrome passive (bus configuration: 4 × 1)	PCLK/4
8-bit single monochrome passive (bus configuration: 8 × 1)	PCLK/8
4-bit single color passive (bus configuration: 4 × 1)	PCLK
8-bit single color passive type 1 (bus configuration: 8 × 1)	PCLK/4
8-bit single color passive type 2 (bus configuration: 8 × 1)	PCLK/2
16-bit single color passive (bus configuration: 16 × 1)	PCLK/5
8-bit dual monochrome passive (bus configuration: 4 × 2)	PCLK/4
8-bit dual color passive (bus configuration: 4 × 2)	PCLK
16-bit dual color passive (bus configuration: 8 × 2)	PCLK/2
TFT color	PCLK

By setting SED1355 REG[02h] (panel type setting), the relation between DOTCLK and PCLK can be arbitrarily defined.

Table 2-11 Restrictions when setting PCLK

<table>
<tr><th rowspan="2">Ink</th><th rowspan="2">Display type</th><th colspan="5">Maximum PCLK that can be set</th></tr>
<tr><th>16/15BPP</th><th>8BPP</th><th>4BPP</th><th>2BPP</th><th>1BPP</th></tr>
<tr><td rowspan="3">OFF</td><td>・Single Panel
・CRT
・Mono/Color Dual Passive Panel
(Half Frame Buffer = Disable)
・CRT & Single Panel simultaneous display
・CRT & Mono/Color Dual Passive Panel simultaneous display
(Half Frame Buffer = Disable)</td><td colspan="5">MCLK</td></tr>
<tr><td>・Mono Dual Passive Panel
(Half Frame Buffer = Enable)
・CRT & Mono Dual Passive Panel simultaneous display
(Half Frame Buffer = Enable)</td><td colspan="4">MCLK/2</td><td>MCLK/3</td></tr>
<tr><td>・Color Dual Passive Panel
(Half Frame Buffer = Enable)
・CRT & Color Dual Passive Panel simultaneous display
(Half Frame Buffer = Enable)</td><td colspan="4">MCLK/2</td><td>MCLK/3</td></tr>
<tr><td rowspan="3">ON</td><td>・Single Panel
・CRT
・Mono/Color Dual Passive Panel
(Half Frame Buffer = Disable)
・CRT & Single Panel simultaneous display
・CRT & Mono/Color Dual Passive Panel simultaneous display
(Half Frame Buffer = Disable)</td><td colspan="2">MCLK</td><td colspan="3">MCLK/2</td></tr>
<tr><td>・Mono Dual Passive Panel
(Half Frame Buffer = Enable)
・CRT & Mono Dual Passive Panel simultaneous display
(Half Frame Buffer = Enable)</td><td colspan="3">MCLK/2</td><td colspan="2">MCLK/3</td></tr>
<tr><td>・Color Dual Passive Panel
(Half Frame Buffer = Enable)
・CRT & Color Dual Passive Panel simultaneous display
(Half Frame Buffer = Enable)</td><td colspan="2">MCLK/2</td><td colspan="3">MCLK/3</td></tr>
</table>

Note:
This table was created by extracting the items for which Nrc=4 from Table 14-1 "Maximum PCLK frequency with EDO-DRAM" in Chapter 14, "Clocking" of the "SED1355F0A Technical Manual."
The Epson Windows CE device driver always has "Ink = OFF" set.
When using the ink function, it is necessary to set REG[27h] to [30h].

#5) For details of setting display FIFO disable (Bit 7) in STARTUP.DAT, see Section 2.3.3, "STARTUP.DAT Settings."

2.3.2.2. Hardware Portrait Mode

By setting REG[0Dh] Bit 7 to 1 the hardware portrait mode can be enabled. The hardware portrait mode is a display mode in which the display image is rotated clockwise through 90 degrees in hardware. For details, see Chapter 13, "Hardware Portrait Mode" in the "SED1355F0A Technical Manual."

In hardware portrait mode, not only the setting of REG[0Dh] Bit 7, but also the memory address offset (REG[16h], [17h]), the screen 1 setting (REG[10h], [11h], [12h]), and the screen 2 setting (REG[13h], [14h], [15h]) must be changed. For the method of making the setting in STARTUP.DAT, see Section 2.3.3. "STARTUP.DAT Settings." Note that the Epson Windows CE video driver does not support the hardware portrait mode on screen 2. This mode is available in 16 bpp and 8 bpp modes. It is not supported in hardware for 4 bpp /2 bpp /1 bpp. Note also that the cursor and ink images are not rotated.

Setting for memory address offset (REG[16h], [17h])

- For 16 bpp: 1024 words (fixed)
- For 8 bpp: 512 words (fixed)

Setting for display start address (REG[10h], [11h], [12h], [13h], [14h], [15h])

- For 16 bpp: 1024 - W (words)
- For 8 bpp: (1024 - W)/2 (words)

In the above, W is the number of lines on the screen after the portrait setting. For example, when a screen 640 pixels × 480 lines is rotated, W = 640. Note that in hardware portrait mode the processing size maximum value is fixed at 1024 pixels × 1024 lines. It is not possible to make a setting which exceeds this.

An example of the display address setting in hardware portrait mode is shown in Table 2-12. Note that in the quick debugger LCD command, setting HDP (REG[04h]) and setting REG[0Dh] Bit 7 to 1, automatically displays the settings of REG[10h] to [17h].

Table 2-12 Example of display address setting in hardware portrait mode

Display size	Register(s)	16BPP	8BPP
640 pixels × 480 lines	REG [10h] or [13h]	80h	C0h
	REG [11h] or [14h]	01h	00h
	REG [12h] or [15h]	00h	00h
	REG [16h]	00h	00h
	REG [17h]	04h	02h
320 pixels × 240 lines	REG [10h] or [13h]	C0h	16h
	REG [11h] or [14h]	02h	00h
	REG [12h] or [15h]	00h	00h
	REG [16h]	00h	00h
	REG [17h]	04h	02h

2.3.2.3. Frame Rate and Display Performance

To realize optimum display performance, the frame rate must be set close to the typical value for the LCD panel. Generally, if the LCD panel is operated at a lower frame rate, the panel may flicker, which is a factor to be considered. The frame rate can be calculated as follows. For details, see Section 14.2, "Frame Rate Calculation" in the "SED1355F0A Technical Manual."

Frame rate = DOTCLK Max. / (HDP + HNDP) × (VDP + VNDP)
Horizontal frequency = DOTCLK Max. / (HDP + HNDP)

- DOTCLK = PCLK, REG[19h] Bit[2:1]
- HDP = ((REG[04h] Bit[6:0]) + 1) × 8DOTCLK
- HNDP = ((REG[05h] Bit[4:0]) + 1) × 8DOTCLK
- VDP = (REG[09h] Bit[1:0]) & (REG[08h] Bit[7:0]) + 1
- VNDP = (REG[0Ah] Bit[5:0]) + 1

Table 2-13 shows example calculations of the frame rate. In the CARD-E09A, the following specification of video memory is used. This table shows parts of the specification extracted from Table 14-3 "Example Frame Rates with Ink Disabled" in the "SED1355F0A Technical Manual."

- 60ns EDO-RAM
- NRC = 4, NRP = 1.5, NRCD = 2 (see detailed description of REG[22h])

Table 2-13 Frame rate calculation examples (when MCLK = 33 MHz)

Display type	Resolution	BPP	Maximum DOTCLK [MHz]	Maximum HNDP [pixels]	Maximum frame rate [Hz]	
					Panel	CRT
・Single Panel	800 × 600	16	33	56	65	55
・CRT		8/4/2/1		32	66	
・Mono/Color Dual Passive Panel (Half Frame Buffer = Disable)	640 × 480	16		56	98	78
		8/4/2/1		32	101	
・CRT & Single Panel simultaneous display	640 × 240	16		56	200	-
・CRT & Mono/Color Dual Passive Panel simultaneous display (Half Frame Buffer = Disable)		8/4/2/1		32	203	
	480 × 320	16		56	196	
		8/4/2/1		32	200	
	320 × 240	16		56	380	
		8/4/2/1		32	388	
・Color Dual Passive Panel (Half Frame Buffer = Enable)	800 × 600	16	11	32	43	
		8/4/2/1	16.5		66	
・Mono Dual Passive Panel (Half Frame Buffer = Enable)	640 × 480	16	11		68	
		8/4/2/1	16.5		103	

Note:
The example is in internal clock mode. When using external clock input mode:

- MCLK = external clock source
- Note that maximum DOTCLK = external clock source or a division thereof, and the maximum HNDP and maximum frame rate values are different with internal clock mode.

If a bandwidth calculation is required to optimize the display performance, see Section 14.3, "Bandwidth Calculation" in the "SED1355F0A Technical Manual."

2.3.2.4. LCD and CRT Simultaneous Display

If the CRT and LCD panel used have overlapping frame rate rating ranges, then by setting the video parameters within the overlap range, and simultaneously setting REG[0Dh] Bit 1 (CRT Enable) and Bit 0 (LCD Enable), the CRT and LCD panel can be driven simultaneously.

Basically, when using a CRT display, the timing must meet the VESA (Video Electronics Standards Association) standard, but for a normal multiscan CRT, the frame rate synchronization can be achieved over the range 50 Hz to 130 Hz, so check the type of CRT being used.
Most LCD panels can be adjusted within the CRT synchronization frequency (50 Hz to 130 Hz) range, and therefore to use a simultaneous CRT and LCD panel display, first the parameters must be set so that the standard value of the frame rate for the LCD panel being considered for use is satisfied, and then a check made whether the values are within the rating range for the CRT being adopted. Table 2-14 shows standard VESA specifications.

Table 2-14 Standard VESA specifications

Resolution	Frame rate [MHz]	Horizontal frequency [KHz]	DOTCLK [MHz]	Standard
640 × 480	60	31.5	25.175	Industry Standard
	72	37.9	31.500	VESA Standard
	75	37.5	31.500	VESA Standard
800 × 600	56	35.1	36.000	VESA Standard
	60	37.9	40.000	VESA Standard
	72	48.1	50.000	VESA Standard
	75	46.9	49.500	VESA Standard

The CARD-E09A has a maximum specification for DOTCLK of 33.2 MHz, and therefore does not meet the standard for the 800 pixel × 600 line (SVGA) resolution, but as described above, if a multiscan CRT is used, a correct display may be able to be obtained.

2.3.2.5. Notes on Connecting a Monochrome LCD Panel

By setting REG[02h], bit 2 to 0, a monochrome (grayscale) LCD panel can be connected. In monochrome mode, output to the LCD panel selects only the green elements of the LUT. When simultaneous display with a CRT is selected, a color image is displayed on the CRT.

In monochrome mode, the maximum number of gray levels is 16. Even if more than 4 bpp is set, the display still has only 16 levels. Therefore, 8 bpp or 15/16 bpp settings do not increase the gray levels, but when the hardware portrait mode is used, an 8 bpp or 16 bpp setting is required. This is because the hardware portrait mode only operates in the 8 bpp and 16 bpp modes.

When operating with an OS developed using the "CARD-E09A Windows CE Development Kit," note the following points. This is because the LUT settings are optimized to display the Windows CE screen on a monochrome LCD panel. For details, see the "CARD-E09A Windows CE Development Kit Instruction Manual."

- The STARTUP.DAT setting must always be 8 bpp. This is so that 16 grayscale levels are displayed using an 8 bpp LUT for color. For details of the STARTUP.DAT settings, see Section 2.3.3.
- In the case of simultaneous display with a CRT, the CRT shows the same monochrome image as the LCD panel. This is because the setting uses the red, green, and blue elements of the LUT superimposed.
- When displaying on a monochrome LCD panel, there is no procedure to be noted during the NK.BIN (in Windows CE) build. If the monochrome LCD setting and the 8 bpp setting are made in STARTUP.DAT, then an LUT for the monochrome LCD panel is automatically used for the display.
- This function is supported from "CARD-E09A Windows CE 2.11 development kit Ver. 1.05." Note that it is not supported in previous versions.

2.3.3. STARTUP.DAT Settings

In this section, the SED1355 register settings determined in Section 2.3.2, "Panel Parameter Setup Method" are reflected in STARTUP.DAT. When the system is powered on, the Epson loader transfers the parameters written in STARTUP.DAT in sequence from the beginning of the file to the SED1355 registers. The sequence of the parameters is such as to take account of the power on/off sequence, and should not be changed.
The STARTUP.DAT file can be edited simply with a text editor.

Next a summary of the settings is given. The video parameters must be set at two places in the STARTUP.DAT file: key "1355" and key "1355PROPERTY". For details, see Section 13.1, "Startup Data Overview" in the "CARD-E09A Windows CE Development Kit Instruction Manual" supplied with the Windows CE Development Kit.

Table 2-15 shows the setting format for key "1355". Here the SED1355 internal register settings are specified. This should be checked with the sequence of steps in Section 2.3.1.2, "Power Sequence."

Table 2-15 Setting format for key "1355"

Index	Data	Comment
;FFFF0002	00	In external clock input mode (see Section 2.3.1.1.2.), remove the semicolon so that it is no longer a comment.
B4000023	80	REG[23h] setting. Set bit 7 (Display FIFO Disable) to 1, to set the display inhibit mode.
B4000001 • • • • • B40000022	Any value	REG[01h] to REG[22h] settings. Set the parameters as determined in Section 2.3.2.1, "SED1355 Register Settings." Here, do not set REG[0Dh]. <When in hardware portrait mode> ・REG[10h] to [12h] or REG[13h] to [15h] For 16 bpp: 1024-W For 8 bpp: (1024-W)/2 W = original screen width in pixels ・REG[16h], [17h] For 16 bpp: 1024 fixed For 8 bpp: 512 fixed <When connecting a monochrome panel with Windows CE> REG[16h], [17h] ; 8 bpp setting
B4000000D	Any value	REG[0Dh] setting. If bit 0 (LCD Enable) is set, then the LCD panel power on sequence starts. bit1 (CRT Enable) bit0(LCD Enable) 1 0 : CRT display 0 1 : LCD display 1 1 : CRT & LCD display <In hardware portrait mode> bit7 (Hardware Portrait Mode Enable) = 1 <When a monochrome panel is connected with Windows CE> 8BPP : bit4 = 0, bit3 = 1, bit2 = 1

;;;FFFF0004	Any value	When FPVCCON is turned on in the next step, the delay time from setting "LCD Enable" until it goes on is set in units of display frames. When the delay time setting is required, remove the semicolons so that this is no longer commented out. Example: If delay time = 128 Frames, set to "80h".
;;;FFFF0005	00	Removing the comment semicolons turns FPVCCON on. Use this in combination with the delay time setting.
FFFF0001	00	Clear screen.
B4000023	00	REG[23h] setting. Set bit 7 (Display FIFO Disable) to 0, and end the display inhibit mode.
FFFFFFFF	FFFFFFFF	End of initialization

Table 2-16 shows the setting format for key "1355PROPERTY". Here the data referenced when Windows CE starts is specified.

Table 2-16 Setting format for key "1355PROPERTY"

Column	Comment
Width, Height	Specify screen size to be displayed. Width = REG[04h] setting value (HDP) Height = REG[08h], [09h] setting value (VDP) <In hardware portrait mode > Width and height must be interchanged.
bpp, Frame Rate	Specify the number of bits of display data in each pixel and the frame rate. bpp = REG[0Dh], setting for bits 4 to 2 Frame Rate = setting calculated in Section 2.3.2.3 "Frame Rate and Display Performance" <When connecting a monochrome panel with Windows CE> BPP = 8
Wait Time for Suspend/Resume	Specify the delay time T4 (units: ms) when moving to suspend mode, or resuming. See Section 2.3.1.2, "Power Sequence." ・"FFFFh" (default): T4 = 10 ms Min. ・In external clock input mode, if T4 = 10 ms Min. cannot be satisfied, a setting change is required. Set the time in units of 1 ms. Example: When T4 = 100ms: "0064h" For the basis for determining the specified time, see Section 2.3.1.2.

2.3.4. Design Notes

The following points should be noted when designing the circuit connected to the LCD panel.

- Check that there is a match between the V_{OL}/V_{OH} rating of the CARD-E09A (the LCD panel I/F output signal rating is: V_{OL} = 0.3V Max., V_{OH} = V_{CC}-0.3V Min., V_{CC} = 3.3V) and the V_{IL}/V_{IH} specification of the LCD panel under consideration. If they do not match, to ensure that the LCD panel specification is met, a TTL level input CMOS device or similar should be inserted as a buffer in all signal lines.

- Be sure to check the LCD panel power on/off sequence rating. As described in Section 2.3.1.2, "Power Sequence," FPVCCON can be used for control of the LCD panel logic power, and FPVEEON for control of the LCD panel device power, but note that when buffers or similar are inserted in the signal lines, depending on the power switching circuit specification, the logic power on/off sequence and LCD panel refresh start timing (when the signal starts to be driven) may be reversed. In cases such as this, in the worst case the LCD panel could be damaged. If LCD panel logic power controlled by FPVCCON is connected to the buffer IC gate signal, then the above problem is solved. However, care is required in cases where there are stringent specifications for the time from applying the logic power until the signal begin to be driven.

- Connect a pull-down resistor of around 10 KΩ to FPVCCON. The SH7709A Port D register Bit 1 is connected to FPVCCON, but in the interval between the system power being applied and the initialization this port has an input setting with a pull-up resistor, and therefore if an external pull-down resistor is not provided, will be held high in this interval.

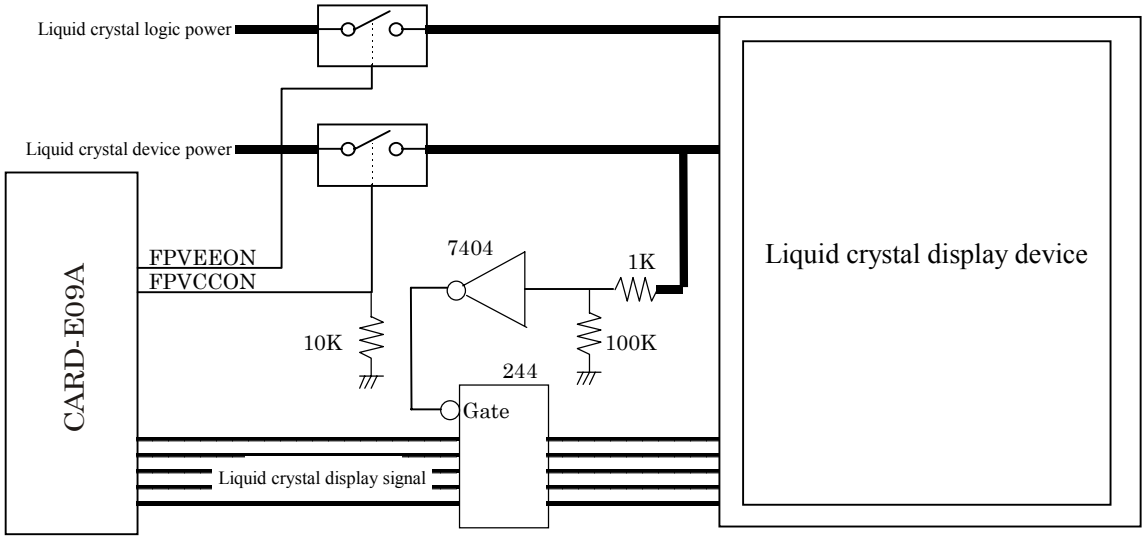


Fig. 2-3 Examples of connection using a buffer IC

- Even when an 18-bit TFT panel is connected, since the SED1355 supports up to 16-bit (65,536 colors), R0 and B0 are not driven. These data lines of the LCD panel should be held either high or low.

- When an external clock circuit is connected to EXTCLKI, the design must meet the conditions in Section 2.3.1.1.2, "External Clock Input Mode."

- Circuit connections to DOTCLK and EXTCLKI must be kept absolutely as short as possible.

3. External Buses

The CARD-E09A is provided with ISA, PCMCIA, and SH bus external expansion bus interfaces.

3.1. Memory Map

The SH7709A has eight memory areas. Since it has no I/O ports, I/O is carried out as memory mapped I/O. Table 3-1 shows the CARD-E09A physical address memory map.

Table 3-1 CARD-E09A memory map

SH7709A physical address	Area	Assignment	Remarks
00000000h to 03FFFFFFh	Area 0	Flash ROM mounted on CARD-E09A (stores IPL)	Normally cannot be used. When the system starts, execution branches to this area. By supplying a low input to pin 172, ROMDIS#, it is possible to start from external expansion ROM.
04000000h to 07FFFFFFh	Area 1	SH7709A internal registers	Cannot be used.
08000000h to 0BFFFFFFh	Area 2	SH BUS	Can be used.
0C000000h to 0FFFFFFFh	Area 3	SDRAM in CARD-E09A	Cannot be used.
10000000h to 13FFFFFFh	Area 4	Companion chip in CARD-E09A	Cannot be used.
14000000h to 17FFFFFFh	Area 5	SED1355 in CARD-E09A	Cannot be used.
18000000h to 1BFFFFFFh	Area 6	PCMCIA/ISA BUS	Can be used.
1C000000h to 1FFFFFFFh	Area 7	SH7709A internal registers	Cannot be used.

The SH bus is assigned to area 2, and the ISA bus / PCMCIA interface is assigned to area 6. Other areas cannot be used.

<< Notes on access >>

The SH7709A has a privileged mode (4 GB space) and a user mode (2 GB space). Table 3-1 shows the physical address space, which does not take account of these modes. Normally, when the user is developing device drivers for a circuit added to an external bus or application software, user mode is used. However, in this mode, since the whole region is a cacheable area, this cannot be used in cases where there would be problems if the data is rewritten from the cache.

In cases such as this, it is necessary to use area P2 (the area not cached) in privileged mode. In practice this means adding A0000000h to the physical address for the access address. For details, see the "SH3 Hardware Manual."

3.2. SH Bus

For details of timing etc., see the "SH3 Hardware Manual."

3.2.1. Notes on Operation

1) There are 26 address signal lines, A[25:0]. A[31:29], and A[28:26] are not connected to the CARD-E09A interface internally. To access area 2, since the fixed internal setting in the CARD-E09A is A[28:26] = [0,1,0], if in an external device address decoding circuit A[25:0] and CS2# are used, there is no problem.

2) Addressing is little-endian. Big-endian is not supported.

3) The memory which can be connected is SRAM, ROM, and other normal memory. The CARD-E09A does not have RAS signal and CAS signal connections, and therefore a RAM device cannot be connected. When Windows CE is used, if a memory controller is connected externally, and a RAM device added, correct operation is not possible. This is because unless it is sequential memory expansion, Windows CE cannot be recognized.

4) By default, the bus width is set to 16 bits. When using an 8-bit width, the SH7709A BCR2 register setting must be changed. Note that the SH7709A also supports a 32-bit width, but in the CARD-E09A, only the 16 data signal lines D[15:0] are present on the interface, and so this cannot be used.

5) The initial idle cycle setting is 1 idle cycle. In the SH7709A, setting up to 3 idle cycles is possible. When a change is required, a change in the setting of the SH7709A WCR1 register is required.

6) The initial wait cycle setting is 3 wait cycles. In the SH7709A, a 1 or 2 wait cycle setting is also possible. When a change is required, a change in the SH7709A WCR2 register setting is required. In addition to the above software settings, a wait cycle can be inserted in hardware by inputting active low to the WAIT# pin. For details, see Section 3.2.2, "Wait Cycles."

7) Do not input an active low signal simultaneously to both of the RESETP# and RESETM# pins. A reset may not be generated.

8) When using the clock output (CKIO) in an external circuit, due care must be taken of the capacitive component of the connected device, and with attention to the following item, the waveform must be met specification, and the delay time kept to a minimum. CKIO is used internally to the CARD-E09A, and therefore there is a possibility of the CARD-E09A itself being unable to carry out normal operation.
   - The external circuit must be connected in such a way that the CKIO clock timing specifications in Chapter 8, "AC characteristics" of the "CARD-E09A Hardware Manual" are met.
   - Clock line on a PCB must be absolutely as short as possible, no more than 20 mm.
   - If a connected device has a large capacitive component, insert a buffer between the CARD-E09A interface and the device. Even in this case, the interconnect between the CARD-E09A interface and the buffer should not exceed 20 mm.
   - If CKIO is not used, leave the pin unconnected.

3.2.2. Wait Cycles

There are two methods of inserting a wait cycle, as follows. For more details, see Section 5.17, "SH7709A BUS" of the "CARD-E09A Hardware Manual."

Method 1: by software setting
- A setting of up to 3 wait cycles can be achieved with the SH7709A WCR2 register.
- The initial setting is 3 wait cycles.
- Regardless of requests from an external circuit or application software, the set number of wait cycles is always inserted.

Method 2: by request from external circuit
- A wait cycle can be inserted by wait request input to WAIT#, pin 66 of the CARD-E09A interface.
- If the WCR2 register is set to 0 wait cycles, the wait request is not accepted.
- When a wait cycle is set by method 1, if a wait request is input it is not accepted.

Note the following points when using method 2.

1) The WAIT# signal is sampled on the rising edge of CKIO. To change to sampling on the falling edge, a change in the setting of SH7709A WCR1 register is required.

2) If the WAIT# signal is not synchronized to CKIO, then the CARD-E09A may malfunction. When generating the WAIT# signal, ensure a setup time (10 ns Min.) and a hold time (0 ns Min.) with respect to CKIO.

3) Note that if a wait exceeds 15 μs, the refresh operation of the SDRAM in the CARD-E09A will stop, and therefore data loss may occur.

3.3. ISA bus

As shown in Table 3-1, the ISA bus physical addresses are assigned to area 6. In area 6, the 4 MB from 1B800000h to 1BBFFFFFFh is assigned to a memory space, and the 4 MB from 1BC000000h to 1BFFFFFFFh is assigned to I/O space. However, since the ISA bus space is 16 MB, the top two bits (CA[23:22]) of the address are specified by the ISA Address Register (11000780h) of the companion chip, to define the logical address. The lower part of the address uses A[21:0] in the same way as the SH bus. Fig. 3-1 shows the ISA bus mapping. For details, see Section 5.13, "ISA Interface" in the "CARD-E09A Hardware Manual."

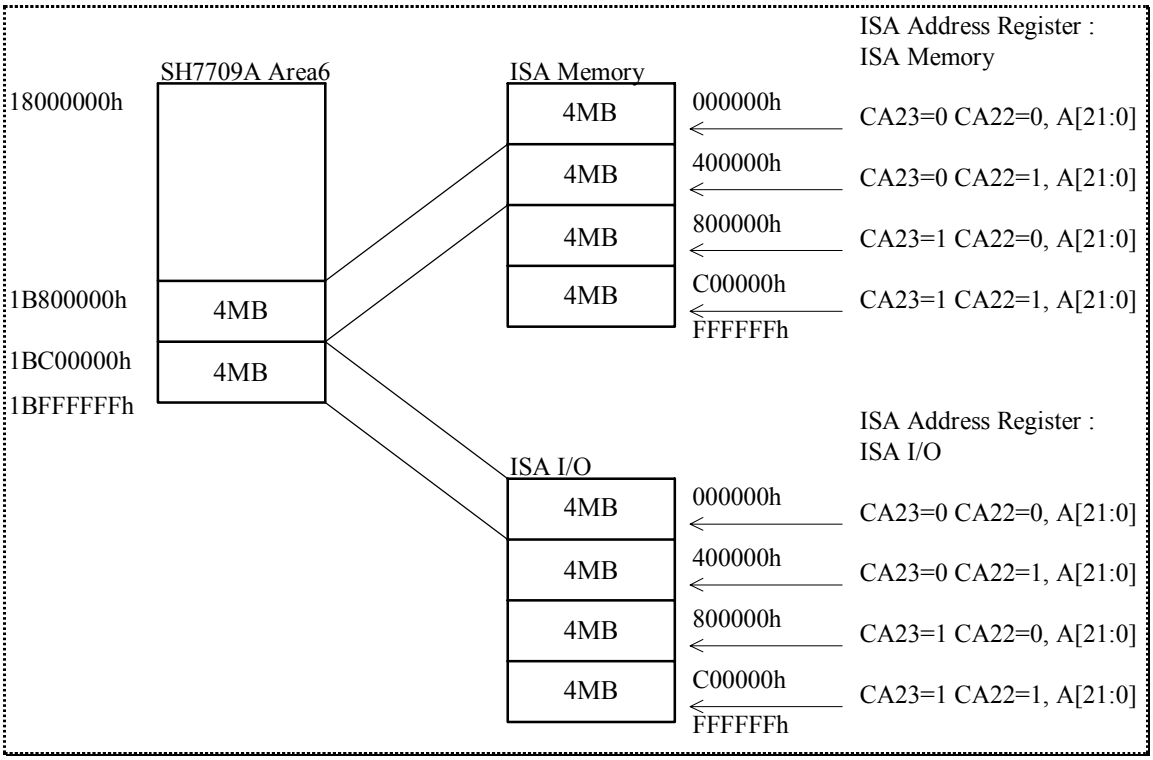


Fig. 3-1 ISA bus mapping

3.3.1. Differences from Full ISA Bus

The CARD-E09A ISA bus is different from the so-called IBM PC/AT "Full ISA bus." Table 3-2 shows the differences.

Table 3-2 Differences from full ISA bus

Item	CARD-E09A ISA bus	Full ISA BUS
ISA memory space	16 MB space. In the ISA Address Register, bits[1:0], specify CA[23:22], to access area 6. The address signals are CA[23:22], A[21:0].	16 MB space. Direct access with LA[23:17], SA[19:0].
ISA I/O space	16 MB space memory mapped I/O. In the ISA Address Register, bits [5:4], specify CA[23:22], to access area 6. The address signals are CA[23:22], A[21:0].	64 KB space. Direct access with SA[9:0].
Number of waits	2 wait cycles Designed to ensure compatibility with full ISA bus 16-bit access, so in 8-bit access the cycle is not extended. If the cycle must be extended, it is necessary to assert IOCHRDY.	16bit Access = 0 wait, 3 SCLK 8bit Access = 3 wait, 6 SCLK SCLK = 8.33MHz
(#1) DC characteristics	3.3 V-tolerant.	5 V-tolerant.
(#2) IRQ	IRQ[4:1], 4 channel support.	IRQ[15:1], 15 channel support. Rising edges are sensed.
(#3) SMEMR# SMEMW#	None. Signals for XT BUS (1 MB and below) are not supported. If necessary, can be generated in an external circuit.	Yes.
(#4) AEN DRQ DACK#	Two channels of the SH7709A internal DMAC are available. But this is different from normal I/O ⇔ memory DMA.	I/O ⇔ memory DMA is supported.
TC REFRESH# MASTER# WS0#	None.	Yes.
IOCHCK#	None. If necessary, the NMI pin can be used for this. But software support is required.	Yes.
(#5) BALE	None.	Yes.
SCLK OSC	None. If necessary, can be constructed externally, but in that case is asynchronous.	Yes.
ISADATAENA# RD/WR#	Control signal for data buffer connected between the CARD-E09A interface and an external expansion device Gate control: ISADATAENA# Direction control: RD/WR#	None.

(#1) When 5V operation device are expanded, buffers or level shifters must be inserted in lines D[15:0] and IRQ[4:1]. However, the MEMCS16#, IOCS16#, and IOCHRDY pins are tolerant of a 5V input, so a buffer or similar is not required, but depending on the device specification, insert a pull-up resistor of around 1 KΩ to 3.3V or 5V.

(#2) IRQ1 is assigned to the LAN circuit on the evaluation board. For this reason, the LAN driver supplied with the "CARD-E09A Windows CE Development Kit" uses IRQ1 (rising edge sense). In the evaluation board, IRQ[4:2] are not used, and therefore these lines are masked. When IRQ1 is used for another purpose, or when IRQ[4:2] are used, a device driver must be created to set the SH7709A interrupt control register.

(#3) A block diagram for generating SMEMR# and SMEMW# externally is shown in Fig. 3-2.

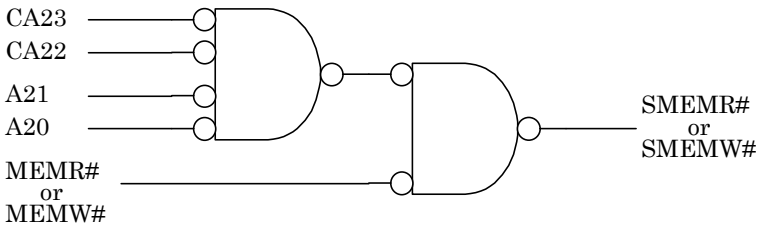


Fig. 3-2 Block diagram for generating SMEMR#/SMEMW#

(#4) SH7709A I/O is memory-mapped I/O, and therefore the supported DMA transfers from memory to memory. In the CARD-E09A, two channels of the SH7709A internal four-channel DMAC are available on the four pins which are DREQ[1:0]# and DACK[1:0]#, but the DMA is different from that on a full ISA bus. For details, see the "SH3 Hardware Manual." Note that the remaining two channels are used as SCIF and AUDIO internally to the CARD-E09A.

(#5) In a full ISA bus, BALE is used to latch LA[23:19], but all of the CARD-E09A address lines are latched so this is not necessary internally.

3.3.2. 8/16-bit Devices

The data bus on the ISA bus can either be 8- or 16-bit. If the cycle target is 8-bit device, CARD-E09A sends data using [D7:0]; if the cycle target is 16-bit device, then CARD-E09A sends data using [D15:0]. Therefore, when the cycle target is a 16-bit device, the device needs to drive MEMCS16# or IOCS16# to become active, and inform CARD-E09A that the target is a 16-bit device. Because MEMCS16#/IOCS16# is a signal that can be "Wired Or", it must be driven at the open collector.

These are 5 V-tolerant input signals, and can drive at 5V or 3.3V depending on the connected device. Internally to the CARD-E09A they are not pulled up. An external pull-up resistor of around 1 KΩ must always be provided to pull up to 5V or 3.3V. By the provision of the pull-up resistor, they are normally (when low is not driven) inactive. Because of this reason, an 8-bit device does not need to drive MEMCS16#/IOCS16# to become inactive.

Fig. 3-3 shows an example of a circuit for generating MEMCS16#. This is an example of a memory device mapped to logical addresses A00000h to BFFFFFh. Assuming that first CA23=1, CA22=0 is set by an ISA address register setting, accessing addresses 1BA00000h to 1BBFFFFFh in the SH7709A 4 MB memory space 1B800000h to 1BBFFFFFh actually accesses logical addresses A00000h to BFFFFFh. The address is decoded, and provides an open collector drive to MEMCS16#. The address lines used in decoding are all latched.

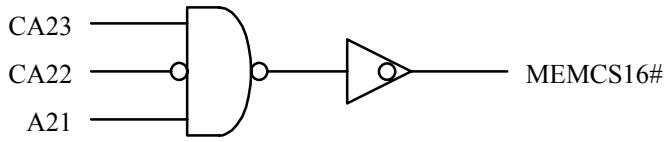


Fig. 3-3 Example circuit for generating MEMCS16# (1)

Fig. 3-4 shows an example of a memory device mapped to logical addresses 0D0000h to 0DFFFFh. In this case again, the address is decoded, and MEMCS16# is driven with an open collector.

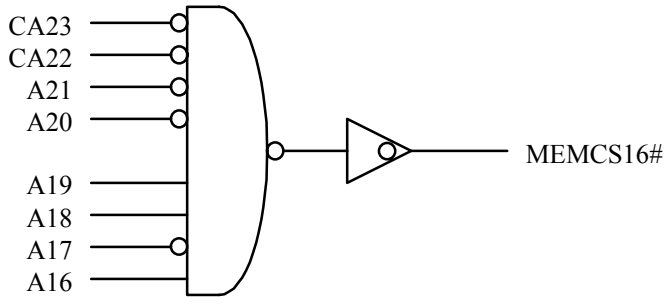


Fig. 3-4 Example circuit for generating MEMCS16# (2)

Above example circuits for generating MEMCS16# were shown, but the case for IOCS16# is exactly the same. For details of the MEMCS16#/IOCS16# timing specifications, see Chapter 8, "AC Characteristics" in the "CARD-E09A Hardware Manual."

3.3.3. Other Notes

This section describes notes on operation not already covered above.

1) For area 6 to which the ISA bus and PCMCIA interface are assigned, the IPL (part of the Epson Windows CE loader) stored in flash ROM mounted on the CARD-E09A sets the SH7709A bus state controller (BSC) as shown below during the power-on sequence. Do not change these settings under any circumstances, because this may cause operation to fail. Note that the bus width is set to 16 bits, but if the access method is set to PCMCIA, then if MEMCS16# / IOCS16# cannot be asserted, 8-bit access is possible.

   Access method : PCMCIA
   Bus width : 16 bits
   Wait cycles : 2 wait cycles
   Idling cycles : 2 idle cycles

2) MEMCS16#, IOCS16#, and IOCHRDY must be connected to 5V or 3.3V by a pull-up resistor of around 1 KΩ.

3) It is possible to extend cycles by asserting IOCHRDY, but do not do this for more than 15 μs. The refresh operation of the SDRAM in the CARD-E09A will stop, and therefore SDRAM data loss may occur.

4) When deasserting IOCHRDY, the hold time (0 ns Min.) for the data lines (D[15:0]) must be strictly observed. See Chapter 8, "AC Characteristics" of the "CARD-E09A Hardware Manual."

3.4. PCMCIA Interface

As for the ISA bus, the physical addresses are assigned to area 6. In the CARD-E09A, a PCMCIA memory space and a PCMCIA I/O space, each with a maximum of 64 MB are supported. The CARD-E09A is provided with three interfaces: a CompactFlash card interface connecting to CARD-E09A directly (no "hot plugging"), and PCMCIA Slot A and Slot B interfaces. Below, "compact flash card" is abbreviated to "CF."

3.4.1. Access Method

3.4.1.1. Windows

For each of the memory and I/O 64 MB spaces, access is made through an 8 MB window assigned in area 6. There are two windows, for memory space and for I/O space.

The 8 MB window is specified by the companion chip Slot Configuration Register: "Slot A=11000100h, Slot B=11000140h, Compact Flash CARD=11000180h" (Memory area Select bit, I/O area Select bit). When using the Epson Windows CE development environment, when system power is on, the IPL (part of the Windows CE loader) stored in flash ROM mounted on the CARD-E09A first carries out window setting, making possible access to Windows CE itself (NK.BIN) which is stored on a PC card (normally CF). Thereafter, the Windows CE PCMCIA driver resets the windows. The window assignment is shown in Table 3-3.

Table 3-3 PCMCIA space 8 MB window

	Window Address	Windows CE driver setting	IPL setting
Memory Window	18000000h to 187FFFFFh	Slot A	Invalid
	18800000h to 189FFFFFh	Slot B	Invalid
	19000000h to 197FFFFFh	CF	Valid
I/O Window	1A000000h to 1A7FFFFFh	Slot A	Invalid
	1A800000h to 1AFFFFFFh	Slot B	Invalid
	1B000000h to 1B7FFFFFh	CF	Invalid

Slot A : PCMCIA Slot A
Slot B : PCMCIA Slot B
CF : CompactFlash card inserted on CARD-E09A

As shown in Table 3-3, first the IPL has the memory window 19000000h to 197FFFFFh set to be valid. Other windows are left invalid, and I/O card operations are not carried out. At this time, each of the slots - slot A, slot B, and CF - can only accept a memory card such as an ATA on which is stored an SBR (Sub Boot Record: for details, see the "CARD-E09A Windows CE Development Kit Operation Manual"). Again, since only one window is valid, the three slots cannot be used simultaneously. The slot priority is in the sequence Slot A => Slot B => CF. Table 3-4 shows the slots recognized.

Table 3-4 Slot priority sequence in IPL setting

Slot recognized	Slot A connected or disconnected	Slot B connected or disconnected	CF connected or disconnected
Slot A	A	NA	NA
Slot B	NA	A	NA
Slot A	A	A	NA
CF	NA	NA	A
Slot A	A	NA	A
Slot B	NA	A	A
Slot A	A	A	A

A : A PC card containing an SBR is inserted
NA : No PC card is inserted, or a PC card not containing an SBR is inserted

The quick debugger supplied with the "CARD-E09A Windows CE Development Kit" or "CARD-E09A evaluation kit (SCE88J0X01)" recognizes a PC card (CF or ATA card) in the above priority sequence. When the setting in the IPL is finished, control is passed to the PC card containing the SBR and Windows CE, and then the Windows CE PCMCIA driver resets the windows. If Windows CE is not to be run, software such as a device driver for window setting must be prepared.

3.4.1.2. Bank Switching

To allow access through the 8 MB windows set as described in Section 3.4.1.1, "Windows," to a 64 MB space for each of memory and I/O, the top 3 bits (CA[25:23]) of the address are specified by the companion chip Slot Address Register "Slot A=11000102h, Slot B=11000142h, CompactFlash card=11000182h" (Slot Memory Address bit, Slot I/O Address bit), and logical addresses defined. The lower part of the address uses A[21:0] in the same way as the SH bus. Fig. 3-5 shows the PCMCIA bus mapping. For details, see Section 5.12, "PCMCIA/CompactFlash Interface" in the "CARD-E09A Hardware Manual."

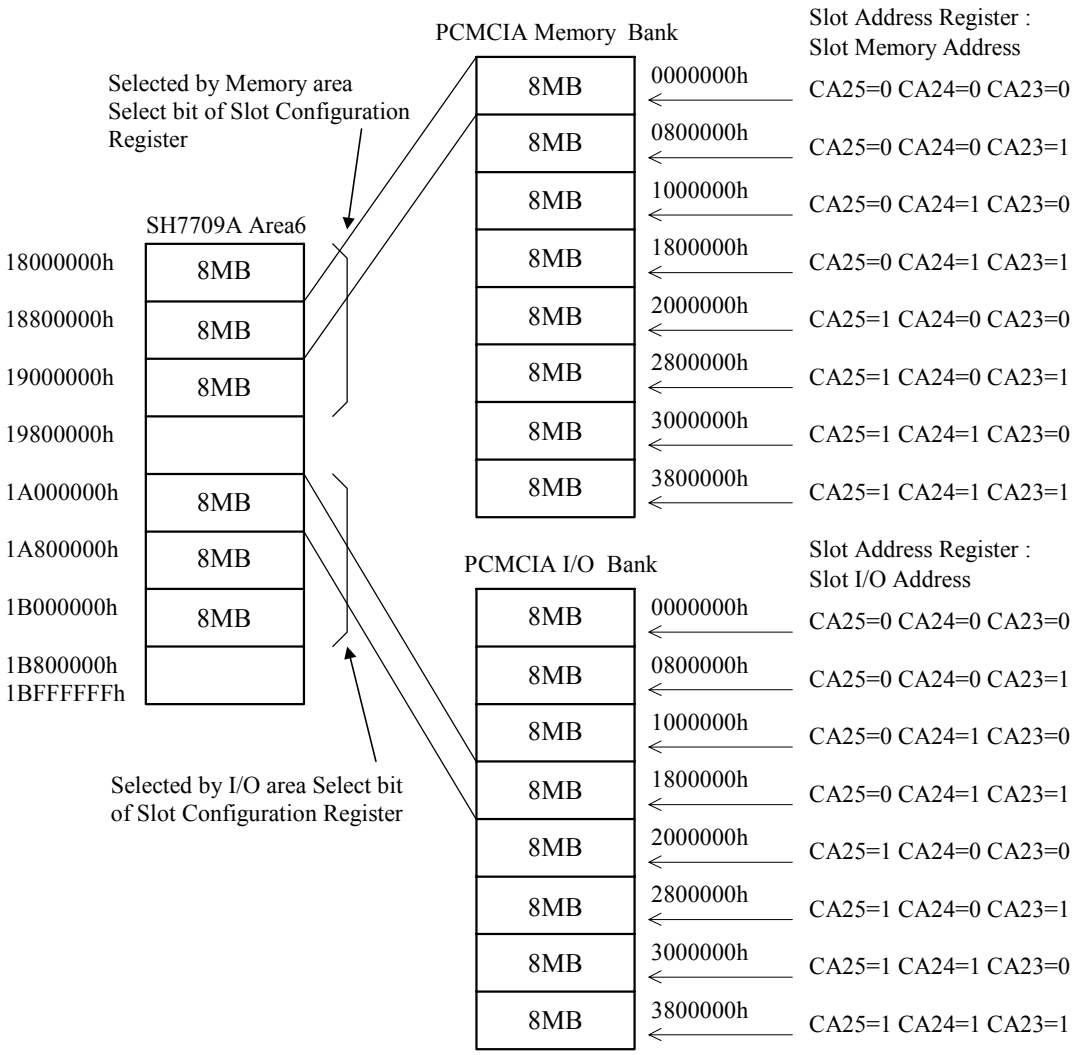


Fig. 3-5 PCMCIA bus mapping

In Fig. 3-5, PCMCIA Memory Bank and PCMCIA I/O Bank are selected by the setting of CA[25:23], and each divided into 8 MB units. For this reason, when exceeding 8 MB and accessing the next bank, software such as a device driver is required to do bank switching.

3.4.2. CompactFlash card connection to the PCMCIA Slot

This section describes an example of connecting a CF directly to the CARD-E09A PCMCIA interface (Slot A, Slot B). When connecting a normal 68-pin type of card, see Sheet 6, "PCMCIA Interface" and Sheet 7, "Buffer circuit for PCMCIA Interface" in Section 13.2.1.2, "Reference Circuit Diagrams."

Fig. 3-6 shows an example of connection of a CF in the PCMCIA slot.

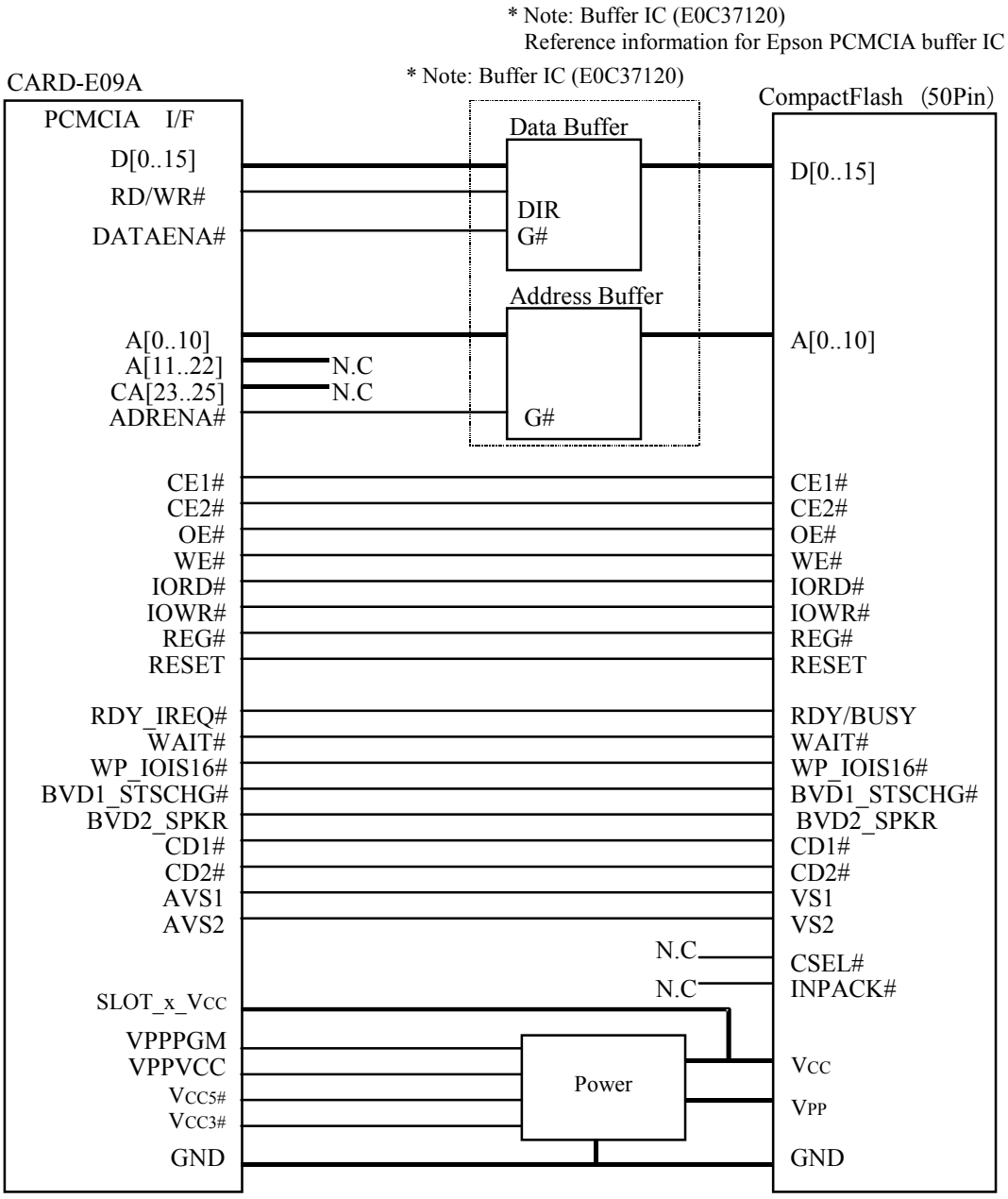


Fig. 3-6 Example of connection of a CF in the PCMCIA slot

The CF can be inserted on the CARD-E09A, but there are the following advantages when connected to the PCMCIA slot.

- A design allowing "hot plugging" is possible (a CF inserted on the CARD-E09A does not allow this function).
- Depending on the CF and motherboard specifications, either 5V or 3.3V power can be used (CF inserted on CARD-E09A is restricted to 3.3V).
- Since the interface connector can be mounted at any position on the motherboard, a configuration so that it can be inserted and removed externally can be considered.
- Since the size is smaller than a 68-pin type PC card, the system can be made more compact.

3.4.3. 8/16-bit Access

The PCMCIA interface is set to the 16 bit bus width by the IPL and Windows CE driver setting, but if the card select signals (ACE1#, ACE2#, BCE1#, BCE2#) and A0 specify byte access, and in the I/O card mode when AWP_IOIS16# or BWP_IOIS16# is "High" level output from the PC card 8-bit access is possible. (In the I/O card mode, during the access to the I/O card, AREG# or BREG# are driven low.)

Table 3-5 shows the assignment in memory card mode, and Table 3-6 shows the assignment in I/O card mode and when PC card attribute memory is being accessed. These settings comply with PCMCIA/JEIDA standards.

Table 3-5 Assignment in memory card mode

Mode	REG#	CE2#	CE1#	A0	OE#	WE#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	Hi-Z	Hi-Z
8bit READ	H	H	L	L	L	H	Hi-Z	EVEN byte
	H	H	L	H	L	H	Hi-Z	ODD byte
	H	L	H	X	L	H	ODD byte	Hi-Z
8bit WRITE	H	H	L	L	H	L	Don’t care	EVEN byte
	H	H	L	H	H	L	Don’t care	ODD byte
	H	L	H	X	H	L	ODD byte	Don’t care
16bit READ	H	L	L	X	L	H	ODD byte	EVEN byte
16bit WRITE	H	L	L	X	H	L	ODD byte	EVEN byte

REG# : AREG#, BREG# CE2# : ACE2#, BCE2# CE1# : ACE1#, BCE1#
OE# : AOE#, BOE# WE# : AWE#, BWE#

Table 3-6 Assignment in I/O card mode and when accessing attribute memory

Mode	REG#	CE2#	CE1#	A0	IORD#	IOWR#	D[15:8]	D[7:0]
Standby	X	H	H	X	X	X	Hi-Z	Hi-Z
8bit READ	H	H	L	L	L	H	Hi-Z	EVEN byte
	H	H	L	H	L	H	Hi-Z	ODD byte
	H	L	H	X	L	H	ODD byte	Hi-Z
8bit WRITE	H	H	L	L	H	L	Don't care	EVEN byte
	H	H	L	H	H	L	Don't care	ODD byte
	H	L	H	X	H	L	ODD byte	Don't care
16bit READ	H	L	L	X	L	H	ODD byte	EVEN byte
16bit WRITE	H	L	L	X	H	L	ODD byte	EVEN byte

REG# : AREG#, BREG# CE2# : ACE2#, BCE2# CE1# : ACE1#, BCE1#
IORD# : AIORD#, BIORD# IOWR# : AIOWR#, BIOWR#

3.4.4. Interface Timing

3.4.4.1. PCMCIA Timing

For details of 16-bit access timing, see Section 5.12.3, "Timing" in the "CARD-E09A Hardware Manual." This section describes the timing for 8-bit memory access. The timing for 8-bit I/O access is the same, so it is omitted.

Area 6	Access method	PCMCIA
	Bus width	8 bit
	Number of waits	Insert 2 waits
	Idle cycles	Insert 2 idle cycles
	Address -OE#/WE# assert delay	1.5 cycles delay
	OE#/WE# negate-address delay	3.5 cycles delay
PTG7	Connector function	General-purpose port

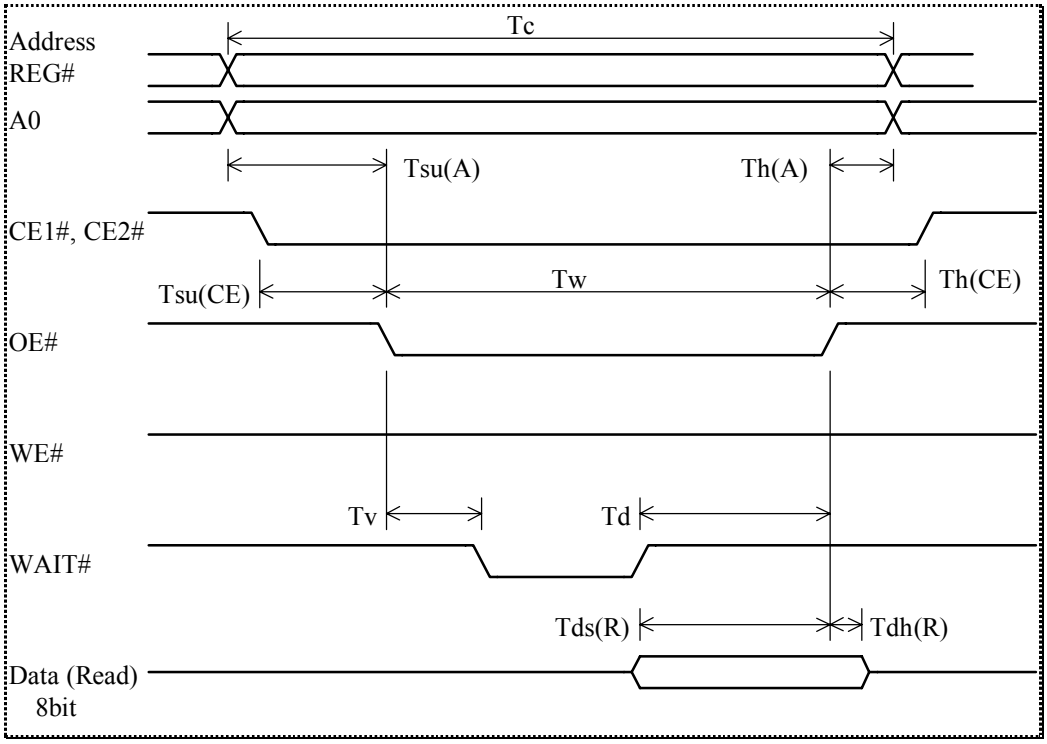


Fig. 3-7 PCMCIA 8bit Memory READ Timing

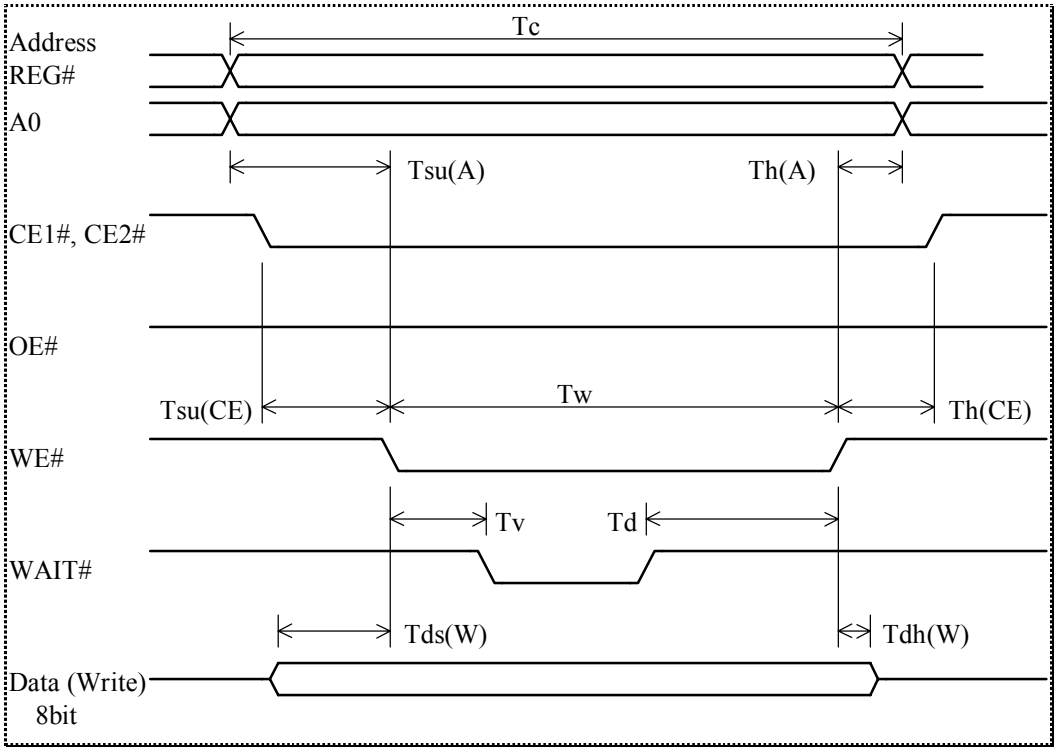


Fig. 3-8 PCMCIA 8bit Memory WRITE Timing

Table. 3-7 PCMCIA Memory 8bit READ/WRITE Timing

Parameter	Symbol	Min.	Typ.	Max.	unit
Cycle Time	Tc	17			CKIO
Address Setup Time	Tsu(A)		6		CKIO
CE# Setup Time	Tsu(CE)		6		CKIO
Address Hold Time	Th(A)		3		CKIO
CE# Hold Time	Th(CE)		3		CKIO
OE#/WE# Pulse Width	Tw		8		CKIO
WAIT# Valid from OE#/WE#	Tv			4	CKIO
OE#/WE# Hold Time from WAIT# Inactive	Td	4			CKIO
Data Setup Time (Read)	Tds(R)	0.5			CKIO
Data Hold Time (Read)	Tdh(R)	0			CKIO
Data Setup Time (Write)	Tds(W)		6		CKIO
Data Hold Time (Write)	Tdh(W)		3		CKIO

3.4.4.2. External Buffer Control Timing for Address/Data Signals

Depending on the PC card inserted in the PC card slot (Slot A or Slot B), slot power may use 5V or it may use 3.3V. CARD-E09A references AVS[2:1] and BVS[2:1] input pins, and detects the power voltage requested by the PC card inserted in the slot, and outputs power control signals (AVCC5#, AVCC3#, BVCC5#, and BVCC3#). In the external circuit these signals must be detected and used to control the slot power. For details of power control, see Section 5.12.4, "Slot Power ON/OFF Signals," Section 5.12.5. "Slot Signals at Power-Off," and Section 5.12.6, "Slot Power-On/Off Timing" in the "CARD-E09A Hardware Manual." Read this in conjunction with the reference circuit diagram on Sheet 6, "PCMCIA Interface" of Section 13.2.1.2, "Reference Circuit Diagrams" of this application note.

When switching the slot power, the PCMCIA interface signal lines must also be 5 V-tolerant and 3.3 V-tolerant with respect to the slot power. For applications such as this, a buffer IC (E0C37120) with internal voltage level shifter function is available. For the method of connection, see Sheet 7, "Buffer circuit for PCMCIA Interface" in Section 13.2.1.2, "Reference Circuit Diagrams."
This buffer IC can be used for the PCMCIA interface address and data lines. Signals other than the address and data lines have level conversion supported internally to the CARD-E09A, and it is not necessary to connect an external buffer IC. See Section 7.4, "Pin Characteristics" in the "CARD-E09A Hardware Manual." In the table, the "Group" column the source power pin is listed. The PCMCIA interface signals are in groups, "Slot_A," and "Slot_B," and these use respective SLOT_A_V_{CC} (Slot A power voltage) and SLOT_B_V_{CC} (Slot B power voltage) as source power. Signals other than the address and data lines are input and output from the CARD-E09A at the SLOT_A_V_{CC} and SLOT_B_V_{CC} voltage levels. The CARD-E09A SLOT_A_V_{CC} and SLOT_B_V_{CC} pins must always be connected to the corresponding slot power.

<<Control signal timing for the buffer IC (E0C37120)>>

In the CARD-E09A, a gate signal is provided for buffer IC control. Normally, for a DIR (direction) signal is used RD/WE#. For connections, see the above reference circuit diagrams.

- AADRENA#, BADRENA#: gate control signals for address bus
  The setting of the PCMCIA Power Control Register internal to the companion chip, and the input level of the card detect signals (ACD[2:1]#, BCD[2:1]#) must be checked. When a PC card is inserted in the slot, and the CardEnable bit is set to "Enable", then this is driven low. Since the levels before accessing the PC card are confirmed, it is not necessary to consider the timing. For details, see Section 5.12.4, "Slot Power-On/Off Signals," Section 5.12.5, "Slot Signals at Power-Off," and Section 5.12.6, "Slot Power-On/Off Timing" in the "CARD-E09A Hardware Manual."

- ADATAENA#, BDATAENA#: gate control signals for data bus
  As with the gate control signals for the address bus see the "CARD-E09A Hardware Manual." The AC timing of the gate control signals for the data bus is described under "PCMCIA Timing" in Chapter 8, "AC characteristics," of the "CARD-E09A Hardware Manual."

- RD/WE#: direction control signal
  The timing is the same as for address signals. This is described in Figure 8-3, "SH-BUS Timing" in Chapter 8, "AC characteristics," of the "CARD-E09A Hardware Manual."

3.4.5. Other Considerations

This describes notes on operation not covered above.

1) "Hot-plugging" of a CF in the CARD-E09A itself is not supported.

2) The CARD-E09A interface must always be connected to slot power (A_SLOT_VCC, B_SLOT_VCC). The CARD-E09A internally also uses these power supplies in the PCMCIA circuit. If not connected the CARD-E09A will not operate correctly. If the PCMCIA function is not used, connect VCC.

3) As described in Section 3.3.3, "Other Notes," do not change the settings of the SH7709A bus state controller (BSC).

4) The card detect signals (ACD[2:1]#, BCD[2:1]#), and voltage sense signals (AVS[2:1], BVS[2:1]) are pulled-up to VCC (3.3V) internally to the CARD-E09A. Do not pull-up an external circuit or connected PC card to 5V. There is a possibility of damage. These signals are normally connected to ground or left open-circuit within the PC card. If the PC card is left connected, note that a current will flow between the CARD-E09A internal 3.3V line and the PC card ground. When in suspend or other low current consumption mode, it is recommended to remove the PC card.

5) In the PCMCIA/JEIDA standard, in I/O card mode, "-SPKR" (digital audio signal) is assigned to pin 62 of the 68-pin interface, but this is not supported by the CARD-E09A.

6) When using a 3.3V power specification memory card, check that the CARD-E09A timing specification is complied with. Depending on the PC card, the specification may not be met in the read cycle.

4. Serial Communication Interface

4.1. Serial Interface

The CARD-E09A incorporates a total of five serial controllers, three (serial 0 to 2) internal to the SH7709A, and two (serial 3, 4) internal to the companion chip. When the "CARD-E09A Windows CE Development Kit" development environment is used, serial 0 to 2 have input the CPU peripheral clock signal (33.2 MHz) divided by 16, and serial 3 and 4 have a 1.8432 MHz input.

Table 4-1 Serial interfaces

	Basic specification	FIFO	Bit rate (bit/s)	Maximum error (%)
Serial 0	SH7709A internal	None	50 to 115200	At 56000 bps: 2.5 Other cases: 0.6
Serial 1	SH7709A internal Can be used by switching with IrDA 1.0	Yes	50 to 115200	
Serial 2	SH7709A internal	Yes	50 to 115200	
Serial 3	16550 compatible	Yes	50 to 115200	2.86
Serial 4	16550 compatible	Yes	50 to 115200	

CARD-E09A's serial port interface can drive the TTL device directly, but long distance transfer via devices such as RS-232 requires driver/receiver IC that meets the standard specification. Sheet 4 "Serial Interface" in Section 13.2.1.2, "Reference Circuit Diagrams" shows an example circuit.

In this example circuit, serial 0 to 4 are connected as follows.

Table 4-2 Connections on the evaluation board

	Connections in the reference circuit diagram
Serial 0	Connected to CN4 at TTL levels
Serial 1	・Connected to CN6 through RS-232C-compliant driver/receiver IC ・Branch to CN4 for IrDA connection (the IrDA circuit is externally connected to CN4)
Serial 2	Connected to CN6 through RS-232C-compliant driver/receiver IC
Serial 3	Connected to CN8 through RS-232C-compliant driver/receiver IC
Serial 4	Connected to CN10 through RS-232C-compliant driver/receiver IC

In the example circuit, serial 0 is directly connected to the connector, but if necessary a driver/receiver IC can be inserted. In the "CARD-E09A Windows CE Development Kit," no device driver is provided for serial 0, so that if necessary, it must be separately created. Again, serial 1 is designed so that it can be driven with switching to IrDA (RXD line can be switched with 0-Ω resistors - R35, R36), but if necessary an optimized design can be used.

In the evaluation board, an NEC μPD4724 is used as the RS-232C-compliant driver/receiver. This IC converts between CARD-E09A TTL level signals and RS-232C-compliant signals. Since the CARD-E09A STANDBY# and μPD4724 STBY# signals are connected, when the CARD-E09A goes into the suspend mode, this IC can also be put on standby. However, note that it is not possible to resume using RI# on serial 3 and 4. The μPD4724 is only guaranteed up to a transfer rate of 9600 bps. To implement 115 kbps, consider a different IC.

4.2. Infrared Communication

The CARD-E09A supports IrDA 1.0 infrared communications. This function uses the SH7709A internal serial controller 1, and therefore when using infrared communications, serial 1 cannot be used. The selection between IrDA and serial 1 can be made when building Windows CE, or dynamically using a Registry editing tool. For details, see the "CARD-E09A Windows CE Development Kit Instruction Manual."

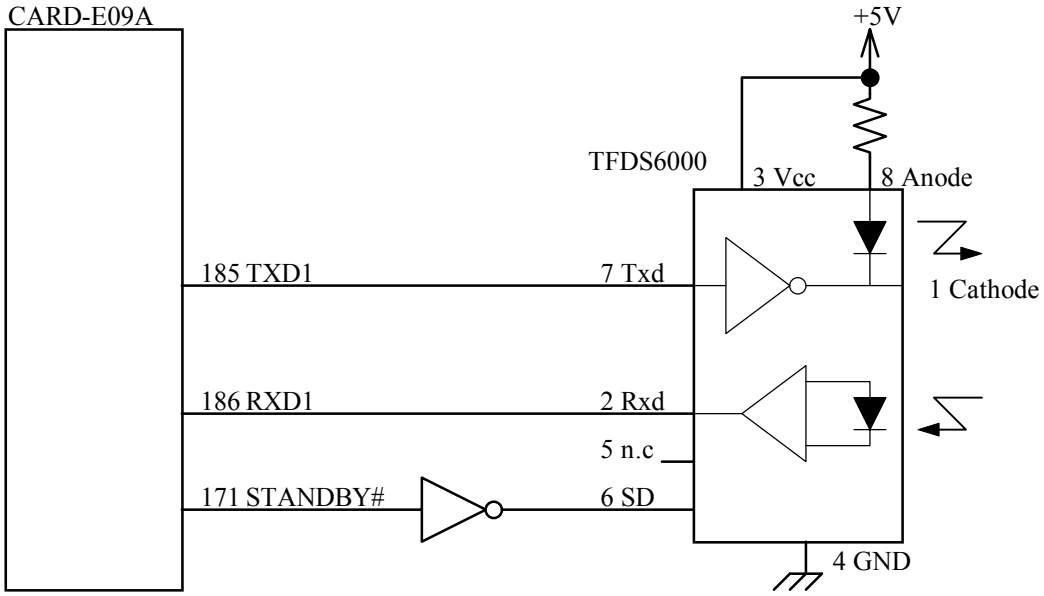


Fig. 4-1 IrDA interface conceptual diagram

Fig. 4-1 shows the concept of the infrared communications interface using the TFDS6000 made by TEMIC. A reference example circuit is shown in Section 13.2.3, "IrDA." TFDS6000 is a light module with built-in light emission and light reception capability for infrared communication.
If the IrDA light module supplies power to the LED for a long time, the LED may become damaged. For this reason, to prevent the optical module input connector (Txd) from remaining high for a long time, thus leaving the photoemitter element continuous activated, the software must ensure that the CARD-E09A output (TXD1) is not held high, or a differentiator circuit must be inserted between the CARD-E09A TXD1 connector and the optical module input connector as protection. Polarity of the TXD1 of CARD-E09A is as follows:

1. Default (reset)
   TXD1 is in the OFF state of the 3-State.
2. During transmission
   TXD1 sends data at active high. Be sure to design in a way so that the LED lights when TXD1 is HIGH.

5. Parallel Port Interface

The CARD-E09A parallel interface supports two modes: a PS/2 style bi-directional parallel port and an expansion parallel port (EPP). An example circuit for the bi-directional parallel port is shown in Sheet 5, "Video, Keyboard/Mouse, and Parallel Interfaces" in Section 13.2.1.2, "Reference Circuit Diagrams."

5.1. Design Notes

Note the following three points when considering the design.

- All signal lines should have pull-up resistors to V_{CC} (3.3V) or 5V.
- Since the direction control signal (DIR) is not supported, it is not possible to insert buffers in the data lines (LPTD[0..7]). The circuit pattern should be designed to optimize the connections.
- In EPP mode, the WAIT# signal active interval should not exceed 15 µs.

5.2. EPP Mode

A Parallel Port Control Register setting can be used to switch to expansion parallel mode (EPP mode). For details, see Section 5.10, "Parallel Port Interface" in the "CARD-E09A Hardware Manual."
In EPP mode, the parallel interface pin functions change as follows.

Table 5-1 Pin functions in EPP mode

Standard mode	EPP mode	IN/OUT	Function
STROBE#	WRITE#	OUT	Write cycle signal, read cycle when high
AFD#	DSTRB#	OUT	Data strobe signal, shows data read/write being executed
BUSY	WAIT#	IN	Wait signal, corresponds to IOCHRDY on ISA bus
ACK#	INTR#	IN	Interrupt request signal, for interrupt request from peripheral
ERROR#	←	IN	Same as in standard mode
PE	←	IN	Same as in standard mode
INIT#	RESET#	OUT	Peripheral reset signal, initialization signal to peripherals
SLCTIN#	ADSTRB#	OUT	Address strobe signal, shows address read/write being executed
SLCT	←	IN	Same as in standard mode
LPTD[0..7]	←	IN/OUT	Bi-directional address/data signals

If the WAIT# signal is held low for 15 µs or more, the CARD-E09A internal SDRAM and expansion memory on the ISA bus will no longer be able to be refreshed, and the contents of memory may be lost. To avoid this, the WAIT# active time must be designed not to exceed 15 µs.

5.3. Current Flows

Parallel port I/O is achieved using CMOS devices, and therefore depending on the manner of use, problems may arise from current flows.

Table 5-2 Current flows in the parallel port

Problem	CARD-E09A power	Device power
1. No problem	ON	ON
2. Current flows in CARD-E09A parallel port	OFF	ON
3. Current flows from CARD-E09A to device	ON	OFF
4. No problem	OFF	OFF

As shown in Table 5-2, the current flows occur between the CARD-E09A and the external connected device when one is powered on and the other is powered off. This can cause an excess current to flow in a CMOS device input or output in the forward direction of an input protective diode or parasitic diode, causing the CMOS device to latch up, and in the worst case resulting in damage. For example, when a device (printer, for example) is powered on and is connected to the CARD-E09A which is powered off, then immediately after power is supplied to the CARD-E09A, a current may flow which is easily large enough to make the device latch up. Avoid use in such a way as to cause the states 2 and 3 in Table 5-2.

6. Keyboard and Mouse Interface

The CARD-E09A is equipped with a PS/2 style keyboard and mouse interface. For an example circuit, see Sheet 5 "Video, Keyboard/Mouse, Parallel Interface" in Section 13.2.1.2, "Reference Circuit Diagrams."

6.1. Design Notes

Note the following three points when considering the design.

- KBCLK, KBDATA, MSCLK, and MSDATA are open drain output bi-directional signals. Provide pull-up resistors external to the CARD-E09A. A keyboard/mouse is normally specified to operation on 5V, so a 5V pull-up is required. (If the keyboard/mouse is specified for 3.3V operation, a 3.3V pull-up may be used. The absolute maximum rating for these pins of the CARD-E09A is 7.5V.)

- To prevent "hot plugging" or other misoperations from causing keyboard/mouse damage, it is recommended to put a fuse in the power line of the interface connector.

- When the CARD-E09A keyboard or mouse interface is connected to proprietary hardware, this must comply with the PS/2 style interface specification. See the item "Keyboard/Mouse Timing" in Chapter 8, "AC Characteristics" of the "CARD-E09A Hardware Manual."

6.2. Interface Connector Pin Layout

In the Reference Circuit Diagrams, one 6-pin PS/2 style interface connector is connected to both keyboard and mouse. In this case, when the keyboard and mouse are used simultaneously, a separate branching connector is required for the keyboard and mouse. Because of the branching connector, it is possible for the keyboard and mouse to be reversed, so care is required.

When using only one of the keyboard and mouse, or when a branching connector is not desirable, the optimum pin layout can be determined with reference to this table.

Table 6-1 Pin layout for keyboard/mouse interface

Pin	Normal PS/2 Keyboard I/F	Normal PS/2 Mouse I/F	Reference circuit diagram I/F
1	KBDATA	MSDATA	MSDATA
2	n.c	n.c	KBDATA
3	GND	GND	GND
4	5V	5V	5V
5	KBCLK	MSCLK	MSCLK
6	n.c	n.c	KBCLK

7. A/D and D/A Conversion

The SH7709A has an 8-channel 10-bit A/D converter (sequential comparison type), and two channels of 8-bit D/A converter built in, but the CARD-E09A interface connector does not include all of these signals. Table 7-1 shows the A/D and D/A converters supported by the CARD-E09A.

Table 7-1 Supported A/D and D/A converters

	Channels	Signal name	Pin number	Assignment in evaluation board
10bit A/D	Analog input 4	AN4	180	Four-wire resistive film touch panel AN4: y-axis data, AN5: x-axis data
	Analog input 5	AN5	182	
8bit D/A	Analog output 0	DA0	184	Speaker
	Analog output 1	DA1	183	Unused

As shown in Table 7-1, six A/D converter channels supported by the SH7709A, that is analog inputs 0 to 3, 6, and 7, are not provided on the CARD-E09A interface, and cannot be used. Analog input 4 (AN4), analog input 5 (AN5), and analog output 0 (DA0) are already used on the evaluation board. The touch panel driver and audio driver provided with the CARD-E09A Windows CE Development Kit are compliant with the specification of the touch panel control circuit and audio (speaker) circuit mounted on the evaluation board. When changing the configuration of the external circuit connected to the AN4 connector, AN5 connector, and DA0 connector, or using them for other purposes, it will be necessary to develop a separate device driver with reference to the "SH3 Hardware Manual."

To prevent damage to the analog input connectors from abnormal voltage such as excess surges, it is necessary to connect a protective circuit as described in Section 5.15, "AD/DA" of the "CARD-E09A Hardware Manual."

For a reference circuit diagram of the touch panel control and audio mounted on the evaluation board, see Sheet 10 "Touch Panel, Audio circuit" of Section 13.2.1.2, "Reference Circuit Diagrams." The following describes the configuration of the touch panel control circuit.

<<Configuration of the touch panel control circuit mounted on the evaluation board>>

1. Description of four-wire resistive film touch panel control circuit supplied on the evaluation board

Fig. 7-1 shows a block diagram, and Table 7-2 shows the relation between PTC4/PINT4, PTC3/PINT3, and PTC2/PINT2 used for switching control of the voltage applied to the x/y-axes and the touch panel status.

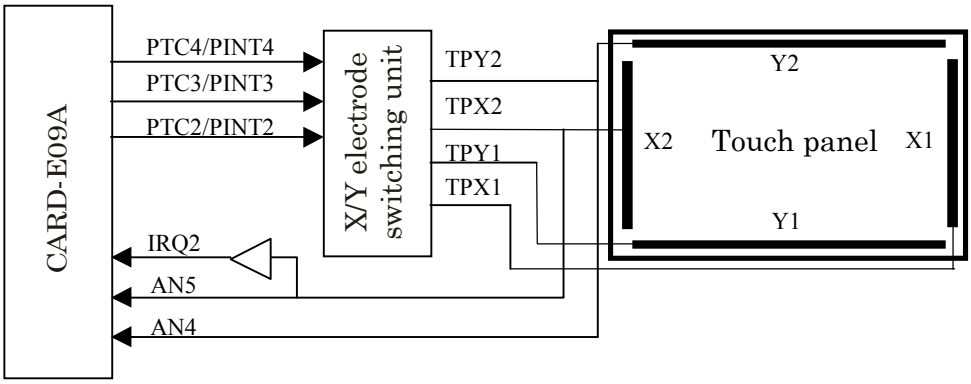


Fig. 7-1 Touch panel control circuit block diagram

Table 7-2 Touch panel status

Status	CARD-E09A signals					
	PTC4 /PINT4 Output value	PTC3 /PINT3 Output value	PTC2 /PINT2 Output value	AN5	AN4	IRQ2
X-axis reading	0	0	0		X-Read	
Y-axis reading	1	1	0	Y-Read		
Awaiting interrupt	1	0	1			Pen-down interrupt generated
Pen up/down detection	1	0	1	Read		

The resistive film touch panel has a uniform resistor film, with film and glass transparent electrodes over the whole effective area, so that a finger or pen (non-metallic) press shorts the upper and lower electrodes, and an analog voltage is detected between them in alternately the x- and y-directions. When detecting along the x-axis, a voltage Vx is obtained from Y electrodes, and when detecting along the y-axis, a voltage Vy is obtained from X electrodes; these voltages are converted to digital values by an A/D converter.

In the evaluation board circuit configuration, PTC4/PINT4, PTC3/PINT3, and PTC2/PINT2 are assigned to the applied x- and y-axis voltage switching, and by means of the combinations shown in Table 7-2, the x-coordinate is read as an analog voltage Vx (input to connector AN5), and the y-coordinate is read as an analog voltage Vy (input to connector AN4). These analog coordinate values are input through the CARD-E09A interface connector to the SH7709A A/D converter, and converted to digital values, after which they are notified to the host. The x-axis or y-axis voltages are not applied continuously: when an interrupt generated by a press on the touch panel (in the evaluation board IRQ2 is used) is recognized by the CARD-E09A, it switches to reading mode.

2. Designing for low current consumption

In the configuration shown in Fig. 7-1, three signals are assigned to switching control of the voltages applied to the x- and y-axes, but in this case, the electrodes cannot all be turned off. Even while waiting for an interrupt, a certain current is flowing. To avoid this situation, four signals must be assigned to switching control of the voltages applied, and TPX1, TPX2, TPY1, and TPY2 switched on and off.

3. Hints on connecting the eight-wire resistive film touch panel

In the evaluation board, a control circuit for a four-wire configuration is provided, but as the LCD panel size increases the touch panel size increases, and reading errors, and malfunctions due to external noise become more common. Generally, to avoid such problems eight-wire resistive film touch panels have become common. In the eight-wire method, close to the four-wire electrodes (X1, X2, Y1, and Y2) are added four more electrodes (X1ref, X2ref, Y1ref, and Y2ref) for the purpose of monitoring the respective voltage values, and are designed so as to output information on the discrepancy between the electrode and input point to the host (A/D converter).
Connecting a touch panel configured in this way requires four A/D converters, for x-coordinate, x-coordinate correction, y-coordinate, and y-coordinate correction, and this is not supported by the channels provided on the CARD-E09A interface. It is necessary to add A/D converters to the ISA bus or SH bus. In this case, a separate device driver for the touch panel must also be developed.

In a configuration in which data correction is not used, two methods of connecting the eight-wire resistive film touch panel to the CARD-E09A can be considered:

(1) The touch panel X1ref, X2ref, Y1ref, and Y2ref electrodes are left open.
(2) The touch panel X1 and X1ref, X2 and X2ref, Y1 and Y1ref, and Y2 and Y2ref electrode are shorted in pairs.

8. Power Management

As low power consumption modes for the CARD-E09A, CPU standby mode and suspend mode are supported. The SH7709A (CPU) itself additionally supports a hardware standby mode and module standby mode, but in the CARD-E09A, the hardware standby mode is not supported. Standard Windows CE does not support module standby mode. When using this mode, separate means such as a device driver will be required.

8.1. CPU standby

When Windows CE HAL has no threads in preparation (no threads to be executed by the kernel), then the SH7709A is put into sleep mode. At this point, the SH7709A stops, but the RAM, SED1355, companion chip, and other device remain in operation mode, and the clock signal output from the CKIO (pin 62) continues. This state is called CPU standby mode. The switch to CPU standby mode and the return from standby mode are both handled by Windows CE.

The return from CPU standby mode occurs when the following events become active and HAL recognizes a thread in preparation.

- NMI
- IRQ0: interrupt from CARD-E09A companion chip
  See Section 5.4.1, "IRQ0" of the "CARD-E09A Hardware Manual."
- IRQ1 to IRQ4
  In the evaluation board, IRQ1 is used for LAN, and IRQ2 for the touch panel
- RTC Alarm
  See Section 8.2.1.

When using an OS other than Windows CE, a step is required to put the SH7709A in sleep mode. For details, see the "CARD-E09A Hardware Manual" and "SH3 Hardware Manual."

8.2. Suspend Mode

When Windows CE HAL detects an active input on the CARD-E09A SRBTN# (pin 192), it puts the CARD-E09A into suspend mode. In the suspend mode, the CARD-E09A is in the state shown in Table 8-1. For details, see Section 5.8, "Power Management" of the "CARD-E09A Hardware Manual."

Table 8-1 State in suspend mode

CPU	SH7709A	CPU STANDBY Mode
	SDRAM	Self Refresh Mode
I/O	Companion Chip	STANDBY Mode
	CompactFlash card	Operation
	PCMCIA Slot	Power Save Mode
Video	SED1355	Hardware SUSPEND Mode
	EDO RAM	Self Refresh Mode
	CRT I/F	OFF
	LCD I/F	OFF

Since the switch to CARD-E09A suspend mode and the return from suspend mode (resume) is all handled by Windows CE, the user is not required to carry out any procedure on the SH7709A or companion chip register settings.
However, when an OS other than Windows CE is used, a procedure for suspending and resuming is required, as described in Section 5.8.5, "Suspend/Resume" of the "CARD-E09A Hardware Manual."

8.2.1. Suspend/Resume Trigger Conditions

The trigger conditions for switching to suspend mode and for resuming from suspend mode are shown in Table 8-2.

Table 8-2 Suspend/resume trigger conditions

Trigger	Note
SRBTN#	Suspend and resume trigger. CARD-E09A, pin 192. Suspend and resume request signal to CARD-E09A. Not edge sensing: recognizes a low pulse.
FrzDri	Suspend trigger. Software can switch to suspend mode by calling FriDri.DLL supplied in the "CARD-E09A Windows CE Development Kit." For details, see the "Windows CE Development Kit Instruction Manual."
RTC alarm	Resume trigger. A resume time can be set in advance, using ALARM.EXE supplied in the "CARD-E09A Windows CE Development Kit." For details, see the "Windows CE Development Kit Instruction Manual."
NMI	Resume trigger. CARD-E09A, pin 207. A resume can be achieved by connecting a trigger circuit to the CARD-E09A NMI pin.

8.2.1.1. Suspend Resume Button (SRBTN#)

By connecting an external request circuit to the SRBTN# pin, a switch to suspend mode, and resume from suspend mode are possible. There are two ways, as follows, of carrying out a suspend/resume using the SRBTN# pin:

1. Connecting a button switch to the SRBTN# pin for manual switching

An example circuit is shown in Sheet 12, "Switches" in Section 13.2.1.2, "Reference Circuit Diagrams." The CARD-E09A internally has no chattering prevention circuit provided for the SRBTN# pin, and therefore as in the reference circuit diagram an external chattering prevention circuit for the button switch should be considered.

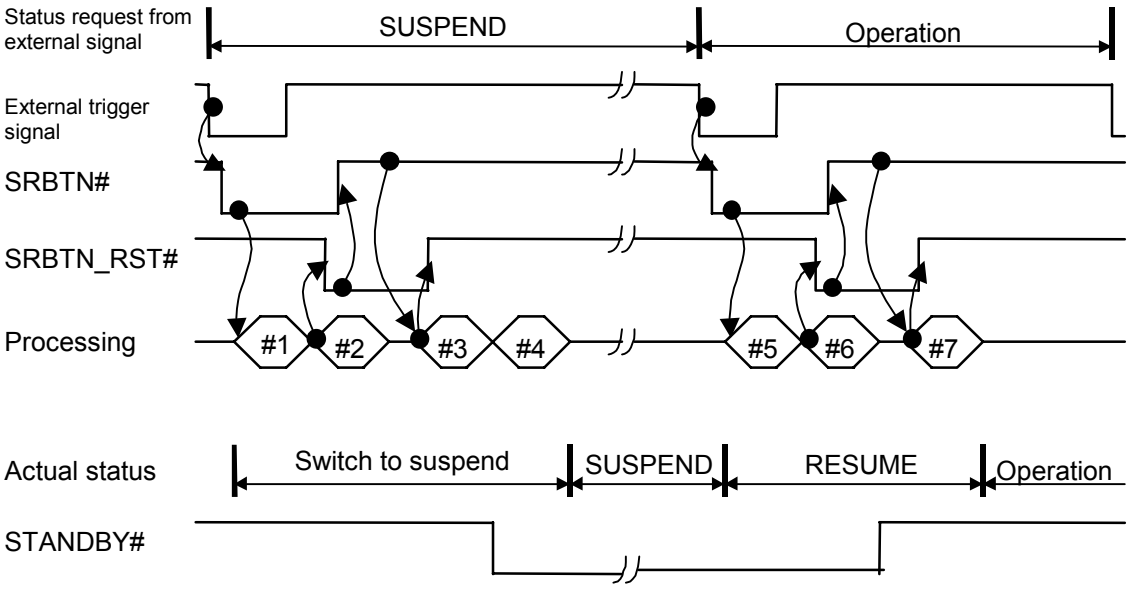
For the button switch mechanism, if the design is such that it is left pressed for the duration of the suspend, then this requires STARTUP.DAT settings and an external circuit the same as in "System 1" in the next method (2. "Connecting a suspend/resume trigger circuit to the SRBTN# pin").

2. Connecting a suspend/resume trigger circuit to the SRBTN# pin

This is the method of connecting an external trigger circuit to the SRBTN# connector.
Since the SRBTN# signal pin does not carry out edge sensing, but recognizes a low level pulse, when making a suspend request, if SRBTN# pin is hold to low, then the resume in the next step will not be possible. The input level must be switched High => Low => High. Again, if the SRBTN# pulse is extremely short, the interrupt handler (Windows CE HAL) may not catch the suspend or resume request.
To avoid these problems, the signal provided is SRBTN_RST# (suspend response logic control flag: on the CARD-E09A interface connector, any one of PTC[7:5], pins 194 to 196 can be assigned by a setting in STARTUP.DAT). After the interrupt handler has accepted a suspend or resume request, SRBTN_RTS# indicates that the SRBTN# pin can be returned high. In the STARTUP.DAT settings, there are two settings which can be made: "System 1," in which after it has been confirmed that the SRBTN# pin level has gone from low to high the next step is operated to, and "System 2," in which the next step is operated to without confirming the SRBTN# pin level. For the method of making STARTUP.DAT settings, see Section 8.2.1.2, "PTC Assignment and STARTUP.DAT Settings."

"System 1"

Fig. 8-1 shows an overview of the sequence. As shown in the figure, the external trigger signal must be driven by a pulse when there is a suspend or resume request. The switch to status #3 and #7 occurs after it has been checked that the SRBTN# pin has changed from low to high.



<<STATUS>>

#1: Interrupt processing
#2: Companion Chip standby processing and SED1355 suspend processing
#3: SH7709A CPU standby processing
#4: Suspend ROM execution (IPL)
#5: Resume ROM execution (IPL)
#6: SH7709A resume
#7: Companion Chip, SED1355 resume

Fig. 8-1 Overview of "System 1" sequence

An example circuit is shown in Fig. 8-2 of a "System 1" external trigger. SRBTN# can be generated from RESETP#, SRBTN_RST#, and the external trigger signal.

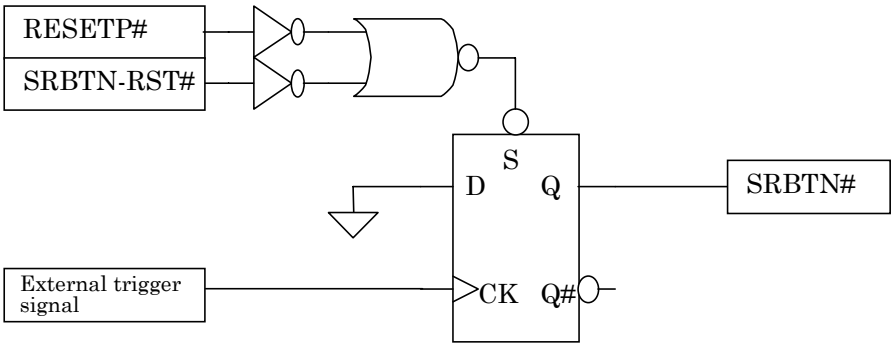
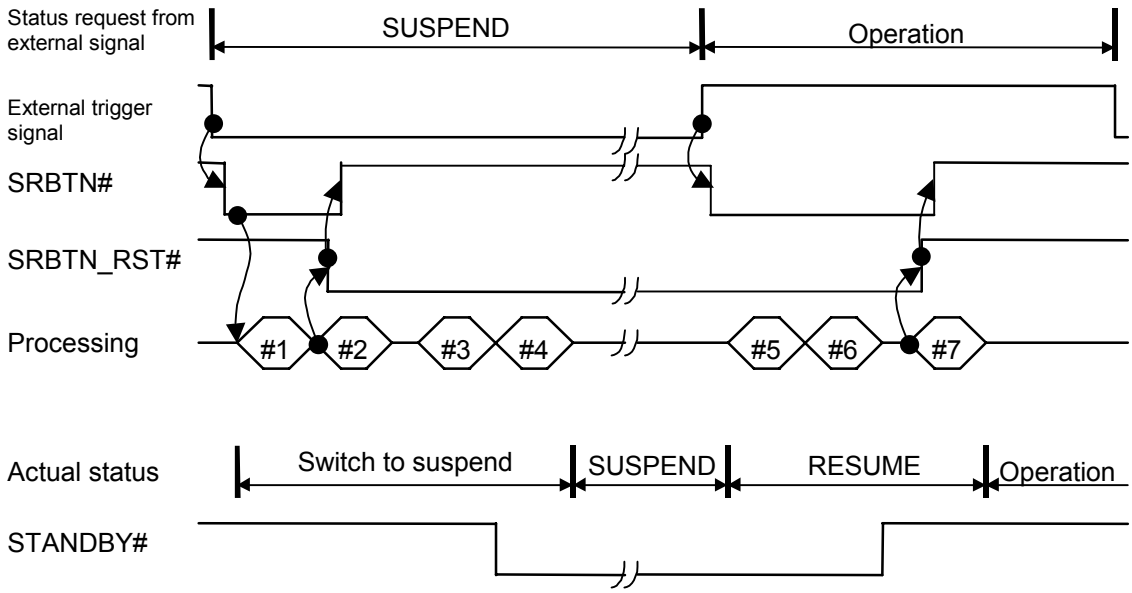


Fig. 8-2 Example "System 1" external trigger circuit

"System 2"

Fig. 8-3 shows an overview of the sequence. As shown in the figure, the external trigger signal must be driven low when there is a suspend request, and high when in operation.
As in "System 1," before the change of status to #3 and #7, no check is made that the SRBTN# pin has gone from low to high. Therefore, if the low level input to the SRBTN# pin continues, the suspend/resume operation will be repeated, and thus care is required.



<<STATUS>>

#1: Interrupt processing
#2: Companion Chip standby processing and SED1355 suspend processing
#3: SH7709A CPU standby processing
#4: Suspend ROM execution (IPL)
#5: Resume ROM execution (IPL)
#6: SH7709A resume
#7: Companion Chip, SED1355 resume

Fig. 8-3 Overview of "System 2" sequence

An example circuit is shown in Fig. 8-4 of the "System 2" external trigger. SRBTN# can be generated from the external trigger signal, SRBTN_RST#, and RESETP#.

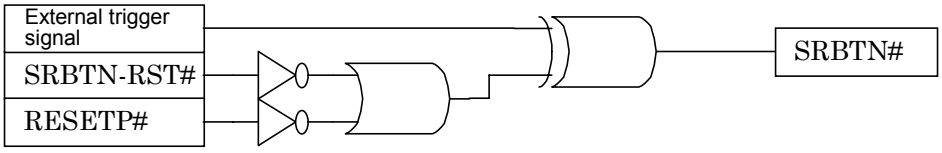


Fig. 8-4 Example "System 2" external trigger circuit

8.2.1.2. PTC Assignment and STARTUP.DAT Settings

The PTC pins are the Port C register internal to the SH7709A, made available on the CARD-E09A interface connector. As described in the previous section, it is assigned to power management related signals. Table 8-3 shows the PTC assignment table.

Table 8-3 PTC assignment table

Signal name	Pin.No.	Assignment
PTC7/PINT7	194	By means of STARTUP.DAT settings, any one pin can have the suspend response logic control flag (SRBTN_RST#) assigned. The other two signals are reserved.
PTC6/PINT6	195	
PTC5/PINT5	196	
PTC4/PINT4	198	Assigned to the four-wire resistor film touch panel signals in the evaluation board (see the reference circuit diagram).
PTC3/PINT3	199	
PTC2/PINT2	200	
PTC1/PINT1	201	Reserved.
SRBTN# (PTC0/PINT0)	192	Assigned to SRBTN# pin.

To execute suspend/resume control, the SRBTN_RST# signal assignment, "System 1"/"System 2" selection, and RTC alarm setting must be made on the key "suspend" of STARTUP.DAT. Table 8-4 shows the setting format for the key "suspend." Read this in combination with Section 13.9, "Suspend/Resume Control Data" in the "CARD-E09A Windows CE Development Kit Instruction Manual."

In a system with an LCD panel connected, apart from the below, the delay time for switching to suspend mode or resuming must be specified on the key "1355PROPERTY". For details, see Table 2-16 in Chapter 2, "Video Interface." Read this also in combination with Section 8.2.2, "LCD Panel Power On/Off Sequence."

Table 8-4 Setting format for STARTUP.DAT key "suspend"

Column	Comment
RTC Alarm, SRBTN# method selection	<RTC Alarm setting> Bit0 ; "1" = RTC Alarm Enable, "0" = RTC Alarm Disable <SRBTN# method selection> Bit 1 = 1: "System 2"; bit 1 = 0: = "System 1"
SRBTN_RST# pin selection	Bits 7 to 5: PTC7 to PTC5 selection flag ・"80h" = PTC7, "40h" = PTC6, "20h" = PTC5, "00h" = Disable ・Other settings are prohibited.

8.2.2. LCD Panel Power On/Off Sequence

The LCD panel power on/off sequence is described in Chapter 2, this section describes it from the point of view of suspend/resume. Fig. 8-5 shows the LCD panel suspend/resume sequence. Check this against the power sequence of Fig. 2-1 in Chapter 2.

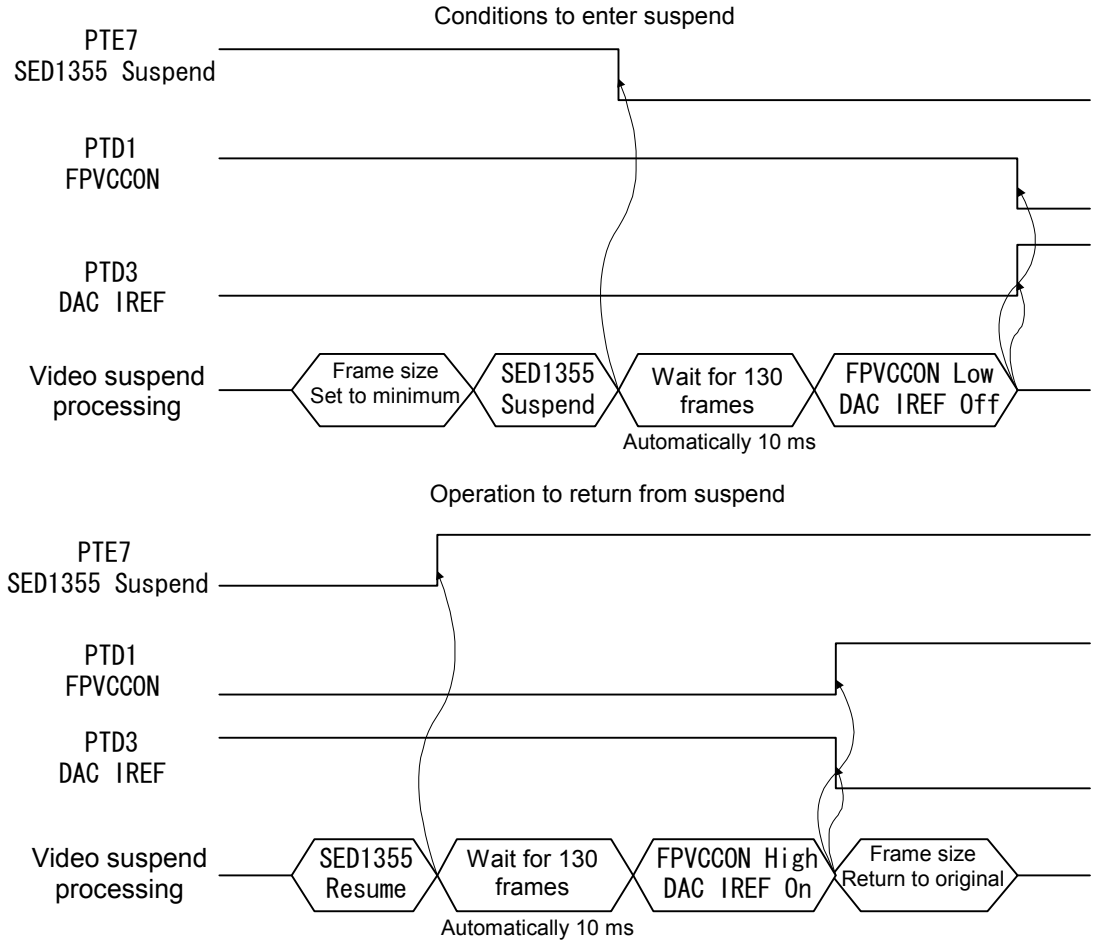


Fig. 8-5 LCD panel suspend/resume sequence

In the figure above, PTE7, PTD1, and PDT3 respectively indicate the SH7709A Port E register Bit 7, Port D register Bit 1, and Bit 3. These signals are not connected to the interface connector internally.

At the time of a suspend, the SED1355 is set to the hardware suspend mode. PTE7 in Fig. 8-5 is connected to the SED1355 SUSPEND# pin. When there is a low input to the SUSPEND# pin, all signal lines of the LCD panel go to low output, and after the time defined in STARTUP.DAT, FPVCCON and FPVEEON (LCDPWR of SED1355) are driven low. The LCD panel logic power and device power are turned off using these power control signals.

Normally, when the SED1355 switches to the hardware suspend mode, the LINE and FRAME signals go to inactive level output, based on the polarity setting of REG[06h], REG[07h]. Supposing that the inactive state is high, then after the LCD panel logic power goes off, this means that a high level signal is input to the LCD panel. In this case, a large current flows from the LINE and FRAME signal lines to the LCD panel, and in the worst case the LCD panel could be damaged. To avoid such problems in the CARD-E09A, the CARD-E09A Windows CE video driver is set to a low output, regardless of the settings of REG[06h], REG[07h]. In a resume, the suspend transition procedure is reversed.

However, when the CARD-E09A is running an OS other than Windows CE, in the suspend mode, care must be taken to ensure that measures are in place to ensure that LINE and FRAME are not driven high. For details, see Section 15, "Power Save Mode" of the "SED1355F0A Technical Manual." Fig. 8-6 shows an example of an external circuit in which LINE and FRAME are masked. In the figure, "FPVCCON controlled "LCD Logic VCC"" is the LCD panel logic power after control by the FPVCCON power on/off circuit.

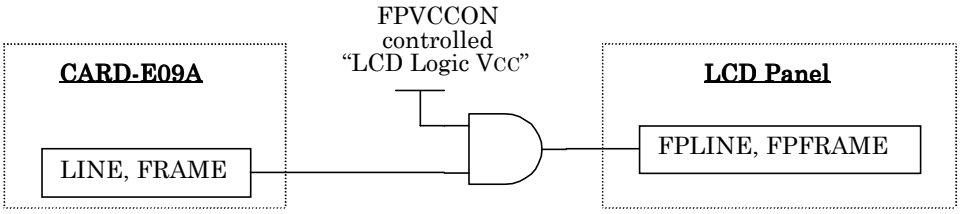


Fig. 8-6 LINE and FRAME masking circuit

8.2.3. PCMCIA Socket Power On/Off Sequence

In suspend mode, the PCMCIA slot goes into power save mode, and the interface output signals all go high impedance. At this time, the Slot A and Slot B slot power control signal outputs are fixed at the level below, and therefore using these signals the slot power (VCC, VPP) can be turned off.

AVPPPGM = "Low", AVPPVCC = "Low", AVCC5# = "High", AVCC3# = "High"
BVPPPGM = "Low", BVPPVCC = "Low", BVCC5# = "High", BVCC3# = "High"

At this point, with the PC card still inserted in the slot, a current will flow in the card detect signals (ACD1#, ACD2#, BCD1#, BCD2#). This is because the card detect signals are input pins with 100 KΩ pull-up resistors. On the other hand, the compact flash card directly inserted on the CARD-E09A cannot have the slot power turned off in suspend mode. "hot plugging" is not provided for, and therefore the interface has no card detect signal.
A PCMCIA slot circuit example is shown in Sheet 6, "PCMCIA Interface" and Sheet 7 "Buffer circuit for PCMCIA Interface," Section 13.2.1.2, "Reference Circuit Diagrams." For details of the slot power on/off sequence, see Section 5.12.6, "Slot Power-On/Off Timing" in the "CARD-E09A Hardware Manual."

8.2.4. Notes on Pin Termination

Refer to Chapter 11, "Pin Termination," Tables 11-1 and 11-2, for a description of the pin state during a suspend. According to the pin state and the CARD-E09A external pin termination, the current consumption of the CARD-E09A may increase. Note the following points, in order to avoid an increase in the current consumption.

- When a pin which the CARD-E09A drives low has a pull-up resistor, a current flows in the resistor, and the current consumption increases. Note that although pins PTC7/PINT7 to PTC1/PINT1 have pull-up resistors in the CARD-E09A itself, depending on the settings they may be driven low, however when the CARD-E09A itself is driving low these pull-up resistors are disconnected so that no current flows in the pull-up resistors.

- If a pin driven high by the CARD-E09A has a pull-down resistor connected, then a current flows in the resistor, and the current consumption increases.

- When a low input is applied to a pin with a pull-up resistor, a current flows in the pull-up resistor, and the current consumption increases.

- When a high input is applied to a pin with a pull-down resistor, a current flows in the pull-down resistor, and the current consumption increases.

- For input pins having no pull-up or pull-down resistor (in the table, pins marked "External" in the Termination item, and RESETP#, RESETM# pins), fix the level. Avoid having inputs floating.

- For output pins having a three-state off, when connected to a CMOS device in the power on state, fix the input to the device with a pull-up or pull-down resistor.

- For devices connected to pins to pins in the following states only, in suspend mode the power can be turned off:
    - Output pin in a three-state off
    - Pin driven low
    - Input pin with a pull-down resistor
    - Input/output pin with a pull-down resistor and being input

  For pins in other states, a current flows in the pull-up or pull-down resistor, or the input is floating, and therefore the device power cannot be turned off. To power off, a buffer is required between the CARD-E09A and the device.

8.3. Other Notes

- It is not possible to restore the system from the suspend mode by using a ring indicator signal (RI3#, RI4#) on serial 3, or serial 4. To resume via a serial interface, the ring indicator signal must be connected to NMI or one of IRQ1 to IRQ4, and an interrupt signal used for the resume.

- The PCMCIA card detect signals (ACD[2:1]#, BCD[2:1]#) are pulled up to V_{CC} (3.3V) internally to the CARD-E09A. If a PC card is left in Slot A or Slot B, note that a current flows between V_{CC} internal to the CARD-E09 and the PC card ground. In a suspend, it is recommended to remove the PC card.

- The CARD-E09A has no battery monitoring signal. In a battery-driven system, if a mechanism to notify the remaining battery capacity is required, or it is desired to selectively power external devices on and off, then unused pins can be used for PTC7/PINT7 to PTC1/PINT1. However, application software or a device driver or similar is required to directly set SH7709A Port C register.

- Pins PTC4/PINT4 to PTC2/PINT2 are assigned to power control of the four-wire resistive film touch panel mounted on the evaluation board. Therefore, in suspend mode, in accordance with the evaluation board touch panel control circuit standby specification, the following levels are output.

  PTC4/PINT4 = high, PTC3/PINT3 = low, PTC2/PINT2 = high

  If the touch panel control circuit is changed, or if other circuits are connected to the pins, in accordance with the changed circuit specification, control of the relevant bits of the SH7709A Port C register must be modified. If a pull-up or pull-down resistor is connected without modifying the control of the Port C register, a current may flow in the external circuit and thus care is required. Check Section 8.2.4, "Notes on Pin Termination."

9. Power Supply

9.1. RTC Backup

In addition to the SH7709A internal RTC (Real Time Clock), the CARD-E09A incorporates an external RTC (Epson RTC-4543). This is because the SH7709A internal RTC is not backed up when the system power is off. The external RTC has a backup function.

The internal RTC and external RTC are synchronized as follows. For details, see the "CARD-E09A Windows CE Development Kit Instruction Manual."

1) When the system power is turned on, the Windows CE loader (NKLOADS.BIN) copies the time from the external RTC to the internal RTC.
2) In operation, when the RTC is set, the Windows CE driver sets the time in both the internal RTC and the external RTC.
3) When the system power is turned off, the Windows CE loader (NKLOADS.BIN) copies the internal RTC time to the external RTC.

Note that if a development environment other than the Epson "CARD-E09A Windows CE Development Kit" is used, the above procedures must be provided by separate software.

V_{BK} (166pin) is a power pin for backup of External RTC. When power (V_{CC}) is supplied to CARD-E09A, the same power as V_{CC5} is supplied to the V_{BK} pin; when power is not supplied to CARD-E09A, power is supplied from the backup power (lithium battery, etc.). If no RTC backup is required, supply the same power to the V_{BK} pin as the CARD-E09A V_{CC}.

An example backup circuit is shown in Sheet 11 "DC Power regulator, Reset circuit" in Section 13.2.1.2, "Reference Circuit Diagrams." The current consumption of the backup power is shown in Section 7.3, "Consumed Current" of the "CARD-E09A Hardware Manual." The backup current (IV_{BK}) during backup is 1 μA Typ. / 3 μA Max., and during a read/write of the RTC is 30 μA Max. The capacity of the backup battery should be calculated to take this into account.

9.2. Reset Circuit

The SH7709A supports two reset signal inputs: RESETP# and RESETM#. In the CARD-E09A these two are both available on the interface connector. RESETP# is a normal power on reset (inverse of the Power Good signal), and initializes all I/O ports and memory devices. RESETM# is a manual reset, and initializes everything except the data stored in SDRAM. The initialization routines are different, and therefore RESETP# and RESETM# cannot be made active simultaneously.

1. RESETP# signal
This is a power on reset signal. When the power is turned on, input the RESETP# signal with the timing shown in Fig. 9-2. This can also be used as a hardware reset signal.

2. RESETM# signal
This initializes the CARD-E09A, but does not affect main memory (SDRAM). When the RESETM# signal is input, the system is rebooted while preserving the contents of main memory.

A reference circuit diagram for RESETP# is shown in Sheet 11 "DC Power Regulator, Reset circuit" in Section 13.2.1.2, "Reference Circuit Diagrams" and a reference circuit diagram for RESETM# is shown in Sheet 12 "Switches." Since the RESETP# reference circuit diagram is based on the evaluation board, for convenience it is generated from the evaluation board input voltage of 5V. However, in practice, it must be generated monitoring the level of the CARD-E09A input voltages of V_{CC} (3.3V) and V_{CORE} (1.9V). Fig. 9-1 shows an example circuit for RESETP#.

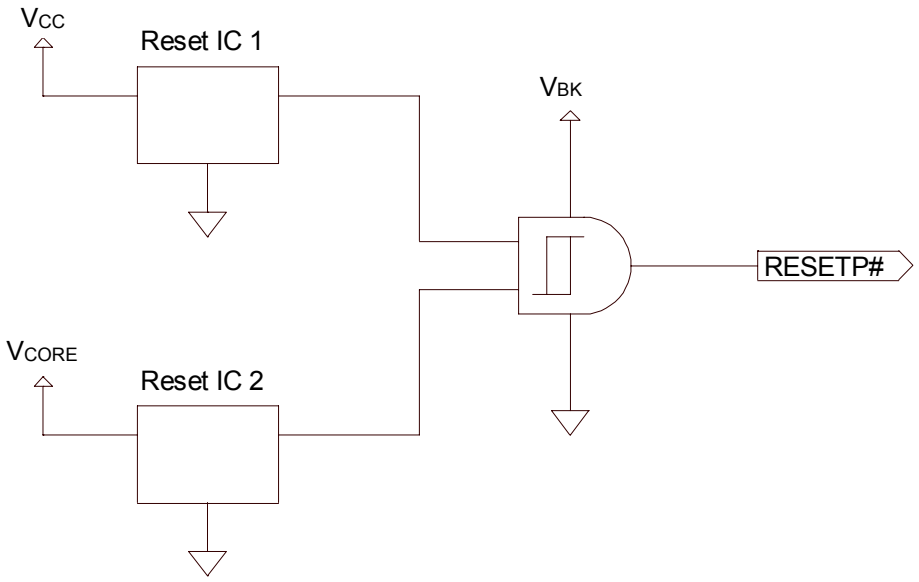


Fig. 9-1 Example circuit for RESETP#

9.3. Power and POWERGOOD

In figure 9-2, the diagram indicates the VCC/VCORE/RESTEP# sequence when the power is ON/OFF. Make sure VCC≧VCORE is always true.
When the power is on, if CARD-E09A is not reset, then it cannot start to function normally. Therefore, POWERGOOD needs to be input according to the timing indicated in the figure 9-2.
In a system with a lithium battery or similar connected to the VBK connector as an RTC backup, if the RESETP# signal goes high before VCC has reached at least 3.0V, then the RTC data may be lost. Ensure that until VCC is at least 3.0V the RESETP# signal does not exceed 0.5V.

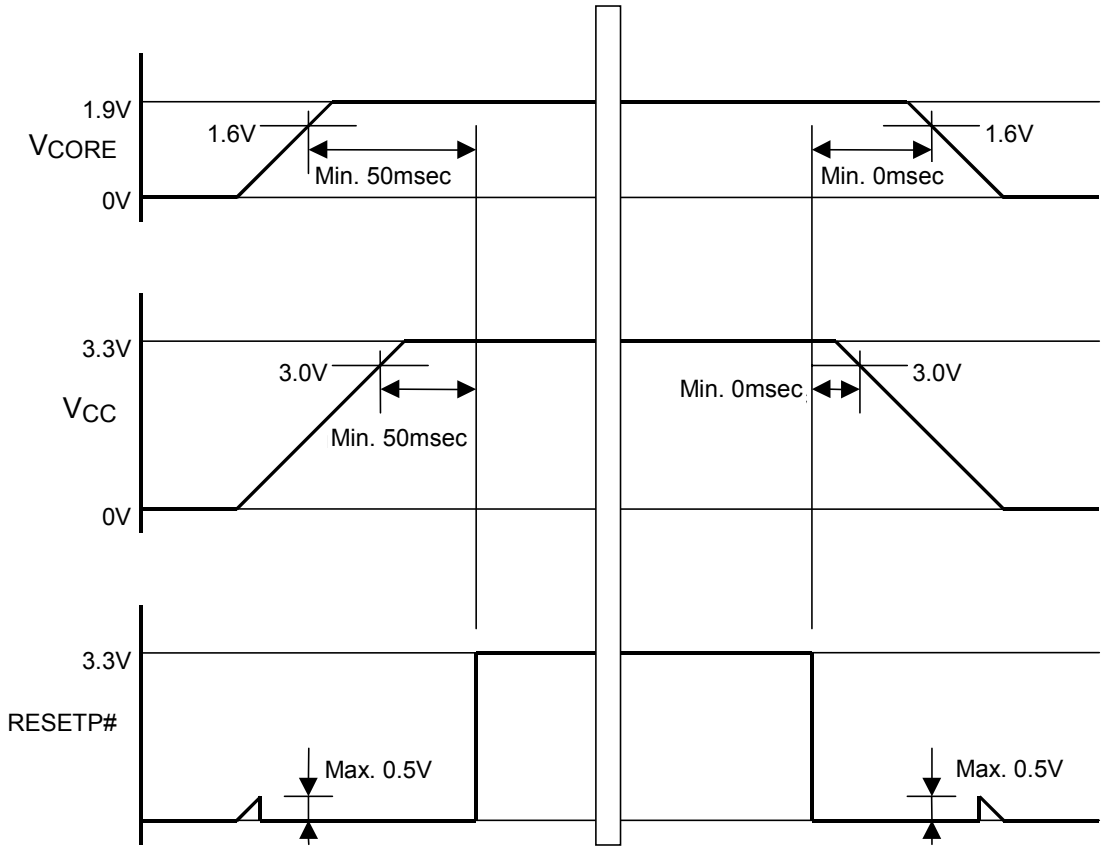


Fig. 9-2 Power on/off sequence

9.4. PWOFF# Signal

This is a power off enable signal from the CARD-E09A. When Windows CE has completed shut-down processing, the PWOFF# signal goes active low. By using this in combination with the power switch, the power can be turned off automatically when Windows CE shuts down. Fig. 9-3 shows a reference example of a circuit for powering off with PWOFF#. For more details, see the "CARD-E09A Windows CE Development Kit Instruction Manual." When used in a development environment other than the "CARD-E09A Windows CE Development Kit," note that original software must be created for this purpose.

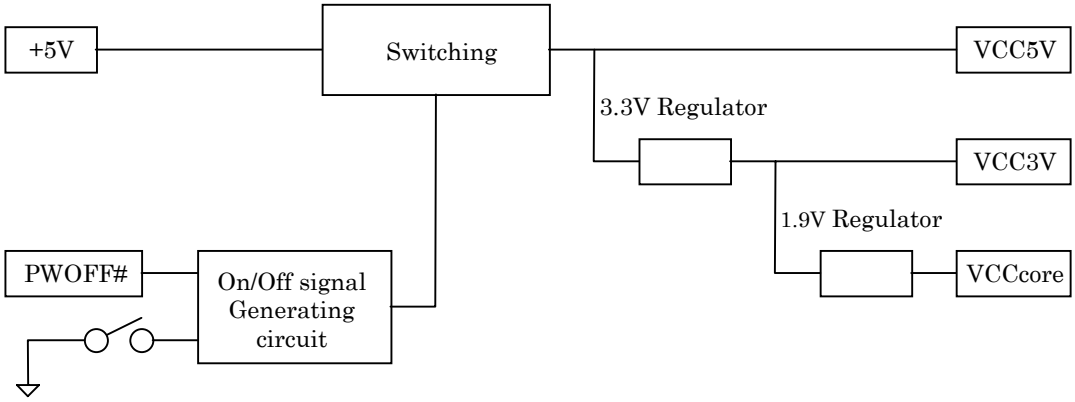


Fig. 9-3 Reference example of circuit for powering off with PWOFF#

10. Matters to be Noted in Use of CARD-E09A

10.1. Power Supply and Grounding

10.1.1. Power Connection

The CARD-E09A has a power management function, and therefore the current consumption may vary depending on the CPU operation mode. To ensure stable CARD-E09A operation and display quality, try as much as possible to use low impedance when connecting CARD-E09A power pin (V_{CC}/V_{CORE}) and ground pin to the power circuitry.
When selecting power circuitry, use electric capacity appropriate to the application and make sure instant power supply can be secured. Also, precaution should be take to handle noise problem and reduce high frequency noise or low frequency noise.

10.1.2. Power Line Wiring

When handling power line wiring and ground wiring external to CARD-E09A, try as much as possible to use power plane / ground plane and lower the wiring inductance. If plane connection is really not possible, try to use as thick as possible cabling and pay detailed attention to reducing noise.

10.2. Matters to be Noted in Designing of Printed Circuit Board

(1) The CARD-E09A CKIO signal operates at the high frequency of 33 MHz, and therefore basic circuit patterns must be made as short as possible so that there are no delays. The CKIO signal is also used internally to the CARD-E09A, so if there is noise interference on the circuit board this may adversely affect the overall system operation.

(2) If the CARD-E09A address and data bus have many cablings, and they change simultaneously, the signal's energy will become more and when the cabling coil around and around this may affect other signals. Therefore, it is necessary to usually insert dumping resistance at the address and data bus to smooth off the wave form, or increase the distance from other signals.

(3) For reset, clock and other control line, bus noise may heavily overlap due to cross talk, etc. If there is fear of noise overlapping, the following remedies, for example, can be tried.

   1) For signal such as clock whose delay would cause system problem, the guard pattern etc. can be used to reduce influence from other signals, or the distance from other signals can be increased.
   2) For signals such as reset signal which has margin in timing, integrated circuit etc. can be used to remove the noise.

(4) Usually, CMOS output buffer has output impedance ranging from several to tens of ohms. However, cables on the printed board has impedance over 100 ohms and so the output buffer and the cable do not match in impedance. As a result, depending on the shape of the board's pattern, influence from reflection, etc. may occur to cause distortion in the wave form. Therefore, it is necessary to check each wave form and, if necessary, add dumping resistance or terminator resistance to correct the problem.

(5) Do not locate a linear regulator or other component emitting large amounts of heat within 20 mm of around the CARD-E09A (component or solder surface). Fig. 10-1 shows the zone of the motherboard on which the CARD-E09A is mounted in which heat-emitting component mounting is prohibited.

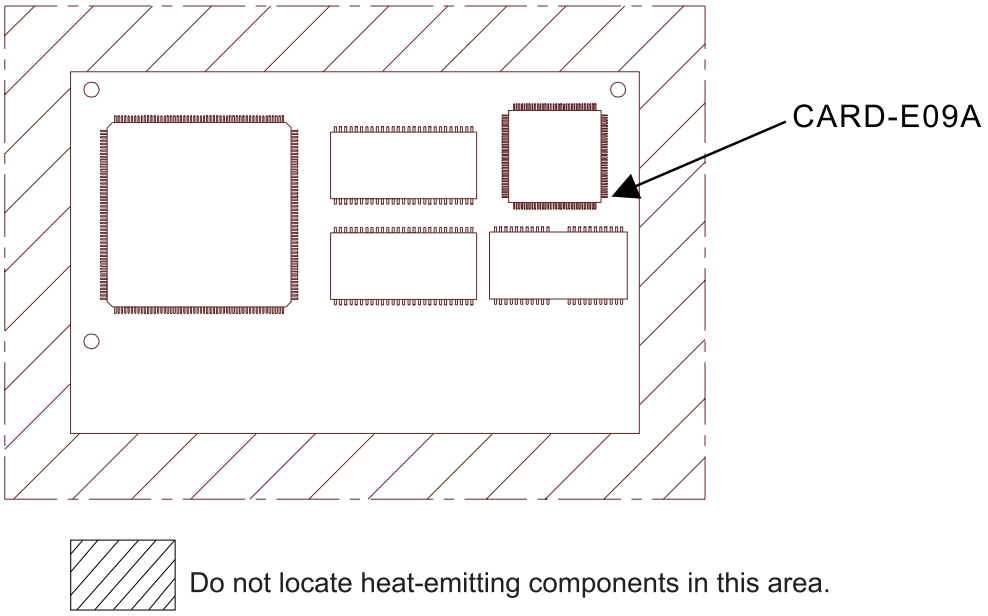


Fig. 10-1 Component restriction area for motherboard

10.3. EMC and Static Noise Solution

The CARD-E09A is not in a case, and its CPU clock is also very high speed, when designing the motherboard circuitry, artwork, and system casing, be sure to take these factors into consideration to handle the EMC and static noise problems.

10.4. Accuracy of RTC

In the CARD-E09A, there are two real-time clocks, the SH7709A internal RTC and the external backed up RTC (Epson RTC-4543). The accuracy of each of these is as follows.

1) RTC accuracy when CARD-E09A in operation
   +50 to -110 ppm (+4.3 to -9.5 sec/day)
2) RTC accuracy when CARD-E09A in backup state
   -140 ppm (+3.5 to -12.1 sec/day)

The precision of RTC is determined by the vibration frequency of the quartz for the RTC. At room temperature, the vibration frequency of the quartz has Tolerance, and the vibration frequency varies according to change in temperature. The frequency Tolerance at room temperature is roughly ±50ppm. The relationship between the temperature and the frequency can be shown in a secondary curve as described Fig. 10-2. The frequency error is least when the temperature is around 25ºC, and if the temperature fluctuates the frequency error increases.
When the temperature reaches the maximum limit of the operating temperature (Ta) of CARD-E09A, the frequency is approximately 45 ppm lower than at room temperature. Also, at close to 0ºC, the frequency is approximately 25 ppm lower than at room temperature. In conclusion, the RTC's precision is by and large about roughly +50 to -110 ppm.

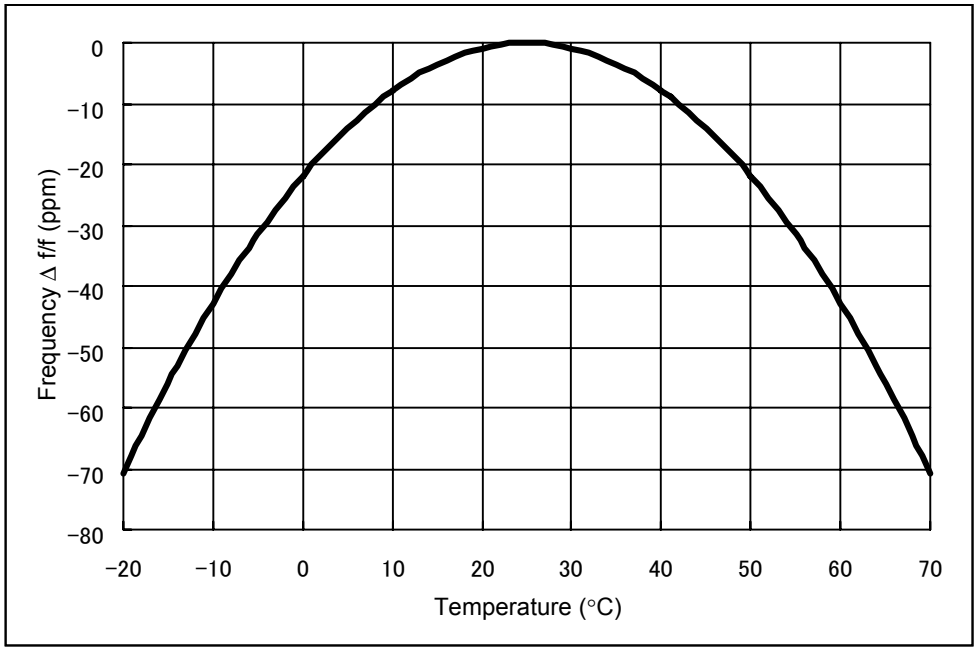


Fig. 10-2 Relation between temperature and wavelength

11. Pin Termination

The following tables indicate characteristics of the pins and how pins are handled when they are not used.

Table 11-1 Name and Meaning of Symbols

Type	Indicates the type of pin. I : Input O : Output Tri : 3-state output I/O : Bi-directional I/OD : Bi-directional, open drain output POWER : Power source
Termination	Indicates the internal terminal resistance. HOLD : Has bus holder xxPU : Pulled up at xxΩ resistance xxPD : Pulled down at xxΩ resistance External : Pull-up resistance external to CARD-E09A is required.
Drive	Indicates the pin drive capacity of the output and the bi-directional pin.
Reset Suspend	This shows pin states during reset and suspend. Input : Is input. High or low input is applied from outside the CARD-E09A, and the input level must be definitive. However, if the CARD-E09A internally has a bus holder or pull-up resistor confirmation is not required. Hi-Z : Is input, but the input level need not be definitive. Input (High) : High level must be input. Input (Low) : Low level must be input. High : Outputs high level. Low : Outputs low level. Drive : Outputs high or low level. Z : Is high-impedance. Of : Turn the PCMCIA interface power off.
Termination of unused pins	Indicates how the pin will be handled when its functions are not used. For pins where input level must be confirmed upfront, handling external to CARD-E09A is required. n.c : Left open Pull-up (V_{CC}) : Add a pull-up resistor to V_{CC} (3.3V) or 5V. Pull-up(5) : Add a pull-up resistor to 5V.

Table 11-2 Connectors

Pin	Name	Type	Termination	Drive (3.3V/5V) I_{OL}, I_{OH} (mA)	Reset	Suspend	Termination of unused pins
1	GND	Power	-	-	-	-	-
2	BCD1#	I	100KPU	-	Input	Input	n.c
3	BCE1#	Tri	-	2/3,-2/-3	Z	Z	n.c
4	BCE2#	Tri	-	2/3,-2/-3	Z	Z	n.c
5	BOE#	Tri	-	2/3,-2/-3	Z	Z	n.c
6	SLOT_B_V_{CC}	Power	-	-	Off	Off	V_{CC} (*5)
7	BVS1	I	100KPU	-	Input	Input	n.c
8	BIORD#	Tri	-	2/3,-2/-3	Z	Z	n.c
9	BIOWR#	Tri	-	2/3,-2/-3	Z	Z	n.c
10	BWE#	Tri	-	2/3,-2/-3	Z	Z	n.c
11	BRDY_IRQ#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
12	BVS2	I	100KPU	-	Input	Input	n.c
13	BRESET	Tri	-	2/3,-2/-3	Z	Z	n.c
14	BWAIT#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
15	V_{CC}	Power	-	-	-	-	-
16	BREG#	Tri	-	2/3,-2/-3	Z	Z	n.c
17	BBVD2_SPKR	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
18	BBVD1_STSCHG#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
19	BWP_IOIS16#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
20	GND	Power	-	-	-	-	-
21	BCD2#	I	100KPU	-	Input	Input	n.c
22	BADRENA#	O	-	2,-2	High	High	n.c
23	BDATAENA#	O	-	2,-2	High	High	n.c
24	BVPPPGM	O	-	6,-6	Low	Low	n.c
25	BVPPVCC	O	-	6,-6	Low	Low	n.c
26	BVCC5#	O	-	6,-6	High	High	n.c
27	BVCC3#	O	-	6,-6	High	High	n.c
28	KBCLK	I/OD	External	12,-	Low	Input(*4)	Pull-up(5)
29	KBDATA	I/OD	External	12,-	Low	Input(*4)	Pull-up(5)
30	MSCLK	I/OD	External	12,-	Low	Input(*4)	Pull-up(5)
31	MSDATA	I/OD	External	12,-	Low	Input(*4)	Pull-up(5)
32	RESETDRV	O	-	6,-6	High	Low	n.c
33	IOCHRDY	I	External	-	Input	Input	Pull-up(V_{CC})
34	IOW#	O	-	6,-6	High	High	n.c
35	IOR#	O	-	6,-6	High	High	n.c
36	MEMCS16#	I	External	-	Input	Input	Pull-up(V_{CC})
37	SBHE#	O	-	6,-6	Drive	Drive	n.c
38	IOCS16#	I	External	-	Input	Input	Pull-up(V_{CC})
39	MEMR#	O	-	6,-6	High	High	n.c
40	MEMW#	O	-	6,-6	High	High	n.c
41	GND	Power	-	-	-	-	-
42	ISADATAENA#	O	-	2,-2	High	High	n.c
43	RI4#	I	50KPU	-	Input	Input	n.c
44	DTR4#	O	-	2,-2	Drive	Drive	n.c
45	V_{CORE}	Power	-	-	-	-	-
46	V_{CORE}	Power	-	-	-	-	-
47	CTS4#	I	50KPU	-	Input	Input	n.c
48	TXD4	O	-	2,-2	High	High	n.c
49	RTS4#	O	-	2,-2	Drive	Drive	n.c
50	RXD4	I	50KPU	-	Input	Input	n.c
51	DSR4#	I	50KPU	-	Input	Input	n.c
52	DCD4#	I	50KPU	-	Input	Input	n.c

Pin	Name	Type	Termination	Drive (3.3V/5V) I_{OL}, I_{OH} (mA)	Reset	Suspend	Termination of unused pins
53	RI3#	I	50KPU	-	Input	Input	n.c
54	DTR3#	O	-	2,-2	Drive	Drive	n.c
55	CTS3#	I	50KPU	-	Input	Input	n.c
56	TXD3	O	-	2,-2	Drive	Drive	n.c
57	RTS3#	O	-	2,-2	Drive	Drive	n.c
58	RXD3	I	50KPU	-	Input	Input	n.c
59	DSR3#	I	50KPU	-	Input	Input	n.c
60	DCD3#	I	50KPU	-	Input	Input	n.c
61	GND	Power	-	-	-	-	-
62	CKIO	O	-	1.6,-0.2	Drive	Drive	n.c
63	TCLK	I	100KPU	-	Input	Input	n.c
64	RESETP#	I	-	-	Input(Low)	Input(High)	Can not be unused. (*6)
65	RESETM#	I	-	-	Input(High)	Input(High)	Pull-up(V_{CC}) (*7)
66	WAIT#	I	4.7KPU	-	Input	Input	n.c
67	CS2#	O	-	1.6,-0.2	High	High	n.c
68	CS0#	O	-	1.6,-0.2	High	High	n.c
69	RD/WR#	O	-	1.6,-0.2	High	High	n.c
70	WE1#	O	-	1.6,-0.2	High	High	n.c
71	WE0#	O	-	1.6,-0.2	High	High	n.c
72	RD#	O	-	1.6,-0.2	High	High	n.c
73	BS#	O	-	1.6,-0.2	High	High	n.c
74	A25	O	HOLD	1.6,-0.2	Z	Low	n.c
75	A24	O	HOLD	1.6,-0.2	Z	Low	n.c
76	A23	O	HOLD	1.6,-0.2	Z	Low	n.c
77	V_{CC}	Power	-	-	-	-	-
78	A22	O	HOLD	1.6,-0.2	Z	Low	n.c
79	A21	O	-	1.6,-0.2	Z	Low	n.c
80	A20	O	-	1.6,-0.2	Z	Low	n.c
81	A19	O	-	1.6,-0.2	Z	Low	n.c
82	GND	Power	-	-	-	-	-
83	A18	O	-	1.6,-0.2	Z	Low	n.c
84	A17	O	-	1.6,-0.2	Z	Low	n.c
85	A16	O	-	1.6,-0.2	Z	Low	n.c
86	A15	O	-	1.6,-0.2	Z	Low	n.c
87	A14	O	-	1.6,-0.2	Z	Low	n.c
88	A13	O	-	1.6,-0.2	Z	Low	n.c
89	A12	O	-	1.6,-0.2	Z	Low	n.c
90	A11	O	Hold	1.6,-0.2	Z	Low	n.c
91	A10	O	Hold	1.6,-0.2	Z	Low	n.c
92	A9	O	Hold	1.6,-0.2	Z	Low	n.c
93	A8	O	Hold	1.6,-0.2	Z	Low	n.c
94	A7	O	Hold	1.6,-0.2	Z	Low	n.c
95	A6	O	Hold	1.6,-0.2	Z	Low	n.c
96	A5	O	Hold	1.6,-0.2	Z	Low	n.c
97	A4	O	Hold	1.6,-0.2	Z	Low	n.c
98	A3	O	Hold	1.6,-0.2	Z	Low	n.c
99	A2	O	Hold	1.6,-0.2	Z	Low	n.c
100	A1	O	Hold	1.6,-0.2	Z	Low	n.c
101	GND	Power	-	-	-	-	-
102	A0	O	Hold	1.6,-0.2	Z	Low	n.c
103	D15	I/O	100KPU	1.6,-0.2	Input	Input	n.c
104	D14	I/O	100KPU	1.6,-0.2	Input	Input	n.c
105	D13	I/O	100KPU	1.6,-0.2	Input	Input	n.c
106	V_{CC}	Power	-	-	-	-	-

Pin	Name	Type	Termination	Drive (3.3V/5V) I_{OL}, I_{OH} (mA)	Reset	Suspend	Termination of unused pins
107	D12	I/O	100KPU	1.6,-0.2	Input	Input	n.c
108	D11	I/O	100KPU	1.6,-0.2	Input	Input	n.c
109	D10	I/O	100KPU	1.6,-0.2	Input	Input	n.c
110	D9	I/O	100KPU	1.6,-0.2	Input	Input	n.c
111	D8	I/O	100KPU	1.6,-0.2	Input	Input	n.c
112	D7	I/O	HOLD	1.6,-0.2	Input	Input	n.c
113	D6	I/O	HOLD	1.6,-0.2	Input	Input	n.c
114	D5	I/O	HOLD	1.6,-0.2	Input	Input	n.c
115	D4	I/O	HOLD	1.6,-0.2	Input	Input	n.c
116	D3	I/O	HOLD	1.6,-0.2	Input	Input	n.c
117	D2	I/O	HOLD	1.6,-0.2	Input	Input	n.c
118	D1	I/O	HOLD	1.6,-0.2	Input	Input	n.c
119	D0	I/O	HOLD	1.6,-0.2	Input	Input	n.c
120	GND	Power	-	-	-	-	-
121	GND	Power	-	-	-	-	-
122	ACD1#	I	100KPU	-	Input	Input	n.c
123	ACE1#	Tri	-	2/3,-2/-3	Z	Z	n.c
124	ACE2#	Tri	-	2/3,-2/-3	Z	Z	n.c
125	AOE#	Tri	-	2/3,-2/-3	Z	Z	n.c
126	SLOT_A_V_{CC}	Power	-	-	Off	Off	V_{CC} (*5)
127	AVS1	I	100KPU	-	Input	Input	n.c
128	AIORD#	Tri	-	2/3,-2/-3	Z	Z	n.c
129	AIOWR#	Tri	-	2/3,-2/-3	Z	Z	n.c
130	AWE#	Tri	-	2/3,-2/-3	Z	Z	n.c
131	ARDY_IRQ#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
132	AVS2	I	100KPU	-	Input	Input	n.c
133	ARESET	Tri	-	2/3,-2/-3	Z	Z	n.c
134	AWAIT#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
135	V_{CC}	Power	-	-	-	-	-
136	AREG#	Tri	-	2/3,-2/-3	Z	Z	n.c
137	ABVD2_SPKR	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
138	ABVD1_STSCHG#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
139	AWP_IOIS16#	I	100K/60KPU	-	Hi-Z	Hi-Z	n.c
140	GND	Power	-	-	-	-	-
141	ACD2#	I	100KPU	-	Input	Input	n.c
142	AADRENA#	O	-	2,-2	High	High	n.c
143	ADATAENA#	O	-	2,-2	High	High	n.c
144	AVPPPGM	O	-	6,-6	Low	Low	n.c
145	AVPPVCC	O	-	6,-6	Low	Low	n.c
146	AVCC5#	O	-	6,-6	High	High	n.c
147	AVCC3#	O	-	6,-6	High	High	n.c
148	CA25	O	-	6,-6	Drive	Drive	n.c
149	CA24	O	-	6,-6	Drive	Drive	n.c
150	CA23	O	-	6,-6	Drive	Drive	n.c
151	SLCT	I	External	-	Input	Input	Pull-up(V_{CC})
152	PE	I	External	-	Input	Input	Pull-up(V_{CC})
153	BUSY	I	External	-	Input	Input	Pull-up(V_{CC})
154	ACK#	I	External	-	Input	Input	Pull-up(V_{CC})
155	LPTD7	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
156	LPTD6	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
157	LPTD5	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
158	LPTD4	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
159	LPTD3	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
160	SLCTIN#	I/OD	External	12,-	Input	Input(*4)	Pull-up(V_{CC})
161	GND	Power	-	-	-	-	-

Pin	Name	Type	Termination	Drive (3.3V/5V) I_{OL}, I_{OH} (mA)	Reset	Suspend	Termination of unused pins
162	LPTD2	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
163	INIT#	I/OD	External	12,-	Low	Input(*4)	Pull-up(V_{CC})
164	LPTD1	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
165	V_{CORE}	Power	-	-	-	-	-
166	V_{BK}	Power	-	-	-	-	V_{CC} (*8)
167	ERROR#	I	External	-	Input	Input	Pull-up(V_{CC})
168	LPTD0	I/OD	External	6,-	Low	Input(*4)	Pull-up(V_{CC})
169	AFD#	I/OD	External	12,-	Input	Input(*4)	Pull-up(V_{CC})
170	STROBE#	I/OD	External	12,-	Input	Input(*4)	Pull-up(V_{CC})
171	STANDBY#	O	-	6,-6	High	Low	n.c
172	ROMDIS#	I	50KPU	-	Input(High)	Input(High)	n.c
173	RESERVE	-	-	-	-	-	n.c
174	EXTCLKI	I	100KPU	-	Input	Input	n.c
175	RESERVE	-	-	-	-	-	n.c
176	CA22	O	-	6,-6	Drive	Drive	n.c
177	TXD0	O	-	1.6,-0.2	Z	Z	n.c
178	SCK0	O	-	1.6/-0.2	High(*1)	Z	n.c
179	RXD0	I	100KPU	-	Input	Input	n.c
180	AN4	I	-	-	Hi-Z	Hi-Z	n.c
181	GND	Power	-	-	-	-	-
182	AN5	I	-	-	Hi-Z	Hi-Z	n.c
183	DA1	O	-	-	Z	Z	n.c
184	DA0	O	-	-	Z	Z	n.c
185	TXD1	O	-	1.6/-0.2	Z	Z	n.c
186	RXD1	I	100KPU	-	Input	Input	n.c
187	TXD2	O	-	1.6/-0.2	Z	Z	n.c
188	RXD2	I	100KPU	-	Input	Input	n.c
189	RTS2#	O	-	1.6/-0.2	High(*1)	Z	n.c
190	CTS2#	I	100KPU	-	Input	Input	n.c
191	PWOFF#	O	-	1.6/-0.2	High(*1)	High	n.c
192	SRBTN#	I	60KPU	-	Input	Input	n.c
193	FPVCCON	O	-	1.6/-0.2	High(*1)	Low	n.c
194	PTC7/PINT7	I/O	60KPU	1.6/-0.2	Input	Input or Output(*2)	n.c
195	PTC6/PINT6	I/O	60KPU	1.6/-0.2	Input	Input or Output(*2)	n.c
196	PTC5/PINT5	I/O	60KPU	1.6/-0.2	Input	Input or Output(*2)	n.c
197	V_{CC}	Power	-	-	-	-	-
198	PTC4/PINT4	I/O	60KPU	1.6/-0.2	Input	High(*2)	n.c
199	PTC3/PINT3	I/O	60KPU	1.6/-0.2	Input	Low(*2)	n.c
200	PTC2/PINT2	I/O	60KPU	1.6/-0.2	Input	High(*2)	n.c
201	PTC1/PINT1	I/O	60KPU	1.6/-0.2	Input	Input or Output(*2)	n.c
202	GND	Power	-	-	-	-	-
203	DACK0#	O	-	1.6/-0.2	High(*1)	Z	n.c
204	DREQ0#	I	100KPU	-	Input	Input	n.c
205	DACK1#	O	-	1.6/-0.2	High(*1)	Z	n.c
206	DREQ1#	I	100KPU	-	Input	Input	n.c
207	NMI	I	100KPU	-	Input	Input	n.c
208	IRQ1	I	60KPU	-	Input	Input	n.c
209	IRQ2	I	60KPU	-	Input	Input	n.c
210	IRQ3	I	60KPU	-	Input	Input	n.c
211	IRQ4	I	60KPU	-	Input	Input	n.c
212	VSYNC	O	-	6,-6	Low	Low	n.c

Pin	Name	Type	Termination	Drive (3.3V/5V) I_{OL}, I_{OH} (mA)	Reset	Suspend	Termination of unused pins
213	HSYNC	O	-	6,-6	Low	Low	n.c
214	B	O	150PD	-	-	-	n.c
215	G	O	150PD	-	-	-	n.c
216	R	O	150PD	-	-	-	n.c
217	FPDAT15	O	-	6,-6	Low	Low	n.c
218	FPDAT14	O	-	6,-6	Low	Low	n.c
219	FPDAT13	O	-	6,-6	Low	Low	n.c
220	FPDAT12	O	-	6,-6	Low	Low	n.c
221	GND	Power	-	-	-	-	-
222	FPDAT11	O	-	6,-6	Low	Low	n.c
223	FPDAT10	O	-	6,-6	Low	Low	n.c
224	FPDAT9	O	-	6,-6	Low	Low	n.c
225	FPDAT8	O	-	6,-6	Low	Low	n.c
226	V_{CC}	Power	-	-	-	-	-
227	FPDAT7	O	-	6,-6	Low	Low	n.c
228	FPDAT6	O	-	6,-6	Low	Low	n.c
229	FPDAT5	O	-	6,-6	Low	Low	n.c
230	FPDAT4	O	-	6,-6	Low	Low	n.c
231	FPDAT3	O	-	6,-6	Low	Low	n.c
232	FPDAT2	O	-	6,-6	Low	Low	n.c
233	FPDAT1	O	-	6,-6	Low	Low	n.c
234	FPDAT0	O	-	6,-6	Low	Low	n.c
235	DOTCLK	O	-	6,-6	Low	Low	n.c
236	MOD	O	-	6,-6	Low	Low	n.c
237	FPVEEON	O	-	2,-2	Low	Low	n.c
238	LINE	O	-	6,-6	Low	Drive(*3)	n.c
239	FRAME	O	-	6,-6	Low	Drive(*3)	n.c
240	GND	Power	-	-	-	-	-

(*1) This is an output connector, but goes high-impedance while system is resetted, and is held high by a pull-up resistor. After a reset, the SH7709A registers are set by software, and this is then an output (no pull-up resistor).

(*2) This is an input or output depending on SH7709A register settings. One of PTC7/PINT7, PTC6/PINT6, and PTC5/PINT5 is assigned to SRBTN_RST# and becomes an output. The other two and PTC1/PINT1 are inputs or as specified by the last setting. For details of SRBTN_RST#, see Chapter 8, "Power Management." On the evaluation board, PTC4/PINT4, PTC3/PINT3, PTC2/PINT2 are used for a four-wire resistor film touch panel. Therefore, depending on the method of use, a setting change is required.

(*3) Depending on the SED1355 register settings, this is high or low. FRAME and LINE are set to Active High or Active Low, according to the specification of the connected panel. When Windows CE is used as the OS, during a suspend the Epson loader sets these low, regardless of the Active High or Active Low setting.

(*4) This is input or low, according to the companion chip register settings. When Windows CE is used as the OS, the Epson loader sets this to input.

(*5) The SLOT_A_V_{CC} and SLOT_B_V_{CC} pins cannot be set to be unused. If the PCMCIA slot is not required, connect V_{CC} (3.3V ± 0.15V).

(*6) The RESETP# pin cannot be set to be unused. When this signal goes active, a power on reset is applied to the CARD-E09A. Connect a circuit for generating Power Good signal. Do not make this active simultaneously with RESETM#. A reset may not occur.

(*7) The RESETM# pin cannot be set to be unused. When this signal goes active, a manual reset is applied to the CARD-E09A. When a manual reset circuit is not required, pull up to V_{CC} (3.3V ± 0.15V). Do not make this active simultaneously with the RESETP# connector. A reset may not occur.

(*8) The V_{BK} pin cannot be set to be unused. If a backup circuit is not required, connect to V_{CC} (3.3V ± 0.15V).

12. Method of fixing and attachment

12.1. Method of Attachment

12.1.1. Installing a CompactFlash card

In the CARD-E09A, the connector used for the CompactFlash card is a Fujitsu FCN-568H050-G/A1. This connector cannot be fitted with an eject mechanism. Fig. 12-1 shows how to attach the compact flash card.

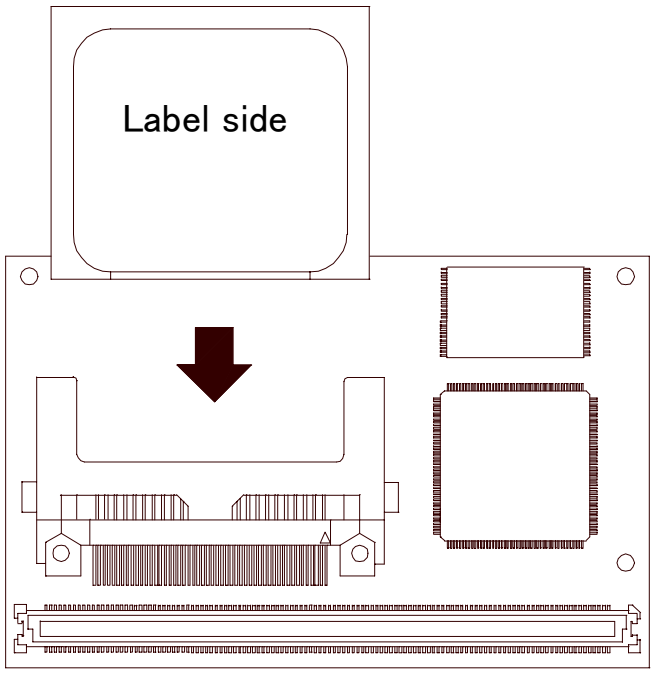


Fig. 12-1 CompactFlash card attachment

12.1.2. CARD-E09A attachment

Required for fixing

- Hexagonal pillars (M2) (7 mm long) (3)
- Nuts (M2) (3)
- Screws (M2) (3)

Attachment procedure

(1) Insert the male ends of the hexagonal pillars into the three holes in the motherboard, and fasten with the nuts.
(2) Next, as shown in Fig. 12-2, plug the CARD-E09A into the 240-pin connector.
(3) Fasten the three screws.

Reference values for fastening torque

Use 0.3 N.m as a guide value. However, this is only a reference value. The torque must be made to be appropriate for the vibration conditions to which the system is subject.

Fig. 12-2 shows the attachment.

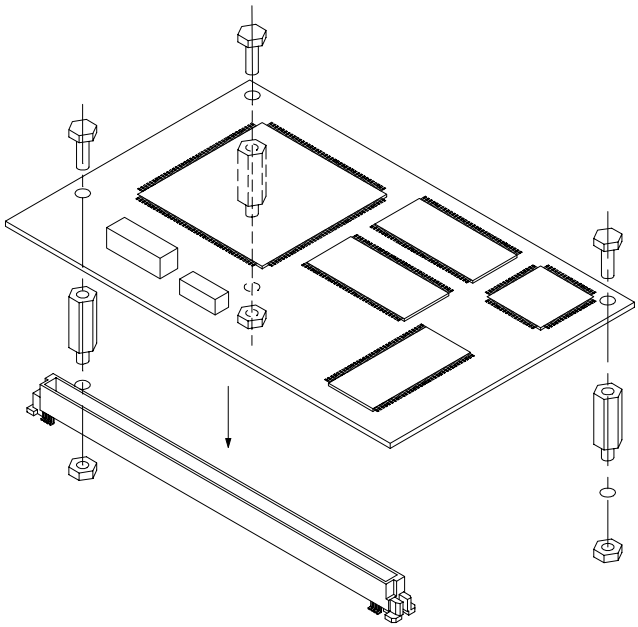


Fig. 12-2 CARD-E09A attachment

12.2. Connector

There are two types of connector which can be used to accept the CARD-E09A (on the motherboard), as follows. The height dimension from the mounting surface is different.

Table 12-1 Connector types

Type number	Manufacturer	Specification
53467-2409	Molex	H = 6mm UL 94V-0
53481-2409	Molex	H = 7mm UL 94V-0

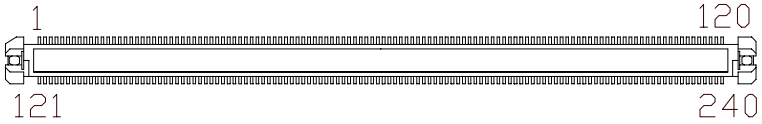


Fig. 12-3 Connector pin assignments

13. Appendix

13.1. Multifunction Buffer IC (E0C37120)

A data sheet for the multifunction buffer IC (E0C37120) used as a level shifter circuit for the evaluation board PCMCIA is shown. It can be used in combination with the CARD-E09A.

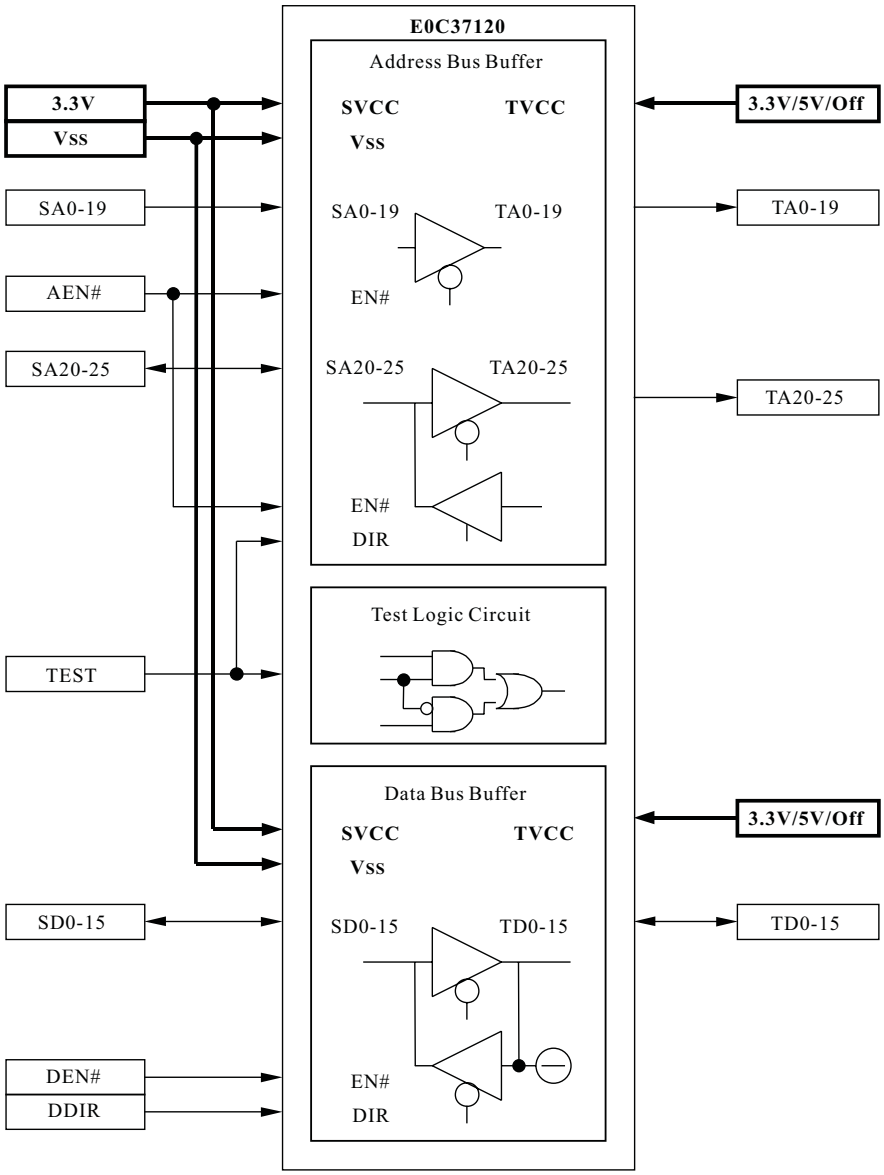
13.1.1. Overview

The E0C37120 is a multifunction buffer IC which can be used as a PCMCIA interface buffer and 3.3V ⇔ 5V level shifter, among other things. Since it allows multiple chip buffer ICs to be replaced by a single chip, it allows the system to be made more compact. Again, it has excellent characteristics as an interface buffer for PCMCIA card "hot plugging."

13.1.2. Features

- Internal 26-bit unidirectional buffer
- Internal 16-bit bi-directional buffer
- Target power (3.3V and 5V) can be turned off
- Internal 3.3V, 5V level shifter
- High-speed 0.35 μm CMOS process
- QFP15-100 compact package

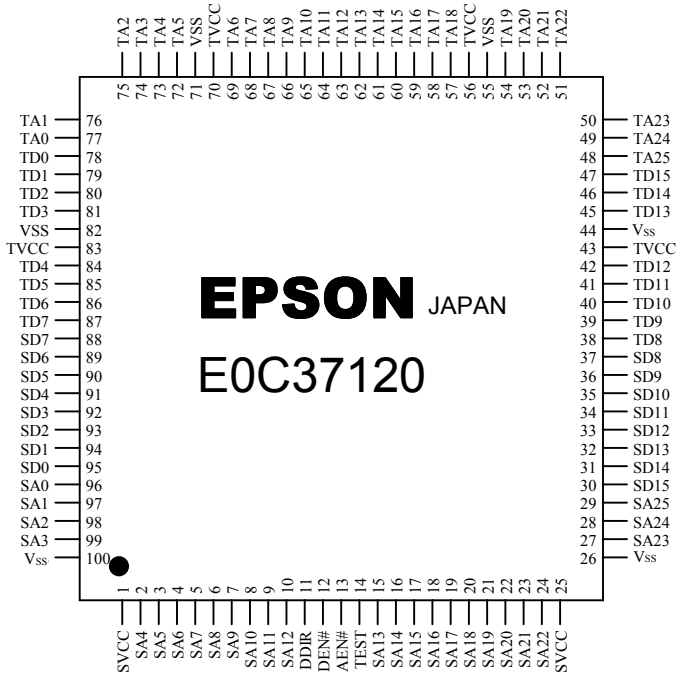
13.1.3. Block Diagram



* A '#' at the end of a connector name indicates active low.

13.1.4. Connector Description

- Connector layout



- Connector functions

Connector name	Description	Type	Number of connectors	Power
SA0-19	System address bus signals	I	20	SVCC
SA20-25	System address bus signals When TEST is high, SA20 to SA25 are a test signal output When unused, connect to VSS through a resistor of at least 10-Kohms	I/O	6	SVCC
SD0-15	System data bus signal When unused, connect to VSS through a resistor of at least 10-Kohms	I/O	16	SVCC
TA0-25	Target address bus signal	O	26	TVCC
TD0-15	Target data bus signal When unused, leave unconnected	I/O PD	16	TVCC
AEN#	Address bus buffer enable signal	I	1	SVCC
TEST	Test signal Be sure to connect to VSS	I	1	SVCC
DEN#	Data bus buffer enable signal	I	1	SVCC
DDIR	Data bus buffer direction signal When DDIR is high, driven in direction SDxx ← TDxx When DDIR is low, driven in direction SDxx → TDxx	I	1	SVCC
SVCC	System power and internal logic power 3.3V Be sure to connect all power connectors to power	P	2	-
TVCC	When target address bus buffer and data bus buffer power (3.3V/5V/Off) is off, to prevent increased static current consumption, set "AEN# high Be sure to connect all power connectors to power	P	4	-
VSS	Ground Be sure to connect all power connectors to ground	P	6	-

Note: The symbols in the connector types have the following meanings.
I：Input port O: Output port I/O: Bi-directional port
P：Power port PD: with pull-down resistance

13.1.5. Electrical Characteristics

- Absolute maximum rating

Vss=0V

Parameter	Symbol	Rating	units
Power voltage	SVCC	-0.3 to 4.6	V
	TVCC	-0.3 to 6.0	V
Pin voltage	VPIN	-0.3 to SVCC+0.5 -0.3 to TVCC+0.5	V V
Output current / pin	IOUT	± 5	mA
Output current / pin Output current (total)	∑IOUT	± 30	mA
Storage temperature	Tstg	-65 to 150	°C

- Recommended operating conditions

Vss=0V

Symbol	Parameter	Min.	Typ.	Max.	units	notes
SVCC	SVCC power voltage	3.0	3.3	3.6	V	–
TVCC	TVCC power voltage	3.0	–	5.5	V	note 1
VPIN	SVCC pin voltage	Vss	–	SVCC	V	–
	TVCC pin voltage	Vss	–	TVCC	V	–
Ta	Operating temperature	-40	–	85	°C	–

Note 1: Power Off (Hi-Z) input power voltage also possible

- DC characteristics

SVCC=3.3V±0.3V, Vss=0V, Ta=-40 to 85°C

Symbol	Parameter	Min.	Typ.	Max.	units	notes
VOH1	High level output voltage (1) I OH=-2mA	SVCC -0.4	–	—	V	note 2
VOL1	Low level output voltage (1) I OL=2mA	–	–	0.4	V	note 2
VIH1	High level input voltage (1)	2.0	–	–	V	note 3
VIL1	Low level input voltage (1)	–	–	0.8	V	note 3

Note 2: Pins SD0 to SD15
Note 3: Pins SA0 to SA25, SD0 to SD15, AEN#, DEN#, and DDIR

TVCC=3.3V±0.3V, V_{SS}=0V, Ta=-40 to 85°C

Symbol	Parameter	Min.	Typ.	Max.	units	notes
V_{OH2}	High level output voltage (2) I_{OH}=-2mA	TVCC -0.4	–	–	V	note 4
V_{OL2}	Low level output voltage (2) I_{OL}=2mA	–	–	0.4	V	note 4
V_{IH2}	High level input voltage (2)	2.0	–	–	V	note 5
V_{IL2}	Low level input voltage (2)	–	–	0.8	V	note 5
Rpu1	Pull-down resistor (1)	40	100	240	kΩ	note 5

Note 4: Pins TA0 to TA25, TD0 to TD15
Note 5: Pins TD0 to TD15

TVCC=5.0V±0.5V, V_{SS}=0V, Ta=-40 to 85°C

Symbol	Parameter	Min.	Typ.	Max.	units	notes
V_{OH3}	High level output voltage(3) I_{OH}=-3mA	TVCC -0.4	–	–	V	note 4
V_{OL3}	Low level output voltage(3) I_{OL}=3mA	–	–	0.4	V	note 4
V_{IH3}	High level input voltage(3)	3.5	–	–	V	note 5
V_{IL3}	Low level input voltage(3)	–	–	1.0	V	note 5
Rpu2	Pull-down resistor(2)	30	60	144	kΩ	note 5

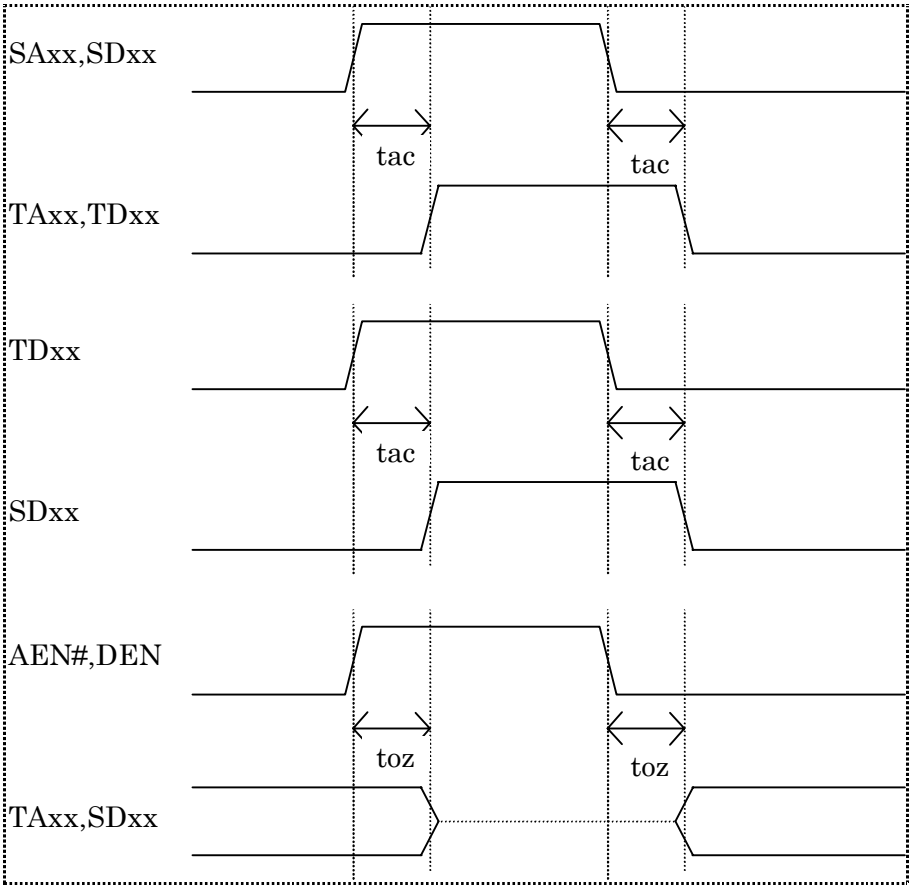
SVCC=3.3V±0.3V, TVCC=5.0V±0.5V, V_{SS}=0V, Ta=-40 to 85°C

Symbol	Parameter	Min.	Typ.	Max.	units	notes
I_{LI}	Input leakage current	-1	–	1	µA	–
I_{OZ}	Output leakage current	-1	–	1	µA	–
C_{IO}	Pin capacitance f = 1MHz , SVCC = 0V, TVCC = 0V	–	–	10	pF	–
I_{CCS}	Static current consumption	–	0.3	35	µA	–

- AC characteristics

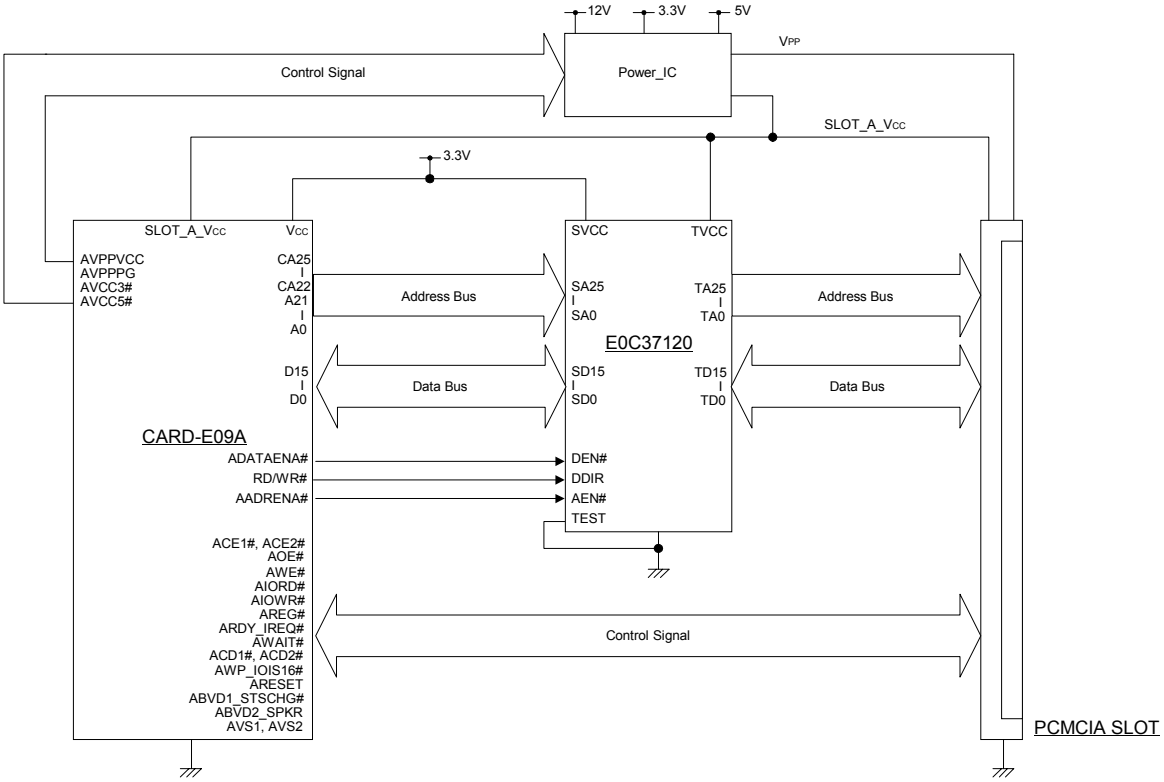
SVCC=3.3V±0.3V, TVCC=3.0V to 5.5V, Vss=0V, CL=30pF, Ta=-40 to 85°C

Symbol	Parameter	Min.	Typ.	Max.	units	notes
t ac	Signal access time	–	–	20	nS	–
t oz	Output signal on/off time	–	–	20	nS	–

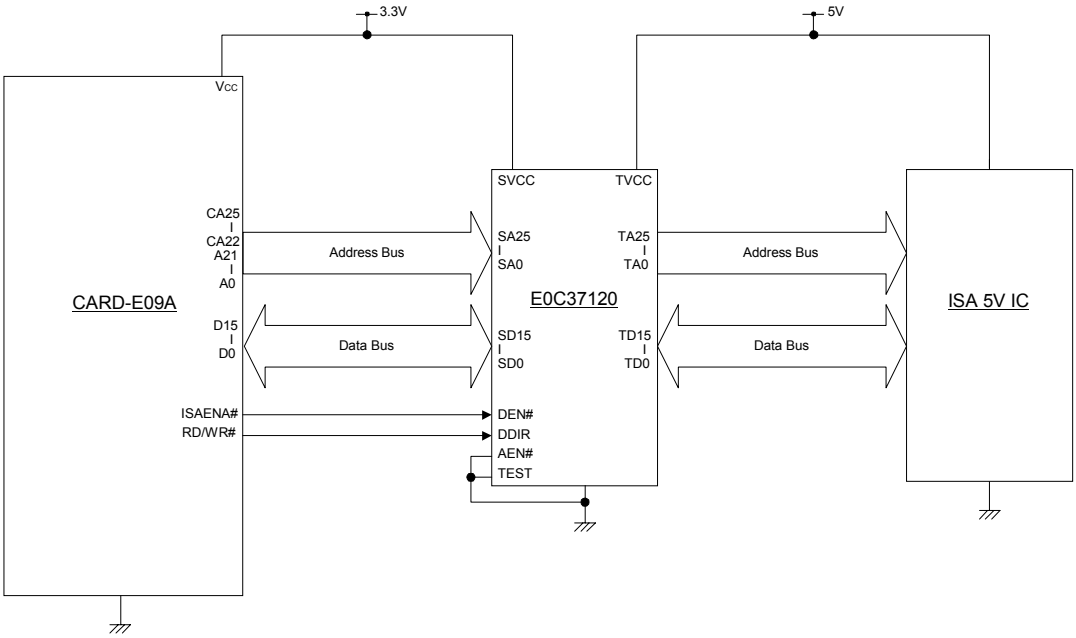


13.1.6. Example Applications

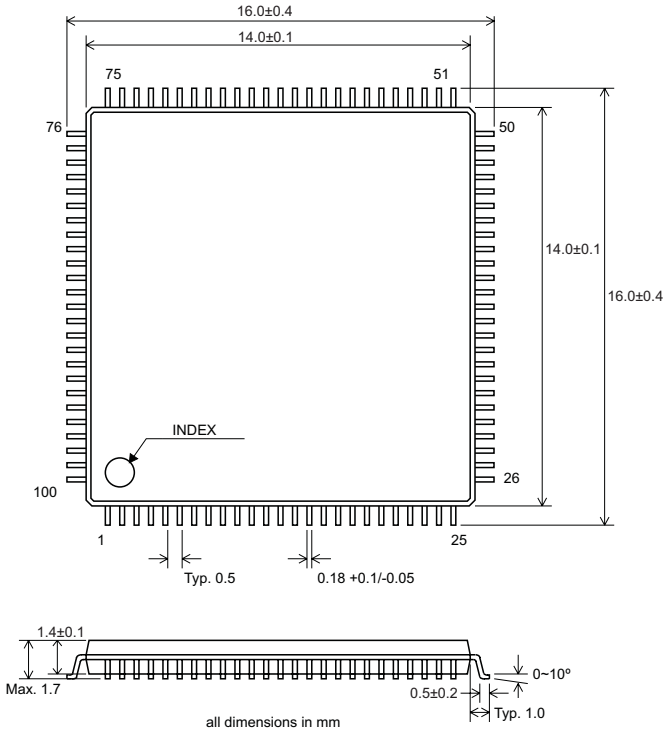
- PCMCIA buffer



- Level shifter buffer



13.1.7. Package Dimensions



13.2. Reference Circuit Diagrams

13.2.1. Reference Circuit Diagrams Based on Evaluation Board

This is a reference circuit diagram based on the evaluation board (SCE88J1B01) supplied with the CARD-E09A evaluation kit (SCE88J0X01). Note that it is not of the evaluation board itself.

13.2.1.1. Differences from the Evaluation Board

Details of changes

The multifunction buffer IC (E0C37120: U2) mounted on the evaluation board is configured as a discrete circuit. This corresponds to Sheets 13/14 to 14/14 of the reference circuit diagrams. In the reference circuit diagrams, U2, R22 to R24, and C8 to C10, which are mounted on the evaluation board are omitted.

Reason for change

The E0C37120 (U1, U2, U6, U7) is a multifunction buffer IC manufactured by Seiko Epson comprising buffer and level shift circuits. It can be used for the PCMCIA interface and 3.3V ⇔ 5V level shifting. In the evaluation board this is adopted for U1, U6, and U7. However, U2 is not a standard manner of use, and since Epson cannot provide a quality guarantee, the reference circuit diagrams have been changed. There is absolutely no problem with any evaluation using the evaluation board.

13.2.1.2. Reference Circuit Diagrams

The reference circuit diagrams comprise the following, a total of 14 sheets.

Sheet 1 CARD-E09A Interface
Sheet 2 Buffer circuit for SH bus
Sheet 3 ISH bus Interface
Sheet 4 Serial Interface
Sheet 5 Video, Key Board/Mouse, Parallel Interface
Sheet 6 PCMCIA Interface
Sheet 7 Buffer circuit for PCMCIA Interface
Sheet 8 Ethernet circuit
Sheet 9 External ROM socket for debugging
Sheet 10 Touch Panel, Audio Circuit
Sheet 11 DC Power regulator, Reset circuit
Sheet 12 Switches
Sheet 13 Buffers
Sheet 14 Misc circuit

Notes

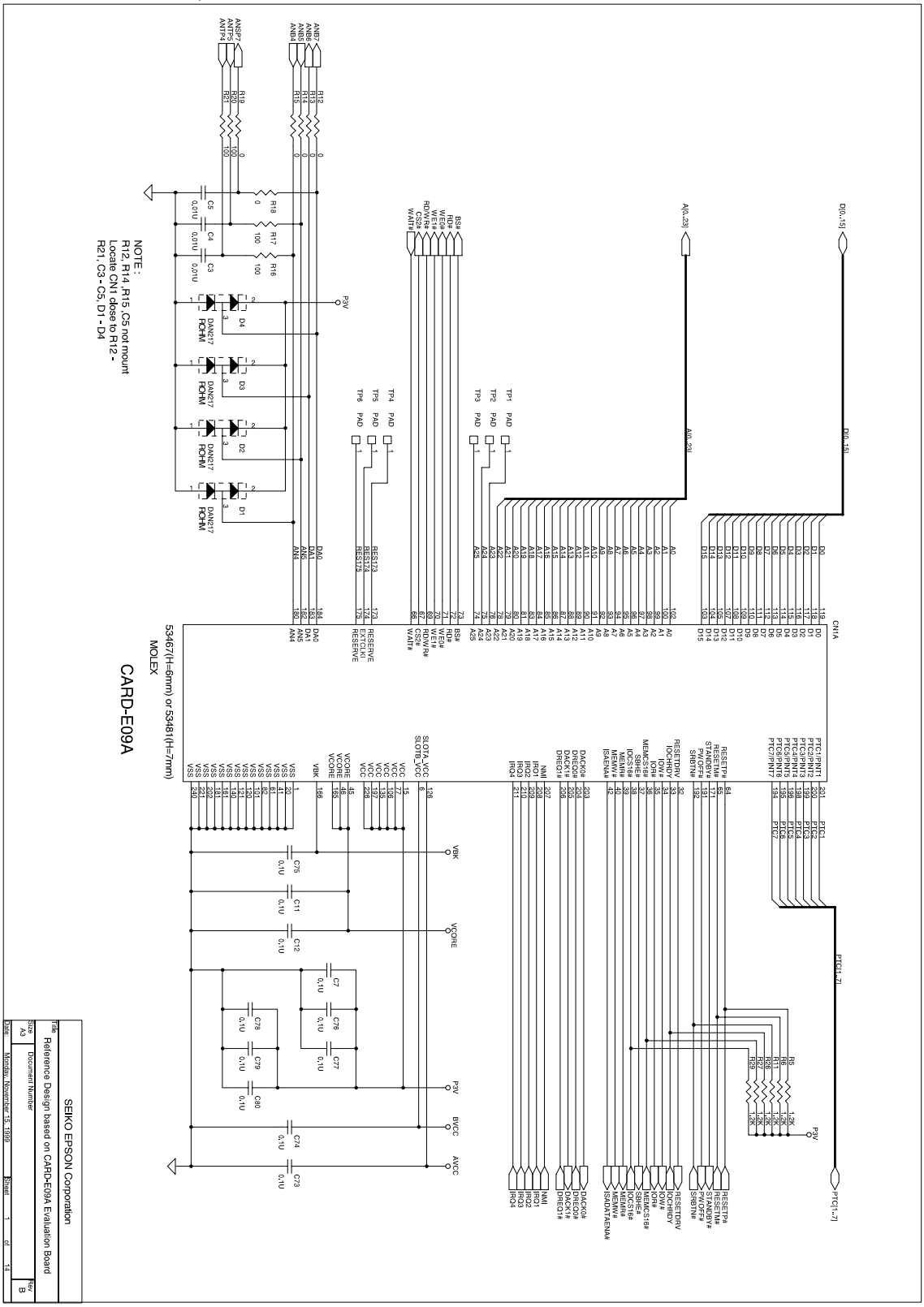
1) Serial interfaces
As described in Section 4.1, "Serial Interfaces," the performance of the NEC RS-232C-compliant driver/receiver used in the evaluation board is guaranteed up to a transfer rate of 9600 bps. When used at a transfer rate above 9600 bps, transfer errors may occur, depending on the cable length or capacitance. For such applications, a different driver/receiver IC should be considered.

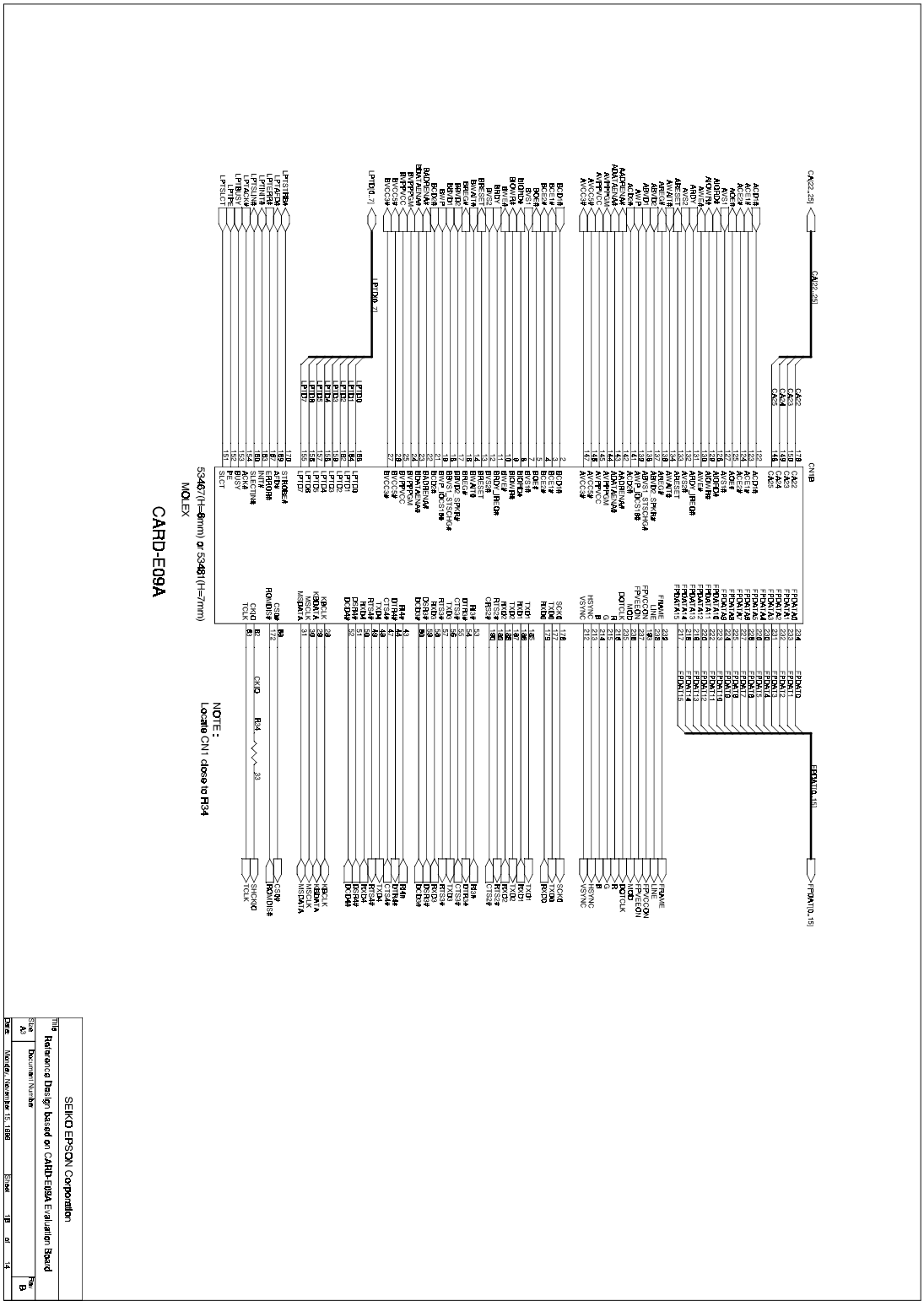
2) Touch panel
As described in the section 7. "A/D and D/A Conversion," the evaluation board only assigns three signals to control the switching of voltage application to the x- and y-axes. Therefore, a current flows even in the standby state. To implement even lower current consumption, four signals should be assigned to control, and the circuit configured so that the voltage is completely off.

3) Reset circuit (RESETP#)
This signal corresponds to Power Good signal. In the evaluation board, the CARD-E09A power V_{CC} (+3.3V) is generated from +5V, and V_{CORE} (+1.9V) is generated from V_{CC} by a regulator circuit. For convenience of circuit design, RESETP# is generated based on only the +5V supply to the evaluation board. However, with this circuit configuration, if the rated voltage cannot be output because of a fault in the regulator circuit for V_{CC} or V_{CORE}, it will still be judged to be normal. To avoid such problems, RESETP# should be generated with reference to the voltage levels both of V_{CC} and V_{CORE}.

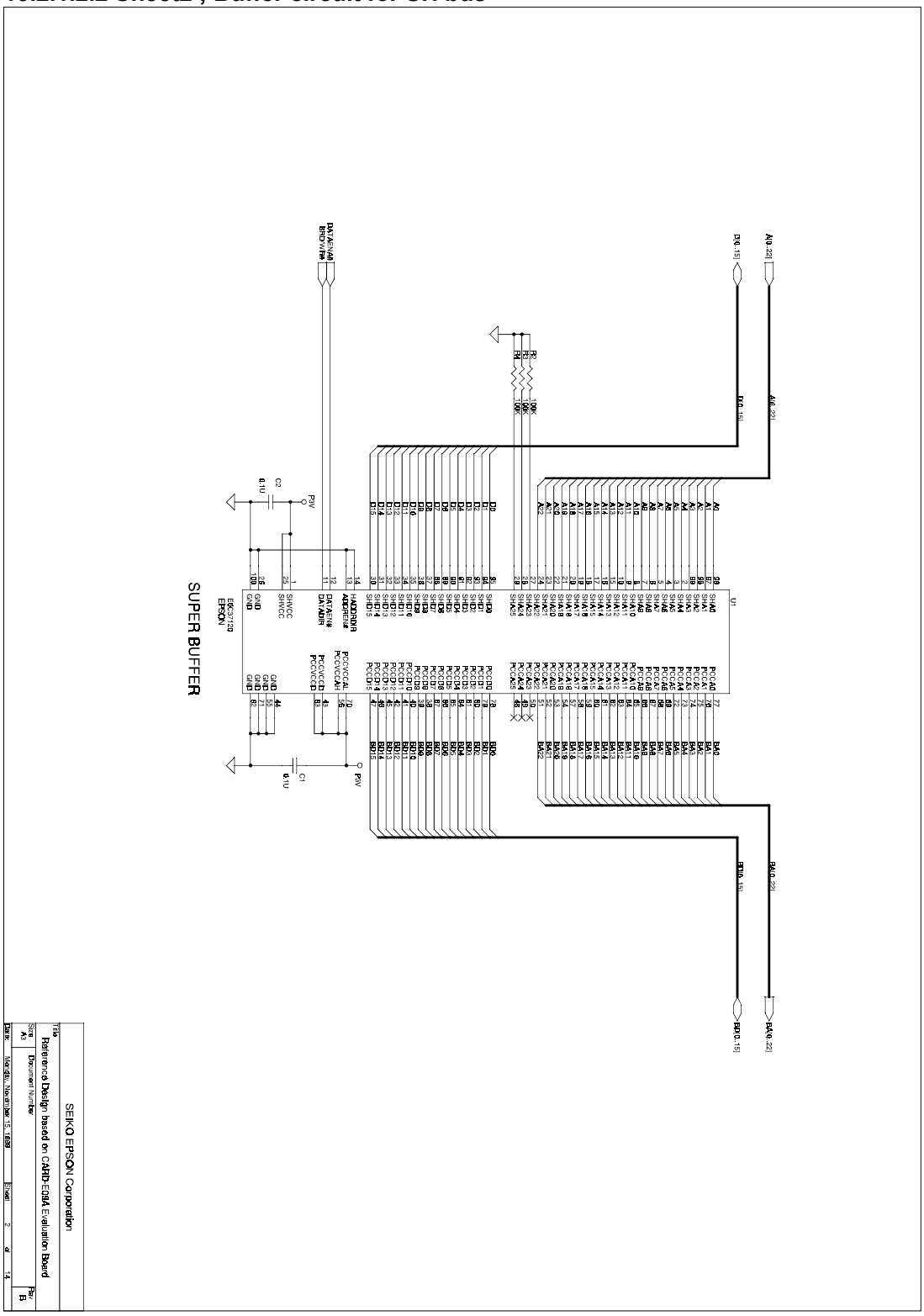
4) Suspend/resume button
See the section 1. "Method of connecting a button switch to the SRBTN# pin for manual switching" in Section 8.2.1.1. "Suspend Resume Button (SRBTN#)." Depending on the manner of use, the circuit shown in Fig. 8-2 is required.

13.2.1.2.1 Sheet 1 ; CARD-E09A Interface

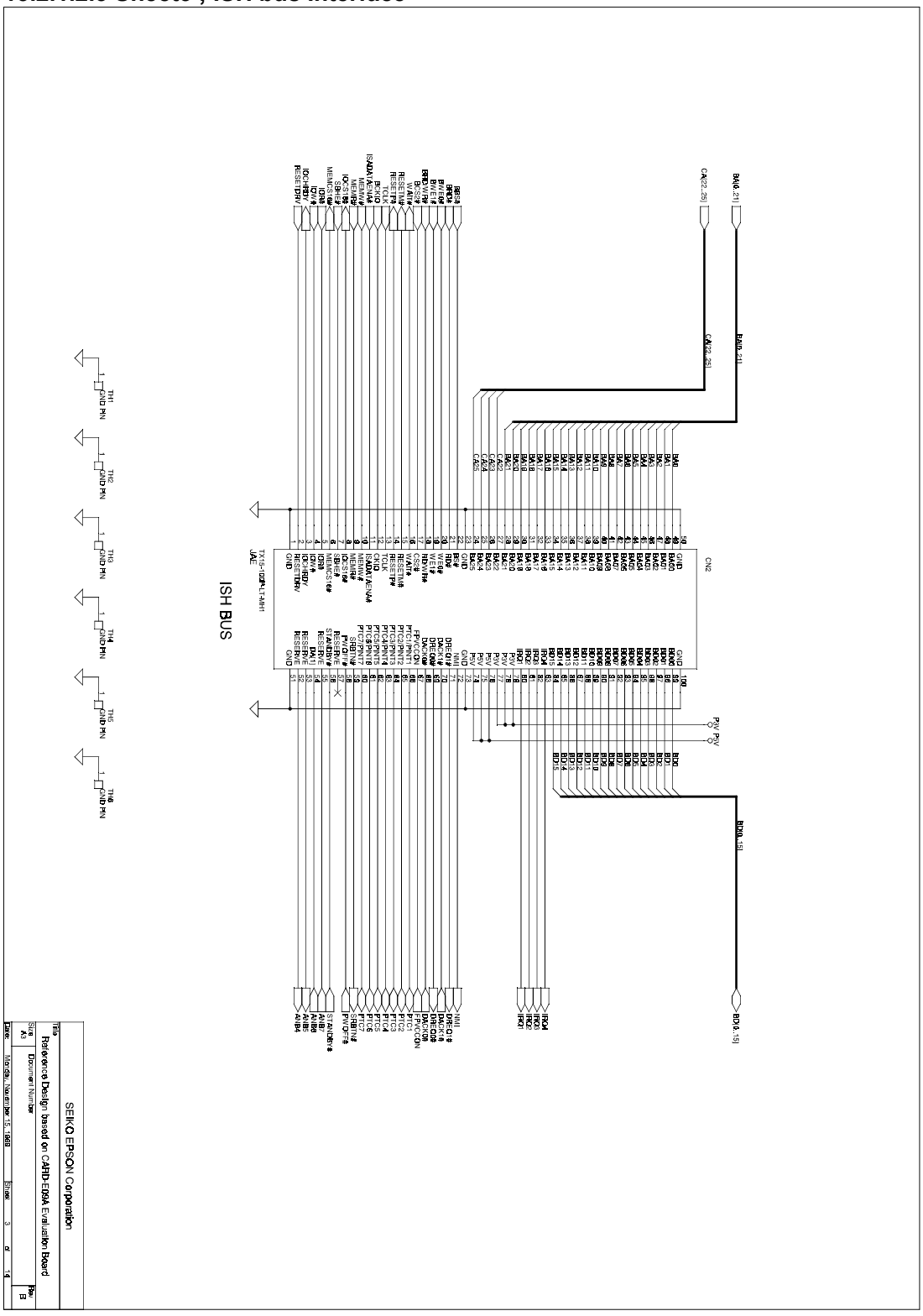



CARD-E09A
53467(H=8mm) or 5348(H=7mm)
MOLEX
CN1B
NOTE :
Locate CN1 close to R34
SEIKO EPSON Corporation
Reference Design based on CARD-E09A Evaluation Board
Document Number
Rev
B
Sheet
14

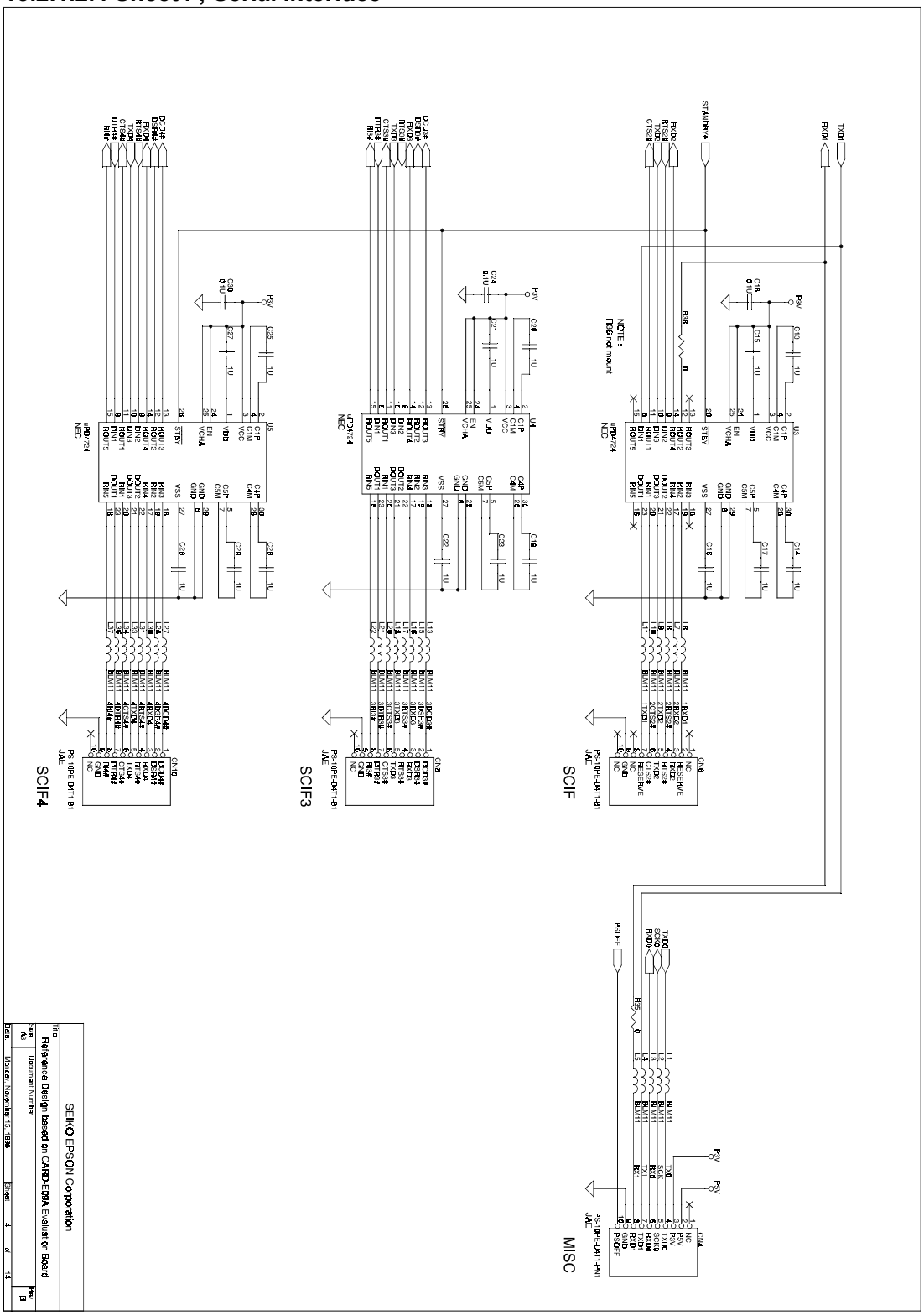
13.2.1.2.2 Sheet2 ; Buffer circuit for SH bus



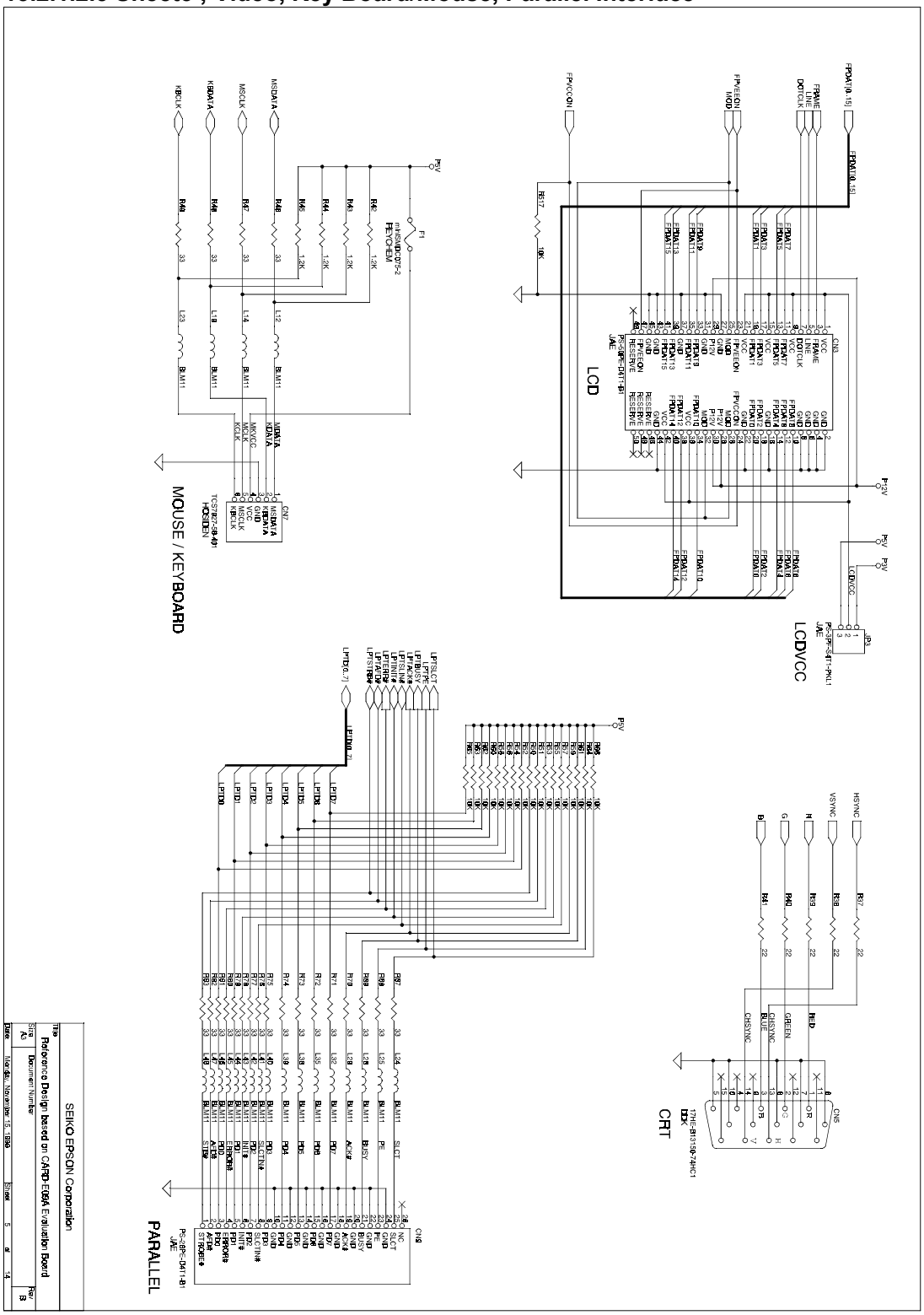
13.2.1.2.3 Sheet3 ; ISH bus Interface



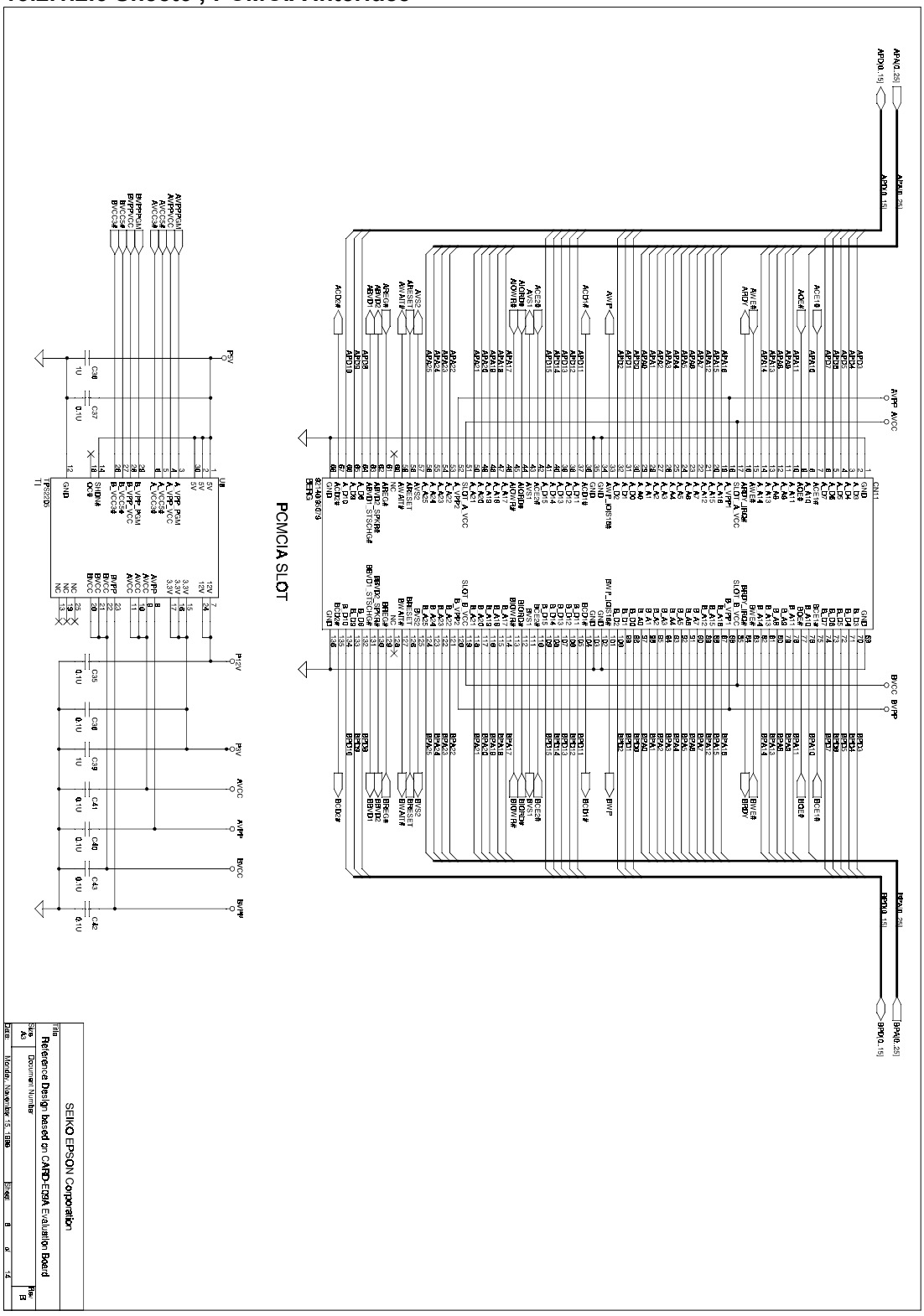
13.2.1.2.4 Sheet4 ; Serial Interface



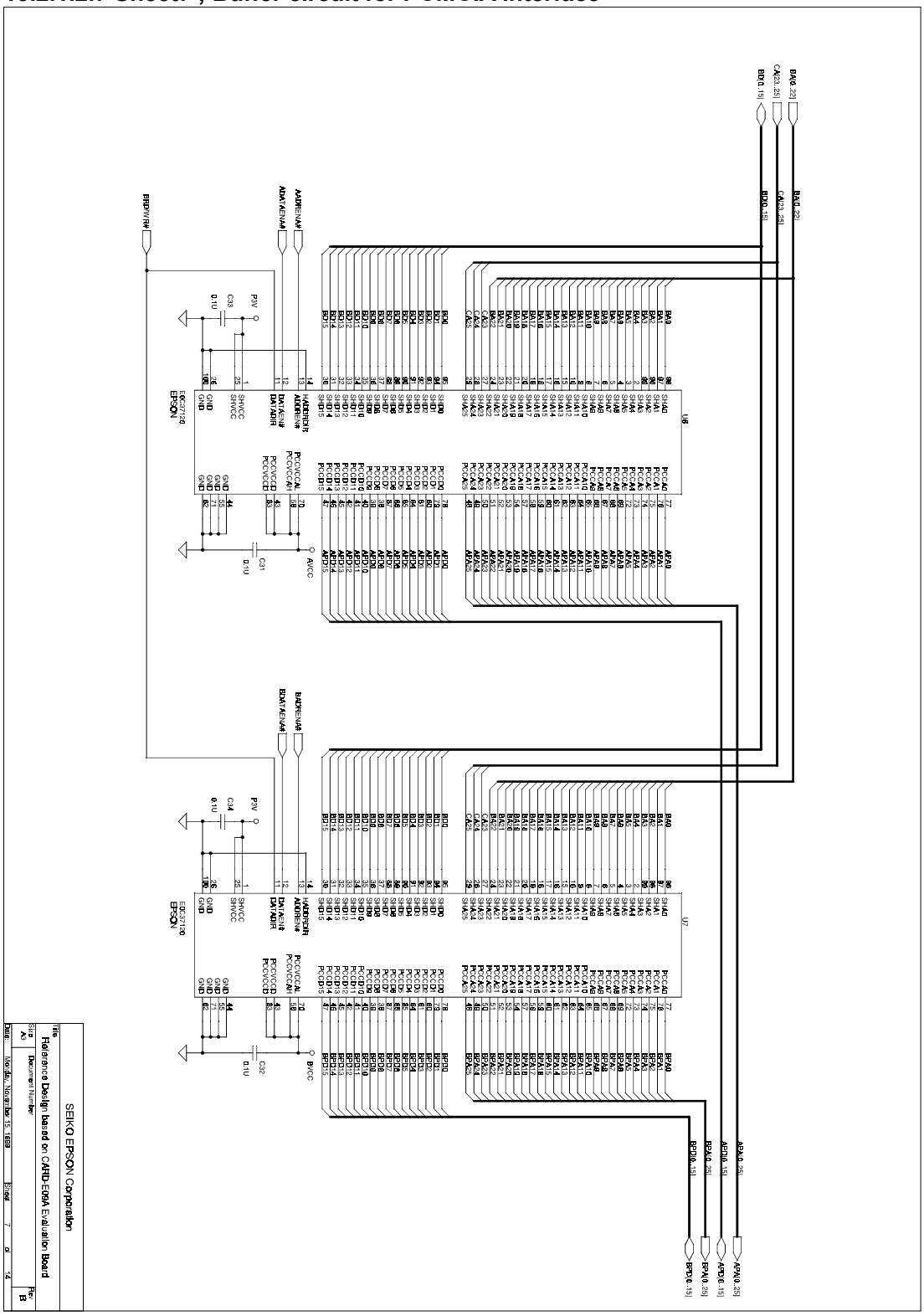
13.2.1.2.5 Sheet5 ; Video, Key Board/Mouse, Parallel Interface



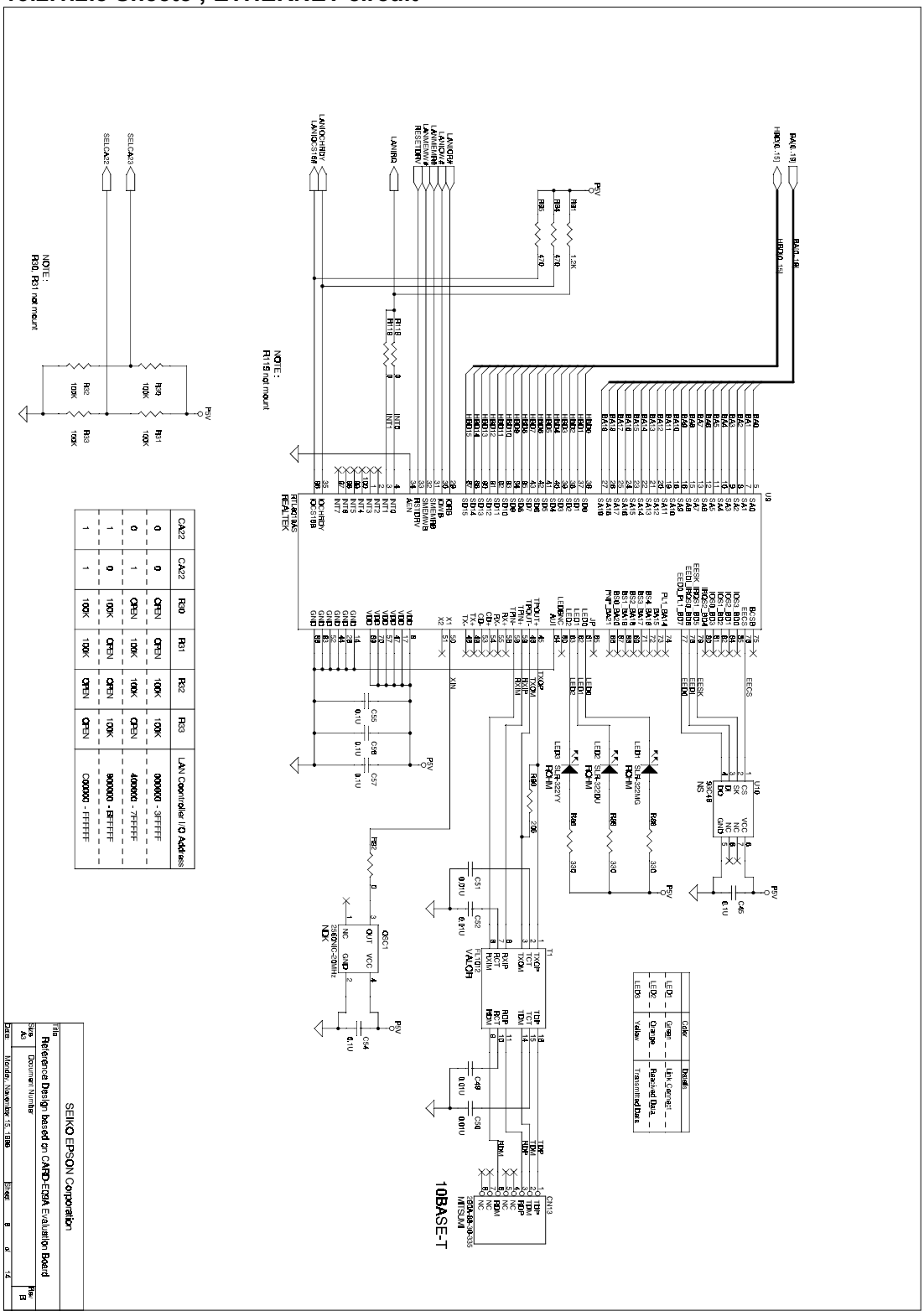
13.2.1.2.6 Sheet6 ; PCMCIA Interface



13.2.1.2.7 Sheet7 ; Buffer circuit for PCMCIA Interface

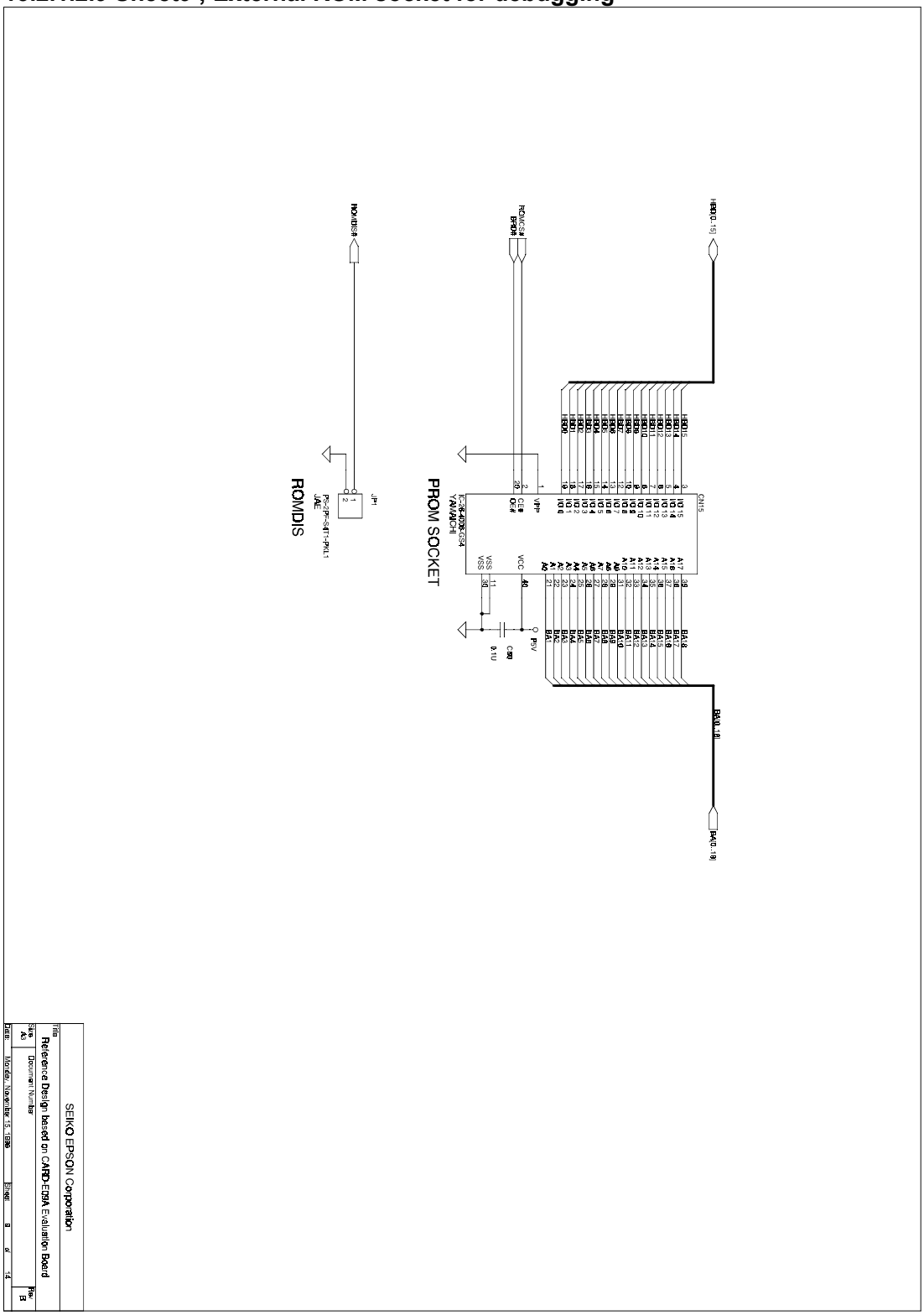


13.2.1.2.8 Sheet8 ; ETHERNET circuit

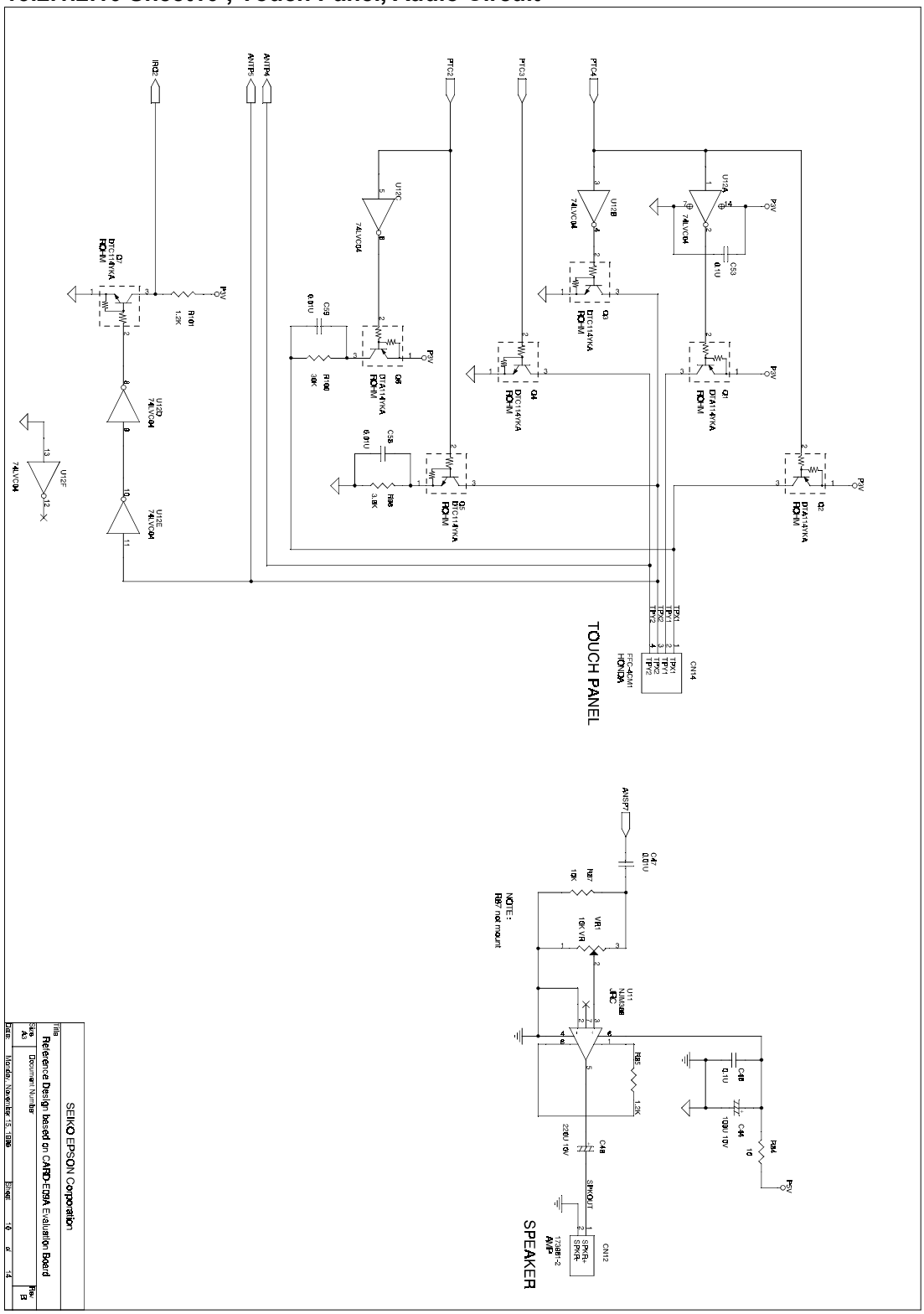


CA22	CA23	R30	R31	R32	R33	LAN Controller I/O Address
0	0	OPEN	OPEN	100K	100K	000000 - 3FFFFF
0	1	OPEN	100K	100K	OPEN	400000 - 7FFFFF
1	0	100K	OPEN	OPEN	100K	800000 - BFFFFF
1	1	100K	100K	OPEN	OPEN	C00000 - FFFFFF

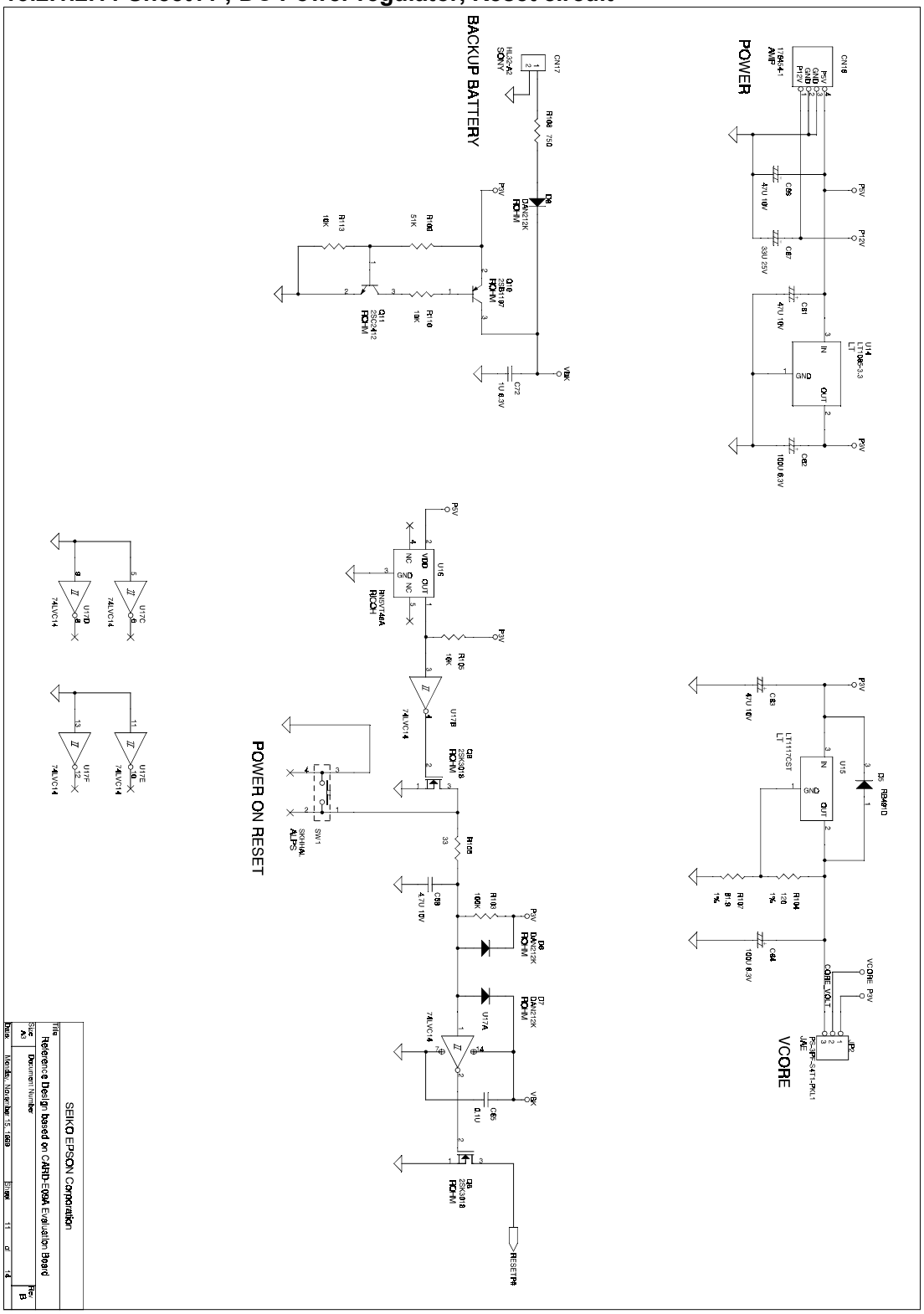
13.2.1.2.9 Sheet9 ; External ROM socket for debugging



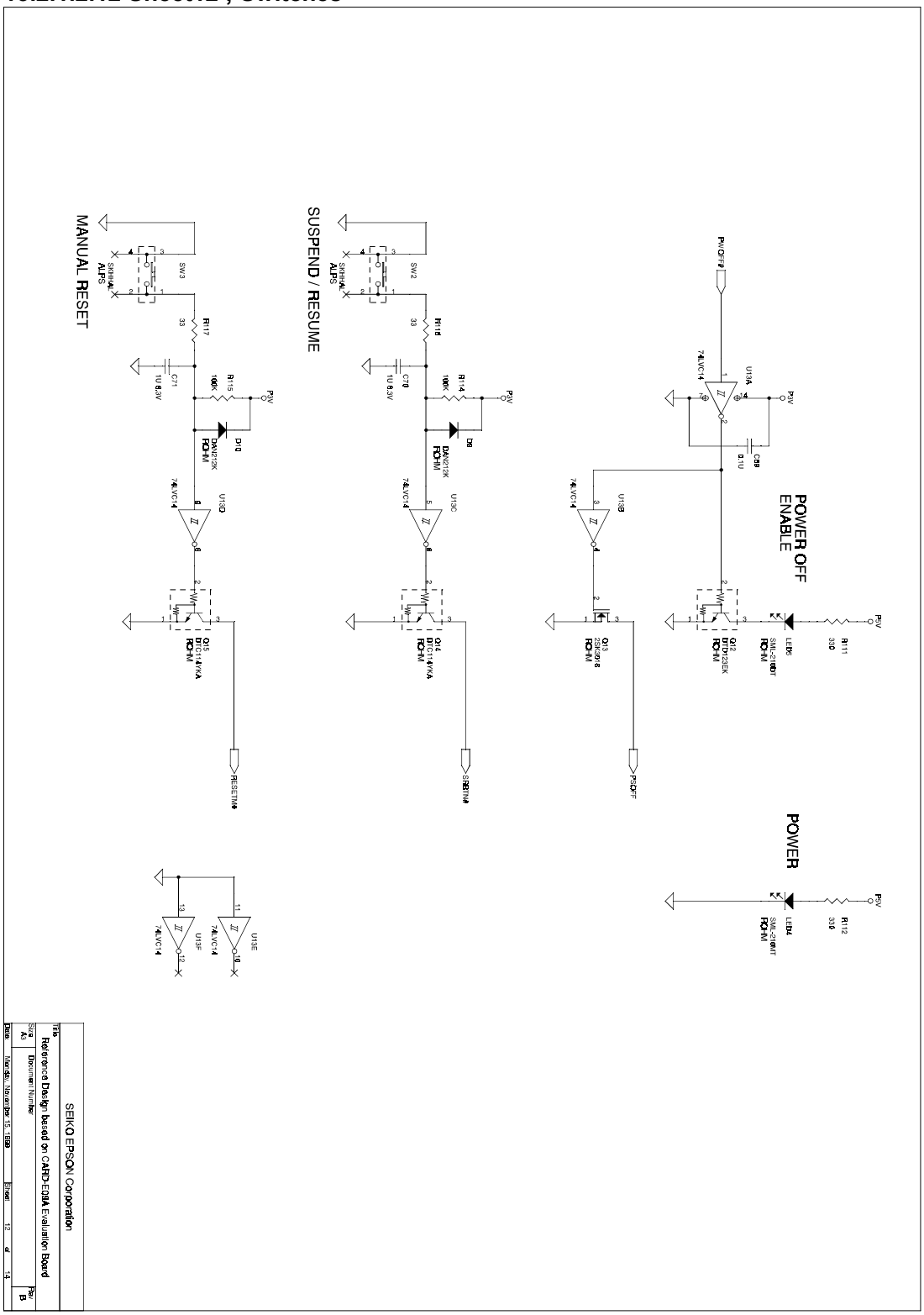
13.2.1.2.10 Sheet10 ; Touch Panel, Audio Circuit



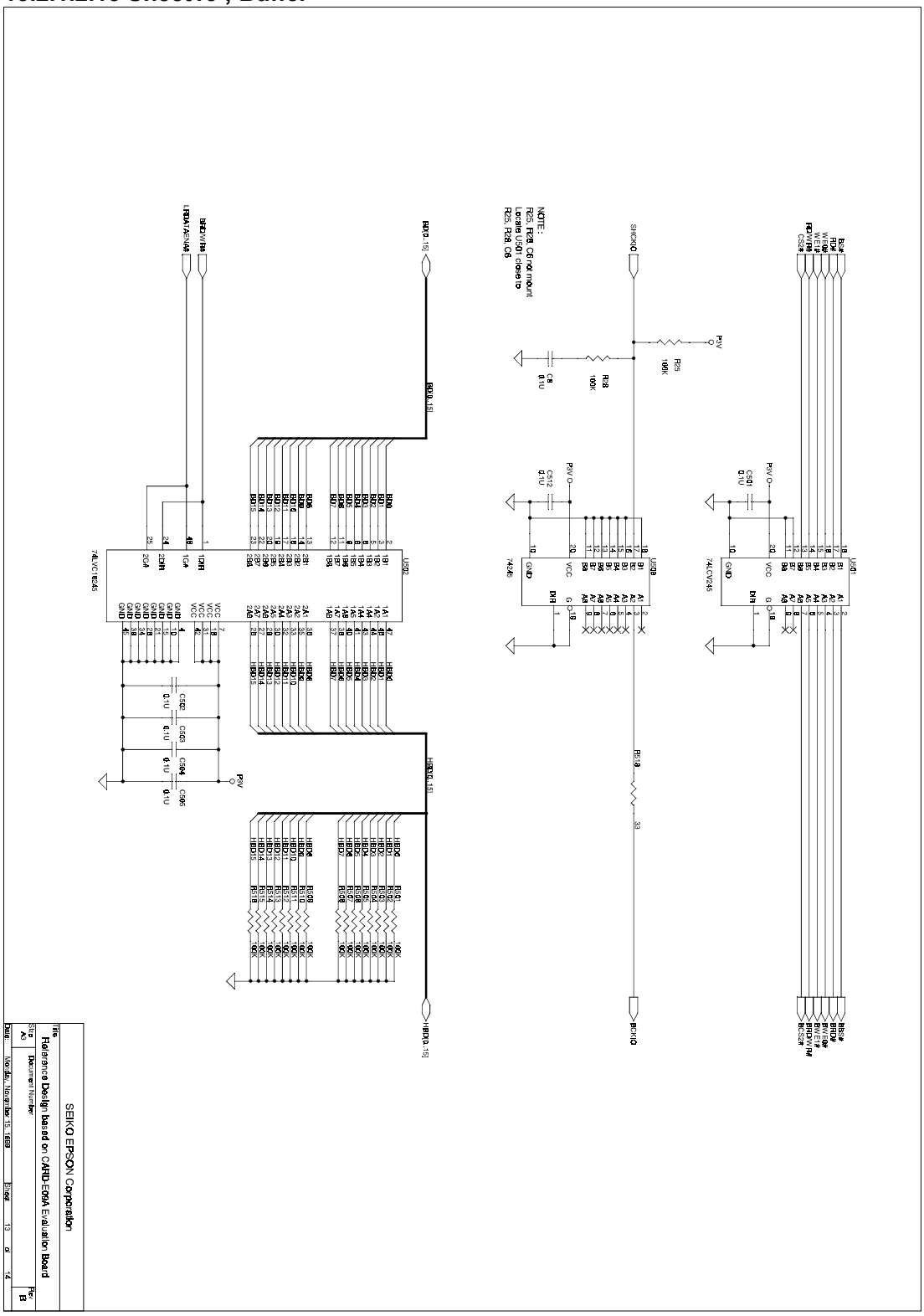
13.2.1.2.11 Sheet11 ; DC Power regulator, Reset circuit



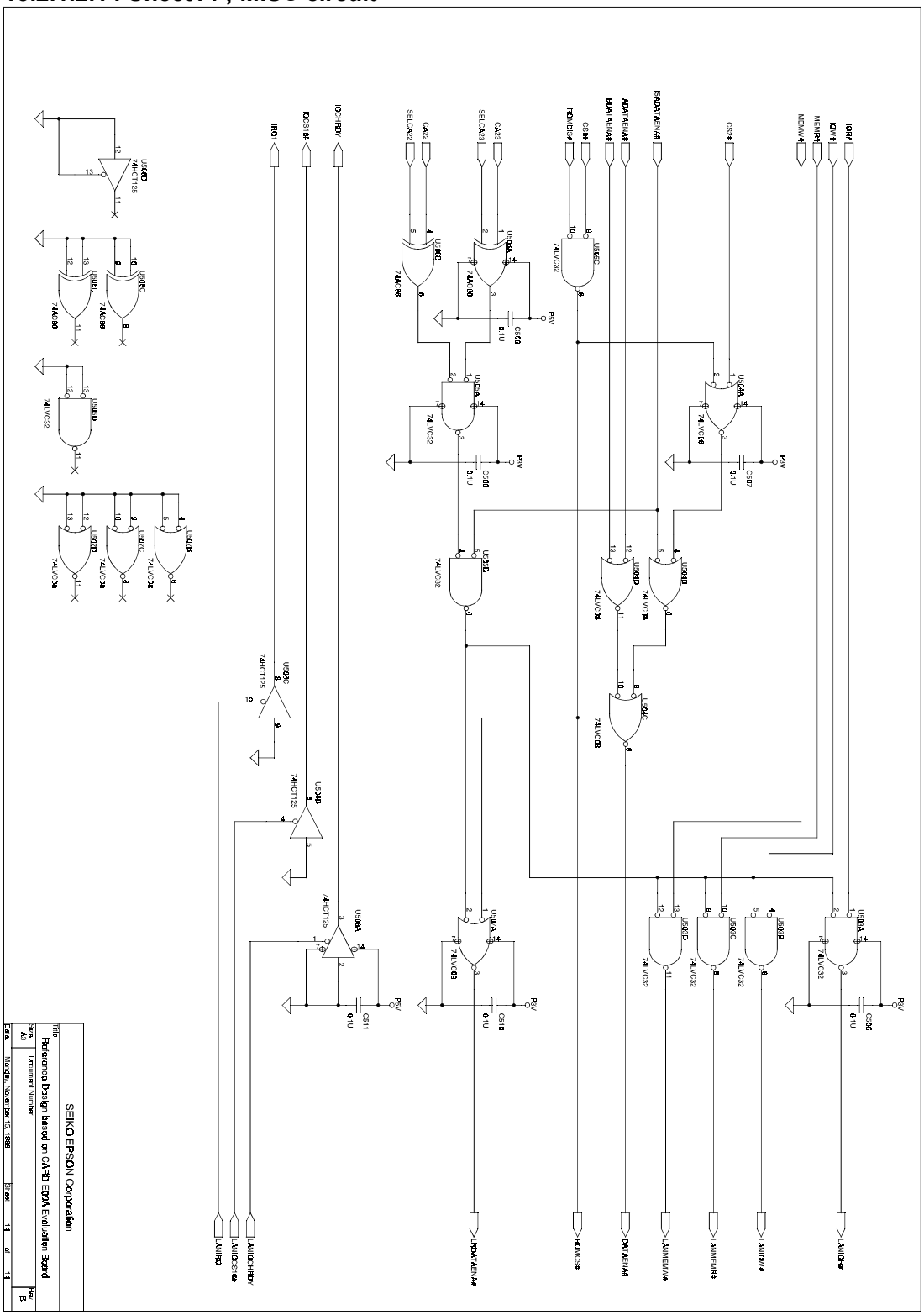
13.2.1.2.12 Sheet12 ; Switches



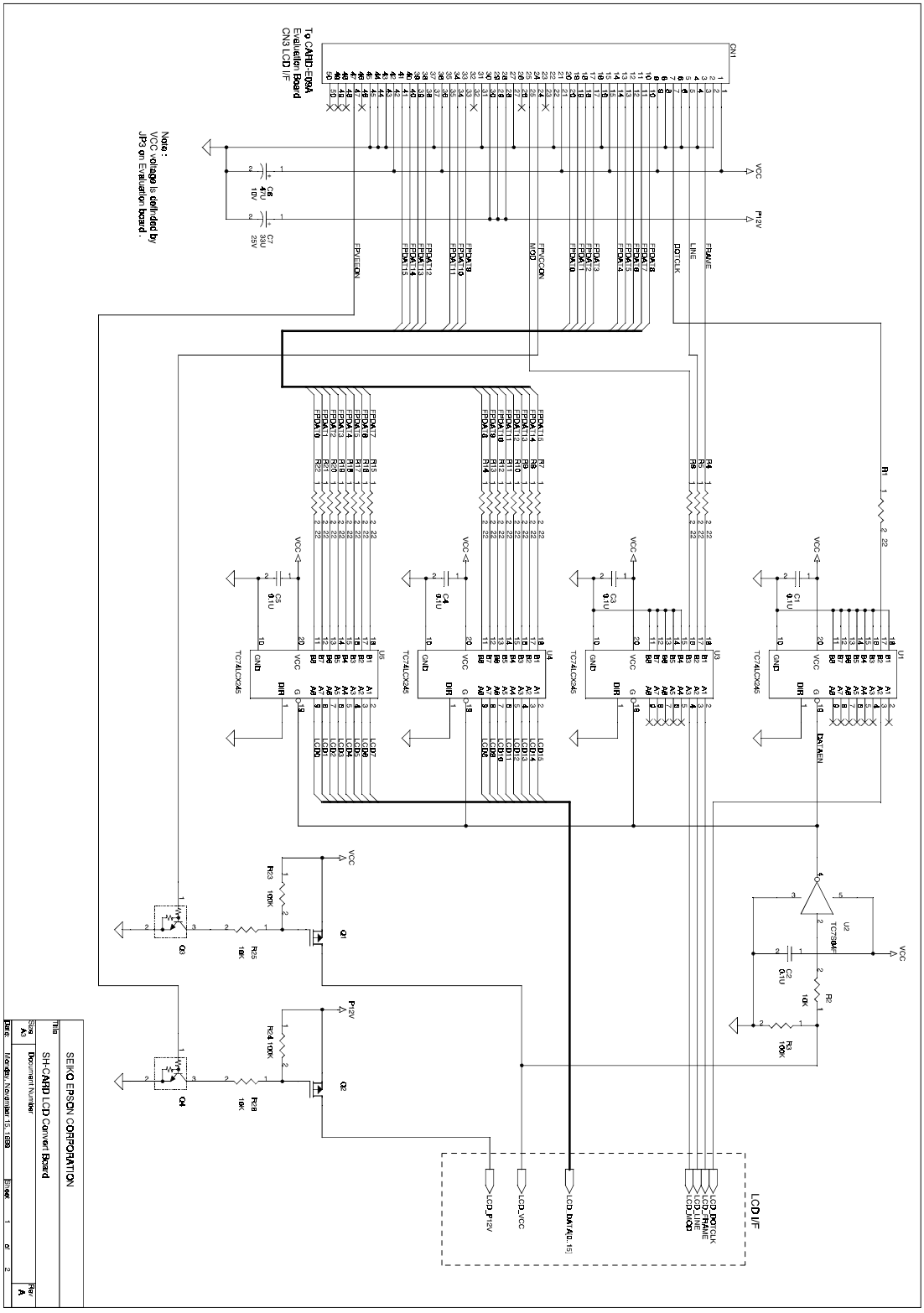
13.2.1.2.13 Sheet13 ; Buffer



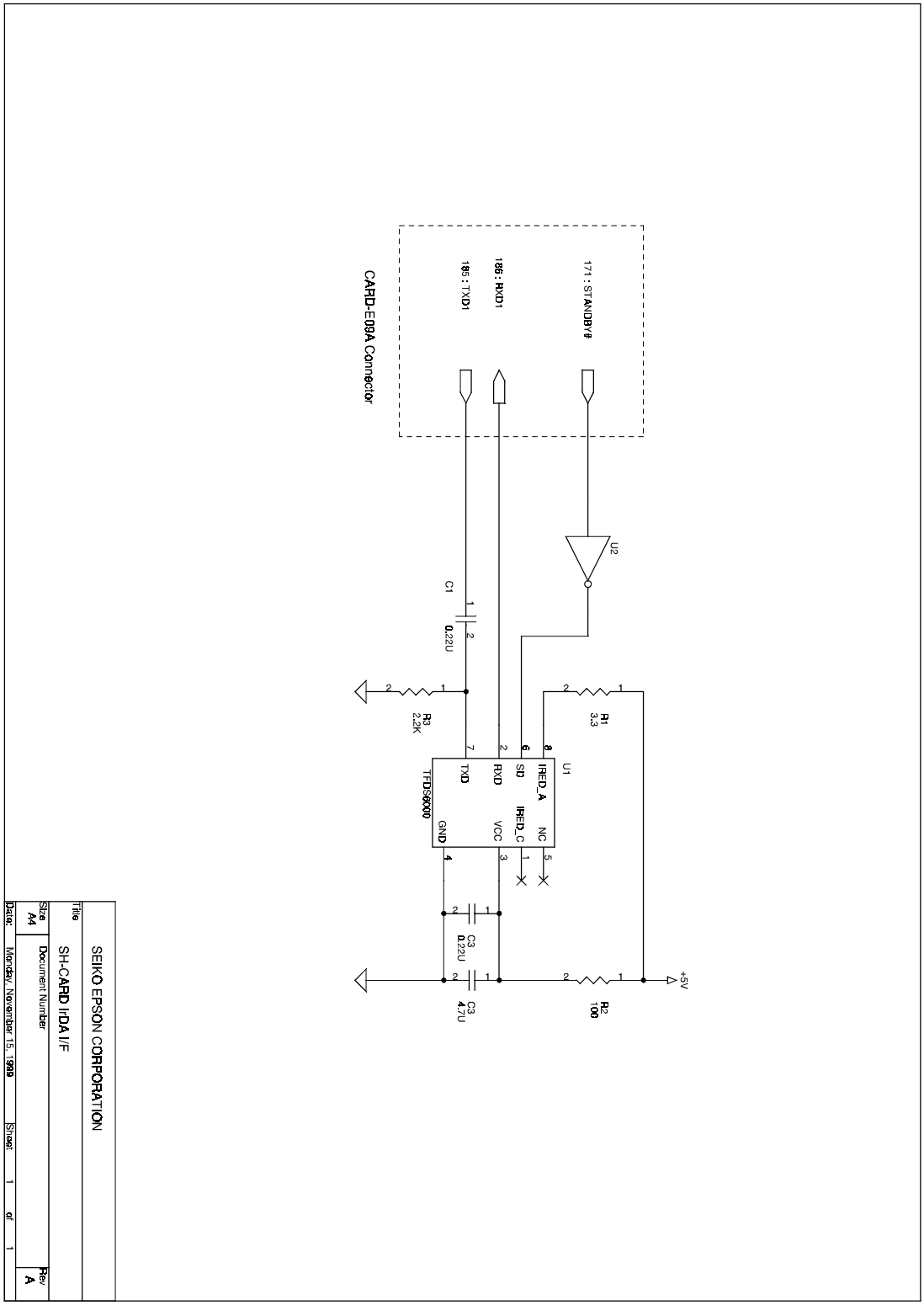
13.2.1.2.14 Sheet14 ; MISC circuit



13.2.1.3. LCD Interface



13.2.1.4. IrDA

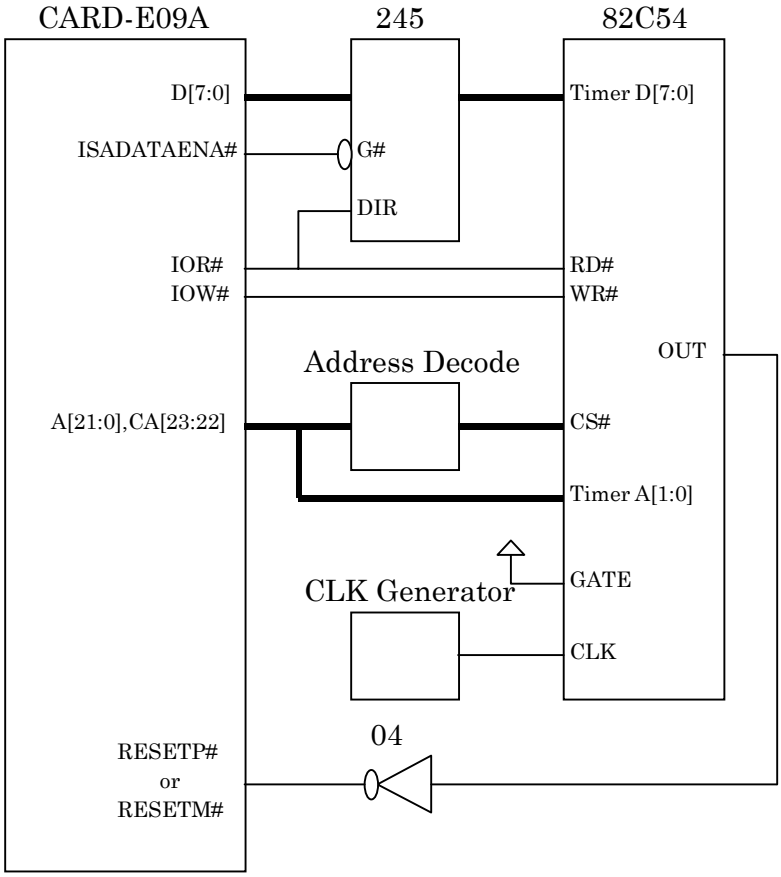

CARD-E09A Connector
185 : TXD1
186 : RXD1
171 : STANDBY#
U2
C1
0.22U
R3
2.2K
R1
3.3
U1
TFDS6000
TXD
RXD
SD
IRED_A
IRED_C
NC
VCC
GND
C3
0.22U
C3
4.7U
R2
100
+5V
SEIKO EPSON CORPORATION
Title
SH-CARD I/F
Size
A4
Document Number
Rev
A
Date: Monday, November 15, 1999
Sheet 1 of 1

13.3. Methods of Using a Watchdog Timer (WDT)

There are two methods of using a watchdog timer (WDT): by connecting an external circuit to the CARD-E09A ISA or SH bus, and by using the SH7709A internal function as it stands. When running Windows CE, because of the interaction between the OS thread switching time specifications and watchdog timer setting timing, the method of connecting an external circuit is recommended.

13.3.1. Method of Connecting an External Circuit

The following block diagram shows an example of a general-purpose timer (82C54) connected to the ISA bus.



In the above example, the OUT pin of the 82C54 is connected to the CARD-E09A reset pins (RESETP#, RESETM#), it can also be connected to the IRQ pin or NMI pin so that when a timeout occurs an interrupt is sent to the CPU. However, care is required, because if the interrupt controller has hung, the interrupt will not be accepted. And also note that for external expansion, a new port must be assigned for the additional timer.
In this case the watchdog timer is used as follows.

1) Set the watchdog timer.
2) The application software resets the timer before a timeout occurs, and restarts the timer.
3) If the software hangs, or for any other reason fails to reset the timer, then when a timeout occurs (counter overflow), the 82C54's OUT pin outputs an active high, and the system is reset. After this the timer continues counting.

This section has described an example using a general-purpose timer (82C54), but equally any commercially available microprocessor monitoring IC with a watchdog timer function (for example, Linear Technology's LTC692 or LTC693) can be connected. For details, refer to the data book for the IC under consideration.

On the other hand, without adding a timer to the external bus, it is possible to use the internal 8254-compatible timer of the CARD-E09A companion chip, but when a fault occurs it will not be possible to notify the fault outside the CARD-E09A, and as a result there will be cases that a system reset is not possible, so care is needed. This is because within the CARD-E09A the timer OUT pin is assigned to an interrupt (IRQ0) of the SH7709A together with other interrupt causes.

13.3.2. Method of Using the SH7709A Internal Function

The SH7709A internal oscillator circuit supports a watchdog timer function. For details, see the "SH3 Hardware Manual." This section describes an overview of using the SH7709A internal watchdog timer. A circuit for generating a reset is provided internal to the SH7709A, and therefore it is not necessary to add a reset circuit outside the CARD-E09A.

1) Set the watchdog timer.
2) The application software resets the timer before a timeout occurs, and restarts the timer.
3) If the software hangs, or for any other reason fails to reset the timer, then when a timeout occurs (counter overflow), then the type of reset (power on reset or manual reset) specified by the SH7709A RSTS bit is generated, and the system is reset. After this the timer continues counting.

In the above, it is possible to judge whether a reset was generated by the watchdog timer, normally this judgment can be made by looking at the SH7709A WTCSR register TME bit. However, when using the CARD-E09A loader, since the IPL (part of the loader) clears the relevant flag, the required reference is not possible. After the system has been reset, a decision as to whether this was due to the watchdog timer utilizes the following characteristic: an IPL manual reset does not clear memory; that is to say, files in RAM and the Windows CE Registry are preserved through a manual reset. The procedure is as follows.

Discriminating procedure whether a watchdog timer reset or not

1) In the application software the watchdog timer is initialized. At this point, the SH7709A RSTS bit is set to 1 (manual reset).
2) The application software creates an arbitrary file in RAM, or makes some setting in the Registry. The arbitrary file or Registry setting must be such as not to exist at a power on reset.
3) The application software regularly writes back zero to the SH7709A WTCNT at an interval shorter than the watchdog timer timeout time.
4) When a fault occurs, a manual reset is generated by the watchdog timer timeout, and the system is restarted.
5) After a restart, the application software checks RAM or the Windows CE Registry, to see if the file- or Registry setting is present. If it is present, the reset can be seen to have been caused by the watchdog timer, and if it is not present, the reset must have been from another cause.

The following is a coding example.

```
start of application program
if WDT registry value exists
    WDT timeout occured
else
    set WDT registry value
    set WTCNT = 0
    set WTCSR = 11100xxx (bin)      ;This starts the WDT.
                    ;TME = 1        (Timer enable)
                    ;WT/IT# = 1     (Watch dog timer mode)
                    ;RSTS = 1       (Manual reset)
                    ;WOVF = 0       (WDT overflow flag = 0)
                    ;IOVF = 0       (Interval timer overflow flag = 0)
                    ;CKS = x        (Clock select = user selection)
    application program main routine (set WTCNT to 0 periodically)
endif
end of application program
```

Notes on Operation

The maximum interval that can be set for the watchdog timer is about 30 ms. This is because the peripheral clock (PΦ) is set to one-fourth of the CPU clock (133 MHz) frequency (133 MHz/4 = 33.25 MHz = 30 ms). For details, see Chapter 9, "Internal Oscillator Circuit" of the "SH3 Hardware Manual." If the application software cannot clear the watchdog timer within this interval, then a reset is generated even if there is no fault.

In particular, for Windows CE, thread switching is done at 25 ms, and therefore however the application software is arranged, the possibility of this occurring is quite high. In cases where this problem cannot be avoided, in place of the SH7709A internal watchdog timer, it is necessary to add an external timer to the CARD-E09A ISA bus or SH bus.

13.4. Temperature Measurement Sample Data

13.4.1. Measurement System Configurations

CARD-E09A	133MHz/32MB
PCB	EVALUATION BOARD (SCE88J1B01)
Disk	CompactFlash Card 45MB (Boot Disk) ATA CARD 75MB
Monitor	MF-5015A (IIYAMA)
KB	RT6672T JP (NMB TECHNOLOGY INC.)
MOUSE	
Power	AT power supply
CASE	PAC-100 (ACQUIRE) ; 230 × 405 ×175 mm
RECORDER	MODEL 3081 (YOKOGAWA)
Conditions	Continuous operation of any application software under Windows CE 2.11/Japanese
Power Voltage	+5.00V +12.0V +3.30V ± 0.15V (generate by linear regulator on evaluation board) +1.90V ± 0.10V (generated by linear regulator on evaluation board)

13.4.2. Measurement Conditions

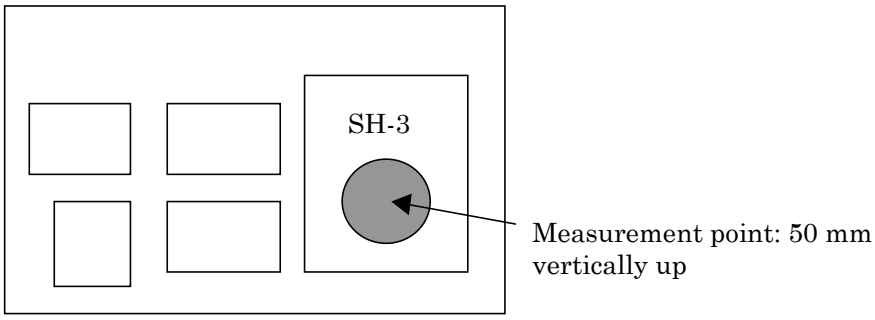
Under the following conditions, the ambient temperature over the SH7709A (Ta1), and the temperature between the CARD-E09A and the evaluation board (Ta2) were measured.

- Definition of measurement points

  The measurement points for Ta1 and Ta2 are shown below. Since both are environmental temperatures, precise positions are not specified.

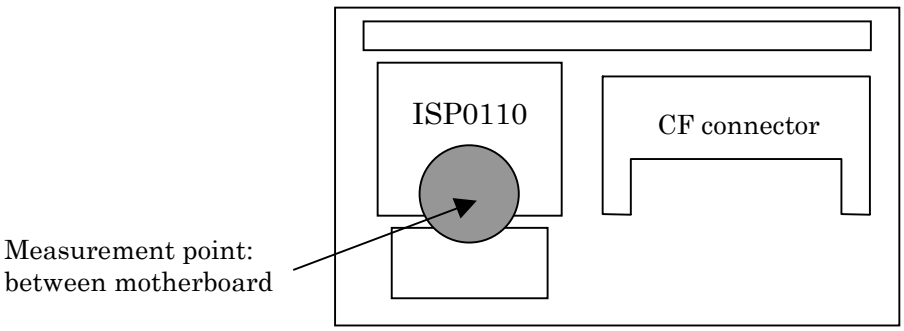
  Ta1 measurement point

  Component surface of CARD-E09A, 50 mm above SH7709A



  Ta2 measurement point

  Solder surface of CARD-E09A (connector side), between companion chip (ISP0110F0A) and motherboard



- The CARD-E09A is attached with the compact Flashcard, and connected to the evaluation board. The evaluation board is installed horizontally within the case.
- All openings in the case are sealed with tape, so that there is absolutely no ventilation within the case.
- In the above state the whole is placed in a constant-temperature chamber, and left for an adequate time, after which Ta1 and Ta2 are measured.

13.4.3. Measurement Results

The temperature measurement data obtained in the unventilated state is given below.

Ambient temperature	Ta1	Ta2
29.7°C	46.2°C	33.3°C
52.6°C	67.5°C	53.9°C

The current consumption does not depend on the SDRAM capacity. Thus although the measurements here were made only for a CARD-E09A with SDRAM = 32MB, the above measurement data is also valid for a card with SDRAM = 16 MB. In any event, this data should be used only as a guideline.

13.4.4. Cautions

This measured values are only for a reference. When designing the system, be sure to measure the temperatures of CARD-E09A and other devices inside the system during actual operation, and make sure they meet the operating temperature specifications.

Circuit layout must be made ensuring that a heat source such as a linear regulator is not close to the CARD-E09A.

13.5. MTTF (Mean Time To Failure)

From the failure rates of the electronic components mounted on the circuit board and the connections (including solder), allowing a factor-of-two safety margin, the MTTF for the CARD-E09A is as follows:

With Ta = 25°C, MTTF = 490,000 hours

Note that if the CARD-E09A fails, repair is not envisaged, so no MTBF (Mean Time Between Failures) is defined.

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone : +1-310-955-5300 Fax : +1-310-955-5400

SALES OFFICES
West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone : +1-408-922-0200 Fax : +1-408-922-0238

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone : +1-815-455-7630 Fax : +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone : +1-781-246-3600 Fax : +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone : +1-877-EEA-0020 Fax : +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Muenchen, GERMANY
Phone : +49- (0) 89-14005-0 Fax : +49- (0) 89-14005-110

- GERMANY -
SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone : +49- (0) 217-15045-0 Fax : +49- (0) 217-15045-10

- UNITED KINGDOM -
UK BRANCH OFFICE
2.4 Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone : +44- (0) 1344-381700 Fax : +44- (0) 1344-381701

- FRANCE -
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone : +33- (0) 1-64862350 Fax : +33- (0) 1-64862355

ASIA

- CHINA -
EPSON (CHINA)CO.,LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing,CHINA
Phone : 64106655 Fax : 64107320

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone : 21-6485-5552 Fax : 21-6485-0775

- HONG KONG, CHINA -
EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone : +852-2585-4600 Fax : +852-2827-4346
Telex : 65542 EPSCO HX

- TAIWAN -
EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287,Nanking East Road, Sec. 3
Taipei, TAIWAN
Phone : 02-2717-7360 Fax : 02-2712-9164
Telex : 24444 EPSONTB

HSINCHU OFFICE
13F-3, No.295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN
Phone : 03-573-9900 Fax : 03-573-9169

- SINGAPORE -
EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone : +65-337-7911 Fax : +65-334-2716

- KOREA -
SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-Dong
Youngdeungpo-Ku, Seoul, 150-010, KOREA
Phone : 02-784-6027 Fax : 02-767-3677

- JAPAN -

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
Card Products & Marketing Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-7503 Fax: +81-(0)42-587-8423

ED International Marketing Department I
(Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

In pursuit of "Saving" Technology, Epson electronic devices. Our lineup of semiconductors, liquid crystal displays and quartz devices assists in creating the products of our customers' dreams.
Epson IS energy savings.

CARD-E09A
Application Note

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Devices Information on Epson WWW server
http://www.epson.co.jp/device/

First issue December,1999
Printed February,2000 in Japan Ⓟ A