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Technical Note

Oscillator Jitter and How to Measure It

Introduction

Jitter is a term that is becoming widely known in working with high-speed designs. Jitter is also a term that causes much confusion. Microprocessor or microcontroller based parts have requirements for their input clocks. One of the requirements that is often listed these days is jitter. A part will specify that it has a certain jitter tolerance that needs to be met for optimum performance.

When choosing a clock oscillator, this jitter requirement has to be taken into account. Some oscillator manufacturers specify a maximum jitter for their oscillators. A jitter specification is not the easiest number to put down on paper. Jitter will vary with frequency and load conditions. Many vendors do not specify jitter because of these variables.

It is important to understand how to measure oscillator jitter. A correct measurement of jitter will determine whether or not an oscillator can be used in a specific design. Before we can understand how to measure it, we must first understand what jitter is.

Jitter

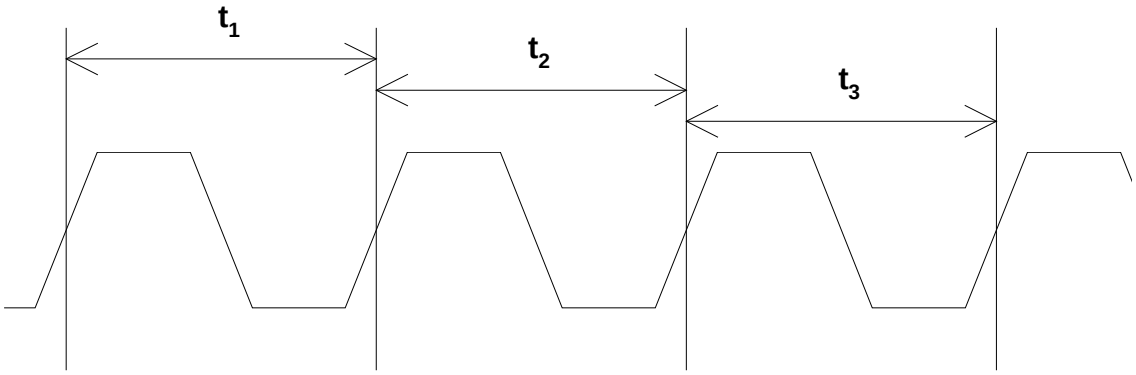
Jitter is noise. Noise in an oscillator comes from different sources. Both the crystal and the amplifier in the oscillator have some inherent noise. This noise gets amplified by the amplifier and appears on the output as jitter. These random types of noise have a uniform or Gaussian distribution.

A major contributor that adds to oscillator jitter is power supply noise. Coupling of the power supply into the input of the amplifier of the oscillator will dramatically increase the jitter on the output. This jitter is not random. It is important to make sure that power supply noise is filtered out properly.

There are different ways to define jitter. Jitter can be expressed in the frequency domain as phase noise. In the time domain, we define jitter as any deviations of a clock's output transitions from their ideal positions. Jitter is specified in three ways. Many times these jitter specifications are confused. Each jitter type is spelled out here.

Cycle-Cycle Jitter

Cycle-cycle jitter is the deviation between one rising/falling clock edge to the next rising/falling clock edge. In this case, consecutive cycles are being measured. A number of consecutive cycles are measured and the maximum difference is the cycle-cycle jitter.



$$\text{Cycle-Cycle Jitter} = \text{Max}[(t_2-t_1), (t_3-t_2),\ldots,(t_n-t_{n-1})]$$

Figure 1 Cycle-Cycle Jitter

Cycle-cycle jitter is important when using a PLL (Phase Locked Loop). If a clock oscillator is feeding a PLL and the cycle-cycle jitter is too high, the PLL may not be able to keep lock.

Period Jitter

The next type of jitter, period jitter, is the maximum change of a clock's rising/falling edge. This is also referred to as peak-peak jitter.

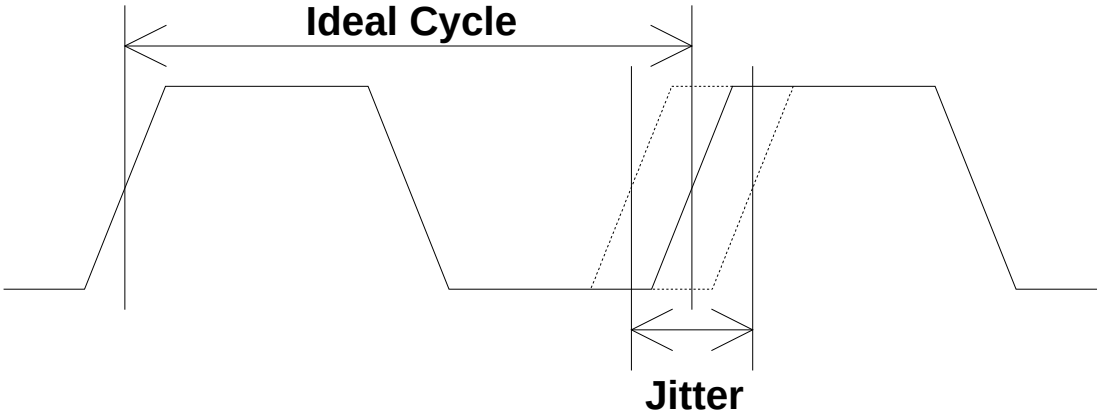


Figure 2 Period Jitter

In comparison to cycle-cycle jitter, period jitter does not look at consecutive cycles. Period jitter is worst case jitter. When dealing with setup and hold times, this jitter spec is critical.

Long-Term Jitter

Long-term jitter looks at the deviation of a rising/falling edge "N" cycles after the first rising/falling edge. The maximum deviation is the long-term jitter.

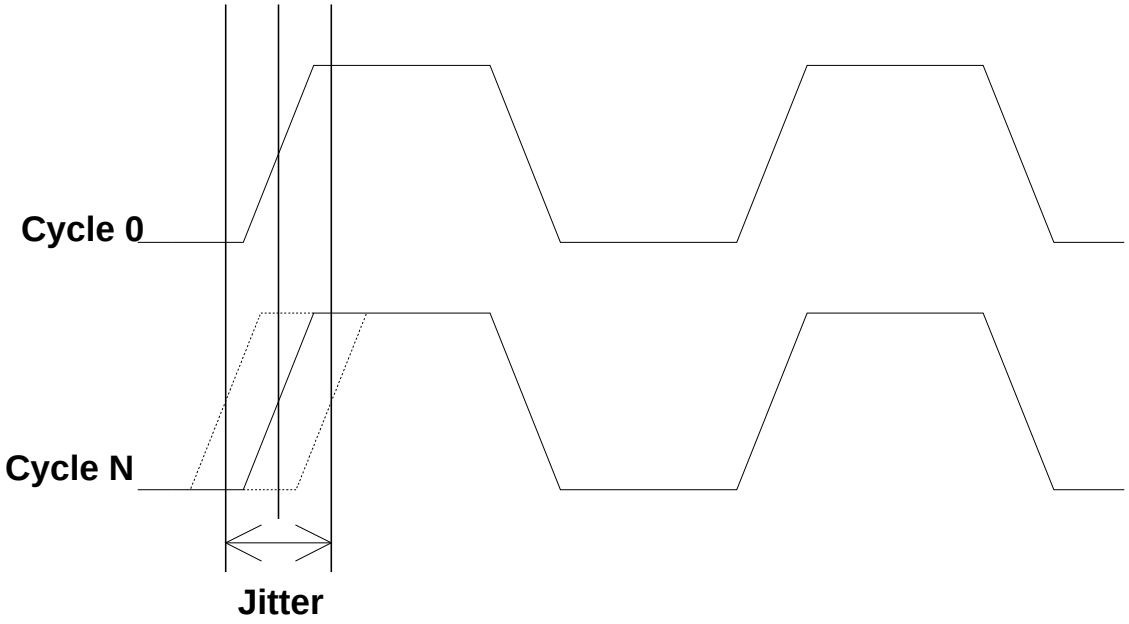


Figure 3 Long-Term Jitter

Long-term jitter is important for graphics applications. Long-term jitter can lead to picture instability.

Jitter Measurement Considerations

Now that jitter has been defined, we can look at how to measure it. Measuring jitter can be done with a Digital Storage Oscilloscope (DSO). There a few factors that need to be considered when choosing a DSO to make accurate jitter measurements. These factors are analog bandwidth, time interval resolution, and intrinsic jitter.

Analog Bandwidth

The DSO must be able to measure all of the frequency components of the signal. There is a common rule of thumb that says the analog bandwidth of the DSO should be five times that of the signal being measured. A 100 MHz signal would require a DSO with at least a 500 MHz bandwidth.

Time Interval Resolution

This is also referred to as sample rate for a DSO. The higher the sample rate the better the timing resolution that can be obtained. Most DSOs today have an 8 bit real-time A/D converter that can sample up to 5 GHz or 200 Pico-seconds per point. A second rule of thumb says that the sample rate should be 5 times the analog bandwidth of the signal.

Intrinsic Jitter

The DSO has some jitter already associated with it. This intrinsic jitter needs to be known so that it can be calculated out of the total jitter measurement. Some manufacturers specify the intrinsic jitter. If it is not specified, it can be measured.

Measuring the intrinsic jitter can be done by measuring the trigger jitter of the DSO. This requires a low jitter signal source or a fast rise time pulse. The DSO should be set to trigger on the rising

edge of the signal. Use the infinite persistence function of the DSO to collect waveforms. Several hundred waveforms should be collected. Then measure the width of the persistence waveform's rising edge. This can be done by using cursors or by using a histogram function (if your DSO has one).

When making a jitter measurement the intrinsic jitter of the DSO must always be calculated out of the equation:

$$\text{Jitter} = \sqrt{\text{Jitter}_{\text{Meas}}^2 - \text{Jitter}_{\text{Scope}}^2}$$

Jitter Measurement

With the measurement considerations understood, let us take a look at measuring each type of jitter.

Cycle-Cycle

Measuring cycle-cycle jitter is not the simplest measurement to make with a DSO. A cycle-cycle jitter measurement requires that consecutive cycles be captured and measured. A typical instrument that is used is a Timing Interval Analyzer (TIA). A TIA can make this measurement very handily. The TIA looks at the signal and measures the difference of time periods over consecutive cycles. The maximum difference over multiple cycles is the cycle-cycle jitter.

TIAs are hard to come by because they are not made anymore. Most engineers do not have a TIA in their lab, but do have a DSO. A DSO can be used along with a software routine to simulate a TIA. Tektronix has a software application that is internal to their TDS 500/600/700 DSOs. The software application (TDSJIT1) takes the sampled data of the DSO and makes a cycle-cycle jitter measurement, Figure 4. A similar software application can be written for any DSO.

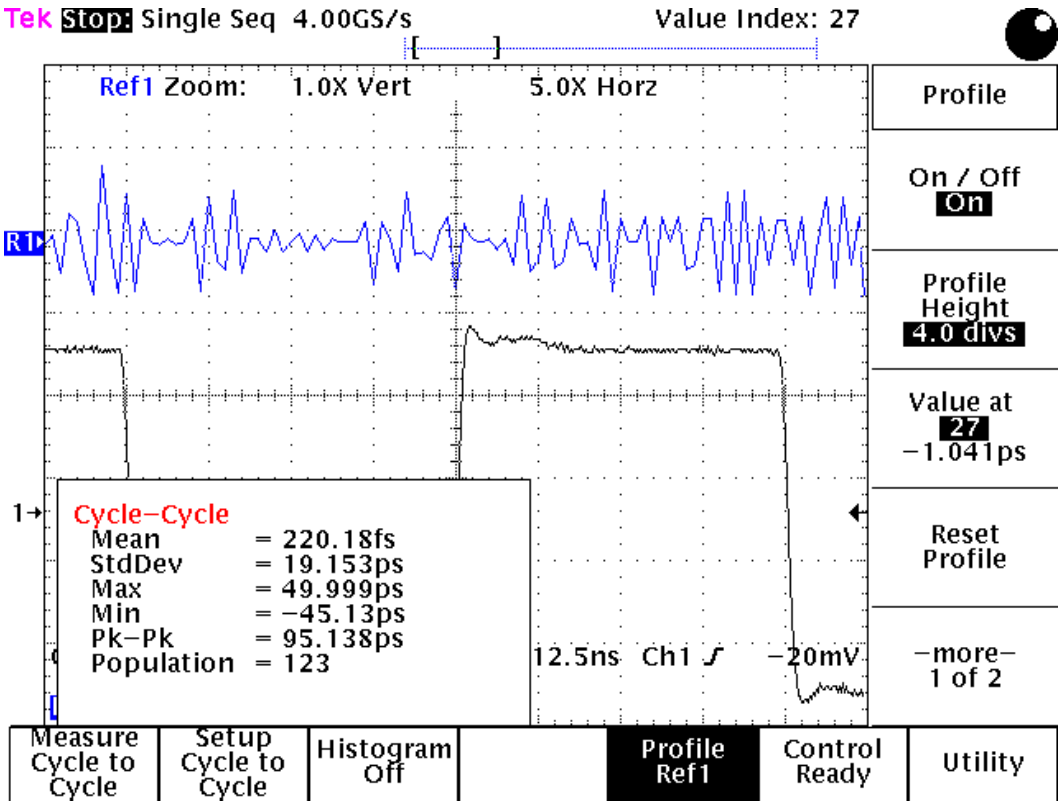


Figure 4 Tektronix TDSJIT1

The worst case cycle-cycle jitter can be determined by making a period jitter measurement. The period jitter measurement will be described in the next section. While the period jitter measurement is not looking at consecutive cycles, it will at least give an idea as to the cycle-cycle jitter. If the period jitter measurement does not exceed the jitter specification, chances are the cycle-cycle jitter measurement will not exceed the specification.

Period Jitter

Period jitter is a straightforward measurement with a DSO. The DSO is used to trigger on the rising edge of the signal. The jitter is then measured on the next rising edge. The infinite persistence function is used to accumulate waveforms. If the histogram function is available, it can be used along with a Pk-Pk (Peak-Peak) measurement. Of course cursors can be used to measure the width of the persistence accumulation, if a histogram function is not available.

Another way to predict period jitter is to use statistics. Most DSOs today have histogram functions and statistical measurements. The same procedure described previously is used to capture the signal. Figure 5 shows the measurement being made.

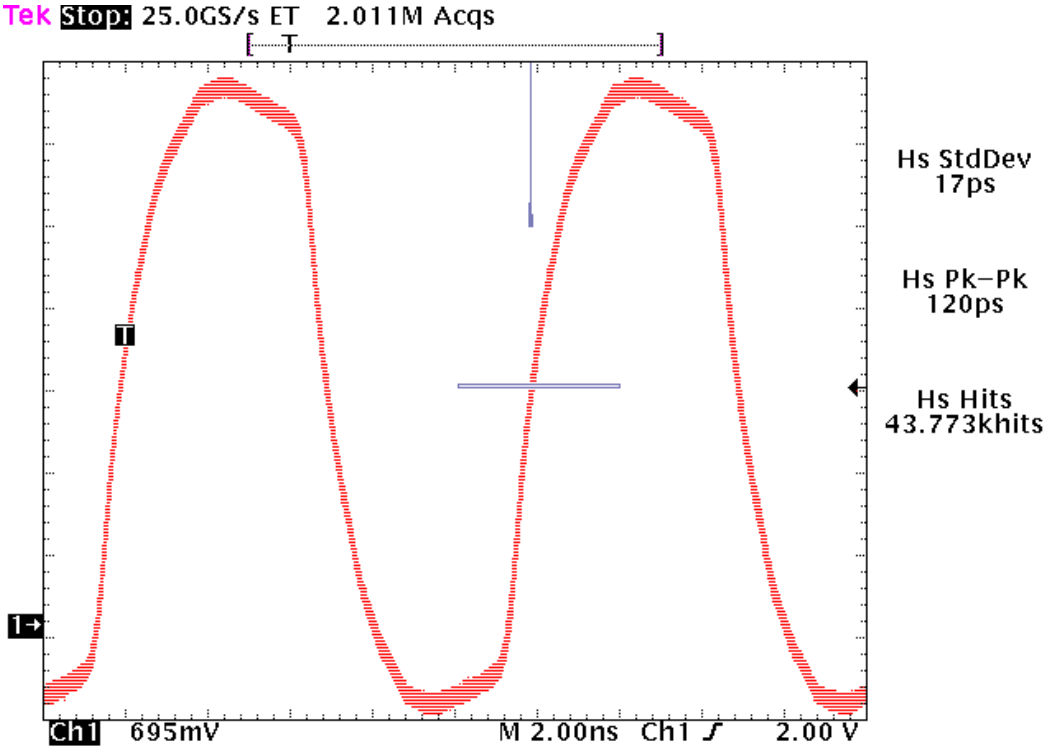


Figure 5 Period Jitter Measurement with Histogram

Using the StdDev (Standard Deviation) measurement, period jitter can be predicted. The standard deviation is 1 sigma. Since the jitter follows a Gaussian distribution, looking at a probability table will give us the confidence levels for various values of sigma.

Sigma	Probability
1	68.26%
2	95.45%
3	99.73%
4	100% - 6.334 x 10^{-3}%
6	100% - 1.973 x 10^{-7}%
8	100% - 1.244 x 10^{-13}%

10	100% - 1.524 x 10^{-21}%

Table 1 Probability

For a 99.9999998027% confidence level, or 6 sigma, the jitter is +/-17 * 6 ps = 102ps. Using a confidence level of 8 to 10 sigma will give a robust number of the period jitter.

Long-Term Jitter

Measuring long term jitter is similar to measuring period jitter. A DSO with a delayed time base is what is required. The DSO should trigger on the rising edge of the signal. Then use the delayed time base feature to look at the signal a number of cycles later. The delayed edge should then be measured for jitter using the same procedure as the period jitter measurement.

Conclusion

Jitter is a specification that is becoming more prevalent. Whether it is a digital design or a data communication system, jitter plays a part in the performance. Clock oscillators that drive these designs will need to have acceptable amounts of jitter. Being able to accurately measure and characterize oscillator jitter is key factor in these designs.