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Technical Note

Techniques for Noise Reduction in the Circuit around the Oscillator

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SEIKO EPSON CORP.

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1. Purpose and Scope

The circuit around a crystal oscillator is generally operating at the fastest speed of the board. Therefore, the circuit produces noise. So, the design of the circuit around the crystal oscillator must be considered carefully from the point of the design of its digital circuit. This document explains the theory of noise generation and noise reduction techniques.

2. Types of Noise

Figure 1. shows the general model of the circuit around the crystal oscillator. The noise can be separated into three noise sources. These are as follows:

(1) Power Line
(2) Clock Line
(3) Crystal Oscillator

Generally, the noise comes from these three sources.

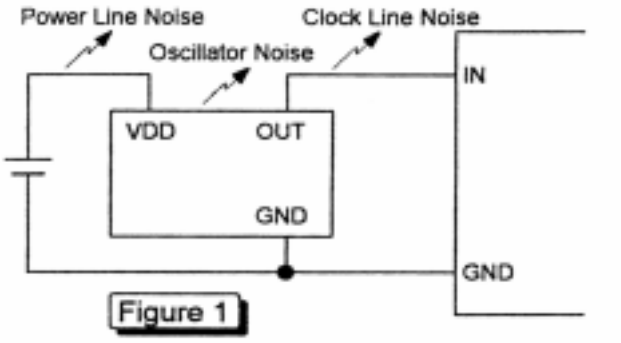

Figure 1

2.1. Power Line Noise

While the crystal oscillator is operating an oscillator leaks ripple noise to a power line. Then the power line radiates this ripple noise like an antenna.
Power line noise can be reduced by preventing or absorbing ripple noise leakage from the oscillator. So, by reducing ripple noise from the oscillator, it will in turn reduce the noise generated from the power line.

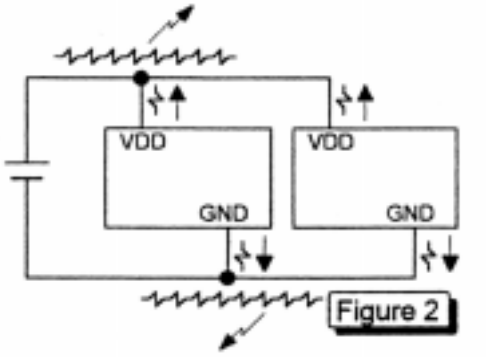

Figure 2

2.2.Clock Line Noise

Clock line noise is generated from a clock line on the Board, The clock signal of the oscillator is placed on the clock line. This clock line will generate noise. To reduce clock line noise, we must... 1) lesson the noise generated by the clock waveform, and 2) ensure that the clock line itself does not radiate noise.

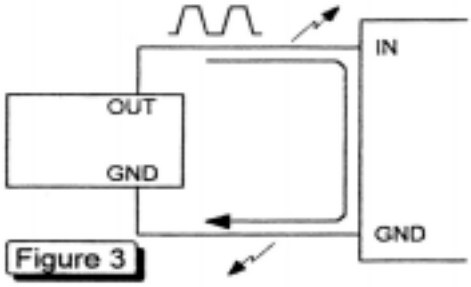

Figure 3

2.3. Crystal oscillator Noise

Crystal oscillator noise is generated from the IC, lead frame and bonding wire inside the oscillator.
In order to reduce this noise the oscillator must be driven with a stable power source and have a clean output (ideally, no noise on the output). In principle this is the same as power line and clock line noise reduction.

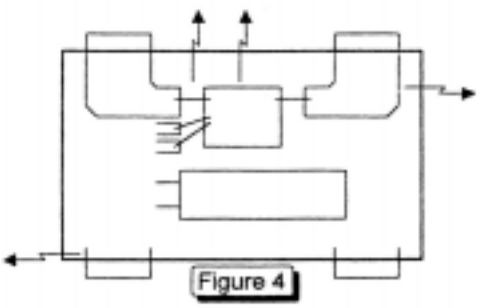
Figure 4

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2.4. Noise Volume of Each Noise Source

The amplitude of noise radiation is proportional to the current and its own current loop. The amplitude of radiation increases when a large thru current is used and when a large current loop is present on the board.

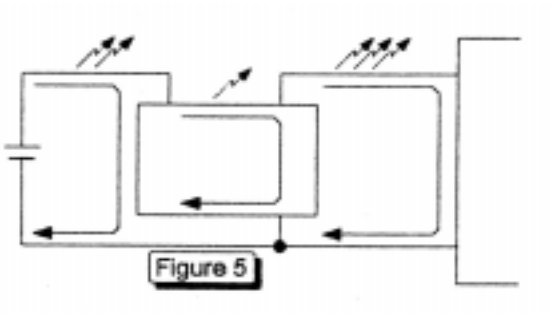
Figure 5

Thru - current size of each noise source has the following relationship:

Power Line = Oscillator > Clock Line

Size of the current loon noise source has the following relationship:

Clock Line > Power Line >> Oscillator

So, with regard to the noise volume of the circuit around the oscillator; clock line noise is the largest, power Line noise is second and oscillator noise volume is very small compared to the other two.

3. Noise Reduction

For noise reduction of the circuit around the oscillator, the following three ways are the suggested basic techniques:

(1)Ensure that you have good power and a good ground
(2)Put a filter in for power line noise
(3)Use acceptable design guidelines for clock line traces on the PCB

3.1. Power and Ground

A definition of good power and good ground means a conductor that has a very low impedance on a wide frequency and has the same voltage level at any point. Specifically, the ground must be stable because the ground is referenced by all components.

To put it simply power and ground traces should be wide in size and have no bottle - necks. In the case of multi-layer boards, design power and ground planes on independent layers. If there are some connections to be made, please keep connection space as wide as possible keeping a low impedance condition with wide frequency bandwidth.

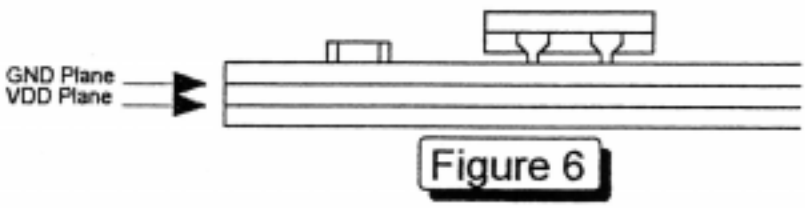

Figure 6

3.2. Power Line Noise Filter

After designing an acceptable power and ground, the next step is designing a filter circuit on the power line in order to prevent noise leakage generated from the oscillator and noise entering the oscillator from other devices.

Generally, the following ways are used in this filter circuit:

(1) By-pass Capacitor
(2) LC Filter

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3.2.1.Using a By-pass Capacitor

A by - pass capacitor absorbs power line noise and is a filter that has a very simple construction. This is a basic method of noise reduction. Usually, most noise problems can be solved by using a by-pass capacitor with the correct value and proper placement.
The following is a guide for correct value and board placement..

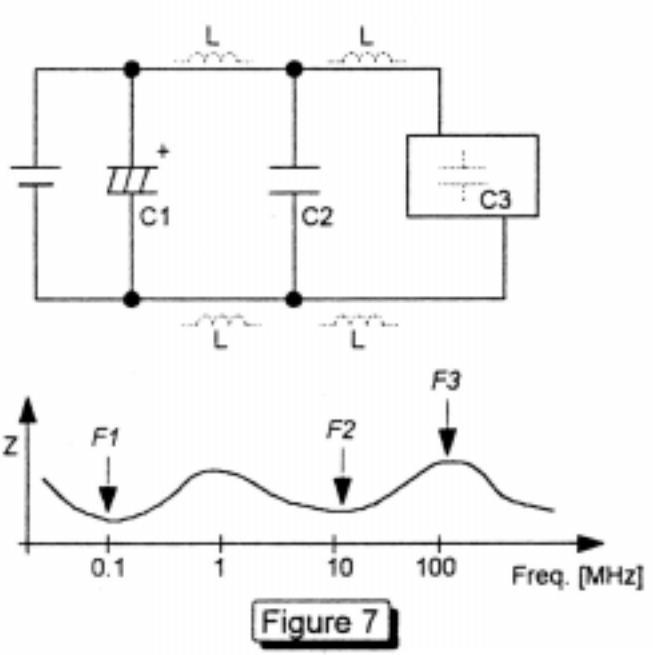

Figure 7

Capacitance size:

Usually a by-pass capacitor typically used has a value of 0.01 μF through 0. l μF. However, this value must be chosen to keep a low power line impedance condition between VDD to GND terminals of the oscillator. This impedance condition should be sufficient to cover up to 3 times the base frequency for the oscillator.
Larger capacitance has high impedance with higher frequencies, therefore it is unable to reduce high frequency noise.
The use of smaller capacitance will tend to reject lower frequency noise. The following is a guide to approximated capacitance for each frequency range:

$$F1=\frac{1}{2\pi\sqrt{4LC_1}}$$

$$F1=\frac{1}{2\pi\sqrt{4LC_2}}$$

$$F1=\frac{1}{2\pi\sqrt{4LC_3}}$$

Frequency	Capacitance
1MHz to 20MHz	0.1μF
20MHz to 40 MHz	0.047μF
40MHz to 70MHz	0.01μF

Mounting a by-pass capacitor:

The by-pass capacitor has to be mounted as close as possible to the oscillator. A long line produces higher impedance on high frequency due to larger stray inductance. In order to reduce this stray inductance, using a chip capacitor will provide a solution.
Figure 8 shows an example of the print pattern layout. Please place a by - pass capacitor before connecting the power line. The noise leakage from the oscillator will definitely pass through the by - pass capacitor. Therefore it should produce a good noise reduction.
Additionally please avoid to place a by-pass capacitor as like figure 9 - a). A high frequency noise generally runs straight. Therefore this placement will not reduce noise from power line. We recommend to place a by - pass capacitor as in figure 9-b).

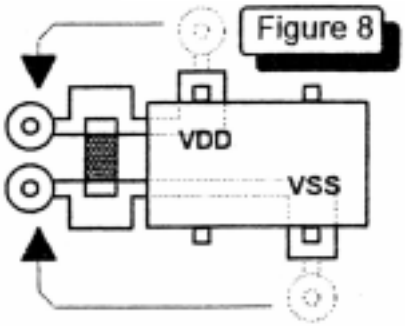

Figure 8

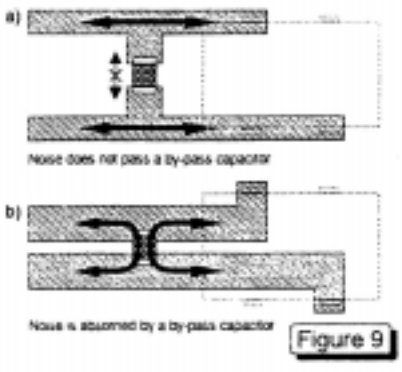

Figure 9

3.2.2. Using a LC Filter

The use of an LC filter produces a higher noise reduction effect than that of the by - pass capacitor. The L (inductance) reduces power line noise, the C (capacitance) absorbs noise. Usually, inductance is gained by using ferrite beads. The capacitance value chosen is usually the same as that of the by-pass capacitor. (see 3.2.1)

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However, please take care to choose an inductor that has a high Q factor; it's resonance characteristic should be sharp and show high gain for it's resonance frequency. With that, it is possible to eliminate slight oscillation in the LC circuit. This LC circuit will and can affect the power line.

3.3. Stable Clock Line

A stable clock line means the line can transmit an oscillator output to the load device accurately without disturbing a waveform and with no radiation noise from the line.

A basic way to get a stable clock line is; first, we must try to keep the critical characteristics of the waveform intact. Items such as Tr, Tf, tOH and tOL should have no major changes. In addition to that, needless signals such as overshoot, undershoot, ringing and reflection should be minimized. Seconds this clock line will act as an antenna. So the transmission for noise from this antenna should be as low as possible.

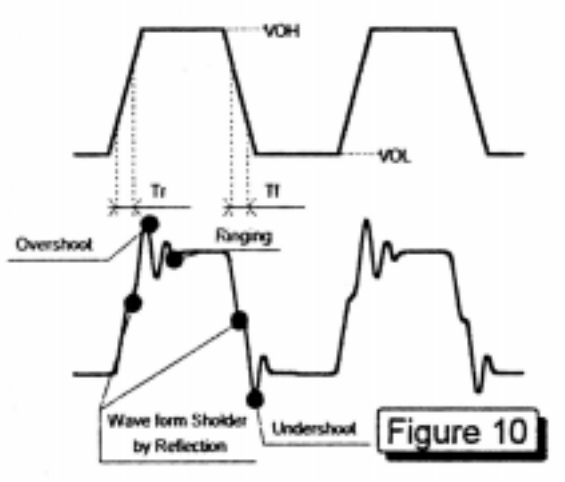

Figure 10

There are four basic methods of avoiding wavefom1 distortion:

(1) Series Resistor
(2) Termination Resistor
(3) Filter
(4) Matching the Impedance of the Clock Line

Additionally, there are two basic techniques to produce a low radiation line:

(5) Shorter Clock Line
(6) Smaller Current Loop

3.3.1. Using a Series Resistor

Generally, the clock line produces waveform distortion such as overshoot, undershoot and ringing. They must be reduced because they include frequency elements approximate 3 to 7 times the oscillation frequency. These higher frequencies will tend to cause EMI problems and should be eliminated.

A series resistor is used in order to reduce them. The series resistor must be placed in series between the oscillator and clock line as in Figure 11 . The value of the resistor should be chosen so that the total impedance of the oscillator and series resistance added are equal to the impedance of the clock line. 20Ω For example, an EPSON crystal oscillator has to 40Ω.

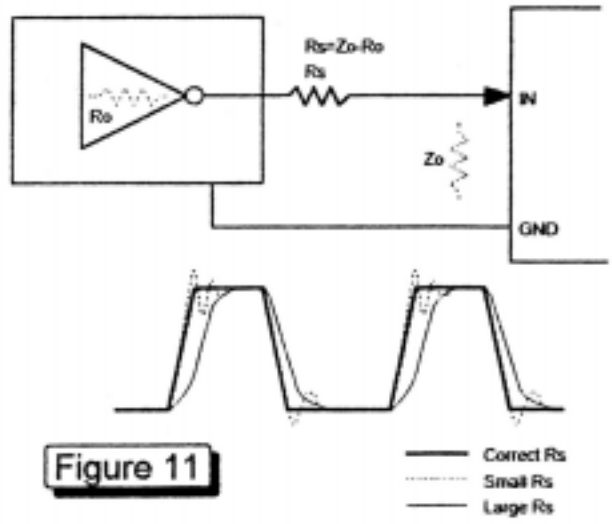

Figure 11

General digital circuits have approximately 60Ω to 100Ω. So, the series resistance will be 40Ω.

The actual series resistance can be determined by testing. To determine the series resistance that needs to be added, you must monitor the output of the oscillator with an oscilloscope while increasing the add-in series resistance. When overshoot, undershoot and ringing are minimized, the correct value of resistance has been found.

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3.3.2. Using a Termination Resistor

The clock signal is disturbed by reflection at the load device input if the clock line impedance and load device input impedance are not matched. The reflection waveform will overlap the running waveform, then the waveform wi11 show distortion. This distortion produces high frequency noise.

This waveform distortion may cause to trigger error if the clock line is used for multiple devices. Therefore this noise must be avoided.

In order to avoid a reflection from the load device input place a termination resistor which has the same resistance as the clock line to match the impedance. Please refer to Figure 12 that shows the separated resistor termination and AC termination.

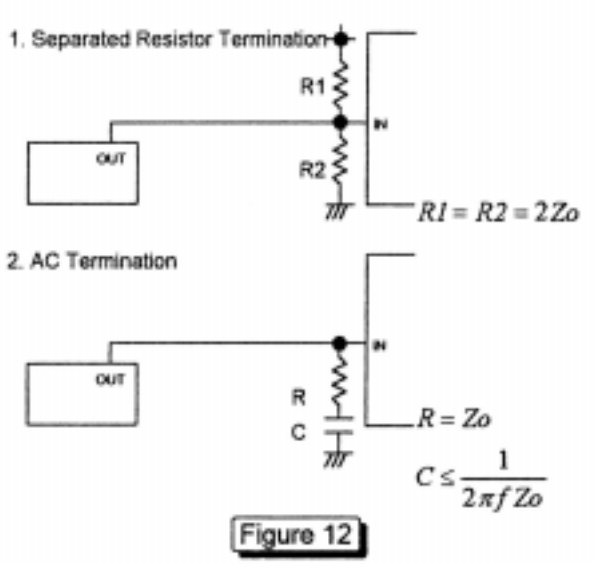

Figure 12

3.3.3. Using a Filter

Usual1y providing series resistance and/or a termination resistor will fix noisy wave forms. If the problem is not solved by these methods, we suggest using a filter. The filter will work effectively to reduce high frequency noise. However, it also affects the wavefom by making it dull (large Tr and Tf). Therefore please choose a filter that will satisfy your Tr and Tf specification. Please be careful when the filter chosen has a large capacitance, it may cause more radiation of noise due to the consumption of increased current.

3.3.4. Matching the impedance of the Clock Line

Please keep the clock line impedance as stable as possible in order to reduce reflection on the clock line.

In order to have a stable clock line impedance, please use 45° bends or round shapes instead of 90° bends. Please avoid using T - type branch-off and through holes.

In the case of driving multiple devices with only one oscillator, please use the suggested trace pattern given in upper of Figure 13 that distributes clock using same length from a trunk line and also terminate this pattern by the use of resistors on the end of the line as shown. With this suggested pattern, it is possible to distribute good wave forms to each device.

However this method may produces phase difference for between the near load device and far load device from the oscillator. If this does not acceptable in your board, please use the middle trace style of Figure13 that distributes clock signals using same 1ength line from a blanching point, but this trace style makes long total line. If the line is difficult to trace shortly on the board, we recommend to use the clock driver for each line, see the lower of Figure 13. Using this, the each clock line length can be designed to

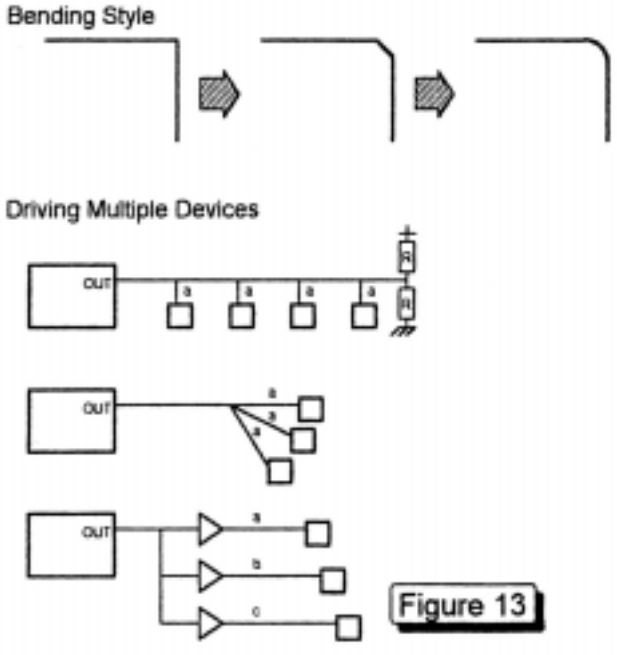

Figure 13

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different. If the long line is produced in either clock driver input and/or output, please put the terminations mentioned above.

3.3.5. Shorter clock Line

The Clock line will radiate noise the easiest. Therefore the printed pattern layout must be of first priority in order to ensure that it is the shortest and has the best impedance stability. In these clock lines, there are stray capacitance's and inductance's that are present. This LC circuit will create some noise in the clock line. The use of a shorter line moves the resonance frequency of the LC higher. Basically, the clock signal contains several frequency elements. By the use of a short line, higher frequency elements are made small. Then, total radiation noise is reduced.

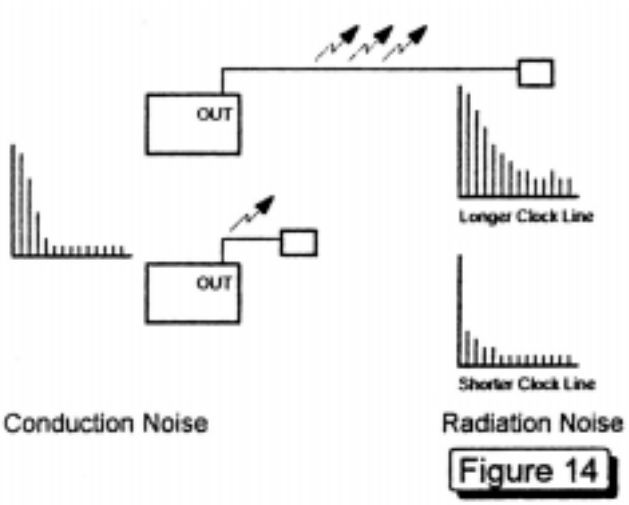

Figure 14

3.3.6. Smaller Current Loop

The noise radiation level is proportional to the current loop size. Therefore please make the shortest clock line and ground line between the oscillator and load device. Please see Figure 15. The best way to design this is to place the ground plane on the opposite side of the board.

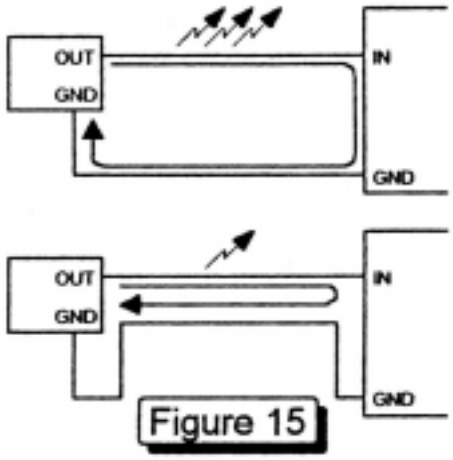

Figure 15

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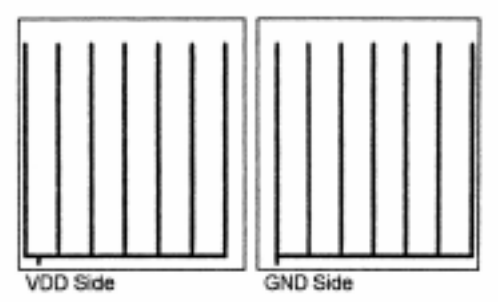
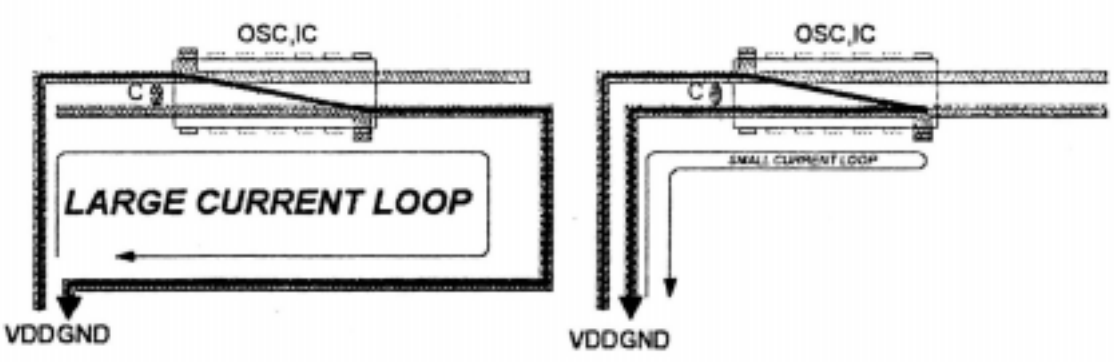
Appendix A. Power Line Desigh on the Board

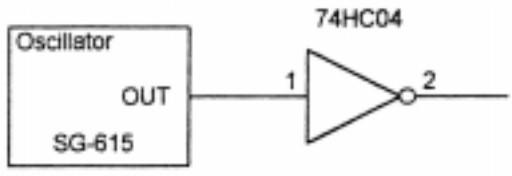
In the case of using a dual-surface board, it is easier to achieve a longer current loop than on a multi - layer board. Please make your power line on the board referring to the following:

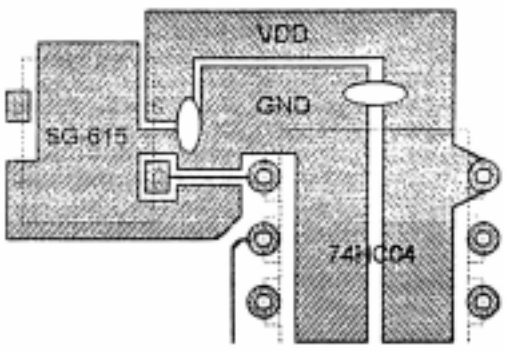


If the power lines (VDD and GND) are supplied from alternate sides, it will produce a large current loop. In order to minimize the current loop size, please supply the power sources from the same side. Please look at the following figure that shows how using the same side power lines can minimize the current loop size. This power line design also produces effective operation of the by - pass capacitor in that the current including noise will definitely pass through it. So this absorbs both noise from other devices and noise generated by the oscillator.



The following shows an example of the circuit when crystal oscillator SG - 615 drives an inverter gate 74HC04. We recommend to connect the same power source of the oscillator with the load's to minimize current loop. In order to minimize the length of the power line between the oscillator and load, please find the optimizal position for the gate when designing the board.
Please don't place any other line under the crystal in order to avoid any interference from them to keep stable oscillation. However, placing any line on it is necessary in present high density mounting. So, please make wide ground just under the crystal, then the other lines can be placed on the opposite side.





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