EPSON

Application Manual

Real Time Clock Module
RTC-4553

SEIKO EPSON CORP.

Contents

EPSON

Overview

This RTC-4553 is an SOP 14-pin size real time clock module which is designed for use in serial interfaces suitable for handy electronic equipments.

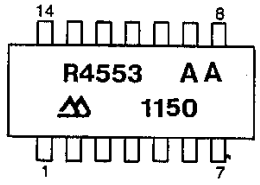
This module has excellent heat-resistance. its small package allows for high density mounting and automatic mounting. It features a wide variety of functions, such as a time and date function, a built-in 30×4 bit S-RAM and much more.

This module is indispensable for handy electronic equipment such as video-cameras, multi-function telephones, and POS systems, where time display is necessary.

Features

- The built-in crystal resonator makes the product streamlined and adjustment-free.
- The small package makes high density mounting possible.
- The built-in calendar that keeps time (hour, minute, second) and calendar. (year, month, day, day of the week).
- Automatic leap year correction.
- It has a built-in 30×4 bit RAM.
- High speed access
- Interface possible with 3V.
- It outoput a rèference pulse (1/10Hz, 1024Hz).
- It has a 30 seconds correction.
- Using a C-MOS IC enables low current consumption (1μA typ.).

Terminal connection

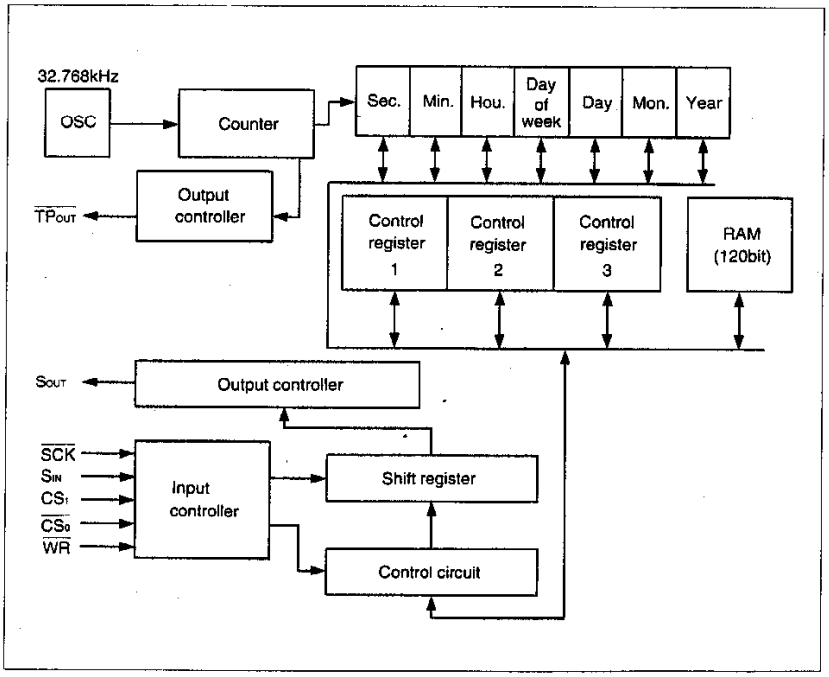


(TOP VIEW)

1	GND	14	$\overline{TP_{OUT}}$
2	$\overline{WR}$	13	S_{OUT}
3	S_{IN}	12	$\overline{CS_1}$
4	SCK	11	$\overline{CS_0}$
5	L1	10	L5
6	L2	9	L4
7	L3	8	V_{DD}

L1 to L5: Test pin.
Do not connect them to any terminals.

Block Diagram



■ Terminal functions

Terminal No.	Terminal Symbol	Output Input	Function
1	GND		Connect this terminal to the ground.
2	$\overline{WR}$ (WRITE & READ enable)	Input	Address and data are written at $\overline{WR}$="L". Writing counter data (second digit to year digit) is in accordance with increment system. (Time and date can not be written indirectly.) The specified address and data are read when $\overline{WR}$="H". The designated data output from S_{OUT}, set in the proceeding time.
3	S_{IN} (Serial input)	Input	This input pin for serial address and data is used to write addresses and data of each counter, register and RAM.
4	$\overline{SCK}$ (Serial clock)	Input	When outputting or inputting serial address and data,input synchronous signal to this pin, so that the address and data can be read and written in synchronization with the signal. 8 clock (address 4 clock + data 4 clock) is one cycle.
5, 6, 7, 9, AND 10	NC		Test pins. Do not connect them to any terminals.
8	V_{DD}		Connected it to the power source. It should be supplied 5V ±10% or 3V ±10% power, when normal access mode. Supply voltage of 2V or more when battery buckup mode.
11	$\overline{CS_0}$ (Chip select 0)	Input	This pin is used to select RTC-4553. In microcomputer, register can be accessed when "$\overline{CS_0}$=L". When"$\overline{CS_0}$=H", S_{OUT} comes to high impedance.
12	CS_1 (Chip select 1)	Input	Connect this pin to the power down detector circuit. (When the circuit does not have power down detector, fix it on V_{DD}.) When "CS_1=L", S_{OUT} and $\overline{TP_{OUT}}$ comes to high impedance.
13	S_{OUT} (Serial output)	Output	This output pin for serial address and data is used to read address and date of each counter register and RAM.
14	$\overline{TP_{OUT}}$ (Timing pulse output)	Output	This pin outputs a 1024Hz or 1/10Hz internal reference clock. It can be used for checking time pace accuracy. Please use output mode 1/10Hz when check clock tolerance. The duty cycle will be vary once per 10 seconds on 1024Hz output mode.

Note : Power supply by-pass capacitor of a 0.01μF or more, should be installed very close between V_{DD} and GND terminals of this RTC.

■ Characteristics

1. Absolute maximum ratings

Items	Symbols	Conditions	MIN.	MAX.	Unit
Supply voltage	V_{DD}	V_{DD} – GND	–0.3	+6.0	V
Input voltage	V_{IN}	S_{IN}, $\overline{SCK}$, $\overline{WR}$, $\overline{CS_0}$, CS_1	–0.3	V_{DD}+0.3	
Output voltage	V_{OUT}	S_{OUT}, $\overline{TP_{OUT}}$	–0.3	V_{DD}+0.3	
Storage temperature	T_{STG}	*1	–55	+125	°C
Soldering conditions	T_{SOL}	—	Once or twice at 260°C or less for up to 10 seconds, or once at 230°C or less for up to 3 minutes.		

*1: Stored without Tape and Reel.

2. Operating conditions

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	V_{DD}–GND	2.7	5.0	5.5	V
Operating temperature	T_{OPR}	—	–30	—	+70	°C

3. Frequency characteristics

Items	Symbols	Conditions		MAX.	Unit
Frequency tolerance	$\Delta f / f_o$	Ta = 25°C V_{DD} = 5 V *2	AA	5 ±5	ppm
			A	5 ±10	
			B	5 ±20	
Frequency temperature characteristics	t_{OP}	Ta = –10 to 70°C, V_{DD} = 5 V *3		+10 –120	
Frequency voltage characteristics	f/V	Ta = fixed, V_{DD} = 2 to 5.5 V *3		±5	
Aging	fa	Ta = 25°C, V_{DD} = 5V, first year		±5	ppm/year

*2: Freqency tolerance is guaranteed at the time of shipment.

*3: The frequency deviation (0 ppm) at Ta=25°C for "t_{OP}" or V_{DD}=5 V for "f/V" is used reference value.

*4: Start up time (t_R) of power is 1.0 µs/V ≤ t_R ≤ 1.6 ms/V

4. DC,AC characteristics

(1) V_{DD} = 5 V ±10%

① DC characteristics (GND=0V, Ta=–30 to 70°C)

Item	Symbol	Condition	V_{DD} = 5V ±10%			Unit
			MIN.	TYP.	MAX.	
Data holding voltage	V_{DH}	—	2.0	—	5.5	V
Current consumption	I_{DD1}	$\overline{SCK}$ = 500 kHz $\overline{CS_0}$ = L, CS_1 = H	—	—	100	µA
	I_{DD2}	$\overline{SCK}$ = 0 Hz $\overline{CS_0}$ = H, CS_1 = L	—	1.0	3.0	
Output voltage	V_{OH}	I_{OH} = – 400 µA	V_{DD} – 0.4	—	—	V
	V_{OL}	I_{OL} = 1.6 mA		—	0.4	
Off leak current	I_{OZH}	V_{OUT} = 5.5 V	–2.0	—	2.0	µA
	I_{OZL}	V_{OUT} = 0 V	–2.0	—	2.0	
Input voltage	V_{IH}	—	4/5 V_{DD}	—	—	V
	V_{IL}	—	—	—	1/5 V_{DD}	
Input current	I_{IH}	V_{IN} = 5.5 V	–2.0	—	2.0	µA
	I_{IL}	V_{IN} = 0 V	–2.0	—	2.0	
Oscillation startup time	T_S	Ta = 25°C	—	—	3.0	sec.

② AC characteristics

(GND= 0 V, Ta= –30 to +70°C)

Item	Symbol	Condition	V_{DD} = 5 V ±10%			Unit
			MIN.	TYP.	MAX.	
$\overline{SCK}$ input frequency	f_{CLK}	—	—	—	500	kHz
$\overline{SCK}$ "L" time	t_{WCKL}	—	1.0	—	—	µsec.
$\overline{SCK}$ "H" time	t_{WCKH}	—	1.0	—	—	
$\overline{SCK}$ Pause time	t_{PS}	—	1.0	—	—	
$\overline{CS_0}$ Set up time	t_{SCS}	—	0	—	—	
$\overline{CS_0}$ Hold time	t_{HCS}	—	0.5	—	—	
S_{IN} Data Set up time	t_{SD}	—	0.2	—	—	
S_{IN} Data Hold time	t_{HD}	—	0.2	—	—	
$\overline{WR}$ Set up time	t_{SWR}	—	1.0	—	—	
$\overline{WR}$ Hold time	t_{HWR}	—	0.5	—	—	
S_{OUT} Delay time	t_{DSO}	CL=100pF	—	150	500	nsec.
$\overline{CS_0}$, and CS_1 Enable to S_{OUT} Output	t_{DSZ1}	CL=100pF	—	—	100	
$\overline{CS_0}$ Disenable to S_{OUT} High Z	t_{DSZ2}	CL=100pF	—	—	100	
CS_1 Enable to $\overline{TP_{OUT}}$ Output	t_{DPZ1}	CL=100pF	—	—	100	
CS_1 Enable to $\overline{TP_{OUT}}$ High Z	t_{DPZ2}	CL=100pF	—	—	100	

(2) V_{DD} = 3V ±10%

① DC characteristics

(GND= 0 V, Ta = –30 to 70°C)

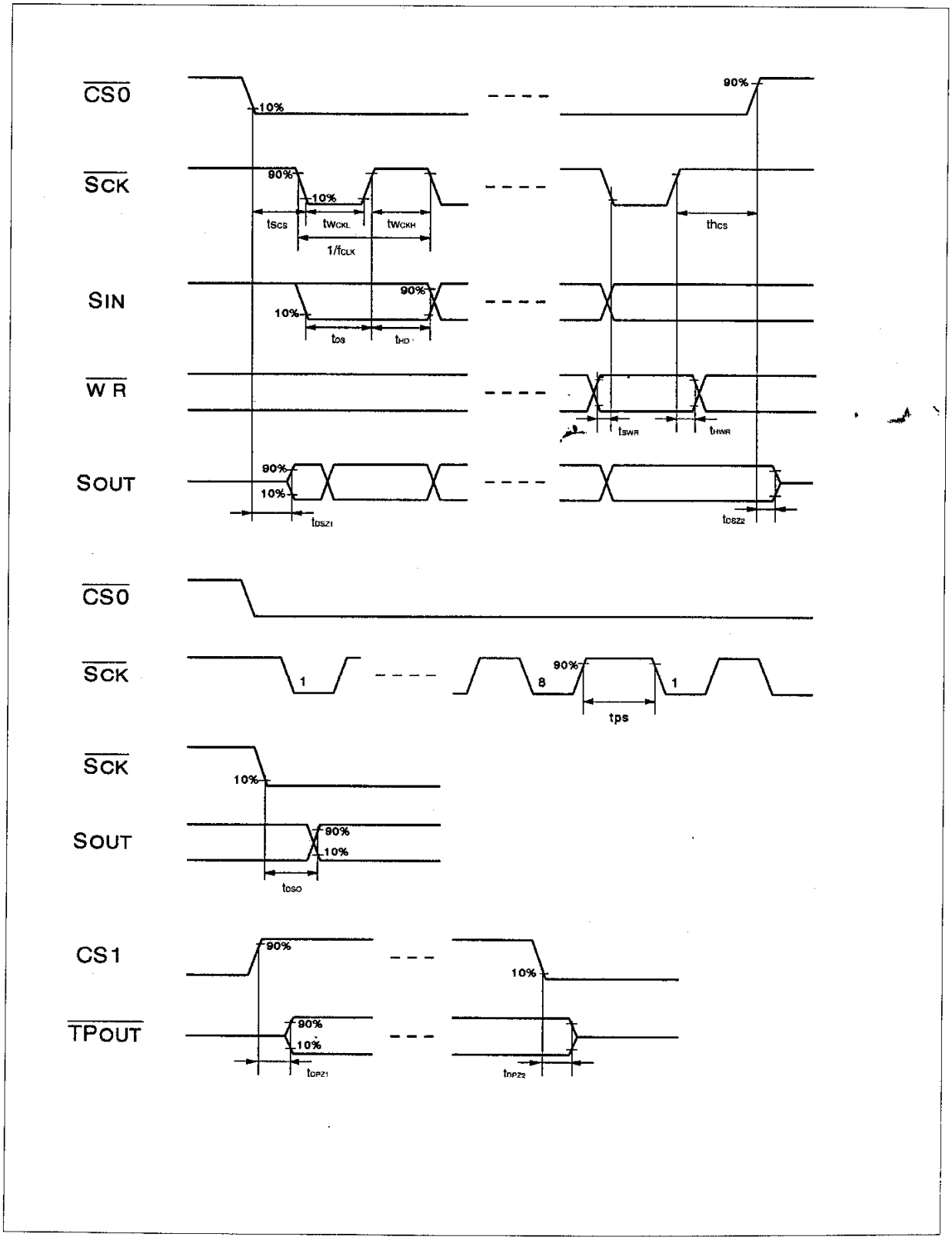
Item	Symbol	Condition	V_{DD} = 3 V ±10%			Unit
			MIN.	TYP.	MAX.	
Data holding voltage	V_{DH}	—	2.0	—	3.3	V
Current consumption	I_{DD1}	$\overline{SCK}$ = 300 kHz, $\overline{CS_0}$ = L, CS_1 = H	—	—	100	mA
	I_{DD2}	$\overline{SCK}$ = 0 Hz, $\overline{CS_0}$ = H, CS_1 = L	—	1.0	3.0	
Output voltage	V_{OH}	I_{OH} = – 400 µA	V_{DD} – 0.4	—	—	V
	V_{OL}	I_{OL} = 1.6 mA	—	—	0.4	
Off leak current	I_{OZH}	V_{OUT} = 3.3 V	–2.0	—	2.0	µA
	I_{OZL}	V_{OUT} = 0 V	–2.0	—	2.0	
Input voltage	V_{IH}	—	4/5 V_{DD}	—	—	V
	V_{IL}	—	—	—	1/5 V_{DD}	
Input current	I_{IH}	V_{IN} = 3.3 V	–2.0	—	2.0	µA
	I_{IL}	V_{IN} = 0 V	–2.0	—	2.0	
Oscillation startup time	T_S	Ta = 25°C	—	—	3.0	sec.

② AC characteristics

(GND= 0 V, Ta = –30 to +70°C)

Item	Symbol	Condition	V_{DD} = 3 V ±10%			Unit
			MIN.	TYP.	MAX.	
$\overline{SCK}$ input frequency	f_{CLK}	—	—	—	300	kHz
$\overline{SCK}$ "L" time	t_{WCKL}	—	1.5	—	—	µsec.
$\overline{SCK}$ "H" time	t_{WCKH}	—	1.5	—	—	
$\overline{SCK}$ Pause time	t_{PS}	—	1.5	—	—	
$\overline{CS_0}$ Set up time	t_{SCS}	—	0	—	—	
$\overline{CS_0}$ Hold time	t_{HCS}	—	1.0	—	—	
S_{IN} Data Set up time	t_{SD}	—	0.2	—	—	
S_{IN} Data Hold time	t_{HD}	—	0.2	—	—	
$\overline{WR}$ Set up time	t_{SWR}	—	1.5	—	—	
$\overline{WR}$ Hold time	t_{HWR}	—	1.0	—	—	
S_{OUT} Delay time	t_{DSO}	CL=100pF	—	300	500	nsec.
$\overline{CS_0}$, and CS_1 Enable to S_{OUT} Output	t_{DSZ1}	CL=100pF	—	—	200	
$\overline{CS_0}$ Disenable to S_{OUT} High Z	t_{DSZ2}	CL=100pF	—	—	200	
CS_1 Enable to $\overline{TP_{OUT}}$ Output	t_{DPZ1}	CL=100pF	—	—	200	
CS_1 Enable to $\overline{TP_{OUT}}$ High Z	t_{DPZ2}	CL=100pF	—	—	200	

(3) Timing Chart



Register

1. Register table

MODE 2 (User RAM region 2)

Address					User RAM register			
	A_3	A_2	A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	RA_{63}	RA_{62}	RA_{61}	RA_{60}

MODE 1 (User RAM region 1)

Address					User RAM register			
	A_3	A_2	A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	RA_3	RA_2	RA_1	RA_0

MODE 0

Address					Register symbol	Counter and control register				
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0	Register name
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	1 second digit register
1	0	0	0	1	S_{10}	0	S_{40}	S_{20}	S_{10}	10 seconds digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	1 minute digit register
3	0	0	1	1	MI_{10}	0	mi_{40}	mi_{20}	mi_{10}	10 minutes digit register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	1 hour digit register
5	0	1	0	1	H_{10}	PM/$\overline{\text{AM}}$	0	h_{20}	h_{10}	10 hours digit register
6	0	1	1	0	W	0	w_4	w_2	w_1	Day of the week digit reg.
7	0	1	1	1	D_1	d_8	d_4	d_2	d_1	1 day digit register
8	1	0	0	0	D_{10}	0	0	d_{20}	d_{10}	10 days digit register
9	1	0	0	1	MO_1	mo_8	mo_4	mo_2	mo_1	1 month digit register
A	1	0	1	0	MO_{10}	0	0	0	mo_{10}	10 months digit register
B	1	0	1	1	Y_1	y_8	y_4	y_2	y_1	1 year digit register
C	1	1	0	0	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	10 years digit register
D	1	1	0	1	CNT 1	TPS	30ADJ	CNTR	24/$\overline{12}$	Control register 1
E	1	1	1	0	CNT 2	BUSY	PONC	(-)	(*)	Control register 2
F	1	1	1	1	CNT 3	SYSR	TEST	MS1	MS0	Control register 3

RA_{64}	
RA_{68}	
RA_{72}	
RA_{76}	
RA_{80}	
RA_{84}	
RA_{88}	
RA_{92}	
RA_{96}	
RA_{100}	
RA_{104}	
RA_{108}	
RA_{112}	
RA_{116}	
MS_0	

RA_4	
RA_8	
RA_{12}	
RA_{16}	
RA_{20}	
RA_{24}	
RA_{28}	
RA_{32}	
RA_{36}	
RA_{40}	
RA_{44}	
RA_{48}	
RA_{52}	
RA_{56}	
MS_0	

0 setzen

Bedeutung als User RAM ocly Mode 0

0 setzen

2. Notes

(1) Do not set data out of range for the time and calendar. Otherwise, a counting error may occur.
(2) When the power is turned on (before initialization) the state of the bits are undefined. Write the registers to set the values.
(3) The user should be set D_0 bit of control register 2 (* bit) to "0".
(4) When the read is bit D_1 of control register 2 (– bit) is undefined.
(5) D_3 bit of control register 3 (TEST bit) is used by us to test the system. The user must set this bit to "0".

3. Functions of the register bits.

<table>
<tr><th>Bit name</th><th>Functions</th></tr>
<tr><td>0 mark</td><td>When this bit is read, the data is "0".</td></tr>
<tr><td>Second to year digit</td><td>BCD code.The data are written by increment method.</td></tr>
<tr><td>PM/$\overline{AM}$</td><td>"1" shows PM and "0" shows AM. This bit can also be read in 24-hour mode(24/12=1). (00:00 to 11:59 = AM; 12:00 to 23:59 = PM)</td></tr>
<tr><td>Day of the week digit</td><td>Encode it before using.
Example:
<table>
<tr><td>Data</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>Day of the week</td><td>Sun.</td><td>Mon.</td><td>Tue.</td><td>Wed.</td><td>Thu.</td><td>Fri.</td><td>Sat.</td></tr>
</table></td></tr>
<tr><td>Year digit</td><td>The leap year is automatically identified up to 2099 years.</td></tr>
<tr><td>User RAM region</td><td>30 × 4 bit SRAM</td></tr>
<tr><td>TPS
(Timing Pulse Selection)</td><td>Constant periodic pulse can be selected.
Note : During for 10 seconds from power on or system reset, 1/10 Hz signal does not output.
<table>
<tr><th>TPS bit</th><th>Frequency (Cycle time)</th></tr>
<tr><td>0</td><td>1024 Hz (976.5 µsec.)</td></tr>
<tr><td>1</td><td>1/10 Hz (10 sec.)</td></tr>
</table></td></tr>
<tr><td>30ADJ
(30 seconds adjustment)</td><td>When this bit is "1", the 30 seconds correction is executed
This bit will be reset automatically, after 76.3 µsec..</td></tr>
<tr><td>CNTR
(Counter reset)</td><td>Counter reset except year.</td></tr>
<tr><td>24/$\overline{12}$</td><td>When "1", then 24-hour mode; when "0", then 12-hour mode with PM/AM...Selection of read mode.</td></tr>
<tr><td>Busy</td><td>This bit is used when reading/writing from/to time and calendar counter. This bit is set to "1",when carry occurs.
<table>
<tr><th>BUSY bit</th><th>Mode</th><th>Function</th></tr>
<tr><td>0</td><td>No carry</td><td>Reading and writing time and date are available.</td></tr>
<tr><td>1</td><td>Carry occur</td><td>Reading and writing time and date are prohibited.</td></tr>
</table></td></tr>
<tr><td>PONC
(Power-ON-Clear detector)</td><td>When turning on the power, power-on-clear function works automatically, and PONC bit set to "1". When power-on-crear function worked, it is same operation as system reset (SYSR bit= 1).
<table>
<tr><th>Register</th><th>Data</th></tr>
<tr><td>Counter (Second to year digit)</td><td>00-year, 01-month, 01-day, AM, 12-o'clock, 00-minute, 00-second, 0-day of the week</td></tr>
<tr><td>Control register</td><td>All "0" (But PONC=1)</td></tr>
<tr><td>User RAM</td><td>Undefined</td></tr>
</table>
Therefore, the time and calendar counter and the control register must be set, when writing PONC = "1".</td></tr>
<tr><td>The bit marked "–"</td><td>When this bit is read, the data is undefined.</td></tr>
<tr><td>The bit marked "*"</td><td>Should be set this bit to "0".</td></tr>
<tr><td>SYSR
(System reset)</td><td>Time and calendar counters and control registers are all-cleared with "1".
<table>
<tr><th>Register</th><th>Data</th></tr>
<tr><td>Counter (Second to year digit)</td><td>00-year, 01-month, 01-day, AM, 12-o'clock, 00-minute, 00-second, 0-week</td></tr>
<tr><td>Control register</td><td>All "0" (But SYSR=1</td></tr>
<tr><td>User RAM</td><td>Undefined</td></tr>
</table>
Setting of the counter and the register should be done after releasing system reset.</td></tr>
<tr><td>TEST</td><td>This bit is used by SEIKO EPSON to test the system.
The user must set this bit to "0".(TEST="0")</td></tr>
<tr><td>MS_0, MS_1
(Mode selection)</td><td>Switch the mode by two bits.
<table>
<tr><th>MS_1</th><th>MS_0</th><th>Mode name</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>Mode 0</td><td>Counter (Second to year digit) & control register 1 to 3.</td></tr>
<tr><td>0</td><td>1</td><td>Mode 0</td><td>Counter (Second to year digit) & control register 1 to 3</td></tr>
<tr><td>1</td><td>0</td><td>Mode 1</td><td>User RAM region (RA_0 to RA_{59}) & control register 3</td></tr>
<tr><td>1</td><td>1</td><td>Mode 2</td><td>User RAM region (RA_{60} to RA_{119}) & control register 3</td></tr>
</table></td></tr>
</table>

■ Register description

1. S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, W, D_1, D_{10}, MO_1, MO_{10}, Y_1, Y_{10}

(Time and calendar register)

(1) Every registers are BCD code and positive logic.

(2) The range of register "W" is 0 to 6, and it is used in a code. The day of the week can not be identified by the date.

Example:

Data	0	1	2	3	4	5	6
Day of the week	Sun.	Mon.	Tue.	Wed.	Thu.	Fri.	Sat.

(3) H_1, H_{10} (Hour digit register)

Possible time is different according to the setting of 24/$\overline{12}$ bit (CNT1 register).

When the 12-hour read mode (24/$\overline{12}$ bit=0) is selected, the PM/$\overline{AM}$ bit must be set.

24/$\overline{12}$ bit	Existent time	Note
0 (12-hour)	AM 12:00 to AM 11:59, PM 12:00 to PM 11:59	PM/AM bit can also be read in 24-hour mode.
1 (24-hour)	AM 00:00 to AM 11:59, PM 12:00 to PM 23:59	

(4) Y_1, Y_{10} (year digit register)

These registers use the Gregorian calendar. Leap year is automatically (up to 2099) adjusted. (years that are multiples of 4 are identified as leap years.)

Example: '92, '96, '00, '04, '08, '12, '16, '20 .....

(5) "0" mark

Even if "1" is written on the bit marked by zero in the register table, automatically turns to "0" when being read.

(6) Setting non-existent times or dates may cause time errors.

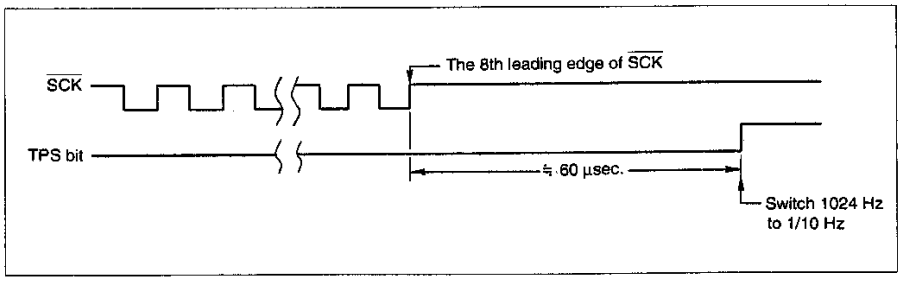
2. CNT 1 register (Control register 1)

(1) TPS (Timing pulse select)

- Bit used for selecting output waveform of reference signal form TP_{OUT}.

TPS bit	Output fequency (Cycle time)	Duty (Time) of "L" level
0	1024Hz (976.5 µsec.)	1/2 (438.25 µsec.)
1	1/10Hz (10 sec.)	3/5 (6 sec.)

- During for 10 seconds from power on or system reset, 1/10 Hz signal source not output.



(2) 30ADJ (30 seconds adjustment)

- 30ADJ function works when the 30ADJ bit is "1".

Seconds digit before 30ADJ	Seconds digit after 30ADJ
29 seconds or less	"00"seconds without carry to 1 minute degit
30 seconds or more	"00"seconds with carry to 1 minute degit

- This bit is automatically cleared (30ADJ = 0) within 76.3 µsec. after finishing 30 seconds adjustment. When reading or writing time/date register immediately after 30 seconds adjustment is required, please make sure that 30ADJ bit is "0" or it should be done, taking a pause for 76.3 µseconds after 30 seconds adjustment.

(3) CNTR (Counter reset)

- The CNTR bit used to initialize the counters of selected time and calendar. (Except year digit.)

CNTR bit	Meaning
0	Normal mode (When writing to time and calendar registers, the counter is incremented.)
1	The time and calendar counter is initialized (expect year counters)

When the second counter is reset, second or less is also reset.

The output at $\overline{TP_{OUT}}$ terminals shows duty cycle change in a reset cycle.

- Notes

a) Data for days or months which do not exist may arise due to improper setting methods. Correct these data referring to procedure for non-existent data (on page 17).
b) Be sure to set "0" after finishing counter reset.

(4) 24/$\overline{12}$ (24-hour system/12-hour system)

- Switch the read mode in accordance with the 24-hour system or 12-hour system.

24/$\overline{12}$ bit	System name	Existent time
0	12-hour system	AM 12:00 to AM 11:59, PM 12:00 to PM 11:59
1	24-hour system	AM 00:00 to AM 11:59, PM 12:00 to PM 23:59

In the 12-hour mode, set the PM/AM bit by incrementing the time, this bit works on 24-hour mode too.

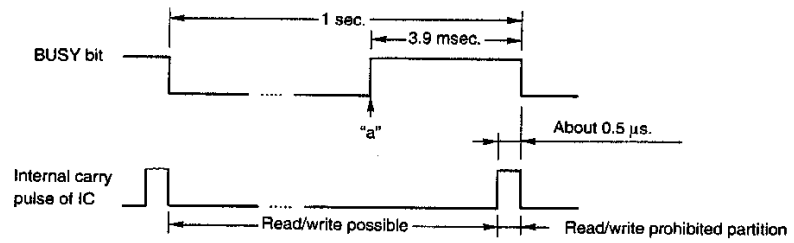
3. CNT 2 register

(1) BUSY

- This bit is used to write and read time and calendar. This bit shows the carry of 1-second digit whether a carry is going on or not.

BUSY bit	Mode	Meaning
0	Normal mode	Reading & writing of time & date are able.
1	Carry mode	Reading and writing of time and calendar are prohibited since the carry is going on.

Busy timing



- Notes

a) It is recommended that Read/Write is finished before Busy bit rise to High. The duration of Busy=1 is 3.9 ms and actual prohibited duration of Read/Write is 0.5 µs.

b) If Read/Write is done in a duration of carry (0.5 µs), followings are occured.
Read: Misreading may occur
Write: Write data are ignored.

- The end of read and write: Refers to the 8th pulse rise of $\overline{SCK}$ as shown in the figure for timing chart (on page 12).

(2) PONC (Power-on-clear)

- This bit is used to show the validity of data. The PONC bit is set to "1" when the power is turned on for the first time and when the power fails.

And "power-on-clear" function works automatically, user are necessary to set data for all registers.

PONC bit	Mode	Meaning
0	Normal mode	—
1	Power-on clear mode	Data is initialized Register: Time and calendar — Meaning: 00-year, 01-month, 0-week,01-day, am, 12-oclock, 00-minute, 00-second Register: Others — Meaning: All control registers = 0. (Only PONC = 1) RAM is undefined.

- Release: Before setting the register data, this bit should be released (PONC = 0) by performing system reset (writingSYSR = 1).

(3) – mark

When this bit is read, the data is undefined.

(4) * mark

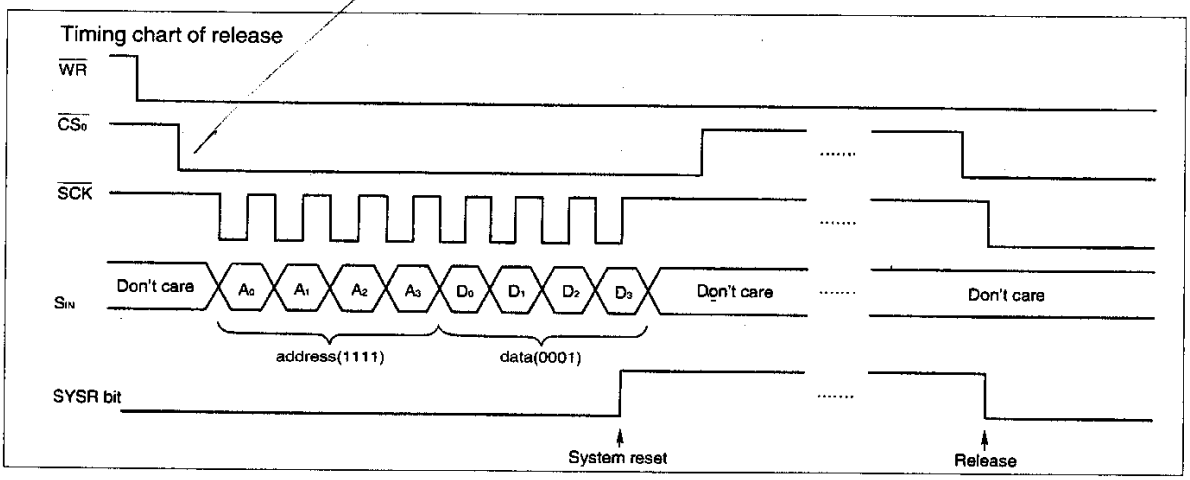
This bit should be "0".

4. CNT 3 Register

(1) SYSR (System reset)

All logic is initialized (refer table of PONC bit) by writing SYSR = 1.

Release: This bit is released by the falling of $\overline{SCK}$ after $\overline{CS_0}$ has fallen.



(2) TEST

The test bit is used for testing in "SEIKO EPSON". Be sure to set TEST = "0".

Operation is not guaranteed for this product when TEST bit is "1".

(3) MS_1,MS_0 (Mode select 1, and 0)

The bit is used for switching address mode.

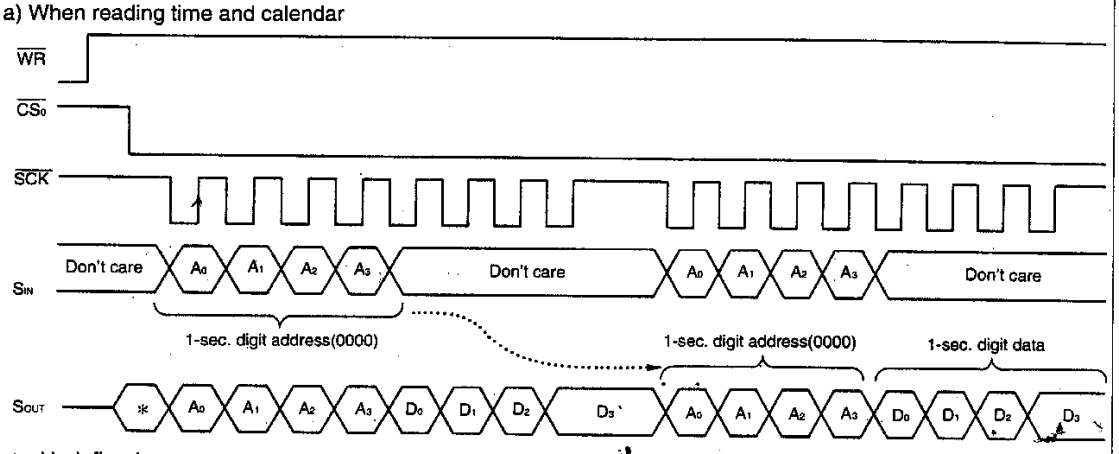
MS_1	MS_0	Mode name	Meaning
0	0	Mode 0	Counter (Second to year digit) and control register 1 to 3
0	1	Mode 0	Counter (Second to year digit) and control register 1 to 3
1	0	Mode 1	User RAM region 1 (RA_0 to RA_{59}) and control register 3
1	1	Mode 2	User RAM region 2 (RA_{60} to RA_{119}) and control register 3

■ Operation procedure

1. Data reading

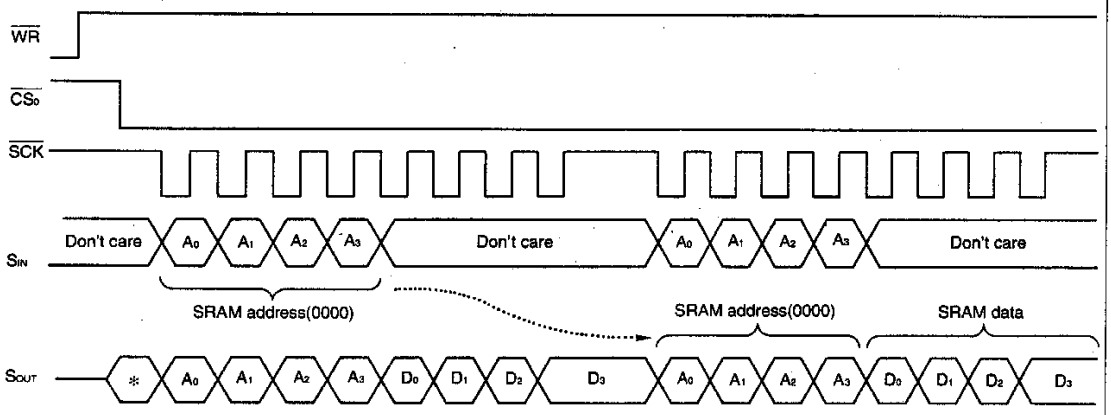
(1) Timing chart

a) When reading time and calendar



* : Undefined
SIN : Input at the trailing edge of SCK.
SOUT: Output at the leading edge of SCK.

b) When reading SRAM data



* : Undefined
SIN : Input at the trailing edge of SCK.
SOUT: Output at the leading edge of SCK.

(2) Explanation

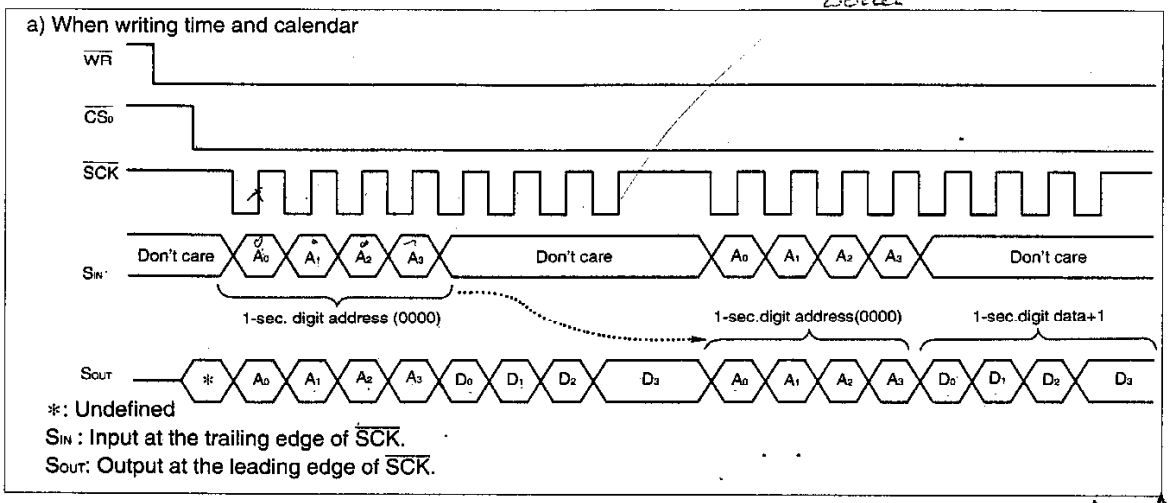
- Serial address data that is input from the SIN when CS0=L is taken in on the SCK rise. Next, when WR=H is taken in on the 8th pulse rise of SCK, either the counter, control register or the SRAM address will be selected. The selected counter, control register or the SRAM address data is output simultaneously with SCK fall from the SOUT in the following cycle.

- When the SCK clock is less than 8 pulses or more, it enters the command wait mode.
  When the SCK in 9 pulses or more, commands are not correctly input.
  The internal counter of the SCK clock is cleared within the pause time and on the trailing edge of CS0.

2. Data writing

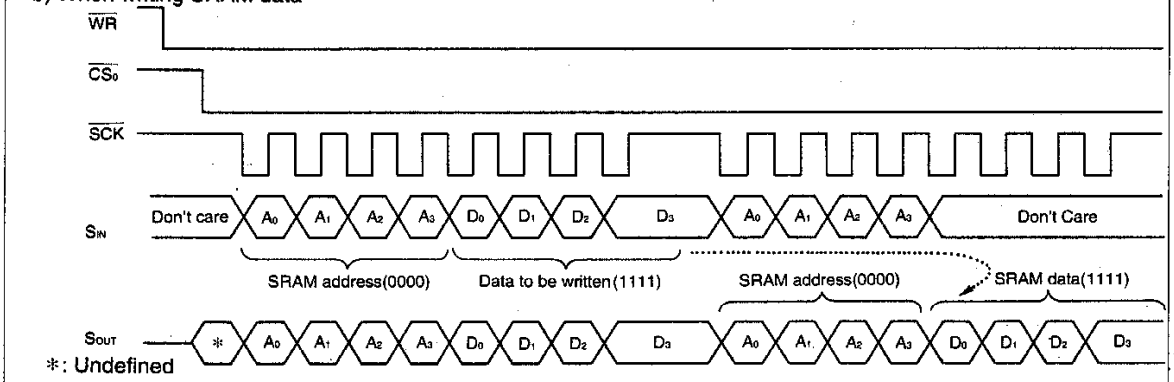
(1) Timing chart

a) When writing time and calendar



*: Undefined
SIN : Input at the trailing edge of SCK.
SOUT: Output at the leading edge of SCK.

b) When writing SRAM data



*: Undefined
SIN : Input at the trailing edge of SCK.
SOUT: Output at the leading edge of SCK.

(2) Explanation

- Serial address data that is input form the SIN when CS0=L is taken in on the SCK rise. Next,when WR=L is taken in on the 8th pulse rise of SCK,either the counter, control register or the SRAM address will be selected.The selected counter, control register or the SRAM address data is written.

Counter register (Time and calendar reg.)	Increment data of the counter [(present data) + 1] sample:

Data before increment	The number of time of increment	Data after increment
0	4	4
8	3	11 (10-digit is carried automatically)

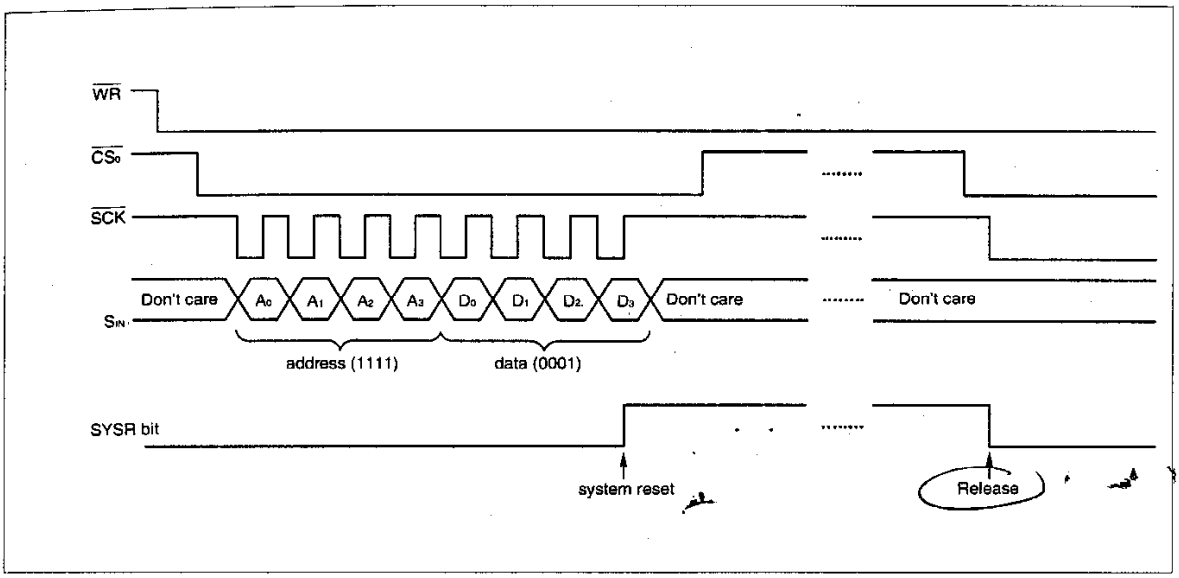
Control register and SRAM	Serial address and data of lower 4 bit are written.

The selected counter control register or the SRAM address data is output simultaneously with SCK fall from the SOUT in the following cycle.

- When the SCK clock is less than 8 pulses or more,it enters the command wait mode.
  When the SCK in 9 pulses or more, commands are not correctly input.
  The internal counter of the SCK clock is cleared within the pause time and on the trailing edge of CS0.

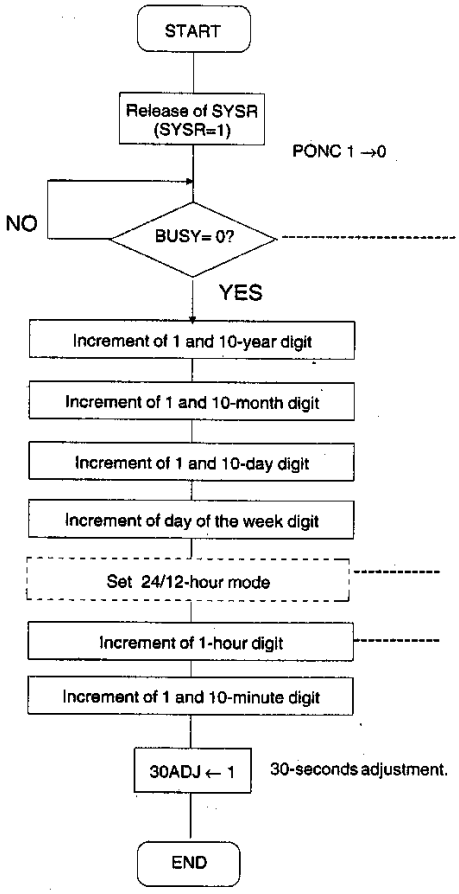
3. Release of system reset

SYSR (system reset) is released by the falling of $\overline{SCK}$ after $\overline{CS_0}$ has fallen.



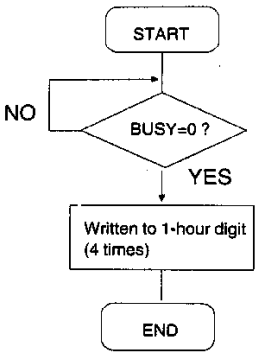
4.Flow chart of write operation

(1)Typical application of initial setting of time and calendar.
(Definition between the power on by battery changed etc.)



- When BUSY = "1", it shows that the carry is on and setting should be prohibited.
  The following processing should be completed within 996msec. after SYSR ← "1" or after BUSY ← "0", be sure to check BUSY bit and then continue the processing.
- It is advisable to set from the Year digit so as not set non-existent data.
- When incrementing the 1st digit of the year, month, day, hour, minute and second, the carry to 10th digit occur within each set digit.
- Please set 24/$\overline{12}$ hours bit before clock registers setting to avoid incorrect clock setting.
- Do not increment the 10 hours digit.

(2) Typical application of initial setting of time and calendar. (8:00→12:00)



MS_0="0", MS_1="0"

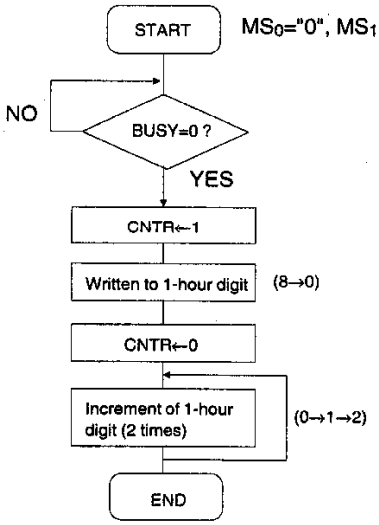
When BUSY=1, carry is going on, and modification should be avoided.

4 times (8→9→10→11→12)

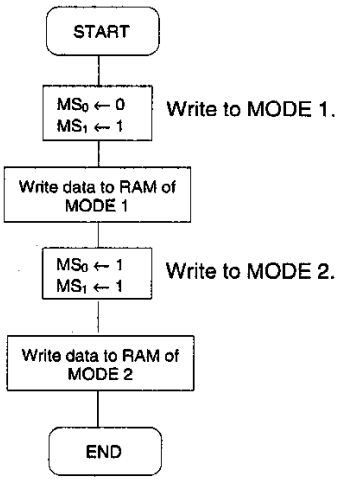
10 hours digit automatically carried.

This processing shoud be completed within 3.8 msec. after BUSY="0"

(3) Typical applications of modifying time & calendar, resetting the counter. (8:00→2:00)



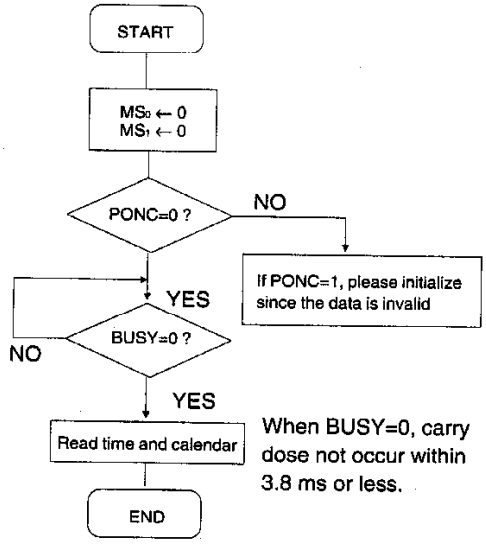
(4) Typical applications of writing RAM.



Note: When the operation can not be completed within 3.8 msec., check BUSY bit.

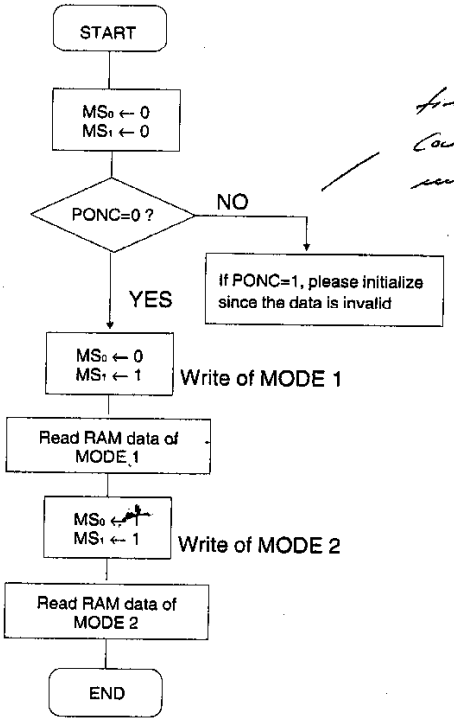
5.Flow chart of reading

(1) Typical application of reading time and calendar.

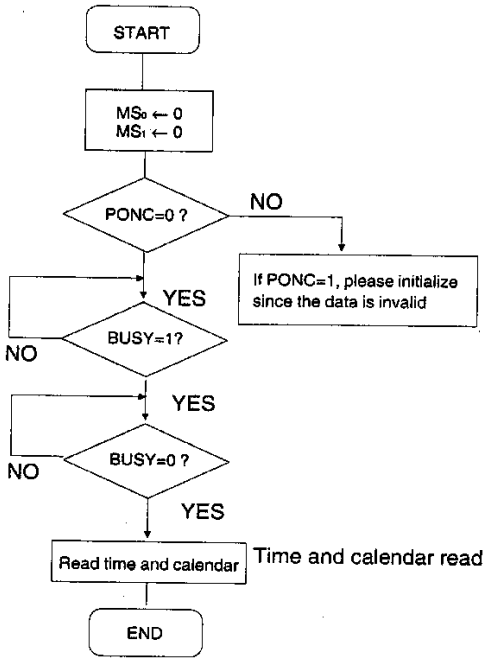


When BUSY=0, carry dose not occur within 3.8 ms or less.

(2) Typical application of reading RAM.



(3) Typical application of reading time & calendar BUSY fall.

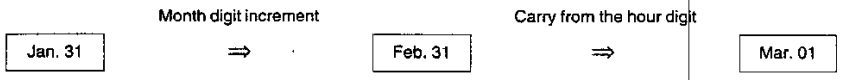


Time and calendar read are within 996 msec.

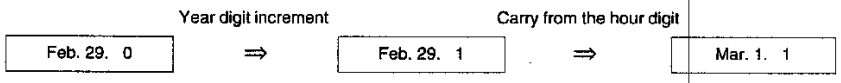
6. Non-existent data

In the following cases, non-existent data are set and additional processing is needed.

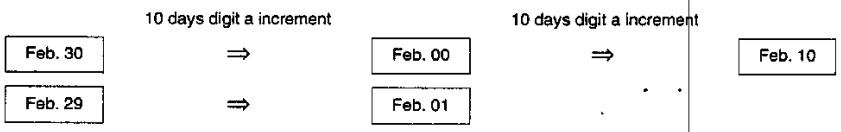
(1) When the month digit of "Jan.(1) 31" is incremented, a non-existent data, "Feb.(2) 31" occurs. This data should be set to "Mar.(3) 1" by carrying from the hour digit.



(2) When the year digit of "Feb.(2) 29" in a leap year is incremented, a non-existent data "Feb. 29" in a ordinary year occurs. This data should be carried over to "Mar.(3) 1" by carrying from the hour digit.



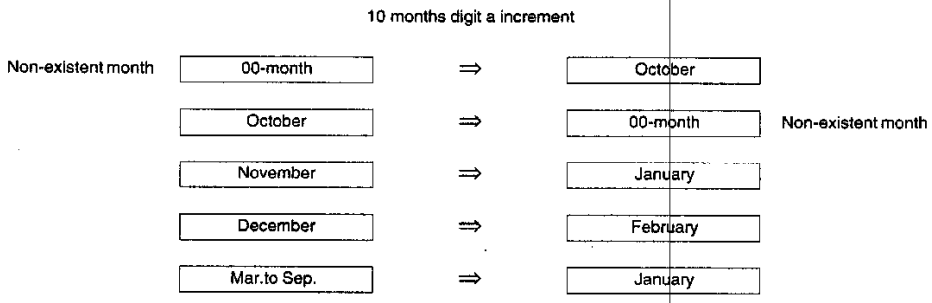
When 10 days digit of non-existent data is incremented, 1 day digit is cleared by overflow of 10 days digit.



Note: When existent data, 1 day digit is not cleared by overflow of 10 days digit.

(3) When the day digit of 31 days is incremented, day digit is 01 day by increment of 10 days digit.

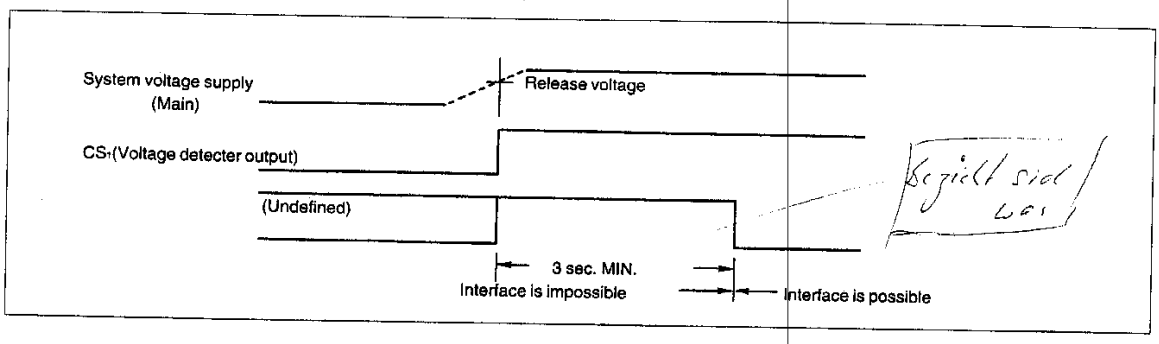
(4) Incrementing of month digit of 10 months digit differs from 1 month digit after overflow by setting of months.



■ Power source and chip select

1. Starting time of access

When interfacing the CPU after power has been turned on, please leave it in stand-by for at least 3 seconds (the rise time is necessary when oscillating circuit is turned on).



This 3 seconds stand-by period is unnecessary when voltage is already being applied from the back-up battery, but if it is not being backed up, it is necessary for proper functioning.

2. CS_1 and $\overline{CS_0}$ operation

$\overline{CS_0}$ terminal can be used on floating state during CS_1 is kept low. However, CS_1 terminal must not be used on floating state, because it makes large current consumption. So, this is cause of short life of back up battery.
When CS_1 goes to low, it disables interfacing, both S_{OUT} and $\overline{TP_{OUT}}$ terminal goes to high impedance.

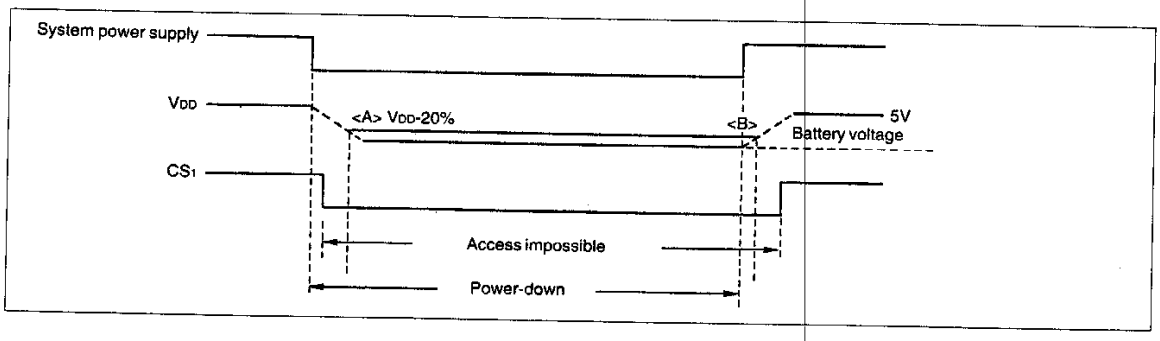
3. System power down during operation

When power goes down and CS_1 goes low during RTC has interfacing with CPU, the interfaced datta will be invalid. So after power turns on again, S_{OUT} terminals output will be unstable after one cycle just CS_1 fixed to high.

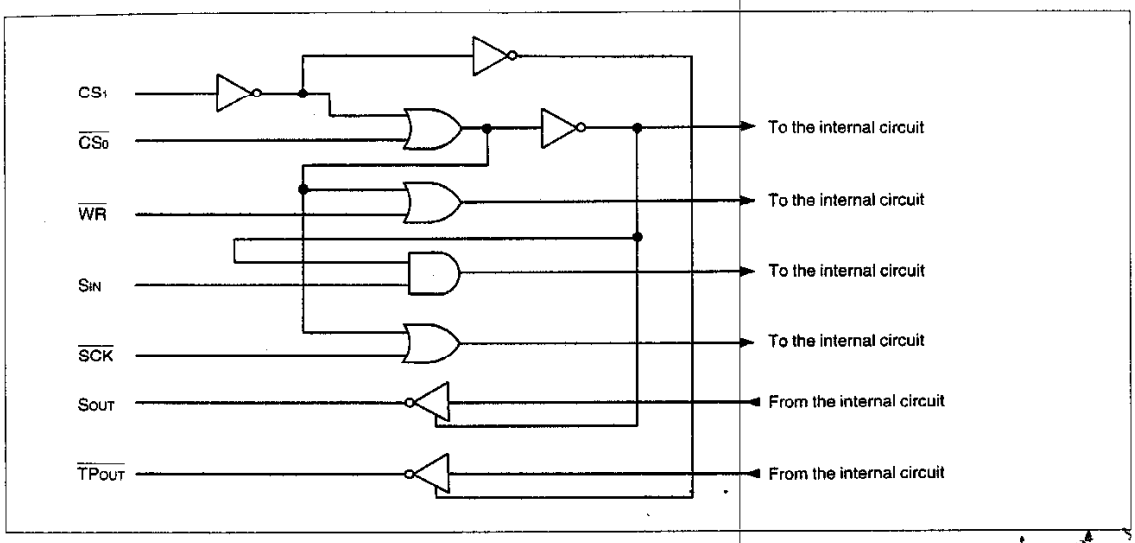
4. Power and CS_1 operation

V_{DD} voltage level goes to battery's level due to system power down. CS_1 should be low before V_{DD} goes down (See <A> point as follows). When power turned on again, CS_1 should be high after power over a level. (See <B> point as follows.)

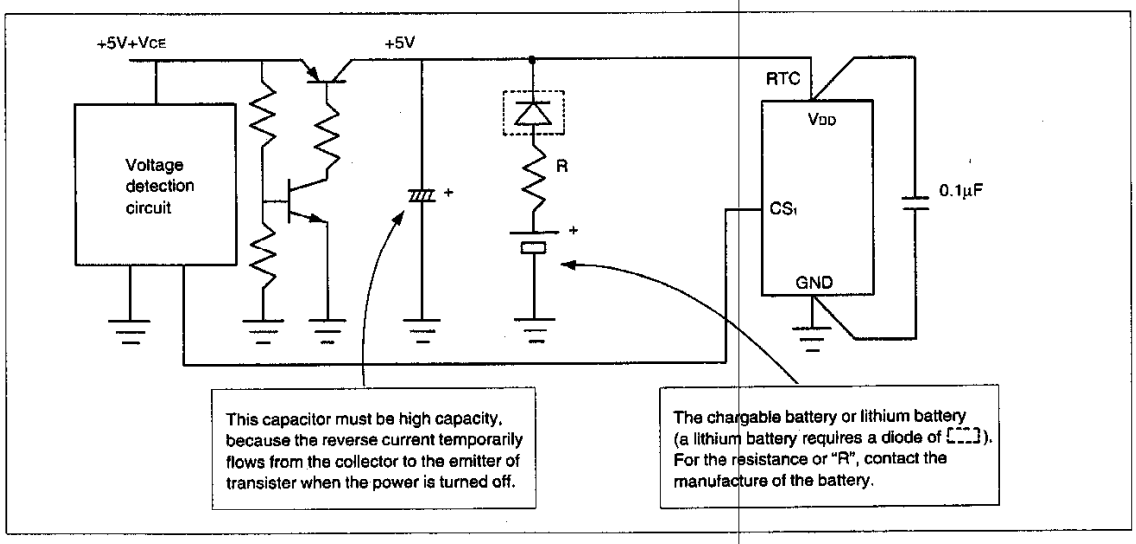
(1) Timing chart of system power supply



(2)The figure below the circuits near inputs

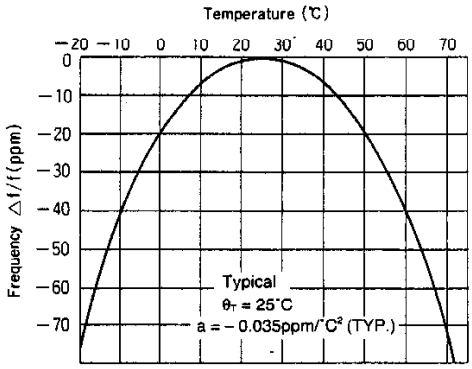


5. Example of connecting the RTC to the power supply circuit



■ Reference data

(1) Frequency-temperature characteristics



• Prosedure of getting the value of frequency stability(time error).

A: Frequency-temperature characteristics are explained as follows:

Δf_T [ppm] $= a\,(\theta T-\theta x)^2$

Δf_T [ppm]	:	Frequency tolerance at optional temp.
a [ppm/°C^2]	:	Temp. coefficient (-0.035 ±0.005ppm/°C^2)
θT [°C]	:	Peak temperature (25°C ±5°C)
θx [°C]	:	Optional temperature

B: To get the value of time error (accuracy), frequency stability and voltage characteristics should be added to the frequency-temperature.

$\Delta f/f$[ppm] $= \Delta f/fo + \Delta f/f_T + \Delta f/fv$

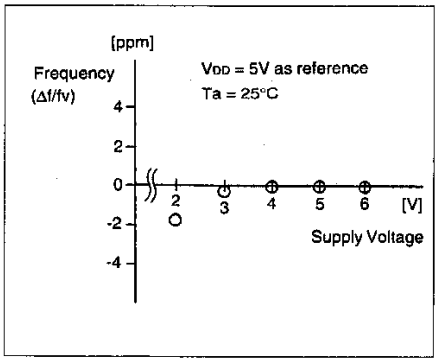
$\Delta f/f$ [ppm]	:	Time accuracy at optional temp./voltage (Frequency stability)
$\Delta f/fo$ [ppm]	:	Frequency tolerances
$\Delta f/f_T$ [ppm]	:	Frequency deviation at optional temp.
$\Delta f/fv$ [ppm]	:	Frequency deviation at optional voltage

C: How to determine the day difference.

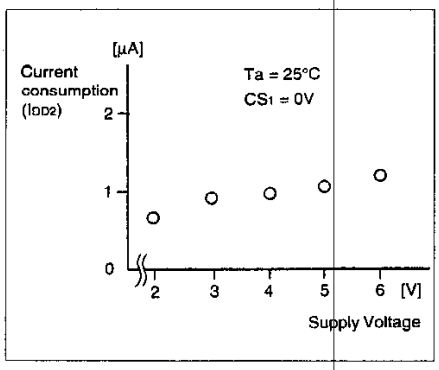
Day difference (second) = $\Delta f/f \times 10^{-6} \times 86{,}400$ (seconds/Day).

The day difference is approximately one second per day, at $\Delta f/f$ is 11.574 ppm.

(2) Example of the frequency/voltage characteristics.



(3) Example of the current consumption /voltage characteristics.



(4) Note

The data shows the standard values for sample lot.

For the rated values, see the specifications.(Please refer to of page 3 to 5)