MQ302-01

EPSON

Application Manual

Real Time Clock Module

RTC-4574SA/JE

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RTC-4574SA/JE

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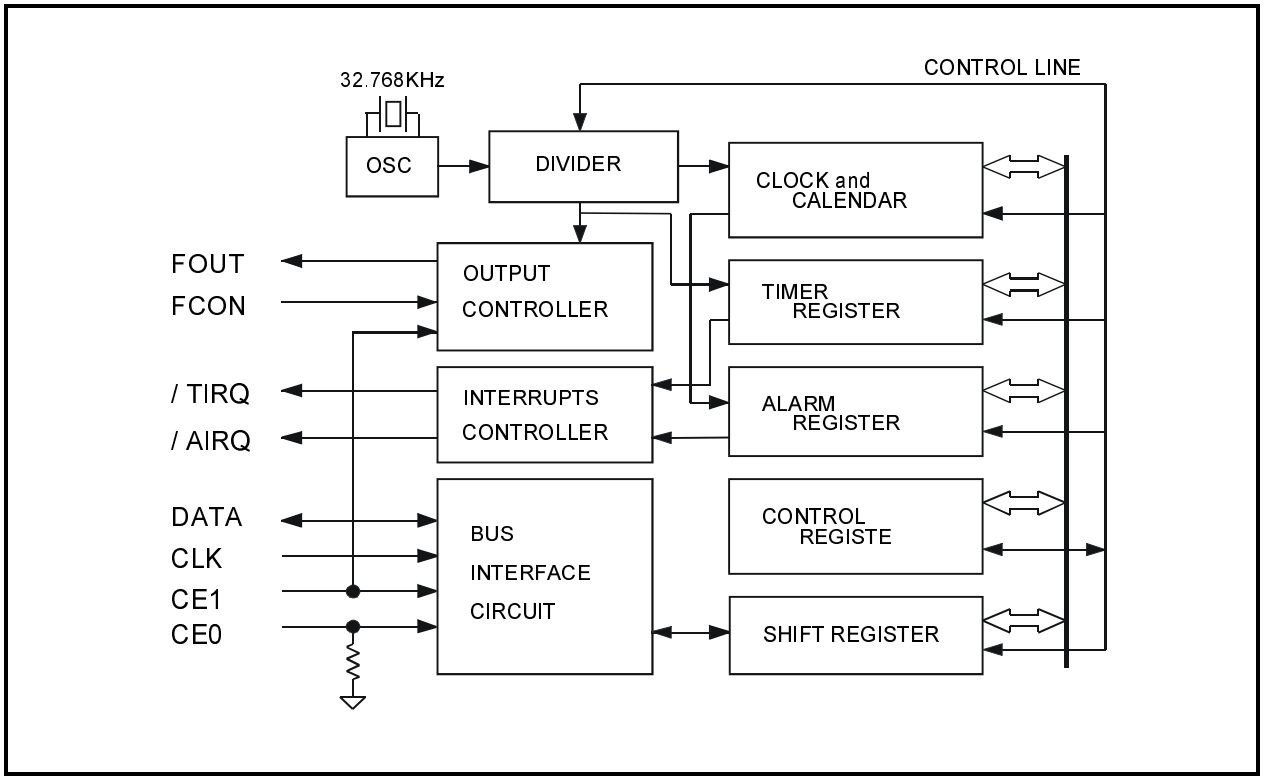
RTC-4574

- Built-in 32.768KHz crystal unit with frequency adjusted
- Serial interface which can be controlled by three signal lines
- Alarm interrupt function for day of week, day, hour, and minute
- Regular cycle interrupt function which can be set up between 1/4096 second and 255 minutes
- Dedicated interrupt output of the two systems (alarm and regular cycle) which allows software masking
- Ability to detect stopping of oscillation and time update
- Automatic adjustment for leap year
- Wide range of interface voltage between 1.6 to 5.5V
- Wide range of clock voltage between 1.6 to 5.5V
- Low power consumption at 0.5μA/3.0V (TYP.)
- Available in two small packages: SOP-14 pin and VSOJ-20 pin. This is mostly suited for high density mounting.

■ Overview

This module is a serial interface real time clock that has a built-in crystal unit. The module offers many functions such as clock & calendar circuitry with automatic leap year adjustment (from seconds to year), alarm, and regular cycle interrupt. In addition, it can detect stopping of oscillation and time update. The serial interface can be controlled by three signal lines, and it enables minimum number of ports required in the system. Because it is available in two small packages, SOP-14 pin and VSOJ-20 pin, in high density mounting, it is ideally suited for applications such as mobile phones, handy terminals or other small electronic systems.

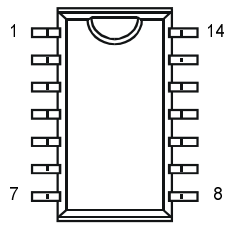
■ Block diagram



■ Terminal description

RTC - 4574SA

1. GND
2. FOUT
3. N.C.
4. N.C.
5. N.C.
6. N.C.
7. V_{DD}

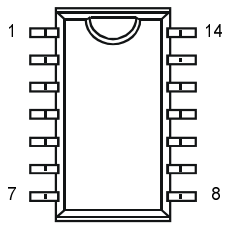


14. FCON
13. CE1
12. DATA
11. CLK
10. / TIRQ
9. / AIRQ
8. CE0

SOP - 14pin

RTC - 4574SA

1. GND
2. FOUT
3. N.C.
4. N.C.
5. N.C.
6. N.C.
7. V_{DD}



14. FCON
13. CE1
12. DATA
11. CLK
10. / TIRQ
9. / AIRQ
8. CE0

SOP - 14pin

Signal name	Pin No. SOP-14pin (VSOJ20pin)	I/O	Signal description
GND	1 (10)	–	This pin connects to the minus side (ground) of the power.
FOUT	2 (2)	Input	This pin outputs the clock signal of frequency set up at the frequency setup register and FCON input pin. See the following table for details. (CMOS output)
V_{DD}	7 (1)	–	This pin connects to the plus side of the power.
CE0	8 (3)	Input	This is a chip enabled 0 input pin with built-in pull-down resistors. When both CE0 and CE1 pins are at the "H" level, access to this RTC becomes possible.
/AIRQ	9 (4)	Output	This is an open drain output pin dedicated for alarm interrupt.
/TIRQ	10 (5)	Output	This is an open drain output pin dedicated for regular cycle interrupt.
CLK	11 (6)	Input	This is a shift clock input pin for serial data transmission. In the write mode, it takes in data from the DATA pin using the CLK signal rise edge. In the read mode, it outputs data from the DATA pin using the fall edge.
DATA	12 (7)	Bi-directional	This is a data input/output pin for serial data transmission. After the input rise of CE0 or CE1, by using the first 8-bit write data to set the write or read mode, this pin can be set as either input pin or output pin.
CE1	13 (8)	Input	This is a chip enabled 1 input pin. When both CE0 and CE1 pins are at the "H" level, access to this RTC becomes possible. When the CE1 pin is at the "H" level, regardless of the state of the CE0 pin, the FOUT pin is in the output state. When the pin is at the "L" level, the FOUT pin is at the high impedance level.
FCON	14 (9)	Output	This pin controls the FOUT output. When the CE1 pin is at the "H" level, if the FCON pin is set to "L", then regardless of the content of the frequency setup register, the FOUT pin outputs at 32.768 KHz. See the table below for details.
N.C.	3 - 6 (11 - 20)		This pin is not connected internally. Be sure to connect using OPEN, or GND or V_{DD}.

* Be sure to connect a filter capacity of at least 0.1µF close to V_{DD} - GND.

*** Relationship between the FOUT output and RTC access, based on CE0, CE1, FCON pin and FE bit**

CE0	CE1	FCON	FE	FOUT output	RTC access
L	L	*	*	high impedance	no
H	L	*	*	high impedance	no
L	H	L	0	output at 32.768 KHz	no
		L	1	output at 32.768 KHz	no
		H	0	high impedance	no
		H	1	FD bit selection frequency output	no
H	H	L	0	output at 32.768 KHz	yes
		L	1	output at 32.768 KHz	yes
		H	0	high impedance	yes
		H	1	FD bit selection frequency output	yes

■ Characteristics

1. Absolute maximum ratings

GND=0V

Parameter	Symbol	Condition	Rating	Unit
Power voltage	V_{DD}	–	-0.3 to +7.0	V
Input voltage	V_{IN}	input pin	GND-0.3 to V_{DD}+0.3	V
Output voltage (1)	V_{OUT1}	/TIRQ, /AIRQ	GND-0.3 to +0.8	V
Output voltage (2)	V_{OUT2}	FOUT, DATA	GND-0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	–	-55 to +125	°C

2. Operating conditions

GND=0V

Parameter	Symbol	Condition	Range	Unit
Power voltage	V_{DD}	–	1.6 to 5.5	V
Clock voltage	V_{CLK}	–	1.6 to 5.5	V
Operating temperature	V_{OPR}	–	-40 to +85	°C

3. Oscillation characteristics

Parameter	Symbol	Condition	Specification	Unit
Frequency precision	$\Delta f/f_O$	Ta=+25°C, V_{DD}=3.0V	± 23 *	ppm
Oscillation start time	tSTA	Ta=+25°C, V_{DD}=1.6V	3 (MAX)	sec
Frequency temperature characteristics	Top	-10 to +70°C, +25°C as reference	+10 / -120	ppm
Frequency voltage characteristics	f/V	Ta=+25°C, V_{DD}=1.6 to 5.5V	± 2.0	ppm/V
Aging	fa	Ta=+25°C, V_{DD}=3.0V	± 5.0	ppm/year

* Equivalent to 1 minute of monthly deviation

4. DC characteristics

If not specifically indicated, GND=0V, V_{DD}=1.6 to 5.5V, Ta= -40 to +85°C

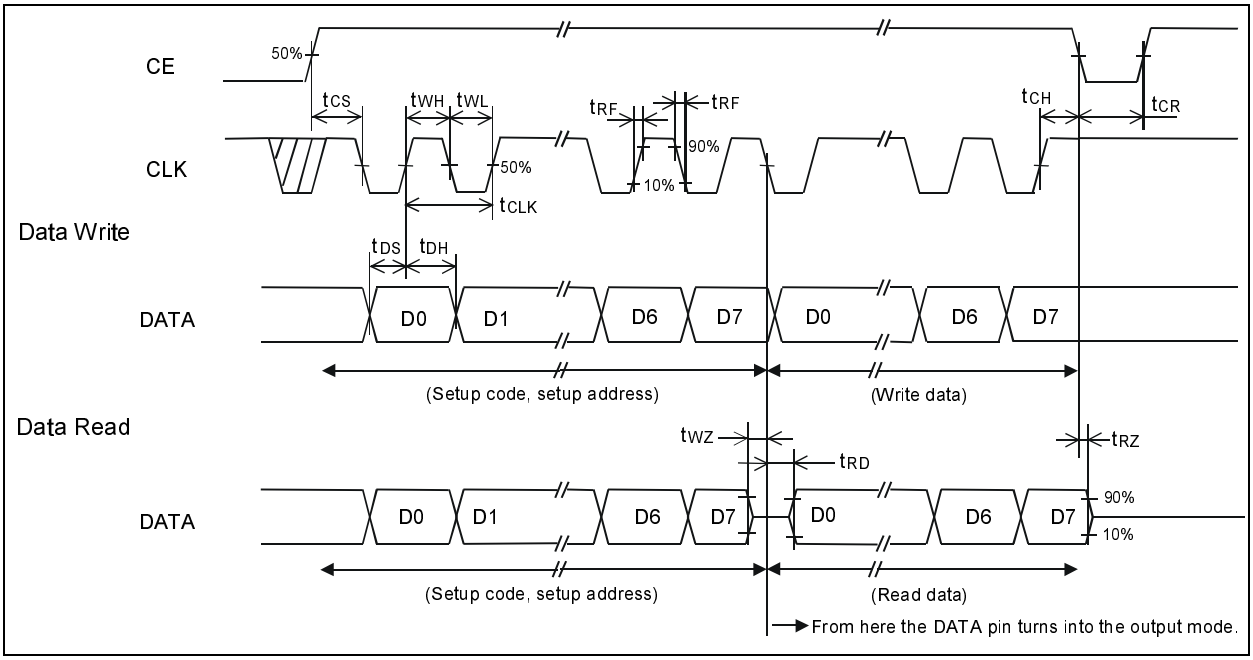
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Current consumption (1)	I_{DD1}	V_{DD}=5V	CE0,CE1=GND and		1.0	2.0	µA
Current consumption (2)	I_{DD2}	V_{DD}=3V	DATA, /AIRQ, /IRQ=V_{DD}		0.5	1.0	µA
Current consumption (3)	I_{DD3}	V_{DD}=5V, CL=0pF	When at 32.768 KHz output,		3.0	7.5	µA
Current consumption (4)	I_{DD4}	V_{DD}=3V, CL=0pF	CE0=GND and		1.7	4.5	µA
Current consumption (5)	I_{DD5}	V_{DD}=5V, CL=30pF	CE1, DATA, /AIRQ,		8.0	20.0	µA
Current consumption (6)	I_{DD6}	V_{DD}=3V, CL=30pF	/TIRQ=V_{DD}		5.0	12.0	µA
Input voltage	V_{IH}	CE0,CE1,CLK,DATA,FCON pins		0.8 V_{DD}		V_{DD}	V
	V_{IL}			0		0.2 V_{DD}	V
Input leakage current	I_{LK}	CE0,CE1,CLK,FCON pins V_{IN}= V_{DD} or GND		-0.5		0.5	µA
Input resistance (1)	R_{DWN1}	V_{DD}=5V	CE0 pin	75	150	300	KΩ
Input resistance (2)	R_{DWN2}	V_{DD}=3V	V_{IN}= V_{DD}	150	300	600	KΩ
Output voltage (1)	V_{OH1}	V_{DD}=5V, I_{OH}=-1mA	DATA, FOUT pins	4.5		5.0	V
	V_{OH2}	V_{DD}=3V, I_{OH}=-1mA		2.0		3.0	V
	V_{OH3}	V_{DD}=3V, I_{OH}=-100µA		2.9		3.0	V
Output voltage (2)	V_{OL1}	V_{DD}=5V, I_{OH}=-1mA	DATA, FOUT pins	GND		GND+0.5	V
	V_{OL2}	V_{DD}=3V, I_{OH}=-1mA		GND		GND+0.8	V
	V_{OL3}	V_{DD}=3V, I_{OH}=-100µA		GND		GND+0.1	V
	V_{OL4}	V_{DD}=5V, I_{OH}=-1mA	/AIRQ, /TIRQ pins	GND		GND+0.25	V
	V_{OL5}	V_{DD}=3V, I_{OH}=-1mA		GND		GND+0.4	V
Output leakage current	I_{OZ}	DATA, /AIRQ,/TIRQ pins V_{OUT}=V_{DD} or GND		-0.5		0.5	µA

5. AC characteristics

If not specifically indicated, GND=0V, Ta= -40 to +85°C

Parameter	Symbol	Condition	V_{DD}=3V±10%			V_{DD}=5V±10%			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
CLK clock cycle	t_{CLK}		800			350			ns
CLK H pulse width	t_{WH}		400			175			ns
CLK L pulse width	t_{WL}		400			175			ns
CE setup time	t_{CS}		400			175			ns
CE hold time	t_{CH}		400			175			ns
CE recovery time	t_{CR}		600			300			ns
Write data setup time	t_{DS}		100			50			ns
Write data hold time	t_{DH}		80			50			ns
Write data disable time	t_{WZ}		0			0			ns
Read data delay time	t_{RD}	CL=50pF			300			120	ns
Output disable time	t_{RZ}	CL=50pF RL=10K			200			100	ns
Input rise/fall time	t_{RF}				100			50	ns
FOUT duty (when output at 32.768kHz)	Duty		35		65	40		60	%
Oscillation stop detection time	t_{OSC}		10			10			ms

Timing chart



■ Registers

1. Register table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	second	fos	40	20	10	8	4	2	1	permitted	permitted
1	minute	fr	40	20	10	8	4	2	1	permitted	only bit 7 not permitted
2	hour	fr	–	20	10	8	4	2	1	permitted	only bit 7 not permitted
3	day of week	fr	6	5	4	3	2	1	0	permitted	only bit 7 not permitted
4	day	fr	–	20	10	8	4	2	1	permitted	only bit 7 not permitted
5	month	fr	–	–	10	8	4	2	1	permitted	only bit 7 not permitted
6	year	80	40	20	10	8	4	2	1	permitted	permitted
7	minute alarm	AE	40	20	10	8	4	2	1	permitted	permitted
8	hour alarm	AE	*	20	10	8	4	2	1	permitted	permitted
9	day of week alarm	AE	6	5	4	3	2	1	0	permitted	permitted
A	day alarm	AE	*	20	10	8	4	2	1	permitted	permitted
B	frequency setup	FE	*	FD4	FD3	*	FD2	FD1	FD0	permitted	permitted
C	regular cycle setup	TE	*	TD1	TD0	*	*	*	*	permitted	permitted
D	regular cycle counter	128	64	32	16	8	4	2	1	permitted	permitted
E	control 1	–	–	–	TI/TP	AF	TF	AIE	TIE	permitted	permitted (note 3)
F	control 2	–	TEST	STOP	RESET	HOLD	–	–	–	permitted	permitted

Note 1: At the initial power supply, the values of all registers are not fixed and so initial set is required.
Note 2: By reading address "D", the preset data value of the previous write can be read.
Note 3: Write is possible only when the AF and TF bits are "0".
Note 4: Before using the device, set values indicated with "-" to "0" after the initial setup.
Note 5: Values indicated with "*" can be used as memory.
Note 6: TEST is the testing bit for use by Epson. Always set it to "0" when using the device.

2. Clock and calendar registers (Reg-0 to Reg-6)

- Data is in the BCD format. For example, if the second register is "0101 1001", this means 59 seconds.
  The time measurement uses the 24-hour format.

- If the alarm interrupt is not used, registers 7 to B can be used as 8-bit memory register. In this case, be sure to set the AIE bit to "0" and forbid use of the alarm interrupt.

- If the regular cycle interrupt is not used, registers C and D can be used as 8-bit memory register. In this case, be sure to set the TIE bit to "0" and forbid use of the regular cycle interrupt.

- Year register and leap year
  If the year register's 2-digit BCD is divided by four and the remainder is 0, this year is determined as the leap year. This works automatically for both the Western calendar as well as the Japanese Heisei calendar. As a note, the next leap year after 99 is 00.

- Day of week register
  The day of week register makes use of the 7 bits from 0 to 6. The bits are assigned as shown in the following table. Be sure not to set multiple day of week to "1".

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day of week
fr	0	0	0	0	0	0	1	Sunday
fr	0	0	0	0	0	1	0	Monday
fr	0	0	0	0	1	0	0	Tuesday
fr	0	0	0	1	0	0	0	Wednesday
fr	0	0	1	0	0	0	0	Thursday
fr	0	1	0	0	0	0	0	Friday
fr	1	0	0	0	0	0	0	Saturday

- **fos** (OSC flag)

This flag is for recording when the oscillation stops. This bit is used to detect when decrease in the power voltage causes the oscillation to stop. "1" indicates oscillation has stopped and this information is kept until "0" is written to it. This flag is not affected even when other bits (STOP, RESET) are "1".

- **fr** (READ flag)

This flag is a bit which becomes "0" when the RTC is set to the non-selection state (either CE0 or CE1 input pin becomes "L"), or "1" when the RTC is set to the selection state (both CE0 or CE1 input pin becomes "H") during which there is a 1 second digit increase. Because of this characteristic, it becomes possible to determine whether a 1 second digit increase has occurred during read-out of the clock register. If fr is "1", it becomes necessary to read all the clock registers again.

3. Alarm registers (Reg-7 to Reg-A)

Alarm can be set to day of week, day, hour, or minute. Each of the respective alarm register has the AE bit (alarm enable bit) attached to bit 7. By taking advantage of this bit, the hourly alarm and daily alarm can easily be set up. The day of week alarm can be set to multiple days of the week. When the AE bit is "0", the appropriate register and the clock register are compared; when the bit is "1", this means "don't care" and so data is ignored and the two are regarded as the same. When the AIE bit of Reg-E is "0", output from the /AIRQ pin will be prohibited. Therefore, to perform alarm interrupt, the AIE bit must be set to "1".

The relationship between the day of week alarm bit and each day of the week is shown as follows:

bit	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Day of week	AE	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

4. Output frequency setup register (Reg-B)

bit	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	FE	–	FD4	FD3	–	FD2	FD1	FD0

When the FE bit is set to "1", the split-cycled clock impulse is output from the FOUT pin at the split cycle ratio which specifies the frequency (source clock). When the FE bit is set to "0", the output is prohibited (high impedance).

● Source clock selection

FD4	FD3	Source clock
0	0	32768Hz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

● Split cycle ratio selection

FD2	FD1	FD0	Split cycle ratio	FOUT Duty
0	0	0	1/1	50%
0	0	1	1/2	50%
0	1	0	1/3	33%
0	1	1	1/6	50%
1	0	0	1/5	20%
1	0	1	1/10	50%
1	1	0	1/15	33%
1	1	1	1/30	50%

* When the FCON pin is "L", regardless of the output frequency setup register (FE bit, FD bit), the FOUT output frequency is 32.768 KHz.

● FOUT output frequency

Split cycle ratio / Source clock	1/1	1/2	1/3	1/5	1/6	1/10	1/15	1/30
32768Hz	32768Hz	16384Hz	10922Hz	6553.6Hz	5461Hz	3276.8Hz	2184.5Hz	1092.3Hz
1024Hz	1024.0Hz	512.0Hz	341.3Hz	204.8Hz	170.67Hz	102.4Hz	68.27Hz	34.13Hz
32Hz	32.0Hz	16.0Hz	10.67Hz	6.4Hz	5.33Hz	3.2Hz	2.13Hz	1.07Hz
1Hz	1s	2s	3s	5s	6s	10s	15s	30s

5. Regular cycle setting and regular cycle counter register (Reg-C, Reg-D)

This is the register for controlling the presettable binary down counter of the 8 bits used during the regular cycle interrupt. Reg-C specifies the source clock of the counter, and Reg-D specifies the split cycle value of the counter. During a source clock cycle, the timer count register counts down and when the data becomes zero, the /TIRQ pin goes to the LOW level. When the TI/TP bit becomes "1", the regular cycle counter register reloads the data and starts the count down again. When the TIE bit of Reg-E becomes "0", output from the /TIRQ pin is prohibited. In order to operate the timer as planned, it is necessary to set up the TI/TP and TIE bits.

● Source clock selection

TD1	TD0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	Update in seconds
1	1	Update in minutes

● Regular cycle interrupt interval

Split cycle ratio / Regular cycle counter setting value	4096Hz	64Hz	Update in seconds	Update in minutes
0	–	–	–	–
1	244.14μs	15.625ms	1s	1min
2	488.28μs	31.250ms	2s	2min
3	732.42μs	46.875ms	3s	3min
·	·	·	·	·
·	·	·	·	·
·	·	·	·	·
255	62.26ms	3.984s	255s	255min

When data write to Reg-D occurs, the presettable counter is updated. Because the data is kept until data written to Reg-D is written again, it can be used as RAM when the regular cycle interrupt is not used (TIE=0)

When the TE bit becomes "0", the presettable counter loads the content of the regular cycle counter and stops counting. When the TE bit becomes "1", counting starts again. Also, when the TE bit is in the "1" state, setting the "0" data to the regular cycle counter (Reg-D) does not result in regular cycle interrupt from the TIRQ pin.

6. Control register 1 (Reg-E)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	–	–	–	TI/TP	AF	TF	AIE	TIE

- **TI/TP bit:** (Interrupt Signal Output Mode Select. Interrupt/Periodic)

This bit sets up the output mode of the regular cycle interrupt signal.

TI/TP	0	1
Function	Level interrupt mode As soon as the regular cycle interrupt occurs, the /TIRQ pin becomes "L" and the TF bit becomes "1". The TIRQ pin remains at "L" until "0" is written to the TF bit. (However TIE=1)	Repeat interrupt mode As soon as the regular cycle interrupt occurs, the /TIRQ pin becomes "L" (however TIE=1) and the TF bit becomes "1". Then, the /TIRQ pin returns to "Hi-Z". The TF bit remains as "1" until "0" is written to it.

- **AF and TF bits:** (Alarm Flag , Timer Flag)

When an alarm occurs the AF bit becomes "1", and the TF bit becomes "1" when the timer is zero. Data is kept until both "0" is written to the two bits. "1" cannot be written to both bits.

- **AIE and TIE bits:** (Alarm , Timer Interrupt Enable)

When the alarm and regular cycle interrupt events occur, these bits determine which IRQ pin to drive. The AIE bit controls the alarm and the TIE bit controls the regular cycle. When the AIE bit becomes "0", the /AIRQ pin is at the high impedance level. When the TIE bit becomes "0", the /TIRQ pin is at the high impedance level.

7. Control register 2 (Reg-F)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	–	TEST	STOP	RESET	HOLD	–	–	–

- **TEST bit:** this bit is reserved for testing work by Epson.

Be sure to set this bit to "0" always. Be careful not to set this bit to "1" accidentally when writing to other bits of Reg-F. It can be cleared by setting CE0 or CE1 to "L".

- **STOP bit**

When this bit is set to "1", the clock stops after 2 KHz of split cycle counter. When this bit becomes "0" the clock resumes. Use this bit together with the RESET bit when writing clock data.

- **RESET bit**

When this bit is set to "1", the counter between 2 KHz and 1 Hz is reset. After "1" is written to this bit, this can be released by setting CE to "L". This bit is not influenced by states of the other bits.

- **HOLD bit**

When this bit is set to "1", second digit increase is prohibited. If second digit increase happens with this bit set to "1", when this bit returns to "0" the automatic compensation will work to correct by one second.
It is recommended that the HOLD bit be within one second.

● Function description table

Bit			Function			
STOP	RESET	HOLD	Clock	Timer	Alarm	FOUT
0	0	0	runs	runs	runs	runs
0	0	1	*1	*2	stops	runs
0	1	0	stops	*3	stops	*4
0	1	1	stops	*3	stops	*4
1	0	0	stops	*3	stops	*4
1	0	1	stops	*3	stops	*4
1	1	0	stops	*3	stops	*4
1	1	1	stops	*3	stops	*4

*1: If the deviation is within one second, the automatic compensation function will kick in to perform the automatic compensation.
*2: Runs at source clock other than source clock at 1/60 Hz (1 min).
*3: Runs when the source clock is at 4096 Hz.
*4: Runs when the source clock is at 32768 Hz.

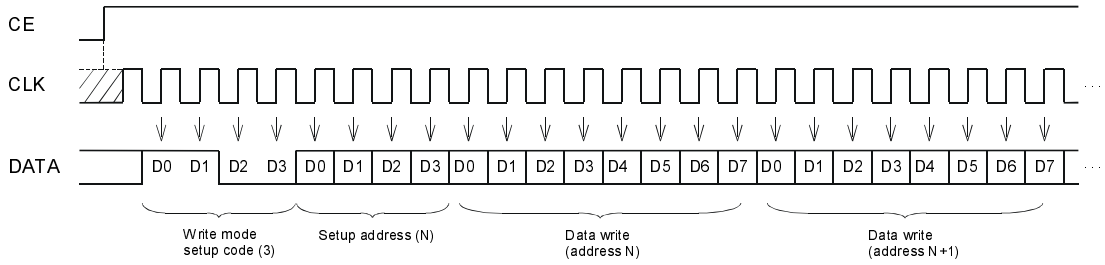
■ How to use

1. Read/write of data

After read/write and the CE input rise, the 4-bit mode is set up and then the 4-bit address is specified. Then, data read/write in units of 8 bits is performed. If input of unit of 8-bit data is not finished before the CE input falls, the 8-bit data will be ignored. (The previous data is undetermined.) . Both read and write use LSB-First.

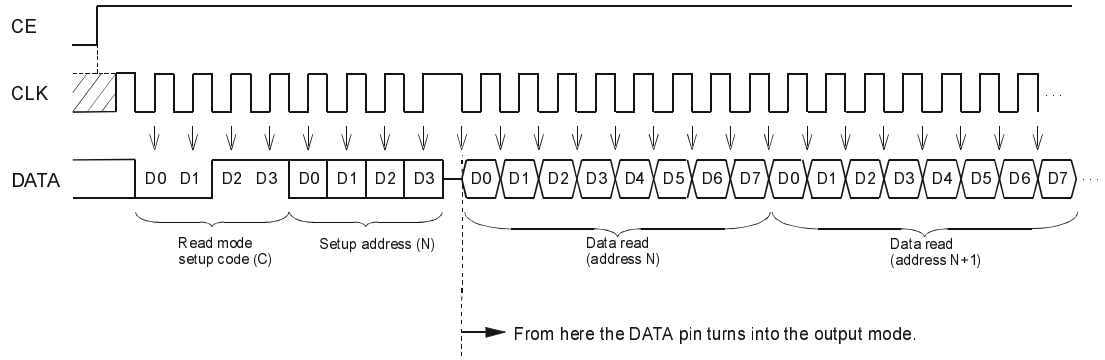
[Write]

1) Take "3" as the write mode in the first four bits after the CE input rise, and set the address to write to the next four bits.
2) The next 8 bits of write data is written to the address set earlier, and the next 8 bits of data is written to the address which is automatically incremented from the last one.
3) The address is incremented automatically in a cycle where address "F" is followed by "0".



[Read]

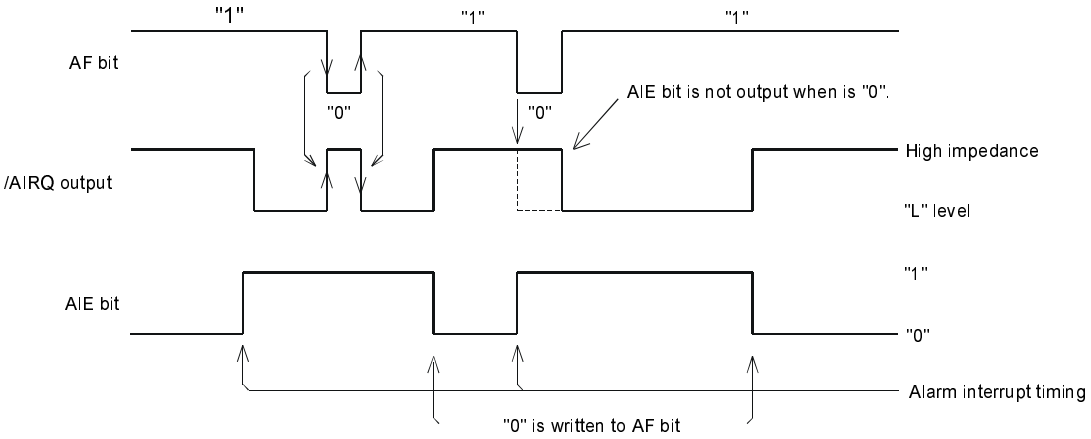
1) Take "C" as the read mode in the first four bits after the CE input rise, and set the address to read to the next four bits.
2) The next 8 bits of read data is read from the address set earlier, and the next 8 bits of data is read from the address which is automatically incremented from the last one.
3) The address is incremented automatically in a cycle where address "F" is followed by "0".



In the mode setting code, if a value other than "C" or "3" is used, the subsequent data will be ignored and the DATA pin remains in the input state.

2. Alarm interrupt

When the alarm matches and AIE=1, the /AIRQ pin outputs "L"; when AIE=0, the /AIRQ pin is at the high impedance level. The alarm interrupt is output when "carry" from the 10-second digit to minute digit occurs



● How to use it

The day of week, day, hour, and minute can be set. For day of week, multiple days can be set at a time. To avoid unintended hardware interrupt during the alarm setup, it is recommended that initially both the AF bit and AIE bit be set to "0". Then, set up the alarm data, and apply zero clear to the AF flag in order to initialize the alarm circuitry with certainty. Afterwards, set the AIE bit to "1". If no hardware is desired to be used, set the AIE bit to "0", and monitor the AF bit with software as required.

● Usage example

1) Set the alarm to go off at 6 pm tomorrow
   - Write "0" to the AIE bit and the AF bit.
   - Write "1" to the AE bit of the day alarm.
   - Get the current day of week stored in register 3 in the day of week alarm register, left shift the data by 1 bit and then perform the write operation. (Be careful with the fr bit. If bit 6 is "1" (Saturday), write "01H (Sunday).)
   - Write "18h" to the hour alarm register.
   - Write "00h" to the minute alarm register.
   - Apply zero clear to the AF bit.
   - Write "1" to the AIE bit.

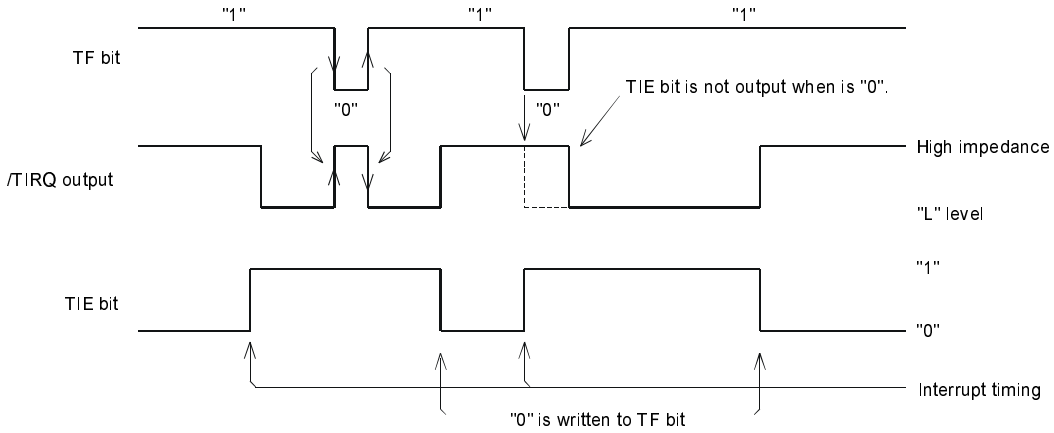
2) Set the alarm to go off 6 am everyday except Saturday and Sunday
   - Write "0" to the AIE bit and the AF bit.
   - Write "1" to the AE bit of the day alarm.
   - Write "3Eh" to the day of week alarm register.
   - Write "06h" to the hour alarm register.
   - Write "00h" to the minute alarm register.
   - Apply zero clear to the AF bit.
   - Write "1" to the AIE bit.

3. Regular cycle interrupt

By setting the TI/TP bit, it is possible to select the level interrupt mode as well as the repeat interrupt mode.

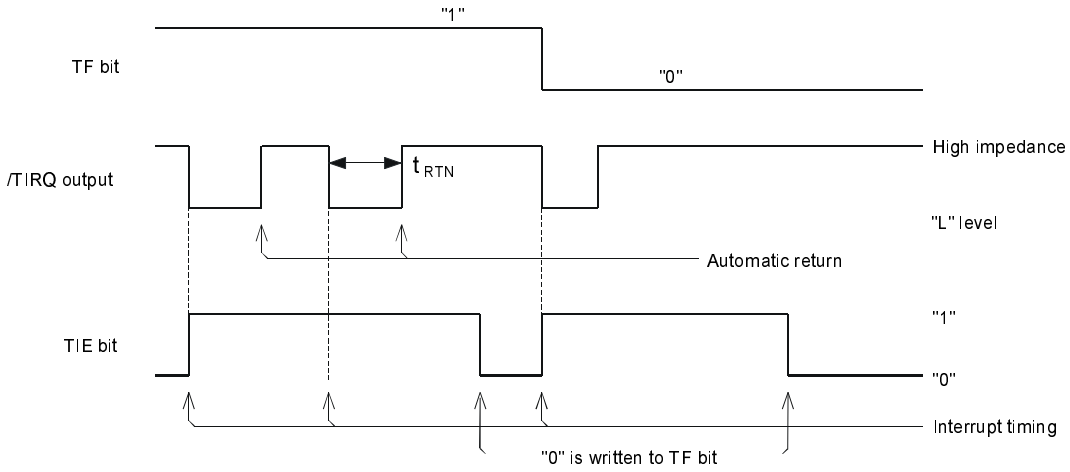
(1) Level interrupt mode (TI/TP = "0")

If TIE=1 when interrupt occurs, the /TIRQ pin becomes "L" output; and TIE=0, the TIRQ pin enters the high impedance state.



(2) Repeat interrupt mode (TI/TP = "1")

- When interrupt occurs, if TIE = 1, the /TIRQ pin outputs "L".
- When interrupt occurs, if TIE= 0, the /TIRQ pin remains at the high impedance level; only the TF pin becomes "1" and stays that way.



● How to use

At the cycle (source clock) specified at the regular cycle interrupt setup register, count down starts from the value of the regular cycle counter register. When the data becomes zero, the /TIRQ pin becomes "L" and interrupt occurs.

It can be used as an interval timer between a minimum of 1/4096 second to a maximum of 255 minutes. To avoid unintended hardware interrupt during the timer setup, it is recommended that initially both the TF bit and the TIE bit be set to "0".

If no regular interrupt is desired to be used, set the TIE bit to "0", and monitor the TF bit with software as required.

● Automatic return

The automatic return time (tRTN) in the repeat interrupt mode is determined by the source clock specified at Reg-C.

Source clock	Automatic return time (tRTN)
4069Hz	0.122ms
64Hz	7.81ms
1Hz	7.81ms
1/60Hz (1min)	7.81ms

● Timer measurement error

Because the timer error is the +0/-1 cycle time of the selected source clock, the timer's set time falls into the following range:

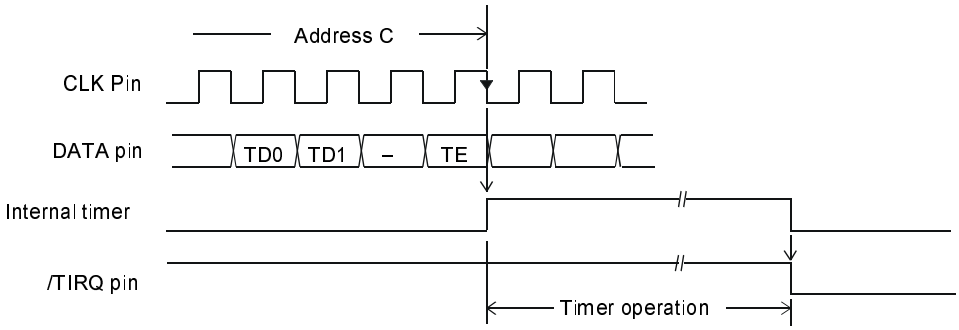
(Timer's set time - source clock cycle) to (Timer's set time)

* Timer's set time = source clock cycle × value of the split cycle of Reg-D

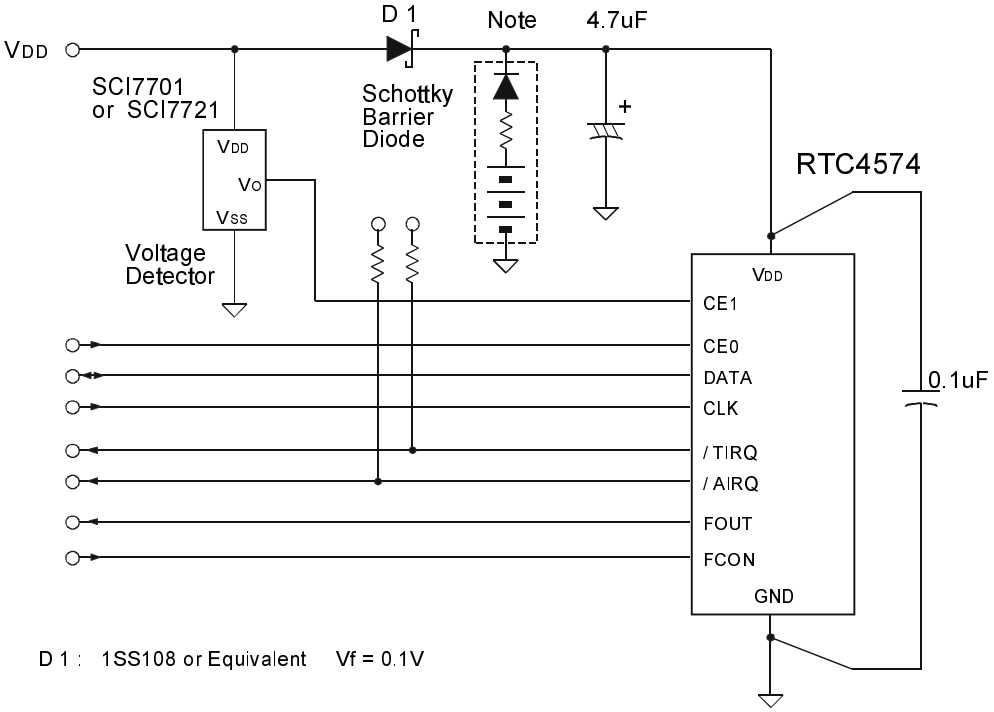
Also, the actual time of the timer is the above time, plus the communication duration of the serial data transfer clock

● Timer start timing

In the data write mode, the timer starts counting from the fall edge of the CLK for the TE bit in the following time chart.

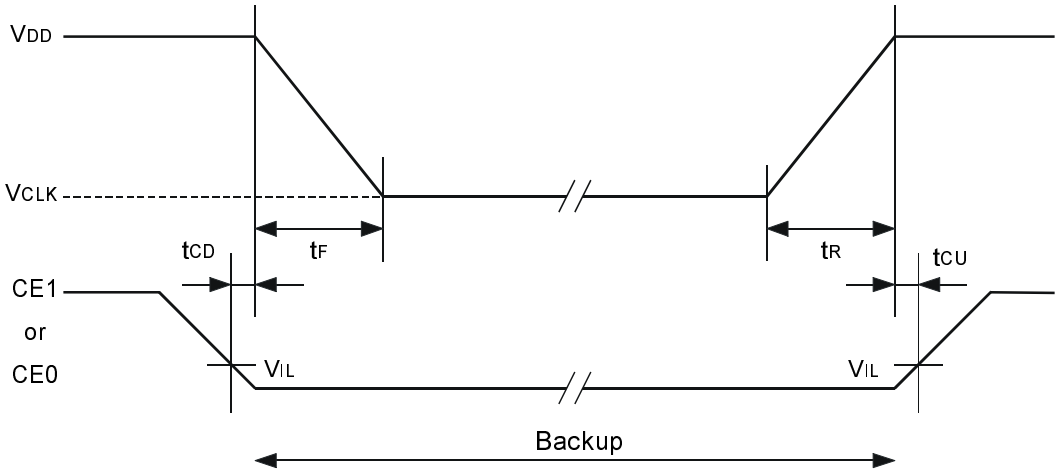


■ External connection example



Note: It uses the secondary battery or a lithium battery. When using the seconding battery, the diode is not required. When using the lithium battery, the diode is required. For detailed value on the resistance, please consult a battery maker.

■ Migrating to backup, and returning

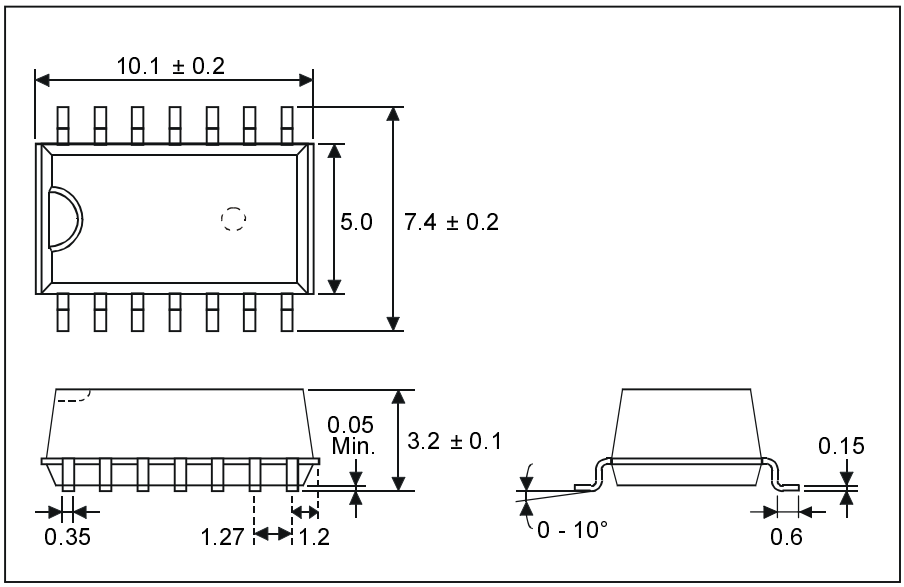


Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CE time before power drop	t_{CD}	–	0			μs
Power drop time	t_F	(V_{DD} -V_{CLK}) ≤ 2.0V (V_{DD} -V_{CLK}) > 2.0V	2 50			μs/V
Power rise time	t_R		1			μs/V
CE time after power rise	t_{CU}		0			μs

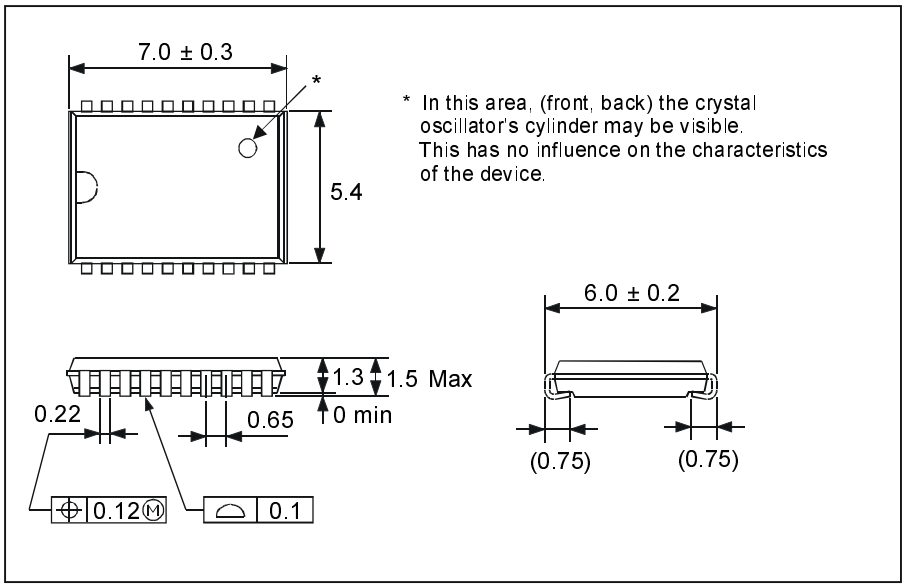
* When migrating to backup, before switching the power source, make sure CE1 or CE0 is definitely LOW and RTC is not selected

■ External dimension

● **RTC-4574SA (SOP 14-pin)**

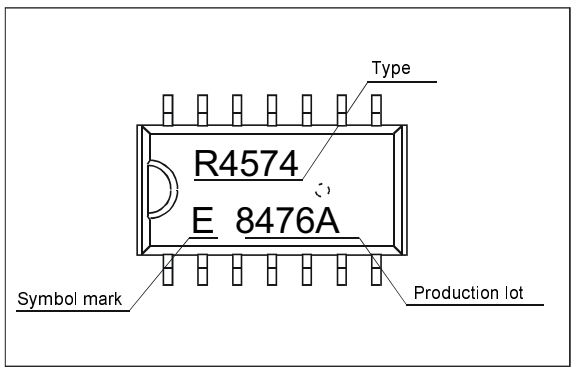


● **RTC-4574JE (VSOJ 20-pin)**

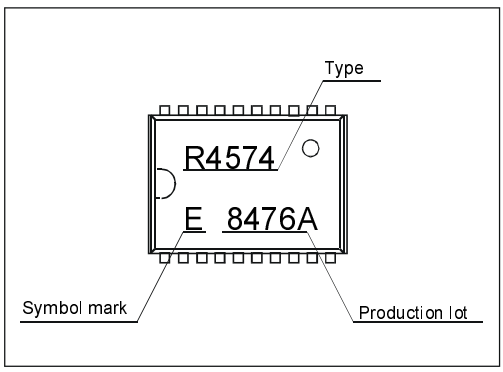


■ Marking layout

● **RTC-4574SA (SOP 14-pin)**



● **RTC-4574JE (VSOJ 20-pin)**



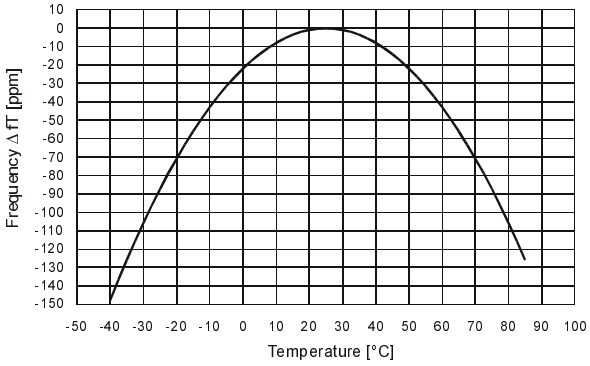
Note: The above indication shows the markings and outlines their general positions. It is not a specification of the type faces, sizes, and positions of the characters.

■ Reference data

(1) Frequency temperature characteristics example

θ_T = +25°C TYP.

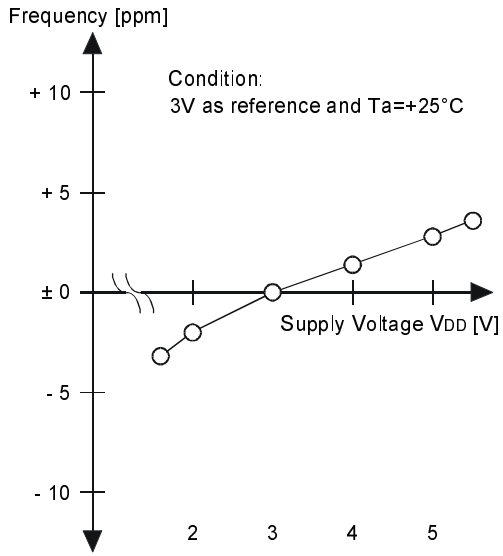
α = -0.035ppm/°C^2 TYP.



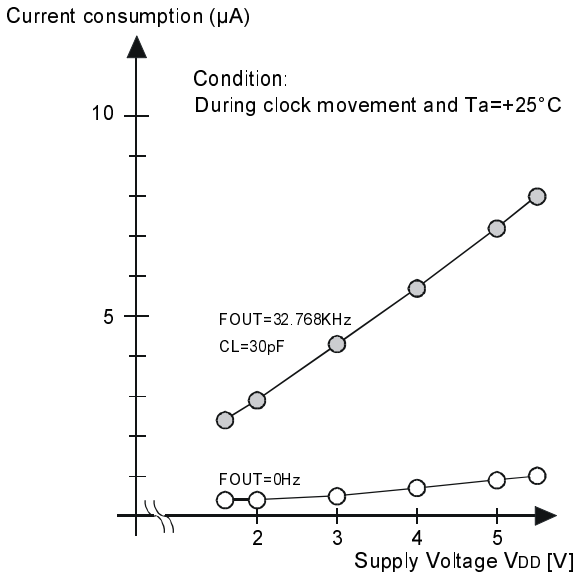
Finding the frequency stability (clock accuracy

1. The frequency temperature characteristics can be approximated by using the following formula:
   $\Delta f_T(ppm)=(\theta_T-\theta x)^2$
   - Δf_T (ppm) : Frequency deviation at target temperature
   - α (ppm/°C) : Secondary temperature coefficient (-0.035±0.005ppm/°C^2)
   - θ_T (°C) : Peak temperature (25°C±5°C)
   - θx (°C) : Target temperature
2. To determine the overall clock accuracy, add the frequency precision and the voltage characteristics:
   $\Delta f/f(ppm) = \Delta f/f_0 + \Delta f_T + \Delta fv$
   - $\Delta f/f$ (ppm) : Clock accuracy at a given temperature and voltage (frequency stability
   - $\Delta f/f_0$ (ppm) : Frequency precision
   - Δf_T (ppm) : Temperature dependent frequency deviation
   - Δfv (ppm) : Voltage dependent frequency deviation
3. Finding the daily deviation:
   Daily deviation = $\Delta f/f \times 10^{-6} \times 86400$ (seconds)
   The clock error is one second per day at 11.574 ppm.

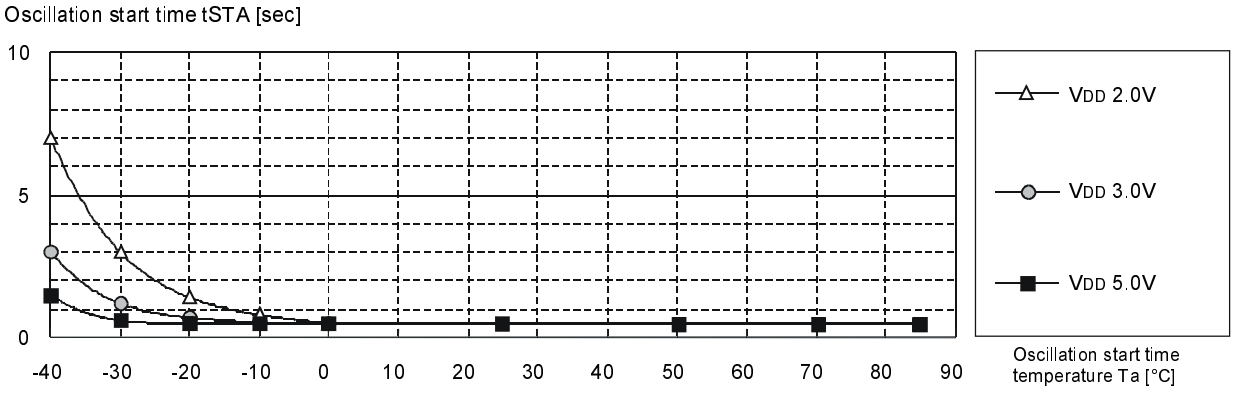
(2) Example of the frequency/voltage characteristics



(3) Example of the current consumption/voltage characteristics



(4) Oscillation start time characteristics



Note: This data is taken from the sample lot. For the rated value, see the specification on page 3.

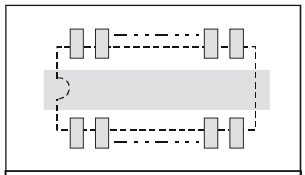
■ Application notes

(1) Notes on handling

In order to enable this module to operate at low power level, the C-MOS circuitry was used in the design of the chip. Note the following cautions when handling it:

1. Static electricity
While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

2. Noise
If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1μF as close as possible to the power supply pins (between V_{DD} and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module. Do not connect signal lines to the shaded area in the figure shown on the right and, if possible, embed this area in a GND land.


Example for the RTC-4574SA

3. Voltage levels of input pins
When the input pins are at the mid-level , this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to V_{DD} or GND.

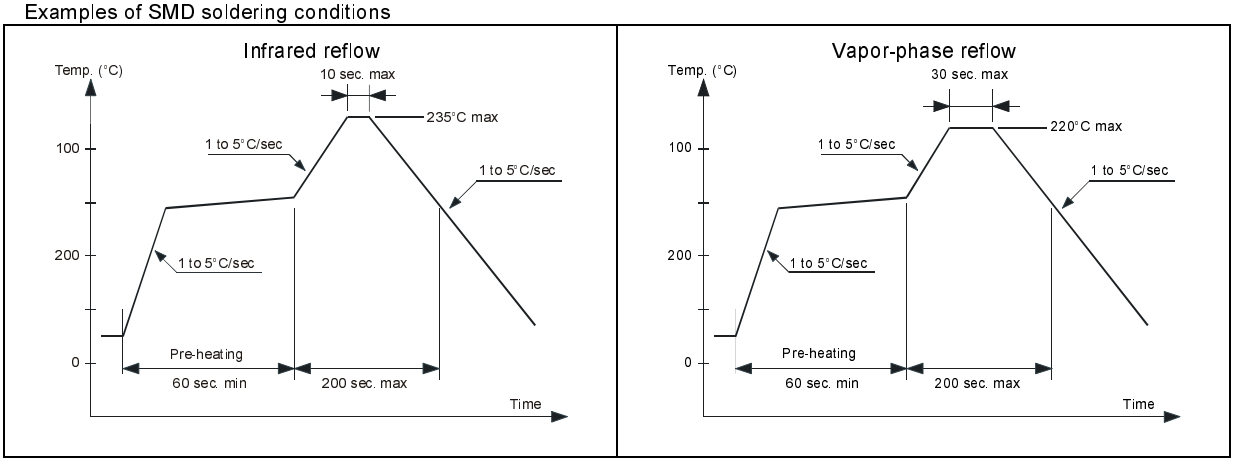
4. Handling unused input pins
Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

(2) Notes on packaging

1. Soldering temperature conditions
If the temperature within the package exceeds 260°C, the characteristics of the crystal unit will be degraded and it may be damaged. Therefore, always check the mounting temperature before mounting this device. Also, check again if the mounting conditions are later changed.

Soldering conditions: Not higher than 260°C for no more than twice at 10 seconds, or not higher than 230°C for no more than 3 minutes

Examples of SMD soldering conditions



2. Mounting equipment
While this module can be used with general-purpose mounting equipment, the internal crystal unit may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

3. Ultrasonic cleaning
Depending on the usage conditions, there is a possibility that the crystal unit will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

4. Mounting orientation
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

5. Leakage between pins
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.