M213-60

EPSON

Application Manual

Real Time Clock Module

RTC-8583

SEIKO EPSON CORPORATION

CONTENTS

■Overview ---- 1

■Block diagram ---- 1

■Terminal connections ---- 1

■Terminal descriptions ---- 2

■Characteristics ---- 3
1. Absolute Maximum Ratings ---- 3
2. Operating Conditions ---- 3
3. Frequency Characteristics ---- 3
4. DC Characteristics ---- 3

■Switching characteristics ---- 4

■Registers ---- 5
1. Register Table ---- 5
2. Notes ---- 5
3. Register functions over view ---- 6
4. Power on reset ---- 6
5. 1 Hz output ---- 7

■Register descriptions ---- 8
1. Control registers ---- 8
(1) TF bit (bit 0) ---- 8
(2) AF bit (bit 1) ---- 8
(3) ALM bit (bit 2) ---- 8
(4) MASK bit (bit 3) ---- 8
(5) MODE1,MODE0 (bit 5, bit 4) ---- 8
(6) HOLD bit (bit 6) ---- 9
(7) STOP bit (bit 7) ---- 9
2. 1/100 seconds register ---- 9
3. Second register ---- 9
4. Minute register ---- 9
5. Hour register ---- 9
(1) AM/PM bit (bit6) ---- 9
(2) 12/24 bit (bit7) ---- 9
6. Year and day register ---- 10
7. Day of the week and month register ---- 10
8. Timer-counter register ---- 10
9. Alarm control register ---- 11
(1) TCP2,TCP1,TCP0 bits (bit2,1,0) ---- 11
(2) TIE bit (bit3) ---- 11
(3) AS1,AS0 bits (bit5,4) ---- 11
(4) TAIE bit (bit6) ---- 11
(5) AIE bit (bit7) ---- 11
10. 1/100 seconds alarm register ---- 12
11. Second alarm register ---- 12
12. Minute alarm register ---- 12
13. Hour alarm register ---- 12
14. Year and day alarm register ---- 12
15. Month and day of the week alarm register ---- 12
16. Timer alarm register ---- 12
17. User RAM ---- 12

■Access procedure ---- 13
1. Characteristic of the I²C BUS ---- 13
2. Bit transfer ---- 13
3. Start condition and stop condition ---- 13
4. Slave address ---- 13
5. System structure ---- 14
6. Acknowledge ---- 14
7. I²C-BUS protocol ---- 14
(1) Write procedure with specifying the address ---- 14
(2) Read procedure with specifying the address ---- 14
(3) Read procedure without specifying the address ---- 15

RTC-8583

■Typical applications ---- 16

■Reference data ---- 17
1. Frequency temperature characteristics ---- 17
2. Example of the frequency/voltage characteristics ---- 17
3. Example of the current consumption/voltage characteristics ---- 17
4 Note ---- 17

■External dimension ---- 18

■Marking layout ---- 18

■Application notes ---- 19
1. Notes on handling ---- 19
(1) Static electricity ---- 19
(2) Noise ---- 19
(3) Voltage levels of input pins ---- 19
(4) Unused signal pins ---- 19
2. Notes on packaging ---- 19
(1) Soldering temperature conditions ---- 19
(2) Mounting equipment ---- 19
(3) Ultrasonic cleaning ---- 19
(4) Mounting orientation ---- 19
(5) Leakage between pins ---- 19

EPSON

— I²C-BUS COMPATIBLE REAL TIME CLOCK MODULE

RTC-8583

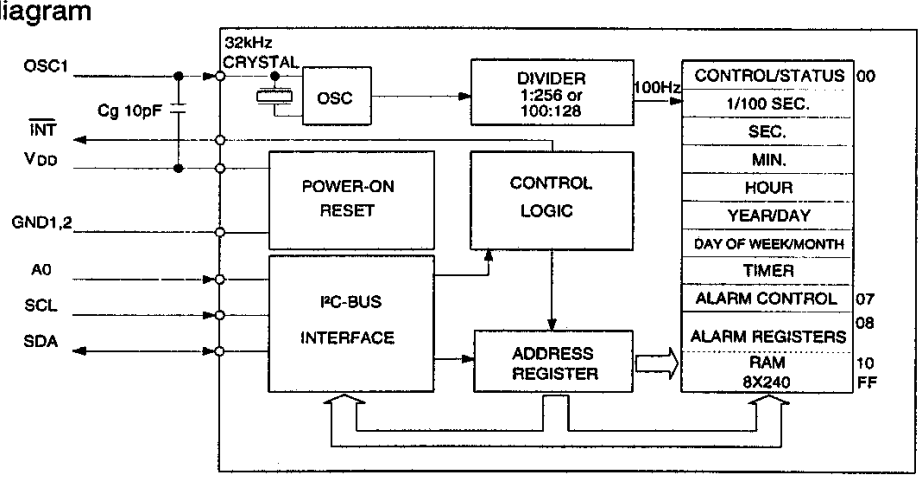
- The Built-in Quartz Crystal Makes The Product Streamlined and Adjustment Free with 10pF External Capacitor
- The Small Package Makes High Density Mounting Possible (SOP-14 Pin)
- Three mode operations internal crystal oscillation, external 50Hz clock and an event counter
- I²C-BUS Interface Compatible
- Built-in 240 × 8 bit S-RAM
- Alarm and Timer Functions are Available
- Wide Operating Voltage Range 2.5V to 6.0V
- Wide Data Holding Voltage Range 1.0V to 6.0V
- Power-on reset function and 1 Hz output function

The I²C-BUS is a trademark of PHILIPS ELECTRONICS N.V.

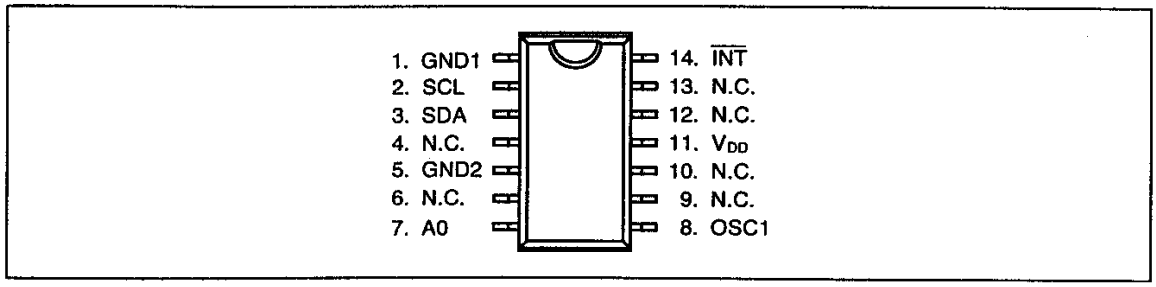
■Overview

This is a real time clock module that has a built-in quartz crystal. The module gives many functions such as calendar clock, alarm, timer, universal RAM that can be controlled with a two (2) lines interface. The event counter function can be used without using the internal crystal's oscillation.
This module is ideally suited for applications requiring many functions with an SMD package such as portable telephones, handy-terminals and other small systems.

■Block diagram



■Terminal connections



RTC-8583

■Terminal descriptions

Signal	Pin No.	I/O	Functions
GND1, GND2	1,5		Connect these pins to ground
SCL	2	Input	Serial clock input. Please use appropriate pull-up resistors depending on the capacitance of the lines.
SDA	3	Bi-D	Input/output address, data, acknowledge, etc. Synchonised with a serial clock. This terminal is an N-channel open-drain in output mode. Please use appropriate pull-up resistors depending on the capacitance of the lines.
A0	7	Input	As in the I²C interface, the device selection is executed with a serial interface by the software. The device address is 7 bits, the LSB is selected by this A0 pin for this device.
OSC1	8	Input	Connect a 10pF capacitor. While in the event counter mode, connect an event reference clock.
VDD	11		Connect this pin to the power source. Supply 2.5V to 6.0V to this pin during normal operation; at least 1.0V during data hold mode.
$\overline{INT}$	14	Output	This pin outputs an interrupt signal such as alarm, timer. This terminal is an N-channel open drain.
N.C.	9,10	—	These pins are not connected internally. Please connect to VDD in order to make stable oscillation.
	4,6, 12,13	—	Do not connect them to any terminals.

Note : Be sure to connect a by-pass capacitor of at least 0.1 μF between VDD and GND.

■Characteristics

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	V_{DD}	V_{DD} - GND1,2	-0.8	+7.0	V
Supply Current	I_{DD}	V_{DD} pin		50	mA
Input Voltage	V_I	Input Terminals	GND1,2-0.8	V_{DD}+0.8	V
DC Input Current	I_I			10	mA
DC Output Current	I_O			10	mA
Operating Temperature Range	Ta		-30	+70	°C
Storage Temperature Range	T_{STG}	As Whole Part	-55	+125	°C

2. Operating Conditions

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	V_{DD}	I^2C-BUS Active	2.5	6.0	V
Data Holding Voltage	V_{DD}	Ta=0 to +70°C	1.0	6.0	V
Operating Temperature Range	Ta		-30	+70	°C
External Capacitor	Cg	OSC1-V_{DD}	10pF±5%		pF

3. Frequency Characteristics

Parameter	Symbol	Condition	Max.	Unit
Frequency Tolerance	Δf/fo	Ta=25°C, V_{DD}=5.0V, C_G=10pF	A: 5±20 B: 5± 50	ppm
Temperature Characteristics		Ta=-10 to 70°C, V_{DD}=5.0V	+10 -120	ppm
Voltage Characteristics	f/V	Ta=25°C, V_{DD}=2.0 to 6.0V, 5V reference	±3	ppm
Oscillation start-up time	t_{STA}	Ta=25°C, V_{DD}=5.0V	5	sec
Aging	fa	Ta=25°C, V_{DD}=5.0V	±5	ppm/Yr

Note:
The frequency precision is the guaranteed value when mounted with Cg = 10 pF ± 5%. (Includes the floating capacitance of the circuit pattern on the board.)

4. DC Characteristics

(V_{DD}=2.5 to 6.0V, Ta=-30 to +70°C)

Parameter	Terminal	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current Operating Mode		I_{DDO}	fSCL=100kHz			200	µA
Supply Current Clock Mode		I_{DD}	fSCL=0Hz, V_{DD}=5.0V		10	50	µA
			fSCL=0Hz, V_{DD}=3.0V		3.5	15	µA
			fSCL=0Hz, V_{DD}=2.0V		2.0	10	µA
Power On Reset Voltage		V_{POR}		0.5		0.8	V
"L" Input Voltage	SDA	V_{IL}		-0.8		0.3 × V_{DD}	V
"H" Input Voltage		V_{IH}		0.7 × V_{DD}		V_{DD}+0.8	V
"L" Output Current		I_{OL}	V_{OL}=0.4V	3			mA
Input Leakage		I_L				1	µA
Leakage Current	A0	I_L	V_{IN}=V_{DD} or GND1,2			250	nA
"L" Output Current	$\overline{INT}$	I_{OL}	V_{OL}=0.4V	3			mA
Leakage Current		I_L	V_{IN}=V_{DD} or GND1,2			1	µA
Leakage Current	SCL	I_L	V_{IN}=V_{DD} or GND1,2			1	µA

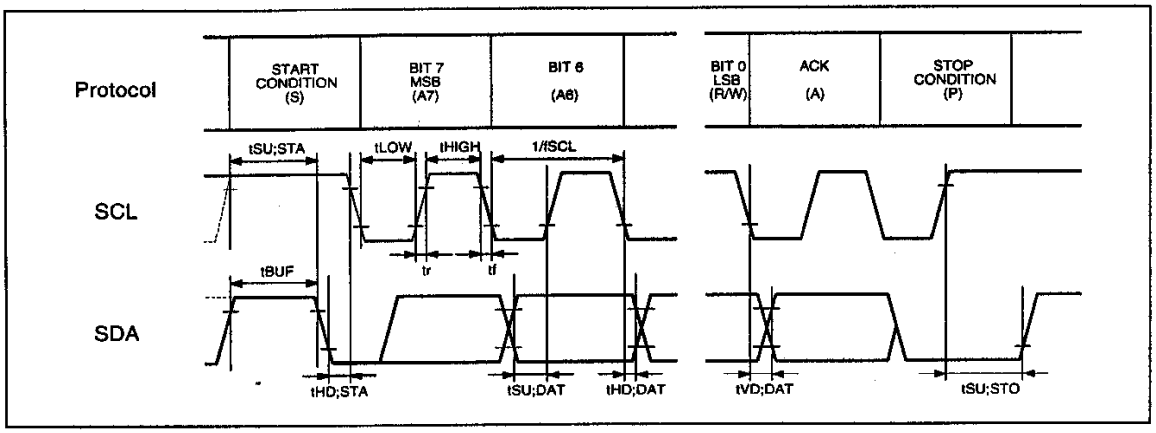
RTC-8583

■Switching characteristics

(VDD=2.5 to 6.0V, Ta=-30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock Frequency	fSCL				100	KHz
Tolerance Spike Width on Bus	tSW				100	ns
Bus Free Time	tBUF		4.7			µs
Start Condition Set-up Time	tSU, STA		4.7			µs
Start Condition Hold Time	tHD, STA		4.0			µs
SCL Low Time	tLOW		4.7			µs
SCL High Time	tHIGH		4.0			µs
SCL and SDA Rise Time	tr				1.0	µs
SCL and SDA Fall Time	tf				0.3	µs
Data Set-up Time	tSU;DAT		250			ns
Data Hold Time	tHD;DAT		0			ns
SCL Low to Data Out Valid	tVD;DAT				3.4	µs
Stop Condition Set-up Time	tSU;STO		4.0			µs
Event Counter Input Frequency	fi				1.0	MHz

Timing Chart



■Registers

1. Register Table

Address	Register name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	CNT	STOP	HOLD	MODE1	MODE0	MASK	ALM	AF	TF
01	1/100 SEC	1/100 seconds							
02	SEC	Second							
03	MIN	Minute							
04	HOUR	12/24	AM/PM	Hour					
05	DAY	Year		Day					
06	MONTH	Day of the week		Month					
07	TIMER	BCD Timer counter							
08	ALARM	AIE	TAIE	AS1	AS0	TIE	TCP2	TCP1	TCP0
09	a-1/100	1/100 seconds alarm							
0A	a-SEC	Second alarm							
0B	a-MIN	Minute alarm							
0C	a-HR	Hour alarm							
0D	a-DAY	Day alarm							
0E	a-MON	Month and day of the week alarm							
0F	a-TIM	Timer alarm							
10		User RAM							
:									
FF									

2. Notes

(1) All data in registers address 1 thru 7 are represented BCD.
(2) Do not set an impossible date or time in the RTC. If such value is set, the effect is unpredictable.
(3) While in the event counter mode, the registers 1 thru 3 are BCD counters which count 0 to 99, the registers 9 thru B are alarm registers corresponding to registers 1 thru 3. The registers 4 thru 6 and C thru E is invalid.
(4) This module has a power-on reset function. Therefore, all registers are initialized to the appropriate value when power-on or the start-up from below the power-on threshold voltage.
(5) The register 0 and 8 contain bits that select the test mode. The test mode is a special operation mode that is used by EPSON for testing. This must not be selected by user. While in the test mode, the operation cannot be guaranteed.

3. Register functions over view

Register	bit	bit name	Functions
0	0	TF	The TF bit is 1 when an overflow has occurred at the timer. When ALM bit is set to 0, this bit is second flag with 50% duty cycle.
	1	AF	The AF bit is 1 when calendar alarm or timer alarm becomes active. When ALM bit is set to 0, this bit is minute flag with 50% duty cycle.
	2	ALM	When ALM bit is set to 1, the alarm functions for calendar and timer work. When this bit is 0, these alarm functions are disabled.
	3	MASK	The MASK bit masks year digit in register 5 and day of the week digit in register 6. With this, the day digit (register 5) and month digit (register 6) can be read directly without any software mask. MASK=0(Normal mode) Register 5 : Data is read that combines year and day digits. Register 6 : Data is read that combines day of the week and month digits. MASK=1(Mask mode) Register 5 : Data is read only day digit. Year digit returns 0. Register 6 : Data is read only month digit. Day of the week digit returns 0.
	4,5	MODE0,1	The mode 0 and mode 1 bits determine operation mode of this module. 00 : This module operates as the real time clock module with internal crystal's oscillation. 01 : This module operates as the real time clock module with external 50Hz clock. 10 : This module operates as the event counter. 11 : This module operates in the test mode. (Do not select this mode)
	6	HOLD	When the HOLD bit is 1, the value of the calendar registers and event counters are held. The internal counter is operating unrelated to the status of this bit. So, when the HOLD bit is released to 0, the value in registers are updated which data is reflected count-ups, etc. while in the hold mode.
	7	STOP	The STOP bit controls the update operation of calendar registers and event counter data. In addition to this operation, the dividers before the second digit are also reset by this bit. When the STOP bit is released to 0, the counting operation restarts from the status of the STOP bit became 1.
1 thru 6		Calendar count registers	These digits are the calendar registers which are written in BCD code. The year digit counts 0 thru 3. The leap year is applied when the value is 0 and counts up to 29 days in February. While in the event counter mode, only the registers 1 to 3 operate as the BCD counters counting from 0 thru 999999.
7		TIMER	This registers is a counter register in BCD code that counts in preset period by TCP2, TCP1 and TCP0 bits.
8	0,1,2	TCP2,1,0	The TCP2, TCP1 and TCP0 bits selects a period for timer counter.
	3	TIE	The TIE bit selects an interrupt output in INT pin when an overflow in the timer counter has occurred. When the TIE bit is 0, an interrupt is disabled, when 1, an interrupt is enabled.
	4,5	AS1,0	The AS1 and AS0 bits specify a comparison range for calendar alarm.
	6	TAIE	The TAIE bit selects an interrupt output in INT pin when a timer alarm has occurred. When the TAIE bit is 0, an interrupt is disabled, when 1, an interrupt is enabled.
	7	AIE	The AIE bit selects an interrupt output in INT pin when a calendar alarm has occurred. When the AIE bit is 0, an interrupt is disabled, when 1, an interrupt is enabled.
9 thru 15		Alarm and timer registers	These alarm registers contains alarm preset data for month, day, day of the week, hour, minute, second, 1/100 second and timer.. The range of comparison in alarm is specified by AS1 and AS0 bits. When the alarm function is not used, these bits can be used as the universal memory.
16-255		RAM	These addresses are the universal memories.

4. Power on reset

Each register after a power-on reset has occurred, will be initialized as follows:

Registers	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	1
6	0	0	0	0	0	0	0	1
8	0	0	0	0	0	0	0	0

The registers that are not mentioned on the above, are unstable after power on reset.

5. 1 Hz output

The 1 Hz output from the INT pin can be controlled according to the following conditions:

1) 1 Hz output conditions
   - The ALM bit of register 0 is set to "0" (indicating that the alarm function is not used) (32 kHz/50 Hz clock mode only)
   - When a power-on reset is generated (because the ALM bit of register 0 is set to "0" by the power-on reset)

2) 1 Hz stop condition
   - The ALM bit of register 0 is set to "1" (indicating that the alarm function is used)

   Note 1: The 1 Hz output cannot be stopped by setting TIE, TAIE, or AIE of register 8 to "0" (disabling output of the respective interrupts).

   Note 2: After the ALM bit of register 0 is changed to "1", there is no guarantee that an alarm or timer interrupt event will not be generated inadvertently, causing the INT pin to go low. Therefore, utilize the following means in order to avoid inadvertent interrupts:
   1) Check the contents of the alarm and timer registers beforehand and reset them if necessary.
   2) Set the AIE bit and TIE bit of register 9 (alarm control register) to "0" (disabling output of timer and alarm interrupts).

RTC-8583

■Register descriptions

1. Control registers

Register name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CNT	STOP	HOLD	MODE1	MODE0	MASK	ALM	AF	TF

(1) TF bit (bit 0)

When the ALM bit is "0", this bit acts as a 50%-duty seconds flag. This bit is "0" when the hundredths of a second digits are between 00 and 49, and is "1" when the hundredths of a second digits are between 50 and 99. The INT pin operates in synchronization with this flag.

When the ALM bit is "1", this bit acts as a timer counter overflow flag. If this bit is "1", it indicates that an overflow occurred in the register 7 timer counter. To clear this flag, write a "0" to the bit.

ALM bit status	TF bit status	Function of TF bit
0	0	Indicates that the hundredths of a second digits are between 00 and 49.
	1	Indicates that the hundredths of a second digits are between 50 and 99.
1	0	No overflow has occurred in the register 7 timer counter.
	1	An overflow has occurred in the register 7 timer counter.

(2) AF bit (bit 1)

When the ALM bit is "0", this bit acts as a 50%-duty minutes flag. This bit is "0" when the seconds digits are between 00 and 29, and is "1" when the seconds digits are between 30 and 59.

When the ALM bit is "1", this bit acts as an alarm flag. If this bit is "1", it indicates that an alarm or a timer alarm interrupt has been generated.

ALM bit status	AF bit status	Function of AF bit
0	0	Indicates that the seconds digits are between 00 and 29.
	1	Indicates that the seconds digits are between 30 and 59.
1	0	No alarm or timer alarm interrupt has occurred.
	1	An alarm or timer alarm interrupt has occurred.

(3) ALM bit (bit 2)

This bit enables the alarm and timer functions.

ALM bit status	Function of ALM bit
0	The timer counter, alarm, and timer alarm functions are disabled. As a result, the area from register 8 to register 15 can be used as general-purpose RAM.
1	The timer, alarm, and timer alarm functions are enabled.

(4) MASK bit (bit 3)

Because normally the year data and day of the month data are combined together in register 5 and the day of the week data and month data are combined together in register 6, the data must be separated after the contents of each register are read. This bit masks the year and day of the week data so that the month and day of the month data can be read directly from the registers. This mask function is effective only for reads. Because the mask function has no effect when writing, it is necessary to write the combined data when writing data to these registers.

MASK bit status	MASK bit function
0	The year data and day of the month data are read together from register 5 and the day of the week data and month data are read together in register 6.
1	The year data in register 5 and the day of the week data in register 6 are masked with zeroes, so only the day of the month data and month data are read from their respective registers.

(5) MODE1,MODE0 (bit 5, bit 4)

These bits determine the basic operating mode of the RTC-8583.

MODE1	MODE0	Function of MODE bits
0	0	Operates as a real-time clock that uses the 32kHz signal from the internal crystal as the clock source.
0	1	Operates as a real-time clock that uses an external 50Hz signal as the clock source.
1	0	Operates as an event counter that counts an externally input signal.
1	1	Test mode. Operation is not guaranteed in this mode.

The internal crystal oscillator is disabled in 50Hz clock mode and event counter mode.

(6) HOLD bit (bit 6)

The HOLD bit holds count data when it is set to 1 from 0. After this bit is set, read out data is the held data at all time. When this bit is released to 0, the hold operation is released. The internal counter continue to works while the data is held. Therefore, data has no delay and no unexpected defeat count.

Using this function, can avoid unusual data by occurred carry (calendar update) when reading many data at the same time. Note that the flag bits are not held. Writing to the registers while data are held is possible, but the written data is not effective for reading. This means, the written data is hiding under the held data.

HOLD bit	Function of HOLD bit
0	Count data is not held. Read out data is current data
1	Count data is held at the time when this bit is set to 1 from 0.

(7) STOP bit (bit 7)

The STOP bit stops count operation and resets internal counter below second digits.

When STOP bit is 1, the count-up operation is stopped and internal counter below second digit is reset.

When STOP bit is 0, the count-up operation is restarted and internal counter reset is released.

This function can be used when executing time correction in order to avoid writing unmatched data by counter update and exact time correction below 1 second.

Operation mode	STOP bit	Function of STOP bit
Real time clock mode (32kHz, 50Hz)	0	Normal operation
	1	Stops the all counter operation and resets internal counter below 1 second digit.
Event counter mode	0	Normal operation
	1	Stops count operation

2. 1/100 seconds register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1/100	32kHz	1/100 seconds data. Data representation is BCD between 0 to 99.							
	50Hz	2/100 seconds data. Data representation is BCD between 0 to 98. bit 0 is always 0 and writing to this bit has no effect.							
	EVENT	Event counter data between 0 to 99. Data representation is BCD between 0 to 99							

3. Second register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SEC	32kHz	Second data. Data representation is BCD between 0 to 59.							
	50Hz	Second data. Data representation is BCD between 0 to 59.							
	EVENT	Upper 8 bit of event counter data between 0 to 9900. Data representation is BCD between 0 to 99.							

4. Minute register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MIN	32kHz	Minute data. Data representation is BCD between 0 to 59.							
	50Hz	Minute data. Data representation is BCD between 0 to 59.							
	EVENT	Upper 8 bit of event counter data between 0 to 990000. Data representation is BCD between 0 to 99							

5. Hour register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HOUR	32kHz	12/24	AM/PM	Hour data. Data representation is BCD between 1 to 12 or 0 to 23 which is determined by 12/24 bit					
	50Hz	12/24	AM/PM	Hour data. Data representation is BCD between 1 to 12 or 0 to 23 which is determined by 12/24 bit					
	EVENT	Free							

(1) AM/PM bit (bit6)

AM/PM	Status of 12/24 bit	Significance of AM/PM bit
0	1	This indicates in AM. The data range of hour digit is 12, 1, 2, ... 10, 11.
1	1	This indicates in PM. The data range of hour digit is 12, 1, 2, ... 10, 11.
0	0	Clock mode is 24 hour mode. AM/PM bit shows always 0.

(2) 12/24 bit (bit7)

12/24 bit	Function of 12/24 bit
1	12-hour clock is selected.
0	24-hour clock is selected.

6. Year and day register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DAY	32kHz	Year data between 0 to 3		Day data. Data representation is BCD between 1 to 31 max.					
	50Hz	Year data between 0 to 3		Day data. Data representation is BCD between 1 to 31 max.					
	EVENT	free							

When year value is 0, the year is leap year. In the leap year, the day 29 is added in February.
The year data will be masked when MASK bit is 1.

7. Day of the week and month register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MONTH	32kHz	Day of the week data between 0 to 6			Month data. Data representation is BCD between 1 to 12.				
	50Hz	Day of the week data between 0 to 6			Month data. Data representation is BCD between 1 to 12.				
	EVENT	free							

The day of the week data will be masked when MASK bit is 1.

8. Timer-counter register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TIMER	32kHz	Timer counter data. Data representation is BCD between 0 to 99.							
	50Hz								
	EVENT								

This is a BCD up-counter. When an overflow has occurred, the TF bit in register 0 is set to 1. In order to use timer counter, setting 1 to the ALM in register 0 is necessary. When the ALM bit is reset to 0 while the timer is working, this register holds the count data at the time. Please refer to the alarm register section in next for the setting of period of timer counter and the overflow interrupt output.

9. Alarm control register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ALARM	32kHz 50Hz EVENT	AIE	TAIE	AS1	AS0	TIE	TCP2	TCP1	TCP0

(1) TCP2,TCP1,TCP0 bits (bit2,1,0)

The TCP2, TCP1 and TCP0 bits sets a period of count-up for timer counter.

TCP2	TCP1	TCP0	Period of clock mode	Period of event counter mode
0	0	0	Stop	Stop
0	0	1	1/100 seconds	1 event
0	1	0	1 second	100 events
0	1	1	1 minute	10000 events
1	0	0	1 hour	1000000 events
1	0	1	1 day	Do not use.
1	1	0	Do not use.	Do not use.
1	1	1	Test mode. Do not select.	Test mode. Do not select.

Note: The count-up synchronizes with carry from clock register or event count register. Therefore, when the period is selected to every minute, the count-up may be faster than 1 minute if second register is not 0.

(2) TIE bit (bit3)

Set the TIE bit to select an interrupt output from INT terminal when an overflow has occurred from timer counter.

TIE bit	Interrupt output
0	None (TF bit works)
1	Yes

(3) AS1,AS0 bits (bit5,4)

Set the AS1 and AS0 bits to select a range of alarm comparison.

AS1	AS0	Clock mode	Event counter mode
0	0	No alarm	No alarm
0	1	Issues alarm everyday. It issues an alarm at preset time. Year, month, day and day of the week is ignored.	Alarm is issued when the event counters 1, 2 and 3 are consistent with comparison alarm registers 9, A and B.
1	0	Issues alarm once per a week. In this mode, the day of the week and month register (address E) changes to an exclusive alarm register for day of the week as follows: bit 7 6 5 4 3 2 1 0 Day of the week Ignored 6 5 4 3 2 1 0 By presetting 1 to expected day of the week bit, an alarm is issued on the preset day of the week at preset time. It is possible to select multiple presets in a week.	Do not use
1	1	An alarm is issued once per year on preset month and day at preset time. Year and day of the week is ignored.	Do not use

The AF bit in register 0 is 1 when an alarm is issued.

(4) TAIE bit (bit6)

Set the TAIE bit to select timer alarm operation.

TAIE bit	Function of TAIE bit
0	Timer alarm is disabled
1	Timer alarm is enabled. It is issued when timer counter register (7) agrees with timer alarm register (F).

The AF bit in register 0 is 1 when a timer alarm is issued.

(5) AIE bit (bit7)

Set the AIE bit to select an interrupt output from INT terminal when an alarm or timer alarm has issued.

AIE	Interrupt output
0	Disabled (AF bit works)
1	Enabled

RTC-8583

10. 1/100 seconds alarm register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
a-1/100	32kHz	1/100 seconds alarm data. Data representation is BCD between 0 to 99.							
	50Hz	2/100 seconds alarm data. Data representation is BCD between 0 to 98.							
	EVENT	Event count alarm data of 0 thru 99. Data representation is BCD between 0 to 99.							

11. Second alarm register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
a-SEC	32kHz	Second alarm data. Data representation is BCD between 0 to 59.							
	50Hz								
	EVENT	Upper 8 bits event count data of 0 thru 9900. Data representation is BCD between 0 to 99.							

12. Minute alarm register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
a-MIN	32kHz	Minute alarm data. Data representation is BCD between 0 to 59.							
	50Hz								
	EVENT	Upper 8 bits event count data of 0 thru 990000. Data representation is BCD between 0 to 99.							

13. Hour alarm register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
a-HR	32kHz	12/24-alarm	AM/PM-alarm	Hour alarm data. Data representation is BCD between 1 to 12 or 0 to 23 depending on clock mode.					
	50Hz								
	EVENT	free							

Both 12/24 bit and AM/PM bit are compared.

14. Day alarm register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
a-DAY	32kHz			Day alarm data. Data representation is BCD between 1 to 31 max.					
	50Hz								
	EVENT	free							

15. Month and day of the week alarm register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
a-MON	32kHz				Month data. Data representation is BCD between 1 to 12.				
	50Hz								
	EVENT	free							

When using an alarm in every week. This register structure changes. See section of alarm control register.

16. Timer alarm register

Register name	Mode	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TIMER	32kHz	Timer alarm data. Data representation is BCD between 0 to 99.							
	50Hz								
	EVENT								

17. User RAM

The 8 bit width user RAM is available in the address between 10h thru FFh.

■Access procedure

1. Characteristic of the I²C BUS

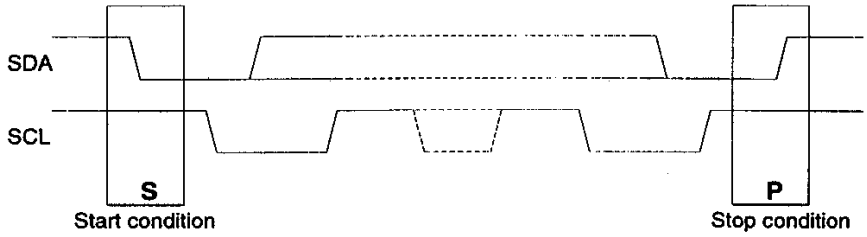
I²C-BUS is a bi-directional interface that uses two (2) lines. This interface has two signal lines that are SDA (data line) and SCL (clock line). Both these lines are connected to plus (+) power source with the pull-up registers. All input and output ports must be open drain on the I²C-BUS, that in order to connect the devices by AND-connection on this bus.

2. Bit transfer

The bit data transfer is executed for one bit on each one clock pulse of SCL line. When the device transmits the data, the data change should be executed during SCL line is at low level. When the device receives the data, the data should be taken in during SCL is at high level.

3. Start condition and stop condition

When I²C-BUS is not interfacing, the two control line keeps high level. When SDA changed to low level from high level, this is defined as a start condition. After that, actual data transfer is executed. When SCL is high level and, SDA changed to high level from low level, this is defined as a stop condition.



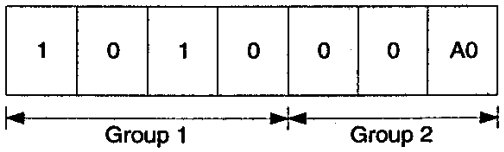
4. Slave address

The I²C-BUS devices do not have any chip select or chip enable pins. All I²C-BUS devices are memorized with a fixed unique number in it. The chip selection on the I²C-BUS is executed, when the interface starts, the master device send the required slave address to all devices on the I²C-BUS. The receiving device only reacts for interfacing, when the required slave address is agreed with its own slave address.

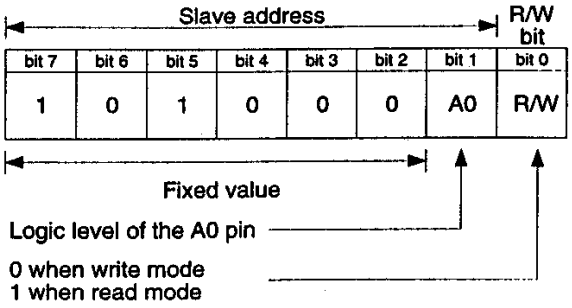
The slave address is 7 bits data that is made of 4 bits fixed data (group 1), and 3 bits data (group 2). As in the RTC-8583, the data in group 1 is (1010), group 2 is (00X). The data X in group 2 is given by A0 pin input logic level. The upper 2 bits of group 2 is fixed as (00).

In case, two RTC-8583s are installed on a system, it is possible to select each device using A0 terminal logic level. Note that if more RTC-8583s are installed, it is possible to access each device by using dynamic control to the A0 pins.

RTC-8583 slave address

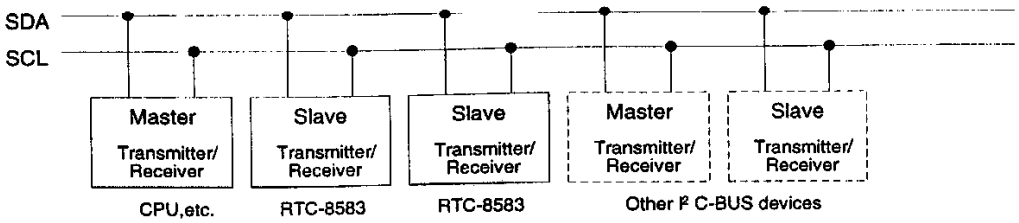


During in actual data transmission, the transmitted data contains the slave address and the data with R/W (read/write) bit.



5. System structure

The *MASTER* is defined the device that controls interfacing of messages, the *SLAVE* is defined the device that is controlling its interfacing.
Note the *TRANSMITTER* is defined to be the one transmitting messages, the *RECEIVER* is defined to be the one receiving messages. Each device can be transmitter and receiver.



6. Acknowledge

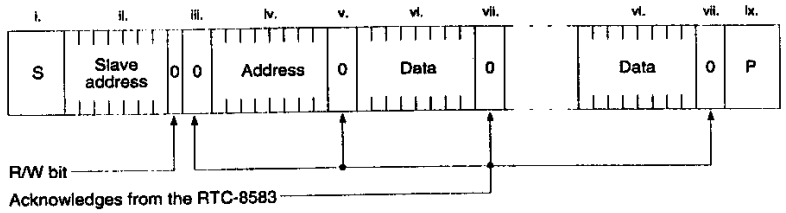
There is no limit to the size of data, between the start and stop condition. During interfacing, the receiver issues an acknowledge bit to the transmitter to confirm it received data. The acknowledge bit is low active logic. So, the transmitter sets high level for the SDA line and issues a clock pulse for the acknowledge bit. If the receiver got 8-bits data from the transmitter, the receiver will set low level for the SDA line when the clock for the last bit is done. Then the SDA line of transmitter becomes low level because the I²C-BUS lines are pulled-up. At this time, a transmitter confirms an acknowledge, then continue to issue next data. A receiver prepares to receive next data with releasing SDA line to high level when a clock for acknowledge bit is done.
When a master device is transmitter, if a master device sets stop condition after confirm an acknowledge without issuing next data communication, the interface is normally completed.
When a master device is receiver, if it issued high level for acknowledge bit then, after that it sets stop condition, the interface is normally completed.

7. I²C-BUS protocol

(1) Write procedure with specifying the address

The RTC-8583 has an increment function of the address. When the address is set the first time, then it is possible to write after this address, by only sending data. The RTC sets the data into auto incremented addresses.
The basic writing procedure is the following:

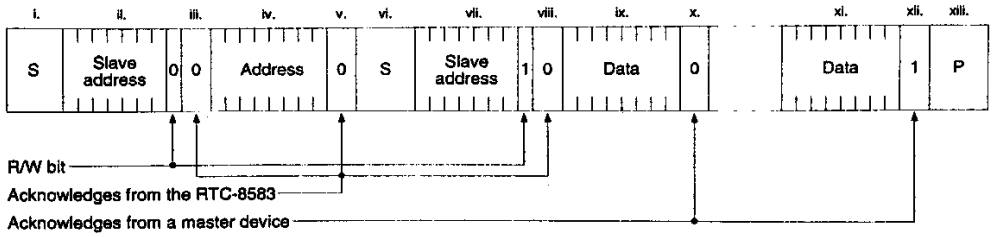
i. A master device sends a start condition.
ii. A master device sends a data of slave address and R/W bit with write mode to the RTC-8583.
iii. A master device confirms an acknowledge from the RTC-8583.
iv. A master device sends an address data for writing to the RTC-8583.
v. A master device confirms an acknowledge from the RTC-8583.
vi. A master device sends a write data that the address is set on (iv.) in the following chart.
vii. A master device confirms an acknowledge from the RTC-8583.
viii. Repeats vi. and vii. as the need arises. Write address is automatically incremented in the RTC-8583.
ix. A master device sends a stop condition.



(2) Read procedure with specifying the address

To read the data from the RTC-8583, set the read mode after writing read address to the RTC then read actual data.
The basic reading procedure is the following:

i. A master device sends a start condition.
ii. A master device sends a data of slave address and R/W bit with write mode to the RTC-8583.
iii. A master device confirms an acknowledge from the RTC-8583.
iv. A master device sends an address data for writing to the RTC-8583.
v. A master device confirms an acknowledge from the RTC-8583.
vi. A master device sends a start condition. At this time, a master device does not send a stop condition before this start condition.
vii. A master device sends a data of slave address and R/W bit with read mode to the RTC-8583.
viii. A master device confirms an acknowledge from the RTC-8583.
From now on, the RTC-8583 becomes a transmitter, and a master device becomes receiver.
ix. The RTC-8583 outputs a data that address is selected on (iv.) in the following chart.
x. A master device sends an acknowledge to the RTC-8583.
xi. Repeats ix. and x. as the need arises. Read address is automatically incremented in the RTC-8583.
xii. A master device sends an acknowledge that value is 1.
xiii. A master device sends a stop condition.

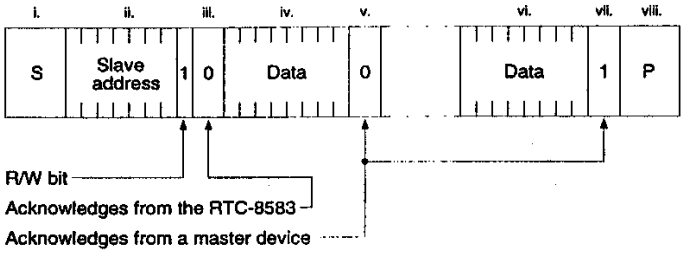


(3) Read procedure without specifying the address

The data of the next address and later addresses of the previous accessed can be immediately read after the read mode has been set at first.

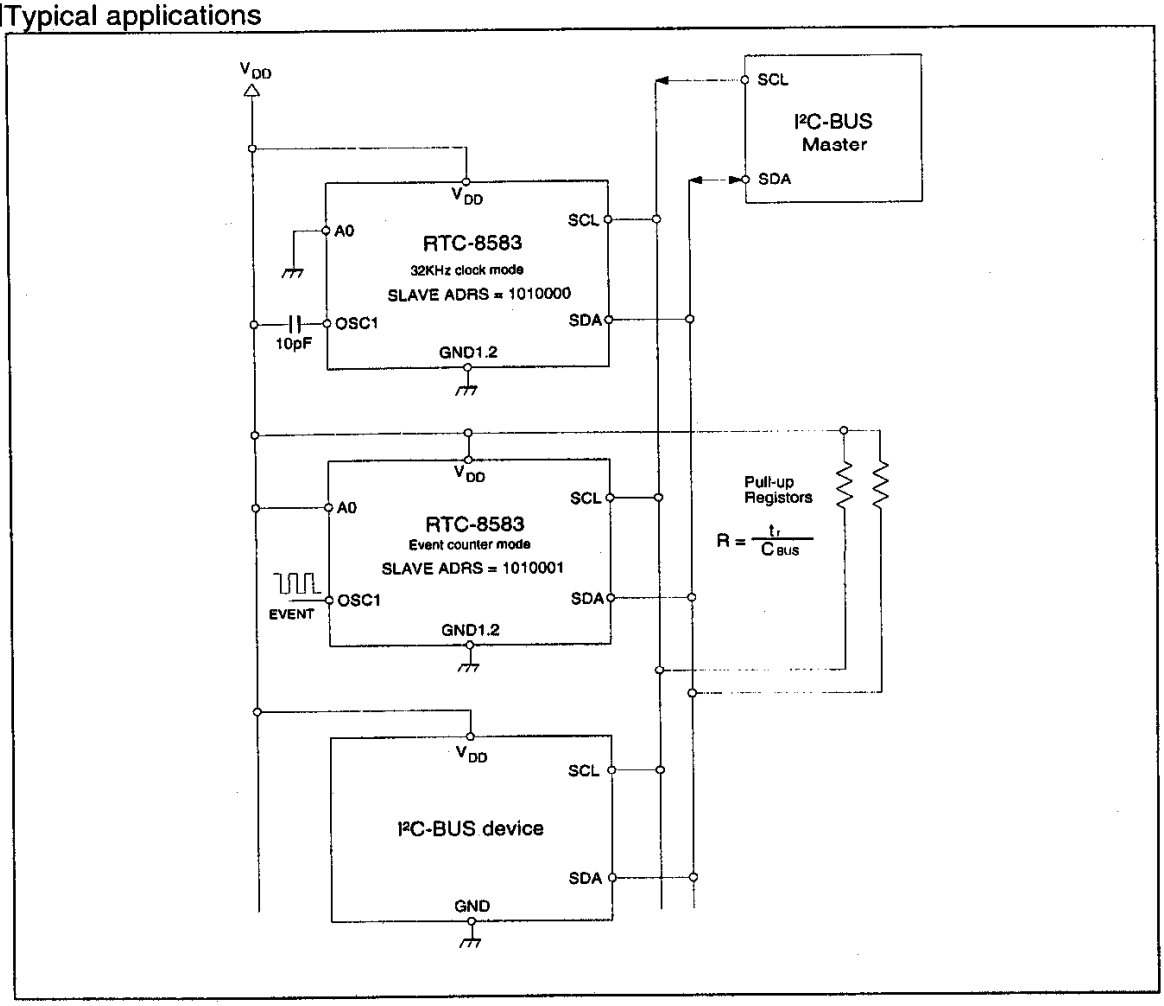
The basic reading procedure is the following:

i. A master device sends a start condition.
ii. A master device sends a data of slave address and R/W bit with read mode to the RTC-8583.
iii. A master device confirms an acknowledge from the RTC-8583.
From now on, the RTC-8583 becomes a transmitter, and a master device becomes receiver.
iv. The RTC-8583 sends a data of address 0.
v. A master device sends an acknowledge to the RTC-8583.
vi. Repeats iv. and v. as the need arises. Read address is automatically incremented in the RTC-8583.
vii. A master device sends an acknowledge that value is 1.
viii. A master device sends a stop condition.



RTC-8583

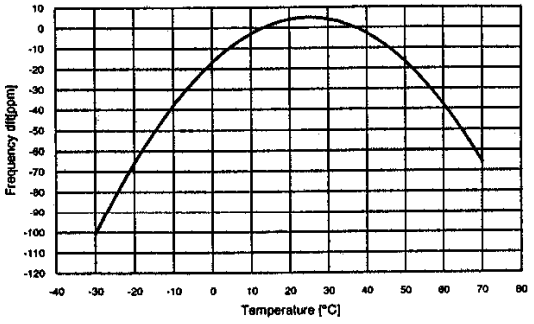
Typical applications



Reference data

1. Frequency temperature characteristics

θT = 25°C TYP.
α = -0.035ppm/°C² TYP.



Finding the frequency stability (clock error)

1.The frequency temperature characteristics can be approximated by using the following expression:

$\Delta f_T(ppm)=\alpha(\theta_T-\theta_X)^2$

Δf_T(ppm)	: Frequency deviation at target temperature
α(ppm/℃²)	: Secondary temperature coefficient (-0.035±0.005ppm/℃²)
θ_T(℃)	: Peak temperature (25℃±5℃)
θ_X(℃)	: Target temperature

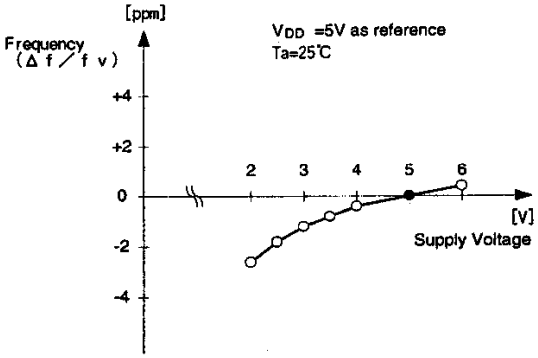
2.To determine the overall clock accuracy, add the frequency tolerance and the voltage characteristics:

$\Delta f/f(ppm) = \Delta f/f_0 + \Delta f_T + \Delta f_V$

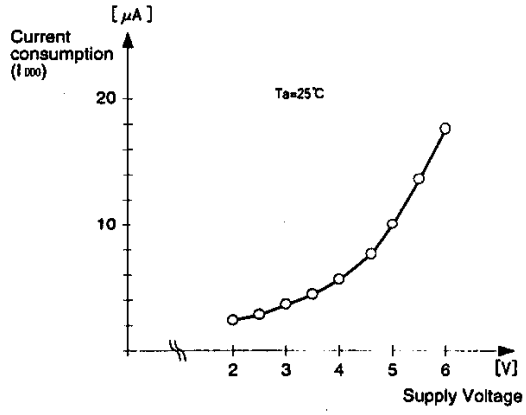
$\Delta f/f$ (ppm)	: Clock accuracy at a given temperature and voltage
$\Delta f/f_0$(ppm)	: Frequency tolerance
Δf_T (ppm)	: Temperature dependent frequency deviation
Δf_V (ppm)	: Voltage dependent frequency deviation

3.Finding the daily deviation:
Daily deviation (seconds) = $\Delta f/f \times 10^{-6} \times 86400$
The clock error is one second per day at 11.574 ppm.

2. Example of the frequency/voltage characteristics (typical)



3. Examlpe of the current consumption/voltage characteristics (typical)

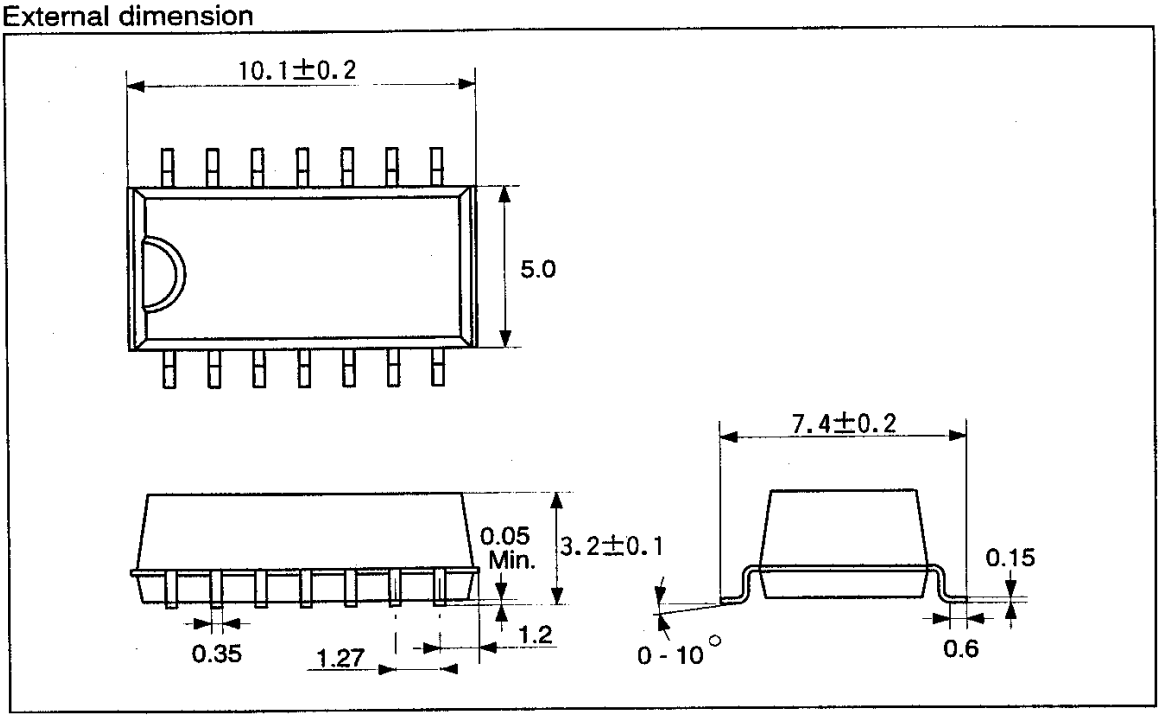


4. Note

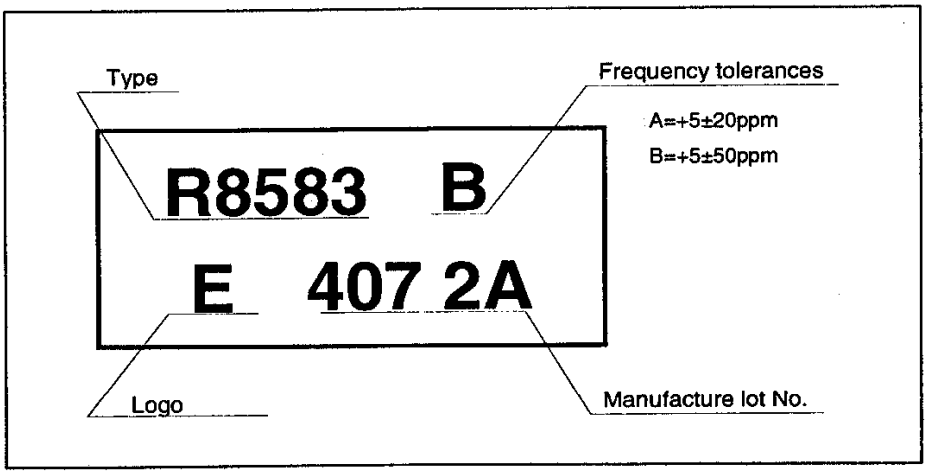
The data shows the standard values for sample lot.
For the rated values,see the specifications.(Please refer to of page 3)

RTC-8583

■External dimension



■Marking layout



Note: The indication above details the markings and outline their positions.But it does not specify of the type faces, sizes of characters and their positions.

■Application notes

1. Notes on handling

In order to enable the RTC-8583 module to operate at low power levels, C-MOS circuitry was used in the design of the chip. To prevent damage to this RTC, note the following points:

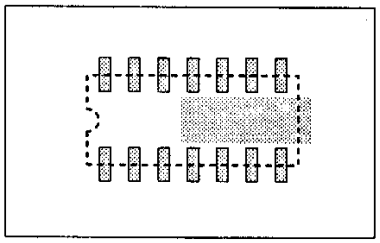
(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltages should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of 0.01 µF to 0.1 µF as close as possible to the power supply pins (V_{DD} and GNDs). Also avoid placing any device that generates high levels of electronic noise near the RTC-8583 module.

Do not connect signal lines to under the package of RTC-8583 module, and, if possible, embed this area in a GND land.



(3) Voltage levels of input pins

Apply signal levels that are as close as possible to V_{DD}, GND1 and GND2 to all pins. Mid-level potentials will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device.

(4) Unused signal pins

Since the input impedance of the signal pins is extremely high, operating the device with these pins open circuit can lead to malfunctions due to noise. Pull-up or pull-down resistors should be provided for all unused signal pins.

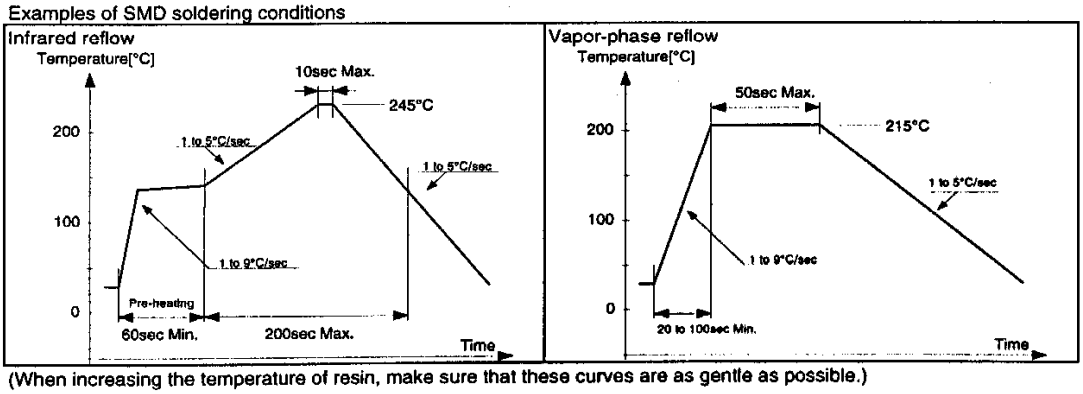
2. Notes on packaging

(1) Soldering temperature conditions

If the temperature within the package exceeds 260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. Therefore, always check the mounting temperature before mounting this device. Reconfirm if the mounting conditions are later changed.

Soldering conditions: No higher than 260 °C for no more than twice at 10 seconds, or no higher than 230 °C for no more than 3 minutes

Examples of SMD soldering conditions



(When increasing the temperature of resin, make sure that these curves are as gentle as possible.)

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, you should confirm that the module will survive the mounting process that will be used before actually using this module in full-scale production. In addition, if the mounting conditions are later changed, the survivability of the module should be reconfirmed under the new conditions.

(3) Ultrasonic cleaning

There is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

EPSON

Application Manual

RTC-8583

Distributer

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