Three-PLL Programmable Clock Generator

MG-5100SA

Preliminary

- High density mounting type SMD, SOP-14pin package
- Cylindrical AT crystal unit built-in, thus assuring high reliability
- Three-PLL circuits allowed being programmable for output frequency.
- Available to choose output in 8 frequencies by selects pin for CPUCLK.

■ Specifications

1. Absolute maximum rating

Item	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	VDD	VDD - GND	-0.5	7.0	V
Storage Temperature	Tstg		- 55	100	°C
Soldering Condition	Tsol	Twice at under 260°C within 10sec			

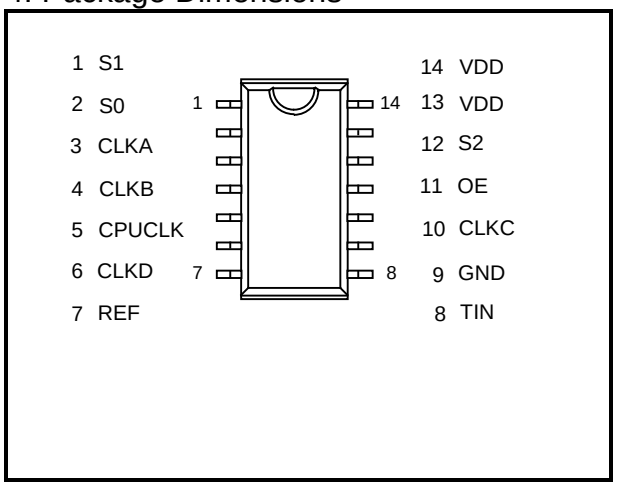
2. Operating range

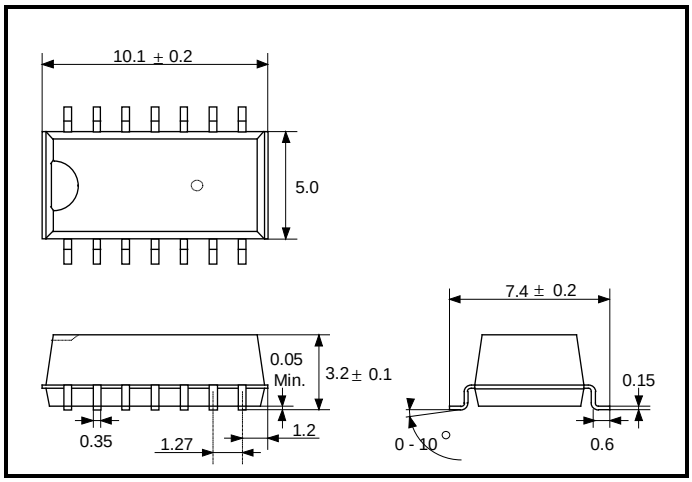
Item	Symbol	Conditions	Min.	Max.	Unit
Operating Voltage	VDD		3.0(4.5)	3.6(5.5)	V
Operating Temperature	Topr		- 20	70	°C

3. Electric Characteristics (If no specified: VDD=3.3V,Ta=-20~+70°C)

Item	Symbol	Conditions	Min.	Max.	Unit
Output Frequency	f0	Vdd = 3.3V ± 0.3V	76.9k	80M	Hz
		Vdd = 5.0V ± 0.5V	76.9k	100M	Hz
Frequency Stability	Δf / f0		-100	+100	ppm
Current consumption	IDD	No Load		65(100)	mA
Load		CMOS		15	pF
Output Voltage □H□	VOH	IOH = -4.0mA	2.4		V
Output Voltage □L□	VOL	IOL = +4.0mA		0.4	V
Input Current □H□	IIH	VIN = VDD - 0.5 V	-10		uA
Input Current □L□	IIL	VIN = +0.5 V		10	uA
Output rise time	tr	20 ~ 80%VDD		5.0	nsec
Output fall time	tf	80 ~ 20%VDD		4.0	nsec
Duty	tw / t	50% VDD level	40	60	%
Skew				0.5	nsec
Oscillation start up time	tSTA			50	msec
Jitter (Peak to Peak)	tj			500	psec

4. Package Dimensions





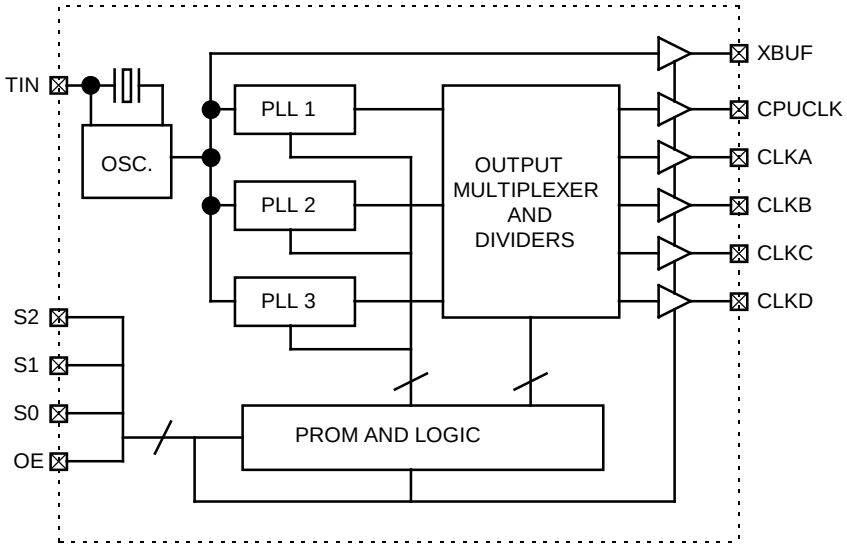
5. Pin Assignment

Symbol	Pin No.	I / O	Function
VDD	13,14	-	Power Supply (3.3V or 5.0V)
GND	9	-	GND
TIN	8	-	Do not connect anything
OE	11	Input	Output Control (□H□ : Enable, □L□ : Disable/High-Z)
CLKA	3	Output	Clock Output ports
CLKB	4	Output	
CLKC	10	Output	
CLKD	6	Output	
CPUCLK	5	Output	
REF	7	Output	Reference clock output (STD : 14.31818MHz or 17.7344MHz)
S0	2	Input	Select pin-0 for Output frequency of CPUCLK
S1	1	Input	Select pin-1 for Output frequency of CPUCLK
S2	12	Input	Select pin-2 for Output frequency of CPUCLK

6. Availability to specify the Vdd & Output Frequency

1) Power supply voltage
   VDD = 3.3V or 5.0V
2) Output Frequency range for CLKA ~ CLKD &CPUCLK
   76.9kHz ~ 80MHz at Vdd = 3.3V
   76.9kHz ~ 100MHz at Vdd = 5.0V
   There are some unable frequencies to make output for the requested frequency.
3) Output Frequency range for CPUCLK
   2.0MHz ~ 80MHz at Vdd = 3.3V
   2.0MHz ~ 100MHz at Vdd = 5.0V
   There are some unable frequencies to make output for the requested frequency.
4) Reference frequency (Crystal Oscillation frequency)
   The standard frequency (recommended frequency) is 14.31818MHz or 17.7344MHz.
   Please consult us for the other frequency if you need.
5) CPUCLK Output
   Available to change the output frequency in 8 frequencies by S0/S1/S2 pins.
6) CLKA ~ CLKD
   Available to set an output frequency individually in the above range.

7. Block Diagram



8. Output configuration

1) Clock Source

(1) Ref. Clock (Crystal Oscillation frequency)

(2) PLL1 (Programmed frequencies ----- 8 frequencies : selected by S0 to S2)

(3) PLL2 (Programmed frequency)

(4) PLL3 (Programmed frequency)

2) Output frequency

1) XBUF : Ref. Clock or OFF

2) CPUCLK : Pre-choose one frequency from PLL1, PLL1/2, PLL1/4 and OFF

3) CLKA, CLKB, CLKC, CLKD : To be set to one of the following 32 selections

Ref	Ref/2	Ref/4	Ref/8*
(PLL1)	(PLL1)/2	(PLL1)/4	(PLL1)/8
(PLL2)	(PLL2)/2	(PLL2)/4	(PLL2)/8
(PLL3)	(PLL3)/2	(PLL3)/4	(PLL3)/8
(PLL3)/3	(PLL3)/6	(PLL3)/12	OFF
(PLL3)/5	(PLL3)/10	(PLL3)/20	(PLL3)/40
(PLL3)/12	(PLL3)/24	(PLL3)/48	(PLL3)/96
(PLL3)/13	(PLL3)/26	(PLL3)/52	(PLL3)/104

Note 1. This palette of choices is generated by the output multiplexers and dividers. Internal signals that originated from the PLLs and the reference crystal oscillator are further divided, resulting in 32 output possibilities as show. ((PLL3)/12 option occurs twice.)