EG-2001CA

Ultra Low Jitter, High Frequency Clock Oscillator

■ Features

- Generates high frequency clock using quartz SAW Technology
- Ultra low jitter / phase noise
- High oscillation stability through fundamental mode resonation
- Small industry standard 7x 5 x 1.2mm ceramic package
- Meets IEEE 802.3z Gigabit Ethernet specification

■ Applications

- Gigabit Ethernet
- High speed CPU and System BUS
- Digital Synthesis Refclk
- Instrumentation

■ Absolute Maximum Ratings

Item	Symbol	Unit	MIN.	TYP.	MAX.	Condition
Supply Voltage	V_{DD}	V	-0.5		+5.5	V_{DD}-GND
Storage temperature	Tstg	°C	-55		+100	Stored as bare product after unpacking
Solder heat resistance of the outer lead	Tsol	Max. 260°C x Max. 10s x 2 times				

■ Operating range

Item	Symbol	Unit	MIN.	TYP.	MAX.	Condition
Supply voltage	V_{DD}	V	3.0	3.3	3.6	
Operating temperature	Topr	°C	0		+70	
Output load	CL	pF		15 15	25 15	f=125.0000 to 135.0000MHz f=135.0001 to 166.0000MHz

■ Frequency characteristics

(V_{DD}=3.0 to 3.6,GND=0.0V,Load CL=25pF)

Item	Symbol	Unit	MIN.	TYP.	MAX.	Condition
Oscillation Range	fosc	MHz	125		166	
Frequency Stability	df/f0	ppm	-100		+100	*1 Ta= 0 to +70°C

*1 This includes initial frequency tolerance, temperature, supply voltage variation, loading variation and 10yrs aging.

■ Electrical characteristics

(V_{DD}=3.0 to 3.6,GND=0.0V,Load CL=25pF)

Item	Symbol	Unit	MIN.	TYP.	MAX.	Condition
Start up time	tosc	ms		2	10	t=0 at V_{DD}=3.0V
Current consumption	I_{OP}	mA		27	50	No load, f=125MHz
Rise time	t_{TLH}	ns			2.0	0.8 to 2.0V
Fall time	t_{THL}	ns			2.0	2.0 to 0.8V
Duty	tw/t	%	45		55	at 1.4V
High level output voltage	V_{OH}	V	V_{DD}-0.4			I_{OH}=-8mA
Low level output voltage	V_{OL}	V			0.4	I_{OL}=8mA
High level input voltage	V_{IH}	V	0.7V_{DD}			Tri-state Terminal
Low level input voltage	V_{IL}	V			0.3V_{DD}	Tri-state Terminal
Accumulative Jitter	tjacc	ps		3	6	rms
Absolute Jitter	tjab	ps		30	40	Peak to peak
SSB phase noise		dBc/Hz		-105		@1KHz offset
		dBc/Hz		-115		@10KHz offset
		dBc/Hz		-120		@100KHz offset

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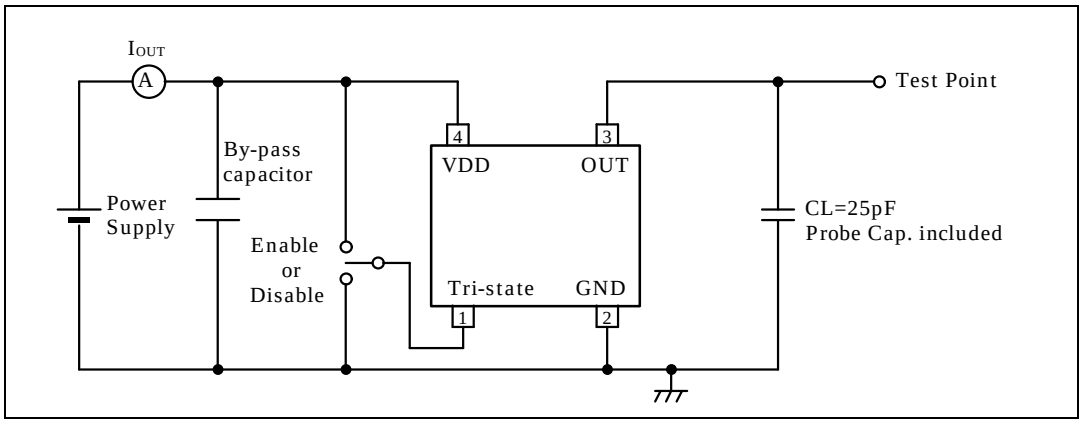
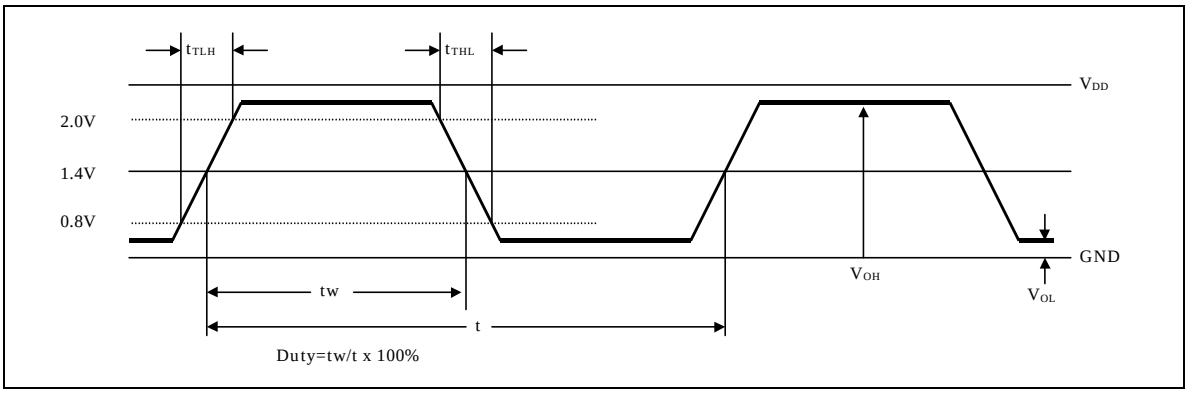
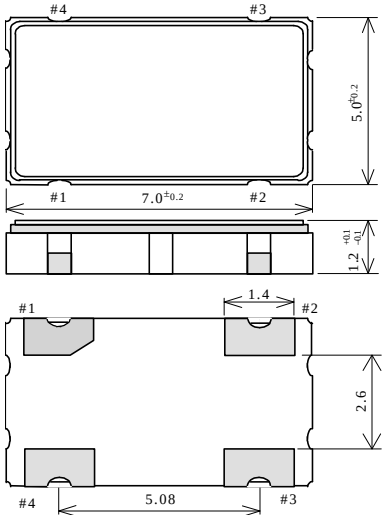
■ Test circuit

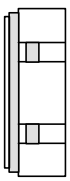


■ Timing chart



■ Package





Pin No.	Pin Name
1	Tri-state
2	GND
3	OUT
4	Vdd