
DEVELOPMENT SPECIFICATIONS

TYPE : VG-2620CA FBX

SPEC. No. : VG-2620CAFBX-001

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SPECIFICATIONS

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Amendment and abolishment

Amendment and/or abolishment of this specification are subject to the agreement of both parties.

[1] Absolute maximum ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD-GND}	-0.3 to +7.0	V	
Storage temperature	T_{STG}	-55 to +125	deg.C	
Input voltage	V_{IN}	-0.3 to $V_{DD}+0.3$	V	Vc Terminal
Solder heat resistance of the outer lead	T_{SOL}	Max.240deg.C X Max.10 sec. X Max.2 times		

[2] Operating range

Parameter	Symbol	Value			Unit	Note
		Min..	Typ..	Max..		
Power voltage	V_{DD}	2.56	2.7	2.84	V	$V_{DD}=2.7V\pm 5\%$
Power voltage	GND	0.0		0.0	V	
Operable temperature	T_{OPR}	-40		+85	deg.C	$V_{DD}=2.7V\pm 5\%$
Operating temperature	T_{OPT}	-20		+75	deg.C	$V_{DD}=2.7V\pm 5\%$
Input voltage	V_{IN}	GND		V_{DD}	V	Vc Terminal
Output load	RL		2.2		k Ω	
	CL		12		pF	
	DC-cut capacitor	C_c	0.01		μ F	

DC-cut capacitor is not included in our VCXO. Please insert DC-cut capacitor in output line.

[3] Frequency characteristics

1) Output frequency 13.000000MHz

2) Frequency characteristics ($V_{DD}=2.7V$, $V_C=1.15V$, $GND=0.0V$, Load 2.2k Ω //12pF(DC cut))

Parameter	Symbol	Value	Unit	Note
Frequency tolerance *1	dF/Fo	+/- 13.0	ppm	Ta = -20 to 75deg.C
Frequency stability vs. Supply voltage	dF/Fv	+/- 1.0	ppm	$V_{DD}=2.7V\pm 5\%$
Frequency stability vs. Load change	dF/FI	+/- 1.0	ppm	Load :2.2k Ω //12pF +/- 5% Ta = 25deg.C
Frequency deviation after reflow cycles	dF/Fr	+/- 2.0	ppm	2 times. Ta = 25deg.C *2
Aging	dF_A	+/- 1.0	ppm	Ta = 25deg.C First Year
		+/- 2.5	ppm	Ta = 25deg.C After 8 Years

*1 Include initial frequency tolerance and temperature characteristics.

*2 The measurement of frequency deviation is made 24h after reflow soldering.

3) Frequency adjustment characteristics

(V_{DD}=2.7V, GND=0.0V, Ta=-20 to +75deg.C, Load 2.2kΩ//12pF(DC cut))

Parameter	Symbol	Value			Unit	Note
		Min..	Typ..	Max..		
Frequency pull range	dFc	+/- 20		+/- 31	ppm	Vc = 1.15+/-1.1 V
Frequency Control Sensitivity	dFc ^ dVc			34	ppm/V	Vc = 0.05 to 2.25 V dVc<0.15V
Frequency tuning linearity		-20		+20	%	Vc = 0.05 to 0.4V
		-20		+20		Vc = 0.4 to 2.25V
Input impedance(Vc terminal)	Zin	10			MΩ	Vc-GND(DC Level)

Frequency tuning linearity

(1) Vc=0.05 to 0.4V

$$\frac{dFc}{dVc} = \frac{f_{(Vc=0.4V)} - f_{(Vc=0.05V)}}{f_{(Vc=0.25V)} \times 10^6} \times 10^6 \quad \text{+/- 20\%}$$

$$\frac{dFc}{dVc} = \frac{f_{(Vc=0.4V)} - f_{(Vc=0.05V)}}{(Vc=0.4V) - (Vc=0.05V)} \quad \text{+/- 20\%}$$

(2) Vc=0.4 to 2.25V

$$\frac{dFc}{dVc} = \frac{f_{(Vc=2.25V)} - f_{(Vc=0.4V)}}{f_{(Vc=0.4V)} \times 10^6} \times 10^6 \quad \text{+/-20\%}$$

$$\frac{dFc}{dVc} = \frac{f_{(Vc=2.25V)} - f_{(Vc=0.4V)}}{(Vc=2.25V) - (Vc=0.4V)} \quad \text{+/-20\%}$$

[4] Electrical characteristics

(V_{DD}=2.7V+/-5%, GND=0.0V Vc=1.15V, Ta=-20 to +75deg.C, Load 2.2kΩ//12pF(DC cut))

Parameter	Symbol	Value			Unit	Note
		Min..	Typ..	Max..		
Start up time	t _{OSC}			4.5	ms	dF/F=2ppm t=0 at V _{DD} =2.56V
				6.5	ms	dF/F=0.05ppm t=0 at V _{DD} =2.56V
Current consumption	I _{OP}		0.8	1.0	mA	2.2kΩ//12pF+/-5%
Output level	V _{OUT}	0.8	1.15		V _{PP}	10kΩ//10pF+/-5%
		0.6	1.0		V _{PP}	2.2kΩ//12pF+/-5%
Duty	TW/T	30		70	%	GND LEVEL
Harmonics				-5	dBc	
SSB Phase noise				-115	dBc/Hz	offset:100Hz Ta=25deg.C
				-130		offset:1kHz Ta=25deg.C

[5] Electrostatic discharge sensitivity

Test method accords with MIL-STD-883C 3015.5 .

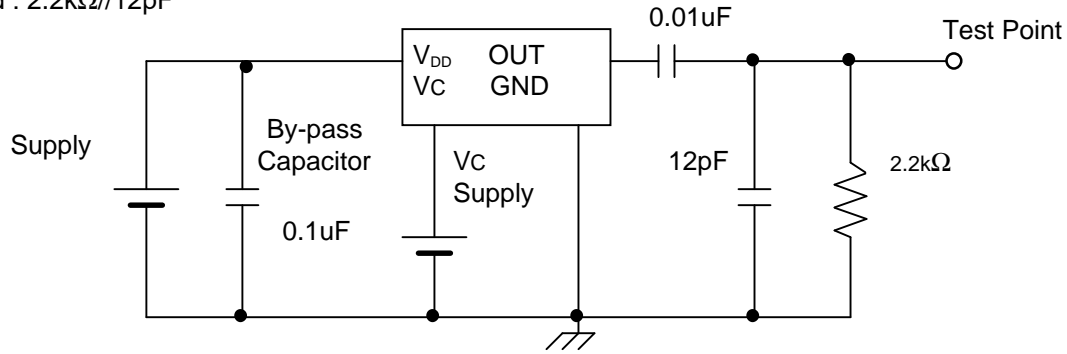
C = 100pF, R = 1.5kΩ

(Ta=25deg.C)

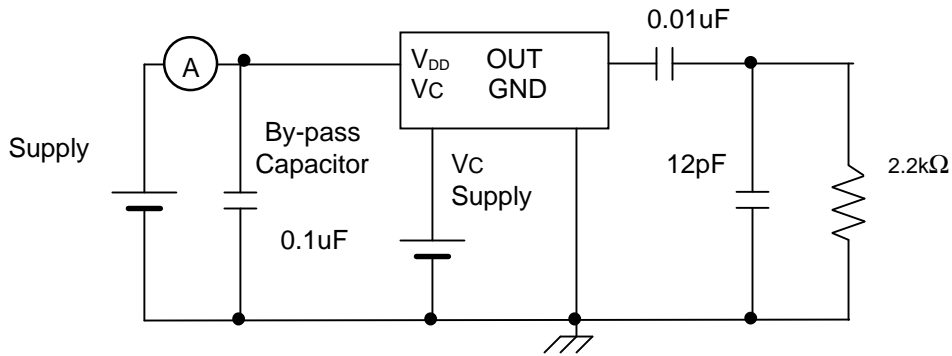
Item	Symbol	Value	Unit
Input pins	vs IN		
Output pins	vs OUT	Min. +/- 1200	V
Each supply pins	V _{DD} V _{SS}		

[6] Test circuit

1) Load : 2.2kΩ//12pF



2) Current consumption



3) Conditions

- | | |
|----------------------------|-------------|
| 1. Oscilloscope :Impedance | Min. 1MΩ |
| Input capacitance | Max. 12pF |
| Band width | Min. 300MHz |

Impossible to measure both frequency and wave form at the same time.(In case of using oscilloscope's amplifier output, possible to measure both at the same time.)

2. CL includes probe capacitance.
3. A capacitor (0.1uF) is placed between V_{DD} and GND, and closely to VCXO.
4. Use the current meter whose internal impedance value is small.
5. Power Supply
Impedance of power supply should be as lowest as possible.
6. GND should apply one point earth.

[7] Environmental and mechanical characteristics

No.	Item	Value *1		Test method [EIAJ ED-4701 be based on]	
		Freq. tolerance *,Q	Electrical characteristics		
1	High temp. storage	+/- 10ppm	Satisfy Item [4] and [3] 3)	+125deg.C X no bias X 1000h	
2	Low temp. storage	+/- 1ppm		-55deg.C X no bias X 1000h	
3	High temp. bias Low temp. bias	+/- 1.5ppm +/- 1ppm		+85deg.C X 2.84V X 1000h -40deg.C X 2.84V X 1000h	
4	Temp. humidity storage	+/- 2ppm		+85deg.C X 85%RH X 2.84V X 1000h	
5	Temp. cycle	+/- 2ppm		-55deg.C to +125deg.C ~ no bias (30 min x 100cycle/each)	
6	PCBT	+/- 10ppm		+121deg.C X 85%RH X 2.84V X 96h	
7	Solder heat resistance	+/- 1ppm		EIAJ ED-4701 SOLDER HEAT METHOD 1(2 times)	
8	Drop	+/- 1ppm		Free drop from 75cm height on a hard wooden board for 3 times.	
9	Vibration (variable frequency)	+/- 1ppm		10 to 500Hz 1.5mm p-p or 10G 10Hz .. 500Hz .. 10Hz 15min./cycle X 6h(2 h each plane)	
10	Solderability	Terminals solderable 90% of dipped portion.		Dip leads into solder bath at 230deg.C for 5 s (Using ROSIN FLUX)	
11	Solvent resistance	No defect for marking and outer appearance.		EIAJ ED-4701	

* Each test is independent.

*1 Measuring condition between before and after each test is same.

*2 Frequency tolerance is changed value between before and after each test, and the value of after test is measured after putting in room temperature for 2 to 24 hours.

Pre conditionings(Item No.1 to 6 are must)

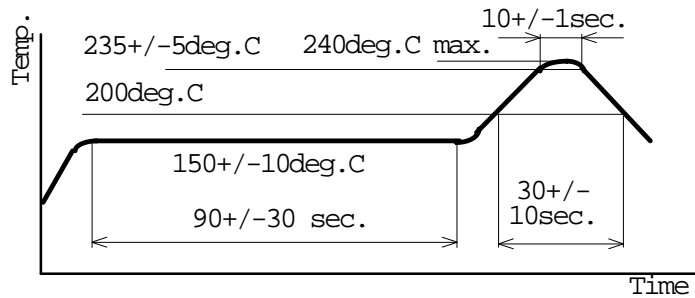
- +125deg.C X 24h to 85deg.C X 85% X 48h .. reflow 2(two) times.
- Initial value shall be after 24 h at room temperature.

Infrared-reflow (EIAJ-4701)

Pre heating temperature : 150+/-10 [deg.C] Pre heating time : 90+/-30 [s]

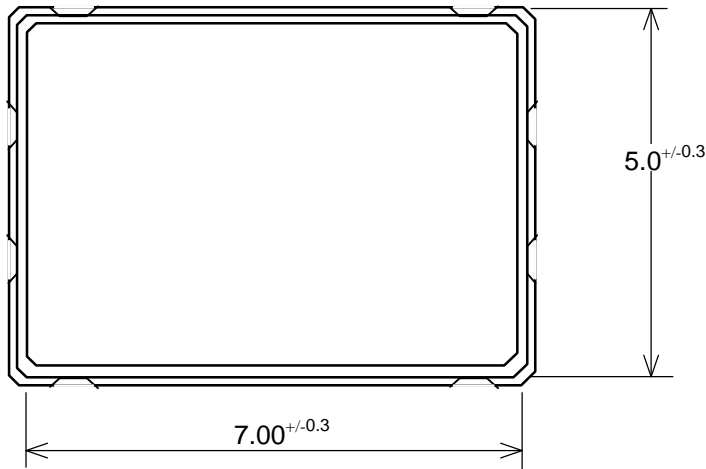
Heating temperature : 235+/- 5 [deg.C] heating time : 10+/-1 [s]

Peak temperature must not exceed 240deg.C and the duration of over 200deg.C should be 30+/-10seconds.

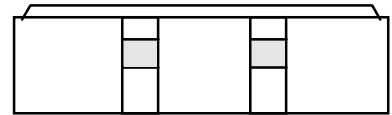
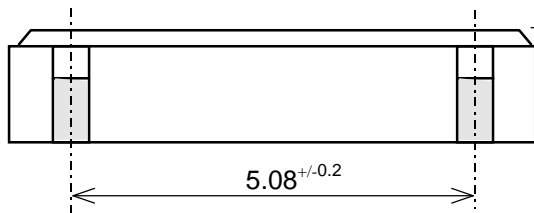


[8] Dimensions and Marking Layout

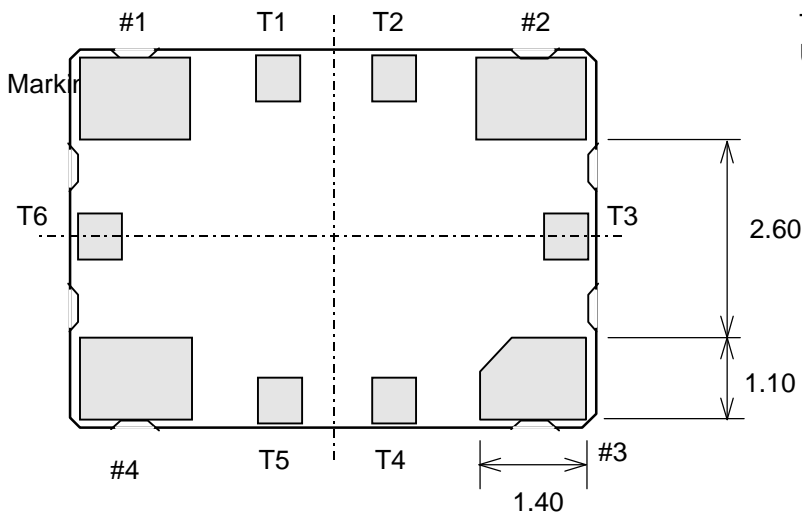
1) Dimensions



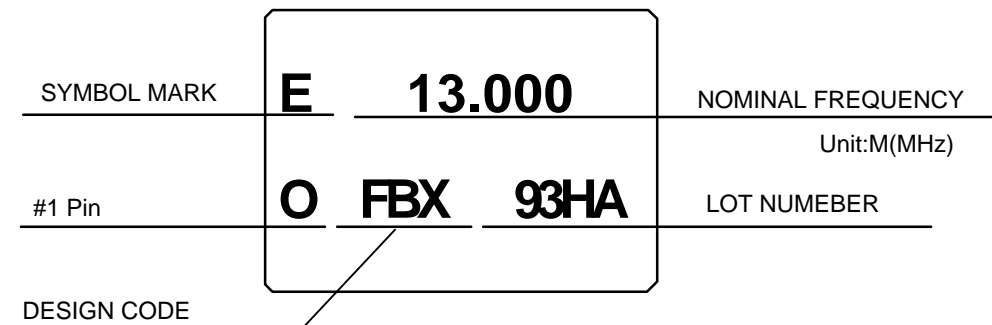
Pin No.	Name
#1	Vc
#2	GND
#3	OUT
#4	VDD



T1-T6 : Test pin. Please do not connect.



Terminal Treatment : Au Plating
Unit : mm

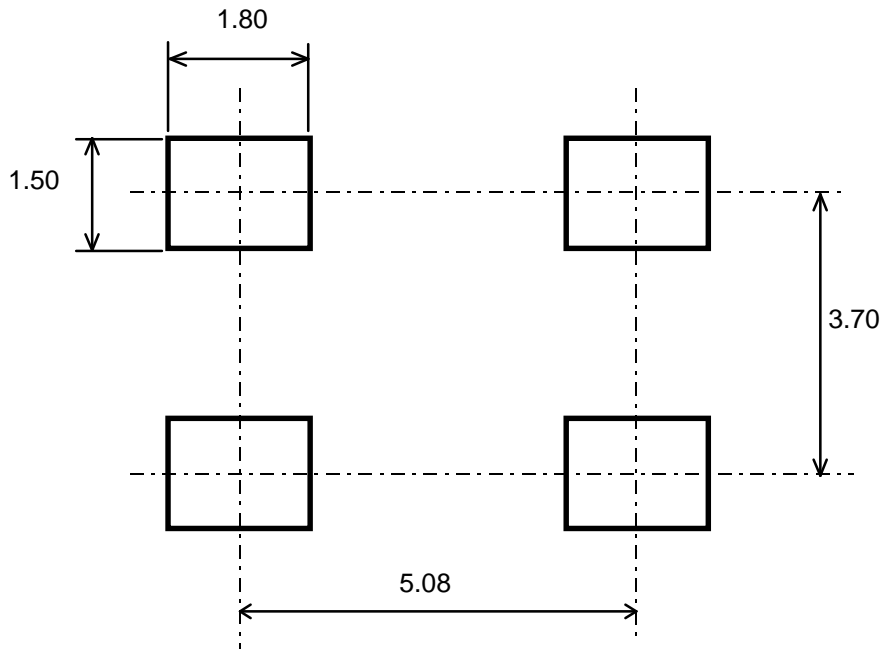


[9] Recommendable patterning

Following is only design example. For actual design work, please consider optimum condition together with mounting density, reliability of soldering and mountability etc.

Soldering position

Unit : mm



[10] Note

1 Static discharge

This device is made with IC. Please take precautions to prevent damage against electrical static discharge.

2 Power fluctuations

We recommend placing a 0.1 μ F capacitor between VDD and GND to obtain stable operation and protect against power line ripple.

VDD and GND pattern shall be biggest as possible

3 Output line

As a long output line may cause irregular output, please take care to design that output line is as short as possible, and also keeps high level signal source away from this device.

4 Shock reliability

This device contains a quartz crystal, so please do not give too much shock or vibration.

We recommend to store device under normal temperature and humidity to keep the specification.

5 Automatic insertion

An automatic insertion is available, however, the internal quartz crystal might be damaged in case that too much shock or vibration is given by machine condition. Be sure to check your machine conditioning in advance.

6 Ultrasonic cleaning

Ultrasonic cleaners can be used on the VG-2620JD, however, since the oscillator might be damaged under some conditions, please exercise in advance.

7 Humidity

When the VG-2620JD is used in high humidity applications, there is a potential problem with condensation. As with other IC's, please take precautions to prevent condensation.

8 Vibration

When some vibration or periodic mechanical shock will be added from piezoelectric sounder , piezoelectric buzzer and from like that to the oscillator , the phenomena such as a frequency drift or swing level change may exist during the time facing such vibration.

Of cause our oscillator has designed to minimize such problems, however please take care to design the layout as follows to avoid such problems.

(1) To mount a sounder or vibrator on the separated circuit board.

(2) When mounted on a same circuit board, to keep the distance as far as possible between a oscillator and vibrator to put some cushion between a vibrator and a circuit board to put some slit on the portion between a vibrator and a oscillator

(3) When you want to proceed a electrical test, it is advised that the circuit should be enclosed in a enclosure because the vibration affects will be changed from the result of a circuit board itself